

GEOMETRIC AND FREQUENCY SCALABLE TRANSISTOR BEHAVIOURAL MODEL FOR MMIC DESIGN

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ABSTRACT

This thesis presents research in developing and validating scaling in terms of geometry and frequency for Behavioural models in order to extend their functionality. Geometric and frequency scalability, once thought to be limited only to Physical and Compact models, greatly reduces the number of measurements for model generation. Besides saving precious time and effort, measurements do not need to be collected at high frequency or power levels, reducing the cost of purchasing measurement hardware.

Scaling in terms of geometry is achieved by combining accurate measurement based non-linear look-up table models of a reference (smaller) transistor with the appropriate passive embedding networks. Experimental results show that the scalable model is successful in predicting the performance of devices up to 5 times larger in gate periphery on two separate Gallium Nitride wafers, one measured at 5 GHz and another at 9 GHz. This approach provides a robust utilization of Behavioural models by providing performance predictions at power levels beyond the limitations of high frequency measurement systems.

The geometric scalable Behavioural model was also used in a CAD environment to help create a prototype single cell MMIC amplifier for operation at 5 GHz. Although the targeted performance was not achieved due to mismatch, the non-linear Behavioural model is still able to predict the performance of the actual fabricated circuit.

The work in this thesis also introduces the first formulation and approach that enables Behavioural models to be frequency scalable. The experimental results

on HFETs from 2 different Gallium Nitride wafers measured from 2 GHz to 8 GHz (2 octaves), support theoretical analysis that frequency domain Behavioural models defined in the admittance domain have frequency scalable coefficients. Load-pull results show that the model can accurately predict non-linear behaviour at frequencies that were not used during the model extraction process.

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LIST OF ABBREVIATIONS

1. ACPR - Adjacent Channel Power Ratio
2. ADC - Analogue to Digital Converter
3. ADS - Advanced Design System
4. AM - Analogue Modulation
5. CAD - Computer Aided Design
6. DAC - Data Access Component
7. DC - Direct Current
8. DHBT - Double Heterojunction Bipolar Transistor
9. DRC - Design Rule Check
10. DSP - Digital Signal Processing
11. DUT - Device Under Test
12. DWLU - Direct Waveform Look-up
13. EM - Electromagnetic
14. FBH - Ferdinand Braun Institut
15. FDD - Frequency-Domain Defined Device
16. FET - Field Effect Transistor
17. FFT - Fast Fourier Transform
18. GaAs - Gallium Arsenide
19. GaN - Gallium Nitride
20. GBIP - General Purpose Interface Bus
21. GSM - Global System for Mobile Communications
22. HBT - Heterojunction Bipolar Transistor
23. HEMT - High Electron Mobility Transistor
24. HFET - Heterojunction Field Effect Transistor
25. HICUM - High Current Model
26. IF - Intermediate Frequency
27. InP - Indium Phosphide
28. IPD - Integrated Passive Design
29. LDMOS - Laterally Diffused Metal Oxide Semiconductor
30. LMS - Least Mean Square

- 31. LO - Local Oscillator
- 32. LSNA - Large Signal Network Analyser
- 33. LUT - Look-up Table
- 34. LVS - Layout Versus Schematic
- 35. MDIF - Microwave Data Interface Files
- 36. MESFET - Metal Semiconductor Field Effect Transistor
- 37. MEXTRAM - Most Exquisite Transistor Model
- 38. MMIC - Monolithic Microwave Integrated Circuit
- 39. MTA - Microwave Transition Analyser
- 40. NVNA - Non-linear Vector Network Analyser
- 41. NMDG - Network Measurement and Description Group
- 42. NMSE - Normalised Mean Square Error
- 43. PA - Power Amplifier
- 44. PAE - Power Added Efficiency
- 45. PDK - Process Design Kit
- 46. PHD - Polyharmonic Distortion
- 47. pHEMT - pseudomorphic High Electron Mobility Transistor
- 48. PM - Phase Modulation
- 49. PNA-X - Performance Network Analyzer (X-Parameter option)
- 50. RF - Radio Frequency
- 51. Si - Silicon
- 52. SiC - Silicon Carbide
- 53. SiGe - Silicon Germanium
- 54. SPICE - Simulation Program with Integrated Circuit Emphasis
- 55. UCSD - University California San Diego
- 56. UHF - Ultra High Frequency
- 57. VBIC - Vertical Bipolar Inter-Company Model
- 58. VCO - Voltage Controlled Oscillator
- 59. VEE - Visual Engineering Environment
- 60. VIOMAP - Volterra Input Output Map
- 61. VNA - Vector Network Analyser

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CHAPTER 1

INTRODUCTION

The invention of the transistor by John Bardeen, Walter Brattain and William Shockley in 1947 revolutionised the world of electronics by replacing bulky vacuum tubes and mechanical relays [1]. Over the years, development and advancement in semiconductor growth and processing has led to the development of Monolithic Microwave Integrated Circuits (MMICs) capable of operating at microwave frequencies. These circuits perform functions such as mixing, switching or power amplification that are vital to any modern day radio frequency (RF) communication system.

In this day and age, it is hard to imagine a world without satellites, base stations and mobile phones as they have been become ubiquitous and crucial to our daily lives. Consumers have now come to expect ever increasing data and download speeds at a lower cost [2]. All this places a burden on designers to produce MMICs that meet the tight specifications of bandwidth, power and linearity set by the market's growing demands. Accurate models for use within Computer Aided Design (CAD) software are key to the successful design of these circuits [3].

However, it remains a challenge to use large-signal measurement hardware to generate models for non-linear simulations. There exist trade-offs between model accuracy and the time it takes for model generation [4]. Recently, with the introduction of the Polyharmonic Distortion Model [3], [5]-[6] (a type of Behavioural model) along with non-linear vector analysers (NVNAs) such as

the PNA-X, a possible solution to this conundrum is emerging. Nevertheless, those Behavioural models extracted directly from such measurements have been criticised as being unable to scale and perform poorly under stimulus where measurements have not been performed [7]-[9].

Therefore, the work in this thesis seeks to investigate the scalability of such Behavioural models in order to improve their functionality. This chapter starts off with a discussion on microwave circuit design and transistor characterisation, followed by an overview of the various types of transistor models, the thesis objectives and finally with a summary of the upcoming chapters.

1.1 RF / Microwave Circuit Design

Circuit design is a challenging process with many stages. As RF circuits become more complex, the need for CAD programs arises in order to allow complex simulations to be performed. One of the first electronic circuit simulator is SPICE (Simulation Program with Integrated Circuit Emphasis), developed by Laurence Nagel at the University of California, Berkeley [10]. Over the years, CAD programs have been improved upon and for RF circuits, the two major software tools commonly used for simulations are Keysight's Advanced Design System (ADS) [11] and National Instrument's Microwave Office [12].

A typical design flow is presented in Fig. 1-1. Firstly, target specifications for the design are defined. For example, in the case of a power amplifier (PA), this includes input and output return loss, gain, output power, efficiency and linearity across a specified bandwidth of operation. Before any design can

take place within the CAD environment, the circuit elements need to be characterised and accurate models produced.

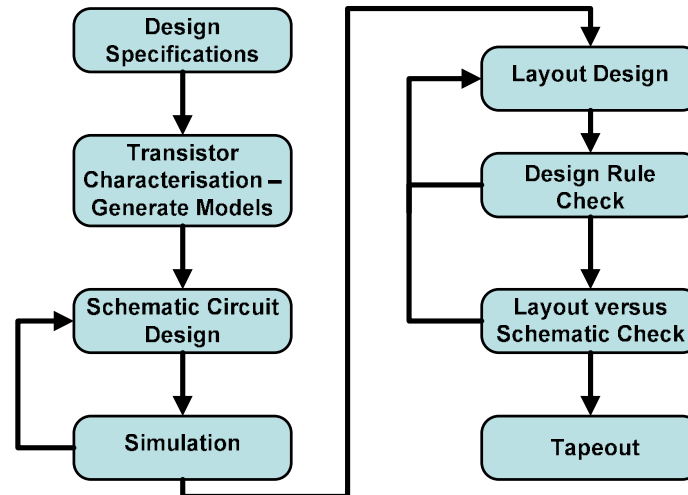


Figure 1-1: Design flow for Monolithic Microwave Integrated Circuits.

More effort and emphasis is placed on modelling the active device (such as the transistor) due to its non-linear behaviour. These transistors are often subjected to rigorous testing such as pulsed DCIVs, multi bias S-parameters and source and load-pull measurements in order to fully characterize its performance.

For a given semiconductor process, the models and associated layouts of circuit elements are made available within Process Design Kits (PDK) supplied by the foundry. It is imperative that these models produce precise results as inaccurate simulations lead to poor designs and increased design time [3].

At the schematic level, circuit design typically involves synthesizing matching circuits and optimizing component values to meet design specifications. This is followed by conversion into a layout (physical design). Design rule checks (DRC) are made to ensure that process rules are not violated and a

comparison of the layout with the schematic (LVS) ensures that both are in agreement prior to submission to a foundry for fabrication.

1.2 Transistor Characterisation

Measurements normally performed on a transistor can be either DC, small or large signal RF measurements. DC measurements of the transistor produces the current-voltage relationships and can be done under pulsed or continuous excitations [13]. Continuous DC measurements are widely used to characterise small periphery transistors since only a small amount of current flows when capturing the voltage and current characteristics. For large transistors, pulsed DC measurements are preferred since a significant amount of self-heating occurs, that can pose a risk of possible destruction or damage to the device under test.

Small-signal RF measurements (S-parameters) can be performed with Vector Network Analysers (VNAs) and these measurements give the differential performance of a transistor under linear conditions where the superposition principle holds. It is the most common way to provide a linear description of its equivalent circuit behaviour, hence its frequency response. Just like with DC measurements, pulsed S-parameters are performed to extract isothermal model parameters though it has a drawback of having a drastic reduction in measurement dynamic range [13].

Large-signal RF measurements are performed on a device where the superpositioning theorem is no longer supported [14]. This typically involves measuring the voltage and current at frequencies other than the stimulus frequency and often when the device is driven into compression.

1.3 Large Signal Modelling

The aim of any modelling technique is to provide a mathematical description in order to accurately predict the performance of a device under real stimulus. Large signal models can be subdivided into 3 main types: Physical, Compact, and Behavioural. A relative comparison between the 3 model types is illustrated in Fig. 1-2 and extracted based on data in [7].

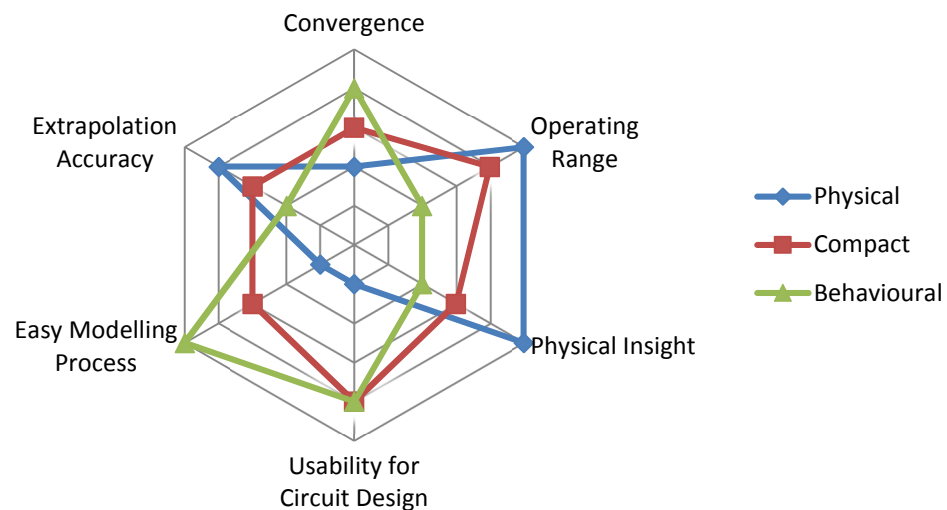


Figure 1-2: Relative comparison between Physical, Compact and Behavioural models [7].

1.3.1 Physical Models

Physical models use equations to describe the physics of the device technology such as topography and the material properties of the transistor [15]-[16]. In Physical modelling, the nonlinear partial differential equation that describes charge distribution, transport, continuity in the transistor structure are solved using finite difference [17] or finite element [18] methods. As shown in Fig. 1-2, although it can be used over a large operating range, simulations using Physical models are memory intensive and time consuming, making it less

suited for circuit design [13]. These are commonly used in process design instead.

1.3.2 Compact Models

Compact models are defined in terms of I-Q as a function of V and are typically extracted from pulsed IV and pulsed S-parameter measurements with validation from load-pull data [7]. Generally, Compact models are equivalent circuit representations of the transistor and are commonly used in the CAD simulators since they do not suffer from the computational overhead of Physical models [13]. Their advantages include being able to work in all simulation modes (including transient analysis, harmonic balance and complex envelope) and can capture complex phenomena such as electro-thermal and trapping effects. However, compared to Behavioural models, most Compact models are technology dependent and involve a longer and more difficult extraction process [19]-[20].

The two main FET Compact models are the Curtice [21] and Angelov [22] models. In 1980, W.R. Curtice developed a circuit model for GaAs MESFETs which accurately describes the drain current control characteristics, transit-time effects, gate capacitance and circuit parasitics. The Angelov model, suitable for HEMTs and MESFETs, is capable of describing the current-voltage characteristics and its derivatives which include the transconductance peak, gate-source and gate drain capacitances. Both Curtice and Angelov models have been extended in the literature for better performance [23]-[24]. Other examples of Compact models for FETs include the Materka [25] and Statz model [26].

For HBTs, Compact models such as the VBIC [27], MEXTRAM [28] and HICUM [29] were initially developed for silicon and SiGe devices. On the other hand, the UCSD [30], Agilent [31] and Ferdinand Braun Institut (FBH) [32] HBT models were created specifically for III-V materials. Nevertheless, all HBT Compact models can all be traced back to the model first developed by Gummel and Poon [33].

Besides implementation using analytical equations [21]-[33], Compact models can also be implemented using look-up tables (LUT) [4], [34]-[36]. LUT models consists of a large number of measurements which are referenced to independent variables such as bias, frequency and input drive. A popular example is the Root Model [34], developed initially for the GaAs HFETs. Due to its nature, LUT model accuracy depends on the density of measurements and the interpolation capabilities of the simulator. Therefore, this approach will be hampered by the need for a large number of data points, leading to increased measurement time, file size and possible interpolation of noise [4].

1.3.3 Behavioural Models

Behavioural models are considered "black-boxes" since no a priori knowledge of the internal circuitry is necessary for modelling purposes. These models relate the responses of the DUT to some stimuli based on mathematical functions [3], [37]-[42]. They were developed to address the shortcomings of Compact models (shown in Fig. 1-2), namely a lengthy and more difficult extraction process and being technology dependent.

Among the three model classifications, Behavioural models can be generated in the least amount of time, making it especially useful when it comes to

characterizing new technologies or processes for PA design. In addition, extraction of the model is relatively easy compared to Physical or Compact models and grants an alternative for MMIC designers to extract their own models instead of depending on those provided by the foundry.

Behavioural models provide complete protection of IP and the model can be passed on to third parties without any fear of leaking sensitive data. They are also often more accurate than Compact models within its characterization range and offer better convergence in the simulator [20]. Furthermore, Behavioural models provide a higher level of abstraction and can be generated for packaged parts or from an integrated circuit as a whole.

The main implementations of Behavioural models used in the industry are the Keysight X-parameters [5]-[6] and the Cardiff Model [39]-[40]. Other examples of Behavioural models include the Volterra Input Output Map (VIOMAP) [41]-[42], Hot S-parameters [43]-[44], S-functions [45] and the Padé Approximation Based Behavioral Model [46].

Nevertheless, unlike Compact models, Behavioural models are considered to be unable to scale and perform poorly outside the range of measurements from which they were extracted [7]-[9]. In other words, Behavioural models are considered to be less functional compared to Compact models.

1.4 Thesis Objectives

The central issue in modelling an RF power transistor has always been scaling. Detailed modelling are often carried out on a smaller nominal device and different to the ones being used [4], [14].

A commonly held belief in the microwave community is that Behavioural models are not scalable [7]-[9]. Although they are quick and easy to generate, if multiple dimensions such as transistor geometry size, bias, power level, frequency of operation and temperature are required, the number of device measurements that will need to be performed will increase exponentially. This places a huge burden on measurement time and hardware availability. Therefore, efforts must be made to improve the functionality of Behavioural models.

X-Parameters have been proven to be geometrically scalable [47]-[48]. But so far, no work has been done to prove geometric scaling using the Cardiff Model. No publications have been made regarding frequency scalable Behavioural models (either with the X-Parameter or Cardiff Model formulation).

Therefore, the objectives of the work in this PhD are:

1. Prove that geometric scaling is possible using the Cardiff Model. This means that the model must be able to scale with the transistor's size (total gate periphery = number of gate fingers multiplied by unit gate width).
2. Develop and verify the modelling framework for implementing geometric scalable Behavioural models. An analysis of the model's capabilities and limitations will also be performed.
3. Utilize geometric scalable model as a design tool for MMIC design within the circuit simulator. A MMIC prototype will be fabricated and tested.
4. Prove that the model coefficients are frequency scalable using both X-Parameters and the Cardiff Model formulations which opens up the possibility of frequency scaling using Behavioural models.

5. Develop, verify and perform an analysis on the modelling framework for frequency scalable Behavioural models.

1.5 Chapter Synopsis

Here the summary of each upcoming chapter will be presented.

Chapter 2 provides a comprehensive literature review on the development of Behavioural modelling concept which has evolved and extended from S-parameters to X-parameters and the Cardiff Model. The formulation, extraction process and discussion of each Behavioural model is presented. This chapter also contains a review of previous work performed on obtaining scalable Behavioural models as a guide to producing novel work and extending the body of knowledge.

Chapter 3 devotes its content to the modelling process in obtaining geometric scalable Behavioural Models, achieved by integrating scalable measurement data look-up table models of a reference device within appropriate passive layout networks. Model validations were performed on 2 different Gallium Nitride (GaN) wafers up to 5 times larger in gate periphery. The model is also shown to be robust as it is able to scale beyond the measurement system's power capability. In addition, limitations of the model and steps to overcome them are also presented.

Chapter 4 focuses on the application of the geometric scalable Behavioural model for MMIC design. The model will be used in the design of a prototype single cell amplifier, optimized for operation at 5 GHz with matching circuits at the input and output. The design process and usage of the model within the circuit simulator will be presented along with modelled and measurement results.

Chapter 5 shows the first ever formulation and approach for Behavioural models to be frequency scalable. By referencing the intrinsic transistor in the admittance domain, experimental results on 2 separate GaN HFETs, measured from 2 - 8 GHz, show that Behavioural models can have frequency scalable model coefficients. Experimental results also show that they can successfully predict results at frequencies that were not used during the measurement based model extraction process.

Validations have been performed with both the X-Parameter and Cardiff Model formulations using engineered voltage stimuli and the Fast Fourier Transform (FFT) extraction concept. With the model structure verified, the model extraction was then performed using the Least Mean Square (LMS) approach to gain the ability of covering the entire measured load-pull area while avoiding dependence on a structured data format.

Finally, Chapter 6 presents the conclusions of this PhD work and possible future work to extend the capabilities of the model.

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CHAPTER 2

LITERATURE REVIEW

Models which are accurate and easy to derive are important to many areas of the industry especially in integrated circuit design. With accurate models, first pass design success can be targeted, reducing the manpower and cost of multiple prototypes. For established technologies, accurate models are available for passive and active components. However, for new emerging technologies such as GaN, models are not readily accessible [1] and most device manufacturers can only provide customers with basic SPICE type model parameters with limited accuracy.

Behavioural models mentioned in Section 1.3.3 can be extracted rapidly from carefully selected measurements. There is no need for a priori knowledge of the internal device composition and is based on a set of mathematical fitting functions. While different Behavioural models may vary in terms of complexity and computational burden, convergence on a solution is orders of magnitude faster when compared to Physical or Compact models [2].

Since the work in this thesis will focus on generating scalable Behavioural models, this chapter will first focus on the development of the Behavioural modelling concept which has evolved and extended from S-parameters, which are considered linear Behavioural models, to non-linear Behavioural models such as the VIOMAP, Hot S-parameters and the Polyharmonic Distortion model, the basis for X-parameters and the Cardiff Model.

Then the discussion will shift towards exploring the work previously performed on Behavioural models in an attempt to make them scalable. This gives an overview of previous research into this area and provides a roadmap for extending the body of knowledge.

2.1 S-parameters

S-parameters [3]-[4] were introduced because measurements to obtain Z, Y, H or ABCD parameters require that the ports be terminated in either a short or open circuits. Such terminations are difficult to achieve at RF frequencies and would also result in potential oscillations in active circuits.

The S-parameter concept uses travelling waves which do not vary in magnitude at points along a transmission line, unlike terminal voltages and currents [5]. With these advantages, S-parameters becomes the standard model of any linear circuit design due to its ability to describe the behaviour of linear systems accurately.

2.1.1 S-parameters Formulation and Extraction

The concept of travelling waves has been introduced along with S-parameters and are defined as:

$$a_i = \frac{V_i + Z_i I_i}{2\sqrt{\text{Re}(Z_i)}} \quad b_i = \frac{V_i - Z_i^* I_i}{2\sqrt{\text{Re}(Z_i)}} \quad (2-1)$$

where a is the incident and b is the reflected wave as shown in Fig. 2-1. Subscript i indicates the port index and $\text{Re}(Z_i)$ is the real part of the complex impedance Z_i .

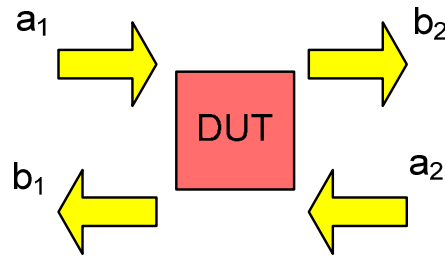


Figure 2-1: Travelling waves of a 2 port device.

For the 2-port system in Fig. 2-1, there are four S-parameters which are the ratio of the reflected travelling wave, b_i to the incident wave, a_i . These four S-parameters are the input match (S_{11}), gain / loss (S_{21}), isolation (S_{12}) and output match (S_{22}) and can be defined by:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (2-2)$$

S-parameters are not limited to only 2-port systems but can be extended to include any number of ports and harmonic as represented by equation (2-3) with i and j being the port and harmonic index respectively.

$$\begin{bmatrix} b_{ij} \\ b_{ij} \end{bmatrix} = \begin{bmatrix} S_{ij} & S_{ij} \\ S_{ij} & S_{ij} \end{bmatrix} \begin{bmatrix} a_{ij} \\ a_{ij} \end{bmatrix} \quad (2-3)$$

Over the years, network analyzers have evolved from being only able to perform scalar measurements such as the 8757D to today's state of the art PNA-X vector network analyzers [6] capable of measuring multiport S-parameters and large signal X-parameters. Nevertheless, a typical network analyser is made up of four sections [7] which are:

- a) source for stimulus
- b) signal separation device

c) receivers for detection and downconversion

d) processor and display for calculating and reviewing the results

Signal sources in a network analyser are typically open-loop voltage control oscillators (VCOs) or synthesized sweepers which provide better performance for measuring narrowband devices.

The signal separation block or "test-set" is typically made up of directional couplers. The functions performed by this block are to measure a portion of the incident signal for reference and to separate the incident and reflected signals.

Vector network analysers use a tuned receiver in order to obtain information about the magnitude and phase of the signal. A tuned receiver uses a local oscillator (LO) to downconvert an RF signal to an intermediate frequency (IF) signal. The information from the IF signal is then extracted via an analogue-to-digital converter (ADC) and digital signal processing (DSP) block.

Finally, the display and processor block allow the user to view the data in various formats such as linear and logarithmic graphs or on a Smith chart.

Based on [7], the setup for measuring S-parameters for a 2-port device is shown in Fig. 2-2. To obtain the four S-parameters, the network analyser will perform both a forward and reverse measurement. In each case, one of the ports will be injected with a small signal from a 50 ohm source while terminating the other with a reference impedance (typically 50 ohms), ensuring no reflection from the load.

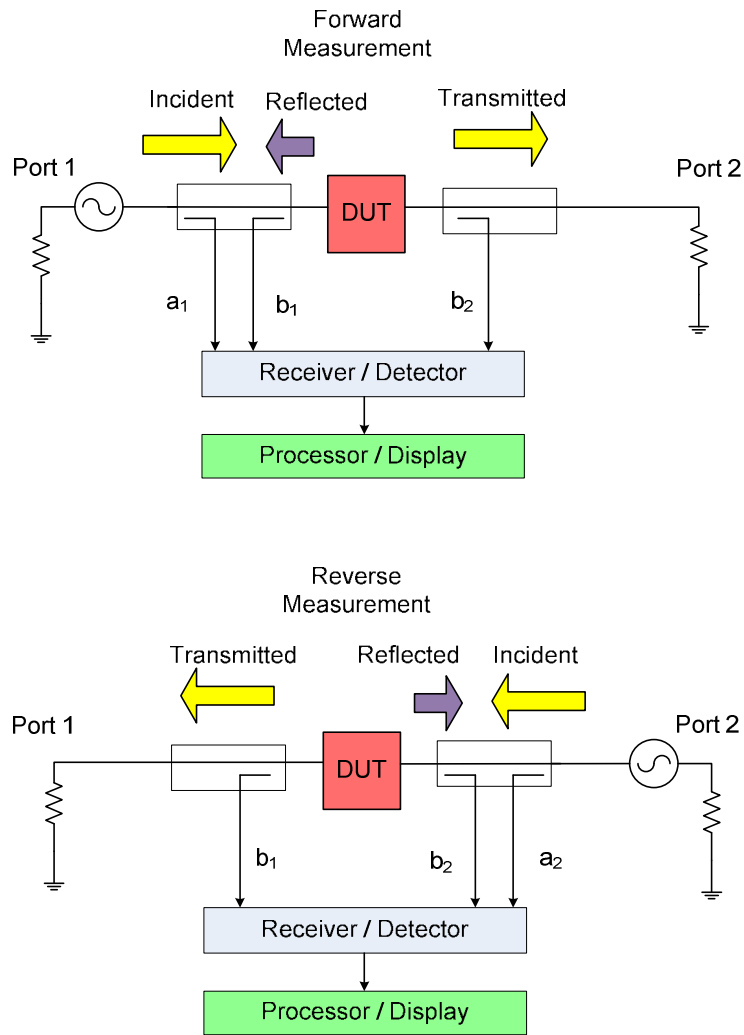


Figure 2-2: Forward and reverse measurement setup for S-parameters [7].

Using the setup in Fig 2-2, the following S-parameters can be obtained. For forward measurements:

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} \quad S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \quad (2-4)$$

For reverse measurements:

$$S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \quad S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} \quad (2-5)$$

2.1.2 S-parameters Discussion

S-parameters form a complete Behavioural model of the DUT operating under linear conditions, providing a very accurate representation of the circuit [8]. In addition, its measurements are repeatable and independent of the measurement system. S-parameters can also be easily cascaded and imported into CAD programs such as ADS and Microwave Office. All these advantages have made it the industry standard for any linear circuit design [9].

However, under large-signal operation, active devices tend to generate harmonics, AM-to-AM or AM-to-PM distortion and spectral regrowth. These characteristics cannot be captured by S-parameters since it is formulated with the assumption that the stimulus is a small signal with the system behaving in a linear fashion.

Attempts have been made by researchers to apply "Large signal" S-parameters to the design of RF amplifiers at the UHF band [10]-[11]. However, these were of limited success especially in Class C operation where the non-linearity is severe. The results concluded that the S-parameters are a function of its operating conditions. Hence, it is valid only at the drive and bias in which measurements were performed.

Therefore, steps have been taken by the modelling community to further develop Behavioural models in order to accurately describe the performance of non-linear systems by going beyond S-parameters.

2.2 VIOMAP

VIOMAP stands for Volterra Input Output Map and is an extension of S-parameters for weakly nonlinear RF and microwave devices [13]. It is based on

the Volterra theory pioneered by Italian mathematician Vito Volterra and applied to systems engineering by Norbert Wiener [12]. The Volterra theory uses kernels which are basically the nonlinear transfer functions to describe nonlinear phenomena such as feedback and memory effects.

Previous work has shown that VIOMAPs are able to predict the behaviour of cascaded non-linear two ports [13], predict the load impedance curves on the Smith Chart [14] and enhance the linearity of digital communication channels [15].

2.2.1 VIOMAP Formulation and Extraction

The concept of VIOMAP as an extension from linear S-parameters can be explained using Fig. 2-3 which shows the equivalence between a physical two port device and its system representation [13]. Incident waves become input signals and reflected waves become output signals.

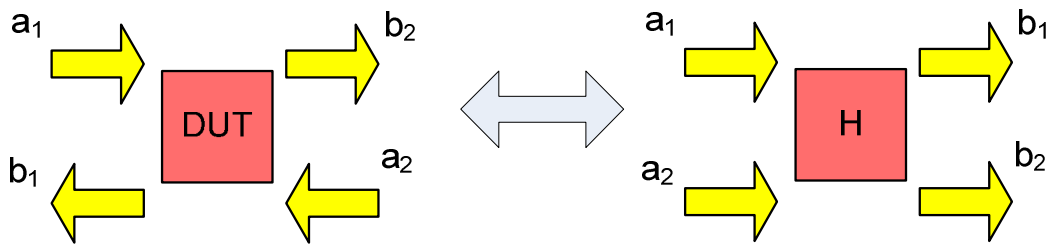


Figure 2-3: A two port device and its system equivalence [13]

S-parameters of the DUT can be expressed as

$$b_1(1) = S_{11}(1)a_1(1) + S_{12}(1)a_2(1) \quad b_1(3) = 0 \quad (2-6)$$

$$b_2(1) = S_{21}(1)a_1(1) + S_{22}(1)a_2(1) \quad b_2(3) = 0 \quad (2-7)$$

For simplification purposes, all frequencies will be expressed relative to frequency f_0 , with $f_0 = 1$ and $3f_0 = 3$.

The VIOMAP kernel $H_{n,j_i i_2 \dots i_n}(f_1, f_2 \dots f_n)$ describes the contribution of the n -th degree of nonlinearity of system H , combining the frequencies f_k at input terminal i_k into the frequency component $f_1+f_2+\dots+f_n$ of the output signal at the output terminal j . The VIOMAP containing third order non-linearity is generated based on the Volterra theory [12] and is shown in equations (2-8) and (2-9).

$$\begin{aligned}
b_1(1) = & H_{1,11}(1)a_1(1) + H_{1,12}(1)a_2(1) \\
& + 3H_{3,1111}(1,1,-1)a_1(1)a_1(1)a_1(-1) \\
& + 3H_{3,1112}(1,1,-1)a_1(1)a_1(1)a_2(-1) \\
& + 6H_{3,1112}(1,-1,1)a_1(1)a_1(-1)a_2(1) \\
& + 6H_{3,1122}(1,1,-1)a_1(1)a_2(1)a_2(-1) \\
& + 3H_{3,1122}(-1,1,1)a_1(-1)a_2(1)a_1(1) \\
& + 3H_{3,1222}(1,1,-1)a_2(1)a_2(1)a_2(-1)
\end{aligned} \tag{2-8}$$

$$\begin{aligned}
b_1(3) = & H_{3,1111}(1,1,1)a_1(1)a_1(1)a_1(1) \\
& + 3H_{3,1112}(1,1,1)a_1(1)a_1(1)a_2(1) \\
& + 3H_{3,1122}(1,1,1)a_1(1)a_2(1)a_2(1) \\
& + H_{3,1222}(1,1,1)a_2(1)a_2(1)a_2(1)
\end{aligned} \tag{2-9}$$

In the case of a purely linear device, the third-order kernels are zero, such that

$$b_1(1) = H_{1,11}(1)a_1(1) + H_{1,12}(1)a_2(1) \quad b_1(3) = 0 \tag{2-10}$$

Comparing (2-10) with (2-6) and (2-7), it is clear that for a linear device, the first-order VIOMAP kernel $H_{1,ij}(f)$ is the S-parameters $S_{ij}(f)$.

To determine the VIOMAP of a two port device, the DUT has to be excited with a set of states similar to the situation where it will be used. The setup in Fig. 2-4 measures the incident waves $a_1(t)$, $a_2(t)$ and the reflected waves $b_1(t)$, $b_2(t)$ at the DUT based on a modified HP70820A Microwave Transition Analyser.

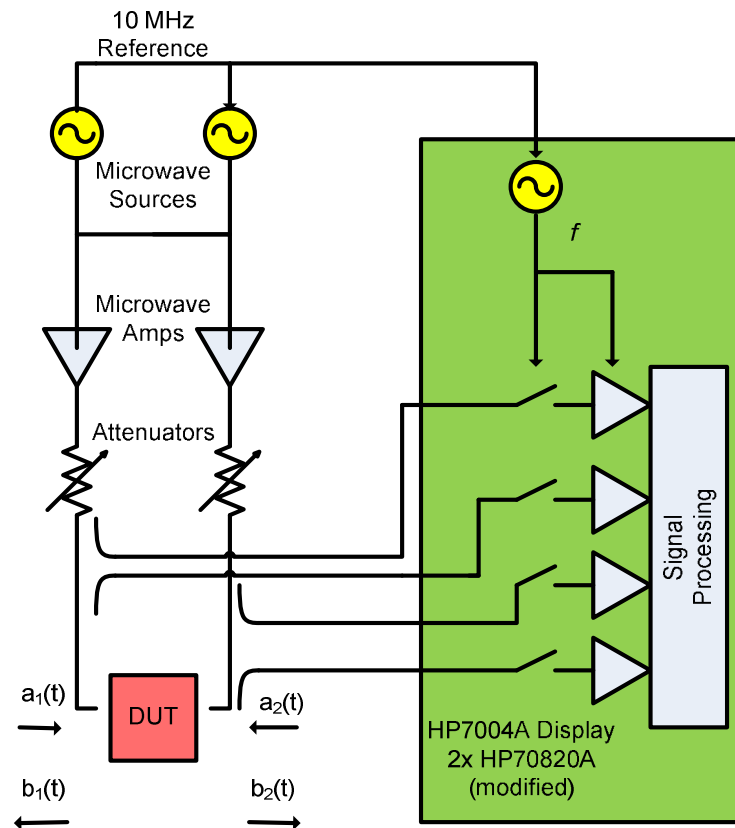


Figure 2-4: The block diagram of the measurement setup for fundamental load-pull and VIOMAP determination [13].

This modification is necessary to synchronize two MTAs with each other to obtain a four channel phase coherent measurement. Two sources are combined to excite the DUT at two different frequencies simultaneously at both port 1 and port 2. The excitation at port 2 emulates the effect of the device being terminated with a mismatch causing reflection of the incident power.

2.2.2 VIOMAP Discussion

Although the VIOMAP solution is indeed promising, identifying VIOMAP kernels is a difficult process, making it impractical for design. Being a series approximation, Volterra theory is only suited to model weak nonlinear devices [16]. Using the orthogonal polynomial approach as its alternative requires an overly complicated computation instead. In order to accurately describe hard nonlinear behaviour, the modelling community has been actively seeking out other methods which ultimately led to the "Describing Function" framework and the Polyharmonic Distortion modelling approach [17].

2.3 Hot S-parameters

Just like S-parameters, Hot S-parameters can characterize how a device under test (DUT) behaves by describing the relationship between B_2 and A_2 travelling voltage waves. However, under large signal input excitation, the DUT (normally a transistor) will start to behave in a non-linear fashion and classical S-parameters which is based on the superposition principle, no longer holds true. Hot S-parameters differs from S-parameters by being valid even at large input drive levels [18].

2.3.1 Hot S-parameter Formulation and Extraction

In 1978, Mazumder et al. [19] proposed the simultaneous application of two signals of the same frequency to accurately determine large signal S_{12} and S_{22} . Since then, many research attempts have been made to extend S-parameters into the large signal domain [18]-[26]. The research done in [26] summarizes how Hot S-parameters can be applied to solve two major power amplifier

design problems: investigate stability and predict distortions under hot operating conditions.

2.3.1.1 Hot S-parameters for Stability Analysis

Using Hot S-parameters to investigate stability is discussed in [20]-[22]. The key is performing the measurements when the DUT is under actual operating conditions by applying a large signal tone to port 1. While this signal is being injected, a small probe tone is added to either to port 1 (during the forward measurement) or port 2 (during the reverse measurement).

Fig. 2-5 and 2-6 illustrates the incident A waves and reflected B waves during the forward and reverse measurements respectively. The large signal carrier is at frequency f_c while f_s is the frequency at which Hot S-parameters are measured.

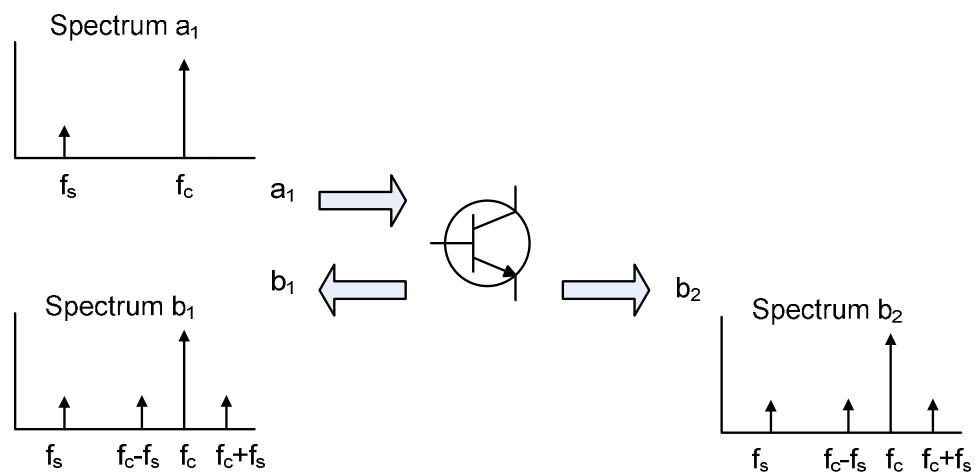


Figure 2-5: Stability Hot S-parameter forward measurement A and B spectra [26].

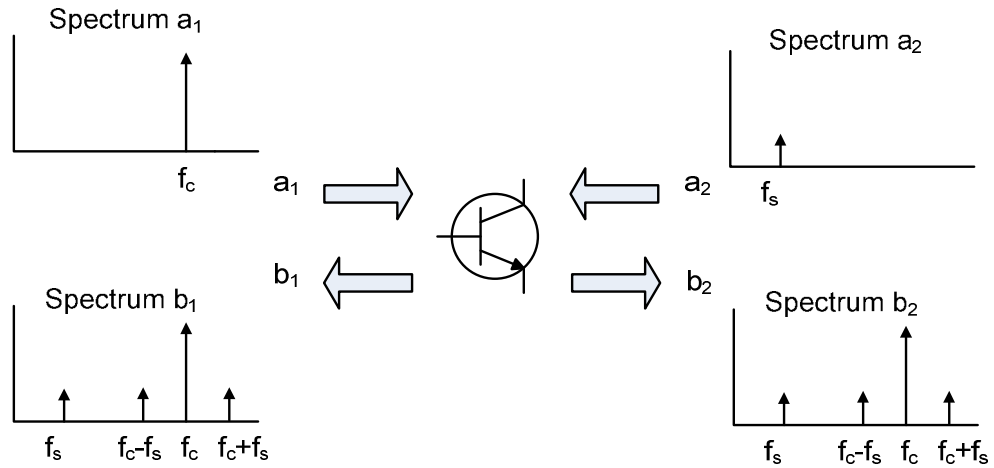


Figure 2-6: Stability Hot S-parameter reverse measurement A and B spectra [26].

The Hot S-parameters are defined as ratios between B waves and A waves, identical to Classical S-parameters, shown in equation (2-11). Stability analysis can now be performed using either the Rollet's or Edwards theory on stability in [27]-[28].

$$\begin{bmatrix} b_1(f_s) \\ b_2(f_s) \end{bmatrix} = \begin{bmatrix} hotS_{11} & hotS_{12} \\ hotS_{21} & hotS_{22} \end{bmatrix} \begin{bmatrix} a_1(f_s) \\ a_2(f_s) \end{bmatrix} \quad (2-11)$$

Note from Fig. 2-5 and 2-6 that mixing products are present but can be neglected as stated in [21] due to f_s being much lower than f_c . The assumption is that the interaction between the tones at f_s is much stronger compared to the interaction between all other tones near the fundamental and harmonics of f_c , thus keeping the stability analysis accurate.

The setup for stability measurements of Hot S-parameters is based on load-pull architecture and shown in Fig. 2-7 [21]. Hot S-parameters measurements are obtained with a large signal tone at frequency f_c and a small probe tone f_s applied to either the input or output port via a switch. Two different VNAs are

used for measurements of f_c and f_s respectively to solve the dynamic range issues due to the power level difference between f_c and f_s .

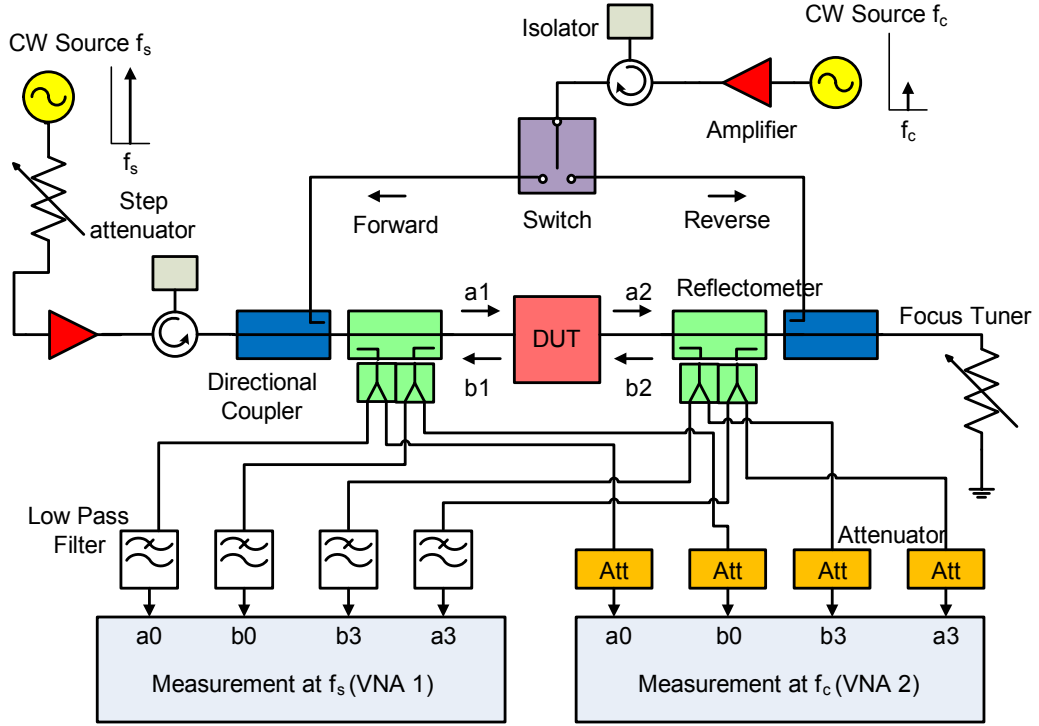


Figure 2-7: Stability Hot S-parameter Measurement Setup [21].

2.3.1.2 Hot S-parameters for Distortion Analysis

The application of Hot S-parameters to predict distortions is examined in [18],[23]-[26]. To predict distortions of the DUT, the incident A-waves and reflected B-waves are described by equation (2-12), where the Hot S-parameters are a function of both the amplitude and the frequency of the large signal $a_1(f_c)$.

$$\begin{bmatrix} b_1(f_c) \\ b_2(f_c) \end{bmatrix} = \begin{bmatrix} hotS_{11} & hotS_{12} \\ hotS_{21} & hotS_{22} \end{bmatrix} \begin{bmatrix} a_1(f_c) \\ a_2(f_c) \end{bmatrix} \quad (2-12)$$

Although very similar to equation (2-11), the above equation is different since it is nonlinear in the incident wave $a_1(f_c)$. Therefore, the Hot S-parameter of

this equation can accurately describe the non-linear transmission characteristics of a DUT and is known as Simple Hot S-parameters.

The work in [18] and [23] explains that inaccurate results may be obtained for describing the Hot S_{22} and Hot S_{12} with equation (2-12) because it lacks the conjugate $a_2(f_c)$ tone. An extension of Hot S-parameters can be described in equation (2-13).

$$\begin{bmatrix} b_1(f_c) \\ b_2(f_c) \end{bmatrix} = \begin{bmatrix} hotS_{11} & hotS_{12} \\ hotS_{21} & hotS_{22} \end{bmatrix} \begin{bmatrix} a_1(f_c) \\ a_2(f_c) \end{bmatrix} + \begin{bmatrix} T_{12} \\ T_{22} \end{bmatrix} e^{j2\phi(a_1(f_c))} conj((a_2(f_c))) \quad (2-13)$$

Delving further into the work done in [18], it is shown that the conjugate terms helps improve the accuracy of the Simple Hot S-parameters by accounting for the dependency on the phase of A_2 .

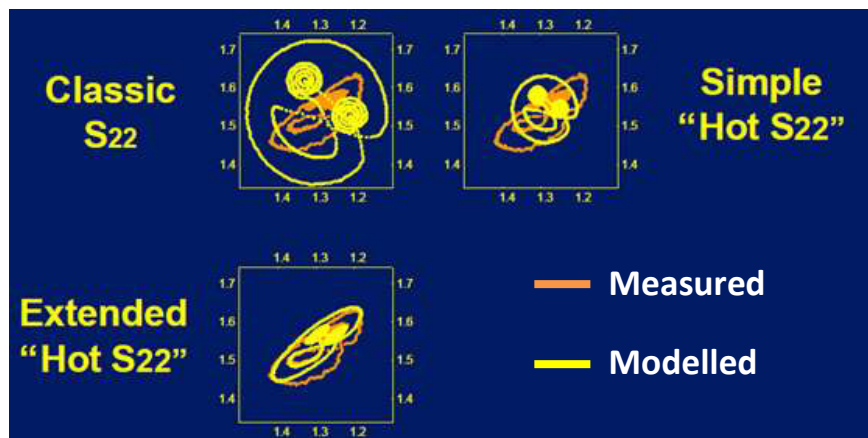


Figure 2-8: Comparison between measured B_2P^{-1} (at highest A_1 amplitude) and modelled B_2P^{-1} with Classic S_{22} , Simple Hot S_{22} and Extended Hot S_{22} equations [18].

Fig. 2-8 shows the orange and yellow "smileys" which are the measured and modelled results of the B_2 waves respectively after phase normalization has occurred, hence becoming B_2P^{-1} . The complex phasor P has the phase equal to the phase of A_1 .

$$B_2 = S_{21}(|A_1|).A_1 + S_{22}A_2 \quad (2-14)$$

Classical S_{22} as defined in equation (2-14) is not capable of describing the relationship between the A_2 and B_2 when it is a clearly a function of A_1 . This is expected since Classical S-parameters, defined in Section 2.1, is not valid during the non-linear operation of a transistor.

$$B_2 = S_{21}(|A_1|).A_1 + S_{22}(|A_1|).A_2 \quad (2-15)$$

Simple Hot S-parameters (defined in equation (2-15)) makes S_{22} a function of the amplitude of A_1 . However, at a large drive level, the squeezing effect does not occur for the model and implies that the phase of A_2P^{-1} is important.

$$B_2 = S_{21}(|A_1|).A_1 + S_{22}(|A_1|).A_2 + T_{22}(|A_1|).P^2.conj(A_2) \quad (2-16)$$

Therefore, a different coefficient is needed for the real and imaginary part of A_2P^{-1} . In fact, A_2P^{-1} and its conjugate is required to model the data accurately, leading to the extended version of Hot S-parameters, as defined by equation (2-16).

An example of a setup to obtain results for distortion characteristics is shown in Fig. 2-9. It is based on the work in [18], where a Large Signal Network Analyser (LSNA) is attached to 2 synthesizers, one for each port. Synthesizer 1 generates the large signal input, A_1 , ensuring that all measurements are performed under "hot" conditions. Synthesizer 2 generates a set of A_2 that are independent from A_1 .

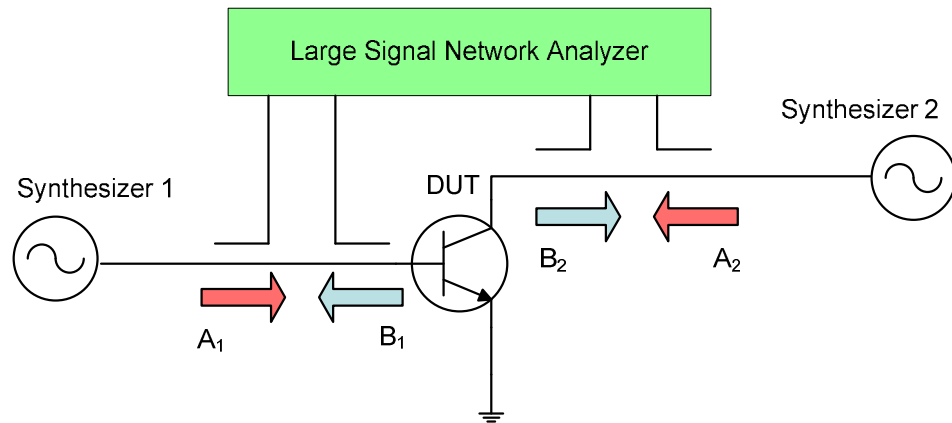


Figure 2-9: Distortion Hot S-parameters Measurement Setup [18].

Using a tuner is also possible though a synthesizer allows active load-pull through emulation of load impedances. Using a LSNA as opposed to a simple network analyser allows the measurements of all the travelling waves (A_1 , A_2 , B_1 and B_2). These quantities can then be used to calculate the Hot S-parameters by using either equation (2-12) or (2-13).

2.3.2 Hot S-parameter Discussion

The Hot S-parameter concept was developed in an attempt extend the capabilities of S-parameters by making Behavioural models capture non-linear characteristics. Its application focused on two main areas which are stability and distortion analysis. Thus, measurement setup will vary accordingly depending on its application.

For stability analysis, note that the B waves in Fig. 2-5 and 2-6 contain tones at the sum (f_c+f_s) and difference frequency (f_c-f_s). In fact, according to [21], there are more tones such as at ($L.f_c+f_s$) and ($L.f_c-f_s$) with L being any positive integer due to the mixing between the probe tone f_s and the fundamental and harmonics of the carrier, f_c .

A problem with this approach occurs when probe frequency f_s is not significantly lower than carrier frequency f_c . For example, if $f_s = f_c/2$, the difference of $(f_c - f_s)$ will result in a mixing product appearing at f_s , making the stability analysis as defined in [27]-[28] invalid. Any conclusions about stability must be taken with precaution when this condition occurs.

In terms of distortion analysis, previous work by Verspect et al. [18] also showed that though Simple Hot S-parameters can capture some of the non-linearity associated with the varying amplitude in drive, the conjugate terms (Extended Hot S-parameters) must be included for greater accuracy in describing the distortion seen in experimental data.

These concepts described in this research work became the precursor to the Polyharmonic Distortion Model [29]-[32] also introduced by Verspect et al. and forms the basis for the X-parameters and the Cardiff Model formulations. Thus, the introduction of Hot S-parameters is a key step in the development of Behavioural models.

2.4 Polyharmonic Distortion Model

The Polyharmonic Distortion (PHD) framework [29]-[32] presents a black-box, frequency domain Behavioural model, generalized from the work first presented in [24] and summarized in [32]. The theory is derived from a multiharmonic linearization around a periodic steady state determined by a large single input tone. Being a "black-box" model means that no a priori knowledge of the circuit is needed for modelling purposes.

In [29], the PHD model was identified from automated measurements on a wide-band microwave IC amplifier using a NVNA [33]. The work in [30] further

improved the design approach and presents an improved algorithm for identifying the Behavioural model discussed in [29].

2.4.1 Polyharmonic Distortion Formulation

For a general frequency domain black-box modelling technique, there exist mathematical functions (denoted by F , known as describing functions) that correlate the input spectral components A_{qn} with the output spectral components, B_{pm} as shown with the following equation.

$$B_{pm} = F_{pm}(A_{11}, A_{12}, \dots, A_{21}, A_{22}, \dots, A_{qn}) \quad (2-17)$$

where q and p range from one to the number of ports whereas m and n range from zero to the highest harmonic index.

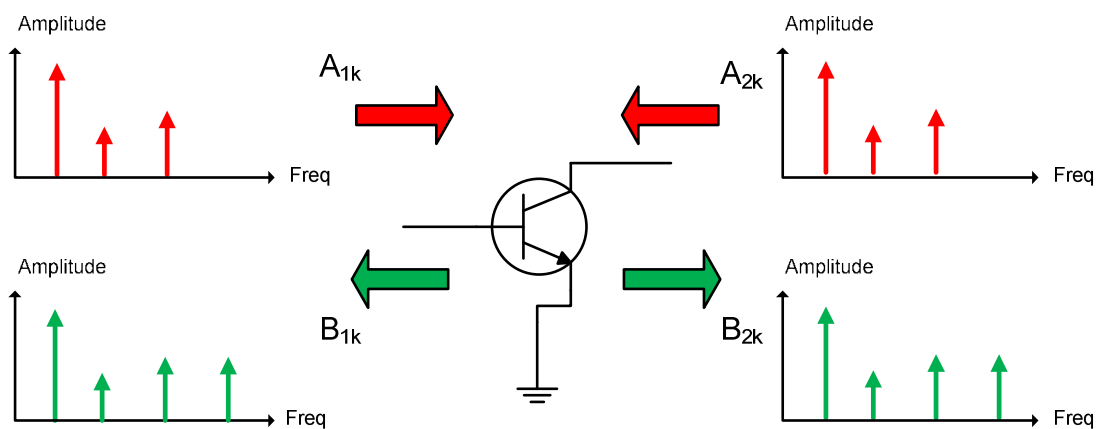


Figure 2-10: Concept of describing functions [32].

Fig. 2-10 illustrates the concept of describing functions. The PHD model is an approximation of the spectral map given by equation (2-17) and exploits 2 mathematical properties of the functions $F_{pm}(\cdot)$ which are time-invariance and nonanalyticity [35].

In a time invariant system, an arbitrary delay to the A waves causes the same time delay in the B waves. A time delay equivalent to applying a phase shift in the frequency domain and can be described by equation (2-18).

$$\forall \theta: B_{pm} e^{jm\theta} = F_{pm}(A_{11} e^{j\theta}, A_{12} e^{j\theta}, \dots, A_{21} e^{j\theta}, A_{22} e^{j\theta}, \dots) \quad (2-18)$$

In order to simplify the mathematics, it is important to use phase-normalized quantities. A component P that has the phase equal to the phase of A_{11} is shown in equation (2-19).

$$P = e^{j\varphi(A_{11})} \quad (2-19)$$

Substituting $e^{j\theta}$ with P^{-1} in (2-18) results in (2-20) which is easier to process compared to equation (2-17).

$$B_{pm} = F_{pm}(|A_{11}|, A_{12}P^{-2}, A_{13}P^{-3}, \dots, A_{21}P^{-1}, A_{22}P^{-2}, A_{23}P^{-3}, \dots)P^{+m} \quad (2-20)$$

Generally, the assumption is that the system can be strongly nonlinear towards a large signal drive but responds linearly to additional signal components at harmonic frequencies. This is known as the harmonic superposition principle and was first discovered during the measurements on a resistive FET mixer circuit [36]. It postulates that the overall deviation in the output spectrum is the superposition of all individual deviations and has been experimentally verified in [37].

Fig. 2-11 illustrates the harmonic superposition principle. When a large A_{11} is pumped into the DUT, it produces the output spectrum in B_2 . This is indicated by the black arrows. Keeping A_{11} the same and adding a small A_{12} , it causes a deviation at the 2nd harmonic for the output spectrum B_2 (represented by blue

arrows). The same applies for the third and fourth harmonic, represented by the red and green arrows respectively.

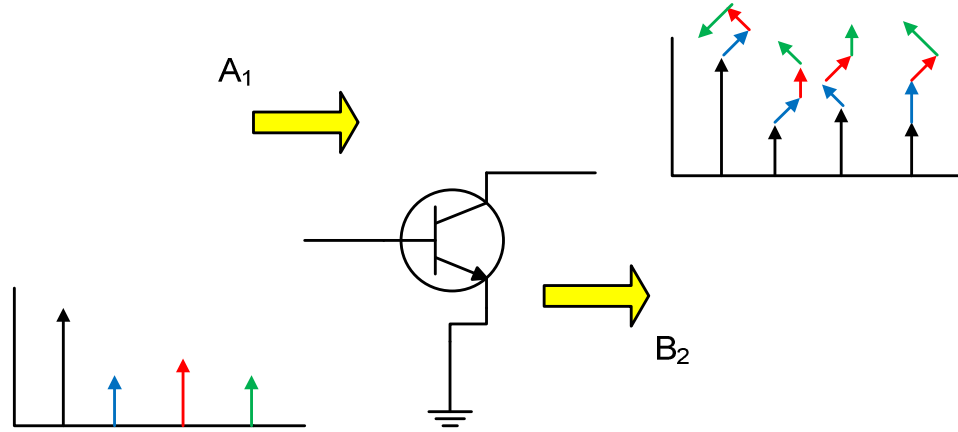


Figure 2-11: The harmonic superposition principle [32].

This principle holds true with power amplifiers of several classes and for applications where the functional block is inserted into impedance environments mismatched from 50 ohms at the fundamental and the harmonics [31]-[32]. Linearization of (2-20) versus all components except the A_{11} will result in

$$\begin{aligned}
 B_{pm} = & K_{pm}(|A_{11}|)P^{+m} \\
 & + \sum_{qn} G_{pq,mn}(|A_{11}|)P^{+m}Re(A_{qn}P^{-n}) \\
 & + \sum_{qn} H_{pq,mn}(|A_{11}|)P^{+m}Im(A_{qn}P^{-n})
 \end{aligned}
 \tag{2-21}$$

where

$$K_{pm}(|A_{11}|) = F_{pm}(|A_{11}|, 0 \dots 0)
 \tag{2-22}$$

$$G_{pq,mn}(|A_{11}|) = \left. \frac{\partial F_{pm}}{\partial \text{Re}(A_{qn}P^{-n})} \right|_{|A_{11}|,0,\dots,0} \quad (2-23)$$

$$H_{pq,mn}(|A_{11}|) = \left. \frac{\partial F_{pm}}{\partial \text{Im}(A_{qn}P^{-n})} \right|_{|A_{11}|,0,\dots,0} \quad (2-24)$$

The function $F_{pm}(\cdot)$ is nonanalytic because the real and imaginary components of the input argument can be treated as separate entities. By substituting these real and imaginary components in (2-21) with

$$\text{Re}(A_{qn}P^{-n}) = \frac{A_{qn}P^{-n} + \text{conj}(A_{qn}P^{-n})}{2} \quad (2-25)$$

$$\text{Im}(A_{qn}P^{-n}) = \frac{A_{qn}P^{-n} - \text{conj}(A_{qn}P^{-n})}{2j} \quad (2-26)$$

the following equation can be derived.

$$\begin{aligned} B_{pm} &= K_{pm}(|A_{11}|)P^{+m} \\ &+ \sum_{qn} G_{pq,mn}(|A_{11}|)P^{+m} \times \left(\frac{A_{qn}P^{-n} + \text{conj}(A_{qn}P^{-n})}{2} \right) \\ &+ \sum_{qn} H_{pq,mn}(|A_{11}|)P^{+m} \times \left(\frac{A_{qn}P^{-n} - \text{conj}(A_{qn}P^{-n})}{2j} \right) \end{aligned} \quad (2-27)$$

Rearranging the terms in (2-27) will lead to the PHD model equation shown in (2-28).

$$B_{pm} = \sum_{qn} S_{pq,mn}(|A_{11}|)P^{+m-n}A_{qn} + \sum_{qn} T_{pq,mn}(|A_{11}|)P^{+m+n}\text{conj}(A_{qn}) \quad (2-28)$$

where

$$S_{p1,m1}(|A_{11}|) = \frac{K_{pm}(|A_{11}|)}{|A_{11}|} \quad (2-29)$$

$$T_{p1,m1}(|A_{11}|) = 0 \quad (2-30)$$

$$\forall \{q, n\} \neq \{1, 1\}: S_{pq,mn}(|A_{11}|) = \frac{G_{pq,mn}(|A_{11}|) + jH_{pq,mn}(|A_{11}|)}{2} \quad (2-31)$$

$$\forall \{q, n\} \neq \{1, 1\}: T_{pq,mn}(|A_{11}|) = \frac{G_{pq,mn}(|A_{11}|) - jH_{pq,mn}(|A_{11}|)}{2} \quad (2-32)$$

Subscript p and m denote the port and harmonic associated with B whereas q and n are the port and harmonic for component A. Equation (2-28) now relates input and output spectral components with different frequencies. For example, it relates how A_{12} , the second harmonic on the incident wave can contribute to a change in B_{22} , the second harmonic at port 2.

2.5 X-Parameters

X-parameters are a trademark of Keysight Technologies and was formulated by restructuring the original PHD formulation into a commercially viable form [38]. A superset of S-parameters, X-parameters can be applied to both linear and non-linear simulations which include the generation of harmonic and intermodulation products [34].

X-parameters are currently the most widely used Behavioural modelling approach in the industry due to its backing by Keysight. X-parameters have been extended to model hard nonlinear behaviour and long term memory effects [39]-[41]. Models have also been developed for packaged GaN transistors [42]-[43] and GSM amplifier modules [44].

Envelope system simulations have now seen the use of X-parameters [45]-[46] and its use has also been demonstrated for modelling RF high power devices

(250W LDMOS) [47], power probes [48] and polar modulated power amplifiers [49]. The work in [49] shows that X-parameters can even be applied to systems which have a baseband port besides a RF and DC port.

Over the years, different variations of X-Parameters have been developed. Examples include S-functions [50] and the Padé Approximation Model [51], developed by NMDG and University College Dublin, respectively. Since the formulations of these models are similar to X-Parameters, this section shall only focus on the discussion of X-Parameters.

2.5.1 X-Parameters Formulation and Extraction

By referring back to equation (2-28), note that when q and n are equal to 1,

$$P^{+m-1}A_{11} = P^{+m+1}conj(A_{11}) = |A_{11}| \quad (2-33)$$

Therefore since only the sum of $S_{p1,m1}(A_{11})$ and $T_{p1,m1}(A_{11})$ is of importance, $T_{p1,m1}(A_{11})$ can be set to zero as defined in eqn. (2-30). With $T_{p1,m1}(A_{11}) = 0$, the X-parameter formulation with its 3 model coefficients, X_F , X_S and X_T can be simplified from eqn. (2-28), resulting in eqn. (2-34).

$$\begin{aligned} B_{pm} = & X_{Fpm}(|A_{11}|)P^{+m} \\ & + \sum_{qn} X_{S_{pq,mn}}(|A_{11}|)P^{+m-n}A_{qn} \\ & + \sum_{qn} X_{T_{pq,mn}}(|A_{11}|)P^{+m+n}conj(A_{qn}) \end{aligned} \quad (2-34)$$

If equation (2-34) is restricted to a simple case of B_{21} depending only on A_{21} and A_{11} , it is reduced to

$$B_{21} = X_{F21}(|A_{11}|)A_{11} + X_{S22,11}(|A_{11}|)A_{21} + X_{T22,11}(|A_{11}|)P^2 \text{conj}(A_{21}) \quad (2-35)$$

Extracting the model coefficients X_{F21} , $X_{S22,11}$, $X_{T22,11}$ for a given value of A_{11} is illustrated in Fig. 2-12.

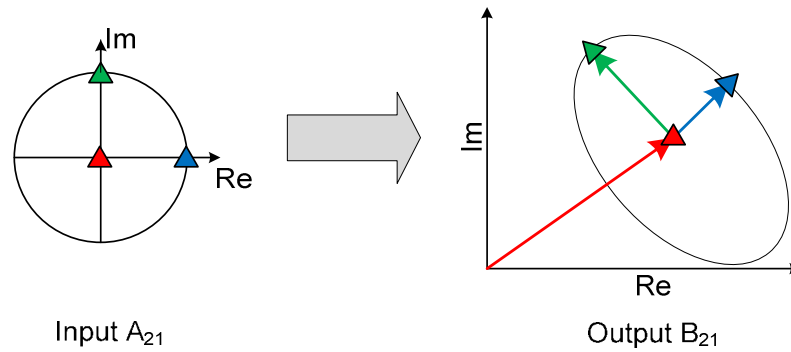


Figure 2-12: X-parameter extraction procedure [31].

A_{11} amplitude is applied and kept constant throughout the measurement. Firstly, to extract X_{F21} no other incident wave is applied besides A_{11} (represented by the red triangle). Then two independent measurements of A_{21} with phase 0° and 90° are applied (represented by the blue and green triangles respectively). These two measurements enable the extraction of $X_{S22,11}$ and $X_{T22,11}$. In other words, measurements include:

- 1) Responses of the DUT at each port and harmonic frequency to the large signal without perturbation.
- 2) Responses when a large signal is added with a small signal perturbation.
- 3) Responses when a large signal is added with small signal perturbation that is at the same frequency but a different phase compared to 2).

Although 3 measurements is the minimum number needed for the model extraction, more measurements are made in combination with a linear

regression technique as redundancy reduces residual model errors and allows noise errors to be obtained.

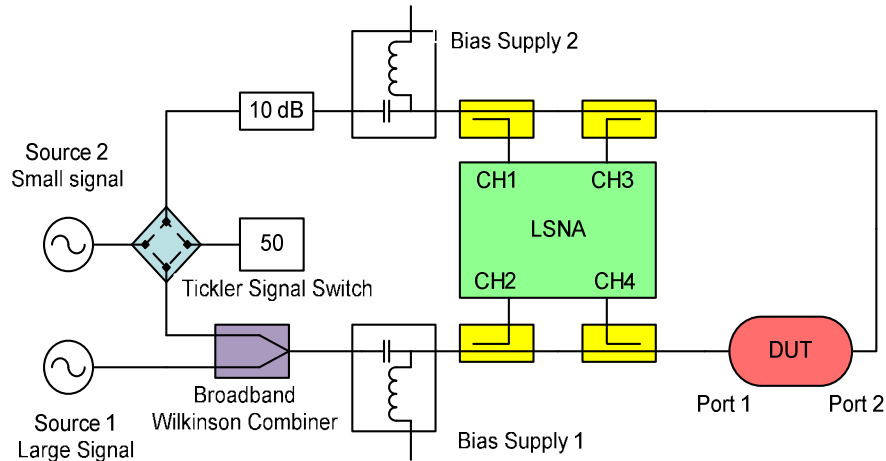


Figure 2-13: X-parameter coefficient extraction measurement setup [31].

The measurement setup based on [31] is shown in Fig. 2-13. The LSNA measures all the relevant A_{mk} and B_{mk} components with m representing the port and k the harmonic response. Source 1 is used for generation of the A_{11} component (a large input tone). Source 2 combined with a switch is used for the generation of small signal harmonic components, known as tickler signals. The switch allows the tickler tones to be applied either the input or output port.

2.5.2 Measurements of Load Dependent X-Parameters

As most high power transistors and amplifiers have an optimum impedance that is far from 50 ohms, X-parameters should be extracted over a large area of the Smith chart and not restricted to 50 ohms as in [29]-[31]. Therefore, reference [52] introduces NNVA measurements coupled with load-pull to obtain X-parameters over a wide impedance range covering the entire Smith

chart. In [53], a MESFET is measured under arbitrary load conditions and used to predict non-linear behaviour such as harmonics, intermodulation products and ACPR.

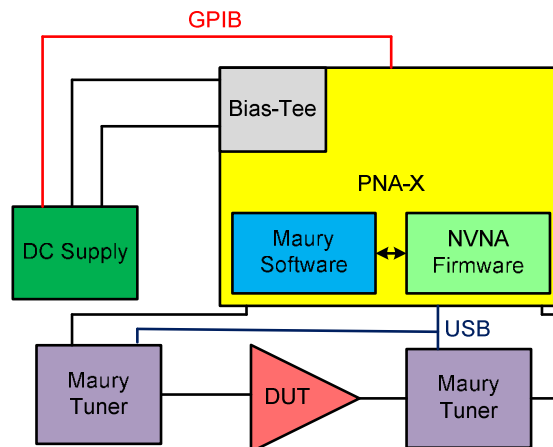


Figure 2-14: Load dependent X-parameter measurement setup [52].

Since X-parameters have a fixed formulation involving 3 coefficients which are X_F , X_S and X_T , the model validity is limited to a small area on the Smith Chart. This is because its formulation does not account for dependence on A_2 by assuming it is small compared to A_1 [38]. The system setup for measurements of load-dependent X-parameters is depicted in Fig. 2-14, based on the work in [52].

The PNA-X acting as the receiver is loaded with the Maury software which runs the user interface and the NVNA firmware which is used for calibration purposes. Bias sweeps are made possible through the use of a GBIP controlled external DC supply. Load-pull is accomplished using the tuners and at each load, the X-parameters can be extracted and stored in a file. This file can be directly imported into ADS for simulation purposes.

2.5.3 X-Parameters Discussion

In terms of equation complexity, X-parameters are limited to three parameters X_F , X_S , and X_T . Having a rigid formulaic structure makes it inflexible when presented with increasing degrees of nonlinearity. A limited number of terms also results in the formulation being load dependent as it can only model a very limited space on the Smith Chart. This in turn will cause the model file size to increase dramatically as it must now be a function of load.

With current trends moving towards measurements with fundamental and harmonic loads, and coupled with having to measure over bias as well as frequency, the model file size can increase to several gigabytes. This places a huge burden on data storage, sharing and processing of the models. Therefore, formulations such as the Cardiff Model reduces the file size due to the fact that it does not have to be load-dependent. The equations for the Cardiff Behavioural Model will be shown in Section 2.6.

2.6 Cardiff DWLU Model

The Cardiff Model began as a Direct Waveform Lookup (DWLU) model which allows direct utilization of large signal data into the PA design process [54]. This "truth table look-up model" imports non-linear measurement data into a CAD simulator. It then was further developed based on the Polyharmonic Distortion model concept resulting in an equation based model with coefficients that can be extracted from measurement data [55]-[64].

2.6.1 Cardiff DWLU Model Formulation and Extraction

As the name suggests, the Cardiff DWLU takes large signal waveform measurements and uses it directly for CAD design. The model is defined in the

frequency domain based on Fig. 2-15 its implementation has been verified using a 100 W LDMOS device [54].

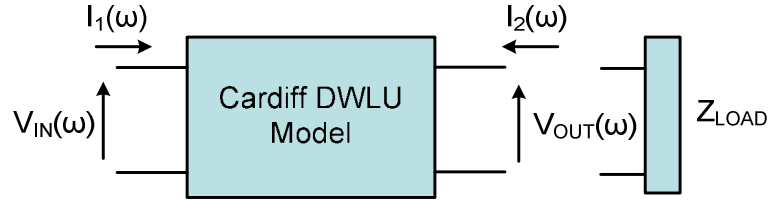


Figure 2-15: Definition of Cardiff DWLU Model [47].

The current response at each port for a particular load impedance, Z_{load} can be defined as:

$$I_1(\omega) = A_0 \cdot \delta(\omega) + \sum_{n=1}^m A_n \cdot V_{IN}^n \cdot \delta(\omega - 2\pi \cdot n \cdot f_0) \quad (2-36)$$

$$I_2(\omega) = B_0 \cdot \delta(\omega) + \sum_{n=1}^m B_n \cdot V_{IN}^n \cdot \delta(\omega - 2\pi \cdot n \cdot f_0) \quad (2-37)$$

where V_{IN} is the input stimulus, n is the order of harmonics, f_0 is the fundamental frequency, and A_0 and B_0 are the DC components.

The coefficients A_n and B_n are functions of V_{IN} , Z_{load} and bias which are $V_{DC IN}$ and $V_{DC OUT}$ and can be expressed as:

$$A_n = \frac{I_1(nf_0)}{V_{IN}^n(nf_0)} = F_1(|V_{IN}|, \Gamma_{LOAD}, V_{DC IN}, V_{DC OUT}) \quad (2-38)$$

$$B_n = \frac{I_2(nf_0)}{V_{IN}^n(nf_0)} = F_2(|V_{IN}|, \Gamma_{LOAD}, V_{DC IN}, V_{DC OUT}) \quad (2-39)$$

These coefficients will be calculated based on measurement data and saved into a data table. For a particular stimulus voltage, load and bias, the CAD

simulator will be able to look up or interpolate the corresponding A_n and B_n and compute the resulting port currents.

Note that the model uses voltage and current (V&I) waves instead of scattered (A&B) waves because the implementation in ADS uses a frequency domain device (FDD) block which computes current and voltage components in the frequency domain [54]. Coefficients A_n and B_n which are $I_n(nf_0)/V_{IN}^n$ are looked up instead of $I_n(nf_0)$ in order to scale I_n with the n^{th} power of fundamental input voltage. This makes the coefficients independent of the reference phase of the input stimulus and smoothens the truth table, enabling a more robust interpolation function.

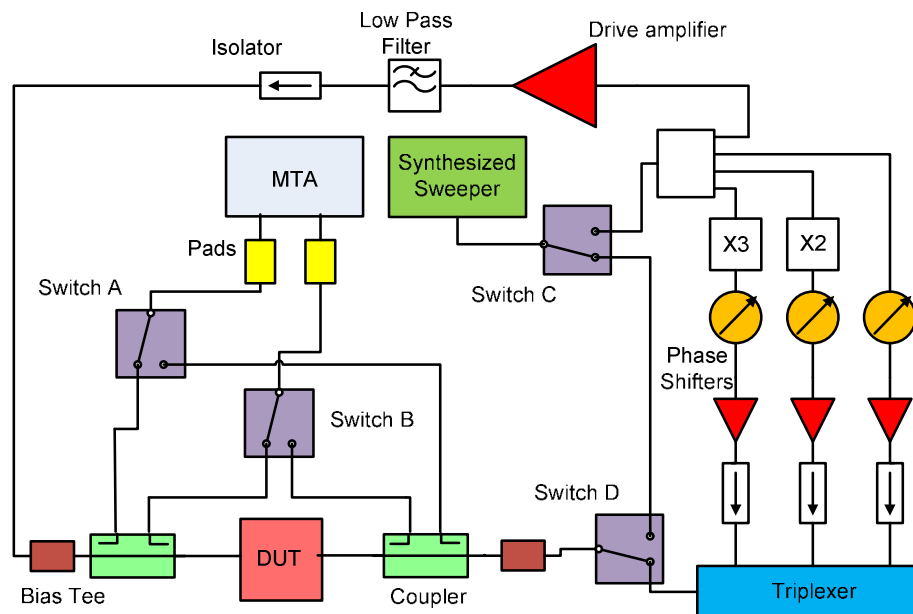


Figure 2-16: Time domain based RF waveform measurement system [65].

The measurement setup for extracting the DWLU model is shown in Fig. 2-16, based on the RF time domain measurement system in [65]. The MTA measures the voltage and current waveforms using couplers that are attached to the DUT.

Since the MTA is a 2 channel instrument, the input and output voltage and current waveforms are obtained and phase synchronised using switches A and B. The waveforms are then used to calculate the A and B coefficients described by equations (2-38) and (2-39). Switch C allows the synthesized sweeper to provide the stimulus at either the input or output whereas Switch D switches between fundamental only or fundamental and harmonic active load-pull.

2.6.2 Cardiff DWLU Discussion

The DWLU approach was developed to enable the direct import of current and voltage waveform measurements into a CAD environment. Large signal waveform data can be compiled into a lookup table without lengthy processing and generates a faithful reproduction of the device non-linear behaviour as long as the simulation is carried out within the measurement space of the data.

However, this approach does have several weaknesses [56]-[57]. Simulations extrapolated outside the measurements space will result in inaccurate results. In addition, obtaining a large set of measurement data is crucial for good accuracy, making it a time consuming process. Simulation speed is also slow and hampered due to the large amount of data that has to be loaded into the simulator.

In order to overcome these limitations, the Cardiff Model has evolved into a polynomial based Behavioural model with model coefficients that can be directly extracted from the measured data.

2.7 Cardiff Behavioural Model

The Cardiff Behavioural Model approach was first developed by Qi et. al. [55]-[57]. It is based on the Polyharmonic Distortion formulation but with several exceptions. In the original PHD formulation seen in [29]-[30] and in equation (2-28), the S and T parameters are dependent only on the magnitude of A_1 , the input travelling wave. It is assumed that A_1 is the only large signal tone and that A_2 is small compared to A_1 . This makes the model valid only around points of model extraction (usually 50 ohms).

Such an assumption would be valid for system components but a large variation in A_2 can be seen in load-pull data especially for high power devices with optimums far from 50 ohms [56]. The Cardiff Model includes the dependence on the A_2 travelling wave, enabling extrapolation at points away from where the model is extracted.

Research on the Cardiff Model formulation has expanded from a fundamental only expression [55]-[58] to equations for harmonic contributions [59]-[64].

2.7.1 Cardiff Behavioural Model Formulation and Extraction (Fundamental only)

A typical 2 port network with travelling waves can be related by the following equations using describing functions.

$$b_1 = f(a_1, a_2) \quad b_2 = g(a_1, a_2) \quad (2-40)$$

General describing functions only define system behaviour on the conceptual level. In order to integrate the describing functions into a CAD simulator, it must be approximated with n^{th} order polynomials. For the sake of brevity, the polynomial is limited to the 3rd order as shown in equation (2-41)-(2-42).

$$b_1 = \varphi_{10}a_1 + \varphi_{01}a_2 + \varphi_{11}a_1a_2 + \cdots + \varphi_{30}a_1^3 + \varphi_{03}a_2^3 \quad (2-41)$$

$$b_2 = \theta_{10}a_1 + \theta_{01}a_2 + \theta_{11}a_1a_2 + \cdots + \theta_{30}a_1^3 + \theta_{03}a_2^3 \quad (2-42)$$

Through regrouping and expansion [57], equations (2-41)-(2-42) can be expressed as:

$$b_1 = S_{11}a_1 + T_{11}a_1^*Q^2 + S_{12}a_2 + T_{12}a_2^*P^2 \quad (2-43)$$

$$b_2 = S_{21}a_1 + T_{21}a_1^*Q^2 + S_{22}a_2 + T_{22}a_2^*P^2 \quad (2-44)$$

With a_n^* being the conjugate of a_n . Q and P are the phase vectors $e^{-j\omega(a_2)}$ and $e^{j\omega(a_1)}$ respectively. The coefficients S and T are defined as shown below:

$$S_{11} = \varphi_{10} + 3\varphi_{30}|a_1|^2 + \varphi_{12}|a_2|^2 \quad T_{11} = \varphi_{12}|a_2|^2 \quad (2-45)$$

$$S_{12} = \varphi_{01} + 3\varphi_{03}|a_2|^2 + \varphi_{21}|a_1|^2 \quad T_{12} = \varphi_{21}|a_1|^2 \quad (2-46)$$

$$S_{21} = \theta_{10} + 3\theta_{30}|a_1|^2 + \theta_{12}|a_2|^2 \quad T_{21} = \theta_{12}|a_2|^2 \quad (2-47)$$

$$S_{22} = \theta_{01} + 3\theta_{03}|a_2|^2 + \theta_{21}|a_1|^2 \quad T_{22} = \theta_{21}|a_1|^2 \quad (2-48)$$

Note that equations (2-43)-(2-44) are similar to the original PHD equations (2-28) except that it is a function of both a_1 and a_2 . T_{11} and T_{21} also does not exist in the original PHD formulation and results from [55] show that these coefficients are close to zero when a_2 is very small. But as a_2 increases, T_{21} starts to increase and its dependency on a_2 can no longer be ignored.

Woodington et al. extended the research on the Cardiff Model by highlighting that each S and T coefficient has a unique phase operator [58] and equations (2-43)-(2-44) can be reformulated as shown:

$$b_{11} = S_{11}|a_1| \cdot P + T_{12}|a_2|P \cdot \frac{P}{Q} + S_{12}|a_2| \cdot Q + T_{11}|a_1|Q \cdot \frac{Q}{P} \quad (2-49)$$

$$b_{21} = S_{21}|a_1| \cdot P + T_{22}|a_2|P \cdot \frac{P}{Q} + S_{22}|a_2| \cdot Q + T_{21}|a_1|Q \cdot \frac{Q}{P} \quad (2-50)$$

The equations above mean that by performing measurements of load-pull locus with a constant $|a_1|$ and $|a_2|$ while sweeping the relative phase θ (P/Q or Q/P), each S and T coefficient can be extracted independently based on equations (2-51) to (2-54).

$$S_{11}|a_1| = \frac{1}{n} \sum b_1 \frac{1}{P} \quad T_{11}|a_1| = \frac{1}{n} \sum b_1 \frac{P}{Q^2} \quad (2-51)$$

$$S_{12}|a_2| = \frac{1}{n} \sum b_1 \frac{1}{Q} \quad T_{12}|a_2| = \frac{1}{n} \sum b_1 \frac{Q}{P^2} \quad (2-52)$$

$$S_{21}|a_1| = \frac{1}{n} \sum b_2 \frac{1}{P} \quad T_{21}|a_1| = \frac{1}{n} \sum b_2 \frac{P}{Q^2} \quad (2-53)$$

$$S_{22}|a_2| = \frac{1}{n} \sum b_2 \frac{1}{Q} \quad T_{22}|a_2| = \frac{1}{n} \sum b_2 \frac{Q}{P^2} \quad (2-54)$$

where n is the number of measured phase steps from 0 to 2π . The measurements setup for measuring the relevant load-pull loci for the model is shown in Fig. 2-17.

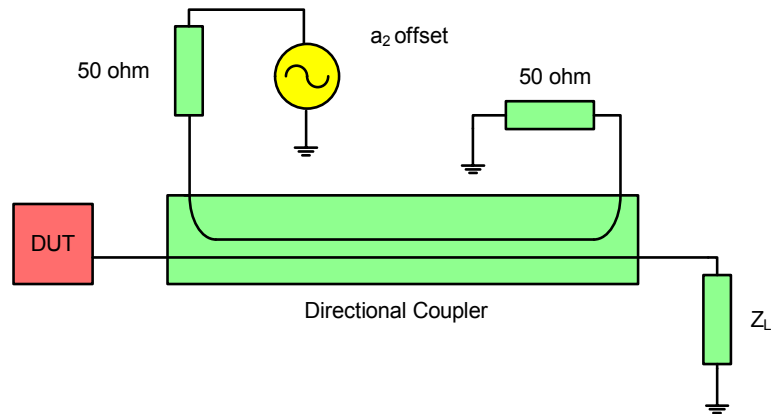


Figure 2-17: Architecture for generating required load-pull loci by integrating active source with passive load-pull system [58].

It is a hybrid combination of an active and passive load-pull system that allows the user to centre the measurements at an optimum impedance other than 50 ohms. The signal generator for a_2 is held at a constant power level while varying its phase from 0 to 2π .

Note that equations describing the b waves in (2-49)-(2-50) are limited up to the 3rd order. In order to consider higher order of mixing, consider the polar form of indexing for the describing function,

$$b_{p,h} = P_1^h g_{p,h} \left(|a_{1,1}|, |a_{2,1}|, \left(\frac{Q_1}{P_1} \right) \right) \quad (2-55)$$

where p and h represent the port and harmonic respectively and $P_1 = \frac{a_{1,1}}{|a_{1,1}|}$ (phase of $a_{1,1}$) and $Q_1 = \frac{a_{2,1}}{|a_{2,1}|}$ (phase of $a_{2,1}$). The phase vector $\frac{Q_1}{P_1}$ is a periodic function and therefore the $b_{p,h}$ is also periodic.

Equation (2-55) allows phase effects to be considered independently of magnitudes and can be expanded, allowing all orders of phase non-linearity to be described by a set of coefficients as shown in equation (2-56) with N being the mixing order complexity [58].

$$b_{p,h} = P_1^h \sum_{n=-(N-1)/2}^{n=(N+1)/2} \left\{ R_{p,h,n} |a_{1,1}|, |a_{2,1}|, \left(\frac{Q_1}{P_1} \right)^n \right\} \quad (2-56)$$

Note that this formulation is the same as the X-parameter equation in (2-34) if it is truncated to only 3 coefficients. For example, for a $b_{2,1}$ wave depending only on $a_{1,1}$ and $a_{2,1}$ like equation (2-35), the $R_{2,1,0}$, $R_{2,1,1}$ and $R_{2,1,-1}$ coefficients are similar to X_F , X_S and X_T . As expected, if $N = 3$, equation (2-56) becomes eqn. (2-49)-(2-50).

The results of measurements on a 0.5 W HBT device shows a comparison between different orders of mixing complexity. When $N = 1$, this is similar to the Simple Hot S-parameters described in Section 2.3.1.2. The results also indicate that 3rd order of mixing ($N=3$) is insufficient to model b_2 accurately when the a_2 is large. An order of 5 or 7 provides a more accurate prediction of b_2 and also load-pull contours [60].

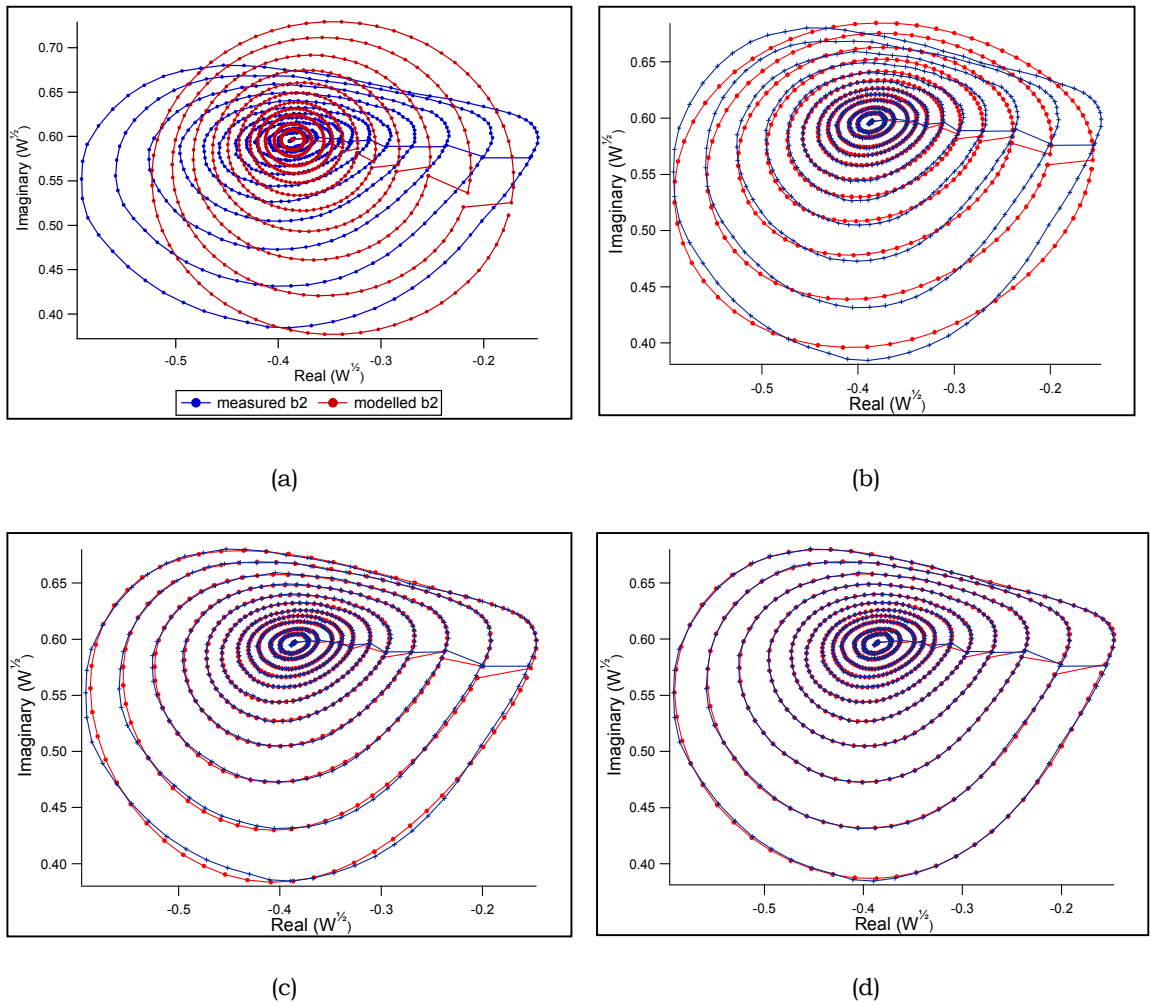


Figure 2-18: Comparison of $B_{2,1}$ measured on 0.5 W HBT extracted with different orders of complexity (a) $N = 1$ (b) $N = 3$ (c) $N = 5$ (d) $N = 7$ [60].

These results are shown in Fig. 2-18(a)-(d). Note that the coefficients $R_{p,h,n}$ in (2-56) are obtained using Fourier Transform on the b waves due to its a

periodic response. An example is shown in Fig. 2-19, extracted from measurements on a 10x75 μm GaAs HEMT [60].

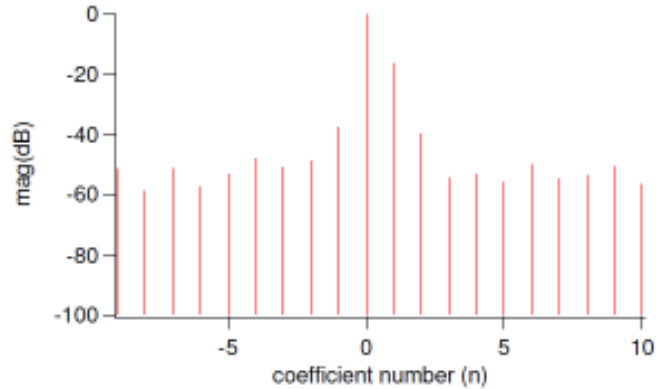


Figure 2-19: Coefficient spectrum for $R_{p,h,n}$ measured on a 10x75 μm GaAs HEMT [60].

This form of analysis allows the user to determine the maximum order needed to model the output response. The results here show that increasing the order, N above 7 is unnecessary as all the higher terms are lower than the noise floor of -50 dB. This means that a low order of model complexity is needed for an accurate model.

2.7.2 Cardiff Behavioural Model Formulation and Extraction (Input and Output Harmonics)

The Cardiff Model was extended to account for harmonic load-pull at the output [59]-[60] and input [62]-[64]. The framework is based on the mixing theory whereby to account for 2nd harmonic contributions at port 2 when there exists the $a_{2,2}$ stimuli, a new phase vector $\frac{Q_2}{P_1^2}$ is present.

To extract these coefficients in a measurement, the new phase vector $\frac{Q_2}{P_1^2}$ would be rotated from 0° to 360° . The coefficients will produce periodic changes with respect to $\frac{Q_2}{P_1^2}$ and can be expressed by:

$$R_{p,h,n} = \sum_r \left\{ G_{p,h,n,r} (|a_{1,1}|, |a_{2,1}|, |a_{2,2}|) \left(\frac{Q_2}{P_1^2} \right)^r \right\} \quad (2-57)$$

$$b_{p,h} = P_1^h \sum_{n=-(N-1)/2}^{n=(N+1)/2} \sum_r \left\{ G_{p,h,n,r} (|a_{1,1}|, |a_{2,1}|, |a_{2,2}|) \left(\frac{Q_1}{P_1} \right)^n \left(\frac{Q_2}{P_1^2} \right)^r \right\} \quad (2-58)$$

Substituting the coefficients from (2-57) into (2-56) results in equation (2-58). Note the coefficients $G_{p,h,n,r}$ are still only a function of magnitude of the stimuli and independent of the phases. The phase difference between the two signals at the output are accounted for by the cross product terms (those related to Q_1Q_2 and Q_1/Q_2).

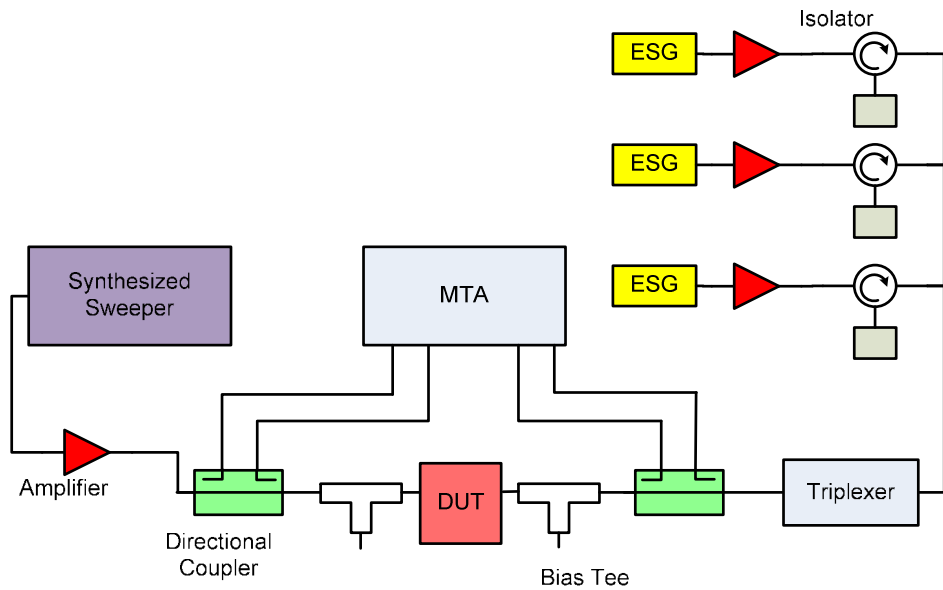
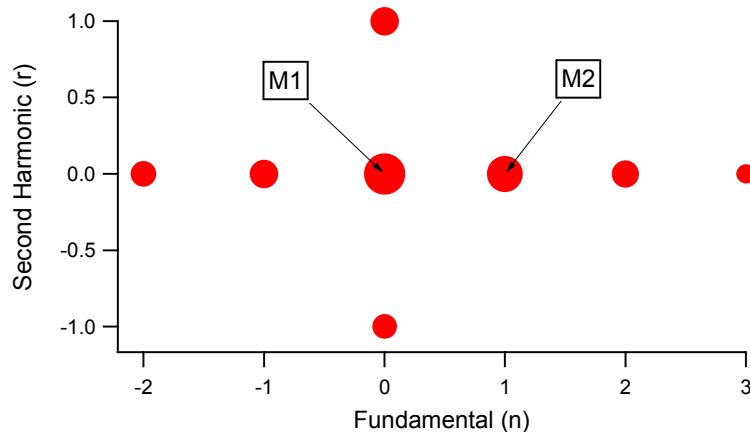


Figure 2-20: Active harmonic load-pull waveform measurement system [66].

Fig. 2-20 illustrates the measurement system in Cardiff University used to obtain the data [66]. A synthesized sweeper acts as the input source whereas active load-pull is employed at the output using phase coherent electronic signal generators (ESGs) and amplifiers. The Microwave Transition Analyser (MTA) measures the waveforms via directional couplers attached to the DUT. In order to extract the coefficients, the following steps are performed:

1. The second harmonic phase vector is rotated from 0° to 360° with a fixed fundamental phase vector.
2. Step 1 is repeated for a different fundamental phase rotated from 0° to 360° .
3. Steps 1 and 2 is repeated for varying values of fundamental and second harmonic stimuli at port 2 ($|a_{2,1}|$ and $|a_{2,2}|$).

The importance of cross product terms is demonstrated in results from [59]. These measurements on a $10 \times 75 \mu\text{m}$ GaAs HEMT device at 9 GHz are shown in Fig. 2-21(a)-(b) to 2-22(a)-(b).



(a)

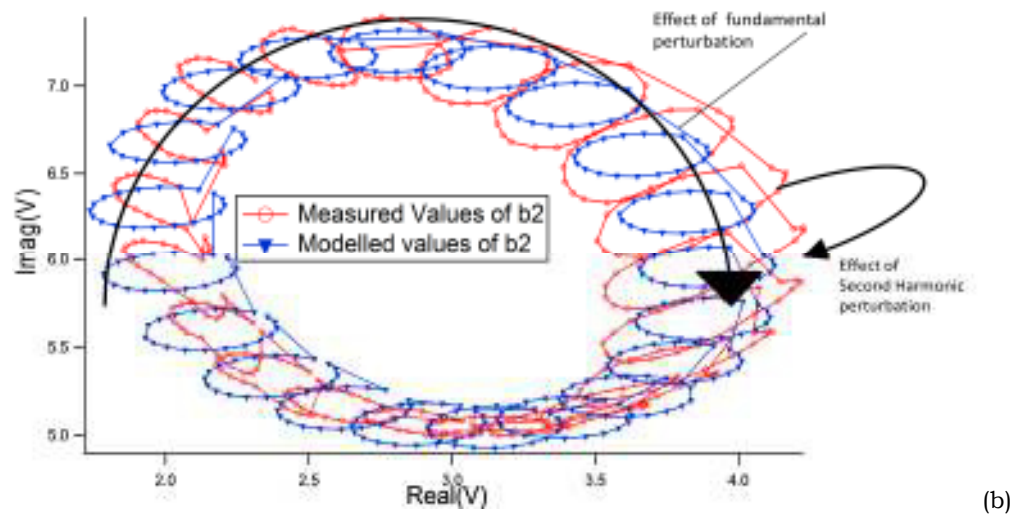


Figure 2-21: Results of measurements on $10 \times 75 \mu\text{m}$ GaAs HEMT (a) Extracted coefficient space without cross product terms (b) Measured and modelled $b_{2,1}$ [59].

In Fig. 2-21(b) the modelled $b_{2,1}$ is represented by the coefficient space in Fig. 2-21(a). The size of the coefficients in Fig. 2-21(a) and 2-22(a) represent the magnitude of the coefficients. In Fig. 2-21(a), M1 is the $R_{2,1,0}$ (most dominant term) while M2 is the $R_{2,1,1}$ (second largest term).

The modelled $b_{2,1}$ results in Fig. 2-21(b) are not accurate since it does not account for mixing between the second harmonic signal at the output, $a_{2,2}$ and fundamental signal at the input, $a_{2,1}$, causing the average error of the extraction to be 1.8%.

To capture the output mixing behaviour, coefficients with cross product terms are produced as shown Fig. 2-22(a). The extraction error now reduces to 0.25 % and the resulting $b_{2,1}$ wave is presented in Fig. 2-22(b). This model is now able to accurately track changes in the 2nd harmonic perturbation around the fundamental phase of $b_{2,1}$.

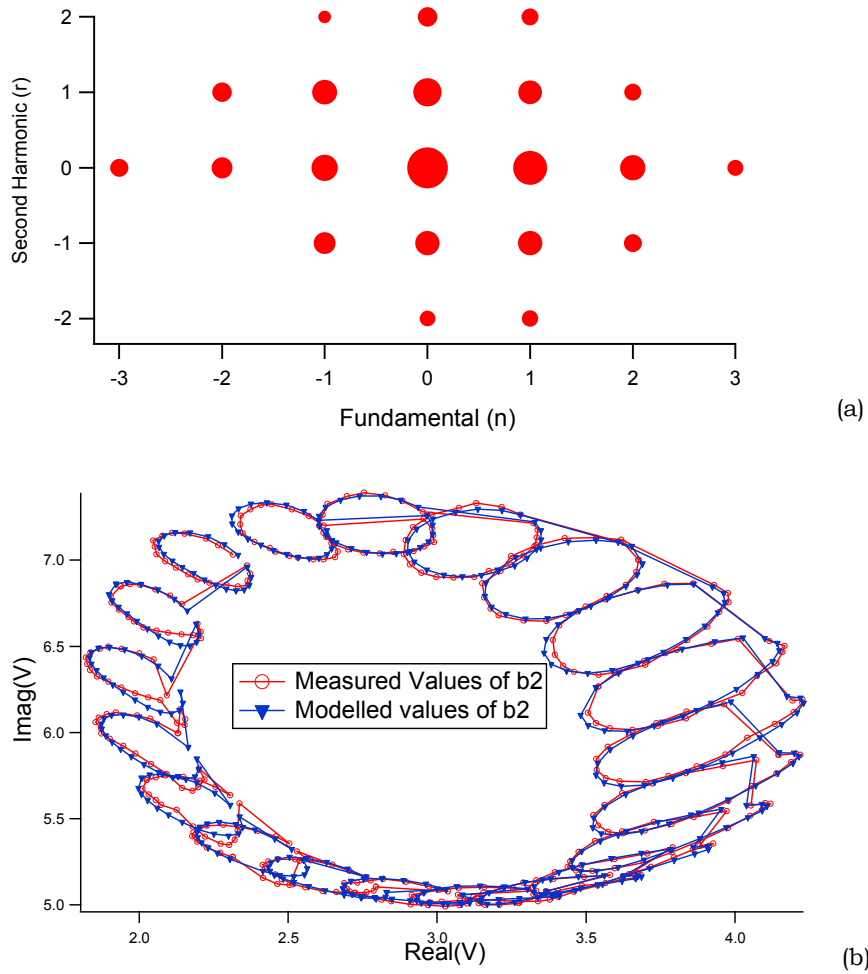


Figure 2-22: Results of measurements on 10x75 μ m GaAs HEMT (a) Extracted coefficient space with cross product terms (b) Measured and modelled $b_{2,1}$ [59].

The equation in (2-58) can also be expanded to account for perturbation in the input second harmonic stimulus [62]-[64] and becomes:

$$b_{p,h} = P_1^h \sum_{n=-(N-1)/2}^{n=(N+1)/2} \sum_r \left\{ G_{p,h,n,r} (|a_{1,1}|, |a_{1,2}|, |a_{2,1}|) \left(\frac{P_{1,2}}{P_{1,1}^2} \right)^n \left(\frac{Q_{2,1}}{P_{1,1}} \right)^r \right\} \quad (2-59)$$

This formulation is now able to account for changes of source impedance at the 2nd harmonic frequency. The mixing model is able to accurately capture the responses due to 2nd harmonic injection at the input and when used in a

CAD environment, is able to increase the efficiency of the Class B amplifier from 73.35 to 78.75% [63].

2.7.3 Cardiff Behavioural Model Discussion

The Cardiff Model has evolved from a DWLU model into a polynomial based Behavioural model and has been improved upon in previous research [54]-[64]. The Cardiff Model formulation valid for fundamental only load-pull was developed in [55], [56] and [58]. It is based on the Polyharmonic Distortion Model but extended to include terms to account for large A_2 in the stimulus [55]. The work in [58] concludes that the coefficient terms are independent of the phase of the stimulus and can be extracted by varying the phase of the source.

Unlike X-parameters, the Cardiff Model coefficient terms are not limited to only 3 (X_F , X_S and X_T). As described by equation (2-56), the order, N and by extension the number of coefficients can be increased for better model accuracy [58]. The maximum order and number of terms is dictated by analysing the Fourier Transform of the b waves. Note that having 2 coefficients (order, $N = 1$) will result in Hot S-parameters.

The Cardiff Model is then improved upon, based on the mixing model formulation and capable of capturing the responses due to the fundamental and harmonic load-pull at the output [59]-[60] and input [62]-[64]. The formulation now contains cross products terms which are vital to accurately track changes due to 2nd harmonic perturbation for all phases of the output fundamental signal.

2.8 Scaling of Behavioural Models

Unlike Compact models, Behavioural models have always been regarded as unable to scale with respect to geometry and frequency [67]. Instead, much work has been conducted on scaling Compact models for various devices [68]-[75]. Scalable Compact models were developed for InP DHBT [68], High Power LDMOS [69], GaN HEMTs [70], HBTs [71]-[73] and mm-Wave FETs [74].

A major breakthrough was achieved by Leckey [75] in 2011 by proving that X-Parameters can scale with transistor gate width and number of fingers by extracting the X-Parameter model at the intrinsic plane.

Model scaling can be achieved by borrowing from techniques previously used in Compact models where the intrinsic transistor is known to scale linearly with the size of the total gate width (unit gate width X number of fingers) and prior determination of extrinsic component values allows the user to de-embed to the intrinsic plane [74].

The verification in [75] was carried out by scaling a 0.15 μm pHEMT device from 10x90 μm down to 4x50 μm . It must be pointed out that the verification was done solely in the simulator and not from experimentally measured values.

The research on scaling of Behavioural models was extended further in [76] by proving via simulation based extractions and experimental measurements that X-Parameters are scalable. The explicit scaling relationship for X-Parameters as a function of geometry are also presented for the first time.

As described in Section 2.5, X-Parameters can be defined as

$$\begin{aligned}
 B_{p,k} = & X_{p,k}^{(F)}(|A_{11}|, A_{21})P^k \\
 & + \sum_{q,m} X_{p,k;q,m}^{(S)}(|A_{11}|, A_{2,1})P^{k-m}A_{q,m} \\
 & + \sum_{q,m} X_{p,k;q,m}^{(S)}(|A_{11}|, A_{2,1})P^{k+m}A_{q,m}^*
 \end{aligned} \tag{2-60}$$

with p and q representing the ports while k and m are the harmonics of the system. At the intrinsic device, scaling of the voltage and current in the time domain can be illustrated by Fig. 2-23 and described using equation (2-61).

$$I_p^{sc}(t) = rI_p(t) \quad V_p^{sc}(t) = V_p(t) \quad r = \frac{W^{sc}}{W} \tag{2-61}$$

where p represents the port and the superscript "sc" denotes the larger device. r also known as the scaling factor, is the ratio between of the total gate width of the larger device, W^{sc} to the total gate width of the smaller device, W.

$$V_{p,k} = \sqrt{Z_0}(A_{p,k} + B_{p,k}) \quad I_{p,k} = \frac{1}{\sqrt{Z_0}}(A_{p,k} - B_{p,k}) \tag{2-62}$$

$$V'_{p,k} = V_{p,k} \quad I'_{p,k} = rI_{p,k} \tag{2-63}$$

The relationship between the spectral components of the voltage and current in the frequency domain and the travelling waves is shown in (2-62). Equation (2-63) describes the voltage and current spectra where scaling has been applied.

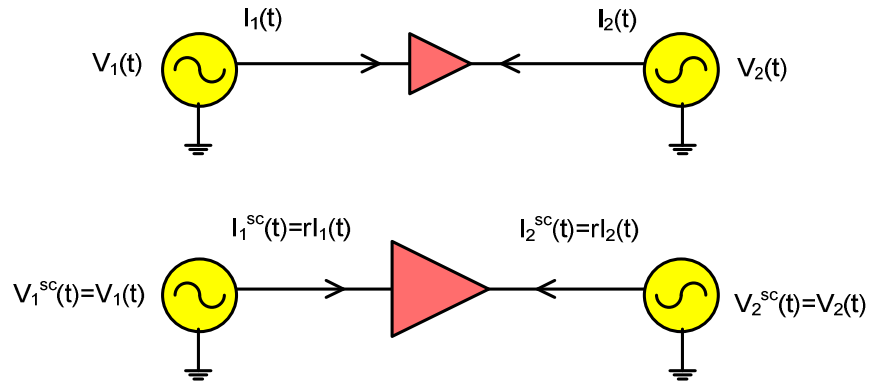


Figure 2-23: Scaling relationship for voltage and current at the intrinsic plane [76].

Using (2-63), the travelling waves of the larger, scaled device can be defined by (2-64)-(2-67).

$$A'_{p,k} = \frac{V'_{p,k} + Z_0 I'_{p,k}}{2\sqrt{Z_0}} = \frac{V_{p,k} + Z_0 r I_{p,k}}{2\sqrt{Z_0}} \quad (2-64)$$

$$B'_{p,k} = \frac{V'_{p,k} - Z_0 I'_{p,k}}{2\sqrt{Z_0}} = \frac{V_{p,k} - Z_0 r I_{p,k}}{2\sqrt{Z_0}} \quad (2-65)$$

$$A'_{p,k} = \left(\frac{1+r}{2}\right) A_{p,k} + \left(\frac{1+r}{2}\right) B_{p,k} \quad (2-66)$$

$$B'_{p,k} = \left(\frac{1-r}{2}\right) A_{p,k} + \left(\frac{1+r}{2}\right) B_{p,k} \quad (2-67)$$

Solving (2-60) with (2-66) and (2-67) simultaneously will result in the new $B^{\text{sc}}(A^{\text{sc}})$ relationship from which the X-Parameters of the scaled device can be extracted. In [76], experimental validation with a scaling factor, $r = 2$ was conducted using $4 \times 60 \mu\text{m}$ and $4 \times 30 \mu\text{m}$ GaAs MESFETs. The X-Parameter coefficients X_F , X_S and X_T of the reference device and the scaled device are shown to be in good agreement and successfully scale with geometry.

2.9 Summary

This chapter provides an overview of Behavioural models, from S-parameters (considered as a linear Behavioural model) to non-linear models such as the Polyharmonic Distortion Model. The formulation and extraction of the model coefficients for the different Behavioural models have been presented and discussed.

Scaling in Behavioural models has also been presented. From the literature review, there has been very little work done on scaling of Behavioural models since it is considered by many as being a inflexible measurement based model and scaling properties is thought to be poor [67]. So far, geometric scaling has only been proven for X-Parameters. Furthermore, the work in [75] only involves verification through simulations. In [76], scaling was experimentally verified only at a scaling factor of 2.

This opens up a huge opportunity for research by trying to apply the Cardiff Model (a generalized Behavioural model formulation) to geometric scaling. Scaling to various gate sizes can also be experimentally conducted to see the limitations of the model.

From the literature, no attempts have been made on frequency scaling using Behavioural models. Therefore, research into this area is novel and can be conducted using both the X-Parameter and Cardiff Model formulations.

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CHAPTER 3

GEOMETRIC SCALABLE BEHAVIOURAL MODELS

Parameter scaling has already been investigated and applied to X-parameters. Leckey [1] showed using simulation techniques, that like S-parameters, if X-parameters are defined at the intrinsic device plane, they can be successfully scaled with respect to transistor gate periphery. Root et al. [2] extended this work and introduced formal mathematical scaling rules. In this chapter, we apply this concept for the first time to a more general Behavioural model formulation (Cardiff Model) [3]-[8]. A complete measurement/modelling procedure for generating the geometric scalable device models required for MMIC design has been developed and validated. This has been achieved by integrating scalable measurement data look-up table models of a reference device within appropriate passive layout networks.

This process is divided into 4 main steps namely, determining the intrinsic plane of the reference transistor, obtaining the large signal measurement data for conversion into Behavioural models, performing scaling at the intrinsic reference plane and embedding with the passive circuit of the scaled device. The following chapter will explain these steps in detail and present the results of the scalable model.

Limitations of the geometric scalable model are also presented and possible solutions are also discussed. Model development was done on 2 different GaN wafers, proving that this method is robust and not limited by a specific foundry process. In both cases, a smaller reference device is able to accurately

predict the performance of devices up to 5 times larger in gate periphery. In addition, the model is shown to be able to extend beyond the power limitations of the measurement system.

3.1 Model formulation

3.1.1 Introduction

A general small signal circuit representation of a transistor is shown in Fig. 3-1 with its extrinsic (passive) and intrinsic (active) components. The extrinsic components are sometimes referred to as the parasitic elements of the transistor.

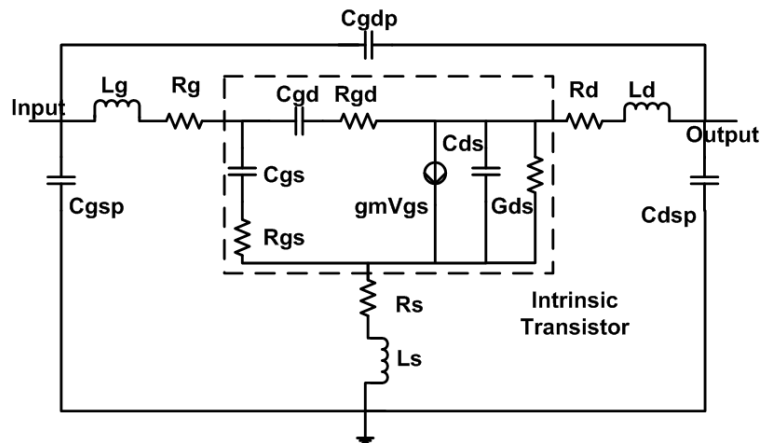


Figure 3-1: Transistor model with extrinsic and intrinsic (enclosed in box) components.

The intrinsic portion of the transistor is able to scale with geometry (gate width and number of fingers) following equation (3-1) where the voltage at ports will remain the same but the current scales with s , the ratio of gate size of the larger device W' to the reference smaller device, W_{ref} [2]. The scaling rules can be applied to the voltage and current spectra as shown in (3-2). Subscripts p and h represent the port and harmonic respectively. The resulting A and B waves can be calculated from equation (3-3). Fig. 3-2 helps put equation (3-1) into perspective.

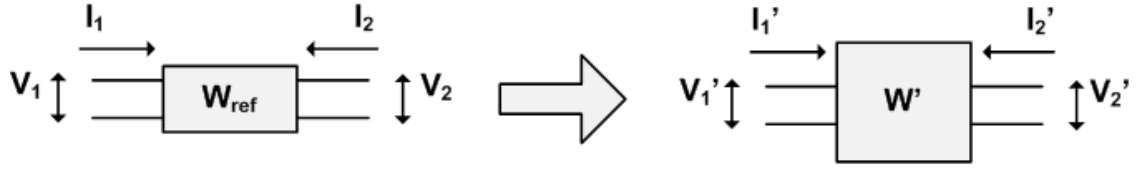


Figure 3-2: Scaling representation of voltage and current with gate geometry.

$$s = \frac{W'}{W_{ref}} \quad V_p'(t) = V_p(t) \quad I_p'(t) = sI_p(t) \quad (3-1)$$

$$V_{p,h}' = V_{p,h} \quad I_{p,h}' = sI_{p,h} \quad (3-2)$$

$$A_{p,h}' = \frac{V_{p,h} + Z_0 s I_{p,h}}{2\sqrt{Z_0}} \quad B_{p,h}' = \frac{V_{p,h} - Z_0 s I_{p,h}}{2\sqrt{Z_0}} \quad (3-3)$$

3.1.2 Modelling process flow

After determining the parasitic components of the reference transistor, extrinsic large signal, engineered RF waveform measurements are performed on a reference device. The bias points and modes of operation can be selected to target required MMIC performance specifications. The Behavioural model parameters are then extracted from the extrinsic measurements of the reference device and stored in a data look-up table.

During simulation, the response of this reference Behavioural model is de-embedded to the intrinsic plane using a passive de-embedding network, scaled and embedded in the required passive network to simulate the extrinsic scaled device behaviour. This can be done using a circuit simulator such as ADS. The modelling process flow is presented in Fig. 3-3.

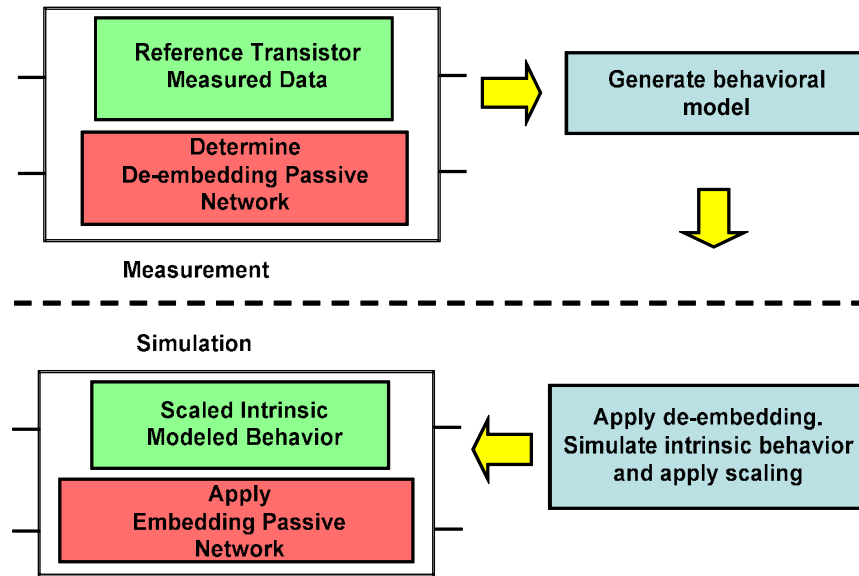


Figure 3-3: Modelling process of geometric scalable transistor Behavioural model.

The parasitic passive networks required can be determined from S-parameter measurements by performing traditional cold FET extraction procedures [9]-[11], characterizing passive test-structures or performing EM simulations [12]. In order to correctly separate the extrinsic from intrinsic component values, a wafer with several widths and number of fingers is needed.

3.1.3 List of devices for experimental validation

Table 3-1 shows a list of GaN devices used for the experimental characterisation and validation, with varying gate widths and number of fingers from a 0.25 μm modelling mask fabricated using WIN Semiconductors' NP25-00 Process (Wafer ID: WN001A). The reference device, which will be utilized in this work to extract the scalable model is the 2x80 μm transistor (highlighted in yellow). Fig. 3-4(a)-(i) show the photos of the devices. The probe pitch is 150 μm .

NOF / Width	80 μm	100 μm	200 μm
2	2x80 μm	2x100 μm	2x200 μm
4	4x80 μm	4x100 μm	4x200 μm
8	8x80 μm	8x100 μm	8x200 μm

Table 3-1: Wafer with varying gate periphery

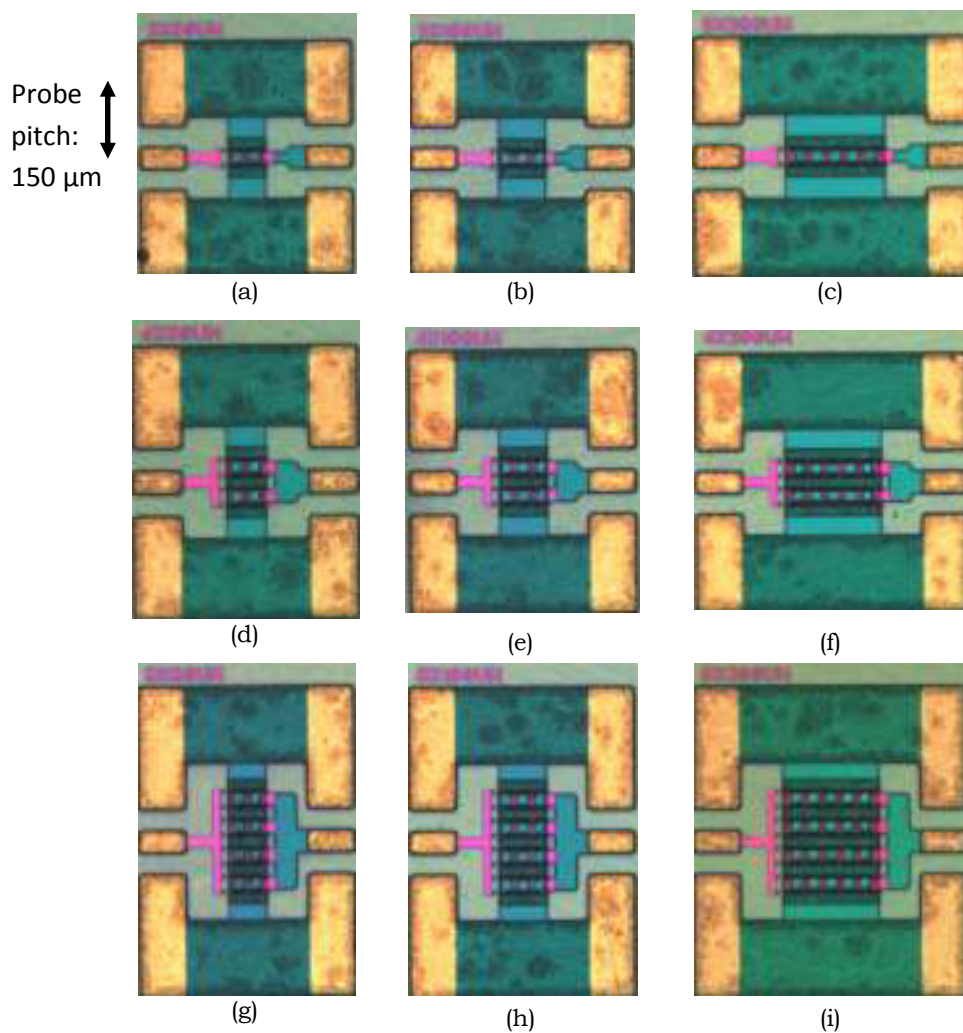


Figure 3-4: Photos of the transistors used in this work with varying widths and number of fingers (a) 2x80 μm (b) 2x100 μm (c) 2x200 μm (d) 4x80 μm (e) 4x100 μm (f) 4x200 μm (g) 8x80 μm (h) 8x100 μm (i) 8x200 μm .

3.2 Passive Circuit Determination

3.2.1 Introduction

Since scaling rules only apply at the intrinsic plane, this must first be established for this device structure. Unit cells of either a Y matrix (parallel pi) or a Z matrix (series T) form the building blocks to establish the complex circuit containing both the intrinsic and extrinsic elements. A general representation of a FET is basically made up of 3 unit cells, an outer Y matrix, a Z matrix and an inner Y matrix [9]. This is shown in Fig. 3-5.

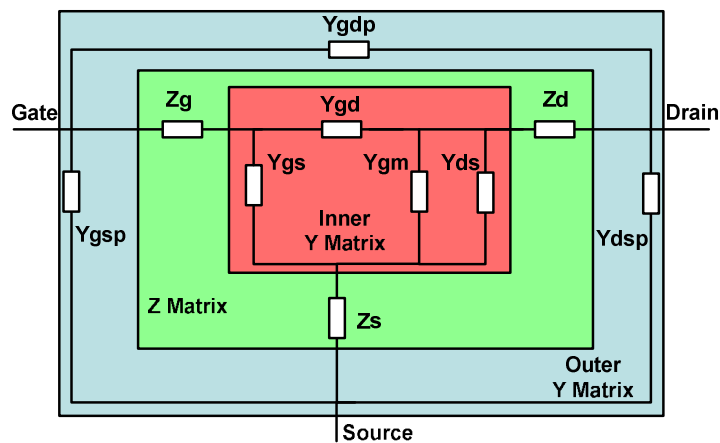


Figure 3-5: Equivalent circuit model for a FET transistor.

The outer Y-matrix is used to model the parasitic capacitances associated with the transistor layout such as pad capacitances and coupling capacitances. The Z-matrix is used to model the parasitic resistances such as the source, drain and gate resistances (from ungated regions of the active layer, contact resistance and layout metallization). It also includes the gate, drain and source inductances of the transistor layout. The inner Y matrix (an active Y-matrix) is a lump element representation of the non-linear distributive RC transmission line formed by the depletion region under the gate electrode and the conducting active channel.

By restricting the configurations to either a parallel pi for the Y-parameter or a series T for the Z-parameter, the frequency behaviour of the individual circuit components can be extracted independently and directly from measured S-parameter data. For example, for the passive Y matrix unit cell in Fig. 3-5,

$$y_{gsp} = y_{11} + y_{12} \quad y_{gdp} = -y_{12} \quad y_{dsp} = y_{22} + y_{12} \quad (3-4)$$

The circuit is passive so $y_{21} = y_{12}$. However, in the active Y matrix in Fig. 3-5 where $y_{21} \neq y_{12}$, the four admittance circuit components can be obtained by:

$$y_{gs} = y_{11} + y_{12} \quad y_{gd} = -y_{12} \quad (3-5)$$

$$y_{gm} = y_{22} + y_{12} \quad y_{ds} = y_{21} - y_{12} \quad (3-6)$$

In a Z matrix (series T) configuration, the 3 individual circuit components can be directly extracted from the measured data by:

$$z_g = z_{11} - z_{12} \quad z_s = z_{12} \quad z_d = z_{22} - z_{12} \quad (3-7)$$

In modelling FET structures, only passive Z-matrix topologies are considered where $z_{21} = z_{12}$. An active Z-matrix is needed only when modelling BJT [9].

From Fig. 3-5, it is clear that we need to be able to properly separate the various matrix elements. This can be done by performing measurements at special bias conditions to eliminate the effects of some of the matrix elements. For example, forward biasing the gate with zero drain bias so that the active Y-matrix can be eliminated. The systematic extraction process will be mentioned in the following sections and is based on techniques introduced by Tasker and Hughes [9] and Dambrine et al. [10].

In this work, S-parameter measurements were performed using a Rohde and Schwarz ZVA67 network analyser and controlled using the Keysight's VEE program using commands send via the VXI interface that has been developed

during this work. The screenshot of the VEE program is shown in Fig. 3-6(a)-(b).

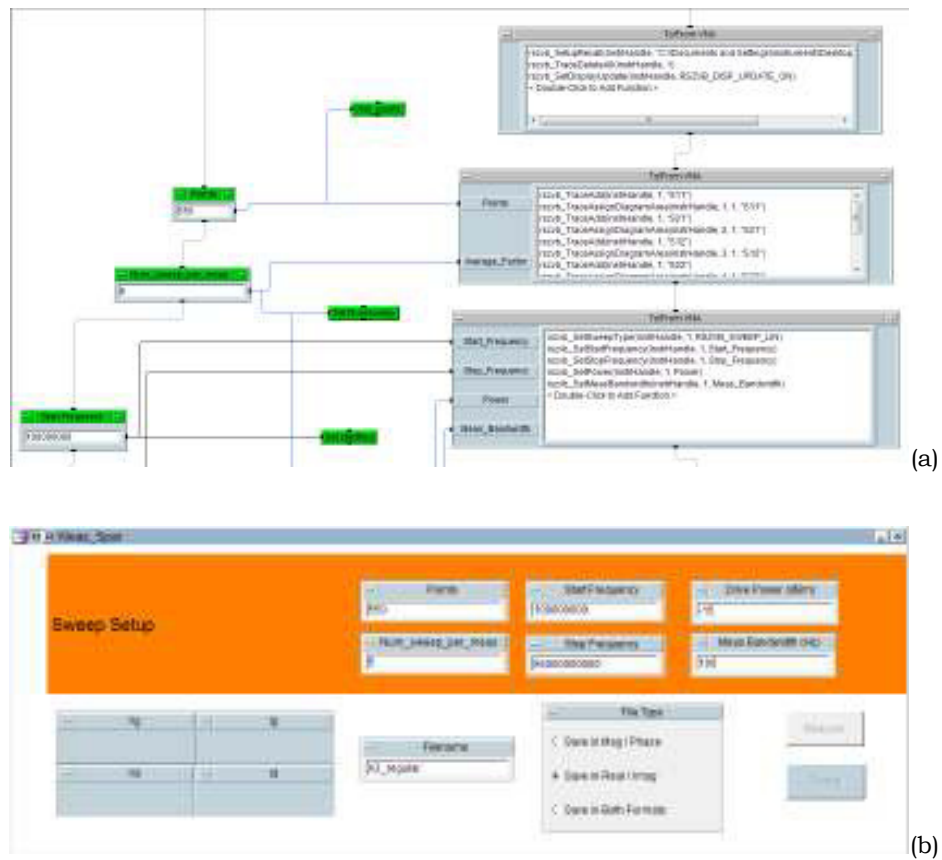
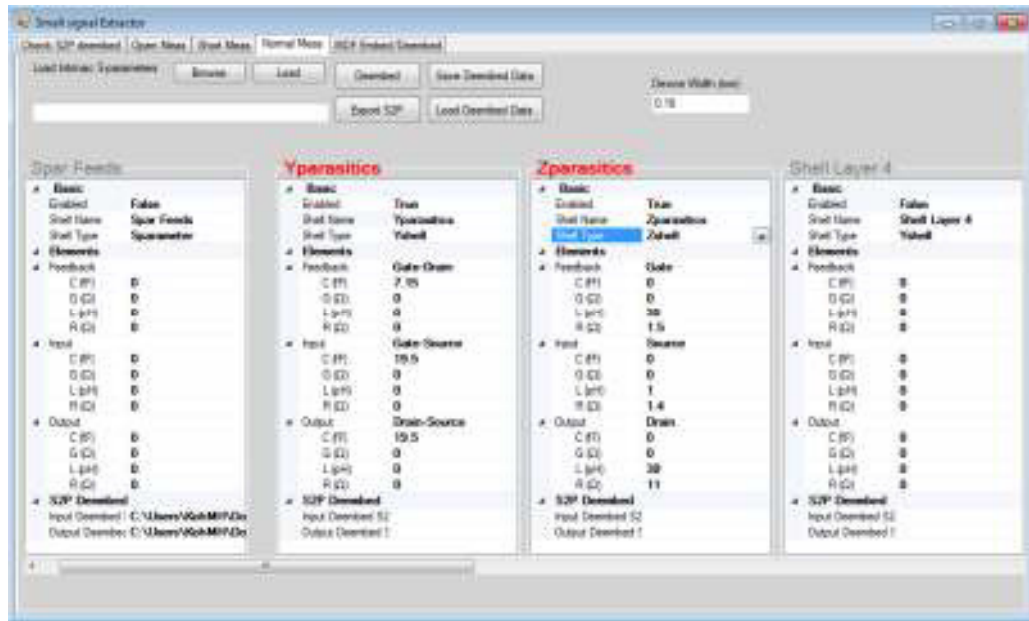


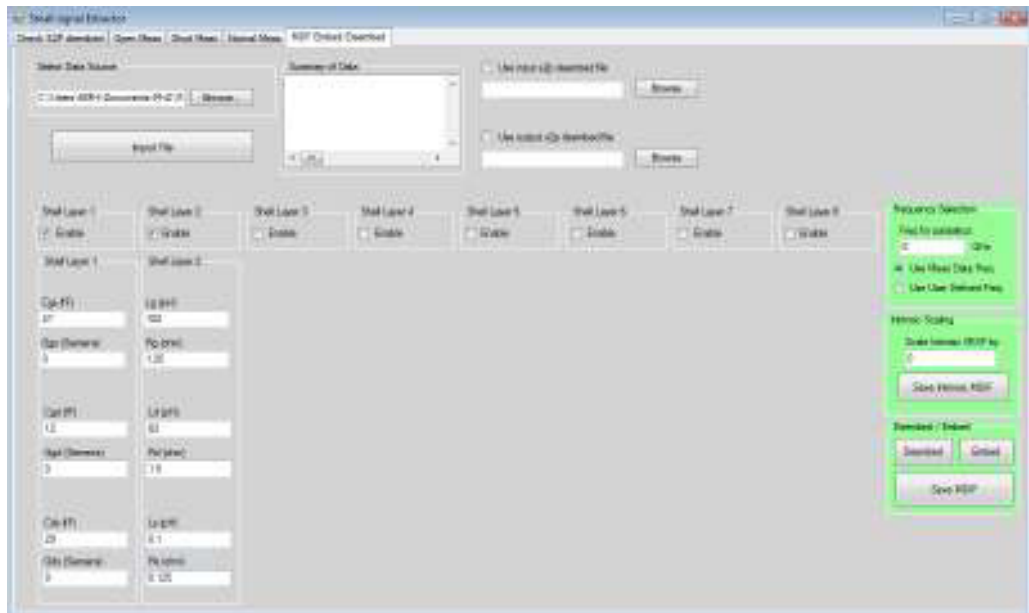
Figure 3-6: Screenshot of VEE program developed in this PhD for automated S-parameter measurements (a) 1st Partial screenshot of VEE program controlling ZVA67 (b) Front panel design for runtime.

The program allows the user to set a desired drain bias current. A software iteration loop that changes the gate bias voltage until the desired current is achieved.

A C# program has also been written during this PhD project that performs the de-embedding / embedding on the S-parameters to obtain the intrinsic transistor values. Fig. 3-7(a)-(b) shows the screenshot of the aforementioned C# program. This program is also able to perform the same process on large signal MDIF data.



(a)



(b)

Figure 3-7: Screenshot of C# program written to perform de-embedding / embedding (a) Using S-parameters (b) Using MDIF large-signal measurement data.

3.2.2 Y-Parasitic Determination

Measurements of the Y-parasitics are done on the devices shown in Fig. 3-4(a)-(i) at deep pinch-off and 0 V V_{ds} . The equivalent FET structure when measured at this operating condition is shown in Fig. 3- 8.

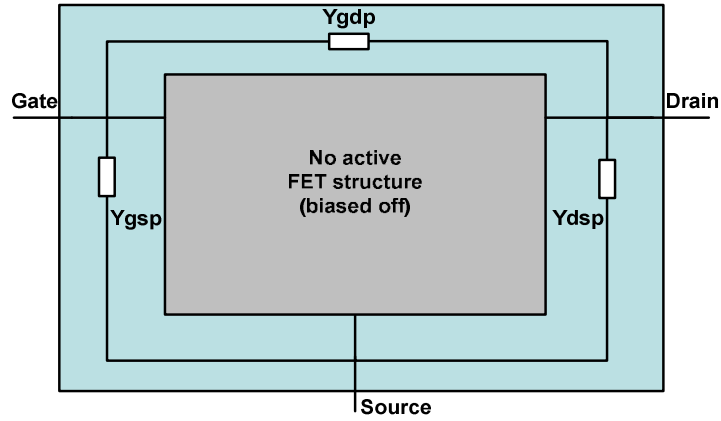


Figure 3-8: Equivalent FET structure for Y-parasitics determination

The Y-parasitics, which basically consists of the pad capacitances, are difficult to determine directly from measurements on the actual FET structure because they are in parallel with the transistor capacitances. Measuring with the device biased in pinch-off produces ambiguous results because of fringing capacitances. The best method of addressing this issue is by using measurements on FET structures with various widths.

$$y_{gsp} = y_{11} + y_{12} \quad c_{gsp} = \frac{\text{imag}\{y_{gsp}\}}{\omega} \quad (3-8)$$

$$y_{gdp} = -y_{12} \quad c_{gdp} = \frac{\text{imag}\{y_{gdp}\}}{\omega} \quad (3-9)$$

$$y_{dsp} = y_{22} + y_{12} \quad c_{dsp} = \frac{\text{imag}\{y_{dsp}\}}{\omega} \quad (3-10)$$

The extraction process for these pad capacitances is given in equation (3-8) to (3-10). The extraction results for the 2x80 μm transistor are shown in Fig. 3-9 showing typical behaviour where there is absence of significant variation in frequency.

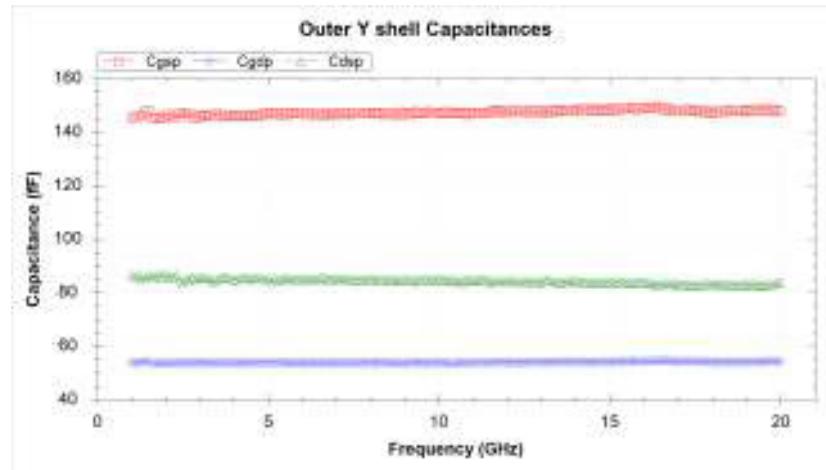
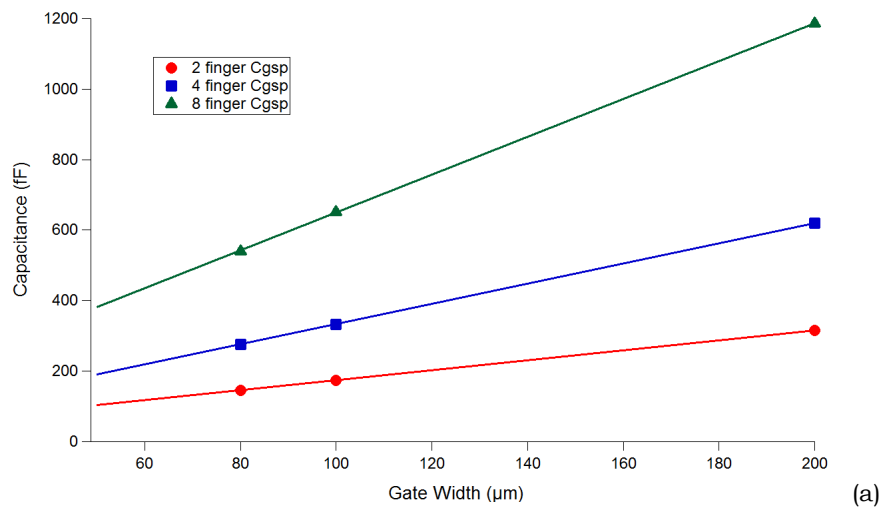


Figure 3-9: Outer Y shell capacitances as a function of frequency for the 2x80 μm device.

Taking the average of these plots, the results over width and number of fingers for the pad capacitances are plotted in Fig. 3-10. Do note that these results include capacitances of the active layer. Therefore, by curve-fitting the results, we can separate the constant intercept (pad capacitance) from the slope (due to active layer) as shown in Fig. 3-10.



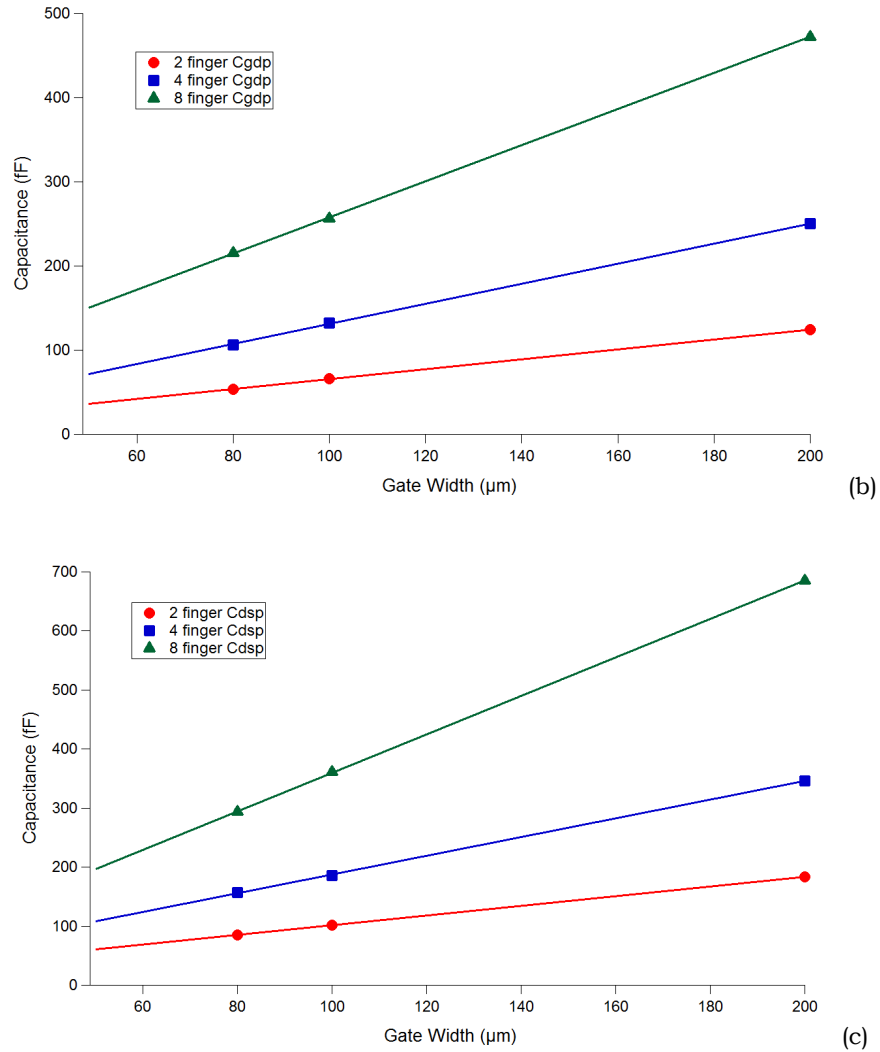


Figure 3-10: Outer Y shell capacitances for the 9 different devices (a) Cgsp (b) Cgdp (c) Cdsp.

3.2.3 Z-parasitic Determination

The Z-parasitic, which basically consists of the layout inductances and resistances, combined with the transistor parasitic resistances, can be measured by forward biasing the FET (at 0 V Vds). In these measurements, they consist of a combination of shells and in order to get the values of the inner unit shell, for example the Parasitic Z matrix, we must first strip the outer unit shell, which in this case are the Parasitic Y matrix.

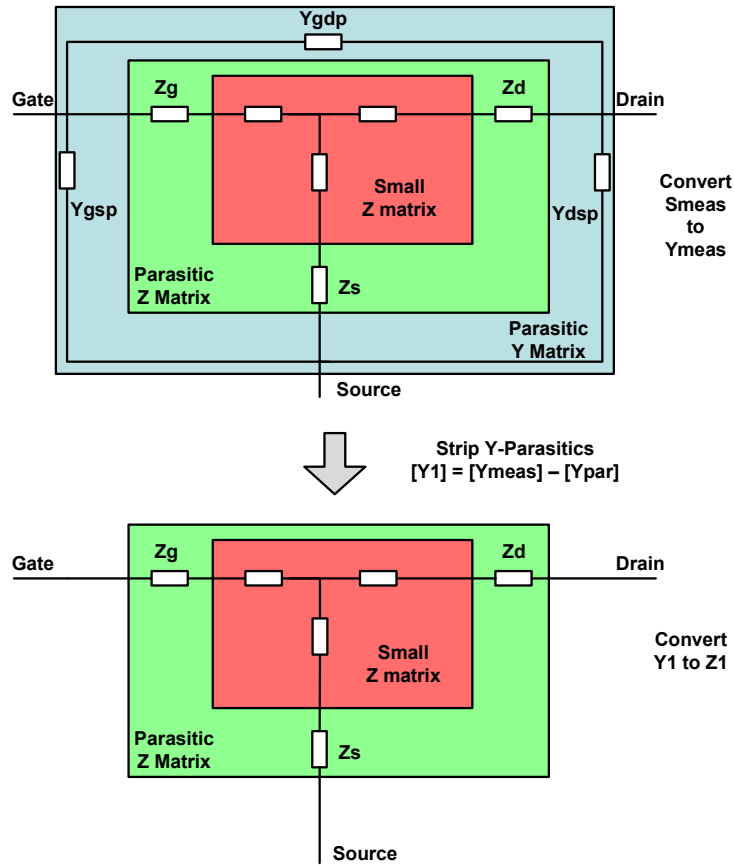


Figure 3-11: Process flow for determining Z-parasitics

This is achieved by just doing matrix subtraction. The value of FET resistances can be very small if a sufficiently high forward bias current is used and the gate length is small compared to source drain spacing.

$$z_g = z_{11} - z_{12} \quad r_g = \text{real}\{z_g\} \quad l_g = \frac{\text{imag}\{z_g\}}{\omega} \quad (3-11)$$

$$z_s = z_{12} \quad r_s = \text{real}\{z_s\} \quad l_s = \frac{\text{imag}\{z_s\}}{\omega} \quad (3-12)$$

$$z_d = z_{22} - z_{12} \quad r_d = \text{real}\{z_d\} \quad l_d = \frac{\text{imag}\{z_d\}}{\omega} \quad (3-13)$$

If we remove the effect of the outer parasitic Y shell, using the stripping technique shown in Fig. 3-11, then the measurement of the passive forward biased FET is assumed to be the Z parasitic alone. Measurements on the

passive forward bias FET transistor structures indicate that it can be modelled using series RL circuits components in the Z matrix. The extraction formulas are shown in equations (3-11) to (3-13). The results for the $2 \times 80 \mu\text{m}$ device is shown in Fig. 3-12(a)-(b) which indicates the absence of variation with frequency, an important criteria for turning these values into an equivalent circuit model.

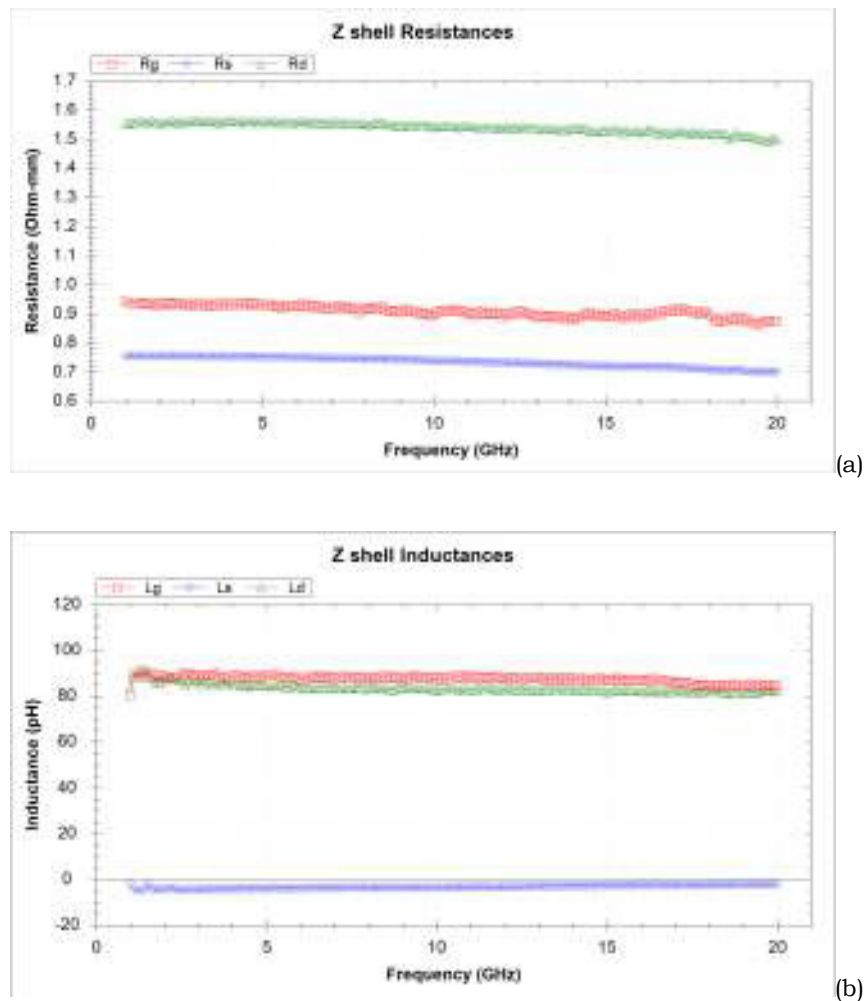


Figure 3-12: Extracted Z -parasitic values (a) resistances (b) inductances as a function of frequency for the $2 \times 80 \mu\text{m}$ device.

It is important to note that R_g and L_g are a strong function of gate current. A very high gate current is needed to satisfy the condition where the forward biased Z matrix is small compared to the Z parasitics. However, too high of a

forward gate current can degrade the transistor. Therefore, 3 values of gate current, 50mA/mm, 100mA/mm and 150 mA/mm are selected and the results for the 2x80 μm device with varying gate current is shown in Table 3-2.

Ig (mA/mm)	Rg (Ω -mm)	Lg (pH)	Rd (Ω -mm)	Ld (pH)	Rs (Ω -mm)	Ls (pH)
50	1.60	66.96	1.56	84.70	0.73	-4.02
100	1.10	83.59	1.56	83.63	0.74	-3.36
150	0.93	87.87	1.56	83.24	0.75	-3.29

Table 3-2: Values of Z-parasitics with varying gate current for 2x80 device.

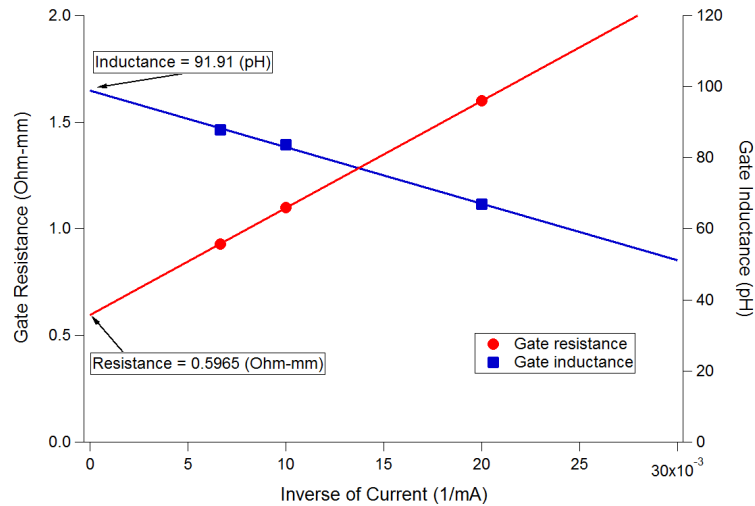


Figure 3-13: Extracted gate resistance and inductance as a function of inverse gate current for 2x80 μm device.

These values can be curve-fitted to the inverse of gate current as shown in Fig. 3-13, which negates the need for performing measurements at too high a gate current. The values for L_s is only an estimate and might be negative due to channel impedance.

3.2.4 Y-intrinsic Determination

The intrinsic FET circuit model consists of four components, y_{gs} (gate source input admittance), y_{gd} (gate drain feedback admittance), y_{ds} (drain source output admittance) and y_{gm} (transconductance admittance). These four components can be extracted from S-parameters after first converting to Y-parameters (and stripped).

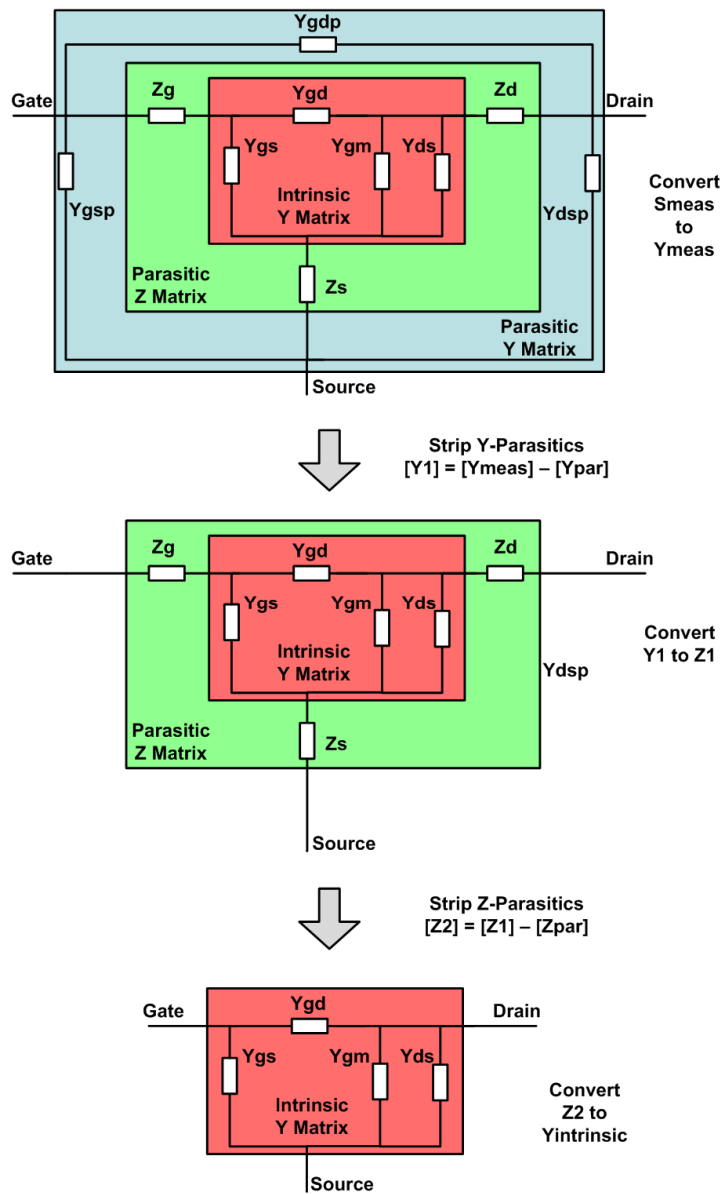


Figure 3-14: Process flow for determining Y-intrinsic values.

Confining the analysis to the first order circuit topologies, this constrains each element to a single real and imaginary component. Typically, y_{gs} and y_{gd} are modelled as a series RG circuit whereas y_{ds} is modelled as a parallel GC circuit. The transconductance is modelled as a voltage controlled current generator with a time (phase) delay. The elements are extracted as follows:

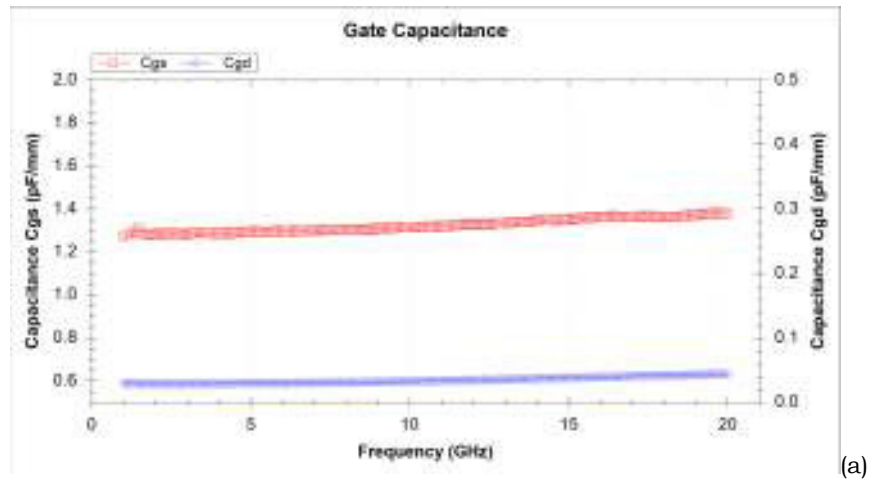
$$y_{gs} = y_{11} + y_{12} \quad r_{gs} = \text{real}\left(\frac{1}{y_{gs}}\right) \quad c_{gs} = \frac{-1}{\text{imag}\left(\frac{1}{y_{gs}}\right) \cdot \omega} \quad (3-14)$$

$$y_{gd} = -y_{12} \quad r_{gd} = \text{real}\left(\frac{1}{y_{gd}}\right) \quad c_{gd} = \frac{-1}{\text{imag}\left(\frac{1}{y_{gd}}\right) \cdot \omega} \quad (3-15)$$

$$y_{ds} = y_{22} + y_{12} \quad g_{ds} = \text{real}(y_{ds}) \quad c_{ds} = \frac{\text{imag}(y_{ds})}{\omega} \quad (3-16)$$

$$y_{gm} = y_{21} - y_{12} \quad g_m = g_{mo} \cdot e^{-j\omega\tau_{gm}} \quad (3-17)$$

$$g_{mo} = \text{mag}(y_{gm}) \quad \tau_{gm} = -\text{phase}(y_{gm}) \cdot \frac{1}{\omega} \quad (3-18)$$



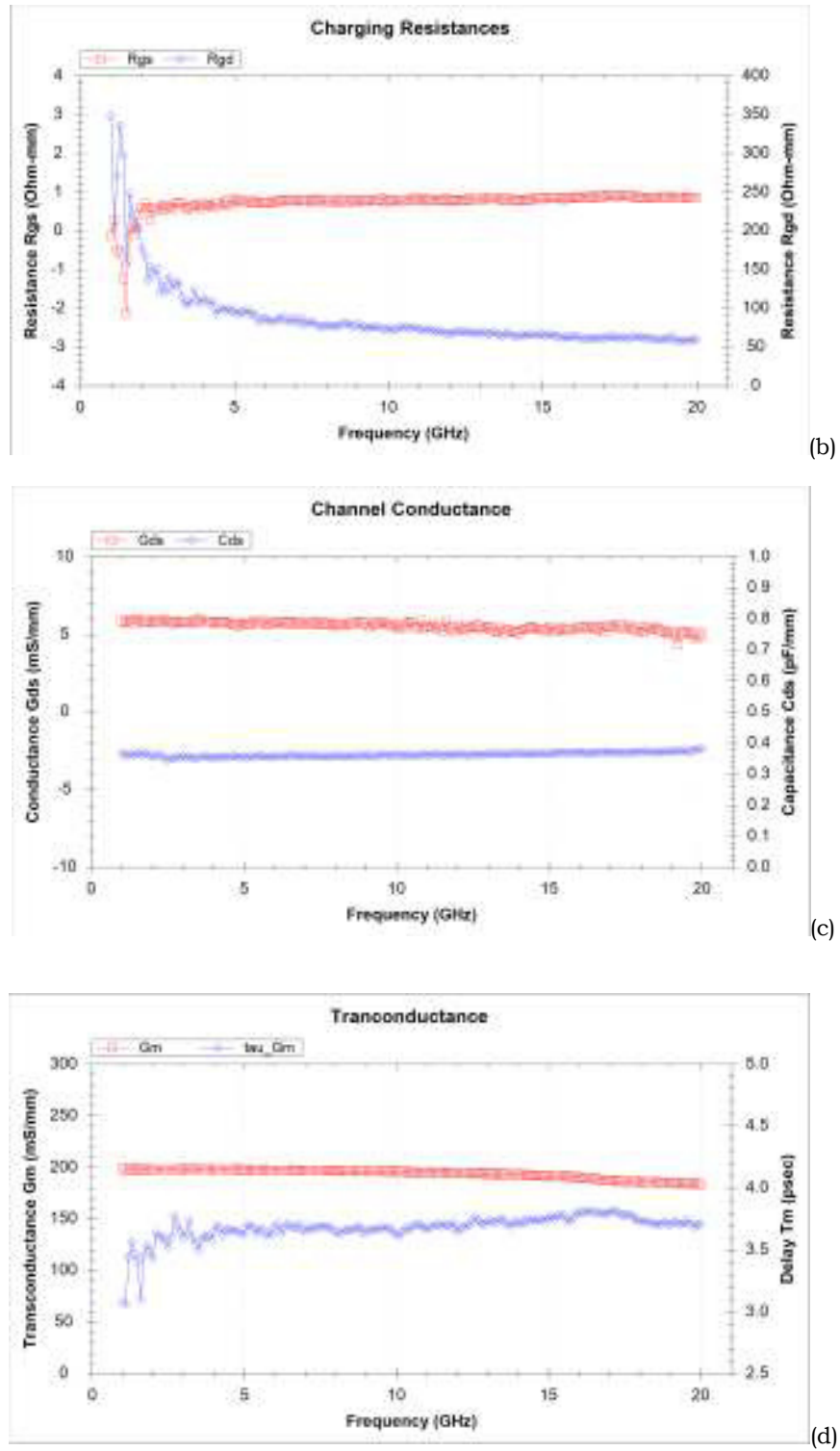


Figure 3-15: Extracted Y-intrinsic values as a function of frequency for 2x80 μm device (a) gate capacitances (b) charging resistances (c) conductance & drain-source capacitance (d) transconductance & delay.

The extracted values of the intrinsic components are basically independent of frequency as shown in Fig. 3-15, indicating the appropriate parasitic values have been extracted. The method mentioned allows for the parasitics to be extracted in a systematic manner.

3.2.5 Small signal model evaluation

All the devices in Table 3-1 were measured at the same drain current, $I_d = 50$ mA/mm. Theoretically, they should all have the same intrinsic transistor values.

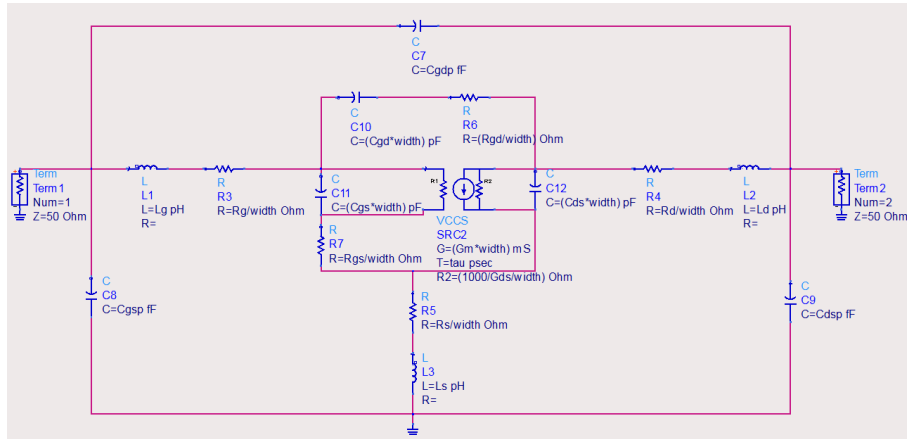


Figure 3-16: ADS circuit used for simulation of extracted component values.

To test whether we have de-embedded to the intrinsic plane accurately, the same intrinsic component values are used for all the devices but with different extrinsic values. The simulation is performed in ADS as shown in Fig. 3-16 and compared with measured S-parameter data. Table 3-3 includes all the parasitic and intrinsic values extracted from the cold FET measurement process.

Device /Value	Cgsp (fF)	Cgdp (fF)	Cdsp (fF)	Lg (pH)	Ld (pH)	Ls (pH)	Rg(Ω -mm)	Rd (Ω -mm)	Rs (Ω -mm)
2x80	33	6	21	106.5	91.5	0.05	0.15	0.45	0.0100
2x100	33	6	21	107.0	92.0	0.05	0.45	0.60	0.0125
2x200	33	6	21	109.5	94.5	0.05	1.90	1.30	0.0250
4x80	47	12	29	101.5	81.5	0.10	0.35	0.45	0.0400
4x100	47	12	29	102.0	82.0	0.10	0.50	0.60	0.0500
4x200	47	12	29	104.5	84.5	0.10	2.20	1.30	0.1000
8x80	107	38	32	100.0	80.0	0.20	0.90	0.45	0.1600
8x100	107	38	32	100.5	80.5	0.20	1.25	0.60	0.2000
8x200	107	38	32	103.0	83.0	0.20	3.20	1.30	0.4000

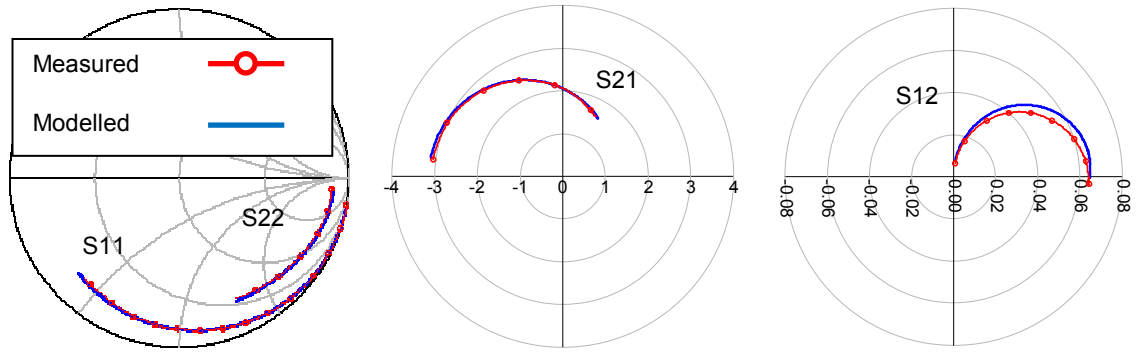
Table 3-3: Values of parasitics components for ADS simulation.

This process is essentially the same as the process flow shown in Fig. 3-3 but with small signal data. The reason this step is performed is to ensure that we have obtained the correct parasitic values as well as to show that the flow in Fig. 3-3 works at small signal power levels. These parasitic values are needed for de-embedding the large-signal data for the scalable Behavioural Model and crucial to the modelling process.

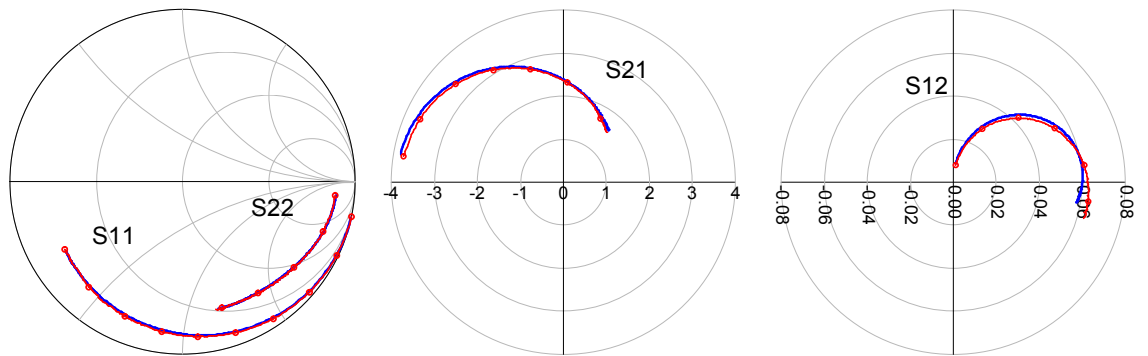
Cgs (pF/mm)	Rgs (Ω -mm)	Cgd (pF/mm)	Cds (pF/mm)	Gm (mS/mm)	Tau (psec)	Gds (mS/mm)
1.3	0.8	0.045	0.36	205	2.5	5.7

Table 3-4: Values of Y-intrinsic components for ADS simulation.

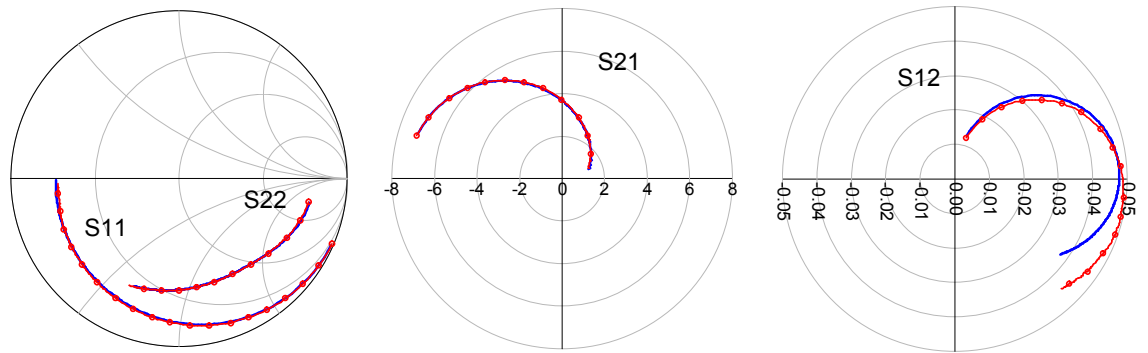
Table 3-4 are the values for the intrinsic components at $I_d = 50$ mA/mm. The results of this simulation and comparison with measured data are shown in Fig. 3-17(a)-(i).



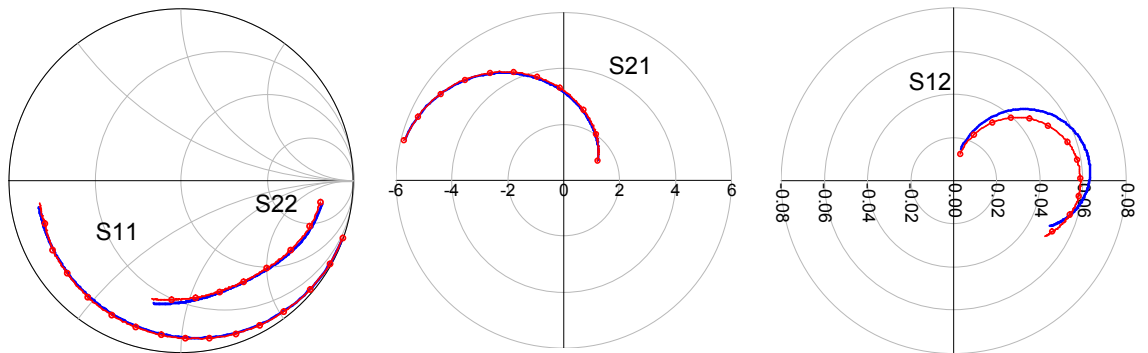
(a)



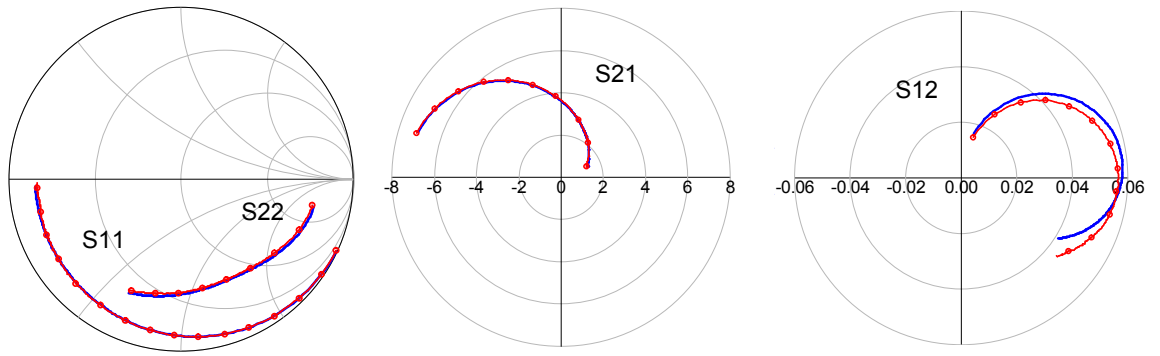
(b)



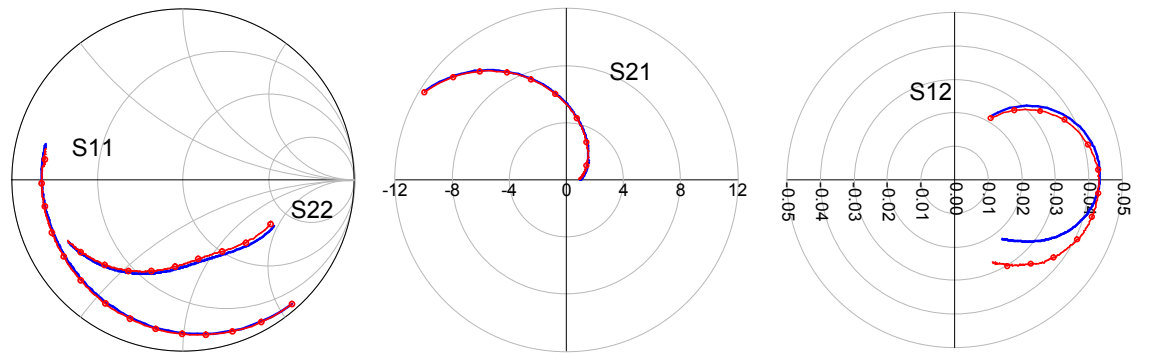
(c)



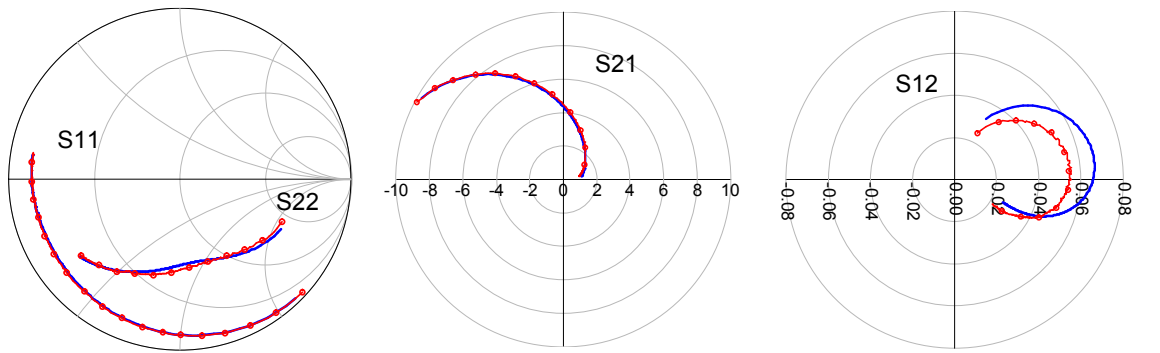
(d)



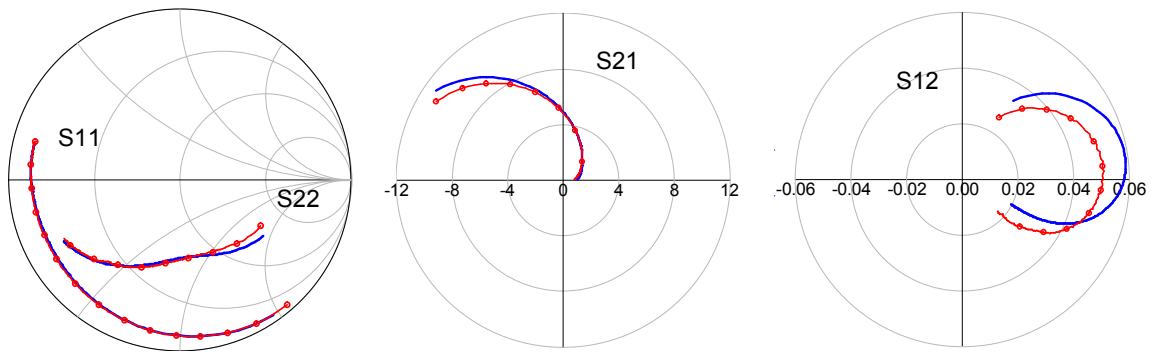
(e)



(f)



(g)



(h)

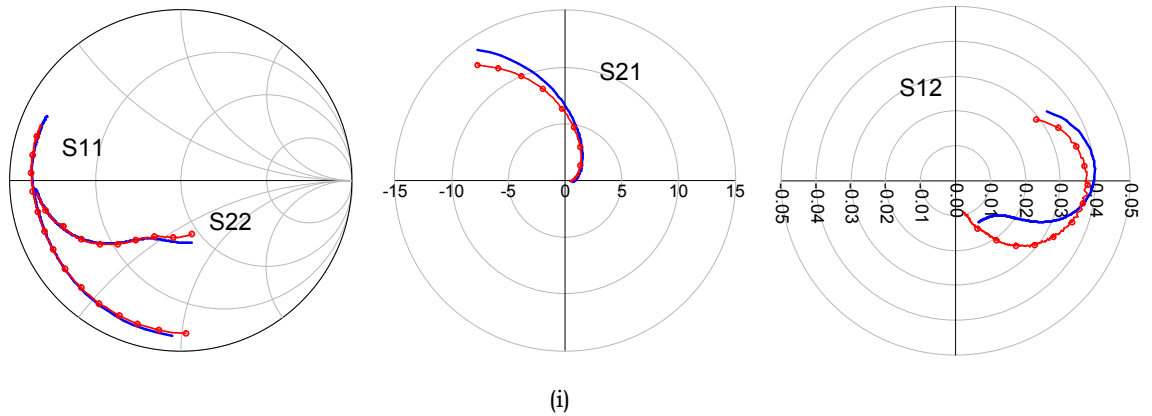


Figure 3-17: Measured versus modelled results of S-parameters from 1 - 20 GHz obtained at $I_d=50$ mA/mm. (a) 2x80 μm device (b) 2x100 μm device (c) 2x200 μm device (d) 4x80 μm device (e) 4x100 μm device (f) 4x200 μm device (g) 8x80 μm device (h) 8x100 μm device (i) 8x200 μm device

At this juncture, measurements for all the devices were repeated but with a different drain current, $I_d = 150\text{mA/mm}$. In theory, only the intrinsic portion should change and the same values for the extrinsic components are maintained. Please refer to Appendix A.1 for the full results, which acts as another validation that the parasitics were extracted correctly.

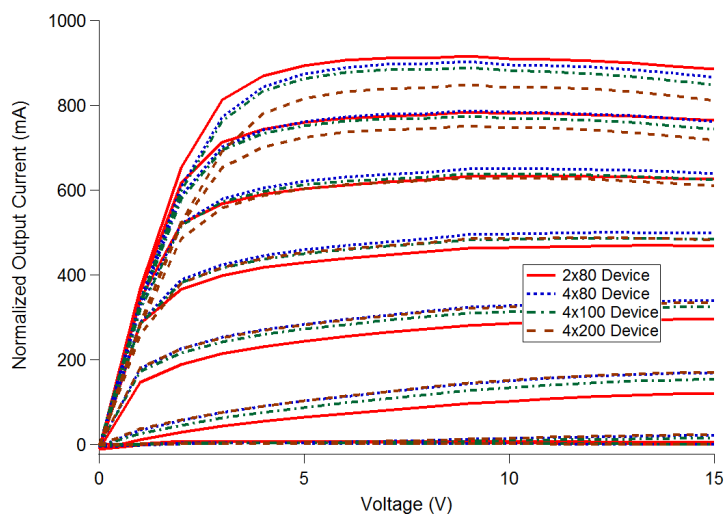


Figure 3-18: DCIV results for 4 different device sizes (gate periphery).

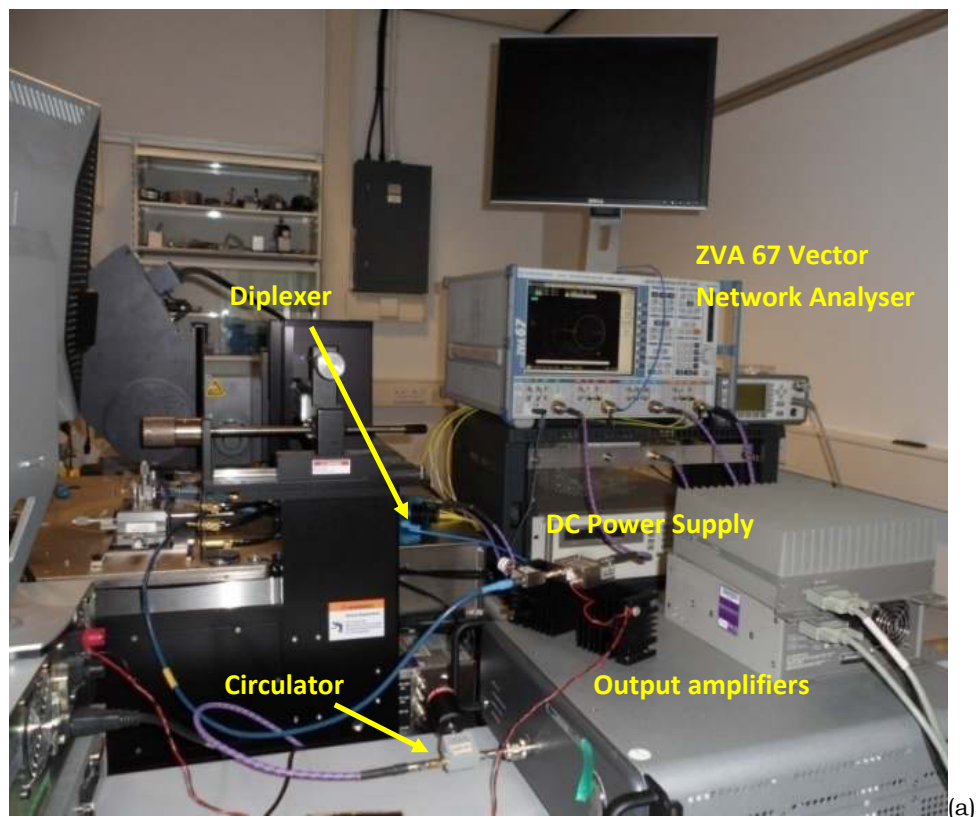
Before attempting to develop a scalable model, an important indicator of scalability is also to look at the DCIV curves for the several devices where

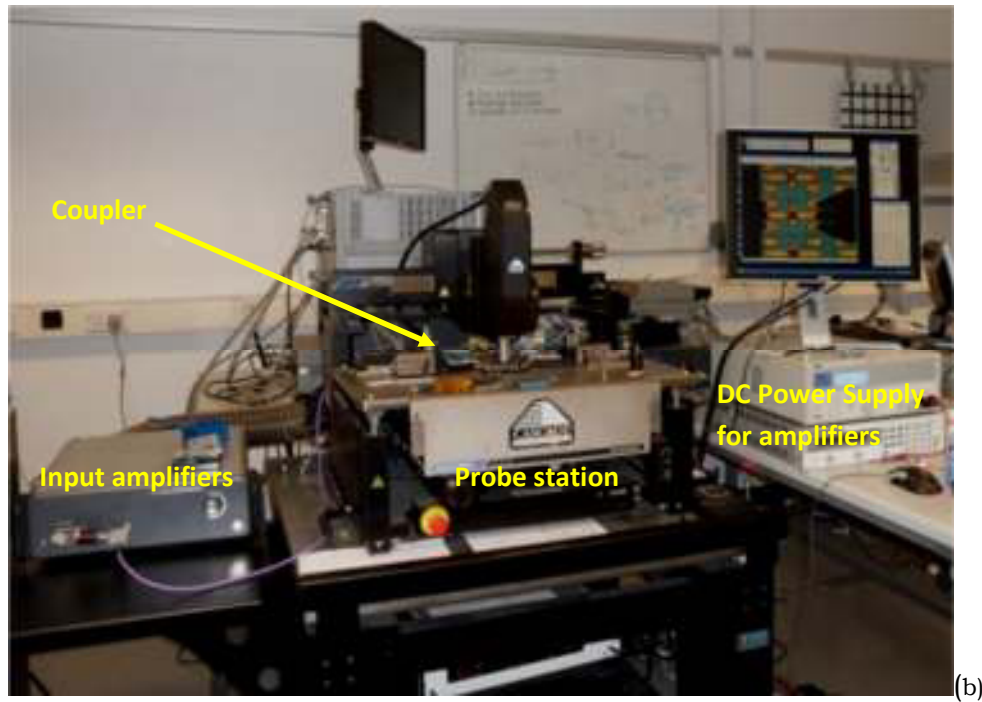
scaling will be applied. As expected, the DCIV start to shrink as we move up in device size due to self-heating. If the DCIV shrinks beyond a certain limit, equation (3-1) will not hold and therefore the model will not be able to scale accurately. From the DCIV results in Fig. 3-18, the output drain current scales within reasonable values when moving to a device up to 5 times larger.

3.3 Large Signal Model Extraction

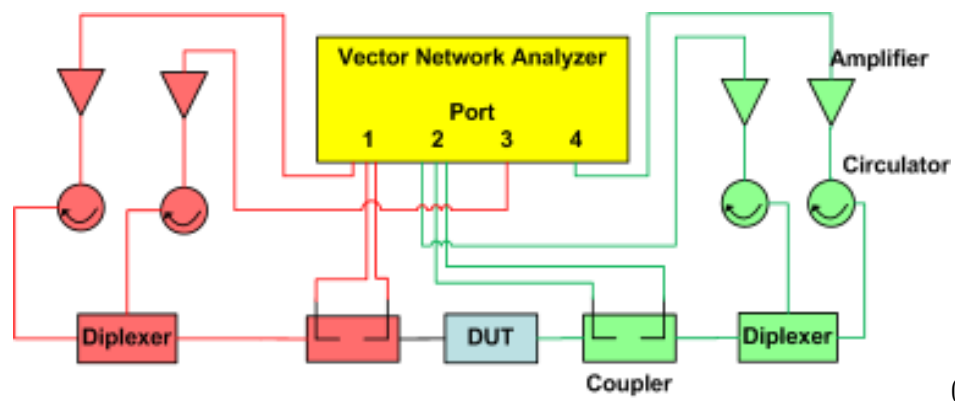
The second step in the modelling process as described in Fig. 3-3 is to perform large signal measurements on the reference device for conversion into the behavioral model. This section will explain in detail the steps and practical considerations that were taken into account.

3.3.1 Large Signal Measurement Setup





(b)



(c)

Figure 3-19: Active load-pull setup for large signal measurements (a) Side photo of setup in Cardiff University (b) Front photo of setup in Cardiff University (c) Diagram depicting measurement setup.

Measurements were performed at a fundamental frequency of 5 GHz using the high frequency measurement system with an active load-pull architecture shown in Fig. 3-19(a)-(c). The system uses a Rhode and Schwarz ZVA67 Vector Network Analyser with a 67 GHz bandwidth as a receiver and configured to perform non-linear time domain waveform measurements.

The ZVA67 instrument is a commercially available instrument that contains four high frequency sources, with independent control over magnitude, phase and frequency of each source, thus making it ideal for use in high frequency active load-pull systems [5]-[8]. The waveforms measured by the ZVA67 are fully phase synchronised by using an external phase reference using a phase reference calibration described in [13].

As shown in Fig. 3-19, the measurement system uses external couplers that are placed close to the DUT to reduce the loss that can be introduced by using long RF cables, increasing the dynamic range of the measurements. Circulators are used to ensure that the output waves from the DUT maintain a constant impedance environment for the system amplifiers and also prevent damage.

Note that load-pull systems can either be passive or active. The reflection coefficient presented to the DUT at a given load, Γ_L is the ratio between reflected wave, a_2 and the forward travelling wave, b_2 . Passive load termination is implemented by using a slide-screw tuner which consists of a 50 ohm slabline with 2 parallel plates, a centre conductor and a metallic probe [15]. As the probe is lowered onto the slabline, part of the signal is reflected towards the DUT and the magnitude of reflection increases. By moving the probe, the impedance presented to the DUT can be varied.

With active load-pull, instead of using passive tuners to reflect the signal back to the DUT, the signal can be adjusted in magnitude and phase and fed back (closed-loop active load-pull) [14]-[15] or a new signal can be injected at the output of the device to synthesize an impedance (open-loop active load-pull) [16]-[17]. The contrast between closed-loop and active-loop load-pull is depicted in Fig 3-20(a)-(b).

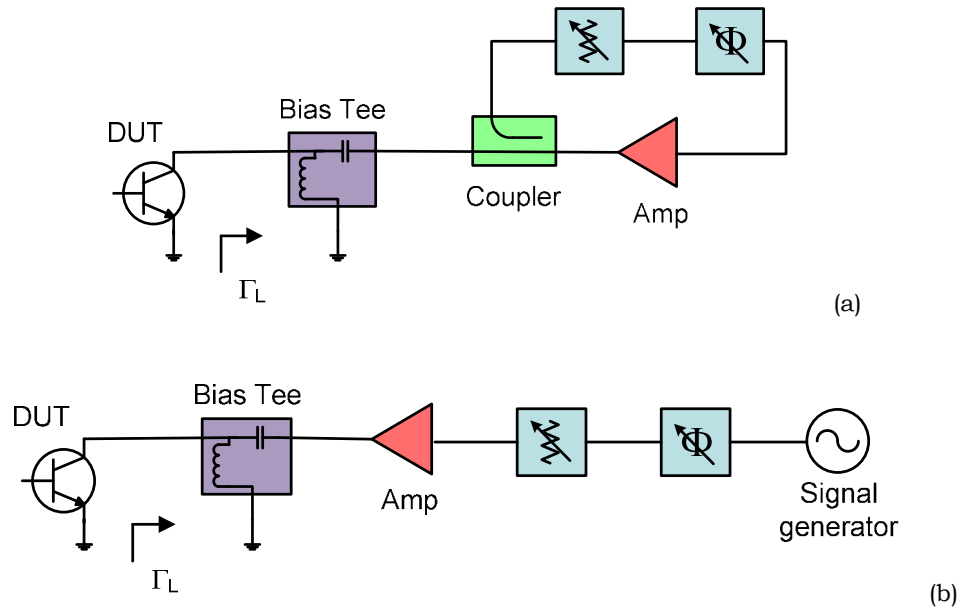


Figure 3-20: Active load-pull implementation (a) Closed-loop setup (b) Open-loop setup [15].

Closed-loop active load-pull does not require a separate signal source for injection but due to its close-loop nature, oscillations may occur during measurements whereas open-loop active load-pull is easier to implement and safe from oscillations. However, an open-loop active load-pull setup will require additional signal sources and larger amplifiers. The measurement system used in this work can be classified as an open-loop active load-pull system.

The initial calibration and set up time for passive load-pull is long but once it is completed, the user would only have to wait for the fast mechanical action of the tuner. On the other hand, active load-pull systems iterate towards the desired load and depending on the algorithm, this can be much slower in comparison to passive load-pull. Nevertheless, its advantage is that it does not suffer from the detrimental effect of system losses and can target loads at the edge of the Smith Chart [18]. Active load-pull also ensures that the 2nd harmonic can be set to a short circuit whereas this condition may not be achievable with passive load-pull tuner.

In this work, the 2x80 μm reference device was biased in a Class B mode of operation, at a drain voltage of 28 V. To achieve optimal Class B behaviour, second harmonic short circuits at the intrinsic device reference plane, are presented at both the input and output.

Fundamental load-pull measurements were performed at 5 GHz to encompass both the optimum P_{out} and Drain efficiency locations (covering at least a 3 dB load-pull space from the optimum), and repeated at different input power levels to provide a range of incident fundamental normalized wave at port 1, ($|A_{11}|$) values.

Knowing the parasitic component values grants us the advantage of predicting the location of the optimum point and the load-pull space with which to measure for the larger devices from the smaller reference device. The grid is ensured to cover at least the 3 dB P_{out} space from the optimum. The load-pull grids for the 2x80 μm , 4x100 μm and 4x200 μm device are shown in Fig. 3-21(a)-(c).

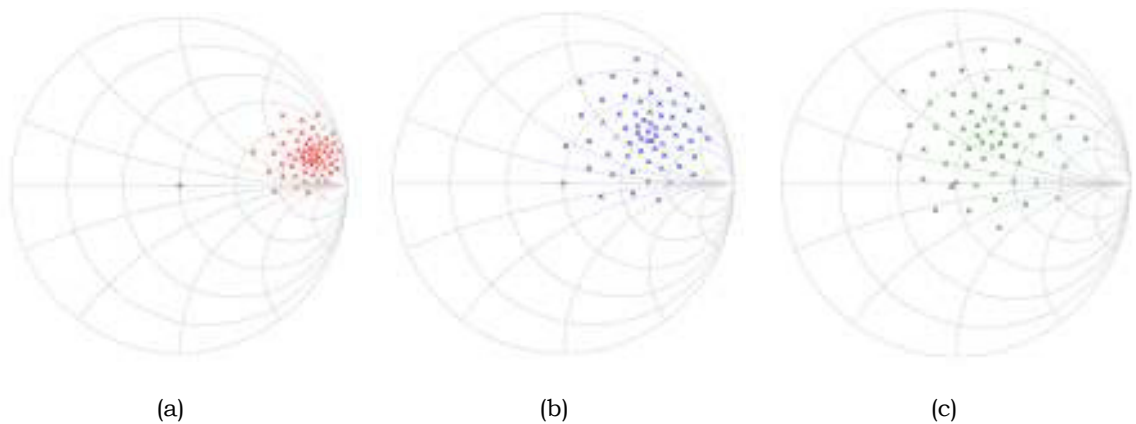


Figure 3-21: Load-pull measurement grids for (a) 2x80 μm (b) 4x100 μm (c) 4x200 μm device.

The 4x100 μm and 4x200 μm device measurements will act as the validation for the scalable model and it is important to note that they are not used in the modelling process. For example, the modelled results for the 4x100 μm device

will not be based on measurements from the device itself but from the scaled prediction from the 2x80 μm reference device.

3.3.2 Extraction of Model Coefficients

The parameters of the large signal model were extracted to populate data tables; data look-up as a function of $|A_{1,1}|$. The Cardiff Model [3]-[8] uses a generalized Behavioural model formulation that is based on the Polyharmonic Distortion principles described in [19]-[21]. With only fundamental load-pull for a fixed DC condition, the measured B waves can be described as:

$$B_{p,h} = P_1^h \cdot f\left(v_{1,0}, |a_{1,1}|, v_{2,0}, \frac{A_{2,1}}{P_1}\right) \quad (3-19)$$

where $P_1 = \angle A_{1,1} = A_{1,1}/|A_{1,1}|$. With the work of Qi et al. [3]-[4] and Woodington et al. [5]-[6], the indexing of $A_{2,1}$ can now be in the polar form as describe by equation (3-20).

$$B_{p,h} = P_1^h \cdot f\left(v_{1,0}, |A_{1,1}|, v_{2,0}, |A_{2,1}|, \frac{Q_1}{P_1}\right) \quad (3-20)$$

where $Q_1 = \angle A_{2,1} = A_{2,1}/|A_{2,1}|$. At this point, load-pull indexing terms have become $|A_{2,1}|$ and Q_1/P_1 .

Since the phase vector Q_1/P_1 is a periodic function, the measured behaviour $B_{p,h}$ must also be periodic with reference to this variable. Hence, the Fourier series concept can be applied with respect to phase vector Q_1/P_1 to eliminate the phase vector indexing and replace it with

$$B_{p,h} = P_1^h \cdot \sum_{n=-r}^{n=+r} K_{p,h,n} \left(\frac{Q_1}{P_1}\right)^n \quad (3-21)$$

where $K_{p,h,m} = g(v_{1,0}, |A_{1,1}|, v_{2,0}, |A_{2,1}|)$. This approach has been experimentally verified in [5]-[6]. The coefficients $K_{p,h,m}$ and its complexity (number of coefficients), r can be determined by performing a least-squares fit to a measured data set or by Fourier transforming an appropriately structured measurement sequence. Replacing $B_{p,h}$ with $K_{p,h,m}$ in the data tables eliminates the phase vector indexing.

Tasker et al. achieved further compression of the data tables by including the variation of the coefficients $K_{p,h,m}$ as a function of $|A_{2,1}|$ [8]. We can model this behaviour using simple polynomial functions to eliminate the $|A_{2,1}|$ indexing.

$$K_{p,h,n} = \sum_{m=0}^{m=q} M_{p,h,m,n} |A_{2,1}|^{2m+|n|} \quad (3-22)$$

where $M_{p,h,m,n} = f(v_{1,0}, |A_{1,1}|, v_{2,0})$. By having the coefficients in this form, the Behavioural model formulation has eliminated the dependence on load and can interpolate in both polar coordinates $|A_{2,1}|$ and Q_1/P_1 . Substituting eqn. (3-22) into (3-21) results in

$$B_{p,h} = P_1^h \cdot \left\{ \sum_{n=-r}^{n=+r} \sum_{m=0}^{m=q} M_{p,h,m,n} |A_{2,1}|^{2m+|n|} \left(\frac{Q_1}{P_1} \right)^n \right\} \quad (3-23)$$

Based on previous work by Simon Woodington and James Bell [5]-[7], the coefficients increase in complexity in the form of a mixing model. In order to determine the number of terms needed to accurately represent the measurement data, the data is extracted with 3, 6 or 9 coefficients as shown in Table 3-5.

The first 3 coefficients ($M_{p,h,0,-1}$, $M_{p,h,0,0}$ and $M_{p,h,0,1}$), in the model are equivalent to the X-parameters (X_T , X_F and X_S). Just using these alone will give a

Behavioural model that is only able to map a small space in the load-pull grid. Therefore, to cover a large impedance space the X-parameters must be load dependent [22] whereas the generalized Behavioural model equation (Cardiff Model) is able to map the entire load-pull space [8]. This is the fundamental difference between X-parameters and the Cardiff Model.

Number of Coeff.	Equation for extraction
3	$\frac{B_{p,h}}{P_1^h} = \left\{ M_{p,h,0,-1} A_{2,1} \left(\frac{Q_1}{P_1}\right)^{-1} + M_{p,h,0,0} + M_{p,h,0,1} A_{2,1} \left(\frac{Q_1}{P_1}\right) \right\}$
6	$\frac{B_{p,h}}{P_1^h} = \left\{ \begin{array}{l} M_{p,h,0,-2} A_{2,1} ^2 \left(\frac{Q_1}{P_1}\right)^{-2} + M_{p,h,0,-1} A_{2,1} \left(\frac{Q_1}{P_1}\right)^{-1} + M_{p,h,0,0} \\ + M_{p,h,0,1} A_{2,1} \left(\frac{Q_1}{P_1}\right) + M_{p,h,0,2} A_{2,1} ^2 \left(\frac{Q_1}{P_1}\right)^2 + M_{p,h,1,0} A_{2,1} ^2 \end{array} \right\}$
9	$\frac{B_{p,h}}{P_1^h} = \left\{ \begin{array}{l} M_{p,h,0,-2} A_{2,1} ^2 \left(\frac{Q_1}{P_1}\right)^{-2} + M_{p,h,0,-1} A_{2,1} \left(\frac{Q_1}{P_1}\right)^{-1} + M_{p,h,0,0} \\ + M_{p,h,0,1} A_{2,1} \left(\frac{Q_1}{P_1}\right) + M_{p,h,0,2} A_{2,1} ^2 \left(\frac{Q_1}{P_1}\right)^2 + M_{p,h,1,-1} A_{2,1} ^3 \left(\frac{Q_1}{P_1}\right)^{-1} \\ + M_{p,h,1,0} A_{2,1} ^2 + M_{p,h,1,1} A_{2,1} ^3 \left(\frac{Q_1}{P_1}\right) + M_{p,h,2,0} A_{2,1} ^4 \end{array} \right\}$

Table 3-5: Cardiff Model equation with 3, 6 and 9 coefficient terms.

The normalized mean square error (NMSE) provides a good representation of model accuracy [23] and can be calculated using eqn. (3-24).

$$NMSE(dB) = 10 \log_{10} \frac{\sum_n |b_{meas}(n) - b_{model}(n)|^2}{\sum_n |b_{meas}(n)|^2} \quad (3-24)$$

The NMSE for B_{21} and B_{22} extracted based on the coefficients in Table 3-5 is shown in Fig. 3-22. From the results, it is obvious that the NMSE reduces when using more coefficients. Nevertheless, the NMSE in B_{21} extraction is better than -40 dB when using the 6 term Cardiff Model and the improvement

when using a 9 term model is very small. The NMSE in B_{22} is larger due to the smaller values of 2nd harmonic signals.

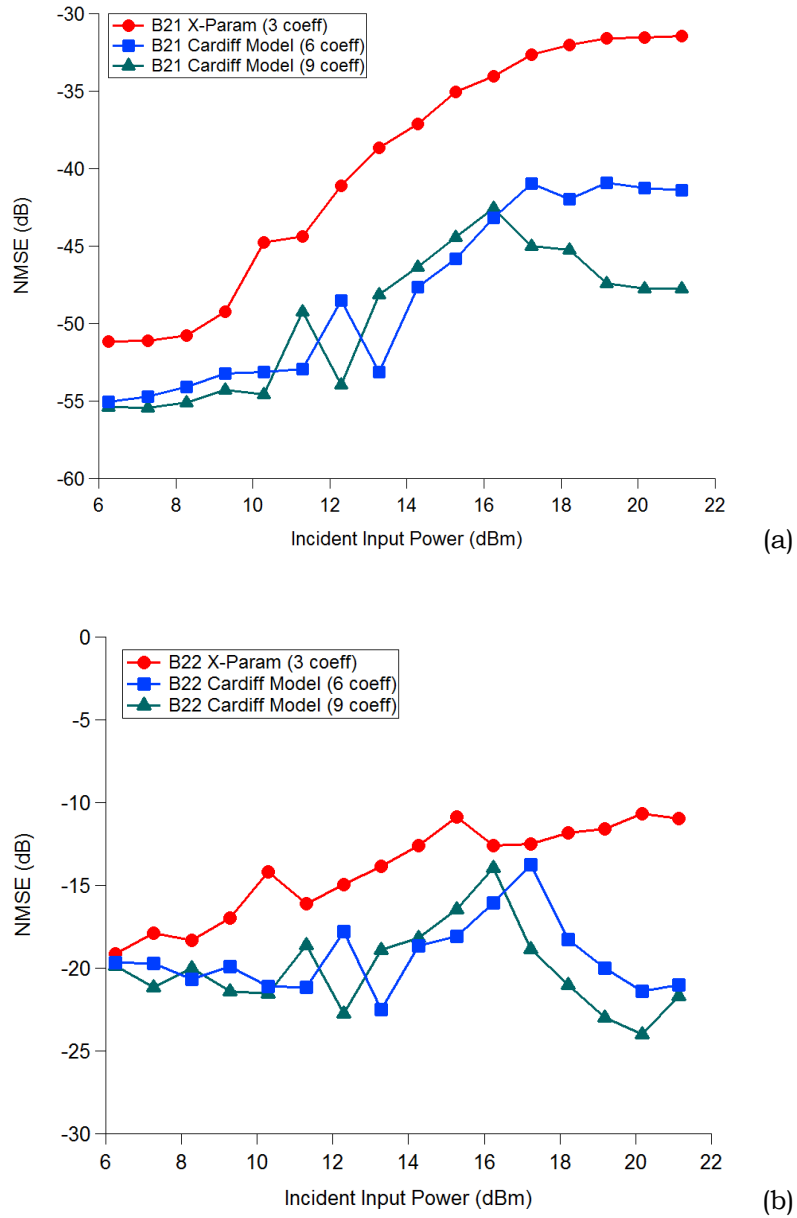


Figure 3-22: NMSE for B waves extracted with X-parameters, Cardiff 6 term and 9 term model (a) B_{21} (b) B_{22}

Therefore, since the measurement data contains only fundamental $B_{p,h}$ waves with fixed 2nd harmonic loads, a Behavioural model with 6 coefficients is sufficient to accurately represent it. This is consistent with previous work that

conclude that a low model complexity is sufficient to model fundamental load-pull [5],[24].

Having a model that is too complex will cause it to fold back on itself. In other words, instead of having a model whose power rolls off as we back-off the input power, it may converge to a value which gets larger, a physically impossible characteristic for the transistor. Furthermore, having too many terms (model coefficients) will cause over-fitting and the model will be "memorizing" the value of the terms and fitting to noise values in the data [25].

As mentioned in the introduction, in previous work by David Root, geometric model scaling has been established for the X-parameters, which has 3 terms X_F , X_S and X_T [2]. In this work, we extend it to the 6 term Cardiff Model (shown in equation 3-25).

$$\begin{aligned}
 & B_{p,h} \\
 &= P_1^h \left\{ \begin{array}{l} M_{p,h,0,-2} |A_{2,1}|^2 \left(\frac{Q_1}{P_1}\right)^{-2} + M_{p,h,0,-1} |A_{2,1}| \left(\frac{Q_1}{P_1}\right)^{-1} + M_{p,h,0,0} \\ + M_{p,h,0,1} |A_{2,1}| \left(\frac{Q_1}{P_1}\right) + M_{p,h,0,2} |A_{2,1}|^2 \left(\frac{Q_1}{P_1}\right)^2 + M_{p,h,1,0} |A_{2,1}|^2 \end{array} \right\}
 \end{aligned}
 \tag{3-25}$$

The X-Parameter and the Cardiff 6 term model coefficients as a function of phase is shown in Fig. 3-23 where the size of the dots represents of the magnitude of the coefficients. As can be seen in Fig. 3-23, the dominant terms are the $M_{p,h,0,0}$, $M_{p,h,0,1}$ and $M_{p,h,0,-1}$ which are essentially the X-parameters. X-parameters coefficients (in red) are a subset of the Cardiff Model (additional terms are in black). Note that $M_{p,h,0,0}$ and $M_{p,h,1,0}$ have the same phase location. The coefficient $M_{p,h,1,0}$ adds a squared dependency on the magnitude of $A_{2,1}$.

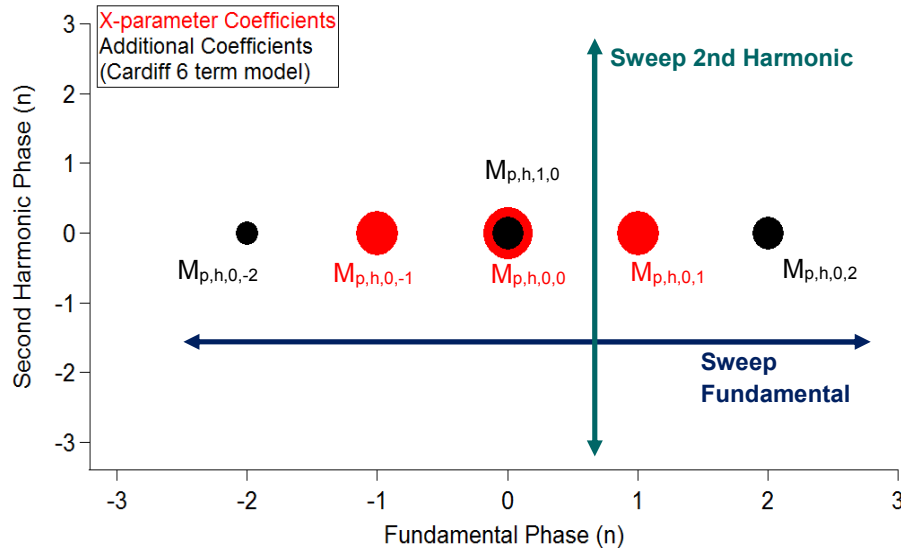


Figure 3-23: Coefficients used in the model extraction as a function of phase.

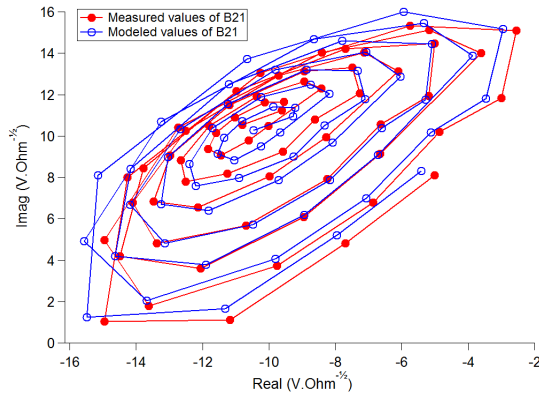
In this work, only the fundamental is swept with a fixed 2nd harmonic, hence the usage of terms in the fundamental space only (along the blue line). If we would include the model with 2nd harmonic variation, coefficients along the green line would appear [7] in Fig. 3-23.

Fig. 3-24(a)-(d) shows a comparison of the B_{21} values when computed with first 3 terms of the Cardiff Model (the X-parameter equivalent model) versus the 6 terms of the Cardiff Model. From these results, it is clear that extracting with the 6 term Cardiff model produces a better model and is sufficient to map any variation in B_{21} . Keep in mind that X-parameters are able to model the points over the entire load space accurately but only if made to be load dependent.

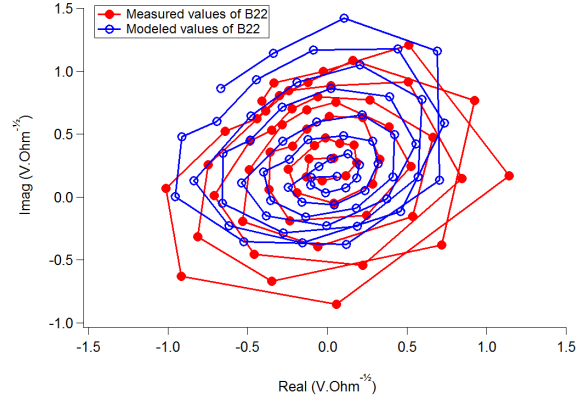
Coefficients for B_{23} are also extracted and included in the model but since we do not control the 3rd harmonic in the measurements (left at 50 ohms), the scaled model will not be able to predict the 3rd harmonic accurately. It should be noted that this is because while the system impedance remains constant, the intrinsic impedance it presents to the unit cell will vary as the device geometry is scaled. The 3rd harmonic cannot be controlled due to a lack of

sources in the present measurement system. In the future, by integrating more sources into the system, this limitation can be overcome.

3 Coefficients

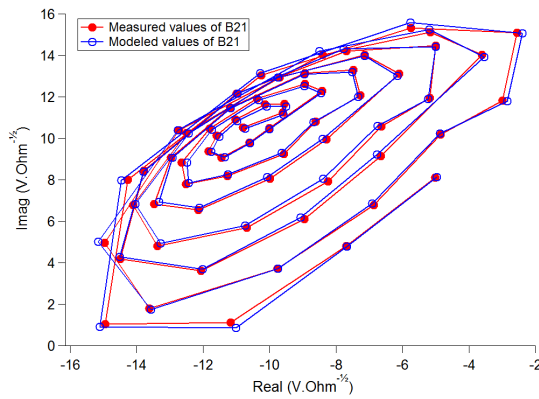


(a)

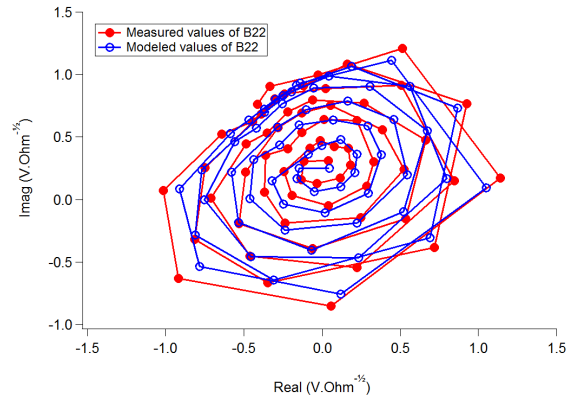


(b)

6 Coefficients



(c)



(d)

Figure 3-24: Measured versus modelled B waves extracted from large signal measurements of 2x80 μm reference device (a) B₂₁ with X-parameter 3 term model (b) B₂₂ with X-parameter 3 term model (c) B₂₁ with Cardiff 6 term model (d) B₂₂ with Cardiff 6 term model

This is the reason a Class B measurement was chosen to ensure that the odd harmonics typically generated, are not large enough to sufficiently alter the scalability of the model. Furthermore, we would like to demonstrate the ability of the model to predict results with high drain efficiencies.

As shown in Fig. 3-25, the Cardiff 6 term model is capable of reproducing the measured load-pull data for the 2x80 μm reference device accurately.

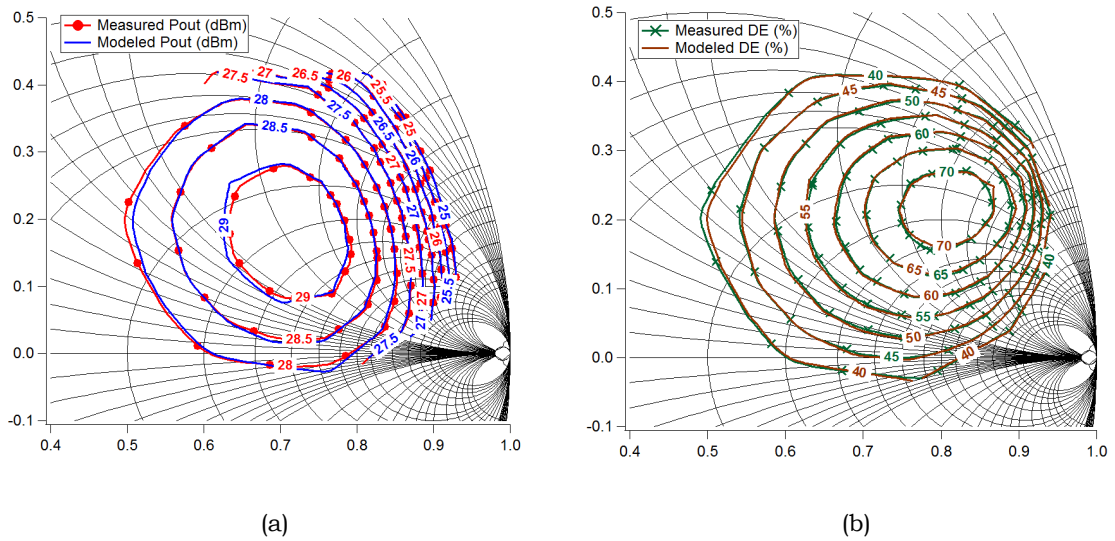


Figure 3-25: Measured versus modelled P_{out} and Drain Efficiency contours for the 2x80 μm reference device (generated using Cardiff 6 term model). (a) P_{out} contours (b) Drain Efficiency contours.

3.3.3 Mathematical Validation of Scaling in Model Coefficients

Model coefficients can be proven to scale mathematically with geometry by performing extraction with a fixed reference impedance Z_0 (usually 50 ohms) or with a scaled reference impedance [2]. The equations for A' and B' waves of the larger device extracted from a fixed reference impedance are already stated in equation (3-3).

Now if we scale the reference impedance by the scaling factor, s (the ratio of the larger device to the smaller reference) the resulting A' and B' waves are calculated based on equation (3-27)-(3-28).

$$Z'_0 = \frac{Z_0}{s} \quad (3-26)$$

$$A'_{p,h} = \frac{V'_{p,h} + Z'_0 I'_{p,h}}{2\sqrt{Z'_0}} = \sqrt{s} \left(\frac{V_{p,h} + Z_0 I_{p,h}}{2\sqrt{Z_0}} \right) = \sqrt{s} A_{p,h} \quad (3-27)$$

$$B'_{p,h} = \frac{V'_{p,h} - Z'_0 I'_{p,h}}{2\sqrt{Z'_0}} = \sqrt{s} \left(\frac{V_{p,h} - Z_0 I_{p,h}}{2\sqrt{Z_0}} \right) = \sqrt{s} B_{p,h} \quad (3-28)$$

Fig. 3-26 shows how the scaling rules apply to the scaled waves in the scaled reference impedance based on the original model coefficients of the reference device. Examples of the explicit scaling rules for the 6 model terms are in equation (3-29)-(3-34).

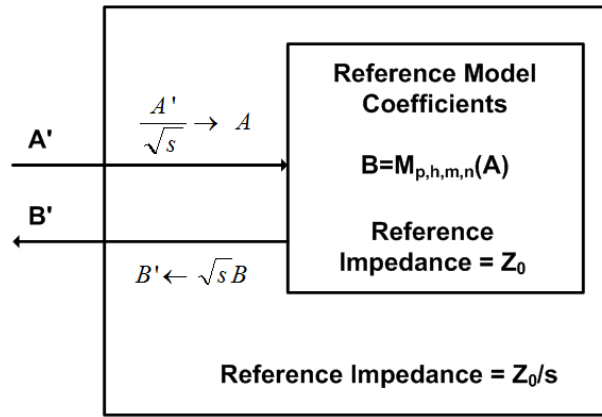


Figure 3-26: Cardiff model scaling using scaled reference impedance method

$$M'_{\frac{Z_0}{s}}{}^{(p,h,0,0)}(\sqrt{s}|A_{11}|, \sqrt{s}A_{21}) = \sqrt{s} \cdot M_{Z_0}{}^{(p,h,0,0)}(|A_{11}|, A_{21}) \quad (3-29)$$

$$M'_{\frac{Z_0}{s}}{}^{(p,h,0,1)}(\sqrt{s}|A_{11}|, \sqrt{s}A_{21}) = M_{Z_0}{}^{(p,h,0,1)}(|A_{11}|, A_{21}) \quad (3-30)$$

$$M'_{\frac{Z_0}{s}}{}^{(p,h,0,-1)}(\sqrt{s}|A_{11}|, \sqrt{s}A_{21}) = M_{Z_0}{}^{(p,h,0,-1)}(|A_{11}|, A_{21}) \quad (3-31)$$

$$M'_{\frac{Z_0}{s}}{}^{(p,h,1,0)}(\sqrt{s}|A_{11}|, \sqrt{s}A_{21}) = \frac{1}{\sqrt{s}} \cdot M_{Z_0}{}^{(p,h,1,0)}(|A_{11}|, A_{21}) \quad (3-32)$$

$$M'_{\frac{Z_0}{s}}(p,h,0,2)(\sqrt{s}|A_{11}|, \sqrt{s}A_{21}) = \frac{1}{\sqrt{s}} \cdot M_{Z_0}(p,h,0,2)(|A_{11}|, A_{21}) \tag{3-33}$$

$$M'_{\frac{Z_0}{s}}(p,h,0,-2)(\sqrt{s}|A_{11}|, \sqrt{s}A_{21}) = \frac{1}{\sqrt{s}} \cdot M_{Z_0}(p,h,0,-2)(|A_{11}|, A_{21}) \tag{3-34}$$

Comparison of model coefficients (at the output port, at the fundamental, $p=2$, $h=1$) extracted at a fixed reference impedance and at a scaled reference impedance with $s = 2.5$ is shown in Fig. 3-27.

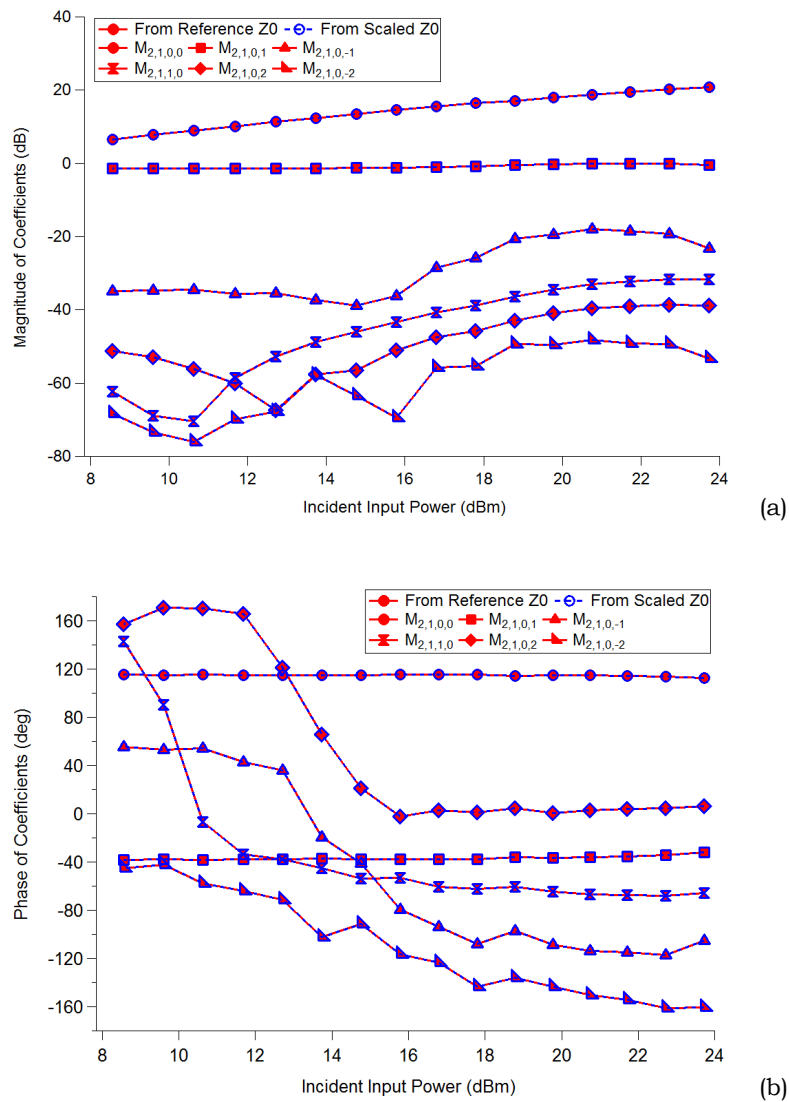


Figure 3-27: Comparison of model coefficients (at $p = 2$, $h = 1$) extracted at fixed reference impedance of 50 ohms and scaled reference impedance by $s = 2.5$ (a) Magnitude of coefficients (b) Phase of coefficients

Do note that the range of incident input power is also scaled by the appropriate factor so that they can be compared directly. The input incident power, $P_{incident}$ is directly related to $|A_{11}|$ as shown in equation (3-35). The Behavioural model is extracted as a function of the magnitude of A_{11} .

$$P_{incident}(dBm) = 10 \log_{10} \left(\frac{|A_{11}|^2}{2Re(Z_0)} * 1000 \right) \quad (3-35)$$

From the results, it is clear that both methods can be used for model extraction (as there is no difference in the values) and so the fixed reference method is used in this work. This exercise also proves that mathematically, the model coefficients are geometrically scalable since they follow explicit scaling rules.

3.3.4 Practical Considerations in Model Extraction

Measurements of the reference device will be used to extract coefficients for the scalable model. Theoretically, the model should be extracted from intrinsic measurement data. However, according to the Polyharmonic Distortion principles, model coefficients are to be extracted at a fixed A_{11} and bias. By de-embedding the measurements to the intrinsic plane, for a particular drive, the A_{11} and bias conditions will vary slightly and violate this condition set for model extraction.

Therefore, to solve this issue, the model extraction will be performed at the extrinsic plane. During its usage within a circuit simulator, the de-embedding network of the reference (smaller) device will be attached around model block. The model will then be scaled and reattached with the embedding network of the larger, scaled device. This is opposed to having an intrinsic model of the

reference device which is scaled and applied with an embedding circuit. The two separate methods are illustrated in Fig. 3-28(a)-(b).

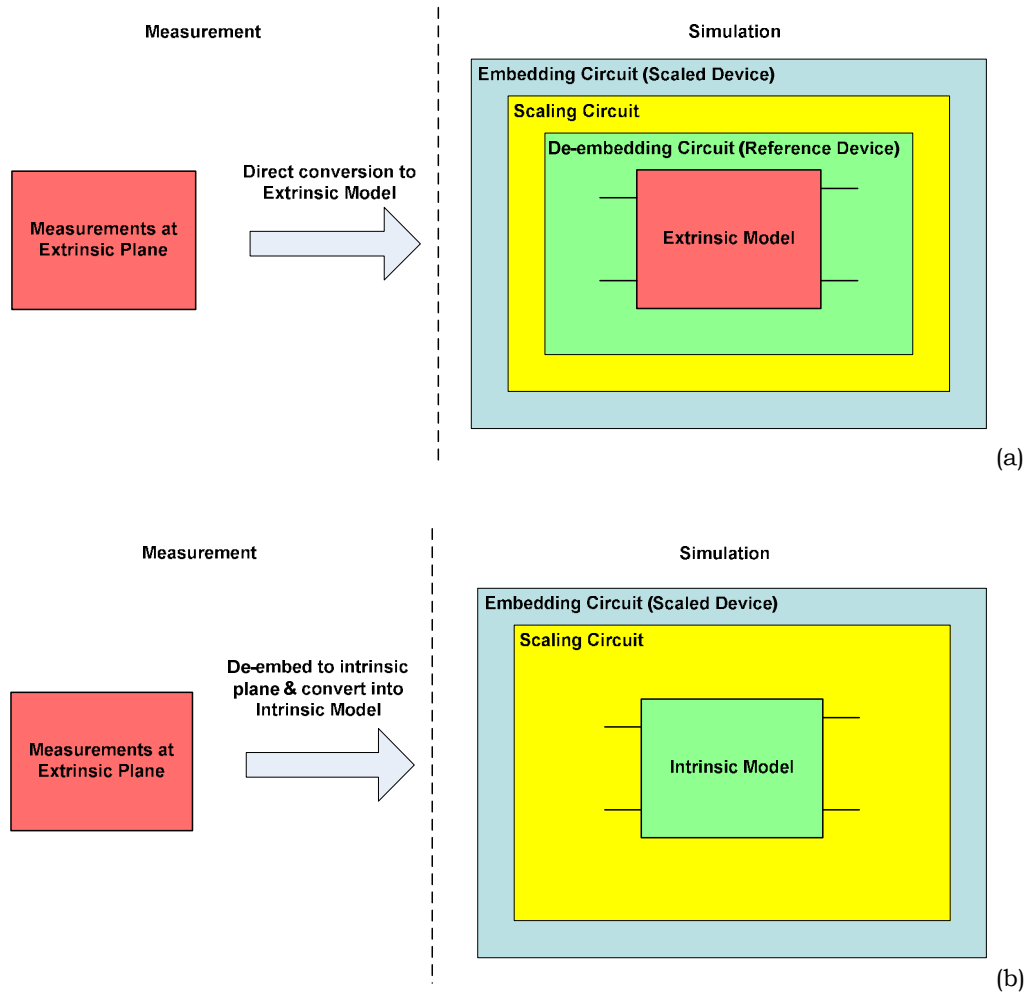


Figure 3-28: Process flow to obtain Behavioural model from reference device measurements (a) Extrinsic model (b) Intrinsic model

Note that extrinsic measurements will fall on a grid whereas intrinsic measurements do not, making it a problem especially for table based models [26]. By having the circuit simulator handle the de-embedding, this practical method provides another advantage by avoiding re-gridding of the data on the intrinsic space.

3.4 Experimental Model Validation

This section will show results of a model extracted from the 2x80 μm reference device and scaled to 2.5 times and 5 times larger (4x100 μm device and 4x200 μm device) to validate the scalable model.

3.4.1 Small signal validation

It is always good practice to check the results with small signal data before moving on the large signal data to ensure that we are starting out on the right track. It is known that at low power levels, the X-parameters as well as the Cardiff model collapses into the S-parameters. The relationship is described in equation (3-36)-(3-37).

$$S_{11} = M_{1,1,0,0}/|A_{1,1}| \quad S_{21} = M_{2,1,0,0}/|A_{1,1}| \quad (3-36)$$

$$S_{22} = M_{2,1,0,1} \quad S_{12} = M_{1,1,0,1} \quad (3-37)$$

Fig. 3-29(a)-(d) shows the S-parameters from 1 to 20 GHz obtained at $I_d = 5$ mA/mm (Class B bias) for 3 different devices, 2x80 μm , 4x100 μm and 4x200 μm . The S-parameters at 5 GHz obtained from large signal data at the lowest measured drive level is also plotted on the same diagrams. As seen from the results, the theory holds true and at small drive levels is essentially the S-parameters.

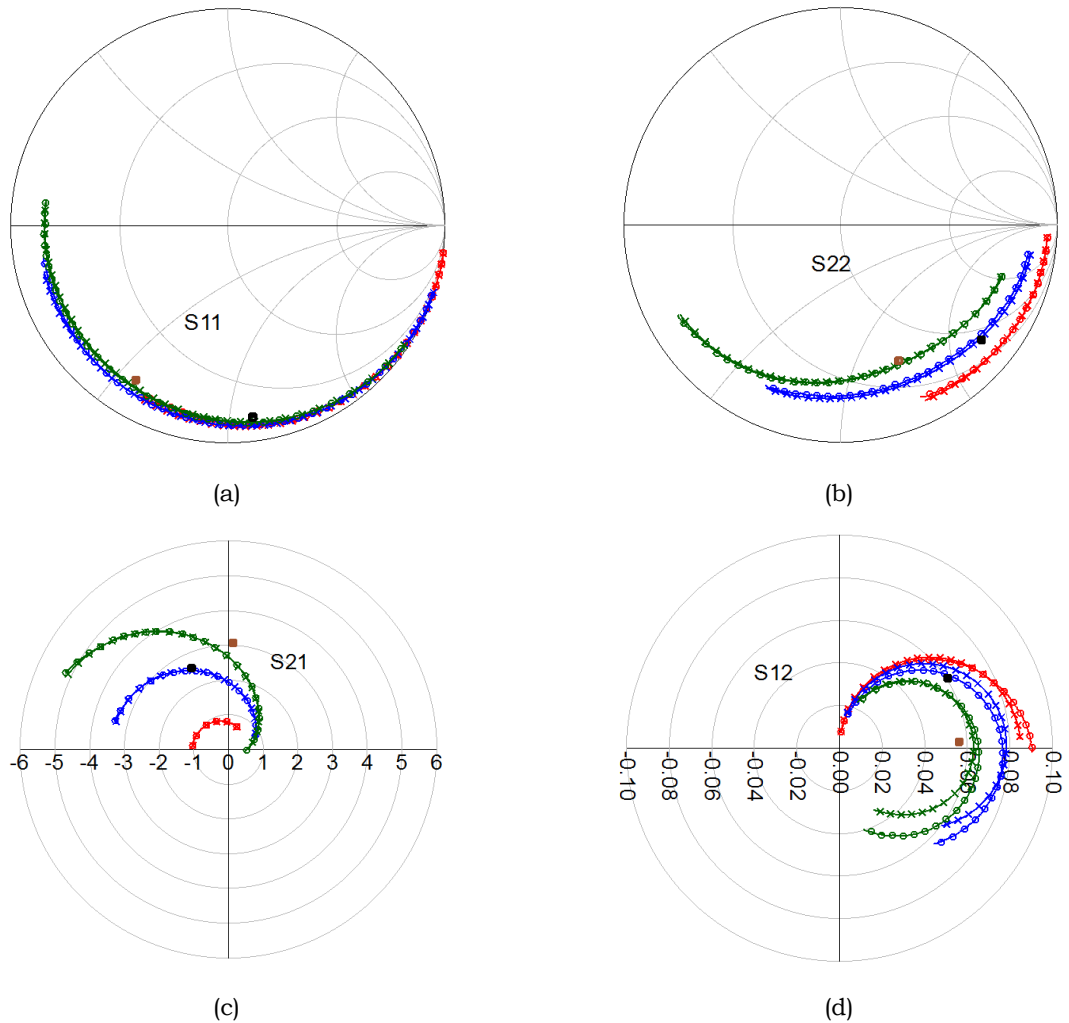
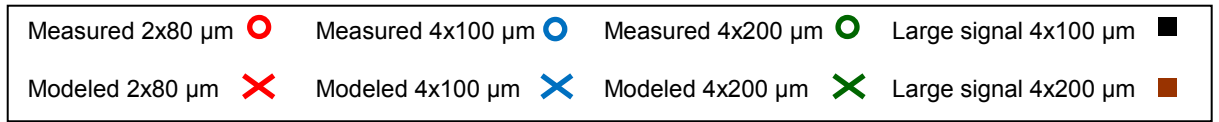


Figure 3-29: S-parameter results from 1 - 20 GHz with large signal S-parameter at 5 GHz for 2x80 μm , 4x100 μm and 4x200 μm devices. (a) S₁₁ (b) S₂₂ (c) S₂₁ (d) S₁₂

3.4.2 Large Signal Simulation Setup in ADS

In order to validate the scalable model, a simulation is setup in ADS as explained by the block diagram in Fig. 3-30. It consists of an FDD block, which reads the model coefficients from a DAC and applies them to equation (3-25). This block is actually embedded in another outer block, which runs the simulation from the external (larger device) world.

For example, in order to simulate the results of a device, which is 2.5 times larger ($s = 2.5$), the external environment will operate the load-pull at the conditions of the larger device. The resulting A_{ext} waves fed into the device will first be converted to A' using the parasitics of the scaled device.

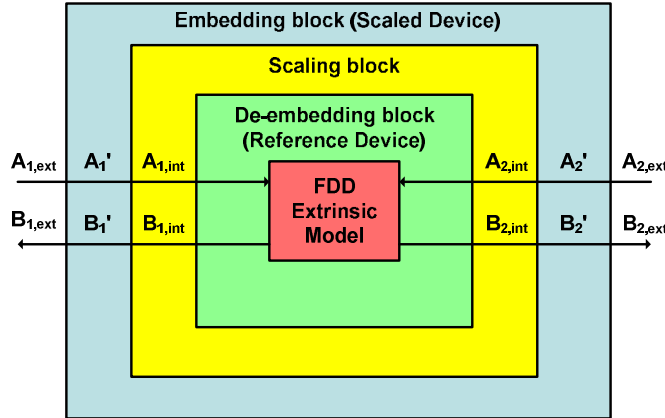
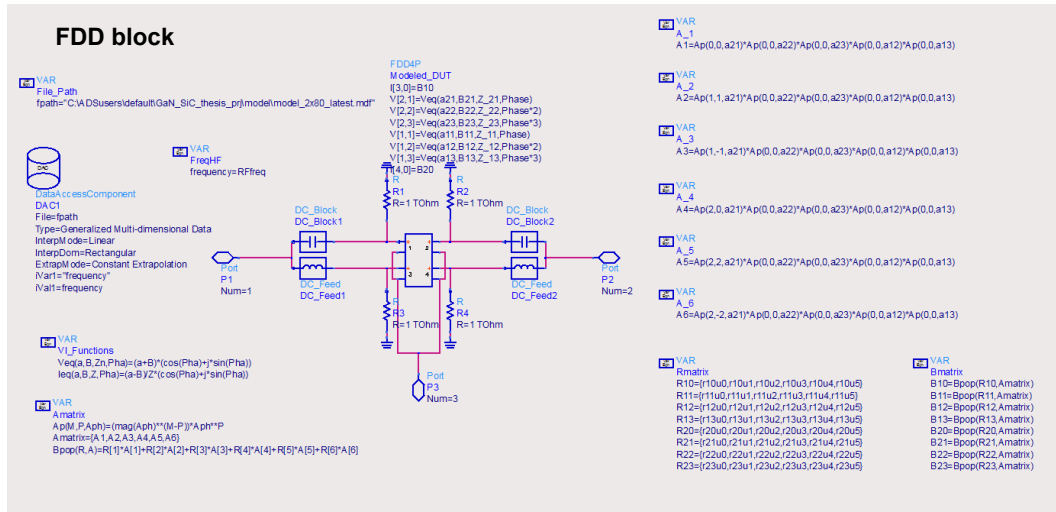


Figure 3-30: Block diagram depicting simulation setup in ADS that runs the scalable model.

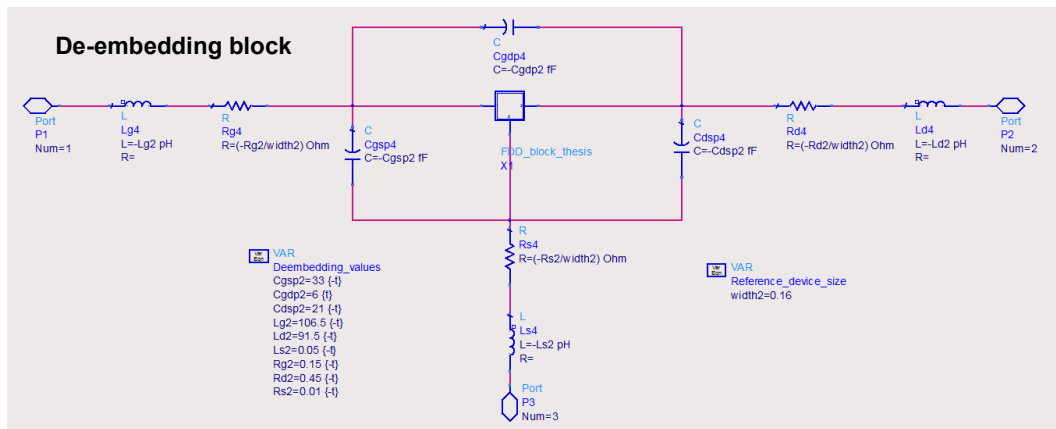
Then the A' wave will be scaled down by 2.5, resulting in the A_{int} wave. The A_{int} wave is then analysed by the FDD block enclosed in a de-embedding circuit of the reference $2 \times 80 \mu\text{m}$ transistor. As explained in Section 3.3.4, the FDD reads a model file which has been extracted at the extrinsic plane so it must be enclosed in a de-embedding circuit. This is to ensure scaling takes place at the intrinsic plane where equation (3-1) is valid. Once the B_{int} waves are calculated from the model coefficients, it will be scaled up accordingly before being embedded to finally result in B_{ext} . The same process goes on for both ports. The modelled results can then be compared with measurements.

Fig. 3-31(a)-(d) shows the actual circuit in ADS that runs the simulation. Note that Fig. 3-31(b) contains the "negative" values of circuit components to perform the de-embedding whereas Fig 3-31(d) uses the "positive" component values to enforce embedding. The values of these circuit elements were obtained in Section 3.2 using cold FET extractions. The scaling is achieved

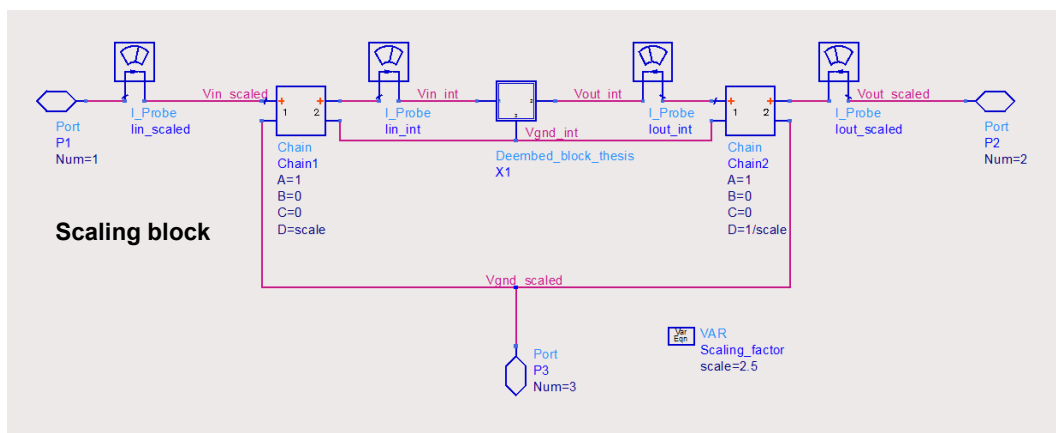
using ABCD block as shown in Fig. 3-31(c). The FDD block produces voltages and currents as its output which are translated into the A and B waves.



(a)



(b)



(c)

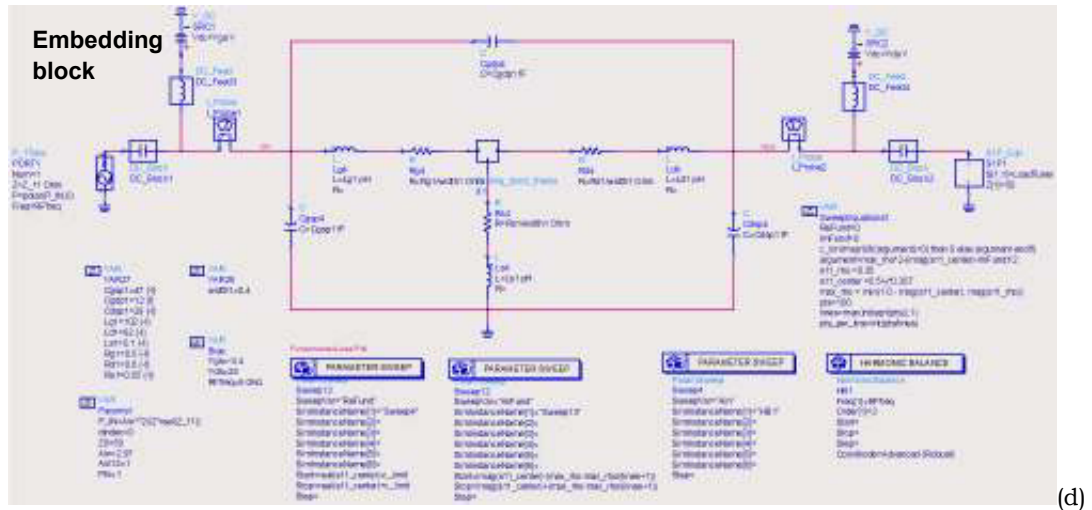


Figure 3-31: ADS simulation diagram that utilizes scalable model (a) FDD block (b) De-embedding block (c) Scaling block (d) Embedding block with load-pull circuit

Taking advantage of the fact that voltage remains the same and current scales with device gate size, the following equation can be applied:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (3-38)$$

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & scale \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \quad (3-39)$$

With scale being the ratio between the scaled device and the reference device as defined in equation (3-1).

As a validation that the scaling block in Fig. 3-31(c) is functioning properly, a screenshot of the simulation is shown in Fig. 3-32. I_{in_scaled} and I_{out_scaled} (shown in Fig. 3-31(c)) are both 2.5 times larger than I_{in_int} and I_{out_int} respectively whereas the voltages at the input and output ports remains the same.

Voltage remain the same **Current is 2.5 times larger**

		V _{in_int-Vgnd_int}	V _{out_int-Vgnd_int}	I _{in_int.i}	I _{out_int.i}
Before scaling	freq				
	ImFund=-0.01118, ReFund=0.000000 Hz	3.40332 / 180.00000	27.95601 / 0.00000	0.00002 / 180.00000	0.01083 / 0.00000
	5.00000 GHz	1.16161 / -38.49287	3.61330 / 102.05707	0.00681 / 42.58771	0.01371 / -69.78893
	10.0000 GHz	0.04534 / 178.73451	0.09369 / 153.27528	0.00037 / 4.37682	0.00692 / -99.27877
	15.0000 GHz	0.01764 / 74.91560	0.03140 / 60.05793	0.00015 / -99.54127	0.00159 / 161.86298
	ImFund=-0.01118, ReFund=0.000000 Hz	3.40377 / 180.00000	27.95053 / 0.00000	0.00001 / 180.00000	0.01218 / 0.00000
	5.00000 GHz	1.30029 / -38.65148	4.14935 / 102.08160	0.00768 / 42.39652	0.01575 / -69.77797
	10.0000 GHz	0.05549 / 176.13256	0.11555 / 151.80839	0.00045 / 1.80332	0.00854 / -100.74418
	15.0000 GHz	0.02113 / 75.91483	0.03775 / 59.47706	0.00018 / -98.53653	0.00191 / 161.30012
	ImFund=-0.01118, ReFund=0.000000 Hz	3.40424 / 180.00000	27.94427 / 0.00000	0.00001 / 180.00000	0.01372 / 0.00000
	5.00000 GHz	1.45966 / -38.84166	4.76182 / 102.20200	0.00866 / 42.22919	0.01803 / -69.66971
	10.0000 GHz	0.06555 / 178.58202	0.13208 / 153.04132	0.00053 / 4.15702	0.00978 / -99.51373
15.0000 GHz	0.02709 / 75.52875	0.04664 / 59.04127	0.00023 / -98.98219	0.00236 / 160.86293	
After scaling	freq				
	ImFund=-0.01118, ReFund=0.000000 Hz	3.40332 / 180.00000	27.95601 / 0.00000	0.00005 / 180.00000	0.02707 / 0.00000
	5.00000 GHz	1.16161 / -38.49287	3.61330 / 102.05707	0.01703 / 42.58771	0.03428 / -69.78893
	10.0000 GHz	0.04534 / 178.73451	0.09369 / 153.27528	0.00092 / 4.37682	0.01730 / -99.27877
	15.0000 GHz	0.01764 / 74.91560	0.03140 / 60.05793	0.00037 / -99.54127	0.00397 / 161.86298
	ImFund=-0.01118, ReFund=0.000000 Hz	3.40377 / 180.00000	27.95053 / 0.00000	0.00003 / 180.00000	0.03044 / 0.00000
	5.00000 GHz	1.30029 / -38.65148	4.14935 / 102.08160	0.01919 / 42.39652	0.03937 / -69.77797
	10.0000 GHz	0.05549 / 176.13256	0.11555 / 151.80839	0.00112 / 1.80332	0.02134 / -100.74418
	15.0000 GHz	0.02113 / 75.91483	0.03775 / 59.47706	0.00044 / -98.53653	0.00477 / 161.30012
	ImFund=-0.01118, ReFund=0.000000 Hz	3.40424 / 180.00000	27.94427 / 0.00000	0.00004 / 180.00000	0.03430 / 0.00000
	5.00000 GHz	1.45966 / -38.84166	4.76182 / 102.20200	0.02165 / 42.22919	0.04519 / -69.66971
	10.0000 GHz	0.06555 / 178.58202	0.13208 / 153.04132	0.00132 / 4.15702	0.02440 / -99.51373
15.0000 GHz	0.02709 / 75.52875	0.04664 / 59.04127	0.00057 / -98.98219	0.00589 / 160.86293	

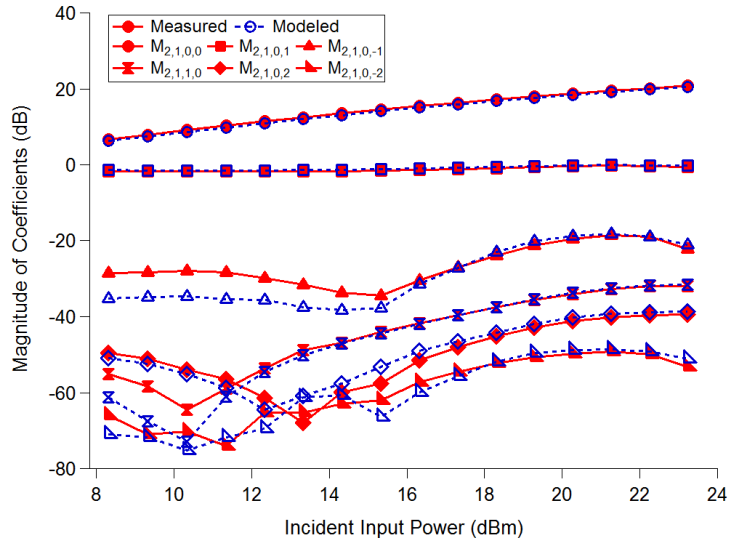
Figure 3-32: ADS simulation results to validate scaling block

3.4.3 Scaling by a factor of 2.5

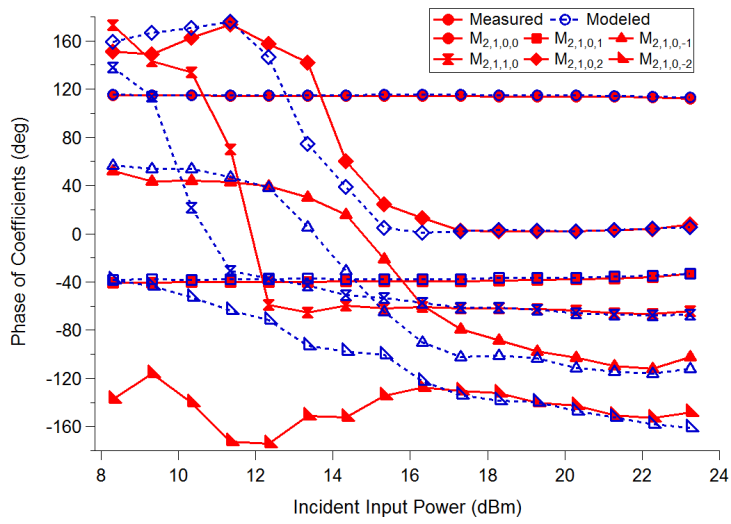
As mentioned earlier, the reference device is the 2x80 μm FET. The model coefficients are extracted from the reference device and will be used to simulate the performance of a 4x100 μm device (2.5 times larger) using the circuit shown in Fig. 3-31(a)-(d).

Firstly, in order to validate that the Behavioural model is scalable, the model coefficients must also be able to scale. The magnitude and phase for the coefficients of B₂₁ and B₂₂ are shown in Fig. 3-33(a)-(d). From the results, both the fundamental and 2nd harmonic model coefficients are in agreement.

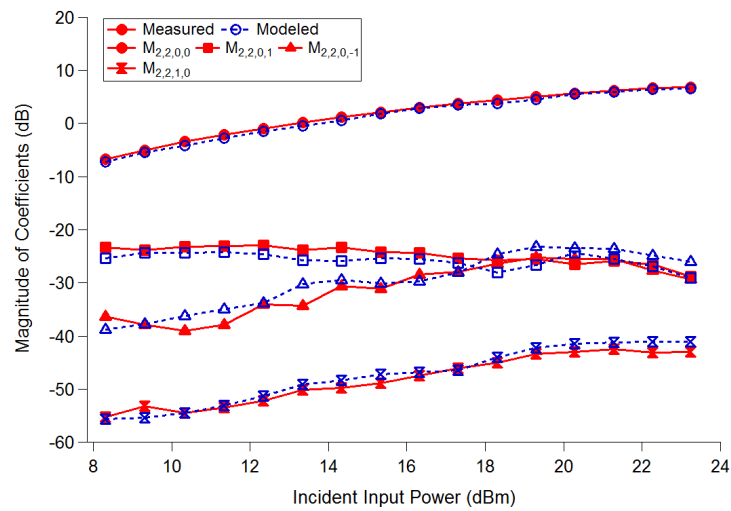
Note that higher order coefficients such as the M_{2,1,0,-2} are smaller in magnitude, especially at lower input power levels, causing a mismatch in phase but the B wave results are dominated by the main terms such as M_{2,1,0,0} and M_{2,1,0,1} (shown in Fig. 3-23) which match up very well.



(a)



(b)



(c)

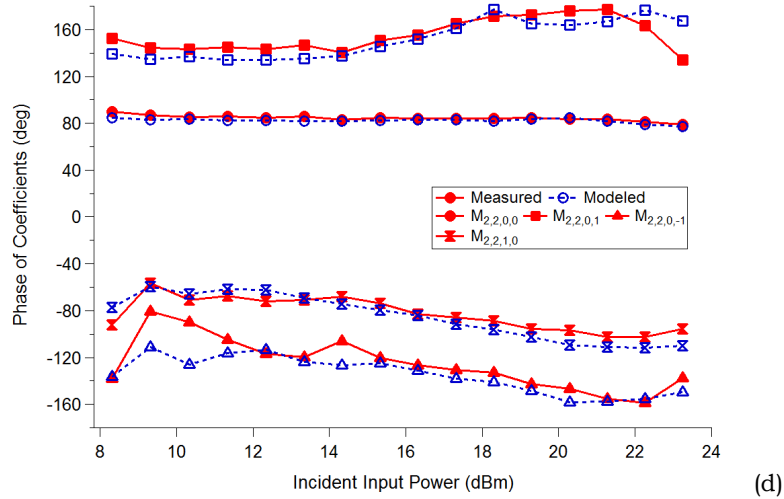


Figure 3-33: Measured versus modelled Cardiff Model coefficients for $4 \times 100 \mu\text{m}$ device as a function of drive level, P_{incident} . (a) Magnitude of Fundamental terms (b) Phase of Fundamental terms (c) Magnitude of 2nd harmonic terms (d) Phase of 2nd harmonic terms

Another cause of mismatch could be due to device-to-device variation within the wafer. Note that these observations are consistent with the results published in [2] for X-parameters. These model coefficients are used to generate the B waves from the input A waves.

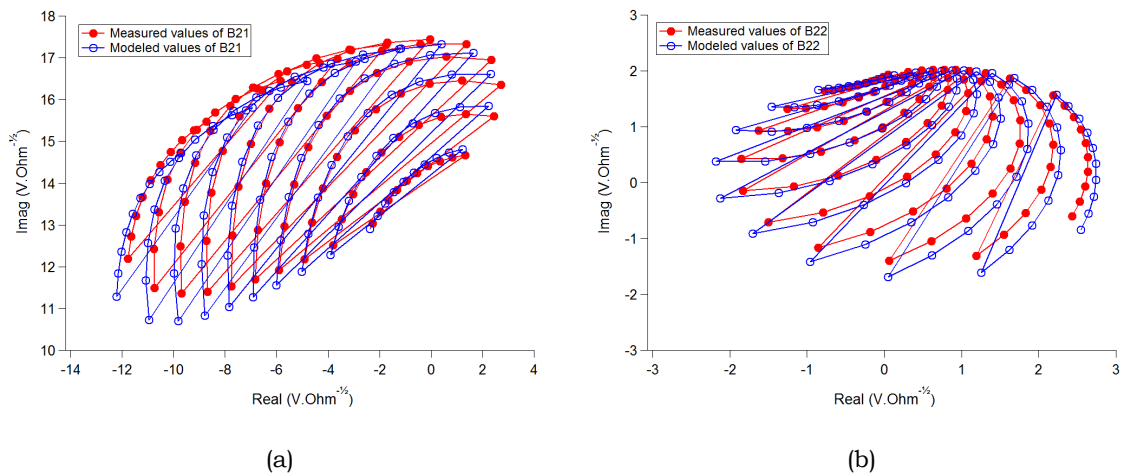


Figure 3-34: Measured versus modelled B waves for $4 \times 100 \mu\text{m}$ device (a) B_{21} (b) B_{22}

Fig. 3-34(a)-(b) shows the B_{21} and B_{22} waves generated from the simulation versus the measured results. Note the shape is due to the way the load-pull

simulation is setup where the imaginary load nested and swept within a swept range of real loads. These results are also in close agreement.

Now, from the B waves, we are able to calculate values, which are more of interest to a circuit designer such as P_{out} and Drain Efficiency. Fig. 3-35(a)-(b) show the P_{out} and Drain Efficiency contours at a $P_{incident}$ of 22.27 dBm. At this drive level, the device is close to 3 dB into compression.

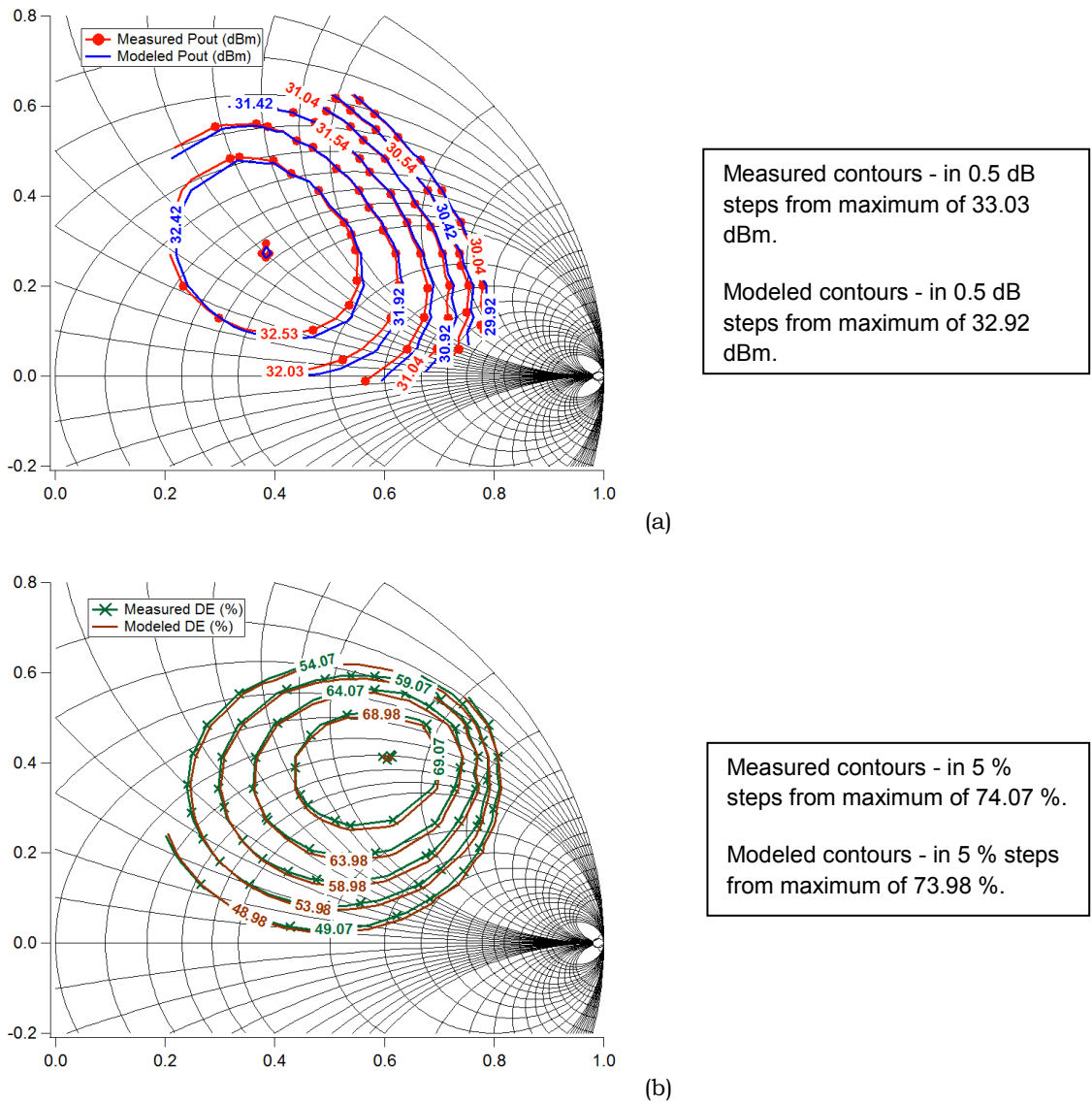


Figure 3-35: Measured versus modelled P_{out} and Drain Efficiency contours for the 4x100 μm device at a $P_{incident}$ of 22.27 dBm. (a) P_{out} contours (b) Drain Efficiency contours.

The measured and modelled contours are plotted with different but very close optimum values to show that the actual shape of the contour does not get distorted and that scaling occurs accurately. It is also to shows that the predicted load, which gives the maximum result is precise.

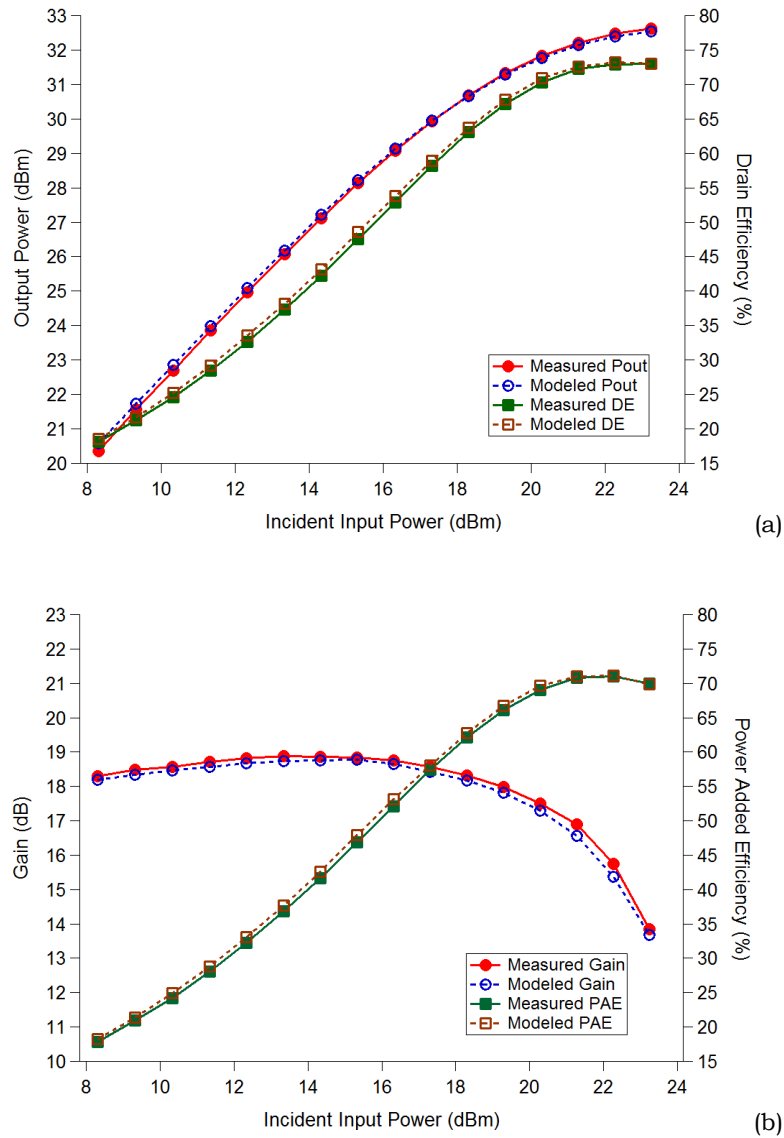


Figure 3-36: Measured versus modelled P_{out} and Drain Efficiency from power sweep at optimum load $\Gamma = 0.539 + j0.342$ for the 4x100 μm device (a) P_{out} and Drain Efficiency (b) Gain and PAE

Performing a power sweep at the optimum load of $\Gamma = 0.539 + j0.342$ that provides the best trade-off between P_{out} and Drain Efficiency, the results are

shown in Fig. 3-36(a). At this optimum load, the error in terms of P_{out} is within 0.22 dBm and Drain efficiency is 1.06 %.

The validation is performed in ADS so that both the measured and modelled can be swept with similar incident input power as defined in equation (3-35) to provide a proper comparison. Do note that actual input power into the device takes into account the reflected B waves on port 1 as defined in equation (3-40). This model is also able to predict actual input power accurately since the maximum error between measured and modelled Gain and PAE shown in Fig. 3-36(b) is 0.39 dB and 1.04 % respectively.

$$P_{in}(dBm) = 10 \log_{10} \left(\frac{|A_1^2 - B_1^2|}{2} * 1000 \right) \quad (3-40)$$

The waveforms that result from the power sweep are also plotted in Fig. 3-37(a)-(b). It is "scalable" because the Behavioural model is generated from measurements of the smaller $2 \times 80 \mu\text{m}$ reference device and are scaled to a $4 \times 100 \mu\text{m}$ device. The good correlation validates the scaling abilities of the Behavioural model.

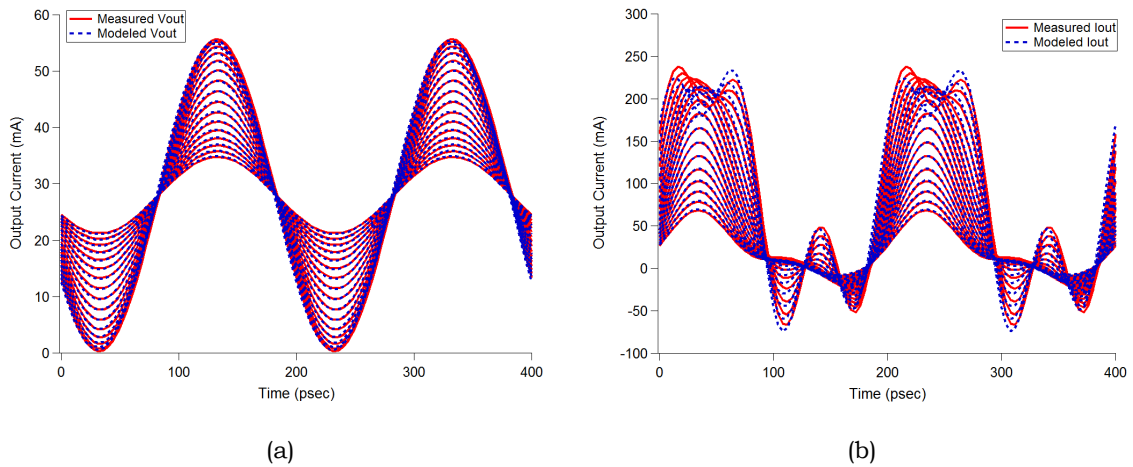
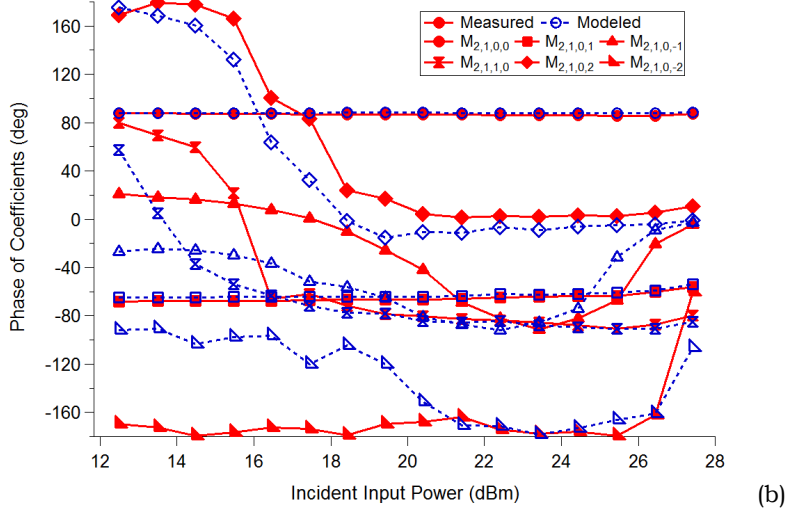
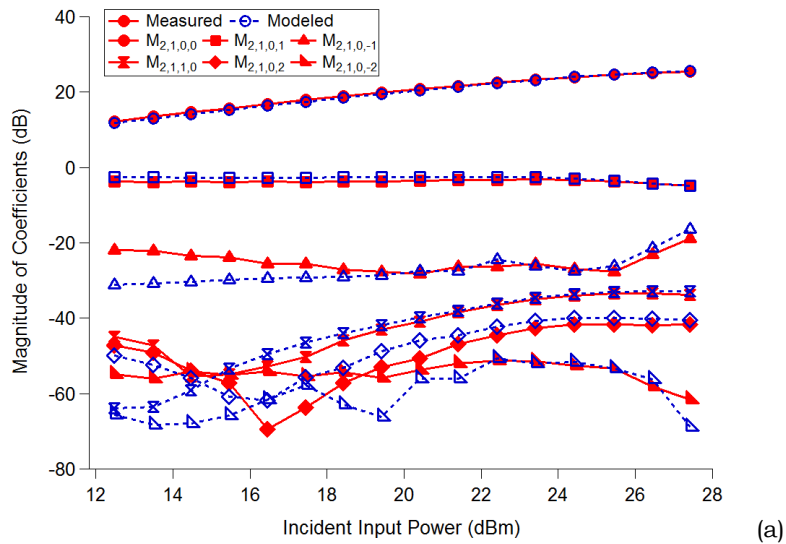


Figure 3-37: Measured versus modelled waveforms from power sweep at optimum load $\Gamma = 0.539 + j0.342$ for the $4 \times 100 \mu\text{m}$ device (a) Output voltage (b) Output current

3.4.4 Scaling by a factor of 5

The next step is to test the scalable model at different scaling factors, s . The larger device chosen for a scaling of $s = 5$ is the $4 \times 200 \mu\text{m}$ device. Fig. 3-38(a)-(d) presents the comparison of the measured versus modelled coefficients for the $4 \times 200 \mu\text{m}$ device at the fundamental and 2nd harmonic.

Once again, the modelled coefficients match up well with the measured except those of higher order at lower input power levels because these values are very small (less than -40 dB). They start to match up better at higher input power when they become more dominant.



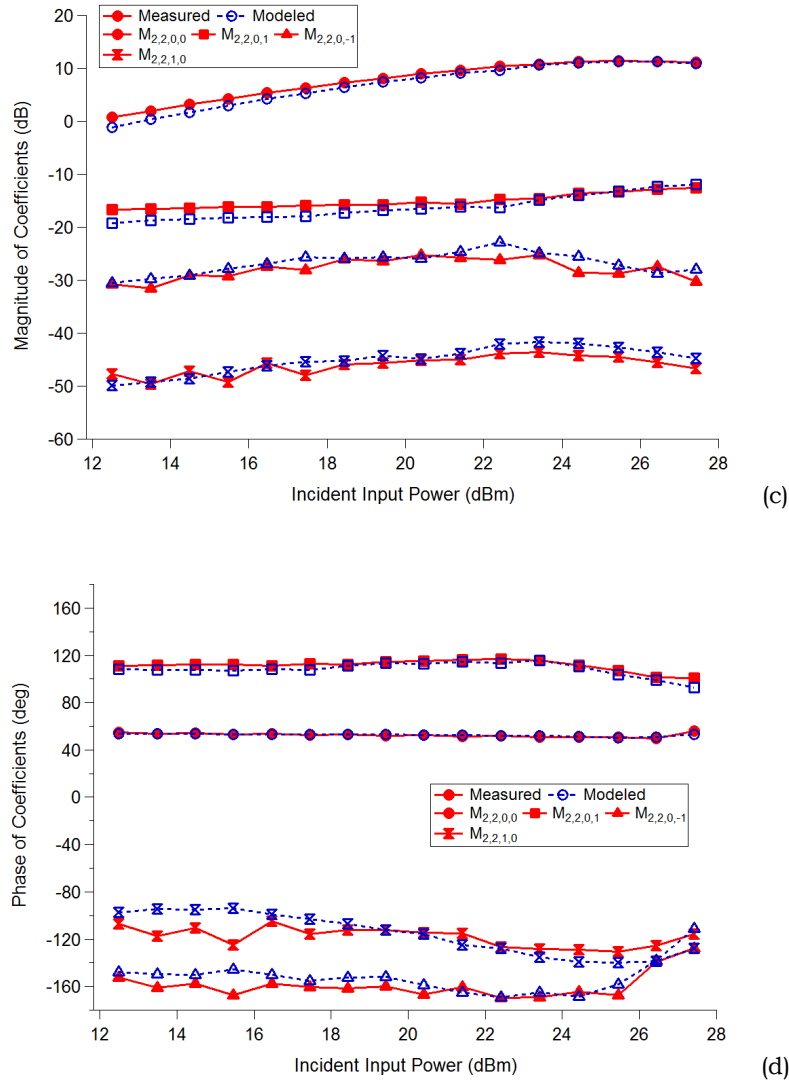


Figure 3-38: Measured versus modelled Cardiff Model coefficients for 4x200 μm device as a function of drive level, $P_{incident}$. (a) Magnitude of Fundamental terms (b) Phase of Fundamental terms (c) Magnitude of 2nd harmonic terms (d) Phase of 2nd harmonic terms

The B waves generated using the model coefficients are in Fig. 3-39(a)-(b). Note that as we move to a larger scaling factor, the error of the scaling gets larger since we are always assuming the same intrinsic condition for the transistors. However, from the results, scaling to a factor of 5 still produces acceptable results.

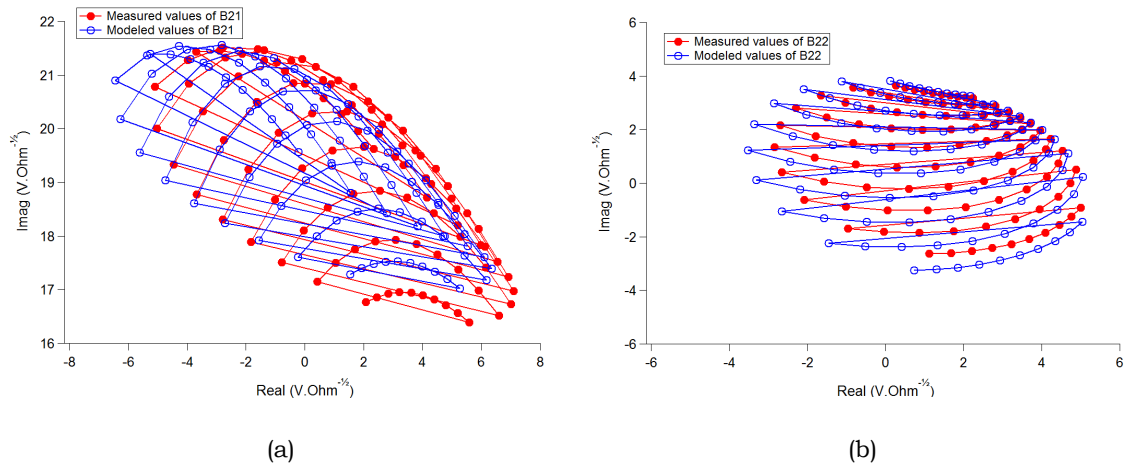
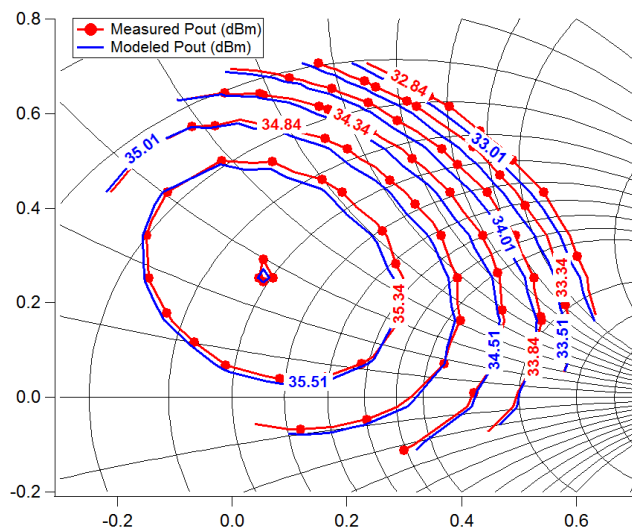


Figure 3-39: Measured versus modelled B waves for 4x200 μm device (a) B₂₁ (b) B₂₂

The P_{out} and Drain Efficiency contours are plotted in Fig. 3-40(a)-(b) at a P_{incident} of 26.44 dBm. From the load-pull results, the model is able to accurately predict the maximum values and optimum load location for the larger measured device.



Measured contours - in 0.5 dB steps from maximum of 35.84 dBm.

Modeled contours - in 0.5 dB steps from maximum of 36.01 dBm.

(a)

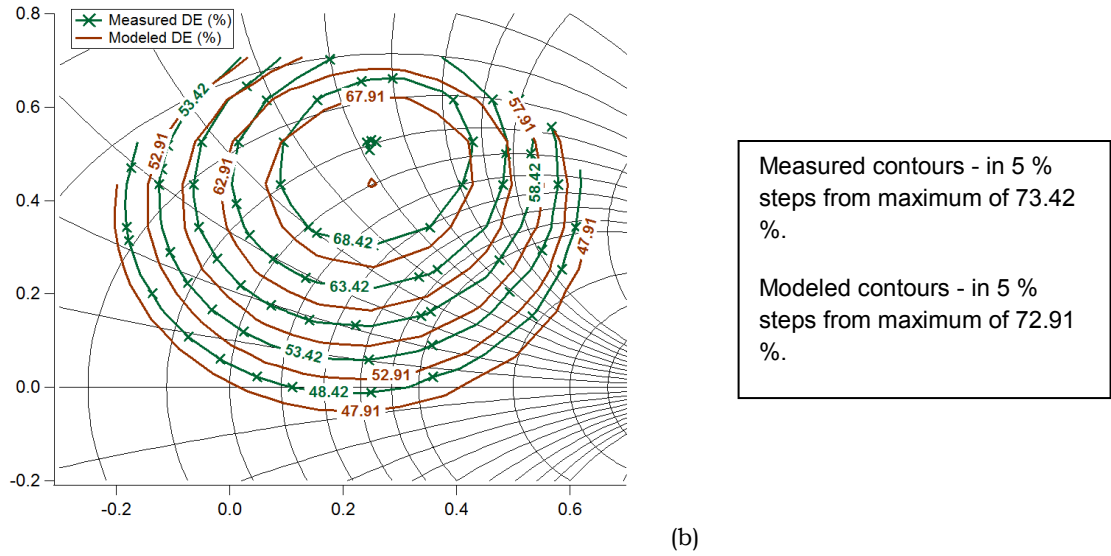
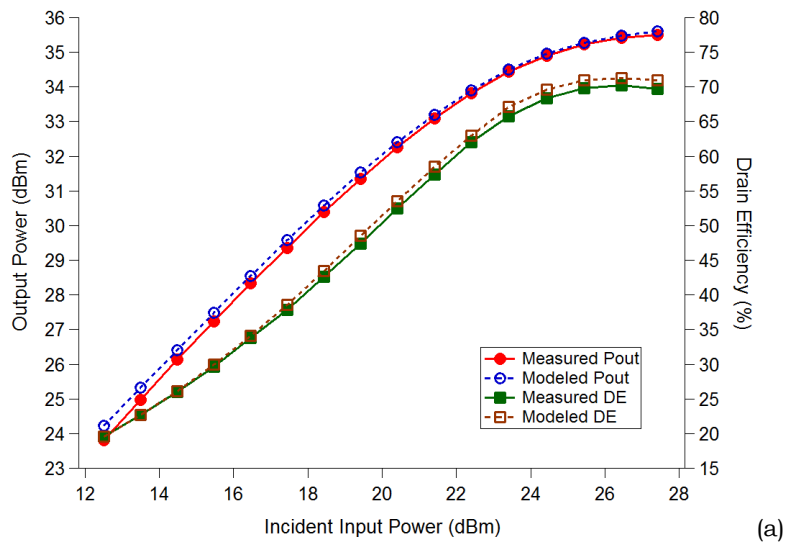


Figure 3-40: Measured versus modelled P_{out} and Drain Efficiency contours for the $4 \times 200 \mu m$ device at a $P_{incident}$ of 26.44 dBm. (a) P_{out} contours (b) Drain Efficiency contours.

The optimum load (for trade-off between P_{out} and Drain Efficiency) is $\Gamma = 0.251 + j0.343$ produces the power sweep results in Fig. 3-41(a)-(b) and the corresponding waveforms in Fig. 3-42(a)-(d). The maximum error for P_{out} and Drain Efficiency in the power sweep is 0.41 dB and 1.30 % respectively. The difference between measured and modelled Gain and PAE is 0.34 dB and 1.48 % respectively.



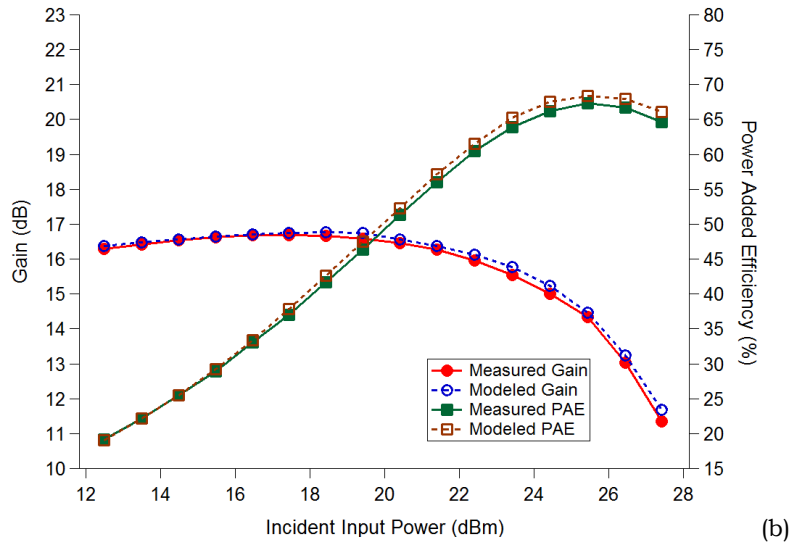


Figure 3-41: Measured versus modelled P_{out} and Drain Efficiency from power sweep at optimum load $\Gamma = 0.251 + j0.343$ for the 4x200 μm device (a) P_{out} and Drain Efficiency (b) Gain and PAE.

Note the modelled waveforms results in Fig. 3-42(a)-(b) are slightly different than the measured due to the impedance of the third harmonic component which is not controlled during measurements. Despite this, the modelled waveforms align very well.

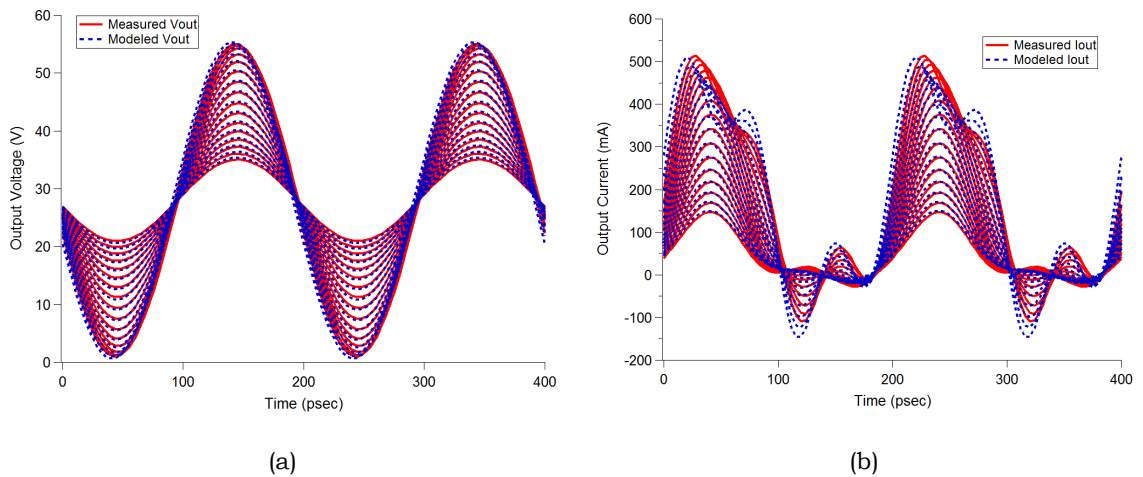


Figure 3-42: Measured versus modelled waveforms from power sweep at optimum load $\Gamma = 0.251 + j0.343$ for the 4x200 μm device (a) Output voltage (b) Output current

Simulations utilizing the model for a scaling factor of 2 (using a 4x80 μm device) and 4 (using a 8x80 μm device) were also performed and the results are plotted in Appendix A.2 and A.3. The results once again confirm that the Cardiff Behavioural model is scalable.

3.5 Overcoming the Limitations of Model Scaling

3.5.1 Introduction

It is obvious that we cannot scale indefinitely, as the model will start to breakdown. As mentioned earlier, a good indication would be to look at the DCIVs and small signal data before attempting to scale the large signal behaviour. If we were use a scaling factor of 10 times on the 8x200 μm device, the DCIVs are plotted in Fig. 3-43 and S-parameters in Fig. 3-44(a)-(d).

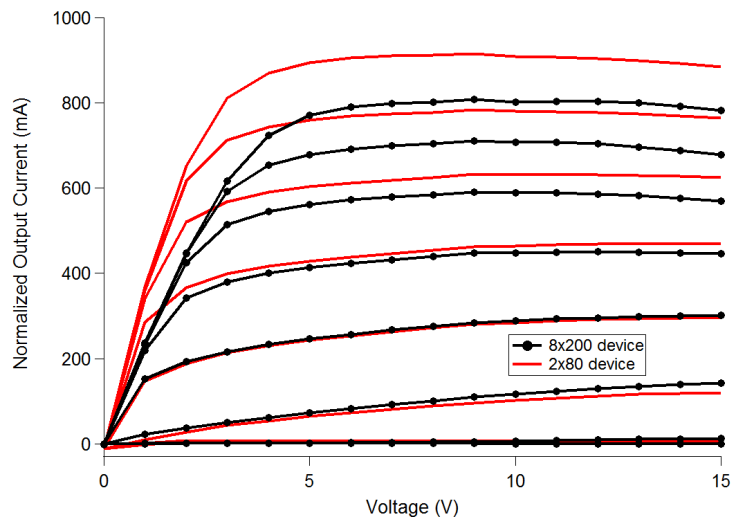


Figure 3-43: DCIV results for the 2x80 μm and 8x200 μm devices.

From the results in Fig. 3-43 and 3-44, it is clear that scaling will fail at a factor of 10. Notice that the modelled S_{21} for the 8x200 μm device does not align with the measured results. This indicates that the transconductance, g_m is different to what is expected.

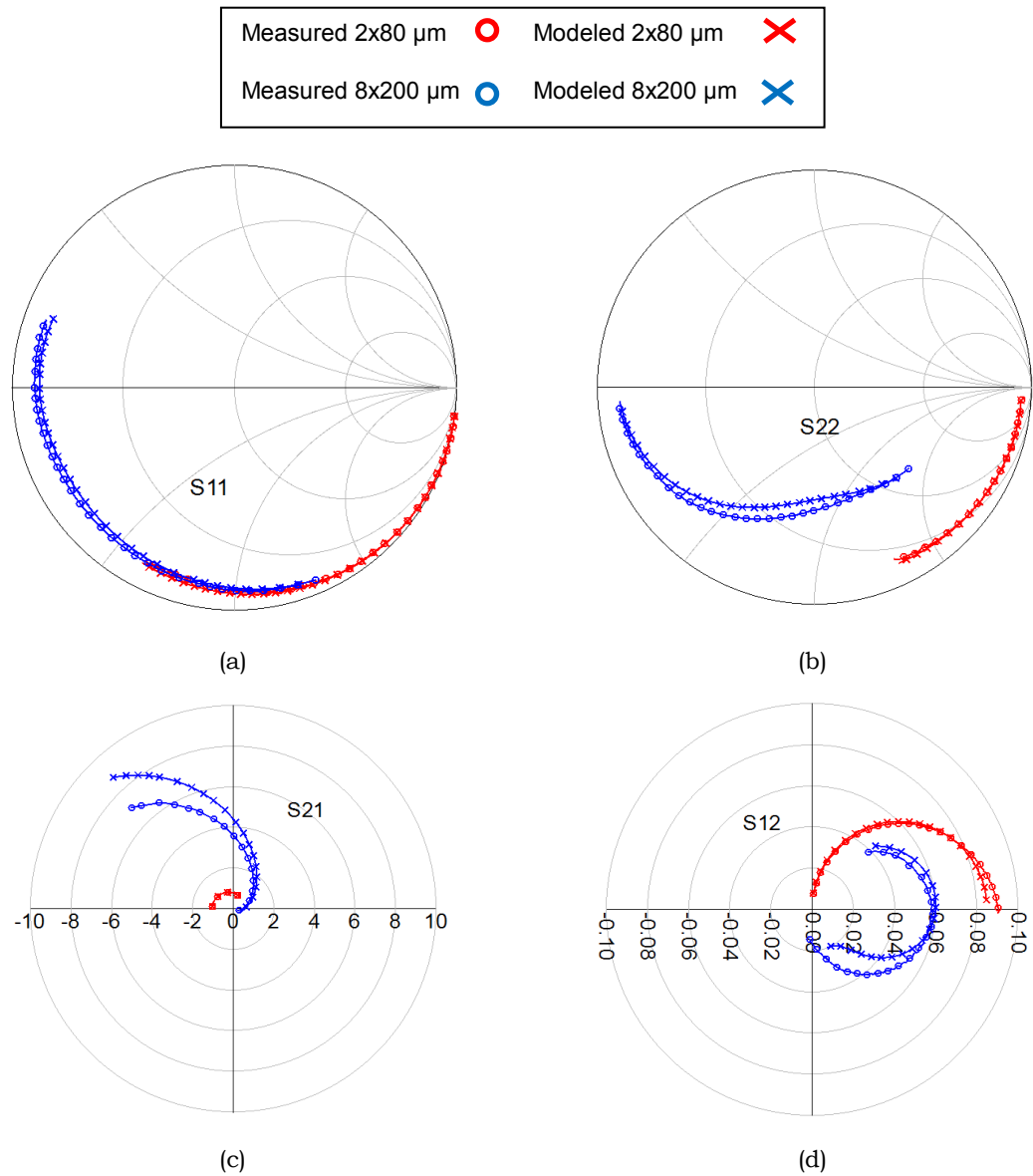
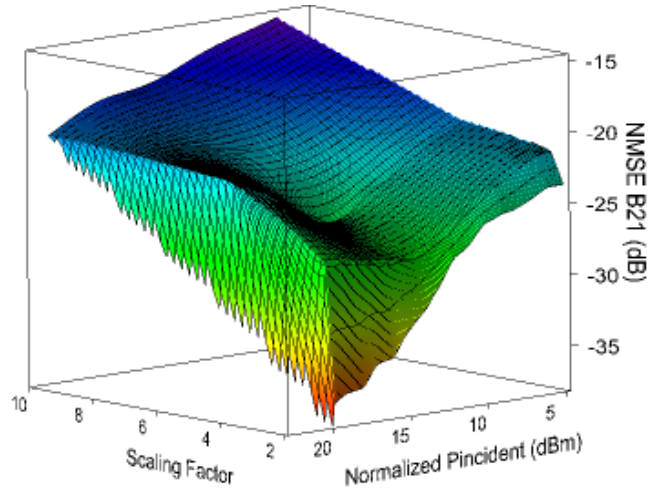
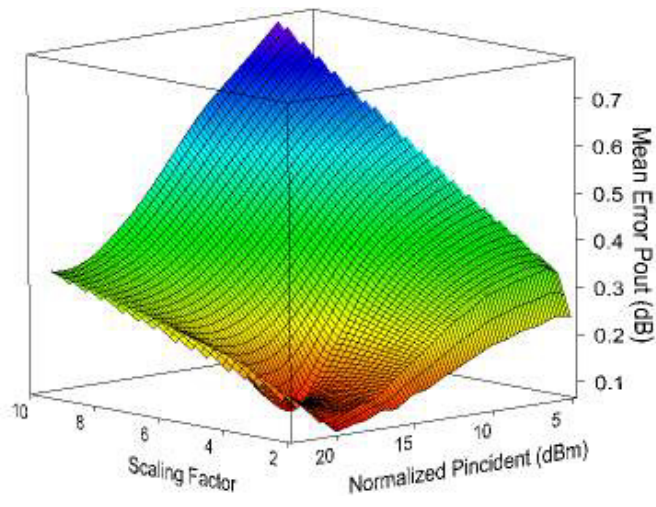


Figure 3-44: S-parameter results with large signal S-parameter at 5 GHz for 2x80 μm and 8x200 μm devices. (a) S_{11} (b) S_{22} (c) S_{21} (d) S_{12}

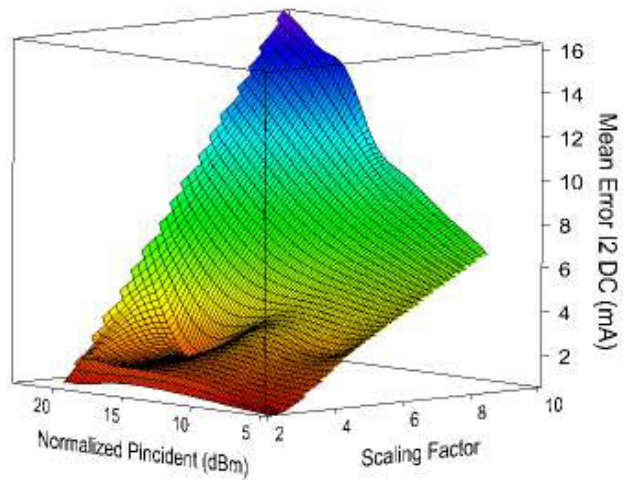
Fig. 3-45(a)-(d) show the 3D plots for errors as a function of normalized input incident power, P_{incident} and scaling factor, s . As expected, increasing the scaling factor will cause the accuracy of the scalable model to drop. One point to note is in Fig. 3-45 (a) and (b) where the error in B_{21} and P_{out} seem to be smaller at higher drive levels. This is consistent with our observation in Fig. 3-33(a)-(b) and Fig. 3-38(a)-(b) where the model coefficients for B_{21} are more accurate at higher drive levels.



(a)



(b)



(c)

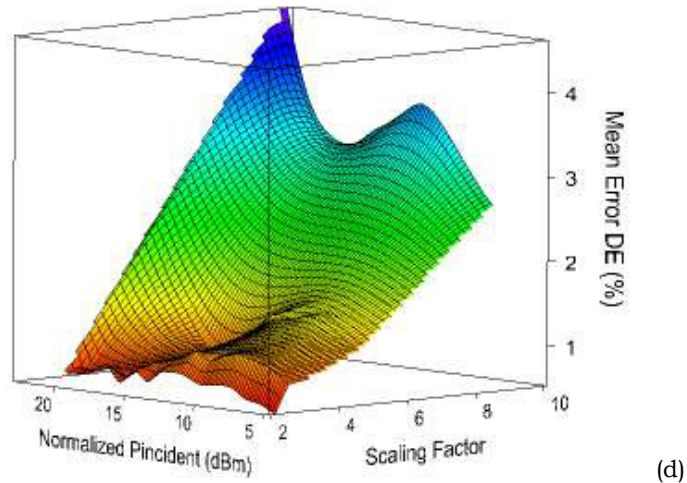


Figure 3-45: 3D plots of errors of measured versus modelled results as a function of normalized input incident power and scaling factor (a) NMSE for Magnitude of B21 (b) Mean error for P_{out} (c) Mean error for drain current (d) Mean error for Drain Efficiency.

This could be due to the dynamic range of the power calibration of the ZVA67 receiver since the calibration was done assuming a high power level in a region is where designers are most interested in. Performing measurements over various drive levels, the accuracy of the power calibration reduces when the measured signal becomes small.

Nevertheless, the errors are still within acceptable values. For example, the mean error in P_{out} and Drain Efficiency of the 3 dB load-pull space is 0.34 dBm and 1.13% respectively throughout the power sweep for a scaling factor of 2.5. Assuming a scaling factor of 5, the mean error in P_{out} and Drain Efficiency of the 3 dB load-pull space is less than 0.47 dBm and 2.28% respectively throughout the power sweep.

3.5.2 Temperature modelling

One factor that often causes the model to fail are thermal issues. The larger the device, the hotter it will operate. A dominant effect of self-heating is a reduction of drain current and occurs due to decreased electron mobility [26].

Therefore, in order to truly claim that the intrinsic conditions of the larger device are the same as the scaled smaller reference version, temperature must be taken into account.

Measuring the DCIVs of the reference 2x80 μm device at various chuck temperatures, we are able to determine from the results in Fig. 3-46 that the DCIV of 2x80 μm device measured at a chuck temperature of 70°C matches up with that of the 8x200 μm device operating at 25°C. These measurements were performed on the Cascade Probe Station using the ERS Aircool system. This thermal control system is able to set the chuck temperature from -55°C to +200°C.

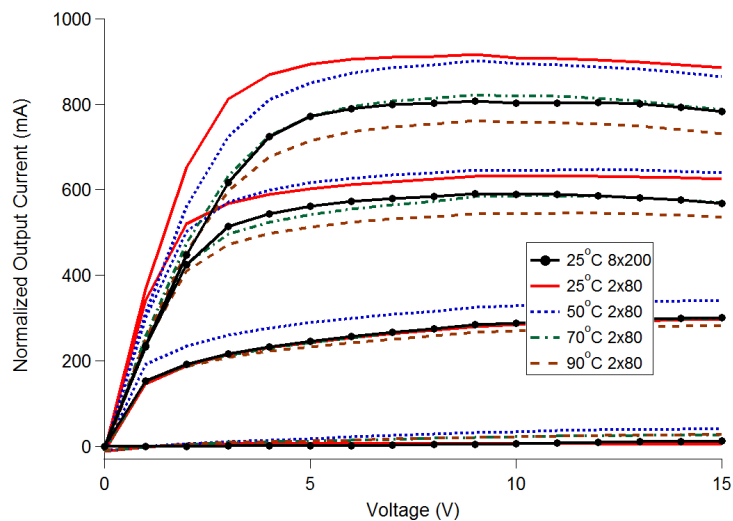


Figure 3-46: DCIV results for the 8x200 μm device and 2x80 μm device at various temperatures

Fig. 3-47(a)-(b) are the power sweeps of P_{out} and Drain Efficiency at various temperatures. As expected, increasing the chuck temperature results in reduced P_{out} and Drain Efficiency. When the chuck temperature is raised 70°C, the model is able to predict the measurements for a scaling factor of 10.

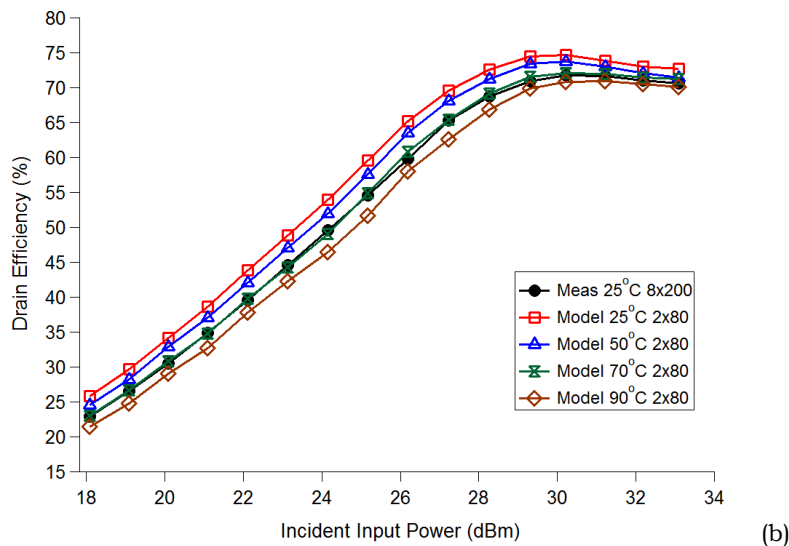
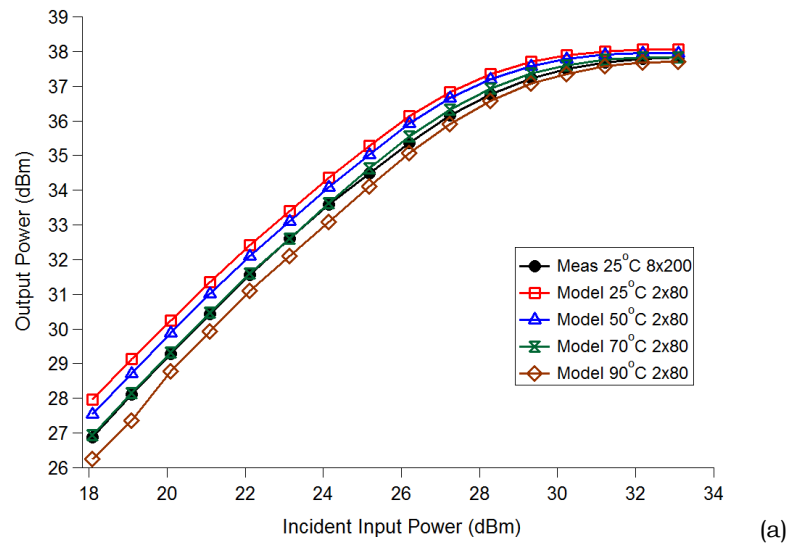
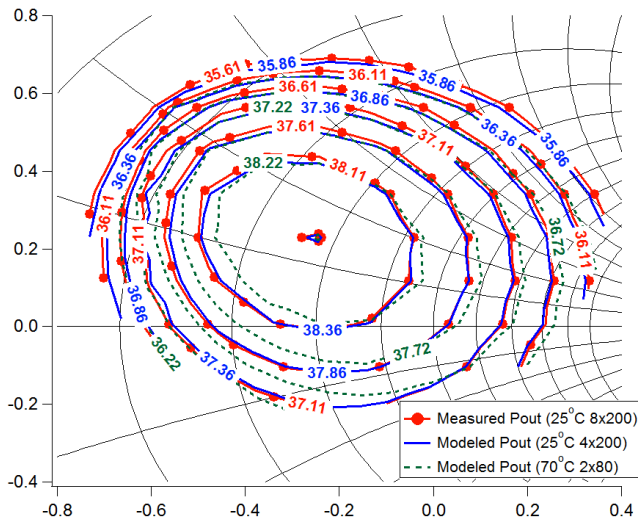


Figure 3-47: Power sweep results as a function of input power at optimum load $\Gamma = -0.126 + j0.452$ with different temperatures (a) P_{out} (b) Drain Efficiency.

In other words, the scalability of the models can be improved by taking into account the junction temperature of the device which is beyond the scope of this work. The model used in this research only uses ambient temperature of the chuck as a look-up parameter. Further work is needed to include the effects of junction temperature into the model coefficients and avoid being another look-up parameter.

3.5.3 Modelling with different reference device

A method to address the limitations of scaling is not to scale beyond the limits as indicated by the DCIVs and S-parameter data. Fig. 3-48(a)-(b) and 3-49 show the results of using the 4x200 μm transistor as the reference device for model extraction (scaling factor of 2).

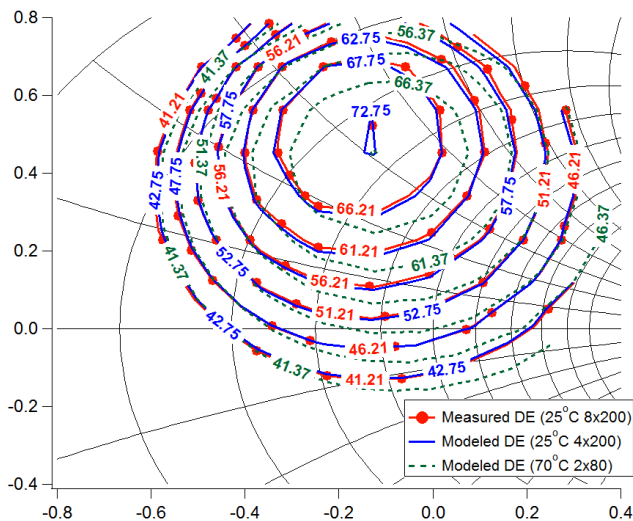


Measured contours - in 0.5 dB steps from maximum of 38.61 dBm.

Modeled with 25°C 4x200 μm - in 0.5 dB steps from maximum of 38.86 dBm.

Modeled with 70°C 2x80 μm - in 0.5 dB steps from maximum of 38.72 dBm.

(a)



Measured contours - in 5 % steps from maximum of 71.21 %.

Modeled with 25°C 4x200 μm - in 5 % steps from maximum of 72.75 %.

Modeled with 70°C 2x80 μm - in 5 % steps from maximum of 71.37 %.

(b)

Figure 3-48: Measured versus modelled P_{out} and Drain Efficiency contours for the 8x200 μm device at a P_{incident} of 32.18 dBm. (a) P_{out} contours (b) Drain Efficiency contours.

The results of the model extracted from the 2x80 μm device measured at 70°C are also included. From the results, it proves that any device can be used as

the reference device for the model. To obtain accurate results, the scaling factor cannot be too large unless temperature effects are taken into account in the model.

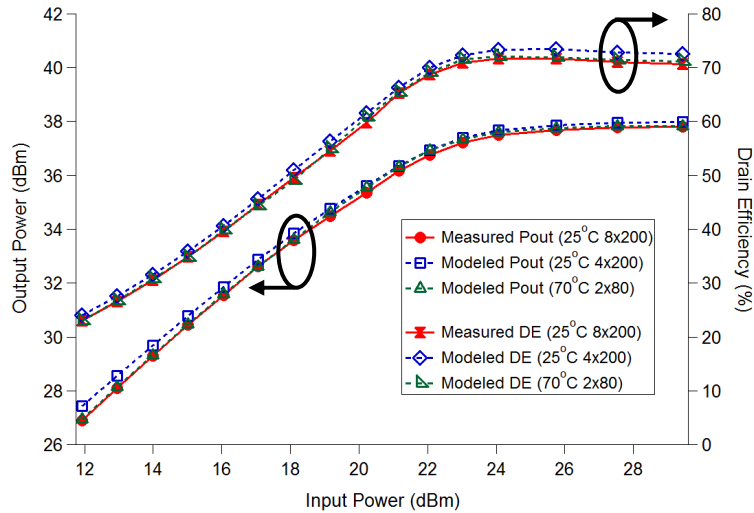


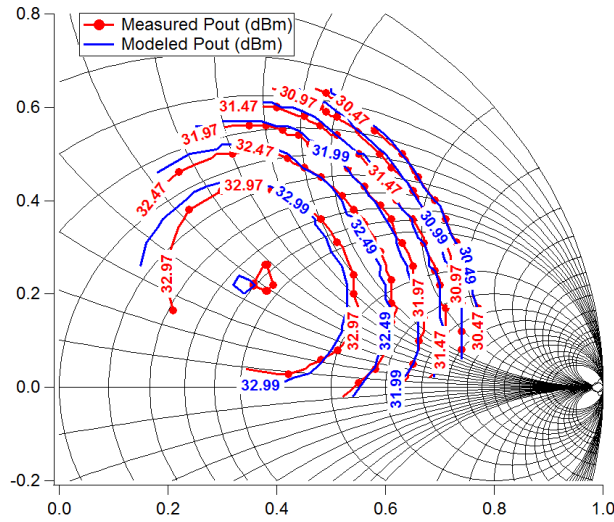
Figure 3-49: Measured versus modelled P_{out} and Drain Efficiency from power sweep at optimum load $\Gamma = -0.126 + j0.452$ for the $8 \times 200 \mu\text{m}$ device.

3.6 Robustness of Scalable Model

This section attempts to show that the method used for implementing the scalable model is robust and can be applied to measurements performed at different bias points, wafers or frequencies.

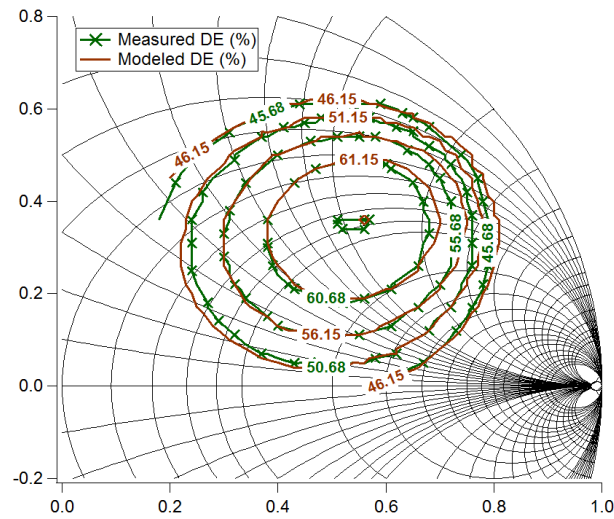
3.6.1 Scaling at different bias point (Class AB)

Measurements were performed on a $2 \times 100 \mu\text{m}$ reference device and used to model a $2 \times 200 \mu\text{m}$ device at Class AB bias ($I_d = 250 \text{mA/mm}$). Fig. 3-50(a)-(b) shows the load-pull results at a $P_{incident}$ of 21.04 dBm whereas Fig. 3-51 shows the power sweep results at the optimum load of $\Gamma = 0.425 + j0.310$.



Measured contours - in 0.5 dB steps from maximum of 33.47 dBm.
 Modeled contours - in 0.5 dB steps from maximum of 33.49 dBm.

(a)



Measured contours - in 5 % steps from maximum of 65.68 %.
 Modeled contours - in 5 % steps from maximum of 65.15 %.

(b)

Figure 3-50: Measured versus modelled P_{out} and Drain Efficiency contours for the $2 \times 200 \mu\text{m}$ device at a $P_{incident}$ of 21.04 dBm measured at Class AB bias. (a) P_{out} contours (b) Drain Efficiency contours.

The maximum error for P_{out} and Drain Efficiency in the power sweep is within 0.17 dB and 1.81 % respectively. The model from the $2 \times 100 \mu\text{m}$ device extracted here will be used for the design of the MMIC prototype in Chapter 4.

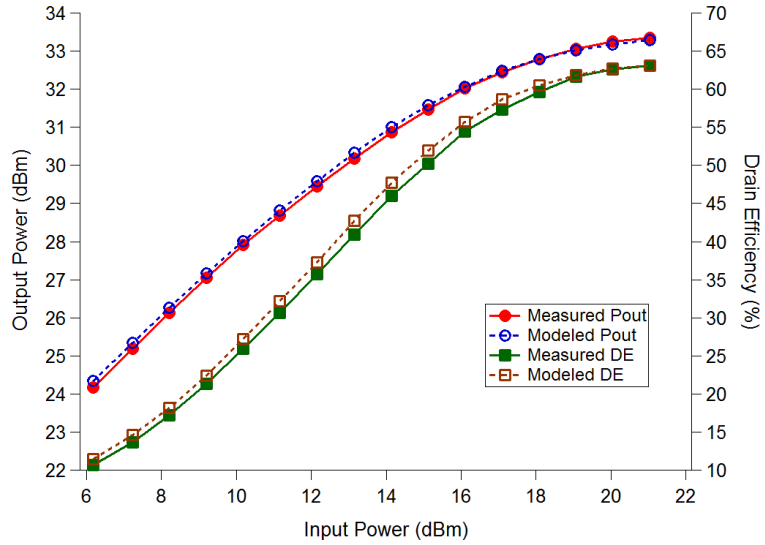


Figure 3-51: Measured versus modelled P_{out} and Drain Efficiency from power sweep at optimum load $\Gamma = 0.425 + j0.310$ for the $2 \times 200 \mu\text{m}$ device at Class AB bias.

3.6.2 Scaling beyond measurement system power capability

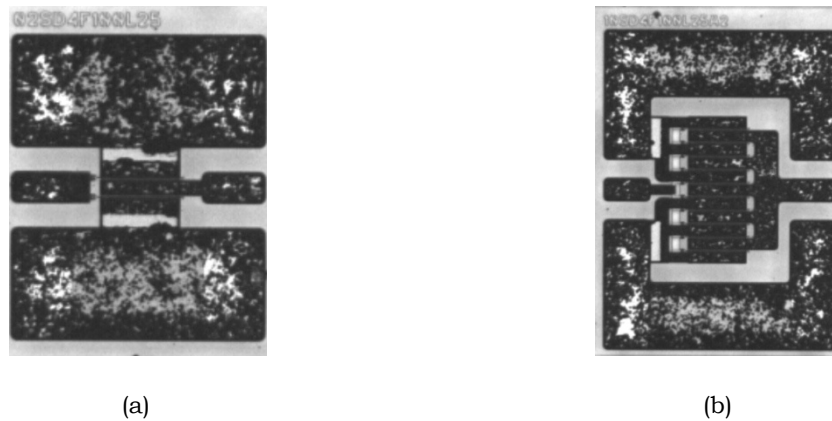


Figure 3-52: Photos of the transistors from WIN wafer ID: EN004013 (a) $2 \times 125 \mu\text{m}$ (b) $10 \times 125 \mu\text{m}$.

The results in this subsection are devices from another WIN Semiconductors wafer (Wafer ID: EN004013), fabricated using the NP25-00 process and at a fundamental frequency of 9 GHz. The 2 devices characterised are the $2 \times 125 \mu\text{m}$ and the $10 \times 125 \mu\text{m}$. The photos of the devices are shown in Fig. 3-52(a)-(b).

Fig. 3-53(a)-(d) is a small signal verification to show that at low drive levels the model matches up with S-parameters. This process has been described in Section 3.2.1. Fig. 3-54(a)-(b) show the P_{out} and Drain Efficiency contours at a $P_{incident}$ of 32.8 dBm.

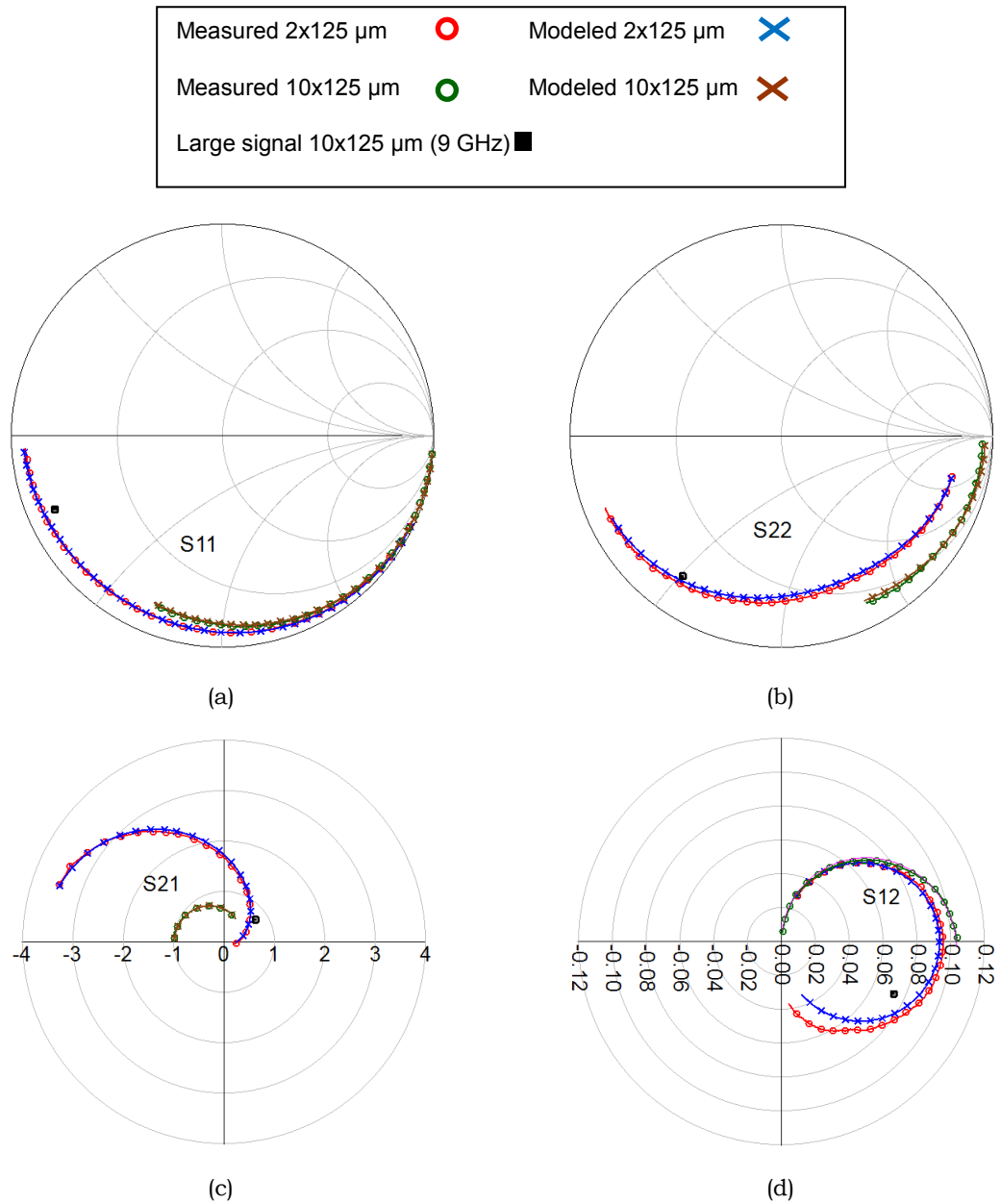
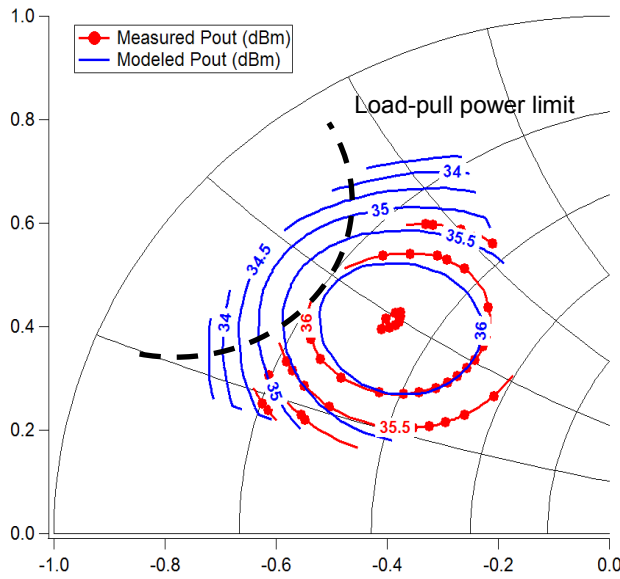
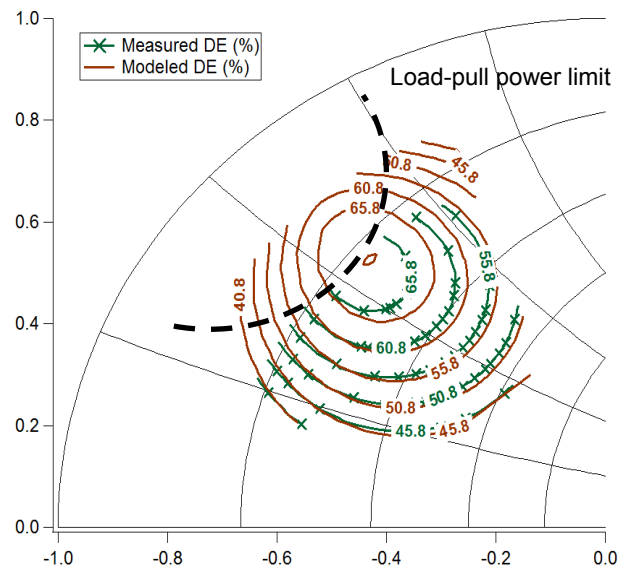


Figure 3-53: S-parameter results with large signal S-parameter at 9 GHz for 2x125 μm and 10x125 μm devices. (a) S_{11} (b) S_{22} (c) S_{21} (d) S_{12}



Measured contours - in 0.5 dB steps from maximum of 36.5 dBm.
 Modeled contours - in 0.5 dB steps from maximum of 36.5 dBm.

(a)



Measured contours - in 5 % steps from maximum of 70.8 %.
 Modeled contours - in 5 % steps from maximum of 70.8 %.

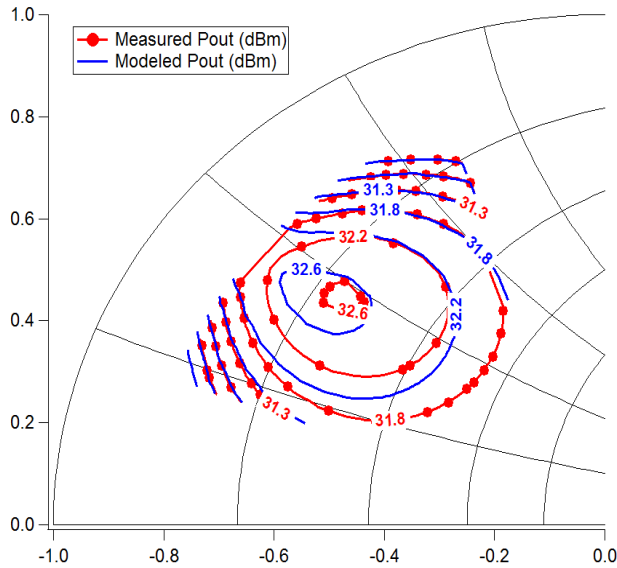
(b)

Figure 3-54: Measured versus modelled P_{out} and Drain Efficiency contours for the $10 \times 125 \mu\text{m}$ device at a $P_{incident}$ of 32.8 dBm. (a) P_{out} contours (b) Drain Efficiency contours.

Fig. 3-54(a)-(b) also shows the measured fundamental load points, which in this case, have been limited in range due to the saturation of the load pull amplifier [27]. The scaled model on the other hand, experiences no such limitation and goes on to predict the behaviour of the 1.25 mm device beyond the measurement capabilities of the system. The load-pull power required to perform active load-pull, P_{LP} can be calculated using equation (3-41) by taking

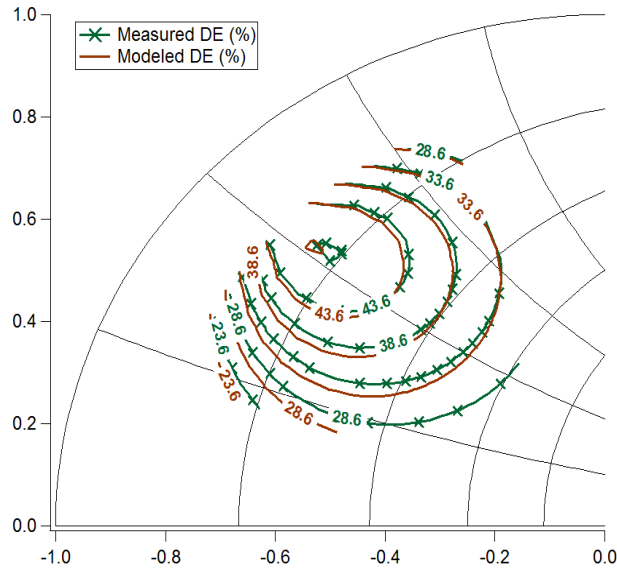
into account the power delivered by the device, P_d and the target load-pull reflection coefficient, Γ_{LP} .

$$P_{LP} = \frac{P_d |\Gamma_{LP}|^2}{1 - |\Gamma_{LP}|^2} \tag{3-41}$$



Measured contours - in 0.5 dB steps from maximum of 32.6 dBm.
 Modeled contours - in 0.5 dB steps from maximum of 32.6 dBm.

(a)



Measured contours - in 5 % steps from maximum of 48.6 %.
 Modeled contours - in 5 % steps from maximum of 48.6 %.

(b)

Figure 3-55: Measured versus modelled P_{out} and Drain Efficiency contours for the $10 \times 125 \mu\text{m}$ device at a $P_{incident}$ of 28.3 dBm. (a) P_{out} contours (b) Drain Efficiency contours.

To further demonstrate that the model corresponds well with the measurement data, load-pull contours of output power and drain efficiency

are shown in Fig. 3-55(a)-(b), for a case where the P_{incident} power is backed off by to 28.3 dBm, allowing the full grid to be measured.

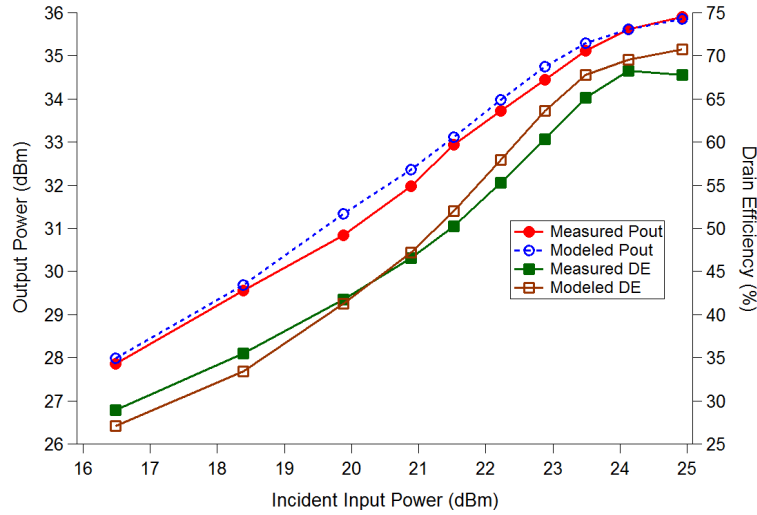


Figure 3-56: Measured versus modelled P_{out} and Drain Efficiency from power sweep at optimum load $\Gamma = -0.450 + j0.536$ for $10 \times 125 \mu\text{m}$ device.

Fig. 3-56 compares a measured and modelled power sweep plot of P_{out} and Drain efficiency versus P_{incident} at the optimum point of $\Gamma = -0.450 + j0.536$. These results show that it is possible to accurately predict the performance of the device at power levels beyond the limitations of the high frequency measurement system.

3.7 Summary

The key contribution of this chapter is proving that geometric scaling is possible using a generalized Behavioural model formulation. Having a model that is able to scale geometrically greatly improves its functionality and provides a viable MMIC design tool. A systematic procedure to generate the geometric scalable Behavioural models has been proposed and validated. It combines the accurate measurements of measurement based non-linear look-up table transistor models with passive embedding networks.

The process involves 4 main steps, which are, determining the intrinsic plane of the transistor, obtaining the large signal measurement data for conversion into Behavioural models, performing scaling at the intrinsic reference plane and embedding with the passive circuit of the scaled device. Practical considerations when generating the Behavioural model involves avoiding re-gridding of the data by extracting the reference model at the extrinsic plane.

The scalable model is able to successfully predict the performance of devices up to 5 times larger in gate periphery on 2 separate GaN wafers, one measured at 5 GHz and another at 9 GHz. Furthermore, this process is robust as the model is able to extrapolate beyond the power limitations of the measurement system, providing the ability to design high power MMICs without having to physically measure the large transistors at high power levels.

Work has also been done to show the limitations of the proposed approach and ways to overcome them. Important indicators of scalability are the DCIVs and S-parameters. Scalability of the model can be improved by including thermal effects or by sticking to a realistic scaling factor. Note that during the design process, this method can be applied to MMIC building blocks containing several transistors (and not one individual transistor model) so that the scaling factor can be reduced to a range which provides an acceptable accuracy.

Having a scalable Behavioural model ultimately overcomes a major weakness of Behavioural (measurement based) models by reducing the number of devices to be characterized. This saves measurement time and reduces the burden placed on the measurement system.

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CHAPTER 4

APPLICATION OF GEOMETRIC SCALABLE MODEL IN MMIC DESIGN

X-parameter models have been used in various publications for design purposes. These include designs for a 6W 2 GHz GaN power amplifier [1], a 10W 1.3 GHz GaN power amplifier [2], a Doherty amplifier [3], frequency doubler [4] and even oscillators [5]-[6]. So far, no design has been performed using a geometric scalable Behavioural model.

In order to test the model that has been extracted, a prototype single cell amplifier is matched with matching circuits at the input and output. In this chapter, the design process and tools used for the circuit optimized for 5 GHz will be presented along with modelled and measurement results. Although the targeted output power and drain efficiency wasn't achieved due to mismatch, the model is still able to predict the prototype's performance accurately when the measured matching circuit S-parameters and appropriate bond wire lengths are used.

4.1 Introduction

M/A-COM foundry's GaAs integrated passive design (IPD) process were used to design the external matching circuits. These matching circuits were then wire bonded to the 2x200 μm GaN on SiC transistor from WIN Semiconductors (Wafer ID: WN001A) which has been characterized in Chapter 3, to form the

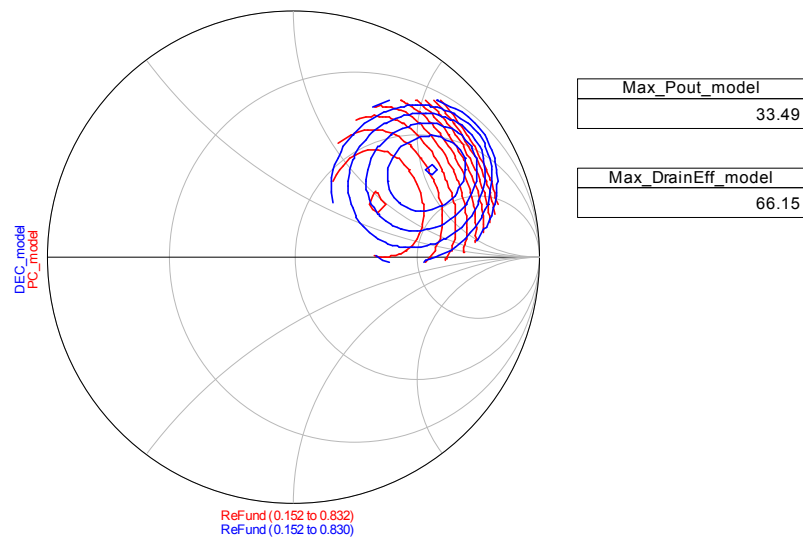
prototype amplifier. A scalable model has been developed for this device based on a smaller unit cell of $2 \times 100 \mu\text{m}$ (scaling factor of 2). This model has already been verified to match the measured results of the $2 \times 200 \mu\text{m}$ device in Section 3.6.1.

4.2 Circuit design using CAD simulators

4.2.1 Finding optimum load

Using the data extracted from the measurements of the $2 \times 100 \mu\text{m}$ device at Class AB bias ($I_d = 250 \text{ mA/mm}$), load-pull simulation is performed in ADS on the scalable model to obtain the optimum load point.

From the results of the load-pull at 5 GHz in Fig. 4-1(a), the maximum P_{out} achievable is 33.49 dBm whereas the maximum Drain Efficiency is 66.15%. Therefore, the optimum load of $\Gamma = 0.425 + j0.310$ is chosen as a target as shown in Fig. 4-1(b). At this load, the P_{out} and Drain Efficiency is 33.28 dBm and 63.07 % respectively. The output matching circuit will be designed to try to obtain this load.



(a)

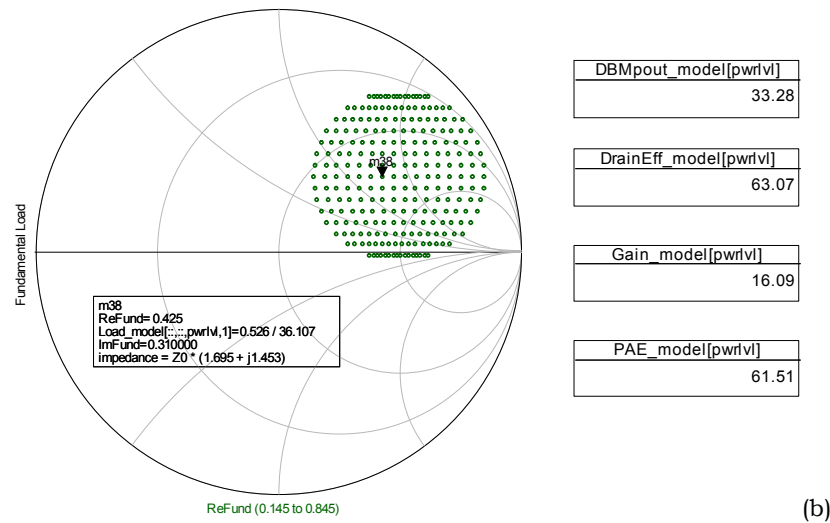


Figure 4-1: Load-pull simulation results at 5 GHz using scalable model (a) P_{out} and Drain Efficiency contours (b) Optimum load location

4.2.2 Output matching circuit

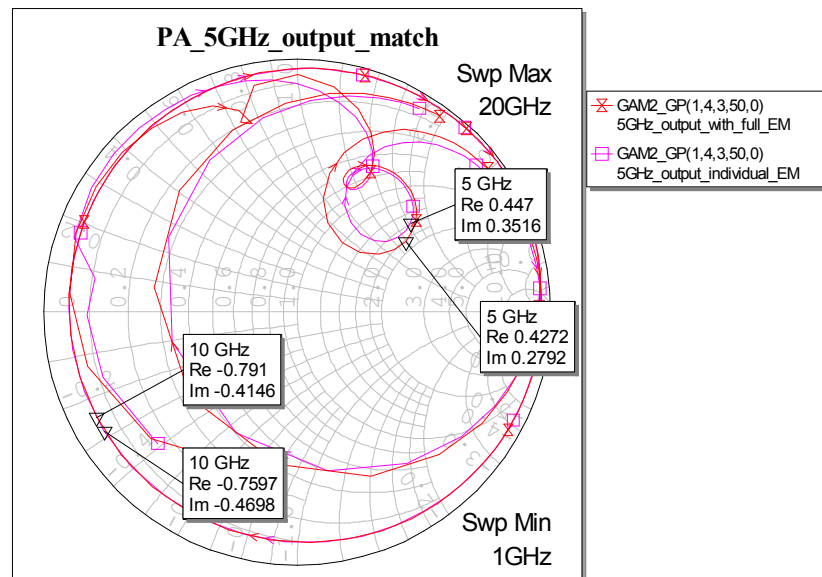
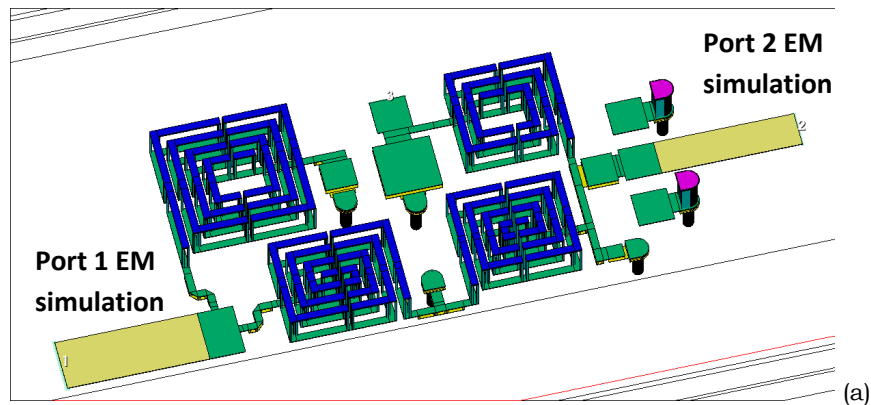
At the output, the matching circuit was designed to present the optimum load to the device. Design and layout of the components are done in Microwave Office AWR due to the availability of the licence for AXIEM to perform the required EM simulations.

The component values were first selected and tuned with lumped elements. Once their values have been selected, electromagnetic simulations for each inductor, capacitor and via are performed to obtain their S-parameters. Finally, the entire circuit is EM simulated with all the elements in place to take into account any cross coupling or mutual inductance.

Fig. 4-2(a) shows the EM simulation setup for the output matching circuit. The reflection coefficient looking into the matching circuit at the port 1 (which is presented to the output of the amplifier) is shown in Fig. 4-2(b). The comparison between simulation results where each component is individually

EM simulated and when EM simulation is performed on the entire matching circuit is shown.

Fig. 4-2(c) is the layout of the output matching circuit that will be converted into a .gds file for tape out. Note that the simulation results were performed by taking into account the addition of an 1850 μm bond wire that will connect the matching circuit to the transistor. From the results, the output circuit is able to get close to the optimum target load of $\Gamma = 0.425 + j0.310$ to obtain a high P_{out} and Drain Efficiency while presenting a short circuit to the 2nd harmonic.



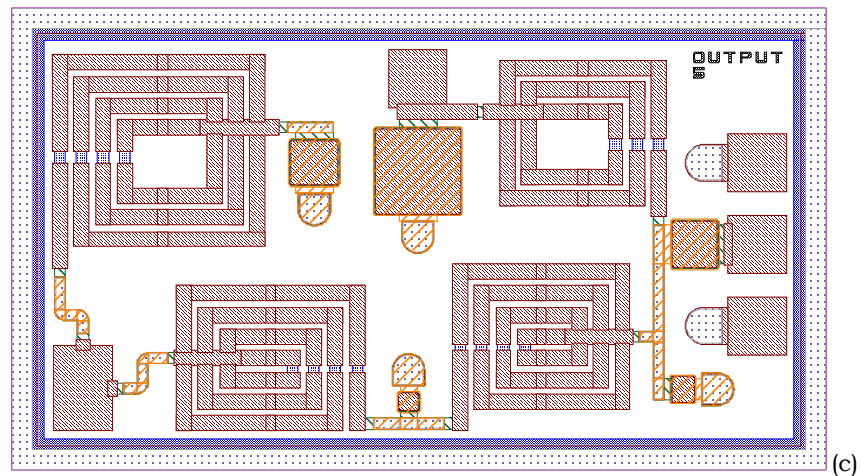
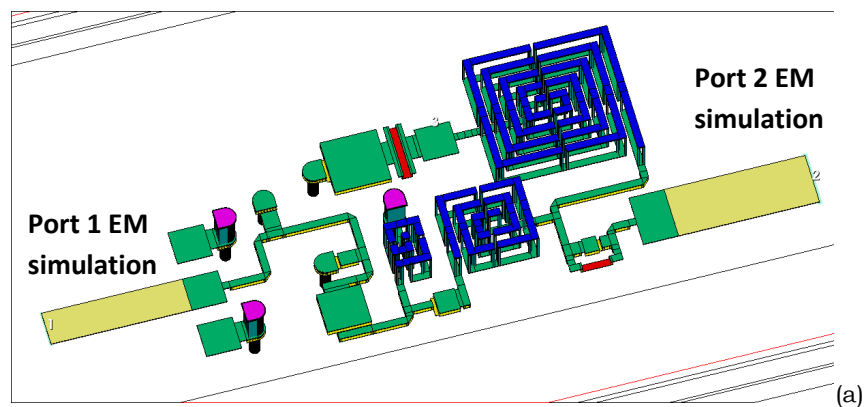
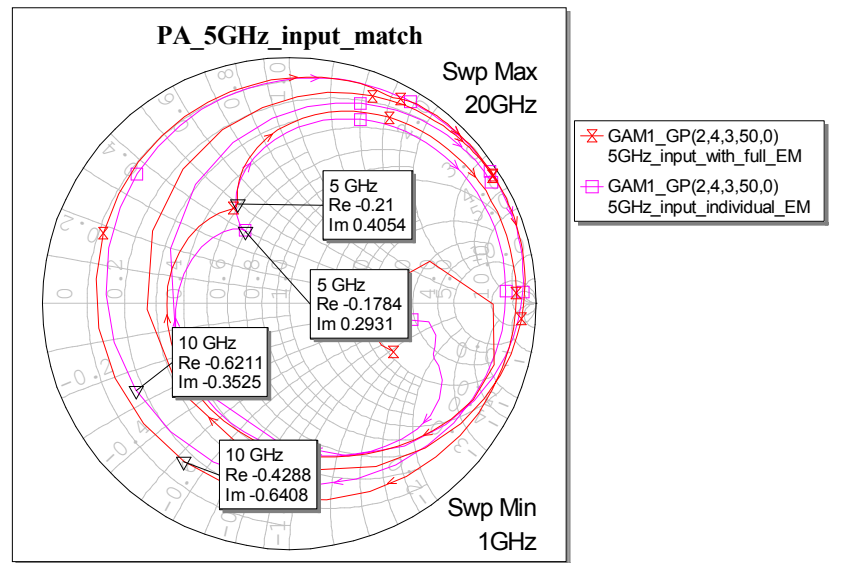


Figure 4-2: Output matching circuit design (a) EM setup of output circuit (b) Output Gamma presented to the device (c) Layout of output matching circuit

4.2.3 Input matching circuit

The input circuit is designed to allow for maximum available gain, G_{\max} while still maintaining stability (K factor > 1). This result will be shown in Section 4.2.4. Other considerations that are taken into account include having a return loss of better than 10 dB.





(b)

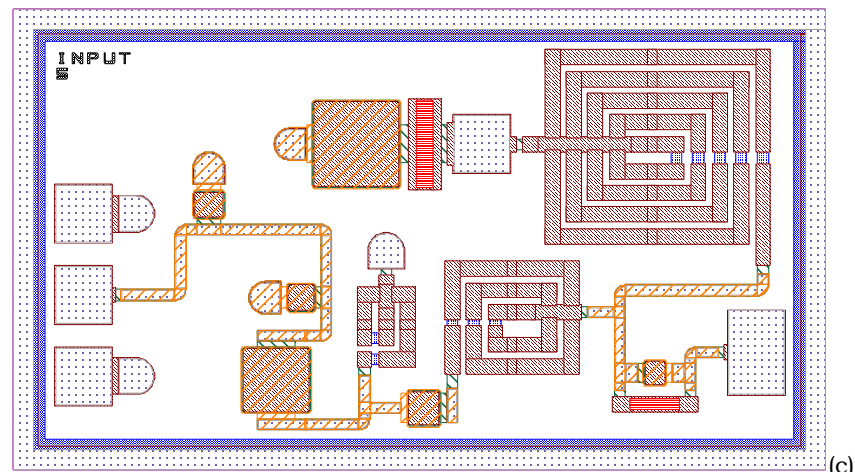


Figure 4-3: Input matching circuit design (a) EM setup of output circuit (b) Input Gamma presented to the device (c) Layout of input matching circuit

Fig. 4-3(a) shows the EM simulation setup for the input matching circuit. The reflection coefficient looking into the matching circuit at port 2 (which is presented to the input of the amplifier) is shown in Fig. 4-3(b). Fig. 4-3(c) is the layout of the input matching circuit that will be taped out.

4.2.4 Simulated prototype results

The small signal simulation setup is shown in Fig. 4-4 with external bond wires taken into account.

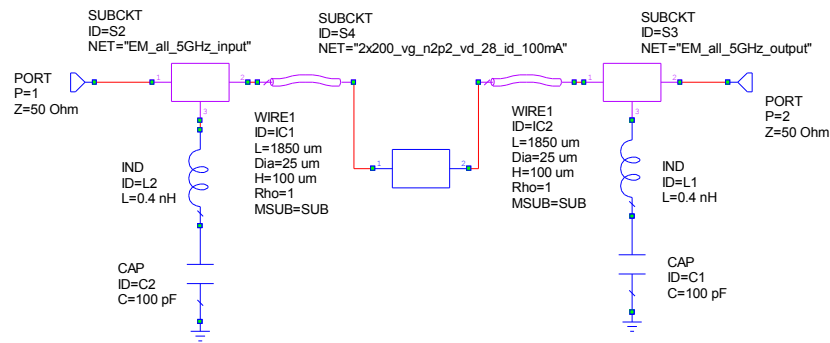
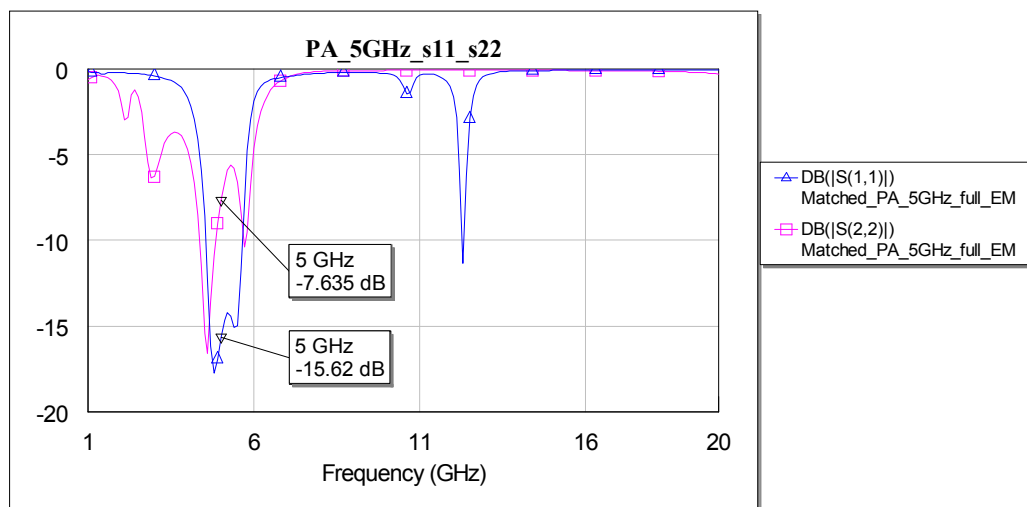
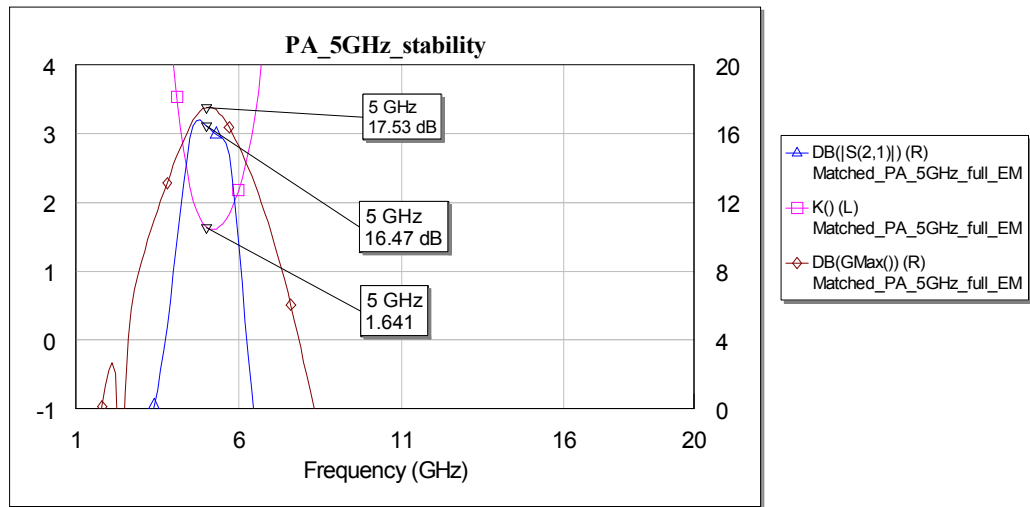


Figure 4-4: Small signal simulation setup in AWR Microwave Office with external bond wires.

From the results of the simulation in Fig. 4-5(a)-(b), the return loss is < -10 dB for the input and due to the output having to match for optimum P_{out} and Drain Efficiency, the return loss is -7.513 dB. The gain is 16.43 dB at 5 GHz, close to the G_{max} of 17.47 dB and the K-factor (stability factor) is > 1 in band and also out of band. The 0.4 nH inductor and 100 pF capacitor at the DC lines represent the bond wires and the external capacitor for the DC probes.



(a)



(b)

Figure 4-5: Targeted results for small signal (a) S_{11} and S_{22} (b) S_{21} and Stability

Now that the small signal results are satisfactory, the matching circuit and bond wire S-parameters are used in ADS together with the scalable model to simulate the expected power sweep results. The implementation is shown in Fig. 4-6(a)-(c).

Note in Fig. 4-6(a) that the FDD reads the extrinsic Cardiff model file of a smaller reference device ($2 \times 100 \mu\text{m}$). It is then de-embedded to the intrinsic plane using parasitic circuit elements of the $2 \times 100 \mu\text{m}$ device. Please refer to Section 3.2.5 for these values.

At the intrinsic plane, the voltages remain the same whereas the current is scaled by a factor of 2 via the ABCD component. These results then are embedded with the parasitics for a $2 \times 200 \mu\text{m}$ device (shown in Fig. 4-6(b)). Finally, the larger device is presented with the external matching circuit and bond wires as depicted in Fig. 4-6(c).

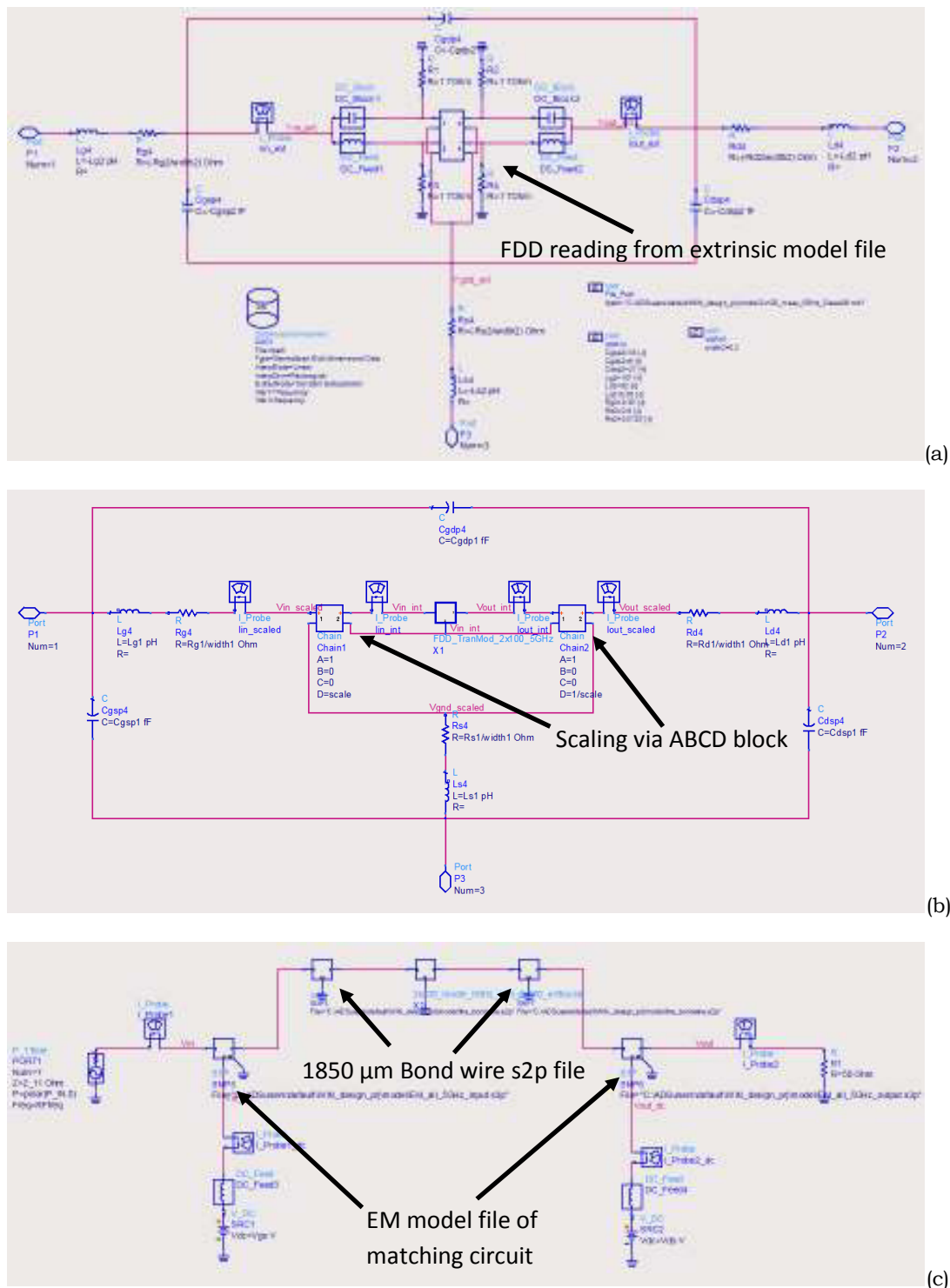


Figure 4-6: ADS simulation for large signal results utilizing scalable Behavioural Model (a) FDD block with de-embedding circuit (b) Scaling block with embedding circuit (c) Transistor with input and output matching circuits.

To keep the simulation consistent with AWR, the bond wires are implemented using .s2p files generated from AWR. The ADS circuit implementation shown here has been discussed in detail in Section 3.4.2.

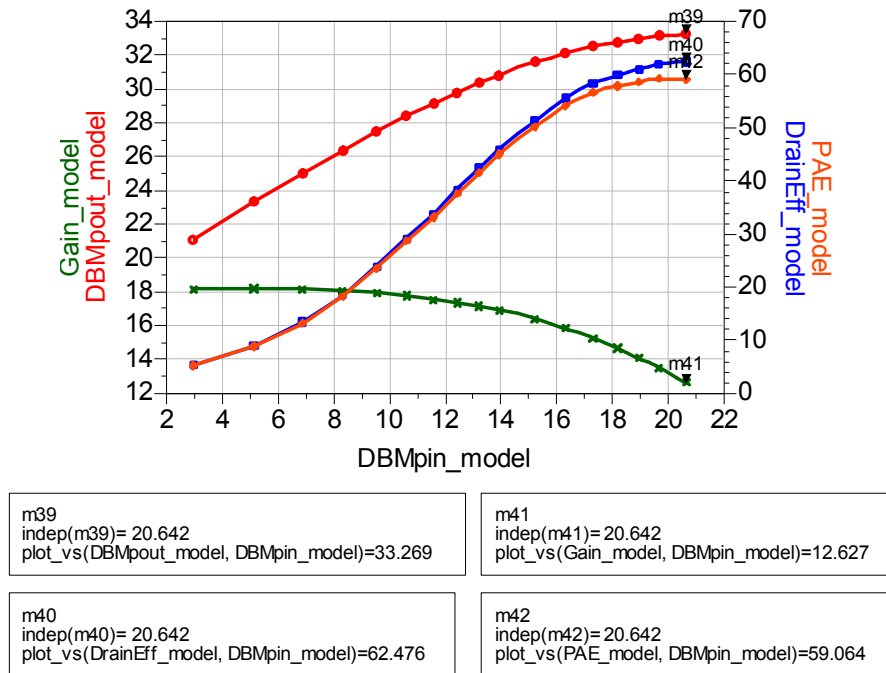


Figure 4-7: Targeted large signal simulation results of 5 GHz prototype with input and output matching circuits

Fig. 4-7 shows the results of a power sweep into 50 ohms when the matching circuit is attached to the model. These results agree closely with the load-pull data from Fig. 4-1 (b).

4.2.5 Actual fabricated circuit

Fig. 4-8(a)-(b) are the photographs of the fabricated input and output matching circuits whereas Fig. 4-8(c) shows the entire prototype with bond wires to the active device (2x200 μm GaN on SiC device).

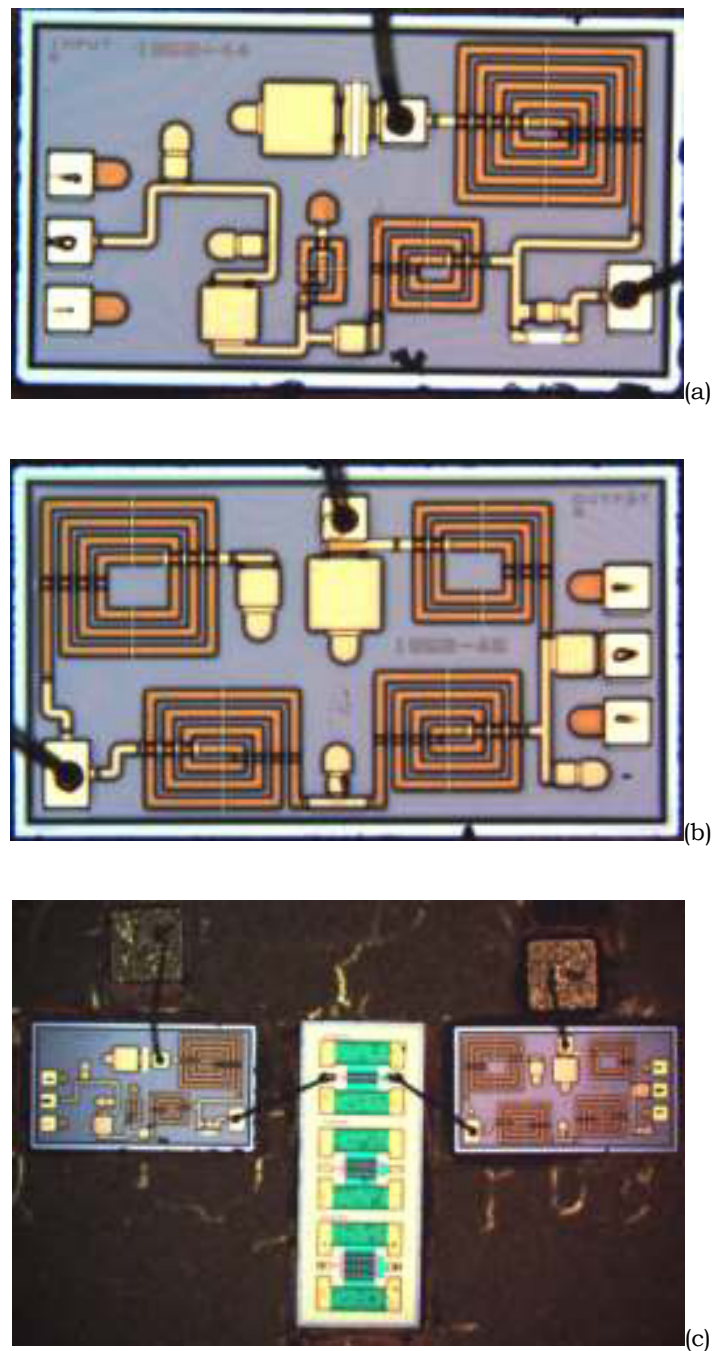


Figure 4-8: Photo of fabricated circuit (a) Input matching circuit (b) Output matching circuit (c) Entire prototype with external bond wires.

From Fig. 4-8(c) it can be seen that the matching circuits also contain probe pads that are connected via bond wires to a 100 pF external capacitor where it can be accommodate DC probes.

4.3 Measured and modelled results

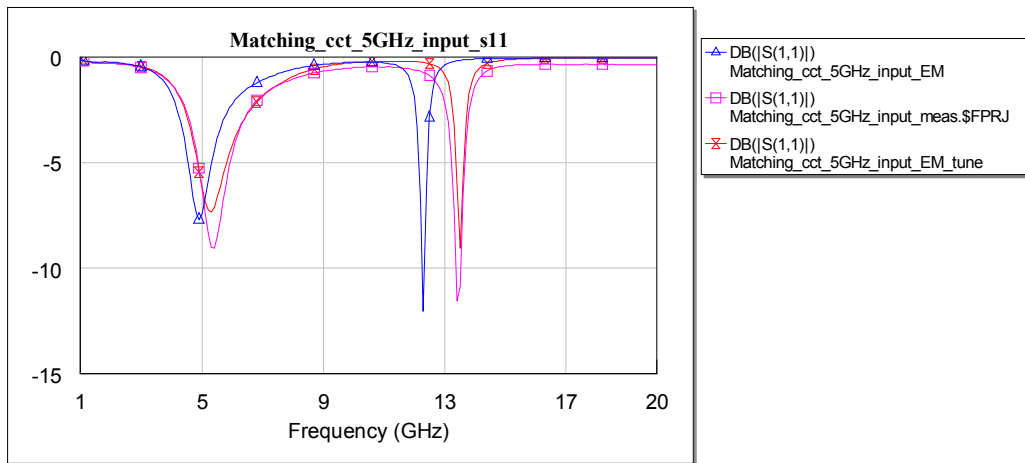
During the design process, large inductance values were needed to match the circuit. The size of the inductor makes it unable to physically fit onto the die area. Therefore, long bond wires were introduced for the extra inductance that is needed. However, this poses a challenge as it would require manual tuning to get the exact inductance values.

Nevertheless, this entire point of the exercise is to show that the models can accurately predict the behaviour of the circuit. So by measuring the actual response of the matching circuit and replacing them into the simulation, the model should be able to show the appropriate outcome as well.

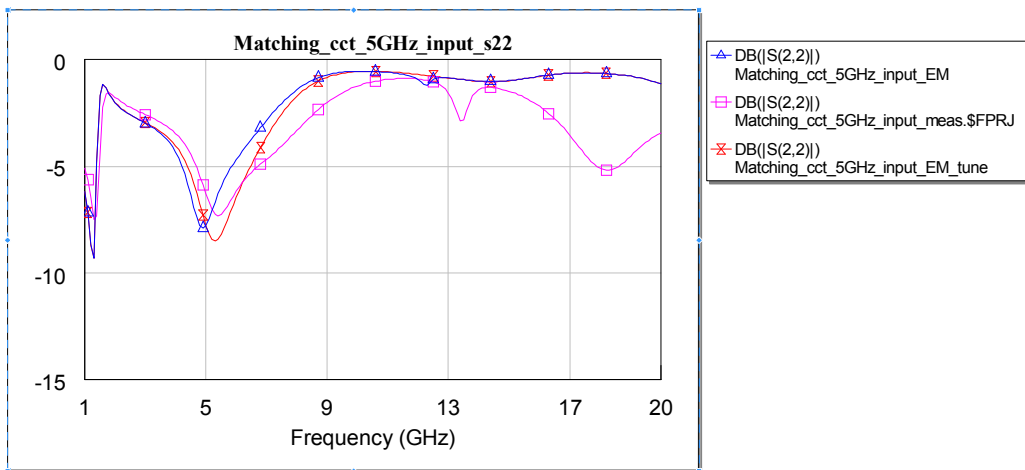
4.3.1 Small signal results

4.3.1.1 Individual Input and Output Matching Circuits

Firstly, the response of each matching circuit is compared with the EM simulations. The results in this section correspond to measurements performed on the input matching circuit shown in Fig. 4-8(a) and the output matching circuit in Fig. 4-8(b). These small signal results of the individual matching circuits (without bond wires) are shown in Fig. 4-9(a)-(b) for the input and Fig. 4-10(a)-(b) for the output.



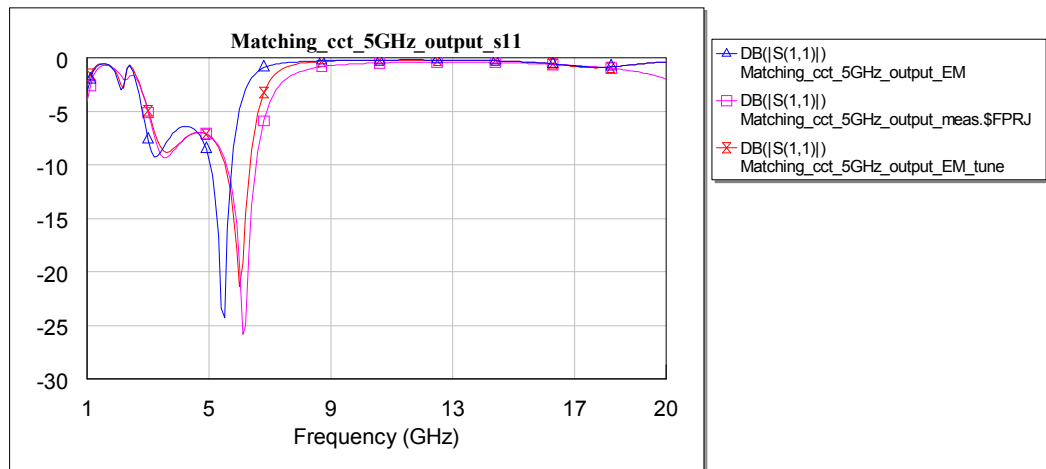
(a)



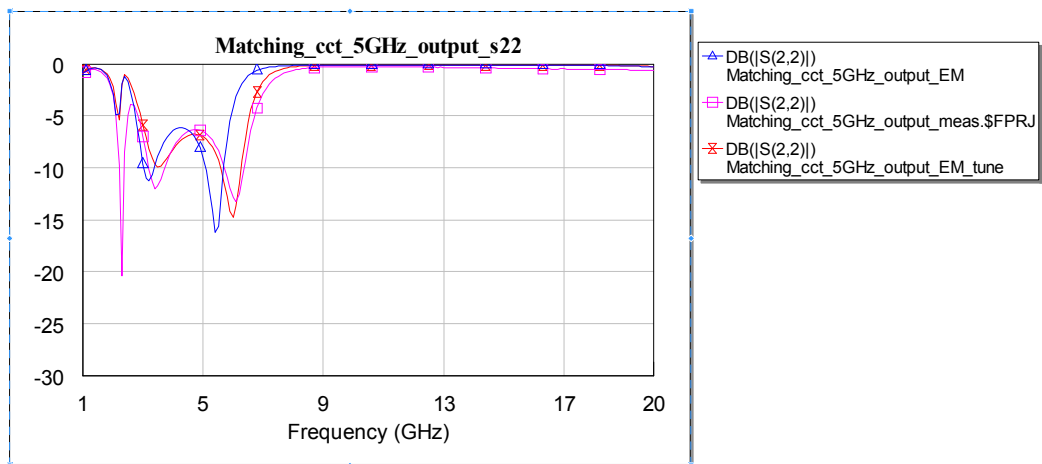
(b)

Figure 4-9: Comparison of small signal results for input matching circuit between measured and EM models (a) S_{11} (b) S_{22}

From the results, there is a slight shift in the frequency response of the measured results (shown in pink) with the EM simulations (in blue). The matching circuit results were sensitive to the capacitors in the circuits. Therefore, by performing the EM simulation again with the capacitors retuned, the S-parameters (in red) are obtained. These small signal results now match up well with the measured ones.



(a)



(b)

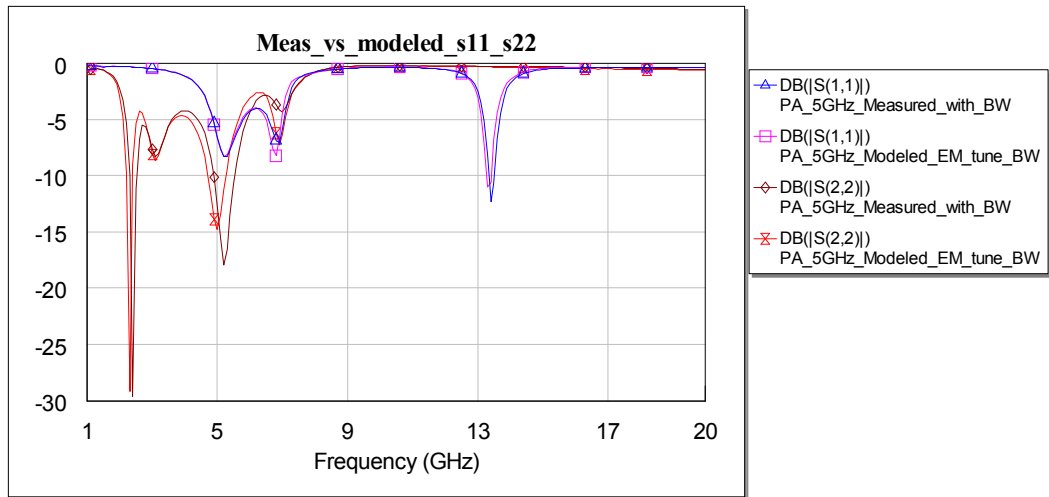
Figure 4-10: Comparison of small signal results for output matching circuit between measured and EM models (a) S_{11} (b) S_{22}

4.3.1.2 Prototype with Matching Circuits

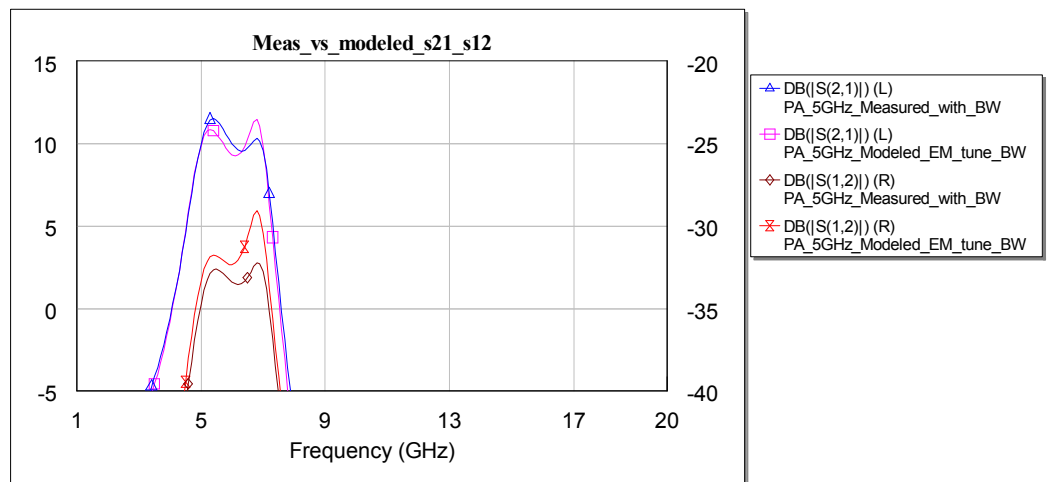
The results in this section correspond to measurements performed on the prototype with bond wires attached to input and output matching circuits as illustrated in Fig. 4-8(c). The bond wires that were physically used were much shorter than the intended length.

To calculate the bond wire inductance in the fully matched prototype, the measured small signal results of the entire circuit is compared with the

retuned EM results of the individual matching circuits but now with a variable bond wire inductance.



(a)



(b)

Figure 4-11: Comparison of small signal results of fully matched prototype between measured and EM models (a) S_{11} and S_{22} (b) S_{21} and S_{12}

With a bond wire of roughly $300\ \mu\text{m}$ at both the input and output of the matching circuits, the modelled small signal results are in close agreement with the measured ones as shown in Fig. 4-11(a)-(b).

4.3.2 Large signal results

Due to physical constraints, a long bond wire of 1850 μm was not able to be placed at input and output of the active device. However, the goal of the modelling work is to show that the scalable model is able to predict the large signal results regardless of whether the matching circuits are able to present the optimum impedance to the device.

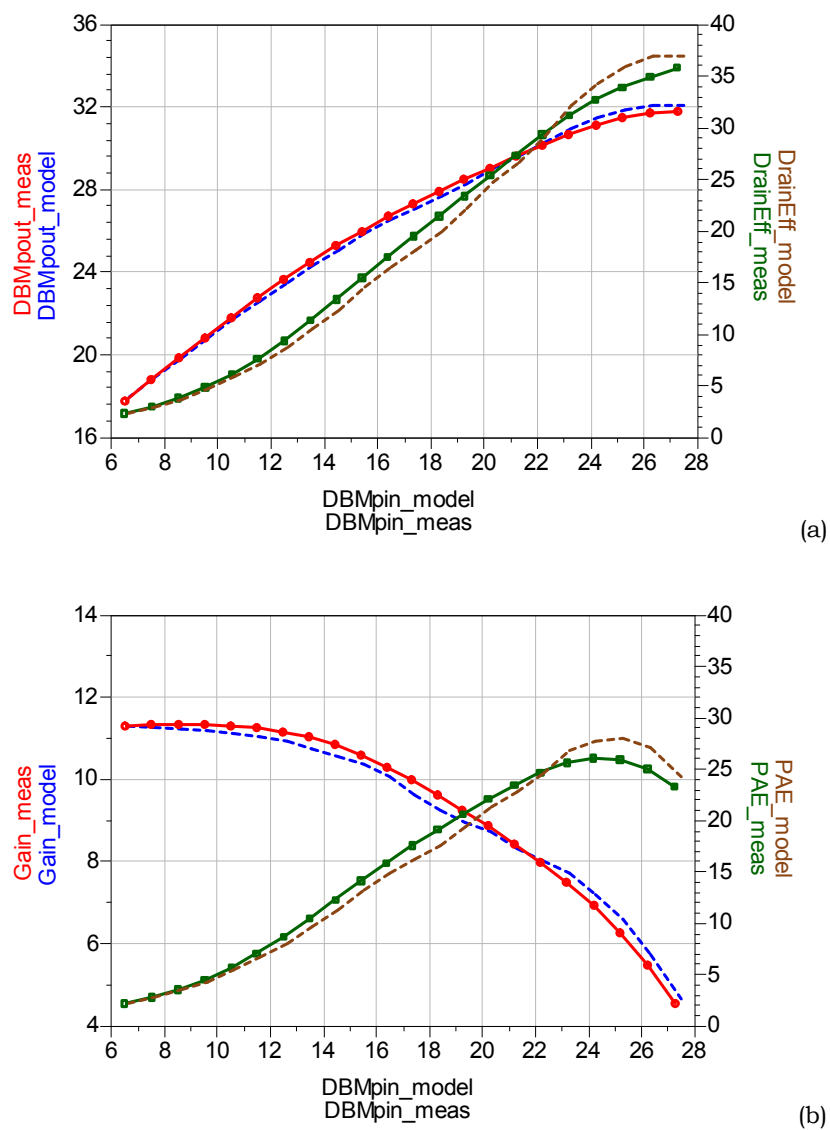


Figure 4-12: Comparison of large signal results of fully matched prototype between measured and scalable model (a) P_{out} and Drain Efficiency (b) Gain and PAE

Performing the large signal simulations but now with the actual measured response of the input and output matching circuits as well as bond wires of about 300 μm , the large signal performance is shown in Fig. 4-12(a)-(b). This involves replacing the EM simulations of the matching circuits in Fig. 4-6(c) with the actual measured S-parameters as illustrated in Fig. 4-13.

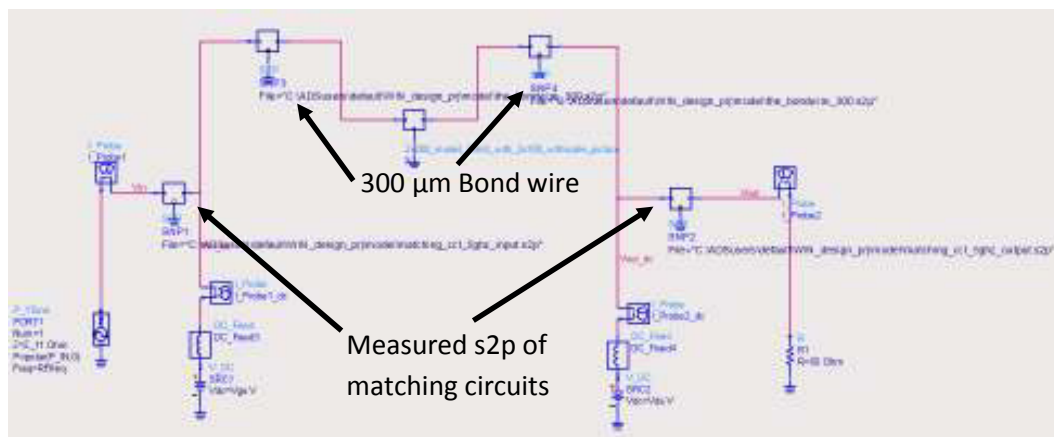


Figure 4-13: ADS simulation for large signal results utilizing scalable Behavioural Model with measured s2p of matching circuits and 300 μm bond wires.

The simulations were performed at the same P_{incident} drive as the measured results in order to put them under the same stimulus conditions. The measured versus modelled P_{out} and Drain Efficiency are within 0.43 dBm and 2.03% respectively. The results for Gain and PAE are within 0.33 dB and 2.12%. Therefore, the scalable model is able to predict the results of the prototype when simulating with the actual matching circuits that were fabricated.

4.4 Summary

A prototype for 5 GHz operation has been designed using the scalable model extracted from measurements. Although the intended performance was not achieved due to issues encountered during module assembly, the scalable

non-linear model was still able to correctly predict the measured performance of the prototype when the actual measured S-parameters of the matching circuits were used during CAD.

The issues encountered in this design were due to the use of external matching circuits and module assembly (instead of having all the matching circuits on a single MMIC die). This firstly places a frequency limitation in the design specifications and secondly, makes the performance difficult to achieve without spending time to tune the bond wire lengths.

Nevertheless, the key point in this chapter is the demonstration that the scalable non-linear Behavioural model can be used to guide design and also predict the performance of the actual fabricated circuit.

By demonstrating the application of scalable models in design of MMICs, possibilities are now open to the use of scalable Behavioural models in the same manner as Compact models. Compact models are generally measured at a nominal cell size and then scaled to various other sizes, thus saving measurement time and effort.

4.5 References

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- [4] J. Cai, T.J. Brazil, "X-parameter-based frequency doubler design," *2012 7th European Microwave Integrated Circuits Conference (EuMIC)*, pp.794-797, 29-30 Oct. 2012.
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- [6] A.M. Pelaez-Perez, S. Woodington, J.I. Alonso, M. Fernandez-Barciela, P.J. Tasker, "X-parameters-based closed-form expressions for evaluating power-dependent fundamental negative and positive real impedance boundaries in oscillator design," *IET Microwaves, Antennas & Propagation*, vol.6, no.8, pp.835-840, June 2012.

CHAPTER 5

FREQUENCY SCALABLE BEHAVIOURAL MODELS

This chapter introduces the first formulation and approach that aims to define how measurement based non-linear Behavioural look-up transistor models can be frequency scalable. In the previous chapter, the method for establishing geometric scalable models has been proposed and validated. This was achieved by integrating scalable intrinsic measurement data models of a reference device within passive layout networks.

In this chapter, the work is taken a step further by now referencing the intrinsic transistor in the admittance domain. Experimental results on 2 separate GaN HFETs, both measured from 2 - 8 GHz, support theoretical analysis that frequency domain Behavioural models defined in the admittance domain can have frequency scalable model coefficients.

By having model coefficients in the form that is frequency scalable, experimental results confirm that they can successfully, within an acceptable range consistent with measurement uncertainty, predict results at frequencies that are not used during the measurement based model extraction process. Therefore, this approach can save measurement time and make the models more robust as they now can be used in MMIC design for broadband applications.

5.1 Model Formulation

5.1.1 Introduction

For a fixed DC operating point, parasitic elements can be de-embedded from transistor S-parameters (small-signal) measurements and converted into an intrinsic admittance representation [1]-[2]. At frequencies ranging from inverse thermal and trap emission time constants (kHz range) to cutoff (typically many tens of GHz), the intrinsic admittance matrix can be represented by the sum of a real conductance matrix with frequency independent elements and an imaginary susceptance matrix with elements depending linearly on frequency.

In other words, the contributions from resistive and reactive elements can be separated by taking into account the real and imaginary parts of the intrinsic Y-parameters and the data at one frequency can be used to predict the results over a wide range of frequencies. This has been shown experimentally in Section 3.2.4. However, under large signal excitations, the contributions produced by a non-linear component of 2 or more ports to the complex port current spectra, cannot generally be separated into its real and imaginary parts.

Separating the contributions from two-port FET current and charge sources directly from large-signal measurements was first examined in [3]. It was shown that separating the I and Q contributions required multiple engineered trajectories going through each specific point in the V_{gs} - V_{ds} space. Engineering the excitations at multiple frequencies to approximately achieve the multiple trajectories is an arduous and time consuming process.

In [4], the even and odd symmetry of the Fourier transform of the equation describing the current and charge sources can be exploited to extract a one-

port device's non-linear constitutive relations directly from large-signal measurements. The work in [5] extended the method presented in [4] to two ports by constraining the output impedance presented to the device. As in the previous case, the excitation is constrained in order to apply this concept. In this case, the V_1 and V_2 excitations are forced to be 180 degrees out of phase to establish the even-odd symmetry.

Both of these approaches are based on considering that the intrinsic transistor behaviour can be modelled in the time domain using the state function approach shown in (5-1), where p represents the transistor port (the gate or drain terminals) as shown in Fig. 5-1.

In equation (5-1), the two-dimensional current source and charge source state functions, $I_p^{(CS)}$ and Q_p are time invariant, a typical assumption in most Compact models in which $I_p^{(CS)}$ and Q_p are computed using analytical expressions [6]-[7]. The coefficients of these analytical expressions are determined using a combination of DCIV and bias dependent S-parameter measurements. More advanced approaches have involved I-V and Q-V data look-up concepts [8]-[9].

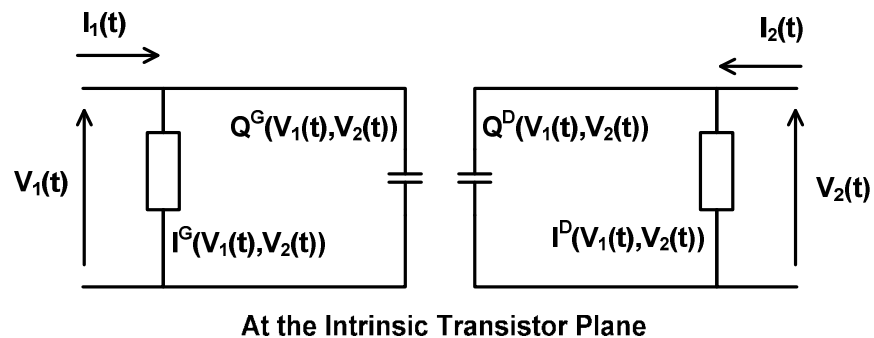


Figure 5-1: Model of intrinsic transistor with current and charge sources.

Assuming small perturbations about a large signal operating point, given by the DC bias state, reference load admittance and fundamental drive level,

theoretical analysis shows that time domain equation (5-1) can be reformulated in the frequency domain giving (5-2) where p and q represent port indices and k and l represent the harmonic of the signal at frequency ω .

$$I_p(t) = I_p^{(CS)}(V_1(t), V_2(t)) + \frac{d}{dt} Q_p(V_1(t), V_2(t)) \quad (5-1)$$

$$\widehat{I}_{p,k} = P_1^k \cdot \left[\begin{array}{c} Y_{pk,11}^{(F)} |V_{1,1}|^k + \\ \sum_{\substack{q=1 \\ l=1 \\ (q,l) \neq (1,1)}}^{q=N, l=K} Y_{pk,ql}^{(S)} V_{q,l} P_1^{-l} + Y_{pk,ql}^{(T)} V_{q,l}^* P_1^{+l} \end{array} \right] \quad (5-2)$$

$$Y_{pk,ql}^{(m)} = G_{pk,ql}^{(m)} + jk\omega C_{pk,ql}^{(m)} \quad (5-3)$$

$$\widehat{I}_{p,k}(\omega_o) = P^k \cdot \left[\begin{array}{c} \left\{ G_{pk,11}^{(F)} + jk\omega_o C_{pk,11}^{(F)} \right\} |V_{1,1}|^k \\ + \sum_{\substack{q=1 \\ l=1 \\ (q,l) \neq (1,1)}}^{q=N, l=K} \left\{ G_{pk,ql}^{(S)} + jk\omega_o C_{pk,ql}^{(S)} \right\} V_{q,l} P^{-l} \\ + \left\{ G_{pk,ql}^{(T)} + jk\omega_o C_{pk,ql}^{(T)} \right\} V_{q,l}^* P^{+l} \end{array} \right] \quad (5-4)$$

The research in this chapter shall set out to prove that all the large-signal admittance Behavioural model coefficients $Y_{pk,ql}^{(m)}$, “Y-parameters”, have the form $G + j\omega C$ as shown in (5-3), hence when extracted at one frequency, they should be usable at another.

Substituting equation (5-3) into (5-2) results in equation (5-4). Notice the similarity of (5-2) with the formulation for X-parameters (based on the Polyharmonic Distortion principles) [10]-[11], except that it is now described in the admittance domain. From the X-parameter formulation, note that for F ($m = 0$), S ($m = 1$) and T ($m = -1$).

5.1.2 Parameter extraction from fundamental "voltage-pull"

This section investigates the validity of equation (5-4). This is best done using a direct extraction approach exploiting engineered voltage stimuli. The required engineered input and output stimulus is described by (5-5) and (5-6) respectively.

$$V_1(t) = V_{1,0} + |v_{1,1}| \cos(\omega t) \quad (5-5)$$

$$\begin{aligned} V_2(t) &= V_{2,0} + |v_{2,1}| \cos(\omega t + \phi) \\ &= V_{2,0} + |v_{2,1}| (\cos(\phi) \cos(\omega t) - \sin(\phi) \sin(\omega t)) \end{aligned} \quad (5-6)$$

Consider that $I_p^{(CS)}$ and Q_p in equation (5-1) can be represented by a polynomial of mixing products $V_1^m(t)V_2^n(t)$. The order of the terms is given by $m+n$.

$$\begin{aligned} I_p^{(CS)} &= G_p(V_1(t), V_2(t)) \\ &= G_{p1}V_1(t) + G_{p2}V_2(t) + G_{p11}V_1^2(t) + G_{p12}V_1(t)V_2(t) \\ &\quad + G_{p22}V_2^2(t) + G_{p111}V_1^3(t) + G_{p112}V_1^2(t)V_2(t) \\ &\quad + G_{p122}V_1(t)V_2^2(t) + G_{p222}V_2^3(t) + \dots \end{aligned} \quad (5-7)$$

$$\begin{aligned}
 Q_p &= C_p(V_1(t), V_2(t)) \\
 &= C_{p1}V_1(t) + C_{p2}V_2(t) + \frac{C_{p11}}{2}V_1^2(t) + C_{p12}V_1(t)V_2(t) \\
 &\quad + \frac{C_{p22}}{2}V_2^2(t) + \frac{C_{p111}}{3}V_1^3(t) + C_{p112}V_1^2(t)V_2(t) \\
 &\quad + C_{p122}V_1(t)V_2^2(t) + \frac{C_{p222}}{3}V_2^3(t) + \dots
 \end{aligned} \tag{5-8}$$

$$\begin{aligned}
 \frac{dQ_p}{dt} &= C_{p1} \frac{\partial V_1(t)}{\partial t} + C_{p2} \frac{\partial V_2(t)}{\partial t} + C_{p11}V_1(t) \frac{\partial V_1(t)}{\partial t} \\
 &\quad + C_{p12}V_1(t) \frac{\partial V_2(t)}{\partial t} + C_{p12}V_2(t) \frac{\partial V_1(t)}{\partial t} \\
 &\quad + C_{p22}V_2(t) \frac{\partial V_2(t)}{\partial t} + C_{p111}V_1^2(t) \frac{\partial V_1(t)}{\partial t} \\
 &\quad + C_{p112}2V_1(t)V_2(t) \frac{\partial V_1(t)}{\partial t} + C_{p112}V_1^2(t) \frac{\partial V_2(t)}{\partial t} \\
 &\quad + C_{p122} \frac{\partial V_1(t)}{\partial t} V_2^2(t) + C_{p122}V_1(t)2V_2(t) \frac{\partial V_2(t)}{\partial t} \\
 &\quad + C_{p222}V_2^2(t) \frac{\partial V_2(t)}{\partial t} + \dots
 \end{aligned} \tag{5-9}$$

5.1.2.1 Linear Operation

If equation (5-1) is linearized to the first order ($m+n=1$, i.e. $m=1$ and $n=0$ or $m=0$ and $n=1$) about a Large Signal Operating Point, which in this case is defined by the DC bias state ($V_{1,0}, V_{2,0}$).

$$\begin{aligned}
 I_p(t) &= I_{p,0}(V_{1,0}, V_{2,0}) + G_{p1}(V_{1,0}, V_{2,0}) (|v_{1,1}| \cos(\omega t)) \\
 &\quad + G_{p2}(V_{1,0}, V_{2,0}) (|v_{2,1}| \cos(\omega t + \phi)) \\
 &\quad - C_{p1}(V_{1,0}, V_{2,0}) \frac{\partial (|v_{1,1}| \cos(\omega t))}{\partial t} \\
 &\quad - C_{p2}(V_{1,0}, V_{2,0}) \frac{\partial (|v_{2,1}| \cos(\omega t + \phi))}{\partial t}
 \end{aligned} \tag{5-10}$$

which can be further reduced to equation (5-11).

$$\begin{aligned}
 I_p(t) = & I_{p,0}(V_{1,0}, V_{2,0}) + G_{p1}(V_{1,0}, V_{2,0})|v_{1,1}|\cos(\omega t) \\
 & + G_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|\cos(\omega t + \phi) \\
 & + \omega C_{p1}(V_{1,0}, V_{2,0})|v_{1,1}|\sin(\omega t) \\
 & + \omega C_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|\sin(\omega t + \phi)
 \end{aligned} \tag{5-11}$$

By considering the Fourier components of these terms for conversion to the frequency domain,

At DC;

$$\widehat{V}_{1,0} = V_{1,0}\widehat{V}_{2,0} = V_{2,0}\widehat{I}_{p,0} = I_{p,0}(V_{1,0}, V_{2,0}) = \text{constant} \tag{5-12}$$

At fundamental frequency;

$$\widehat{V}_{1,1} = |v_{1,1}| \tag{5-13}$$

$$\widehat{V}_{2,1}(Q) = |v_{2,1}|(\cos(\phi) - j\sin(\phi)) = |v_{2,1}|e^{-j\phi} = |v_{2,1}| \cdot Q \tag{5-14}$$

$$\begin{aligned}
 \widehat{I}_{p,1}(\phi) = & G_{p1}(V_{1,0}, V_{2,0})|v_{1,1}| + j\omega C_{p1}(V_{1,0}, V_{2,0})|v_{1,1}| \\
 & + G_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|(\cos(\phi) - j\sin(\phi)) \\
 & + \omega C_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|(\sin(\phi) + j\cos(\phi))
 \end{aligned} \tag{5-15}$$

$$\begin{aligned}
 \widehat{I}_{p,1}(\phi) = & G_{p1}(V_{1,0}, V_{2,0})|v_{1,1}| + j\omega C_{p1}(V_{1,0}, V_{2,0})|v_{1,1}| \\
 & + \{G_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|(\cos(\phi)) \\
 & + \omega C_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|(\sin(\phi))\} \\
 & + j\{G_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|(-\sin(\phi)) \\
 & + \omega C_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|(\cos(\phi))\}
 \end{aligned} \tag{5-16}$$

In equation (5-16), the G and C terms cannot be separated. Rearranging the terms will result in equation (5-19).

$$\begin{aligned}
 \widehat{I}_{p,1}(\phi) = & G_{p1}(V_{1,0}, V_{2,0})|v_{1,1}| + j\omega C_{p1}(V_{1,0}, V_{2,0})|v_{1,1}| \\
 & + G_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|(\cos(\phi) - j\sin(\phi)) \\
 & + j\omega C_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|(\cos(\phi) - j\sin(\phi))
 \end{aligned} \tag{5-17}$$

$$\begin{aligned}
 \widehat{I}_{p,1}(\phi) = & G_{p1}(V_{1,0}, V_{2,0})|v_{1,1}| + j\omega C_{p1}(V_{1,0}, V_{2,0})|v_{1,1}| \\
 & + \{G_{p2}(V_{1,0}, V_{2,0})|v_{2,1}| \\
 & + j\omega C_{p2}(V_{1,0}, V_{2,0})|v_{2,1}|\}(\cos(\phi) - j\sin(\phi))
 \end{aligned} \tag{5-18}$$

$$\begin{aligned}
 \widehat{I}_{p,1}(Q) = & \{G_{p1}(V_{1,0}, V_{2,0}) + j\omega C_{p1}(V_{1,0}, V_{2,0})\}|v_{1,1}| \\
 & + \{G_{p2}(V_{1,0}, V_{2,0}) + j\omega C_{p2}(V_{1,0}, V_{2,0})\}|v_{2,1}| \cdot Q
 \end{aligned} \tag{5-19}$$

$$\widehat{I}_{p,1}(Q) = \{y_{p1,11}\}|v_{1,1}| + \{y_{p1,21}\}|v_{2,1}| \cdot Q \tag{5-20}$$

Now the G and C variables can be separated and obtained. From (5-20), a minimum of 2 measurements with different values of Q (the phase of $V_{2,1}$) are required to determine the four fundamental Y-parameters, $y_{p1,q1}$.

Note that the functions $\widehat{V}_{2,1}(Q)$ and $\widehat{I}_{p,1}(Q)$ are periodic functions of Q. Hence if Q is swept from 0 to 2π , these functions can be Fourier transformed with respect to $Q\langle 0,1\rangle$. For $\widehat{V}_{1,1}$ the coefficients determined would be $\langle |v_{1,1}|, 0\rangle$, for $\widehat{V}_{2,1}(Q)$ they would be $\langle 0, |v_{2,1}| \rangle$, and for $\widehat{I}_{p,1}(Q)$ they would be $\langle y_{p1,11}|v_{1,1}|, y_{p1,21}|v_{2,1}| \rangle$.

Since the coefficients are of the form $G + j\omega C$, it implies that once they are determined at one frequency, they can be used to predict behaviour at another frequency.

$$\begin{bmatrix} \widehat{I}_{1,1} \\ \widehat{I}_{2,1} \end{bmatrix} = \begin{bmatrix} y_{11,11}(V_{1,0}, V_{2,0}) & y_{11,21}(V_{1,0}, V_{2,0}) \\ y_{21,11}(V_{1,0}, V_{2,0}) & y_{21,21}(V_{1,0}, V_{2,0}) \end{bmatrix} \begin{bmatrix} \widehat{V}_{1,1} \\ \widehat{V}_{2,1} \end{bmatrix} \tag{5-21}$$

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} y_{11}(\omega) & y_{12}(\omega) \\ y_{21}(\omega) & y_{22}(\omega) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \quad (5-22)$$

$$Y_{gs}(\omega) = y_{11}(\omega) + y_{12}(\omega) \quad (5-23)$$

$$Y_{gd}(\omega) = -y_{12}(\omega) \quad (5-24)$$

$$Y_{gm}(\omega) = y_{21}(\omega) - y_{12}(\omega) \quad (5-25)$$

$$Y_{ds}(\omega) = y_{22}(\omega) + y_{12}(\omega) \quad (5-26)$$

These linear Y-parameters link the small signal output current to input voltages as shown in equation (5-21) and are traditionally written in the form shown in (5-22). Using (5-23)-(5-26), these Y-parameters for a linear operation (small drive level) can be transformed to determine the small-signal equivalent circuit components as shown in Fig. 5-2.

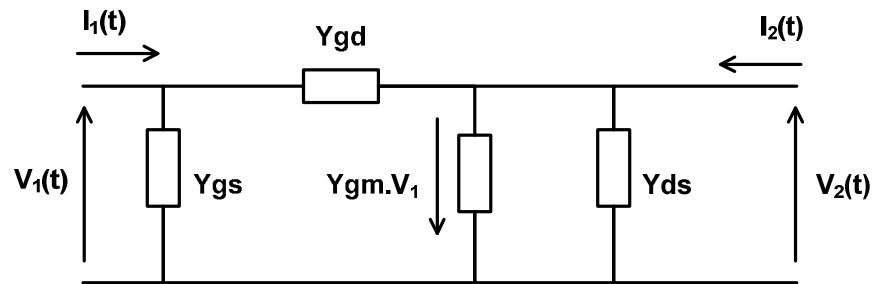


Figure 5-2: Equivalent circuit model of intrinsic transistor at small drive levels.

5.1.2.2 Non-Linear Operation

If equation (5-1) now linearized, up to third order ($m+n=1$ and $m+n=3$), about a Large Signal Operating Point, in this case defined by the DC bias state and input drive level, $(V_{1,0}, V_{2,0}, |v_{1,1}|)$. Second order terms ($m+n=2$) are ignored since they either mix up to the 2nd harmonic or down to DC and do not produce terms at the fundamental. Output stimulus is given by (5-27).

$$\begin{aligned}
 V_2(t) &= V_{2,0} + |v_{2,1}| \cos(\omega t + \phi) \\
 &= V_{2,0} + |v_{2,1}| (\cos(\phi) \cos(\omega t) - \sin(\phi) \sin(\omega t))
 \end{aligned} \tag{5-27}$$

So,

$$\begin{aligned}
 I_p(t) &= \{I_{p,0}\} \\
 &\quad + \{G_{p1} (|v_{1,1}| \cos(\omega t)) + G_{p2} (|v_{2,1}| \cos(\omega t + \phi)) \\
 &\quad + \omega C_{p1} (|v_{1,1}| \sin(\omega t)) \\
 &\quad + \omega C_{p2} (|v_{2,1}| \sin(\omega t + \phi))\} \\
 &\quad + \left\{ G_{p111} \left((|v_{1,1}| \cos(\omega t))^3 \right) \right. \\
 &\quad + G_{p112} \left((|v_{1,1}| \cos(\omega t))^2 |v_{2,1}| \cos(\omega t + \phi) \right) \\
 &\quad + G_{p122} \left(|v_{1,1}| \cos(\omega t) (|v_{2,1}| \cos(\omega t + \phi))^2 \right) \\
 &\quad \left. + G_{p222} \left((|v_{2,1}| \cos(\omega t + \phi))^3 \right) \right\} \\
 &\quad - \left\{ C_{p111} \frac{\partial \left((|v_{1,1}| \cos(\omega t))^3 \right)}{\partial t} \right. \\
 &\quad + C_{p112} \frac{\partial \left((|v_{1,1}| \cos(\omega t))^2 |v_{2,1}| \cos(\omega t + \phi) \right)}{\partial t} \\
 &\quad + C_{p122} \frac{\partial \left(|v_{1,1}| \cos(\omega t) (|v_{2,1}| \cos(\omega t + \phi))^2 \right)}{\partial t} \\
 &\quad \left. + C_{p222} \frac{\partial \left((|v_{2,1}| \cos(\omega t + \phi))^3 \right)}{\partial t} \right\}
 \end{aligned} \tag{5-28}$$

Expanding this results in,

$$\begin{aligned}
 I_p(t) = \{I_{p,0}\} & \\
 & + \left\{ G_{p1} (|v_{1,1}| \cos(\omega t)) + G_{p2} (|v_{2,1}| \cos(\omega t + \phi)) \right. \\
 & + \left. \omega C_{p1} (|v_{1,1}| \sin(\omega t)) + \omega C_{p2} (|v_{2,1}| \sin(\omega t + \phi)) \right\} \\
 & + \left\{ G_{p111} \left(|v_{1,1}|^3 \left(\frac{3}{4} \cos(\omega t) + \frac{1}{4} \cos(3\omega t) \right) \right) \right. \\
 & + G_{p112} \left(|v_{1,1}|^2 |v_{2,1}| \left(\frac{1}{2} \cos(\omega t + \phi) + \frac{1}{4} \cos(\omega t - \phi) \right. \right. \\
 & + \left. \left. \frac{1}{4} \cos(3\omega t + \phi) \right) \right) \\
 & + G_{p122} \left(|v_{1,1}| |v_{2,1}|^2 \left(\frac{1}{2} \cos(\omega t) + \frac{1}{4} \cos(\omega t + 2\phi) \right. \right. \\
 & + \left. \left. \frac{1}{4} \cos(3\omega t + 2\phi) \right) \right) \\
 & + G_{p222} \left(|v_{2,1}|^3 \left(\frac{3}{4} \cos(\omega t + \phi) + \frac{1}{4} \cos(3\omega t + 3\phi) \right) \right) \left. \right\} \\
 & + \left\{ \omega C_{p111} |v_{1,1}|^3 \frac{3}{4} (\sin(\omega t) + \sin(3\omega t)) \right. \\
 & + \omega C_{p112} |v_{1,1}|^2 |v_{2,1}| \left(\left(\frac{1}{2} \sin(\omega t + \phi) + \frac{1}{4} \sin(\omega t - \phi) \right. \right. \\
 & + \left. \left. \frac{3}{4} \sin(3\omega t + \phi) \right) \right) \\
 & + \omega C_{p122} |v_{1,1}| |v_{2,1}|^2 \left(\frac{1}{2} \sin(\omega t) + \frac{1}{4} \sin(\omega t + 2\phi) \right. \\
 & + \left. \frac{3}{4} \sin(3\omega t + 2\phi) \right) \\
 & + \left. \omega C_{p222} |v_{2,1}|^3 \left(\frac{3}{4} \sin(\omega t + \phi) + \frac{3}{4} \sin(3\omega t + 3\phi) \right) \right\}
 \end{aligned} \tag{5-29}$$

which can be further expanded to

$$\begin{aligned}
 I_p(t) = \{I_{p,0}\} & \\
 & + \left\{ G_{p112} |v_{1,1}|^2 |v_{2,1}| \frac{1}{4} \cos(\omega t - \phi) \right. \\
 & + \left. \omega C_{p112} |v_{1,1}|^2 |v_{2,1}| \frac{1}{4} \sin(\omega t - \phi) \right\} \\
 & + \left\{ G_{p1} (|v_{1,1}| \cos(\omega t)) + \omega C_{p1} (|v_{1,1}| \sin(\omega t)) \right\} \\
 & + \left\{ G_{p111} |v_{1,1}|^3 \frac{3}{4} \cos(\omega t) + \omega C_{p111} |v_{1,1}|^3 \frac{3}{4} \sin(\omega t) \right\} \\
 & + \left\{ G_{p122} |v_{1,1}| |v_{2,1}|^2 \frac{1}{2} \cos(\omega t) \right. \\
 & + \left. \omega C_{p122} |v_{1,1}| |v_{2,1}|^2 \frac{1}{2} \sin(\omega t) \right\} \\
 & + \left\{ G_{p2} (|v_{2,1}| \cos(\omega t + \phi)) + \omega C_{p2} (|v_{2,1}| \sin(\omega t + \phi)) \right\} \\
 & + \left\{ G_{p112} |v_{1,1}|^2 |v_{2,1}| \frac{1}{2} \cos(\omega t + \phi) \right. \\
 & + \left. \omega C_{p112} |v_{1,1}|^2 |v_{2,1}| \frac{1}{2} \sin(\omega t + \phi) \right\} \\
 & + \left\{ G_{p222} |v_{2,1}|^3 \frac{3}{4} \cos(\omega t + \phi) \right. \\
 & + \left. \omega C_{p222} |v_{2,1}|^3 \frac{3}{4} \sin(\omega t + \phi) \right\} \\
 & + \left\{ G_{p122} |v_{1,1}| |v_{2,1}|^2 \frac{1}{4} \cos(\omega t + 2\phi) \right. \\
 & + \left. \omega C_{p122} |v_{1,1}| |v_{2,1}|^2 \frac{1}{4} \sin(\omega t + 2\phi) \right\}
 \end{aligned} \tag{5-30}$$

Consider now the Fourier components of these terms.

At DC;

$$\widehat{V}_{1,0} = V_{1,0} \widehat{V}_{2,0} = V_{2,0} \widehat{I}_{p,0} = I_{p,0}(V_{1,0}, V_{2,0}) = \text{constant} \tag{5-31}$$

At fundamental frequency;

$$\widehat{V}_{1,1} = |v_{1,1}| \tag{5-32}$$

$$\widehat{V}_{2,1}(Q) = |v_{2,1}| (\cos(\phi) - j \sin(\phi)) = |v_{2,1}| e^{-j\phi} = |v_{2,1}| \cdot Q \tag{5-33}$$

$$\begin{aligned}
 \widehat{I}_{p,1}(Q) = & \left\{ G_{p112} |v_{1,1}|^2 \frac{1}{4} + j\omega C_{p112} |v_{1,1}|^2 \frac{1}{4} \right\} |v_{2,1}| \cdot Q^{-1} \\
 & + \{ G_{p1} + j\omega C_{p1} \} |v_{1,1}| \\
 & + \left\{ G_{p111} |v_{1,1}|^2 \frac{3}{4} + j\omega C_{p111} |v_{1,1}|^2 \frac{3}{4} \right\} |v_{1,1}| \\
 & + \left\{ G_{p122} |v_{2,1}|^2 \frac{1}{2} + j\omega C_{p122} |v_{2,1}|^2 \frac{1}{2} \right\} |v_{1,1}| \\
 & + \{ G_{p2} + j\omega C_{p2} \} |v_{2,1}| \cdot Q \\
 & + \left\{ G_{p112} |v_{1,1}|^2 \frac{1}{2} + j\omega C_{p112} |v_{1,1}|^2 \right\} |v_{2,1}| \cdot Q \\
 & + \left\{ G_{p222} |v_{2,1}|^2 \frac{3}{4} + j\omega C_{p222} |v_{2,1}|^2 \frac{3}{4} \right\} |v_{2,1}| \cdot Q \\
 & + \left\{ G_{p122} |v_{1,1}| \frac{1}{4} + j\omega C_{p122} |v_{1,1}| \frac{1}{4} \right\} |v_{2,1}|^2 \cdot Q^2
 \end{aligned} \tag{5-34}$$

$$\begin{aligned}
 \widehat{I}_{p,1}(Q) = & Y_{p1,21}^{(-1)} |v_{2,1}| \cdot Q^{-1} + Y_{p1,11}^{(0)} |v_{1,1}| + Y_{p1,21}^{(1)} |v_{2,1}| \cdot Q \\
 & + Y_{p1,21}^{(2)} |v_{2,1}|^2 \cdot Q^2
 \end{aligned} \tag{5-35}$$

If we assume that $|v_{2,1}|$ is small, then this equation simplifies as follows;

$$\widehat{I}_{p,1}(Q) = Y_{p1,11}^{(F)} |v_{1,1}| + Y_{p1,21}^{(S)} |v_{2,1}| \cdot Q + Y_{p1,21}^{(T)} |v_{2,1}| \cdot Q^{-1} \tag{5-36}$$

Note all the coefficients based on this mathematical analysis are predicted, in a similar manor to the linear case, to have the form $Y = G + j\omega C$, hence can be extrapolated as a function of frequency.

In this form, again, the process for separating the G and C variables can be derived. A minimum of three measurements, for different values of Q, are simply required to determine the six fundamental y-parameters, $Y_{p1,11}^{(F)}$, $Y_{p1,21}^{(S)}$ and $Y_{p1,21}^{(T)}$.

Note that the functions $\widehat{V}_{2,1}(Q)$ and $\widehat{I}_{p,1}(Q)$ are periodic functions of Q . Hence if Q is swept from 0 to 2π , these functions can be Fourier transformed with respect to Q ($\langle -1, 0, 1 \rangle$). For $\widehat{V}_{1,1}$ the coefficients determined would be $\langle 0, |v_{1,1}|, 0 \rangle$, for $\widehat{V}_{2,1}(Q)$ they would be $\langle |v_{2,1}|, 0, |v_{2,1}| \rangle$, and for $\widehat{I}_{p,1}(Q)$ they would be $\langle Y_{p1,21}^{(T)}|v_{2,1}|, Y_{p1,11}^{(F)}|v_{1,1}|, Y_{p1,21}^{(S)}|v_{2,1}| \rangle$.

Note in this case we also have a third harmonic component.

$$\begin{aligned}
 I_p(t) = & \left\{ G_{p111}|v_{1,1}|^3 \frac{1}{4} \cos(3\omega t) + \omega C_{p111}|v_{1,1}|^3 \frac{3}{4} \sin(3\omega t) \right\} \\
 & + \left\{ G_{p112}|v_{1,1}|^2 |v_{2,1}| \frac{1}{4} \cos(3\omega t + \phi) \right. \\
 & \left. + \omega C_{p112}|v_{1,1}|^2 |v_{2,1}| \frac{3}{4} \sin(3\omega t + \phi) \right\} \\
 & + \left\{ G_{p122}|v_{1,1}| |v_{2,1}|^2 \frac{1}{4} \cos(3\omega t + 2\phi) \right. \\
 & \left. + \omega C_{p122}|v_{1,1}| |v_{2,1}|^2 \frac{3}{4} \sin(3\omega t + 2\phi) \right\} \\
 & + \left\{ G_{p222}|v_{2,1}|^3 \frac{1}{4} \cos(3\omega t + 3\phi) \right. \\
 & \left. + \omega C_{p222}|v_{2,1}|^3 \frac{3}{4} \sin(3\omega t + 3\phi) \right\}
 \end{aligned} \tag{5-37}$$

$$\begin{aligned}
 I_{p,3}(Q) = & \left\{ G_{p111} \frac{1}{4} + j3\omega C_{p111} \frac{1}{4} \right\} |v_{1,1}|^3 \\
 & + \left\{ G_{p112}|v_{1,1}|^2 \frac{1}{4} + j3\omega C_{p112}|v_{1,1}|^2 \frac{1}{4} \right\} |v_{2,1}| \cdot Q \\
 & + \left\{ G_{p122}|v_{1,1}| \frac{1}{4} + j3\omega C_{p122}|v_{1,1}| \frac{1}{4} \right\} |v_{2,1}|^2 \cdot Q^2 \\
 & + \left\{ G_{p222} \frac{1}{4} + j3\omega C_{p222} \frac{1}{4} \right\} |v_{2,1}|^3 \cdot Q^3
 \end{aligned} \tag{5-38}$$

$$I_{p,3}(Q) = Y_{p3,11}^{(0)} |v_{1,1}|^3 + Y_{p3,21}^{(1)} |v_{2,1}| \cdot Q + Y_{p3,21}^{(2)} |v_{2,1}|^2 \cdot Q^2 + Y_{p3,21}^{(3)} |v_{2,1}|^3 \cdot Q^3 \tag{5-39}$$

Again, assuming that $|v_{2,1}|$ is small then this equation simplifies as follows;

$$I_{p,3}(Q) = Y_{p3,31}^{(F)} |v_{1,1}|^3 + Y_{p3,21}^{(S)} |v_{2,1}| \cdot Q \tag{5-40}$$

Again, this mathematical analysis, predicts that this parameter also has the form $Y = G + j\omega C$ and so can again be used to extrapolate with frequency.

5.1.3 Modelling process flow

In order to investigate experimentally whether Behavioural models are actually frequency scalable, the first step is similar to generating Geometric scalable models. The intrinsic transistor plane must be determined from Cold FET measurements because equation (5-1) is only valid at the intrinsic plane.

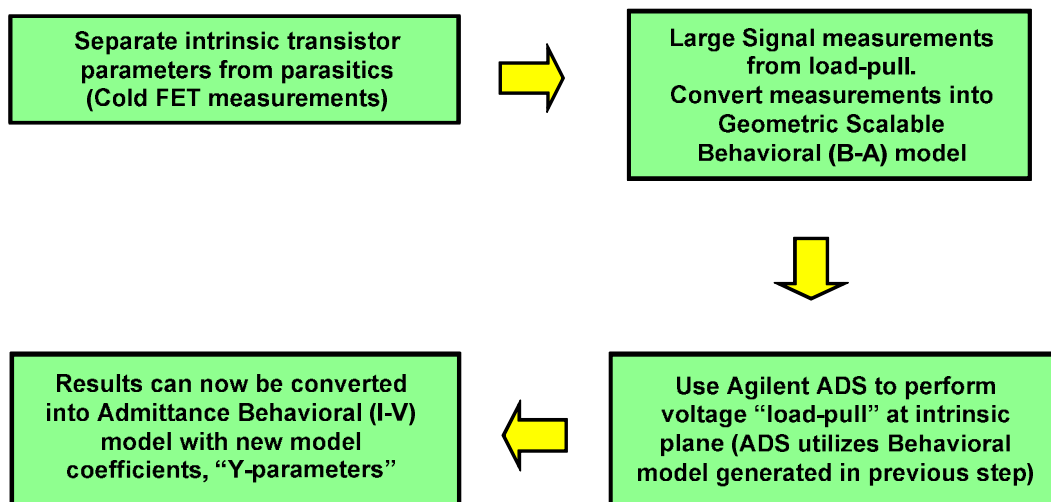


Figure 5-3: Modelling process of frequency scalable transistor Behavioural model.

Then large signal load-pull measurements over several drive levels are performed on the transistor. Please see Section 3.3.1 for the description of the

load-pull setup. These measurements are then again converted into the Cardiff Behavioural model (which is geometrically scalable). Note that this model is in the B-A domain, whereby it outputs the B waves based on the input A waves.

The reason it needs to be converted into this form is because it would be practically impossible to perform voltage load-pull with the stimulus described by equations (5-5), (5-6) and (5-27) using a real world measurement system. The Network Analyser is able to maintain A waves going into a device at a constant magnitude but maintaining a constant $V_{1,1}$ (input voltage drive) magnitude is very difficult since it was not designed to operate in that fashion.

However, in Keysight's Advanced Design System (ADS), a simulation can be easily setup with voltage sources in order to achieve this condition. The only caveat is that the model must be measured over a large range of drive levels and load impedances so that it can cover the desired input and output voltage levels that will be simulated.

The results from the simulation of voltage load-pull, which utilizes the Behavioural model generated from measurements in the B-A domain, can now be utilized to directly extract the Admittance Behavioural model (I-V domain), hence investigate its mathematical form. The simulation setup and extraction of the model coefficients will be shown in detail in Section 5.3. The frequency scalability of these new coefficients, which are large signal "Y-parameters", will be investigated in Section 5.4.

5.1.4 List of devices for experimental validation

In this section, the results from 2 separate GaN wafers are analysed. The first is a GaN on Si wafer with 0.5 μm gate length. This shall be referred to henceforth as the GaN on Si wafer. The other is a GaN on SiC wafer with a

0.25 μm gate length. This shall be called the GaN on SiC wafer and is the same wafer as mentioned in Chapter 3 with ID: WN001A. The device chosen on both wafers is the 2x200 μm device (2 finger by 200 μm gate width). Both devices have a probe pitch of 150 μm .

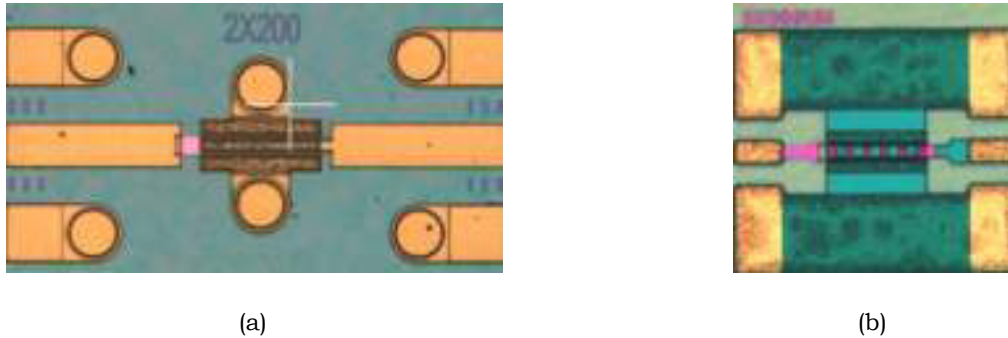


Figure 5-4: 2x200 μm devices used for frequency modelling (a) GaN on Si (b) GaN on SiC

The reason 2 wafers were used is because these experiments were conducted in conjunction with efforts by the sponsor company MACOM to use GaN on Si transistors in their product line-up. Therefore, measurements were performed on both GaN on Si and GaN on SiC transistors. Results will show that the approach is robust and can be applied to both wafers regardless of its substrate difference.

5.2 Passive Equivalent Circuit Model

5.2.1 Introduction

A regular model for the intrinsic transistor of a FET is not a true Y-shell with only capacitances and admittances as shown in "Case A" of Fig. 5-5. There is a gate-source resistance, R_{gs} in series with the gate-source capacitance, C_{gs} . With the presence of R_{gs} , the assumption that the frequency scalable model is an admittance model with only Y-parameters cannot be upheld.

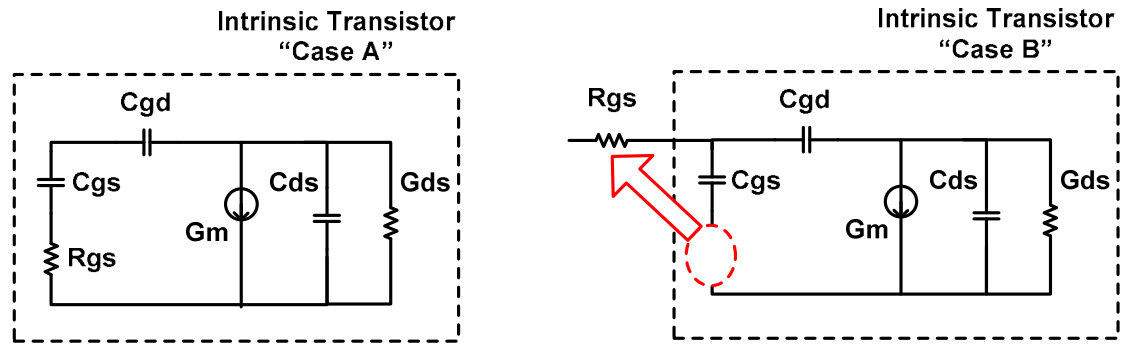


Figure 5-5: Regular intrinsic transistor small signal model (Case A) versus True Y-shell intrinsic transistor small signal model (Case B)

However, it is possible over a limited bandwidth, that we can de-embed the R_{gs} out of the intrinsic model with minimal effect to the S-parameters of the model. R_{gs} will be placed in series with the gate of the intrinsic transistor as depicted in "Case B" of Fig. 5-5. The impact of this model modification will only start to be seen at very high frequencies.

Therefore, it is important to note that the frequency scalable model approach that is proposed has a bandwidth limitation. An insight into a possible valid bandwidth can be achieved by referring back to the ability of the modified topology to predict the S-parameters.

The methods for establishing either geometric or frequency scalable models are always rooted to the small signal, S-parameters. Any fundamental limitations of the models can be easily traced back to its failure to predict the measured S-parameters. If at small signal the model fails to work, it would definitely fail at large drive signals as well.

5.2.2 Small signal model evaluation

The first step is to prove that de-embedding the R_{gs} from the intrinsic transistor will not cause the S-parameters predictions to change significantly within our bandwidth of interest.

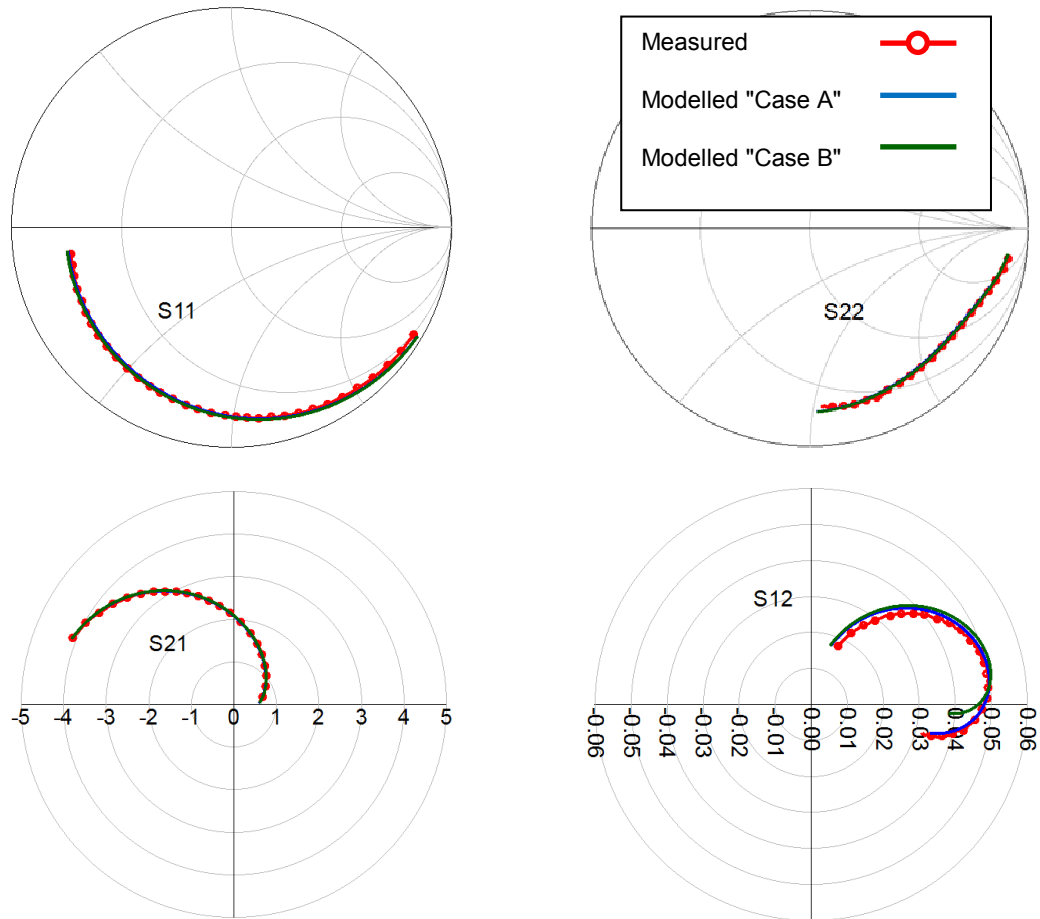


Figure 5-6: S-parameters from 1 -20 GHz between measured, modelled "Case A" and modelled "Case B" for the 2x200 μm transistor on the GaN on Si wafer.

The S-parameter results on the GaN on Si wafer from 1 - 20 GHz with measured, modelled with intrinsic transistor in "Case A" and modelled with intrinsic transistor in "Case B" is shown in Fig. 5-6. According to the results, there is only a minimal difference in the S_{12} with all the other parameters remaining the same within our bandwidth of interest.

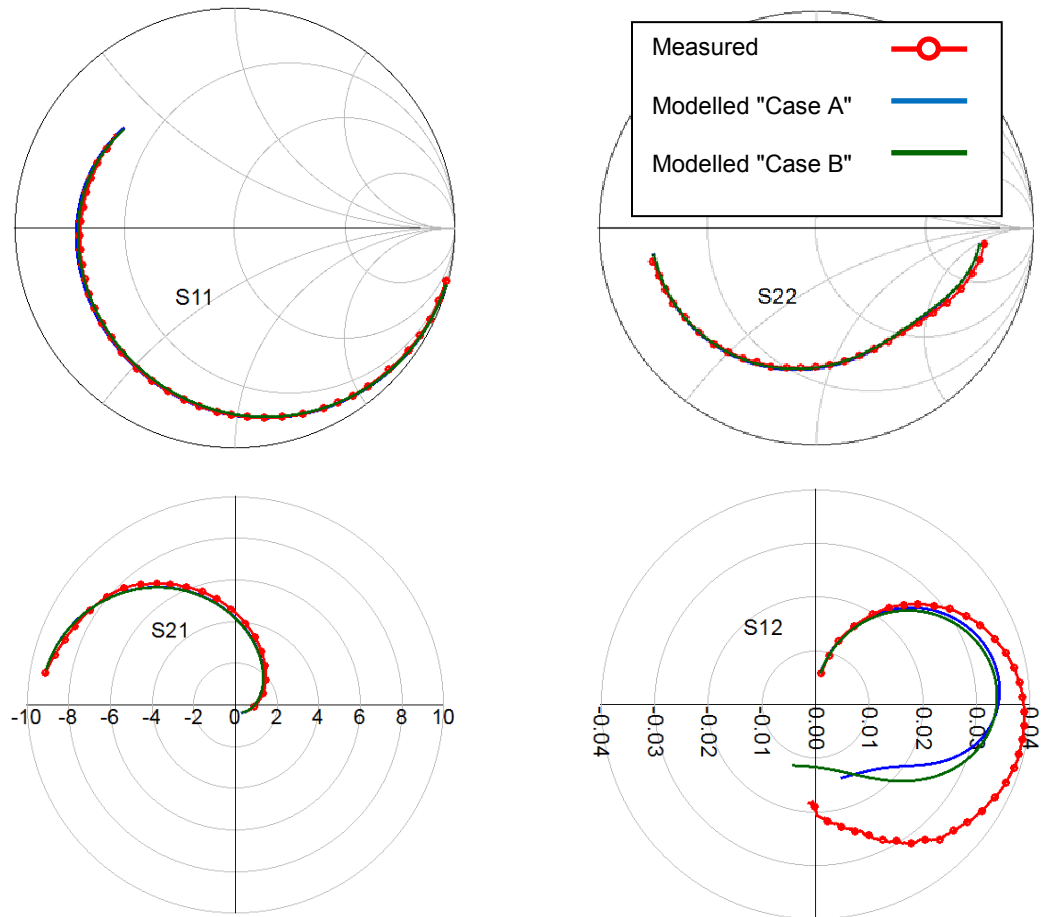


Figure 5-7: S-parameters from 0.5 -40 GHz between measured, modelled "Case A" and modelled "Case B" for the 2x200 μm transistor on the GaN on SiC wafer.

A repeat of this step on the GaN on SiC wafer also show the same results, shown in Fig. 5-7. These observations concur with the assumption that the R_{gs} can be de-embedded from the intrinsic transistor model to produce a Y-shell with only capacitances and admittances without affecting the small signal parameters of the device. This can then, hopefully, be carried forward into the large signal realm. This affectedly assumes that the R_{gs} is drive level invariant.

These simulated results were obtained from ADS using small-signal component values obtained through Cold FET measurements as described in Section 3.2.

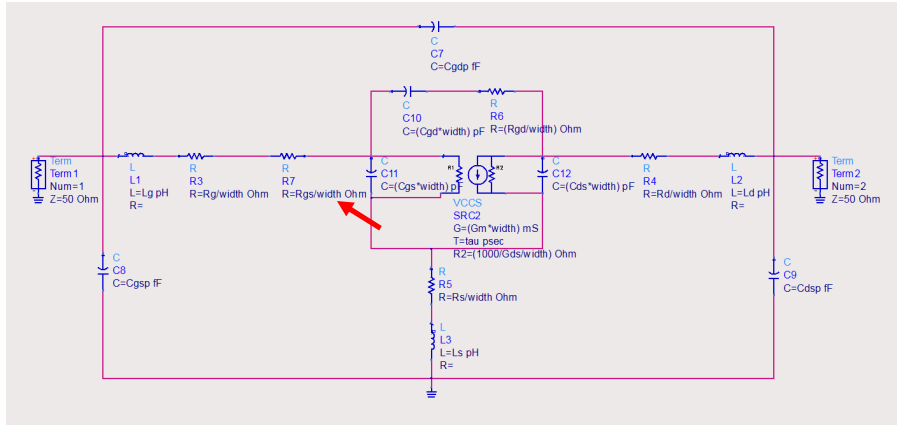


Figure 5-8: ADS circuit used for simulation of small signal "Case B" results

Fig. 5-8 shows the ADS circuit used to obtain the results for "Case B". The component values for the transistor from the GaN on Si wafer is shown in Table 5-1 whereas the component values for the GaN on SiC wafer is in Table 5-2.

Device	Cgsp (fF)	Cgdp (fF)	Cdsp (fF)	Lg (pH)	Ld (pH)	Ls (pH)	Rg(Ω- mm)	Rd (Ω- mm)	Rs (Ω- mm)
2x200	19.5	14.3	19.5	50	50	1	1.48	1.48	0.01
Cgs (pF/mm)	Rgs (Ω-mm)		Cgd (pF/mm)	Cds (pF/mm)		Gm (mS/mm)	Tau (psec)		Gds (mS/mm)
1.9	1.27		0.04	0.25		112	6		1.93

Table 5-1: Values of small signal component for the 2x200 μm device on the GaN on Si wafer

Device	Cgsp (fF)	Cgdp (fF)	Cdsp (fF)	Lg (pH)	Ld (pH)	Ls (pH)	Rg(Ω- mm)	Rd (Ω- mm)	Rs (Ω- mm)
2x200	33	6	21	109.5	94.5	0.05	1.90	1.30	0.0250
Cgs (pF/mm)	Rgs (Ω-mm)		Cgd (pF/mm)	Cds (pF/mm)		Gm (mS/mm)	Tau (psec)		Gds (mS/mm)
1.72	1.2		0.04	0.36		270	2.5		7

Table 5-2: Values of small signal component for the 2x200 μm device on the GaN on SiC wafer

5.3 Large Signal Model Extraction

5.3.1 Introduction

In order to investigate the ability to extract a frequency scalable model, measured data of the devices must first be obtained via load-pull over a range of input drive levels and frequencies. The active load-pull measurement setup has been described in detail in Section 3.3.1.

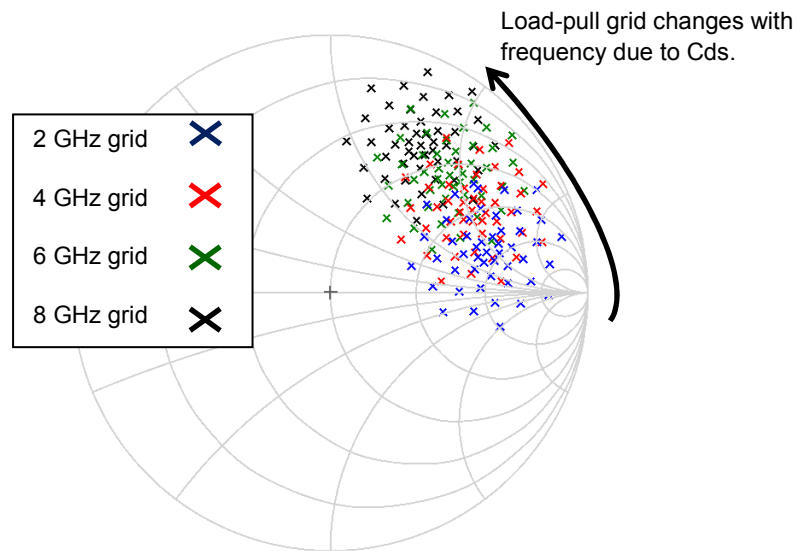


Figure 5-9: Measured load-pull grid of transistor from 2 to 8 GHz

The $2 \times 200 \mu\text{m}$ GaN on Si transistor was chosen and measured at a bias of $I_d = 25 \text{ mA/mm}$. Measurements were performed from 2 GHz to 8 GHz in 2 GHz steps. Fig. 5-9 shows the measured load-pull grid of the $2 \times 200 \mu\text{m}$ transistor, which takes into account the C_{ds} of the device. Note that since the parasitic component values and C_{ds} have already been determined, it is possible to predict variation of the load-pull grid that needs to be measured as frequency increases. This aims to ensure that when all the results over frequency are de-embedded to the current generator plane, they form the same load-pull measurement grid.

The 2nd harmonic at the input and output of the device under test (DUT) were shorted out. The reason this bandwidth was chosen in this first run was to establish the theory and make measurements easier as calibration must be more stringent as we move to X-band and beyond. Furthermore, using an active load-pull setup means that to set the 2nd harmonic to a short circuit, amplifiers working up to 16 GHz would be necessary in the measurement setup.

Going to a higher frequency range puts more pressure on the equipment availability. In addition, it is difficult and costly to obtain amplifiers that would have high P_{out} at X-band. Having too small a P_{out} will cause the load-pull system to saturate and not complete the measurements.

5.3.2 Simulation Setup in ADS

Once the measured data has been obtained from load-pull, it is then converted into a Cardiff Model for utilization in ADS simulations. The large signal measured intrinsic current response, $I_{p,1}$ is then probed by simulating "load-pull" using voltage sources. The required input and output voltage stimulus is given by (5-41) and (5-42) respectively.

$$V_{1,1} = |v_{1,1}|e^{-j\theta} = |v_{1,1}|P_1 \quad (5-41)$$

$$V_{2,1}(Q_1) = V_{2,1 ref} + |\Delta V_{2,1}|e^{-j\phi} = V_{2,1 ref} + |\Delta v_{2,1}|Q_1 \quad (5-42)$$

$$\begin{aligned} I_{p,1}(Q_1) &= K_F + K_S Q_1 + K_T Q_1^{-1} \\ &= \{Y_{F,p}|v_{1,1}| + Y_{S,p}V_{2,1 ref} + Y_{T,p}V_{2,1 ref}^*\} \\ &\quad + \{Y_{S,p}|\Delta v_{2,1}|\} \cdot Q_1 + \{Y_{T,p}|\Delta v_{2,1}|\} \cdot Q_1^{-1} \end{aligned} \quad (5-43)$$

P_1 and Q_1 are the phases of $V_{1,1}$ and $\Delta V_{2,1}$ respectively. In order to simplify the extraction, P_1 is set to zero. The stimulus $V_{2,1}(Q_1)$ and response $I_{p,1}(Q_1)$, which should be described by (5-43) (a fundamental load-pull simplification of the general equation (5-2)), are predicted to be periodic functions of Q_1 . Hence, if Q_1 is swept from 0 to 2π , the model coefficients can be determined by Fourier transforming with respect to Q_1 . Note the similarity to X-parameters and their extraction, except the formulation is now in the admittance domain.

Fig. 5-10 shows the circuit diagram in ADS that performs the voltage load-pull. It utilizes voltage sources at both the gate and drain of the device and simulates the response based on actual measured data provided by the FDD block. This FDD block reads model coefficients extracted in the B-A domain from measured data (at the extrinsic plane) using the Cardiff Behavioural Model equations already described in Section 3.3.2. Note that the FDD is placed inside a de-embedding block, which de-embeds the parasitic components so that the simulation results are at the intrinsic plane.

In Fig. 5-10, the input and output voltage sources are set based on (5-41) and (5-42) respectively. The variable `magspin` in Fig. 5-10 refers to $|\Delta V_{2,1}|$ whereas the variable named `phasespin` is Q_1 . A $V_{2,1ref}$ is present in equation (5-42) so that the voltage load-pull is performed at the optimum location for the transistor in terms of P_{out} or Drain Efficiency. Do note that there is a C_{ds} component in the simulation, which takes into account the movement of the optimum location based on frequency.

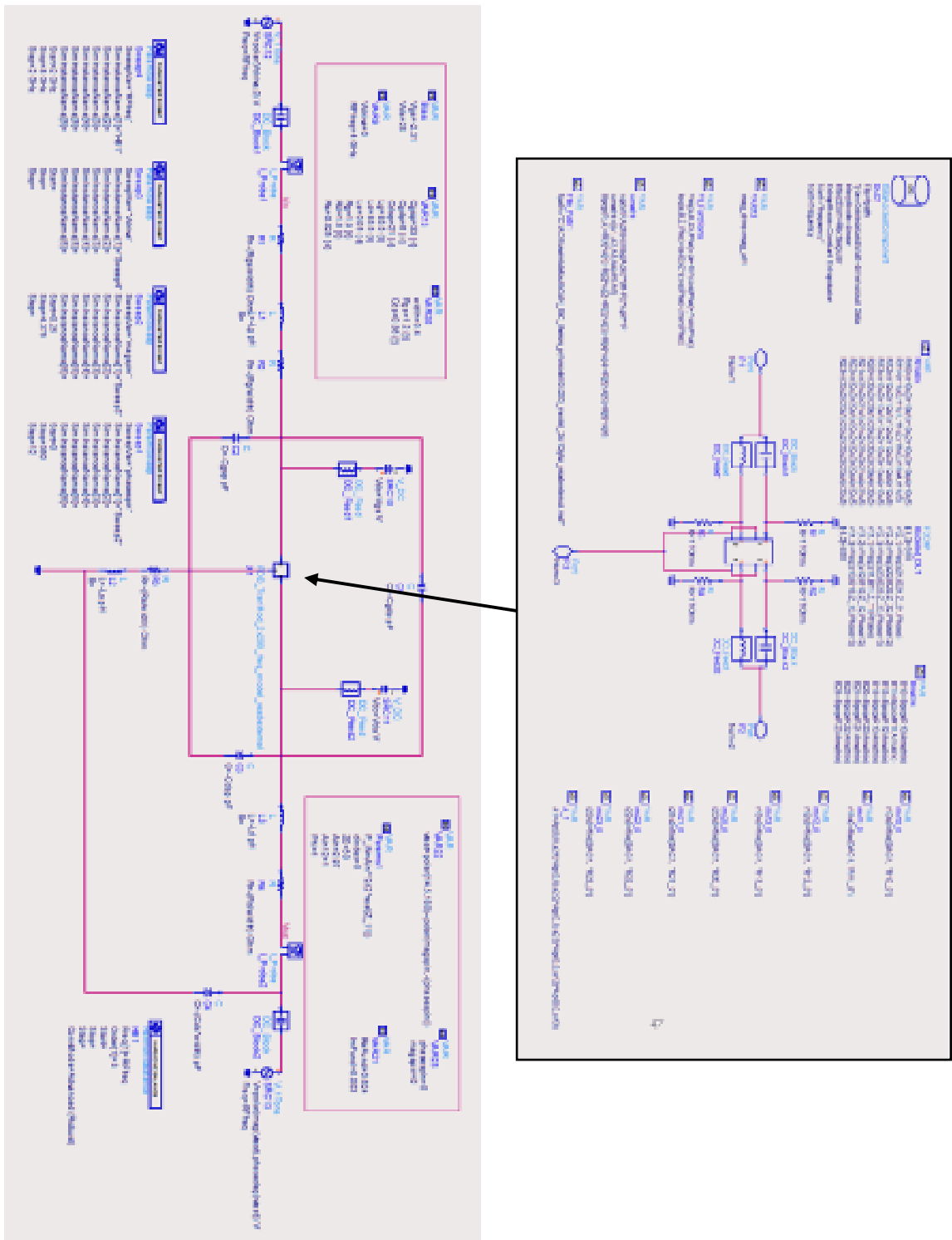


Figure 5-10: ADS simulation circuit diagram that performs voltage load-pull to generate frequency scalable model

All the results are then written into a .csv format and loaded into an Igor programme written specifically during the course of the PhD to extract the model coefficients. Fig. 5-11 shows an example of the .csv file generated from

the ADS voltage load-pull whereas Fig. 5-12 is the screenshot for the front panel of the Igor programme that runs the model extraction.

Constant $V_{1,1}$

phasespin	magspin	Vdrive	freq	harmindex	Vin	Vout	I_Probe1.i	I_Probe2.i
0	0.5	3.2	2.00E+09	0	1.65012271 / 180.00000000	27.74961003 / 0.00000000	0.00001785 / 0.00000000	0.06767297 / 0.00000000
0	0.5	3.2	2.00E+09	1	3.20000000 / -3.20895307E-16	23.50000000 / -180.00000000	0.03677750 / 86.24021161	0.11246454 / -25.87231343
0	0.5	3.2	2.00E+09	2	2.57564224E-18 / 48.00286546	2.58584598E-17 / -121.81533161	0.02246925 / 64.69866761	0.04273750 / -40.10566499
0	0.5	3.2	2.00E+09	3	1.02665161E-18 / 154.97948483	2.60593437E-18 / 98.13261845	0.00689643 / 25.43490433	0.01836230 / 168.67802263
0	0.5	3.2	4.00E+09	0	1.65155915 / 180.00000000	27.74846011 / 0.00000000	0.00022679 / 0.00000000	0.06798375 / 0.00000000
0	0.5	3.2	4.00E+09	1	3.20000000 / -1.58503873E-16	23.50000000 / -180.00000000	0.07342800 / 86.84839640	0.13455195 / -46.50732540
0	0.5	3.2	4.00E+09	2	3.95893639E-17 / 90.00976681	1.40759267E-17 / -172.62287950	0.04484539 / 100.80063417	0.04236800 / -19.27953841
0	0.5	3.2	4.00E+09	3	5.15559637E-18 / 115.36575062	1.10315299E-17 / 96.58475877	0.00737794 / -35.30385795	0.02078344 / 120.97853833
0	0.5	3.2	6.00E+09	0	1.65225950 / 180.00000000	27.75847659 / 0.00000000	0.00032865 / 0.00000000	0.06527660 / 0.00000000
0	0.5	3.2	6.00E+09	1	3.20000000 / -3.59825243E-15	23.50000000 / -180.00000000	0.10935658 / 85.82296828	0.16517904 / -62.41731948
0	0.5	3.2	6.00E+09	2	2.77716811E-17 / 165.74691235	5.71424882E-18 / 140.12172344	0.06686244 / 51.97887595	0.04170909 / -82.62130905
0	0.5	3.2	6.00E+09	3	7.00047665E-18 / -52.41653542	1.28282769E-17 / -113.05569623	0.01139060 / -78.15100949	0.02871316 / 107.47527274
0	0.5	3.2	8.00E+09	0	1.65116299 / 180.00000000	27.75811852 / 0.00000000	0.00016916 / 0.00000000	0.06537337 / 0.00000000
0	0.5	3.2	8.00E+09	1	3.20000000 / 1.59158859E-15	23.50000000 / -180.00000000	0.14493508 / 86.60406707	0.18530044 / -66.31004456
0	0.5	3.2	8.00E+09	2	1.60616073E-17 / 149.29169597	8.23238190E-18 / -136.38497057	0.07156048 / 60.04998831	0.04116780 / -86.84606265
0	0.5	3.2	8.00E+09	3	3.92887337E-18 / 54.05555252	1.39195063E-17 / 152.25439521	0.00674523 / -32.86409325	0.02089200 / 110.95113615

Figure 5-11: CSV file generated from voltage load-pull simulations in ADS at a fixed fundamental input voltage.

Note from Fig. 5-11 that Vdrive is the fundamental input voltage of the source, $V_{1,1}$ which is set to a constant value in the ADS simulation. This is because from equation (5-4), model coefficients are always extracted as a function of the magnitude of $V_{1,1}$.

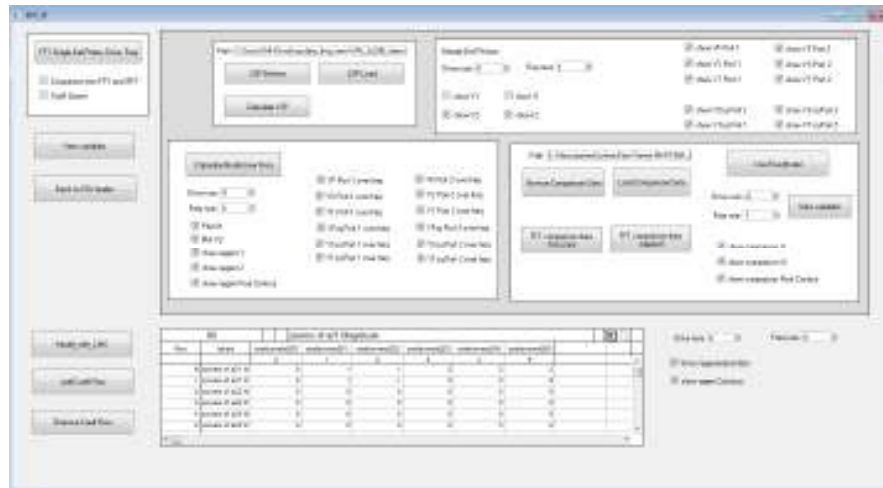


Figure 5-12: Igor programme front panel that loads and performs calculations to extract frequency independent model coefficients.

5.4 Experimental Model Validation 1st GaN wafer (Using 3 model coefficients)

The results presented in this section are based on simulations performed in ADS using measurements on the GaN on Si transistor described in Section 5.2.2.

5.4.1 Admittance Domain Model Coefficients

The stimulus of voltage "load-pull" (sweeping Q_1 and stepping $|\Delta V_{2,1}|$) as defined in equation (5-42) can be seen in Fig. 5-13 and is performed with $|\Delta V_{2,1}|$ from 0.5 V to 2 V in 0.5 V steps. The DC voltage is 28 V and $V_{2,1 \text{ ref}}$ is set to 24 V. The $I_{2,1}(Q_1)$ response to voltage "load-pull" at 4 GHz is shown in Fig. 5-14(a). Performing a Fourier transform on each sweep (on each individual ring), enables K_F , K_S and K_T to be determined, as shown in Fig. 5-14(b). Fig. 5-14(c) shows, as expected from (5-43), that K_F is constant whereas K_S and K_T are linear functions of $|\Delta V_{2,1}|$.

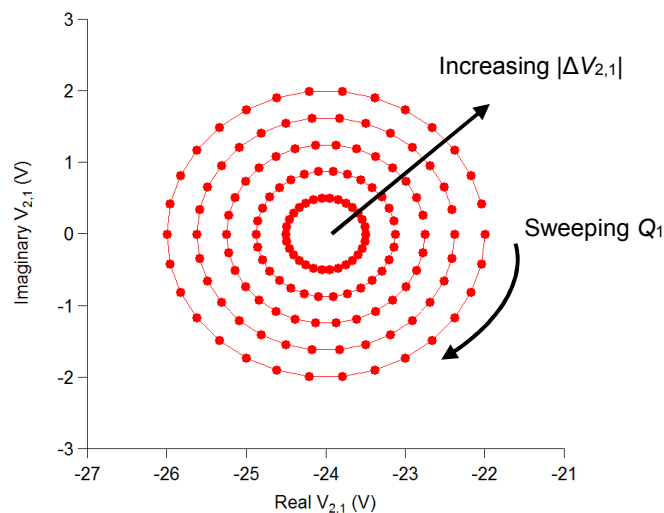


Figure 5-13: Port 2 Voltage stimulus on 2x200 μm GaN on Si transistor generating 3 coefficients.

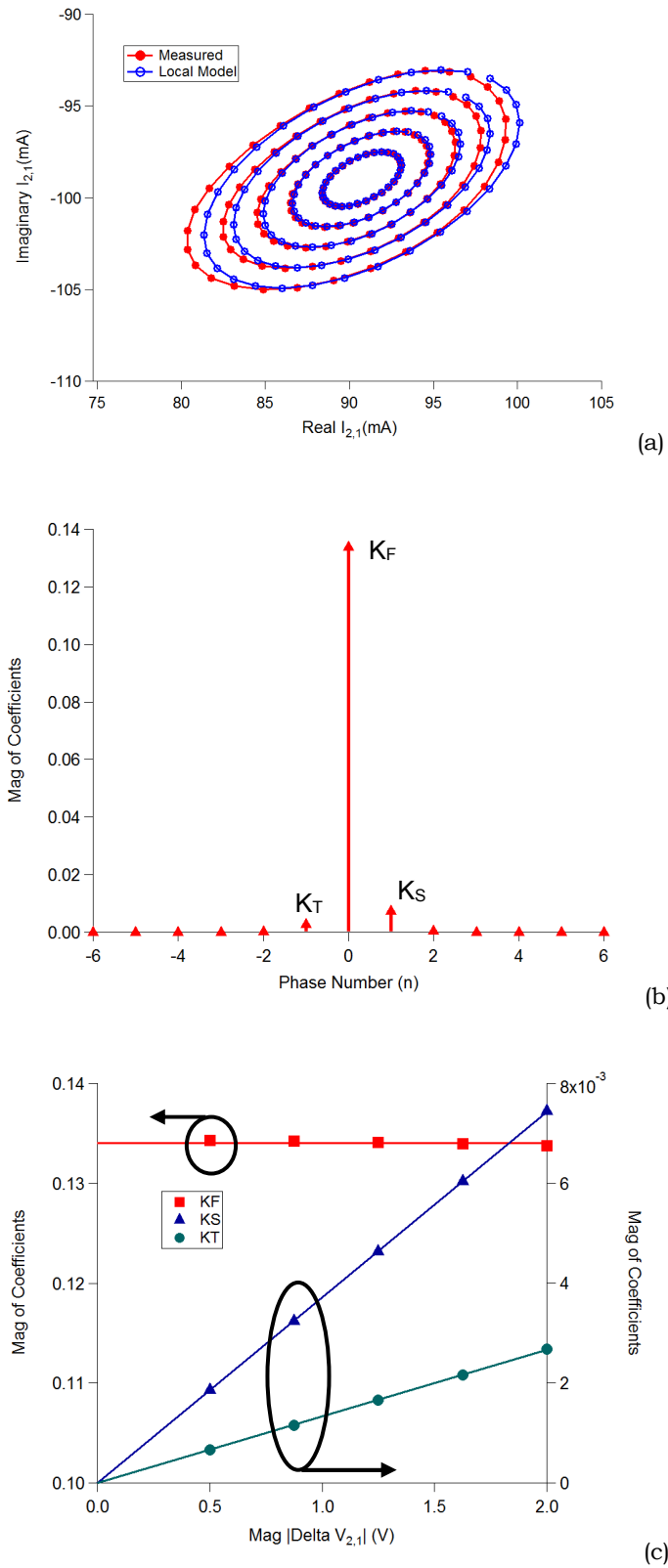
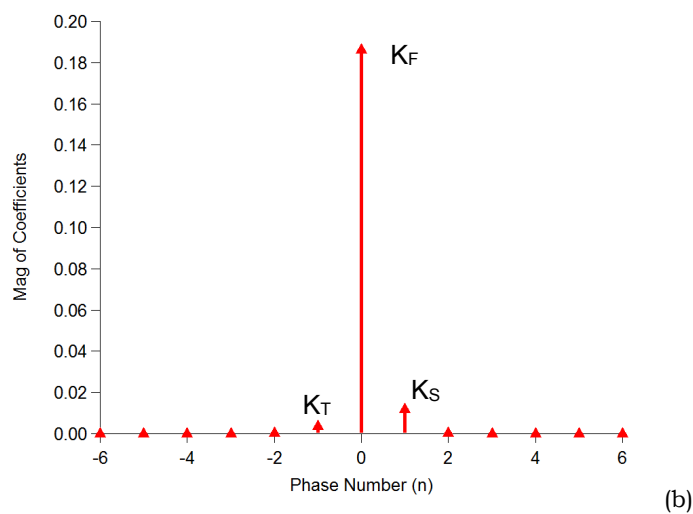
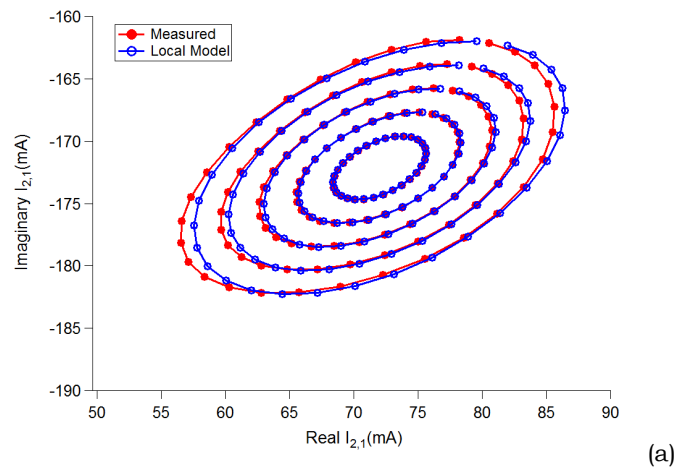


Figure 5-14: Voltage load-pull results performed on the 2x200 μm GaN on Si transistor at 4 GHz (a) $I_{2,1}(Q_1)$ results (b) Fourier Coefficients of $I_{2,1}$ with $|\Delta V_{2,1}| = 2\text{V}$ (c) Fourier Coefficients of $I_{2,1}$ versus $|\Delta V_{2,1}|$

This analysis demonstrates that the response of the transistor can be described using equation (5-43) for fundamental voltage load-pull under the small perturbation constraint. Using equation (5-43), the Y_F , Y_S and Y_T for 4 GHz can be extracted to provide a local model at that frequency. The $I_{p,1}(Q_1)$ prediction of the local model is also plotted in Fig 5-15(a), showing good agreement for small perturbations.

The analysis at all measured frequencies from 2 to 8 GHz (in 2 GHz steps) results in the same trend. The diagrams plotted in Fig. 5-15(a)-(c) are based on results at 8 GHz confirming the observations seen at 4 GHz.



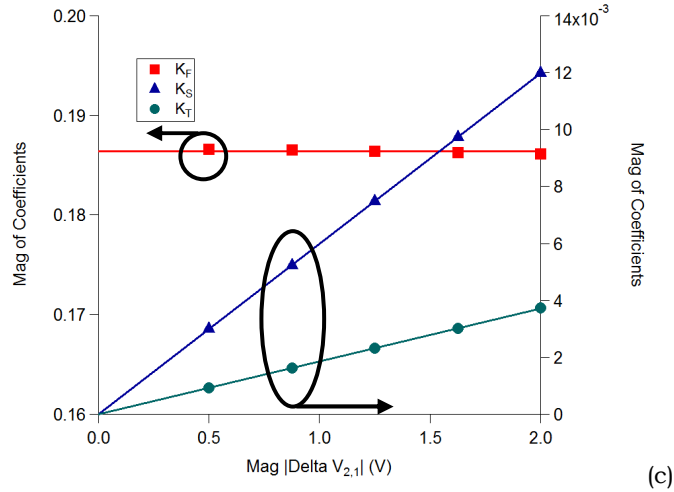


Figure 5-15: Voltage load-pull results performed on the 2x200 μm GaN on Si transistor at 8 GHz (a) $I_{2,1}(Q_1)$ results (b) Fourier Coefficients of $I_{2,1}$ with $|\Delta V_{2,1}| = 2\text{V}$ (c) Fourier Coefficients of $I_{2,1}$ versus $|\Delta V_{2,1}|$

5.4.2 Model Coefficients Over Frequency

Ranging from a small $V_{1,1}$ level, where the device is operating in the linear region, to a large $V_{1,1}$, where the device is operating into at least 3 dB compression.

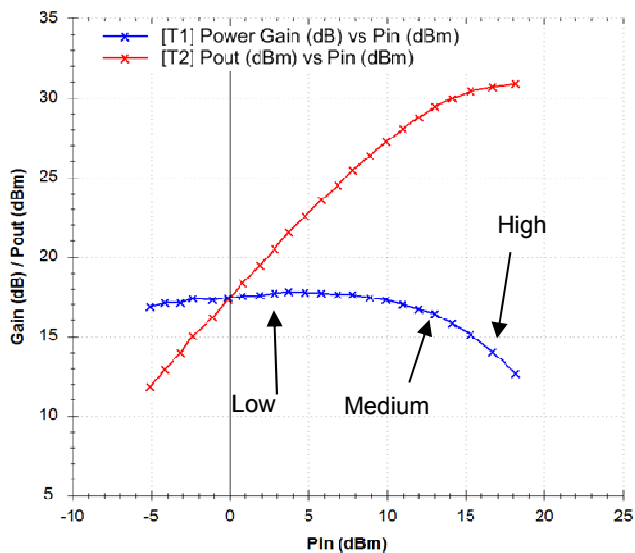
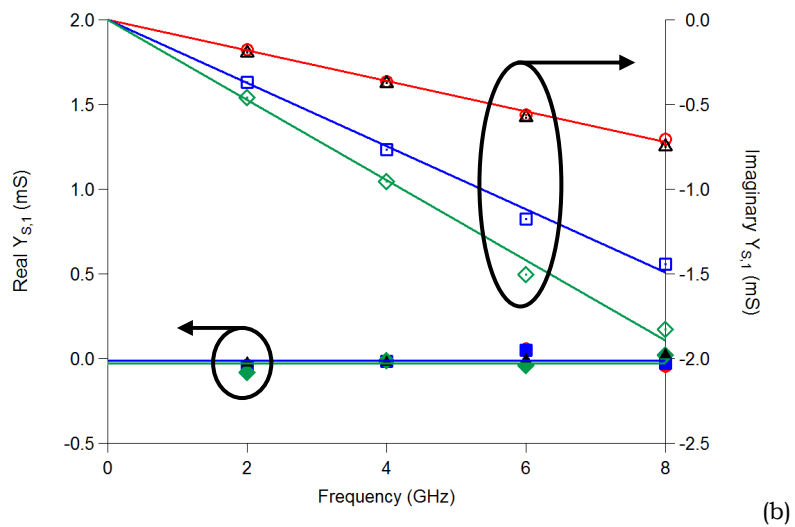
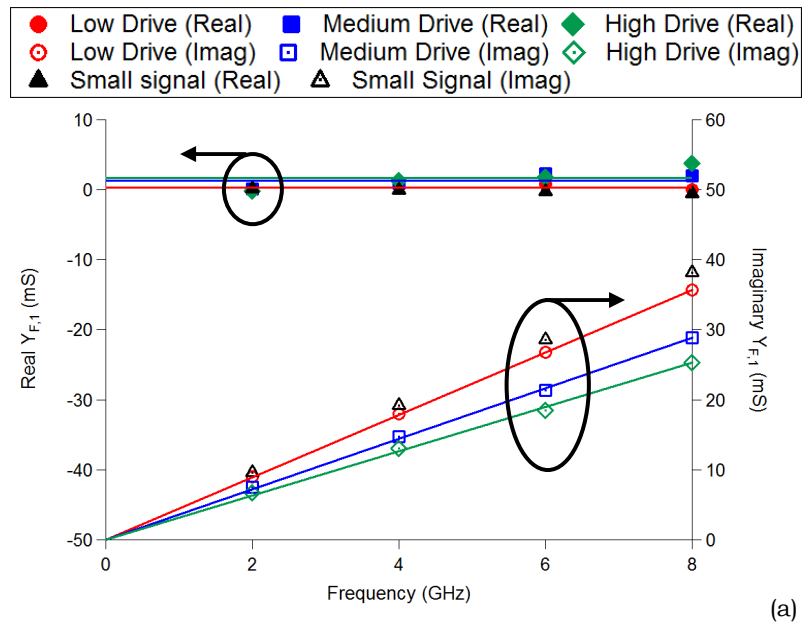
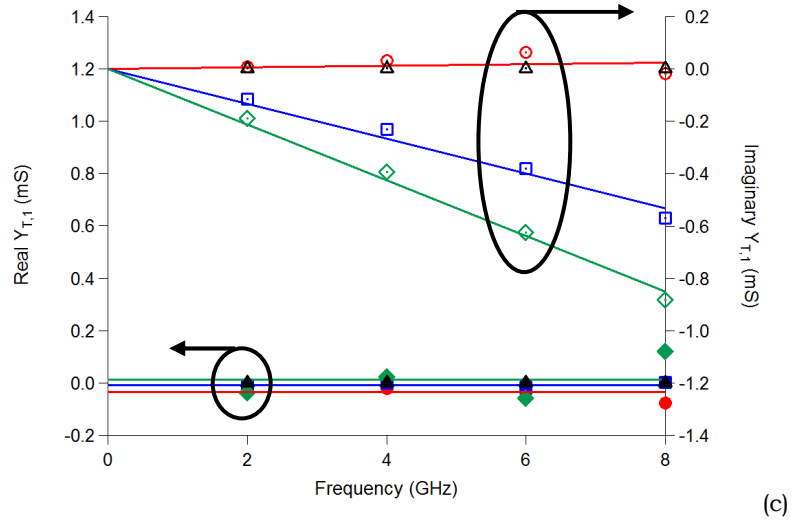


Figure 5-16: Voltage drive levels for simulations in ADS using measurements on the 2x200 μm GaN on Si transistor.

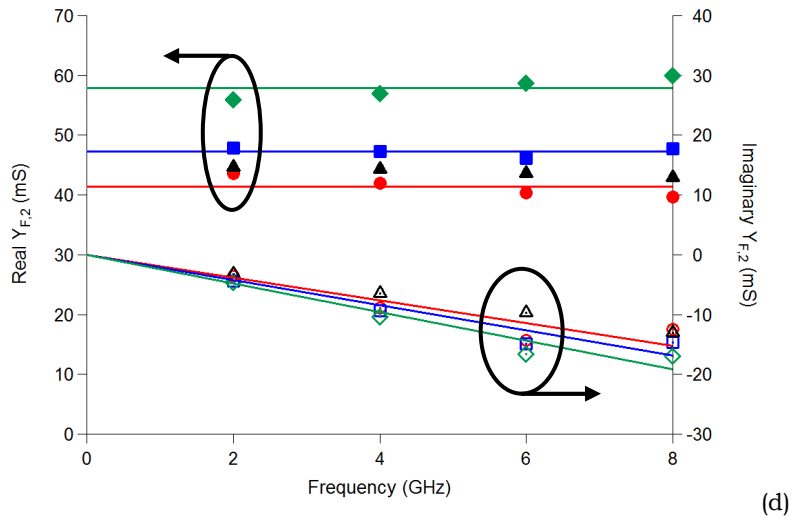
The 3 voltage levels shall be termed as low, medium and high and corresponds to a $V_{1,1}$ of 0.8 V, 2.8 V and 3.2 V respectively. Note that the drive is in terms of voltage so the level of compression is estimated based on the P_{out} that is generated and is shown in Fig. 5-16.

By plotting the extracted model coefficients, Y_F , Y_S and Y_T , versus frequency, it is clear from Fig. 5-17(a)-(f) that they support the mathematical prediction of equation (5-4) that they have the form $Y = G + j\omega C$. Fig. 5-17(a)-(c) are coefficients for port 1 whereas Fig. 5-17(d)-(f) are for port 2.

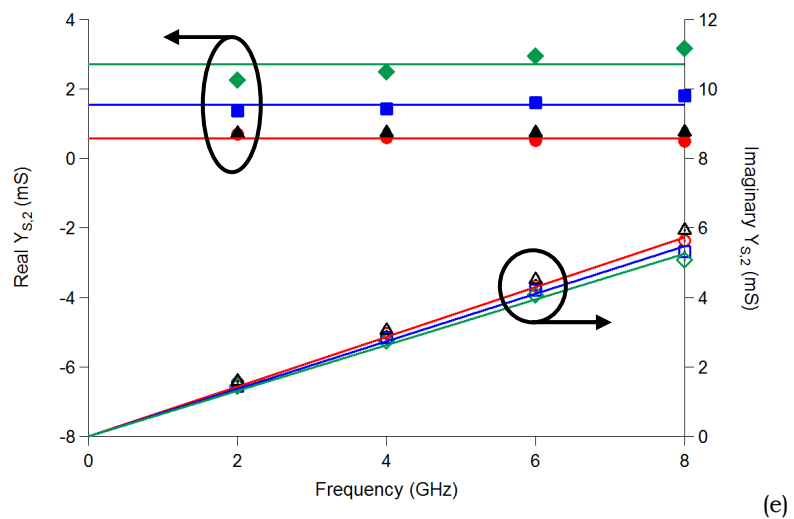




(c)



(d)



(e)

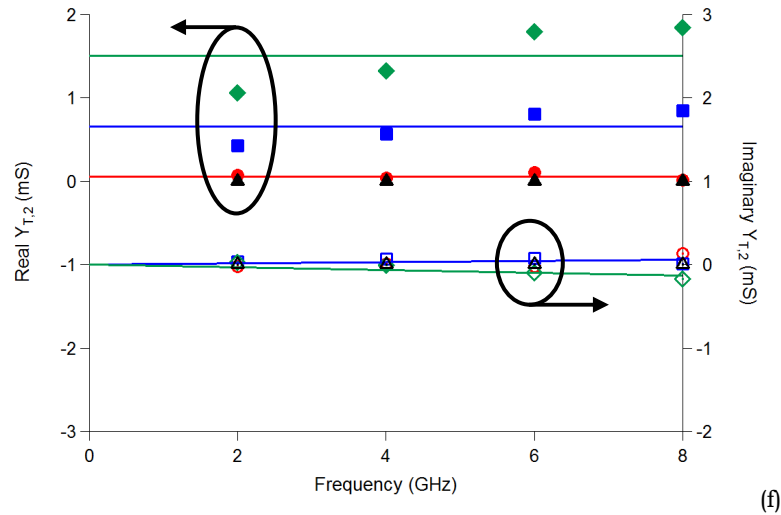


Figure 5-17: Real and imaginary coefficients as a function of frequency with varying drive levels for the 2x200 μm GaN on Si transistor (a) $Y_{F,1}$ (b) $Y_{S,1}$ (c) $Y_{T,1}$ (d) $Y_{F,2}$ (e) $Y_{S,2}$ (f) $Y_{T,2}$.

Importantly, the plots show that at small $V_{1,1}$ drive levels, values obtained are similar to the small-signal measured Y-parameters. The mathematical derivation in Section 5.1.2 that model coefficients are frequency scalable, has been experimentally verified.

Furthermore, Fig. 5-17(c) indicate the new conjugate term $Y_{T,1}$ is close to zero when operating in the linear region and appears when driven harder, just as observed with X-parameters. The same observation can be made for $Y_{T,2}$ as shown in Fig. 5-17(f). The solid lines plotted in Fig. 5-17(a)-(f) represent the curve fit over frequency, a global model, defining Behavioural model coefficients now in the form of $G_{pk,ql}^{(m)}$ and $C_{pk,ql}^{(m)}$ which are frequency independent.

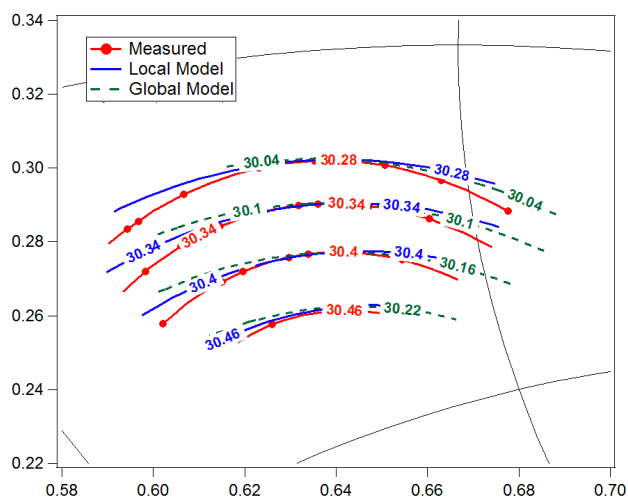
5.4.3 Model Results using 3 coefficient Frequency Scalable Model

To test the extracted models, load-pull data is regenerated, see Fig. 5-18(a), and compared with measurements, a local model at 4 GHz and the global

model (curve fit from 2-8 GHz). For this limited space, restricted by the requirement to confine use of the model to that consistent with a small perturbation, the maximum error in terms of P_{out} for the local model is 0.04 dB. Switching to a global model results in an accuracy trade-off where the maximum error is now 0.24 dB in terms of P_{out} .

However, this new global model is also able to interpolate and predict large signal behaviour at other frequencies. Fig. 5-18(b) shows the global model is able to predict, again within an accuracy of 0.22 dB, load-pull behaviour at 5 GHz (note this measured data was not used in global model extraction).

This preliminary work shows for the first time, that when appropriately defined, intrinsic admittance domain, Behavioural model coefficients that can be scaled in terms of frequency. Do note that in this experiment, the load space that can actually be modelled accurately by 3 coefficients is restricted which can be seen by referring back to in Fig. 5-15(a) and 5-16(a). The local model itself works very well at the centre of the spirals but as the $|\Delta V_{2,1}|$ is increased, it starts to fail to capture the response of the measured results.



(a)

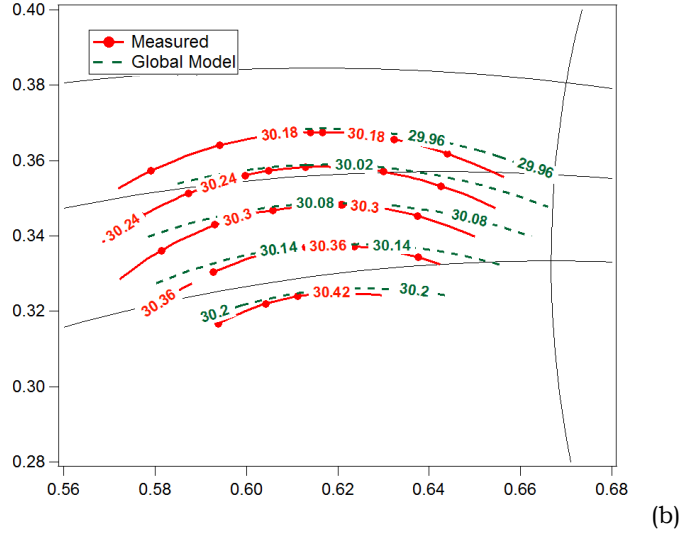


Figure 5-18: Output power contours (in dBm) for measured and modelled data for the 2x200 μm GaN on Si transistor at (a) 4 GHz (b) 5 GHz (interpolation).

This is consistent with observations that the X-parameter can only model a small localized area since its Behavioural model formulation is restricted to 3 coefficients [12]. The load-pull space for the contours cannot extend further without re-referencing the centre, either by using load-dependent X-parameters, or by increasing model complexity, such as in the Cardiff Model.

5.4.4 Discussion on Vref in model extraction

During the extraction process, $V_{2,1\text{ref}}$ must always be a real number. In this work, the optimum load is defined on the real axis and the load-pull measurements were performed by taking into account C_{ds} . This means that all the load-pull data when de-embedded will be at the same location on the real axis of the Smith Chart.

By considering the output current,

$$\begin{aligned}
 I_{2,1} &= Y_{F\ 2,1} |v_{1,1}| + Y_{S\ 2,1} V_{2,1} + Y_{T\ 2,1} V_{2,1}^* \\
 &= Y_{F\ 2,1} |v_{1,1}| + Y_{S\ 2,1} (V_{2,1\text{ref}} + \Delta V) + Y_{T\ 2,1} (V_{2,1\text{ref}} + \Delta V)^*
 \end{aligned} \tag{5-44}$$

$$= \{Y_{F\ 2,1}|v_{1,1}| + Y_{S\ 2,1}V_{2,1\ ref} + Y_{T\ 2,1}V_{2,1\ ref}^*\} + Y_{S\ 2,1}\Delta V \\ + Y_{T\ 2,1}\Delta V^*$$

If $V_{2,1\ ref}$ is a complex number, the equation will expand to

$$I_{2,1} = (G_F + j\omega C_F)|v_{1,1}| \\ + (G_S + j\omega C_S)(\alpha + j\beta) + (G_T + j\omega C_T)(\alpha + j\beta) \\ + Y_{S\ 2,1}\Delta V + Y_{T\ 2,1}\Delta V^* \\ = G_F|v_{1,1}| + j\omega C_F|v_{1,1}| + G_S\alpha \\ + jG_S\beta + j\omega C_S\alpha - \omega C_S\beta + G_T\alpha - jG_T\beta + j\omega C_T\alpha \\ + \omega C_T\beta + Y_{S\ 2,1}\Delta V + Y_{T\ 2,1}\Delta V^* \quad (5-45)$$

Having a $-\omega C_S\beta + \omega C_T\beta$ term creates a frequency dependence that makes it unable to be separated. Therefore, the reference load should only be a real number.

5.5 Experimental Model Validation on 2nd GaN wafer (Extension to 6 model coefficients)

Here the same extraction process is performed on WIN Semiconductors (Wafer ID: EN004013) 2x200 μ m GaN on SiC transistor with stimulus as described in equation (24) - (26). This is to prove that the extraction process is robust and can be used on different wafers. Measurements were performed at 2, 4, 5, 6 and 8 GHz on the GaN on SiC transistor but extraction is performed on frequencies 2, 4 and 8 GHz so that the resulting model can be used to predict behaviour at 5 GHz and 6 GHz.

In this validation, the work is extended from the previous example to include more coefficients to model a larger perturbation space, i.e. a larger load-pull

space. In other words, the ADS circuit in Fig. 5-10 is now used to perform voltage load-pull on measurements from the GaN on SiC transistor but with a larger $|\Delta V_{2,1}|$ so that additional Fourier Terms will be generated.

In this investigation the aim will be to see if the theoretical prediction of having model coefficients in the form $Y = G + j\omega C$ is still valid if the number of coefficients is extended beyond 3 coefficients (X-Parameter terms).

5.5.1 Admittance Domain Model Coefficients

When $|\Delta V_{2,1}|$ of the stimulus in equation (5-42) is increased to cover an even larger load-pull space, this will result in the appearance of additional Fourier terms when $\widehat{I_{p,1}}(Q)$ is Fourier Transformed. By reviewing the FFT results, the number of model terms (complexity) can be determined. Typically, the terms that would appear are $\langle K_{p1,21}^{(Tsq)}, K_{p1,21}^{(T)}, K_{p1,11}^{(F)}, K_{p1,21}^{(S)}, K_{p1,21}^{(Ssq)} \rangle$ or in the Y-parameter form of $\langle Y_{p1,21}^{(Tsq)}|v_{2,1}|, Y_{p1,21}^{(T)}|v_{2,1}|, Y_{p1,11}^{(F)}|v_{1,1}|, Y_{p1,21}^{(S)}|v_{2,1}|, Y_{p1,21}^{(Ssq)}|v_{2,1}| \rangle$. These are squared phase terms at location 2 and -2. There is also appearance of terms $K_{p1,11}^{(Fsq)}$ and $Y_{p1,11}^{(Fsq)}|v_{1,1}|$ at the center phase location of 0.

Note from equation (5-42) that $V_{2,1}(Q_1)$ is actually a reference voltage plus a small perturbation around the reference voltage point. The reference voltage helps to bring the simulation to the optimum location for the voltage load-pull. To simplify the extraction equation, the output voltage stimulus is considered in the form as described by equation (5-46). With additional FFT terms, resulting current response, $I_{p,1}(Q_1)$ is extended from (5-43) and becomes (5-47).

$$V_{2,1res} = V_{2,1}(Q_1) - V_{2,1ref} = |\Delta V_{2,1}|e^{-j\phi} = |\Delta v_{2,1}|Q_1 \quad (5-46)$$

$$\begin{aligned}
 I_{p,1}(Q_1) &= K_F + K_S Q_1 + K_T Q_1^{-1} + K_S^2 Q_1^2 + K_T^2 Q_1^{-2} \\
 &= Y_{F,p} |v_{1,1}| + Y_{S,p} V_{2,1res} + Y_{T,p} V_{2,1res}^* + Y_{S,p}^2 V_{2,1res}^2 \\
 &\quad + Y_{T,p}^2 V_{2,1res}^{*2} \\
 &= Y_{F,p} |v_{1,1}| + Y_{S,p} |\Delta v_{2,1}| Q_1 + Y_{T,p} |\Delta v_{2,1}| Q_1 \\
 &\quad + Y_{S,p}^2 |\Delta v_{2,1}| Q_1 + Y_{T,p}^2 |\Delta v_{2,1}| Q_1
 \end{aligned} \tag{5-47}$$

The statement above can be investigated experimentally by performing the extraction with larger $|\Delta V_{2,1}|$ than used previously allow for the appearance of these 6 coefficients.

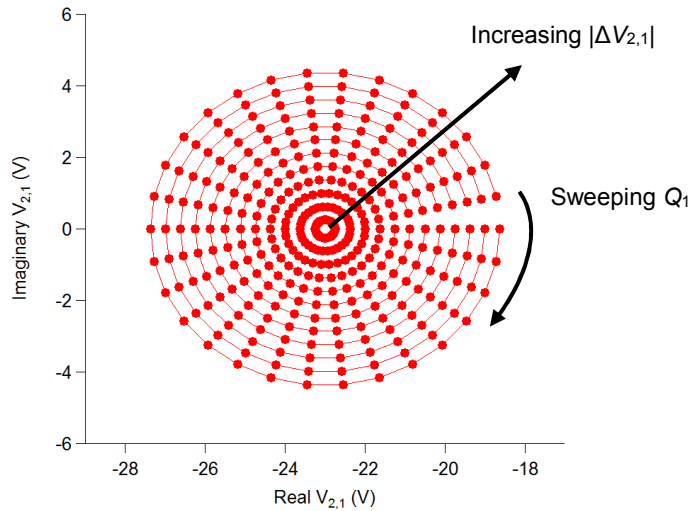
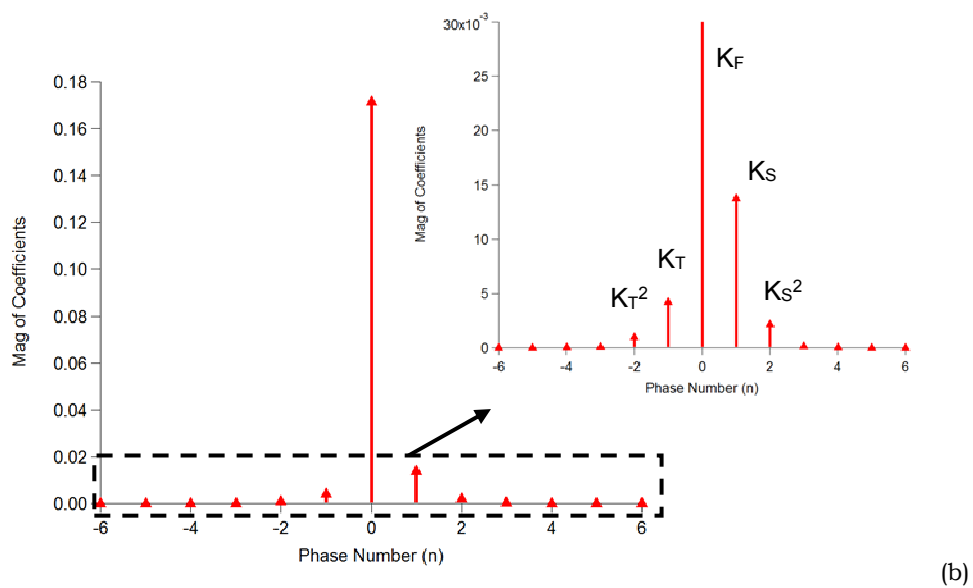
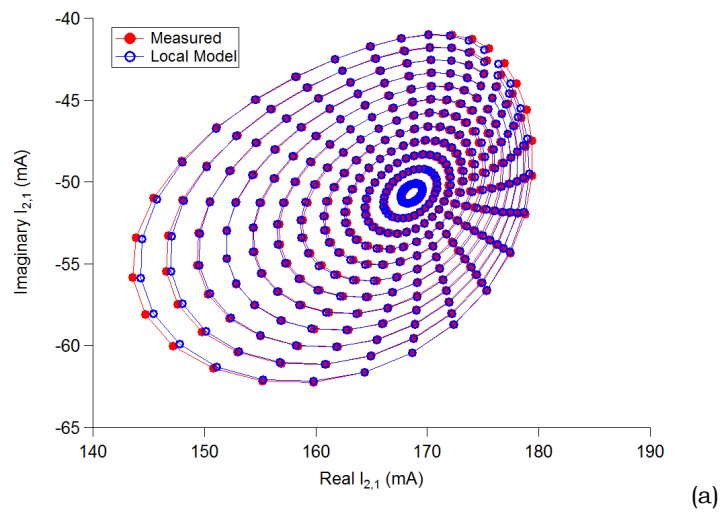


Figure 5-19: Port 2 Voltage stimulus on 2x200 μm GaN on SiC transistor generating 6 coefficients.

In Fig. 5-19, the Port 2 voltage stimulus described by equation (5-42) is performed with $|\Delta V_{2,1}|$ from 0.25 V to 4.375 V in steps of 0.375 V (larger compared to the simulation in Section 5.4). The resulting $I_{2,1}$ at 2 GHz is shown in Fig. 5-20(a). The Fourier Coefficients extracted from the $I_{2,1}$ spiral at the largest $|\Delta V_{2,1}|$ of 4.375 V is shown in Fig. 5-20(b). Notice the zoomed

diagram of Fig. 5-20(b) which shows the appearance of the additional "squared terms" when a large $|\Delta V_{2,1}|$ is used.

This is a confirmation of equation (5-47) which states that the $I_{2,1}(Q_1)$ response can be described by 6 coefficients. As shown in Fig. 5-20(c), increasing $|\Delta V_{2,1}|$ will cause the appearance of additional FFT terms such as K_S^2 and K_T^2 as well as a curvature in K_F . The modelled results of the $I_{2,1}$ can be regenerated from the extracted Fourier Coefficients and these are plotted Fig. 5-20(a).



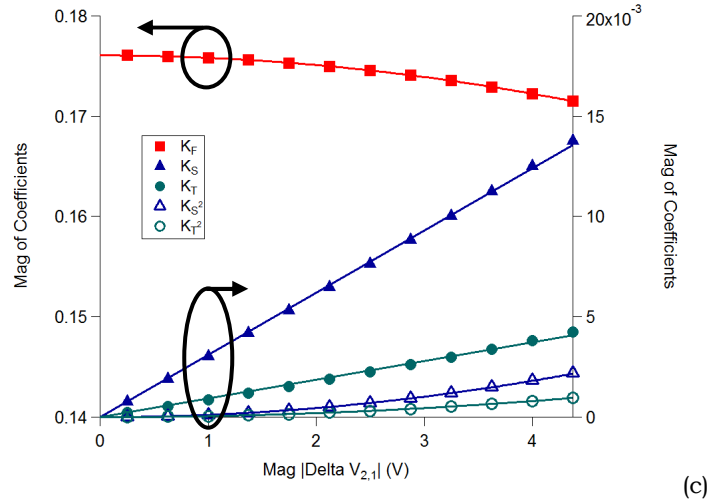


Figure 5-20: Voltage load-pull results performed on the 2x200 μm GaN on SiC transistor at 2 GHz (a) $I_{2,1}(Q_i)$ results (b) Fourier Coefficients of $I_{2,1}$ with $|\Delta V_{2,1}| = 4.375\text{V}$ (c) Fourier Coefficients of $I_{2,1}$ versus $|\Delta V_{2,1}|$

The need for using more coefficients (in this case 6 terms) just like in the Cardiff Model is highlighted in Fig. 5-21 where we use just the first 3 major terms, the X-Parameter type model, over the full range. At large $|\Delta V_{2,1}|$, this “small perturbation” model, as expected, fails to capture both the movement of the centre and the more complex shape.

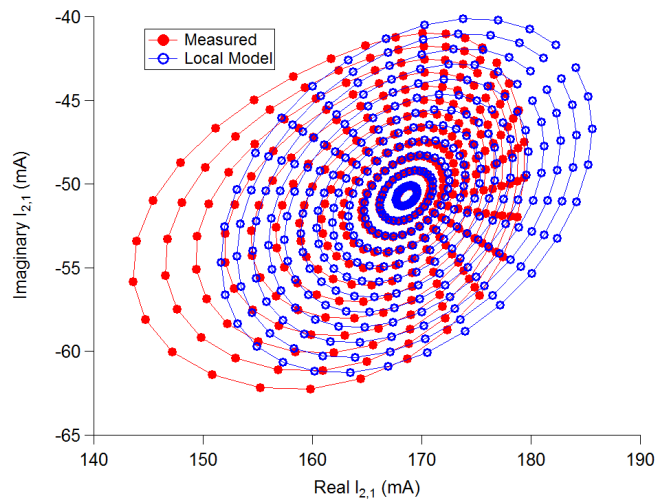
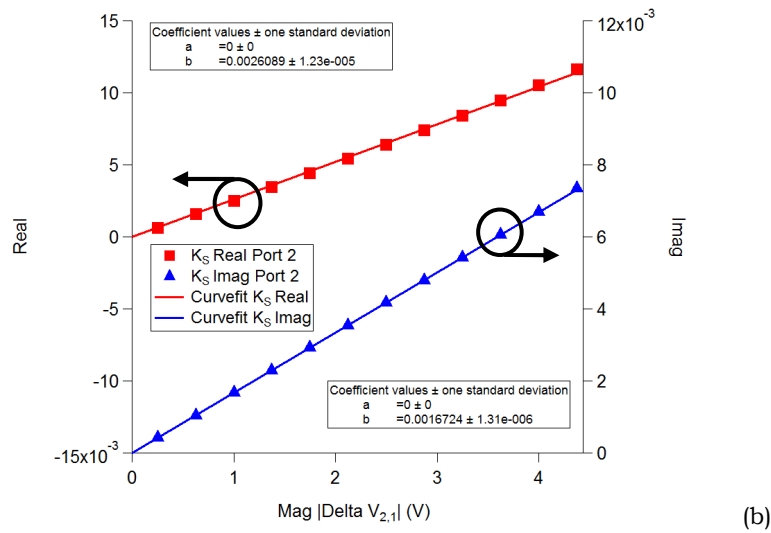
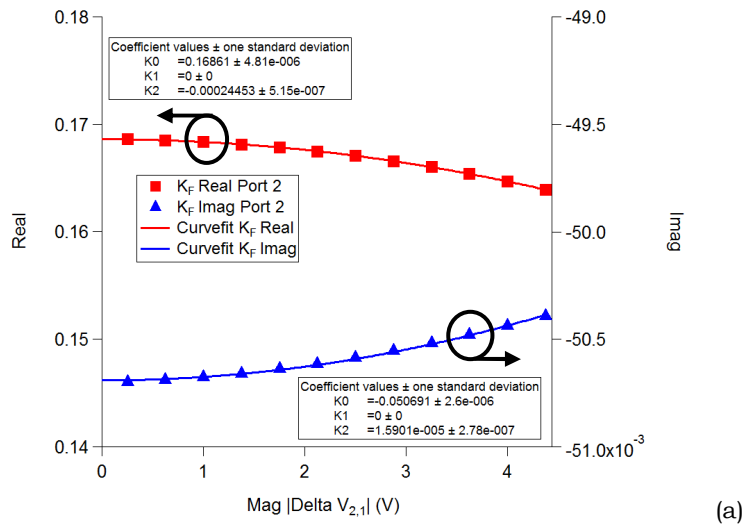


Figure 5-21: $I_{2,1}(Q)$ for 2x200 μm GaN on SiC transistor at 2 GHz modelled using only 3 coefficients

Now with this trend confirmed for $L_{2,1}$, based on equation (5-47), the 6 coefficients can be curve fitted over $|\Delta V_{2,1}|$ so that a local model for all values of $|\Delta V_{2,1}|$ can be extracted. The plots for the real and imaginary parts of K_F , K_S , K_T , K_S^2 and K_T^2 versus $|\Delta V_{2,1}|$ at 2 GHz is shown in Fig. 5-22 (a)-(f). Note that the appearance of K_F^2 is on the same phase location as K_F .



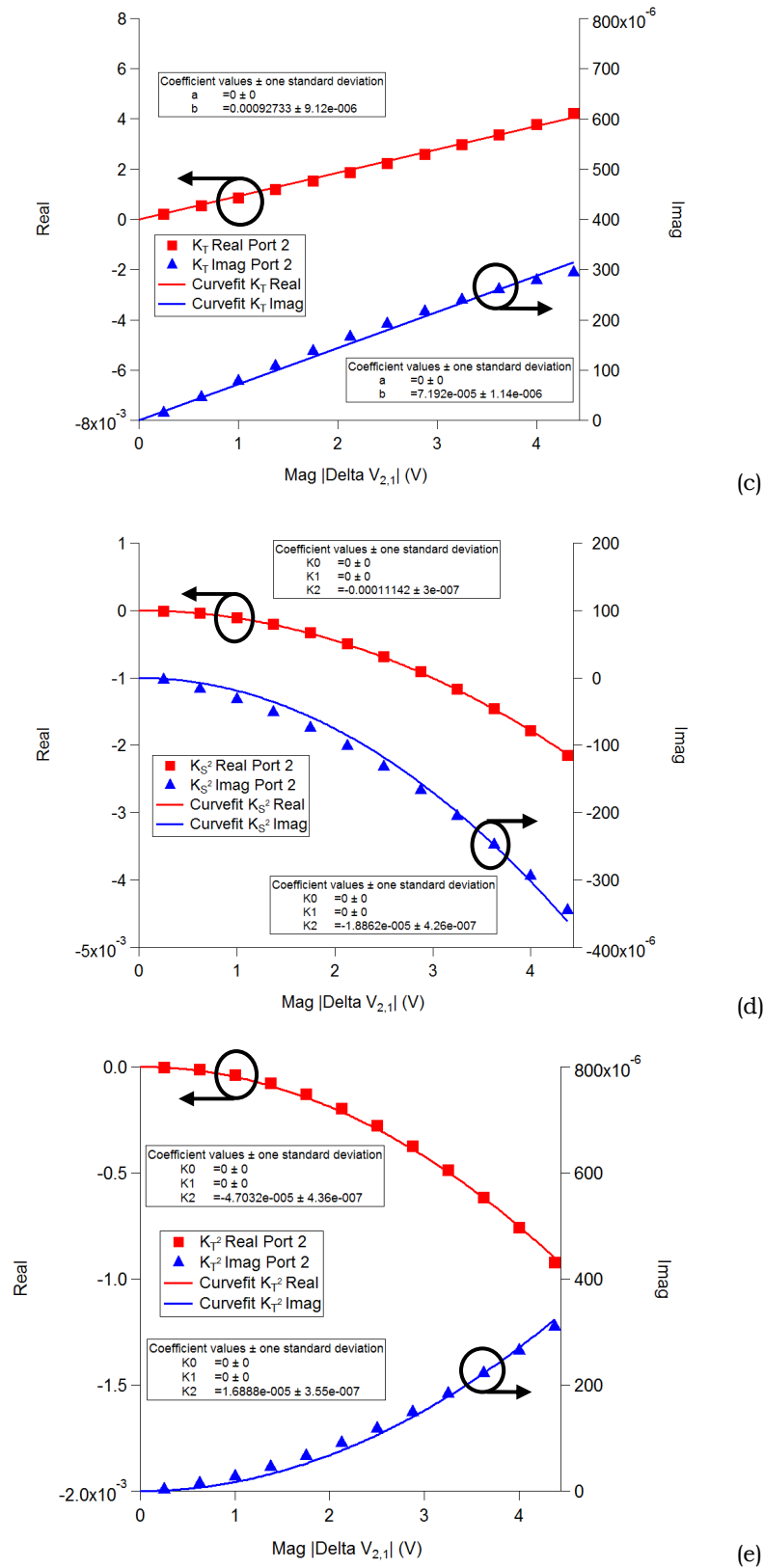
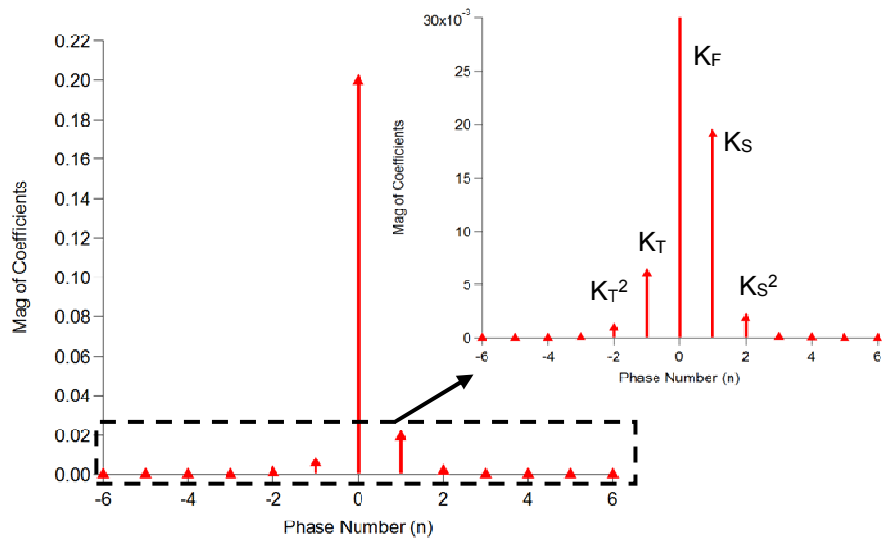
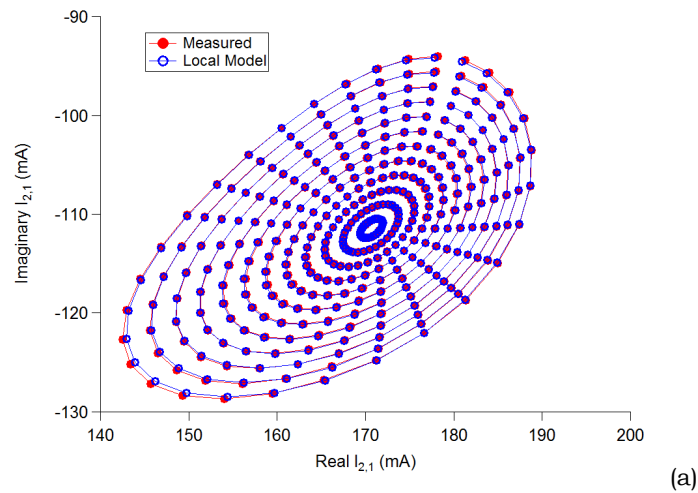


Figure 5-22: Curve fit of coefficients for $I_{2,1}(Q)$ over $|\Delta V_{2,1}|$ to obtain local Y-parameters at 2 GHz

(a) K_F and K_F^2 (b) K_S (c) K_T (d) K_S^2 (e) K_T^2

Depending on the location of the phase terms, the curve fit of either $A+Bx$ or $A+Cx^2$ is used. For example, the K_S^2 term has phase location of 2 so the plot over $|\Delta V_{2,1}|$ is curve-fitted with $A+Cx^2$ to obtain the C term. This C term would be the Y_S^2 . It is these (A, B and/or C) coefficients, 6 in total, which form the Y-parameters. These Y-parameters become the local model coefficients for the frequency at which it was extracted.



(b)

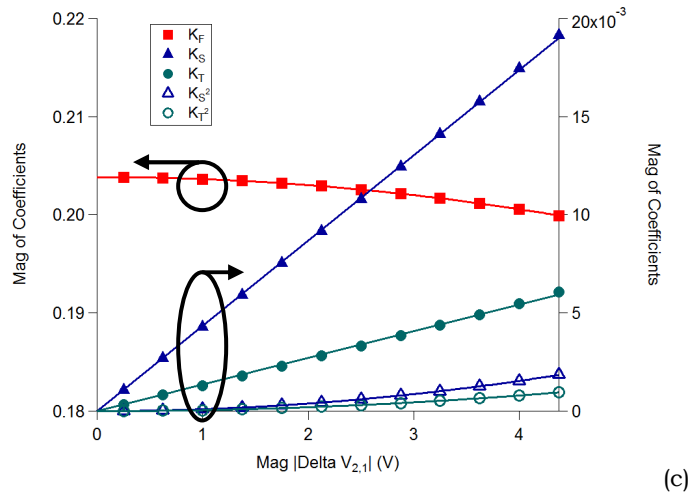


Figure 5-23: Voltage load-pull results performed on the 2x200 μm GaN on SiC transistor at 4 GHz (a) $I_{2,1}(Q_1)$ results (b) Fourier Coefficients of $I_{2,1}$ with $|\Delta V_{2,1}| = 4.375\text{V}$ (c) Fourier Coefficients of $I_{2,1}$ versus $|\Delta V_{2,1}|$

Now the entire extraction process is repeated at 4 and 8 GHz. The results for 4 GHz is shown here as a confirmation that the process is sound and that the response observed is very similar to that already shown at 2 GHz. Results in Fig. 5-23(a)-(c) are to serve as a confirmation that the trends observed at 2 GHz are also valid at 4 GHz and hence, at other frequencies as well. For further confirmation, please see Appendix B.1 for the results of the extraction at 8 GHz.

As shown in Fig. 5-24, with a larger $|\Delta V_{2,1}|$, as compared to Fig. 5-23(a), the 3 term coefficients is not enough to describe the system over this extended perturbation area. Most noticeable is the centre shift in the $I_{2,1}$ model because of the Y_F "squared term". Fig. 5-25 (a)-(e) show the curve fit over $|\Delta V_{2,1}|$ to obtain the Y-parameters at 4 GHz.

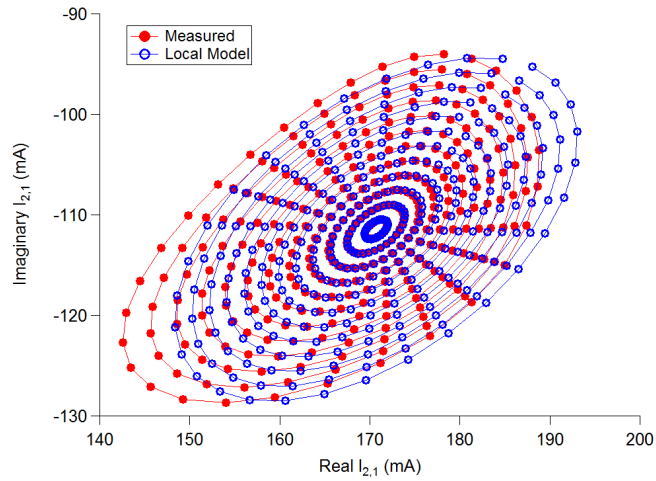
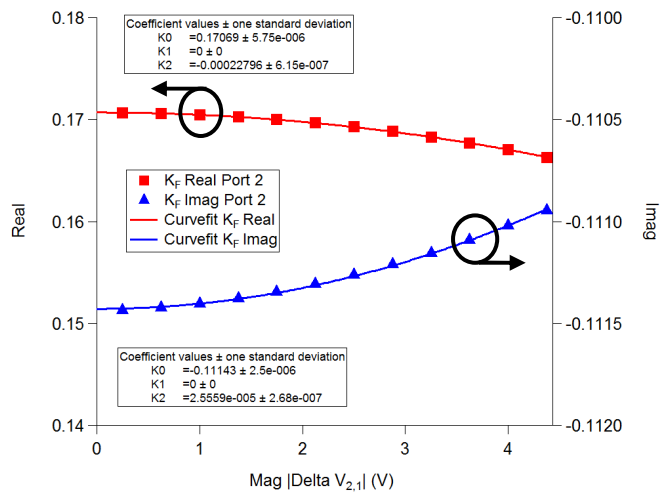
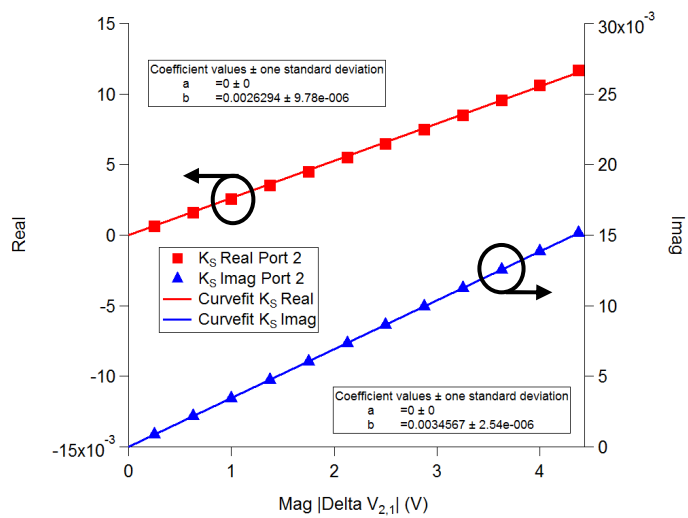


Figure 5-24: $I_{2,1}(Q)$ for 2x200 μm GaN on SiC transistor at 4 GHz modelled using only 3 coefficients



(a)



(b)

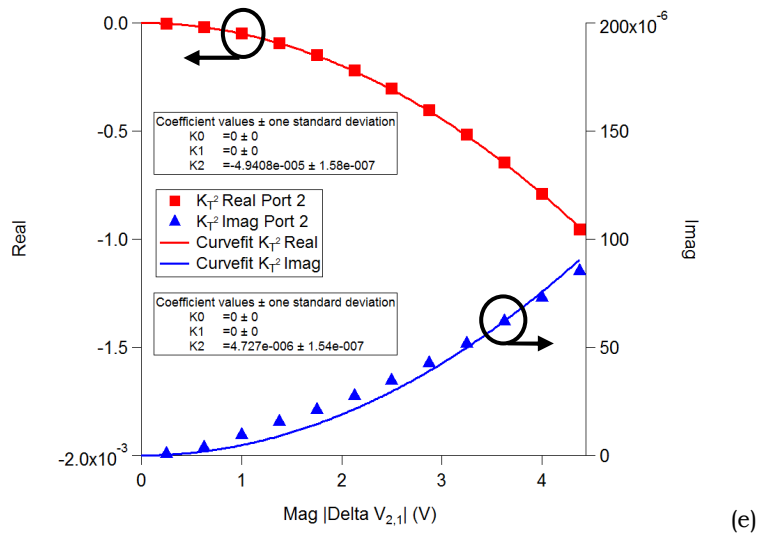
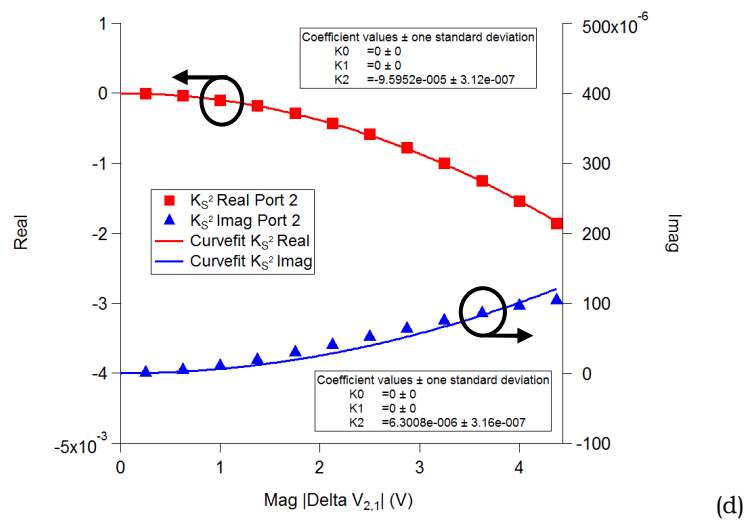
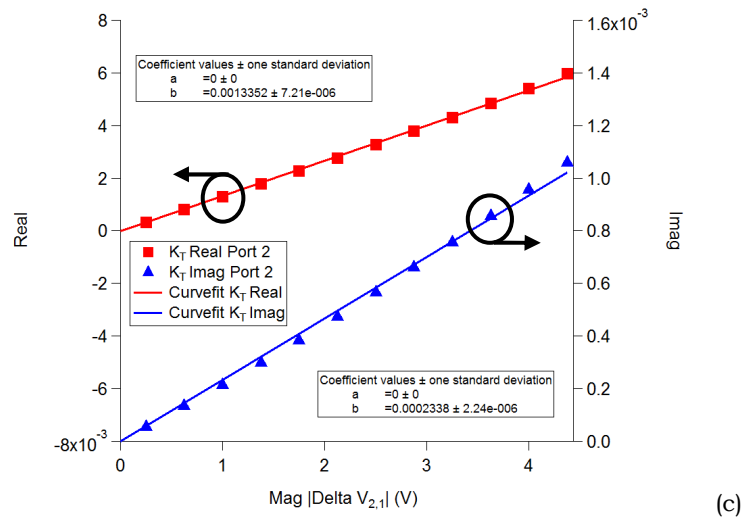


Figure 5-25: Curve fit of coefficients for $I_{2,1}(Q)$ over $|\Delta V_{2,1}|$ to obtain local Y-parameters at 4 GHz

(a) K_F and K_F^2 (b) K_S (c) K_T (d) K_{S^2} (e) K_T^2

5.5.2 Model Coefficients Over Frequency

To investigate whether a frequency independent model, using the 6 model coefficients extracted at 2, 4 and 8 GHz is possible, their variation with frequency is investigated.

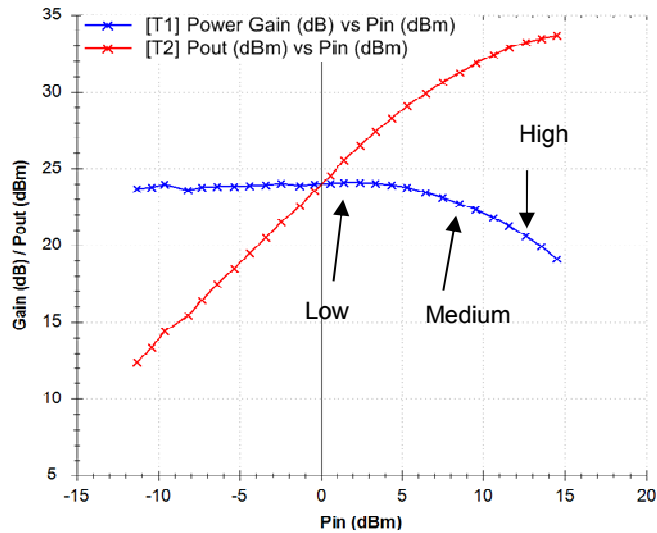
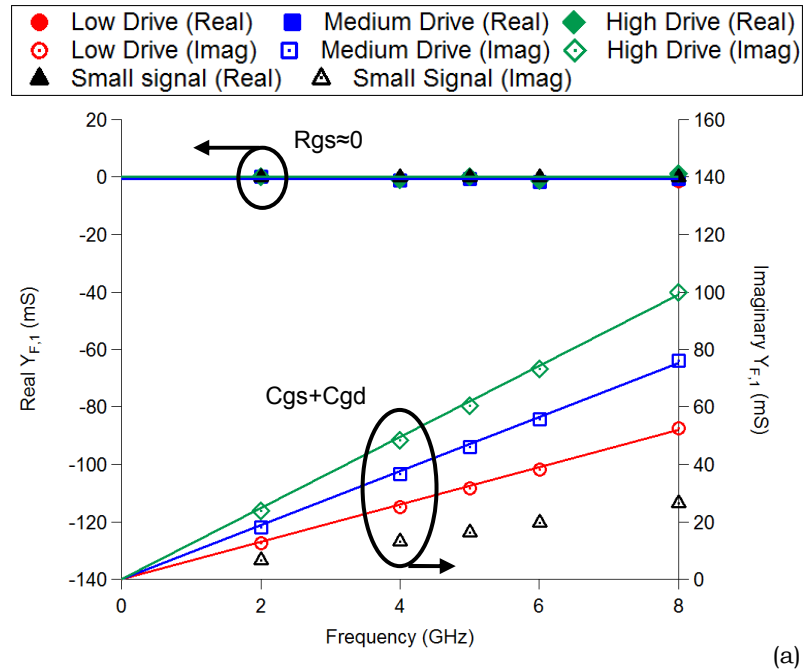


Figure 5-26: Voltage drive levels for simulations in ADS using measurements on the 2x200 μm GaN on SiC transistor.

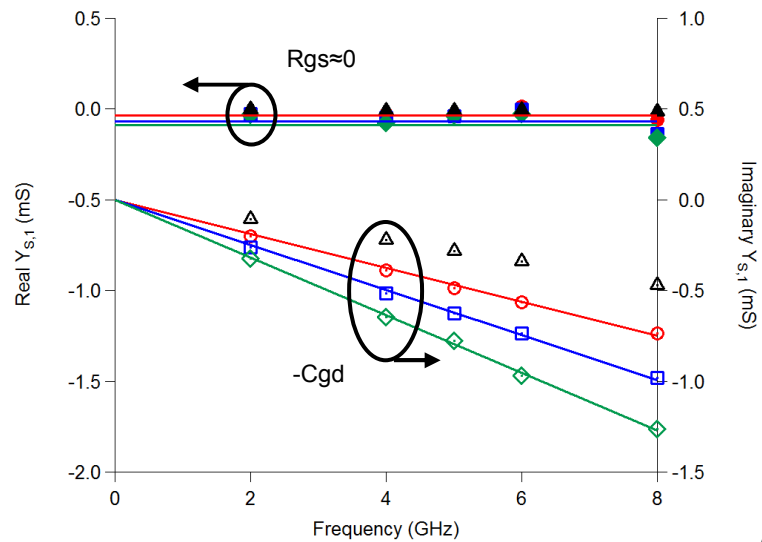
At each measured frequency, results at 3 different voltage drive levels are shown which corresponds to the drive levels shown in Fig. 5-26. As before, extraction is performed at 3 voltage levels, denoted as low (linear), medium (1 dB into compression) and high (3 dB into compression) and corresponds to a $V_{1,1}$ of 1.4 V, 2.1 V and 2.7 V respectively.

By plotting the extracted model coefficients, Y_F , Y_S , Y_T , Y_{Fsq} , Y_{Ssq} and Y_{Tsq} versus frequency, it is clear from Fig 5-27 (Port 1 results) and Fig. 5-28 (Port 2 results) that they do have the form $Y = G + j\omega C$. As expected, the plots show that at small $V_{1,1}$ drive levels, values obtained are similar to the small-signal measured Y-parameters.

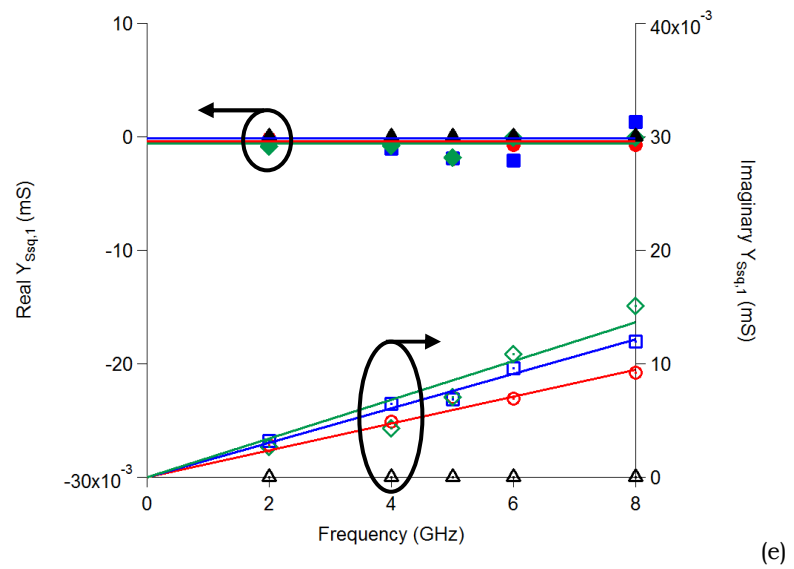
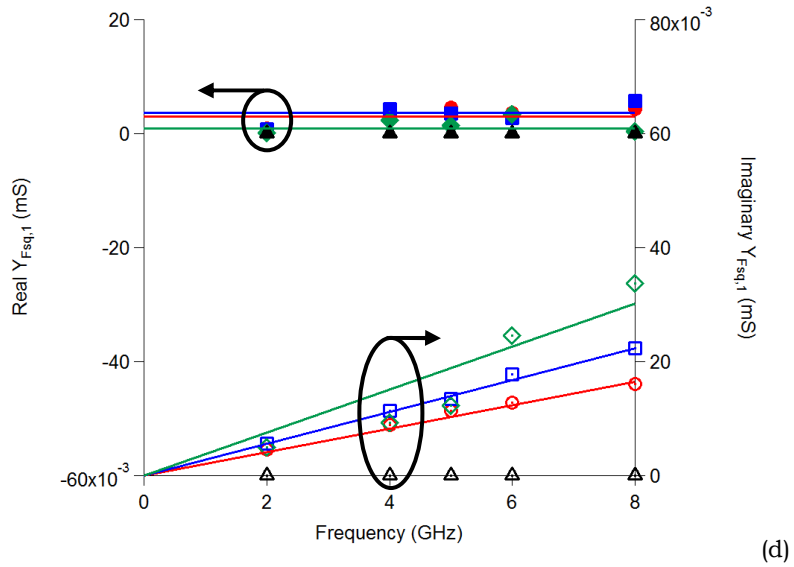
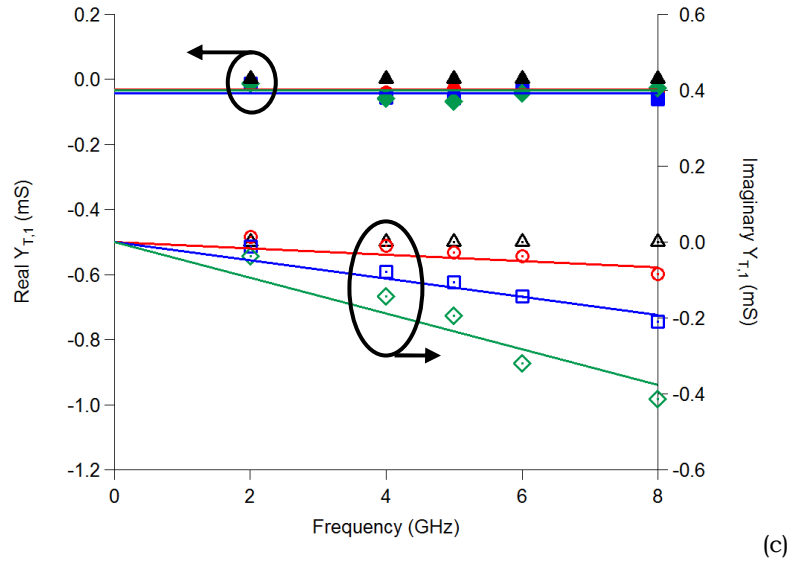
The solid lines plotted in Fig. 5-27 and Fig. 5-28 represent the curve fit over frequency, which will become the frequency independent global model. These results reconfirm the mathematical prediction that the model coefficients in the form $Y = G + j\omega C$ is valid even as the number of coefficients is extended.



(a)



(b)



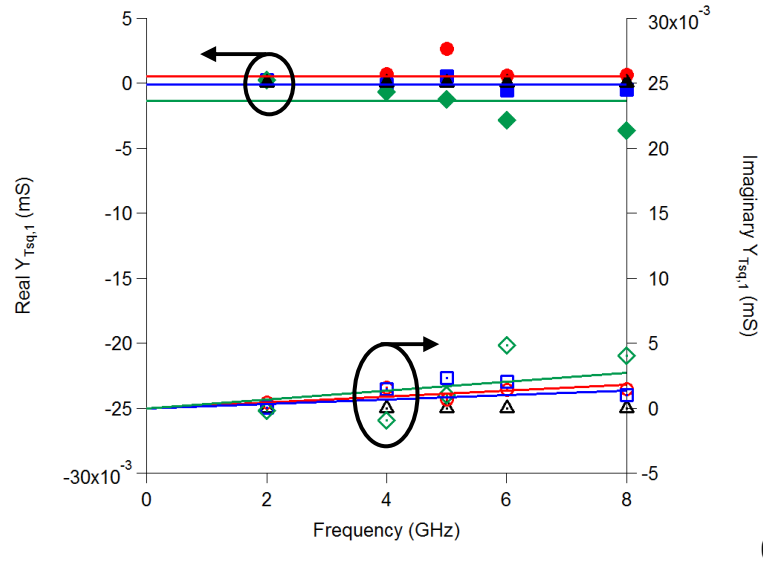
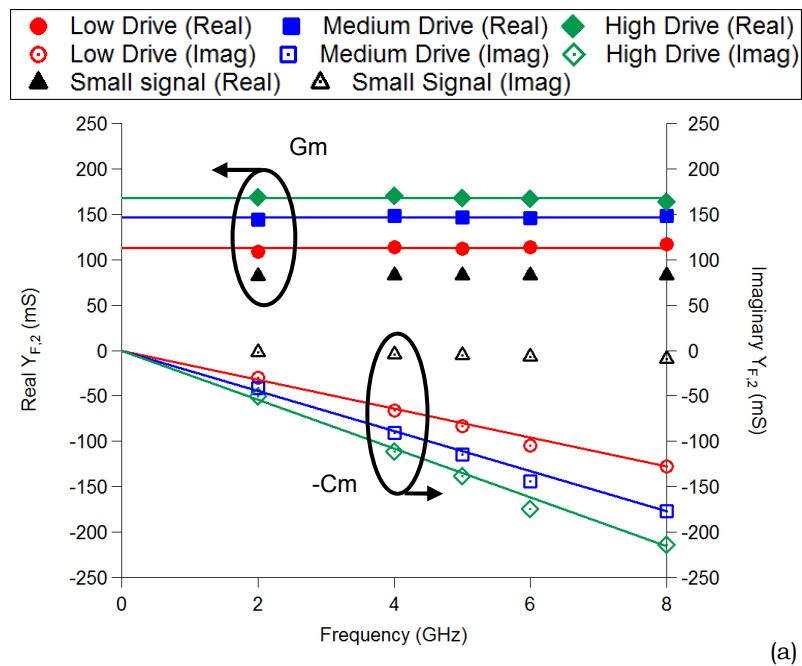
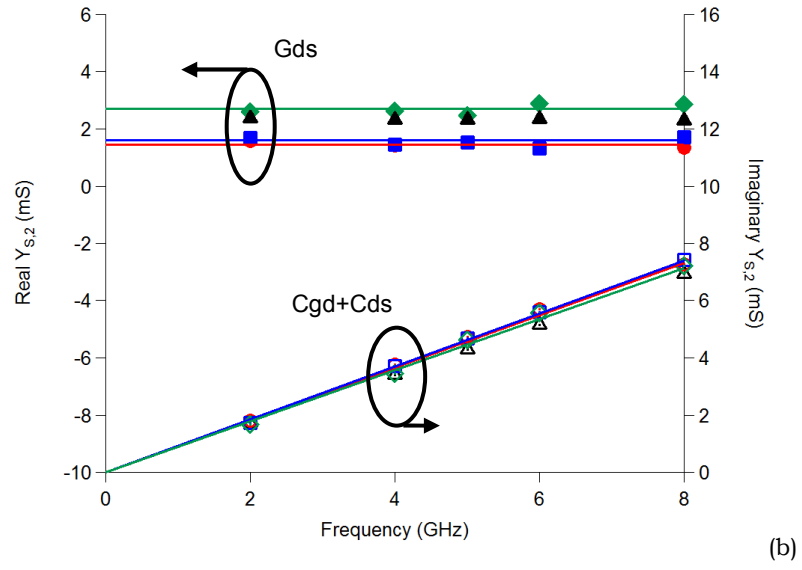


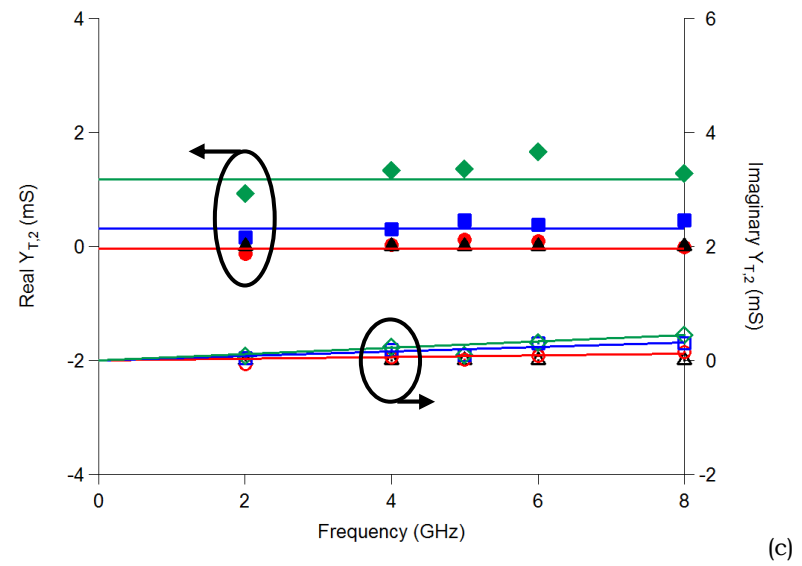
Figure 5-27: Real and imaginary coefficients as a function of frequency with varying drive levels for 2x200 μm GaN on SiC transistor on Port 1 (a) $Y_{F,1}$ (b) $Y_{S,1}$ (c) $Y_{T,1}$ (d) $Y_{Fsq,1}$ (e) $Y_{Ssq,1}$ (f) $Y_{Tsq,1}$.

Scatter from the results especially at higher order coefficient terms can be seen since these values are very small but the general trend of the coefficients is very obvious. For completeness, results at 5 and 6 GHz are also shown in Fig. 5-27 and 5-28, indicating that the trend is valid throughout this frequency range. However, the global model was not extracted from these frequencies.

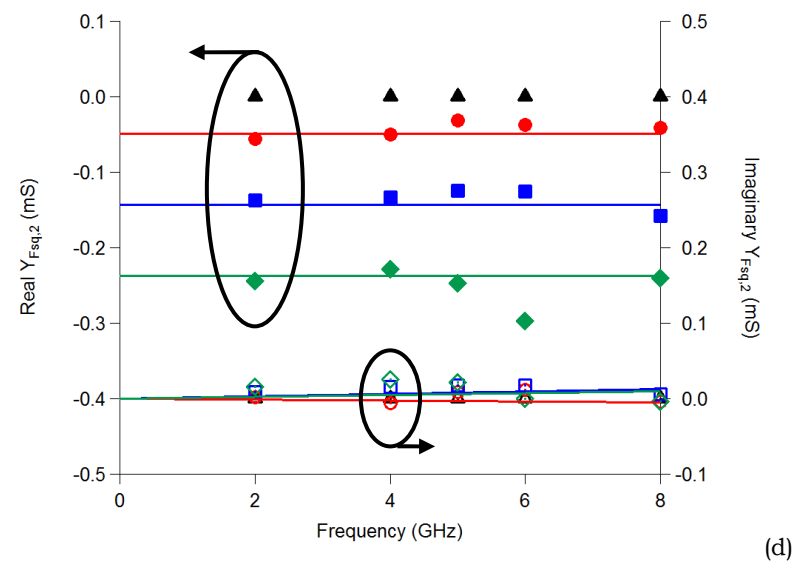




(b)



(c)



(d)

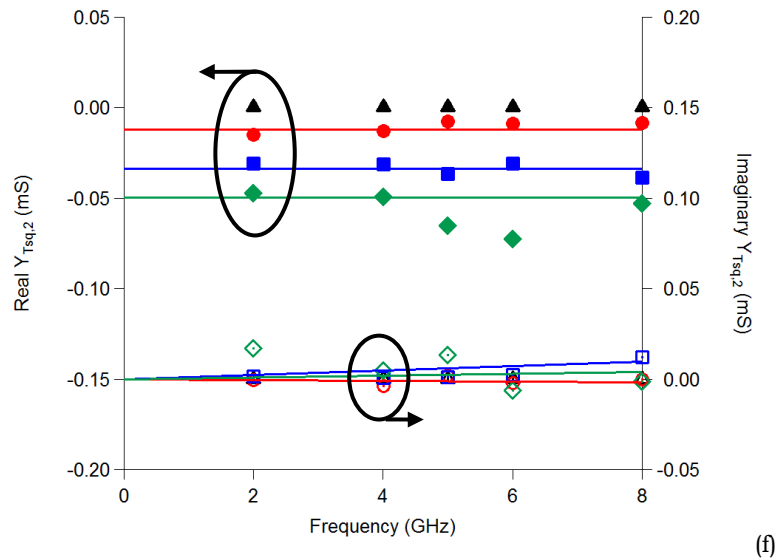
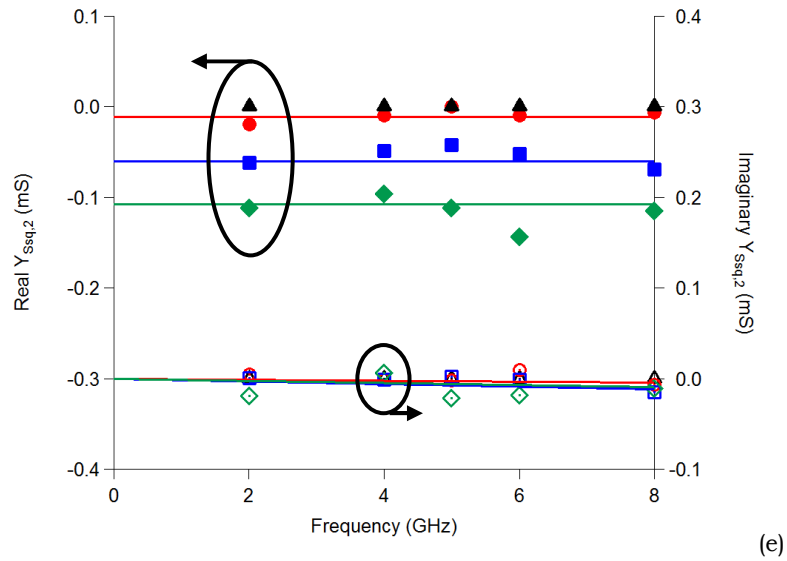


Figure 5-28: Real and imaginary coefficients as a function of frequency with varying drive levels for 2x200 μm GaN on SiC transistor on Port 2 (a) $Y_{F,2}$ (b) $Y_{S,2}$ (c) $Y_{T,2}$ (d) $Y_{Fsq,2}$ (e) $Y_{Ssq,2}$ (f) $Y_{Tsq,2}$.

During the extraction process, only results from 2, 4 and 8 GHz were selected for the curve fit via a "datamask" function in the Igor program. Further analysis of the results shown in Fig. 5-27(a)-(b) and 5-28(a)-(b) confirm that the coefficients match the representation of the intrinsic circuit shown in Fig. 5-29.

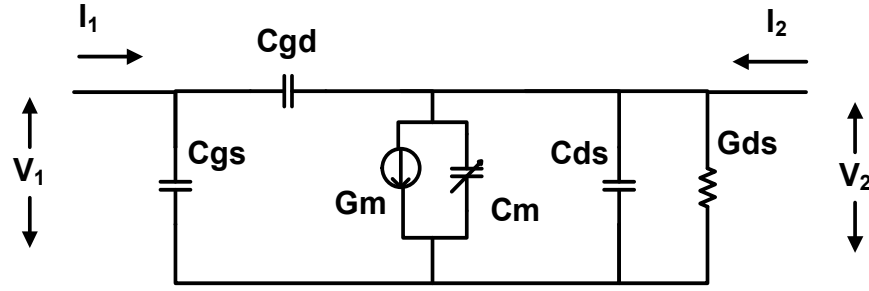


Figure 5-29: Intrinsic transistor modelled by Y-parameter coefficients.

At the input port,

$$I_1 = Y_{F,1}V_1 + Y_{S,1}V_2 + Y_{T,1}V_2^* + Y_{FSq,1}^2 + Y_{SSq,1}^2V_2^2 + Y_{TSq,1}^2V_2^{*2} \quad (5-48)$$

$$Y_{F,1} = y_{11} = j\omega(C_{gs} + C_{gd}) \quad (5-49)$$

$$Y_{S,1} = y_{12} = -j\omega C_{gd} \quad (5-50)$$

Notice how all the Port 1 coefficients from Fig. 5-27(a)-(f) have a real component that is essentially zero. This is because R_{gs} has been de-embedded in order to present a true Y configuration. The measured results indicate that the higher order coefficients such as $Y_{T,1}$ and $Y_{SSq,1}$ are dominated by non-linear capacitive mixing.

At the output port,

$$I_2 = Y_{F,2}V_1 + Y_{S,2}V_2 + Y_{T,2}V_2^* + Y_{FSq,2}^2 + Y_{SSq,2}^2V_2^2 + Y_{TSq,2}^2V_2^{*2} \quad (5-51)$$

$$Y_{F,2} = y_{21} = g_m - j\omega C_m + j\omega C_{gd} \quad (5-52)$$

$$Y_{S,2} = y_{22} = g_{ds} - j\omega C_{gd} + j\omega C_{ds} \quad (5-53)$$

For the output port, the results confirm that g_m dominates hence the higher order coefficients from Fig. 5-28(a)-(f) are dominated by non-linear resistive mixing. C_m represents the nonlinear transcapacitance present in the device.

With 6 coefficients, the current response, $I_{p,h}$ can now be modelled by the Cardiff Model equation in the admittance domain as shown in (5-54).

$$I_{p,h} = P_1^h \left\{ \begin{array}{l} Y_{Fp,h} + Y_{Sp,h} |V_{2,1}| \left(\frac{Q_1}{P_1}\right) + Y_{Tp,h} |V_{2,1}| \left(\frac{Q_1}{P_1}\right)^{-1} \\ + Y_{Fsqp,h} |V_{2,1}|^2 + Y_{Ssqp,h} |V_{2,1}|^2 \left(\frac{Q_1}{P_1}\right)^2 + Y_{Tsqp,h} |V_{2,1}|^2 \left(\frac{Q_1}{P_1}\right)^{-2} \end{array} \right\} \quad (5-54)$$

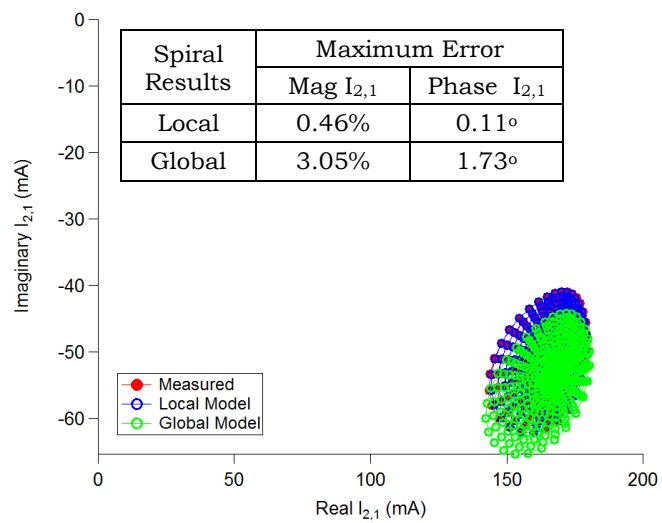
where $Q_1 = \angle V_{2,1} = V_{2,1} / |V_{2,1}|$ and $P_1 = \angle V_{1,1} = V_{1,1} / |V_{1,1}|$. Note that P_1 was set to zero in the experiments to simplify the equation. Since the Y-parameters have been proven to have the form $Y = G + j\omega C$, equation (5-54) becomes (5-55) and thus can be scaled with frequency.

$$I_{p,h}(\omega) = P_1^h \left\{ \begin{array}{l} \{G_{Fp,h} + j\omega C_{Fp,h}\} + \\ \{G_{Sp,h} + j\omega C_{Sp,h}\} |V_{2,1}| \left(\frac{Q_1}{P_1}\right) + \\ \{G_{Tp,h} + j\omega C_{Tp,h}\} |V_{2,1}| \left(\frac{Q_1}{P_1}\right)^{-1} + \\ \{G_{Fsqp,h} + j\omega C_{Fsqp,h}\} |V_{2,1}|^2 \\ \{G_{Ssqp,h} + j\omega C_{Ssqp,h}\} |V_{2,1}|^2 \left(\frac{Q_1}{P_1}\right)^2 \\ \{G_{Tsqp,h} + j\omega C_{Tsqp,h}\} |V_{2,1}|^2 \left(\frac{Q_1}{P_1}\right)^{-2} \end{array} \right\} \quad (5-55)$$

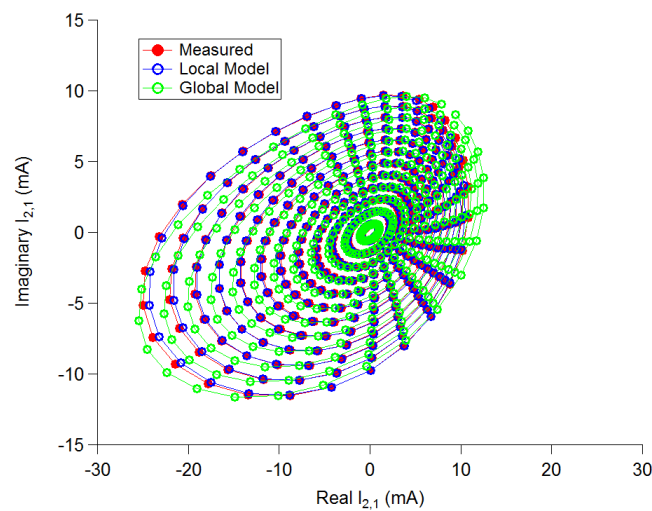
5.5.3 Model Results at Frequencies used in Extraction Process

From Fig. 5-27 and 5-28, it is clear that there are deviations between the local model and the global model especially for the higher order coefficient terms. This naturally occurs due to measurement inaccuracies and difficulty in

extracting very small coefficient values. From the graphs, the worst case scenario occurs at the high drive power levels. This may be an indication of the difficulty of maintaining a fixed large signal operating point, LSOP, while varying the frequency. Factors affecting the LSOP which are presently not fully controlled include temperature (already discussed in chapter 3) and waveform shape (only limited harmonic source and load-pull was used in this investigation).



(a)



(b)

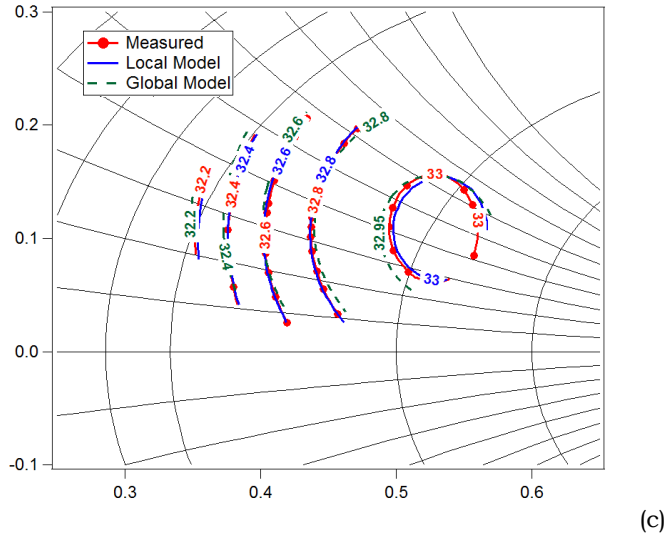


Figure 5-30: Measured and modelled results for 2x200 μm GaN on SiC transistor at 2 GHz (a) $I_{2,1}(Q)$ results (b) $I_{2,1}(Q)$ results without Y_F coefficient (c) Output power contours (in dBm).

The measured, local and global model $I_{2,1}$ and P_{out} contour results at 2 GHz for the high $V_{1,1}$ drive (set as 2.8 V in the ADS simulation) is plotted in Fig. 5-30(a)-(c). Results are also obtained for 4GHz and plotted in Fig. 5-31(a)-(c). For the sake of brevity, 8 GHz results are plotted in Appendix B.2.

From the results, the global model shows a slight shift in the centre of the results. To show that the shift is mainly due to the Y_F term, the results are also plotted with Y_F term contribution removed so that it is centred at (0,0). This highlights that any errors due to the higher order terms such as Y_S and Y_T , which govern the shape of the loops, are very small.

Nevertheless, even with the shift of Y_F , the global model for $I_{2,1}$ at frequencies used in extraction process is less than 3.05 % error in the magnitude and a 1.73 degree error in phase, indicating that the errors are all within the measurement tolerance. Over the measured range, the maximum P_{out} error is within 0.18 dB.

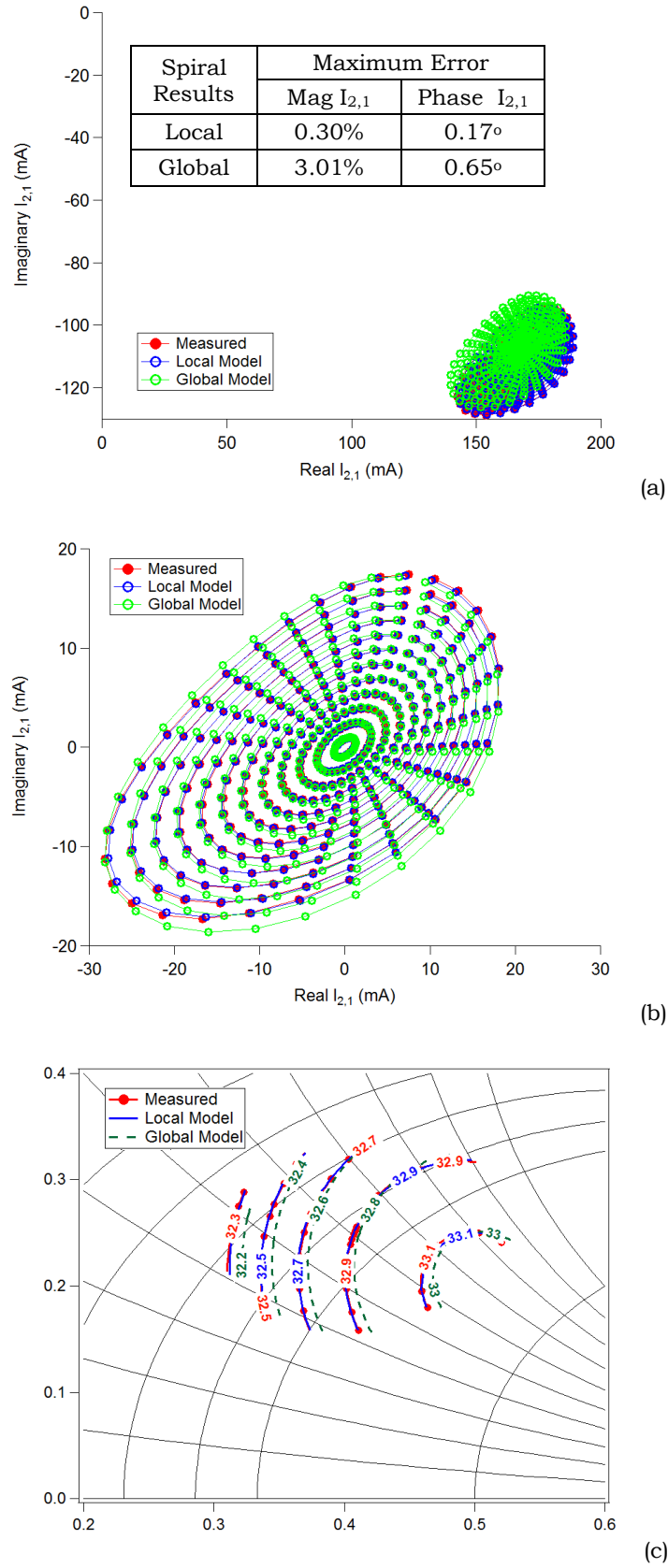


Figure 5-31: Measured and modelled results for 2x200 μm GaN on SiC transistor at 4 GHz (a) $I_{2,1}(Q)$ results (b) $I_{2,1}(Q)$ results without Y_F coefficient (c) Output power contours (in dBm).

Do note that the contours are not covering the 3 dB space in terms of P_{out} because the voltage stimulus can only cover a limited area of the measured load-pull space. However, once the model formulation has been established, model extraction can be switched to the Least Mean Squared approach. Data can now be in an unstructured form which covers the entire 3 dB load-pull measurement space and this will be shown in Section 5.6.

Note that using LMS cannot take place without prior knowledge of the model coefficients (number of terms and complexity) required to represent the data accurately. Only by performing the voltage load-pull and FFT can the model coefficients required be identified. As shown in Section 5.5.1, in this work, 6 coefficients is sufficient to model the data accurately.

5.5.4 Model Results at Interpolated Frequencies

By having a global model, it can now be used to predict load-pull behaviour at frequencies not used in the extraction process. Results of $I_{2,1}$ and P_{out} contours at 5 GHz and 6 GHz for the high drive ($V_{1,1} = 2.8$ V) are plotted in Fig 5-32(a)-(c) and Fig. 5-33(a)-(c) respectively. Modelled results confirm that the model is indeed scalable with frequency and in agreement with the measured performance.

The errors at 6 GHz is much larger due to the deviation of the coefficients from the global curve-fit as can be seen from Fig. 5-28(a)-(f). Nonetheless, the predicted results is still within a maximum of 5.50% for magnitude and 3.0 degrees for phase of $I_{2,1}$, well within any measurement uncertainties in the system. Results from the contours reveal that the load-pull P_{out} error is within 0.20 dB.

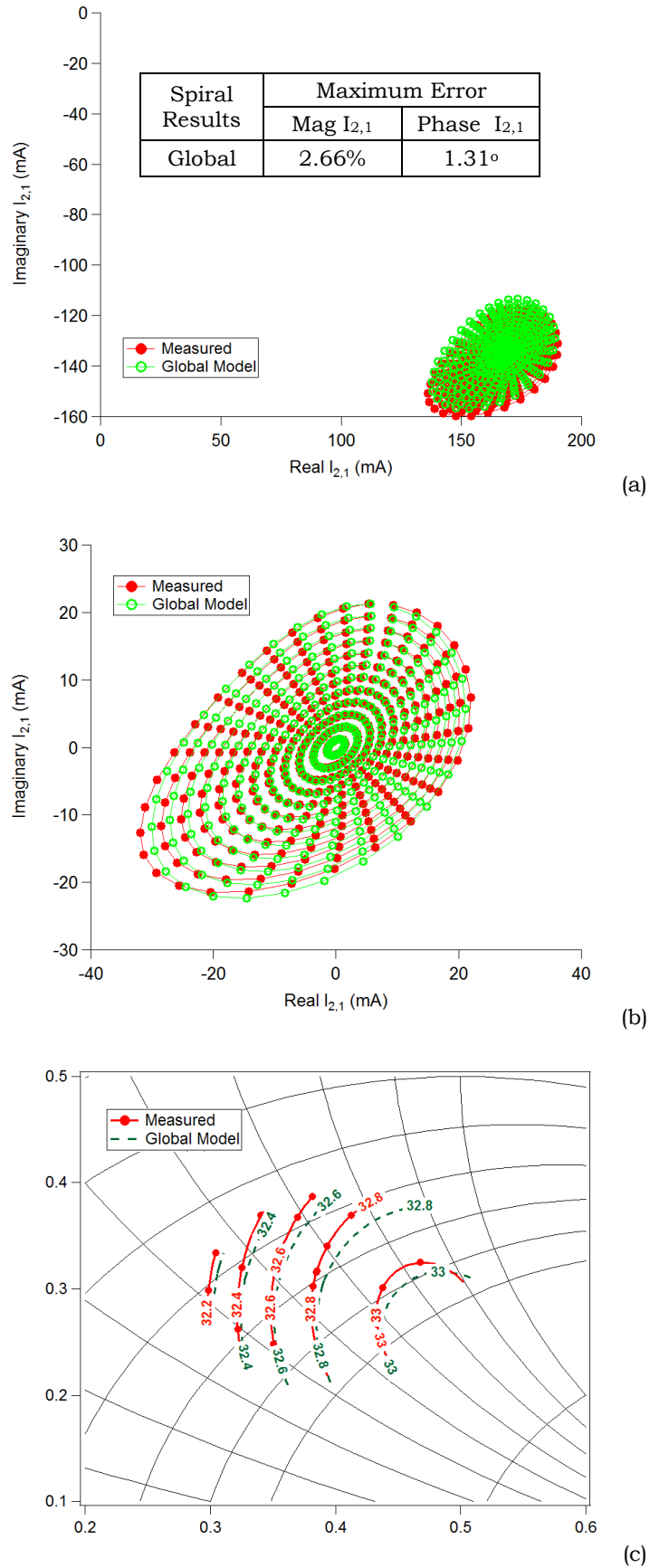


Figure 5-32: Measured and modelled results for 2x200 μm GaN on SiC transistor at 5 GHz (a) $I_{2,1}(Q)$ results (b) $I_{2,1}(Q)$ results without Y_F coefficient (c) Output power contours (in dBm).

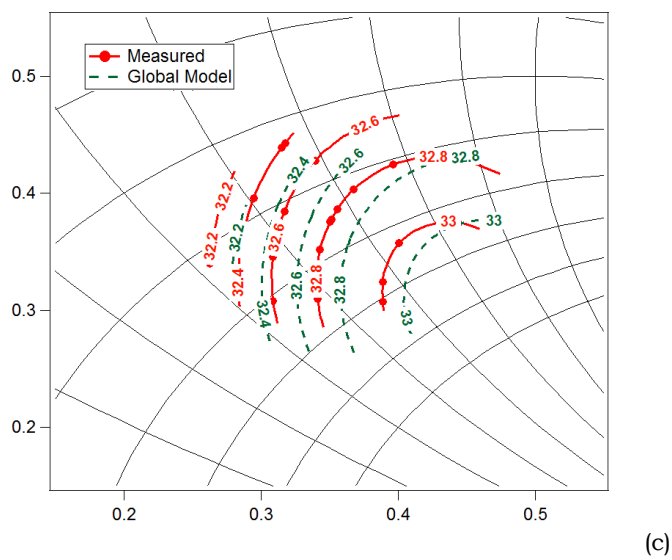
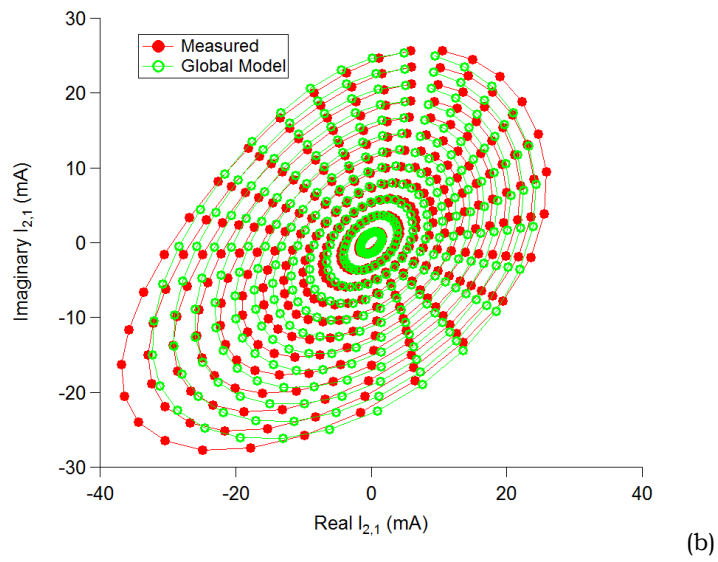
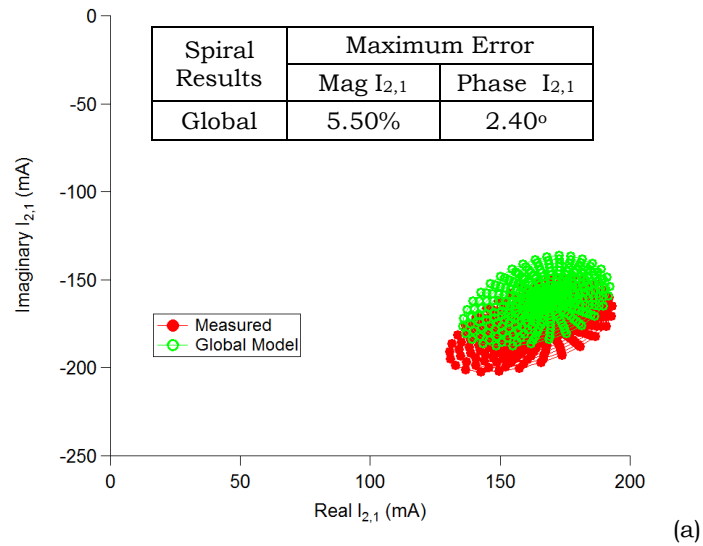


Figure 5-33: Measured and modelled results for 2x200 μm GaN on SiC transistor at 6 GHz (a) $I_{2,1}(Q)$ results (b) $I_{2,1}(Q)$ results without Y_F coefficient (c) Output power contours (in dBm).

5.6 Application of modelling concept to Least Mean Square extraction

5.6.1 Switching from FFT to LMS

So far the approach taken to extract the model coefficients has utilized engineered voltage stimuli and a Fast Fourier Transform concept. While this requires very complex stimuli it does allow the required model coefficients to be identified confirming the variation with perturbation stimulus, both magnitude and phase as well as with frequency. An alternative is to use Least Mean Square to obtain the coefficients instead of having to FFT each phase loop individually.

As can be seen from the results in Fig. 5-34(a)-(d), there is no difference between using FFT and LMS for the extraction process. The only constraint is that in this case the model structure needs to be defined in advance. However, the key advantage of this approach is that it does not required specifically engineered voltage stimuli but can be based on all the original measured load-pull points.

The current can be determined from the Y-parameters with voltage as the input,

$$I_{p,h} = Y_{p,h}^F + Y_{p,h,2,1}^S v_{2,1} + Y_{p,h,2,1}^T v_{2,1}^* + Y_{p,h,2,2}^S v_{2,2} + Y_{p,h,2,2}^T v_{2,2}^* \quad (5-56)$$

If multiple samples of points on this equation are taken:

$$\begin{aligned}
 & \begin{bmatrix} I_{p,h,0} \\ I_{p,h,1} \\ \vdots \\ I_{p,h,n} \end{bmatrix} \\
 &= \begin{bmatrix} Y_{p,h}^F + Y_{p,h,2,1}^S v_{2,1,0} + Y_{p,h,2,1}^T v_{2,1,0}^* + Y_{p,h,2,2}^S v_{2,2,0} + Y_{p,h,2,2}^T v_{2,2,0}^* \\ Y_{p,h}^F + Y_{p,h,2,1}^S v_{2,1,1} + Y_{p,h,2,1}^T v_{2,1,1}^* + Y_{p,h,2,2}^S v_{2,2,1} + Y_{p,h,2,2}^T v_{2,2,1}^* \\ \vdots \\ Y_{p,h}^F + Y_{p,h,2,1}^S v_{2,1,n} + Y_{p,h,2,1}^T v_{2,1,n}^* + Y_{p,h,2,2}^S v_{2,2,n} + Y_{p,h,2,2}^T v_{2,2,n}^* \end{bmatrix} \quad (5-57)
 \end{aligned}$$

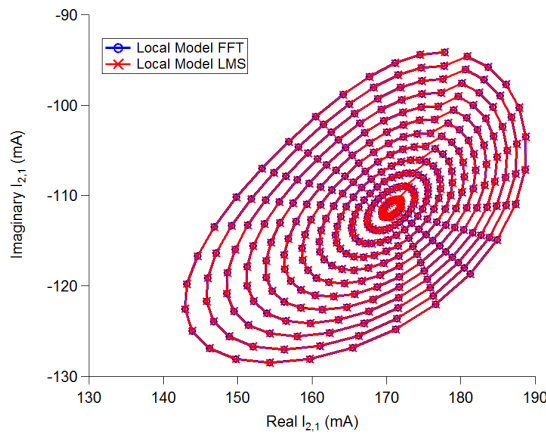
$$= \begin{bmatrix} 1 & v_{2,1,0} & v_{2,1,0}^* & v_{2,2,0} & v_{2,2,0}^* \\ 1 & v_{2,1,1} & v_{2,1,1}^* & v_{2,2,1} & v_{2,2,1}^* \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 1 & v_{2,1,n} & v_{2,1,n}^* & v_{2,2,n} & v_{2,2,n}^* \end{bmatrix} \begin{bmatrix} Y_{p,h}^F \\ Y_{p,h,2,1}^S \\ Y_{p,h,2,1}^T \\ Y_{p,h,2,2}^S \\ Y_{p,h,2,2}^T \end{bmatrix}$$

$$[I] = [V][Y] \quad (5-58)$$

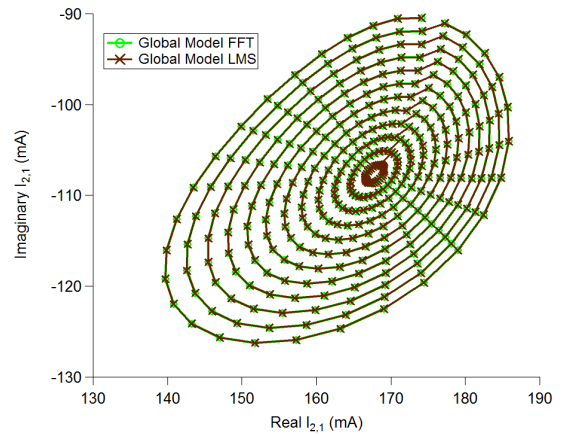
$$[V]^H [I] = [V]^H [V][Y] \quad (5-59)$$

$$[Y] = ([V]^H [V])^{-1} [V]^H [I] \quad (5-60)$$

The $[Y]$ in equation (5-60) represent the LMS extracted coefficients, Y-parameters which will be used to model the results. These, like in the case of the FFT, are curve-fitted over frequency to obtain a global model.



(a)



(b)

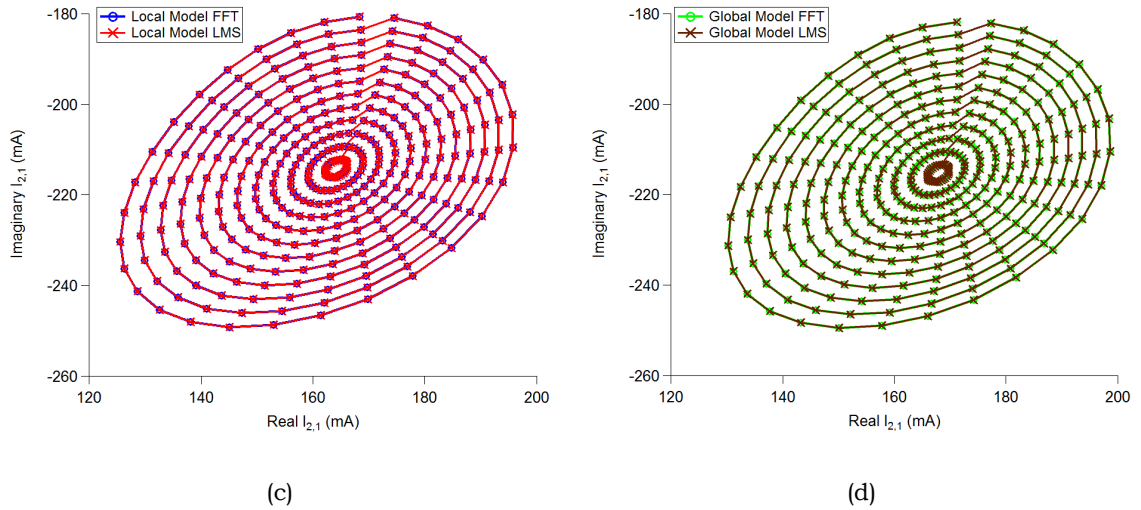


Figure 5-34: Comparison between FFT and LMS results of $I_{2,1}$ for 2x200 μm GaN on SiC transistor (a) Local model at 4 GHz (b) Global model at 4 GHz (c) Local model at 8 GHz (d) Global model at 8 GHz

5.6.2 Model Results at Frequencies used in Extraction Process

Now that the formulation and extraction procedure has been proven to be valid, LMS can be applied to the entire 3 dB load-pull space to extract a global model over frequency. Note that the results presented here will be at the same drive level in Section 5.5.

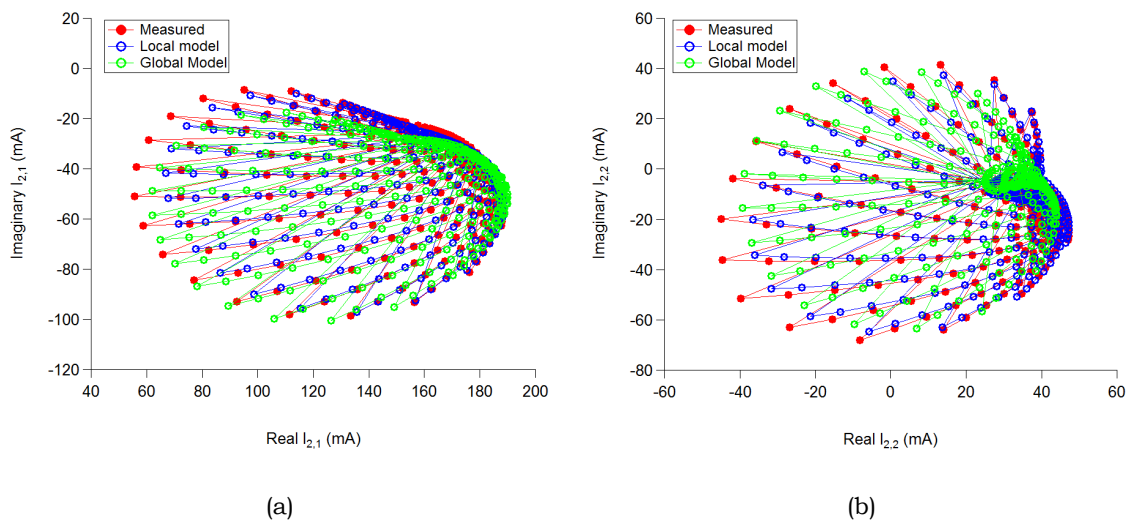


Figure 5-35: LMS results on load-pull data at 2 GHz for (a) $I_{2,1}$ (b) $I_{2,2}$

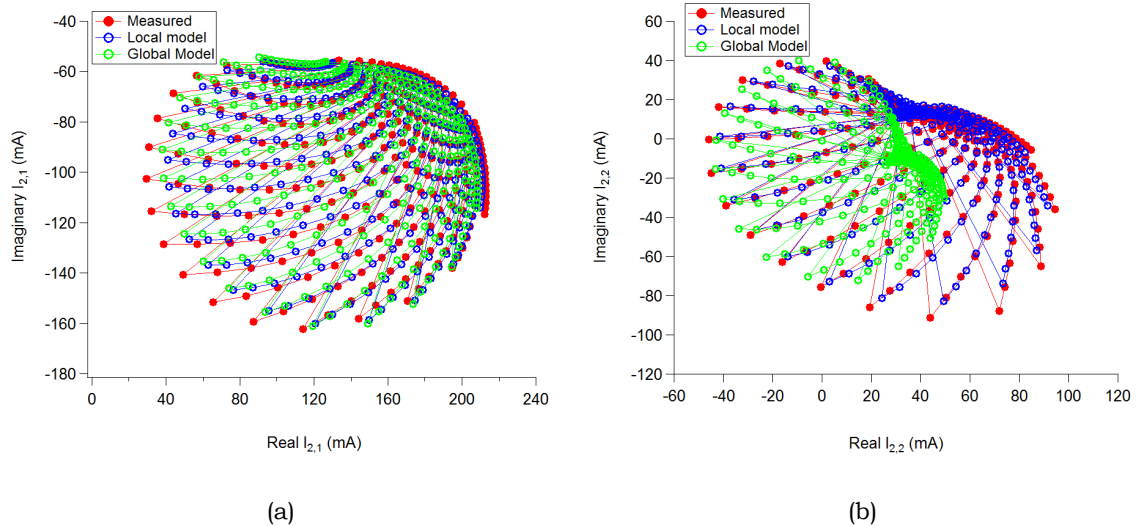
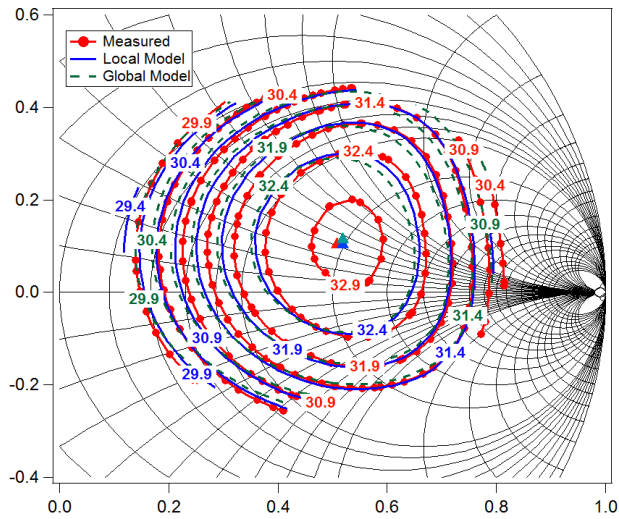


Figure 5-36: LMS results on load-pull data at 4 GHz for (a) $I_{2,1}$ (b) $I_{2,2}$

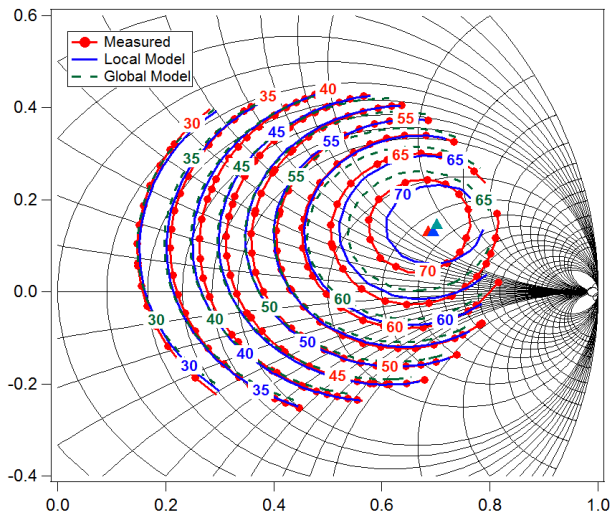
The plots of the $I_{2,1}$ and $I_{2,2}$ at 2 GHz and 4 GHz are plotted in Fig. 5-35(a)-(b) and Fig. 5-36(a)-(b) respectively. The P_{out} and Drain Efficiency contours as well as the Output current waveform at the optimum load for 2 GHz are shown in Fig. 5-37(a)-(c). The 3rd harmonic is not being controlled during measurements and so the output current waveforms is truncated to the 2nd harmonic. Fig. 5-38(a)-(c) are the contours and waveform (at the optimum load providing the best trade-off between P_{out} and Drain Efficiency) results at 4 GHz.

In the interest of being succinct, the results for 8 GHz will be plotted in Appendix B.3. From the load-pull results, it is clear that though the global model has an accuracy trade-off, it is still able to predict the optimum locations of the P_{out} and Drain Efficiency.



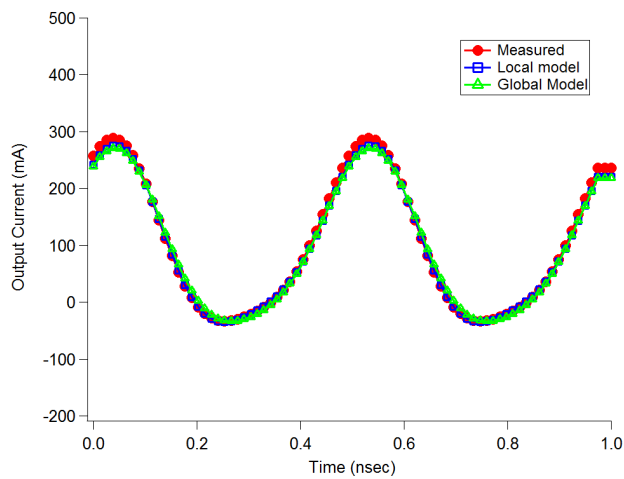
▲ Max Meas Pout: 33.02 dBm
 ▲ Max Local Model Pout: 32.90 dBm
 ▲ Max Global Model Pout: 32.87 dBm

(a)



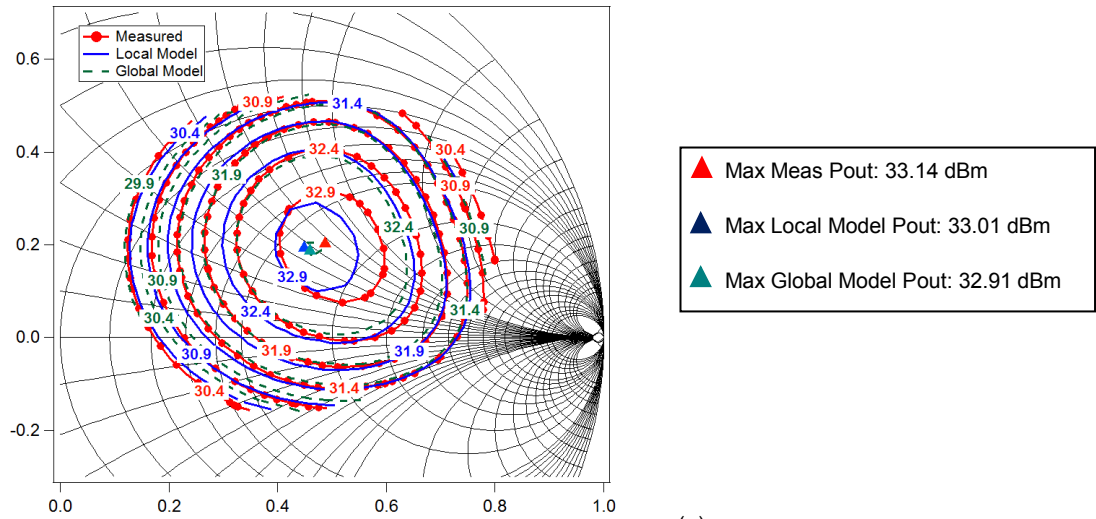
▲ Max Meas DEff: 72.99%
 ▲ Max Local Model DEff: 72.37%
 ▲ Max Global Model DEff: 69.90%

(b)

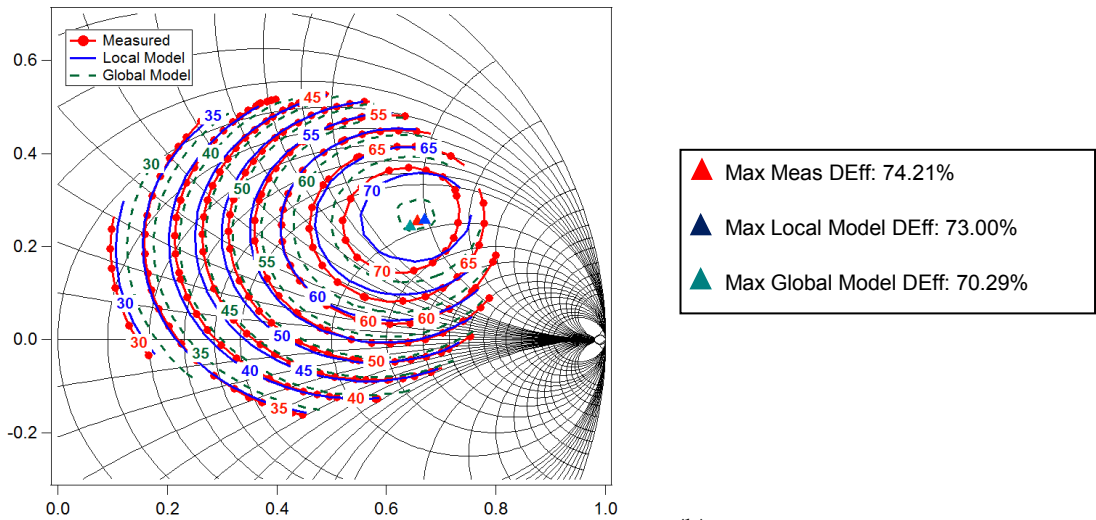


(c)

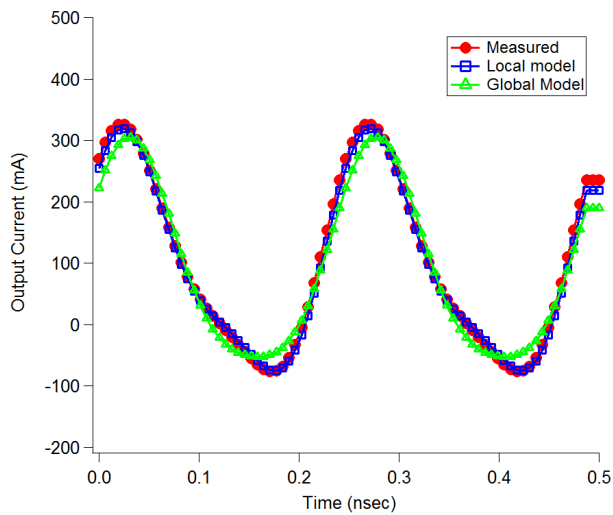
Figure 5-37: LMS results on load-pull data at 2 GHz for (a) P_{out} contour (b) Drain Efficiency contour (c) Output current waveform (at optimum load $\Gamma = 0.59 + j0.16$)



(a)



(b)



(c)

Figure 5-38: LMS results on load-pull data at 4 GHz for (a) P_{out} contour (b) Drain Efficiency contour (c) Output current waveform (at optimum load $\Gamma = 0.59 + j0.27$)

5.6.3 Model Results at Interpolated Frequencies

Just like in the FFT case, model coefficients extracted using LMS can be curve fitted and applied to predict results at frequencies that are not part of the extraction process. Here the coefficients are applied to 5 GHz and 6 GHz data to demonstrate that interpolation is possible for frequency scalable coefficients. The plots of the $I_{2,1}$ and $I_{2,2}$ at 5 GHz and 6 GHz are plotted in Fig. 5-39(a)-(b) and Fig. 5-40(a)-(b) respectively.

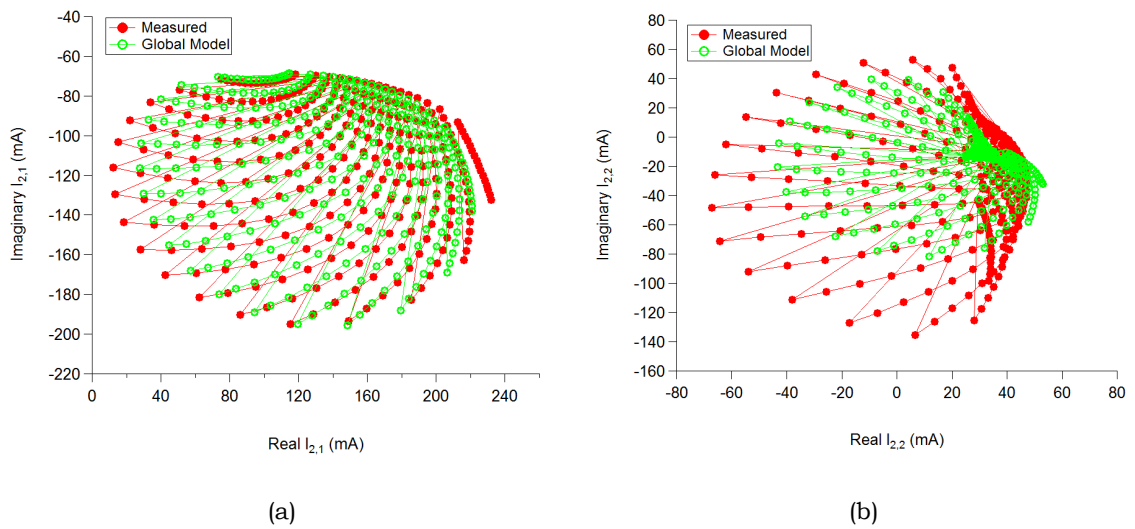


Figure 5-39: LMS results on load-pull data at 5 GHz for (a) $I_{2,1}$ (b) $I_{2,2}$

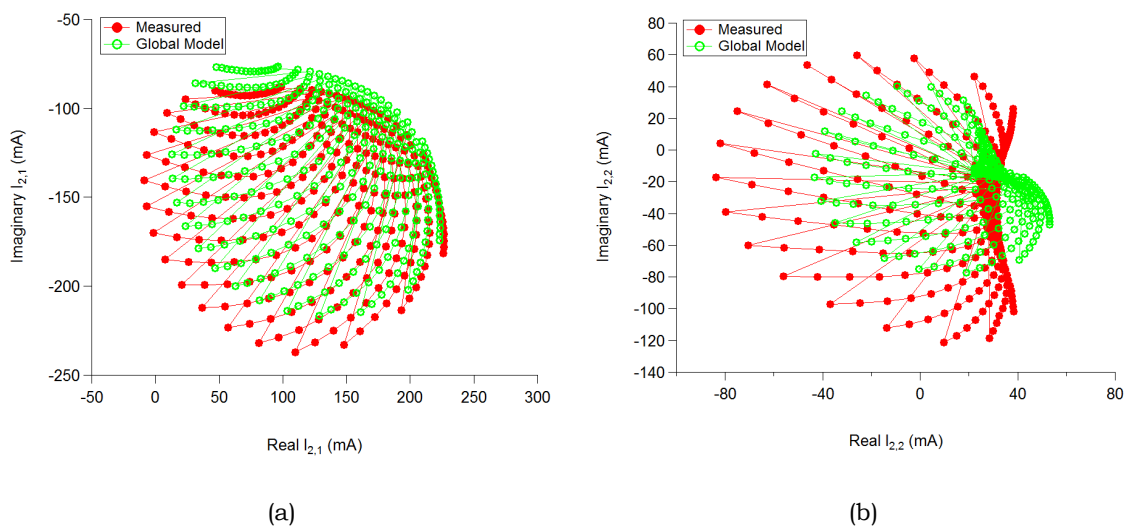
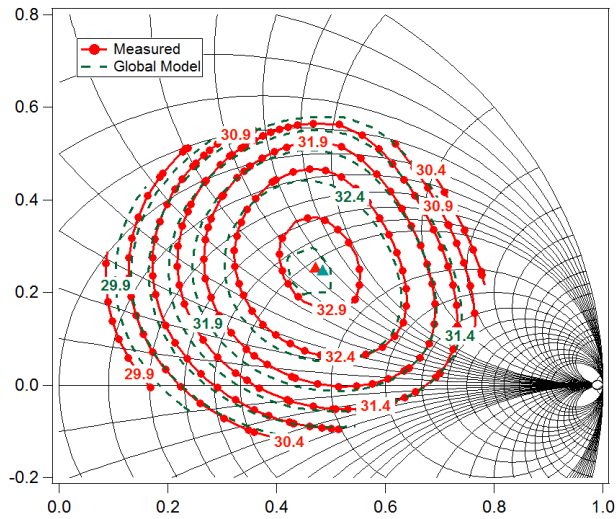
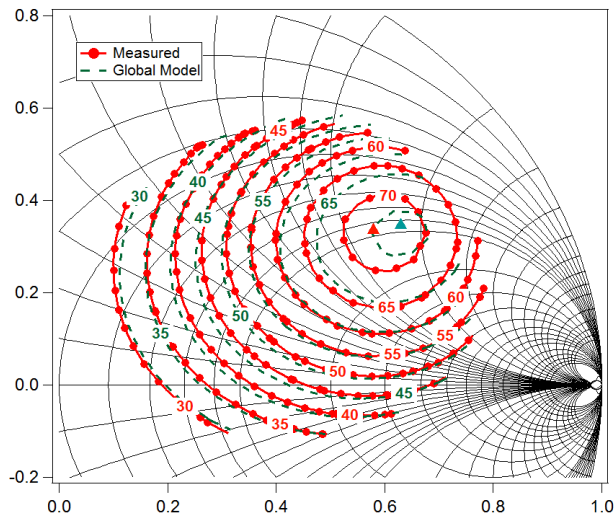


Figure 5-40: LMS results on load-pull data at 6 GHz for (a) $I_{2,1}$ (b) $I_{2,2}$



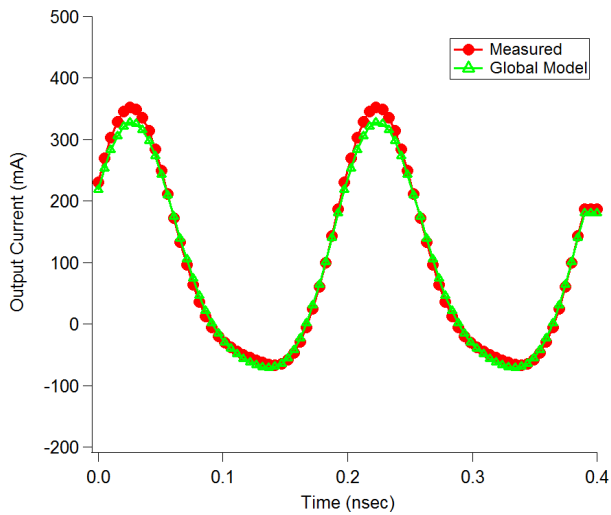
▲ Max Meas Pout: 33.05 dBm
 ▲ Max Global Model Pout: 32.93 dBm

(a)



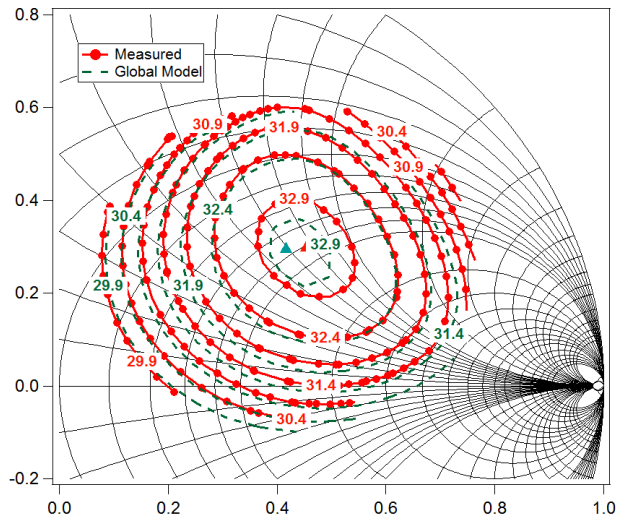
▲ Max Meas DEff: 71.98%
 ▲ Max Global Model DEff: 70.79%

(b)



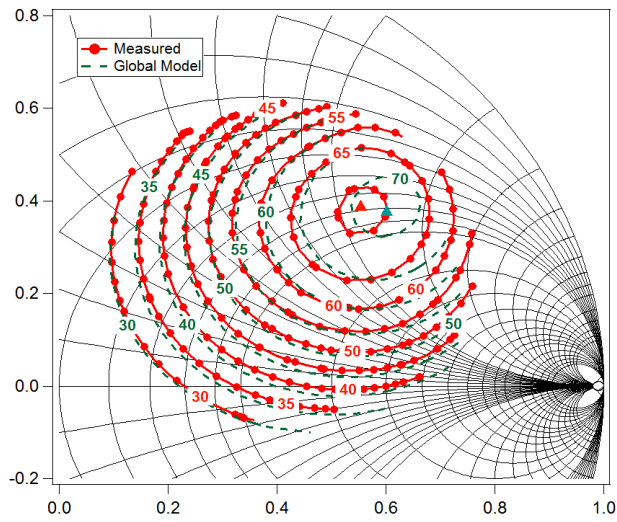
(c)

Figure 5-41: LMS results on load-pull data at 5 GHz for (a) P_{out} contour (b) Drain Efficiency contour (c) Output current waveform (at optimum load $\Gamma = 0.54 + j0.32$)



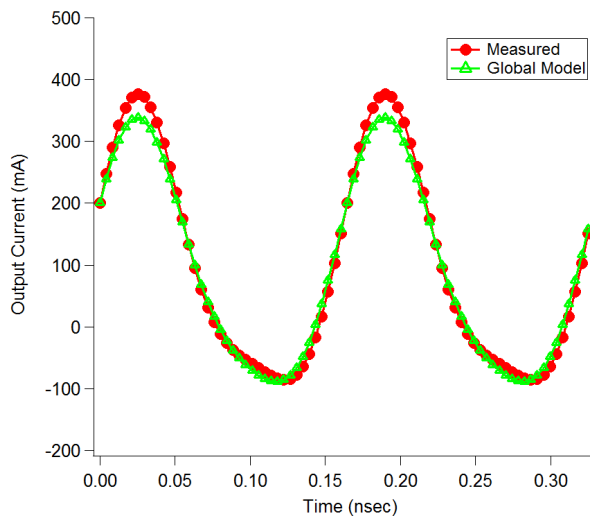
▲ Max Meas Pout: 33.11 dBm
 ▲ Max Global Model Pout: 32.96 dBm

(a)



▲ Max Meas DEff: 70.86%
 ▲ Max Global Model DEff: 71.23%

(b)



(c)

Figure 5-42: LMS results on load-pull data at 6 GHz for (a) P_{out} contour (b) Drain Efficiency contour (c) Output current waveform (at optimum load $\Gamma = 0.54 + j0.35$)

P_{out} and Drain Efficiency contours and the Output current waveform at the optimum load for 5 GHz are shown in Fig. 5-41(a)-(c). Contours and waveform plots for 6 GHz are shown in Fig. 5-42(a)-(c). This broadband model works over 2 octaves (from 2-8 GHz) and load-pull results show that it can predict the maximum P_{out} and Drain Efficiency values to within 0.23 dB and 4.0% respectively.

5.7 Discussion on Model at Extrapolated Frequencies

Since the global model uses a constant of $G_{pk,ql}^{(m)}$ and $C_{pk,ql}^{(m)}$ to provide for scaling with frequency, an extrapolation to other frequencies can also be carried out. An attempt was made to perform load-pull at 10 GHz but since the measurement system is based on an active load-pull, limitations in the power amplifier caused the measured load-pull area to be limited and not reach the edge of the Smith Chart as shown in Fig. 5-43. The similar situation has occurred as discussed in Section 3.6.2. This causes the load-pull results to be skewed and not suitable for model extraction.

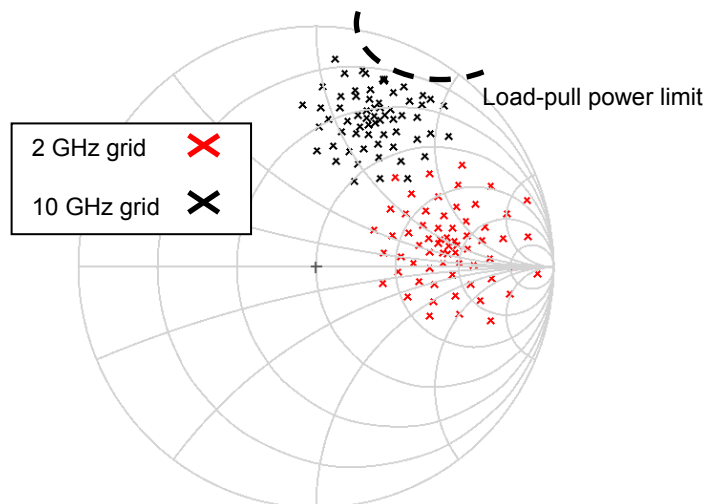


Figure 5-43: Measured load-pull points at 2 GHz and 10 GHz on the 2x200 μm GaN on SiC transistor

It is important to note that the measurements are not trivial as the same intrinsic transistor conditions must be held for at all frequencies used in the extraction process. Experimentally, it is a challenge to maintain the same I-V trajectory as frequency is increased.

It must be pointed out that the measurements were not carried out at much higher frequencies due to a hardware limitation of the amplifiers for the 2nd harmonic measurements (set to short on both input and output). The amplifier used in the measurement system setup is the GT1000A [13] that is limited to 20 GHz. Further work is necessary to test the limits of extrapolation in using this frequency scalable model.

Note from Section 5.2 that the model assumes a Y-parameter model with R_{gs} de-embedded from the intrinsic model. This inherently places a bandwidth limitation on the model and it is believed that the model will start to fail when the topology modification used results in the small-signal results becoming inaccurate, which is at a much higher frequency. This is the very reason that a small-signal validation is necessary at the beginning of the model formulation.

5.8 Summary

An important outcome of this chapter is the first demonstration that non-linear Behavioural transistor models can be mathematically described in a manner that allows for frequency scalability.

By referencing the intrinsic transistor in the admittance domain and applying voltage load-pull, the Y-parameters that form the Behavioural model can be investigated and extracted. These parameters have been shown to be frequency independent with experimental results on 2 separate GaN HFETs, both measured from 2 - 8 GHz (over 2 octaves).

Experimental results also show that they can successfully predict results at frequencies that are not used during the measurement based model extraction process. This saves a significant amount of time for data collection and reduces the burden placed on the measurement system to measure each frequency iteration for a broadband Behavioural model.

FFT approach was first used in the extraction process to establish the model complexity that would be needed to represent the data. Model coefficients have been proven to be frequency independent using X-Parameters (3 coefficient formulation) and when extended to the Cardiff Model (6 coefficient formulation). Once that has been done, LMS extraction approach can be applied to the measured data with confidence that it will fully represent the data without loss in accuracy. Results show that there is no difference between using FFT or LMS for the extraction process.

Investigation of the extrapolation capability was limited due to hardware restrictions and this can be a topic for future work. This model can also be extended for harmonic source and load-pull by including perturbations in the 2nd and 3rd harmonics in future research.

5.9 References

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CHAPTER 6

CONCLUSIONS & FUTURE WORK

The research in this PhD has successfully achieved its goal of extending the functionality of Behavioural Models by investigating and successfully proving, scaling in terms of geometry (size of transistor) and frequency. These two degrees of design freedom, once thought to be limited to only Physical and Compact Models, can now be applied to Behavioural Models, making it a viable MMIC design tool.

6.1 Conclusions

From the literature review in Chapter 2, geometric scaling had been proven but only for X-parameters [1]-[2]. Therefore, in Chapter 3, this PhD work extends the research into this subject by applying the concept to a general Behavioural model formulation (Cardiff Model). Geometric scalable Behavioural models were generated by combining measurement data look-up table models of a reference (smaller) transistor with the required passive layout networks.

The modelling process and framework which includes 4 main steps have been developed and verified through experimental results. The steps are: determining the intrinsic plane of the reference transistor, obtaining the large signal measurement data for conversion into Behavioural models, performing scaling at the intrinsic plane and embedding with the passive circuit of the scaled device.

Obtaining the right parasitic values is a vital modelling step since scaling rules apply only to the intrinsic portion of the transistor. These component values, extracted from Cold FET measurements of several transistors with varying gate width and number of fingers, have been validated by comparing small-signal measurements with ADS simulations.

Active load-pull measurements were performed with varying fundamental load and a fixed 2nd harmonic to extract a 6 coefficient Behavioural Model. Chapter 3 has also presented the extraction formula for the model coefficients and the confirmation that 6 coefficients are sufficient to model the measurements of fundamental load-pull accurately. A discussion on the practical considerations when generating the Behavioural model which involves extracting the reference model at the extrinsic plane to avoid re-gridding of the data has also been presented.

Large signal validations of scaling were performed using ADS so that the measured and modelled values can be generated from the same input incident power. The ADS circuit uses an FDD block to read the file containing the model coefficients, ABCD blocks to enforce scaling as well as "negative" and "positive" components to perform the de-embedding and embedding respectively.

The B waves, waveforms, power sweep and load-pull results successfully demonstrate geometric scaling up to a scaling factor of 5 for 2 different GaN wafers, one measured at 5 GHz and another at 9 GHz. This process is robust as it also is able to extrapolate beyond the measurement power limitations of the active load-pull system, thus granting the ability to design high power

MMICs without having to measure the transistors at an extremely high power level in order to generate a model.

Chapter 4 presents the utilization of the geometric scalable model in MMIC design where a prototype single cell amplifier is matched for operation at 5 GHz. Although the targeted performance was not achieved due to mismatch in the fabricated circuit, the non-linear Behavioural model is still able to predict the measured results when the measured S-parameters of the realized matching circuits were placed into the simulator. This demonstrates that the scalable non-linear Behavioural model can be used for MMIC design and predict the performance of the actual fabricated circuit.

In Chapter 5, the novelty of this research is solidified by demonstrating for the first time that non-linear Behavioural transistor models have coefficients which are frequency scalable.

By referencing the intrinsic transistor in the admittance domain and applying voltage load-pull, the Y-parameters of the Behavioural model can be extracted and have the form $Y = G + j\omega C$, which can scale with frequency. This condition has been proven through experimental results on 2 separate GaN HFETs, both measured from 2 - 8 GHz (over 2 octaves, covering the S and C bands).

In order to determine the model complexity required to sufficiently model the data, FFT approach was first applied in the extraction process. Model coefficients have been proven to be frequency independent using X-Parameters (3 coefficient formulation) and was extended to the Cardiff Model (6 coefficient formulation) to include a larger perturbation space. Once the model complexity has been determined, the research is taken a step further by applying the LMS extraction approach to model the entire 3 dB load-pull space. Note that the

LMS approach can only be applied to the measured data with confidence once the model complexity is known.

Though there is an accuracy trade-off when choosing a global model (which represents the entire frequency range), experimental results show that the broadband model can accurately reproduce data at frequencies used in the extraction process as well as predict results at other frequencies.

One major advantage of Behavioural models over other model types is the speed in which it can be produced. However, the time saved in terms of model generation is traded off with the limitation that the model can only represent conditions at which the measurements were performed. In other words, a major conundrum limiting the use of Behavioural models is its inability to scale. To have a comprehensive model, measurements must be performed for every single device periphery, frequency, bias and temperature which will cause the number of measurements to exponentially increase to an impractical value.

In this research, by successfully proving the modelling framework for scaling in terms of geometry and frequency, Behavioural models can now be used to predict results (at device sizes and frequencies) outside its extraction range. This substantially reduces the number of measurements that need to be performed, saving precious time and effort. Depending on the model coverage and speed of the measurement system, several weeks of measurements to obtain a geometrically scalable, broadband model can now be accomplished in only a few days.

Furthermore, the burden placed on hardware availability is also reduced. Previously, in order to obtain a model at a particular power level or frequency,

the measurement system must be able to measure the transistor operating in the said condition. For example, in order to model a transistor operating at 50 W, the high power setup must contain sources, bias tees and tuners (passive load-pull) / amplifiers (active load-pull) that can perform this measurement. The same is true if a transistor is to be characterized over several frequency bands of operation. In addition, hardware that can handle both high levels of power and frequency of operation are extremely rare and expensive.

Besides the increased cost in hardware, the measurement setup also becomes more complex. All these disadvantages are solved with the implementation of scaling in the models. From this research, Behavioural models can now be extracted in a manner similar to Compact models where characterization is performed at a nominal cell size and frequency and used to predict results at other cell sizes and frequencies.

6.2 Future Work

In Chapter 3, the passive circuit was determined using the Cold FET extraction process and represented with lumped elements in the ADS simulations. While it is sufficiently accurate for this work, the parasitics can be represented with greater accuracy by using EM simulations. This could be achieved by leveraging the work in [3] where a single finger FET model is combined with EM simulations to accurately model the transistor. Using EM simulations will enable the user to model complex structures surrounding the active portion of the transistor. This may include bond wires or other parasitics associated with the package of the device.

In Chapter 3, results from a scaling factor of 10 indicate that due to self-heating, the model accuracy has degraded and scaling is no longer valid. In

order to overcome this limitation, temperature needs to be taken into account or a smaller scaling factor should be used. Various attempts has been carried out to capture thermal effects for Compact models [4]-[5] and exploring the relationship of Behavioural model coefficients with temperature is another topic that can be explored in the future. Solving this issue will remove the dependency of temperature being a look-up parameter.

In Chapter 4, the prototype was designed with a new experimental IPD process where the input and output matching circuits were external to the active device and bond wires were used to complete the circuit. Besides limiting its frequency of operation, it also increases the possibility of fabrication uncertainty. Future work could include a 2nd design run with the entire circuit on a single substrate. A prototype with a higher output power and frequency of operation can also be designed.

In Chapter 5, in order to obtain a data with a constant V_{11} , the measurement data was first converted into a Behavioural model in the (B-A) domain and voltage load-pull was performed in ADS to satisfy the aforementioned condition. This is a long and complex extraction procedure to obtain Behavioural models in (I-V) domain which should be simplified in future research attempts.

Due to hardware limitations, the extrapolation limits of the frequency scalable model could not be fully explored in this work. A limitation in terms of bandwidth is bound to occur since the model uses a simple method of de-embedding R_{gs} in order to implement a true Y intrinsic model (described in Section 5.2.2). Measurements at higher frequencies must be carried out in order to determine the point where the model starts to breakdown. One

method of overcoming the bandwidth limitation is to implement linear delays to account for the quadratic frequency dependency of Y-parameters at high frequencies [6].

Note that results shown in this work were done with fundamental load-pull with a fixed 2nd harmonic. Now that geometric and frequency scaling for this dataset have been proven successful, measurements with 2nd and 3rd harmonic source and load-pull perturbations as described in [7]-[9] can now be performed to extend the capability of the scalable model.

Research into frequency scaling has recently been extended with the work in [10] where the frequency scalable model is generated from X-parameter data at a single fundamental frequency of 1 GHz. The model is obtained by computing the admittance space X-parameters (XY parameters) first using forward excitations, and then with the phase conjugate of these excitations.

This produces an exact periodically varying time-reversed Large Signal Operating Point to each of the forward conditions. At any one frequency, it is impossible to separate G and C terms from forward or reverse XY terms alone, but with a forward and time-reversed pair, these terms can be identified. Validation of the scalable intrinsic model shows good agreement from 100 MHz up to 50 GHz. Nevertheless, accuracy using the full model (with parasitics) is not as good as the intrinsic model but can be improved by denser sampling of the XY-parameter generation and this work is still in progress.

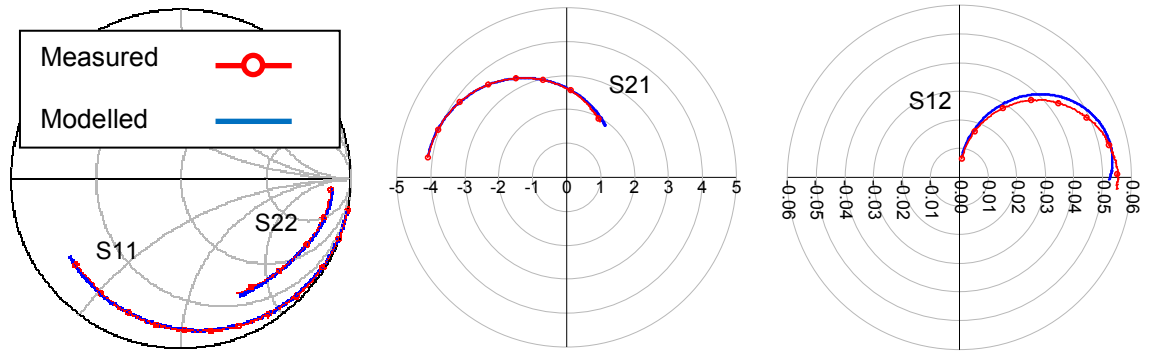
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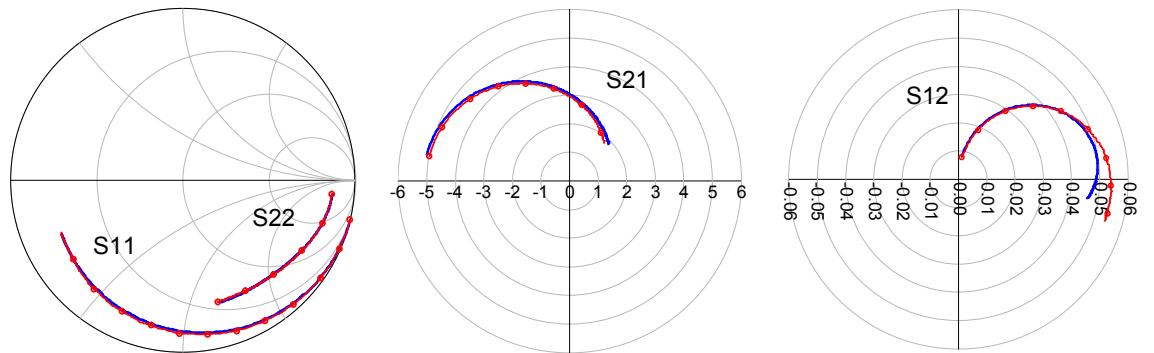
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APPENDIX A

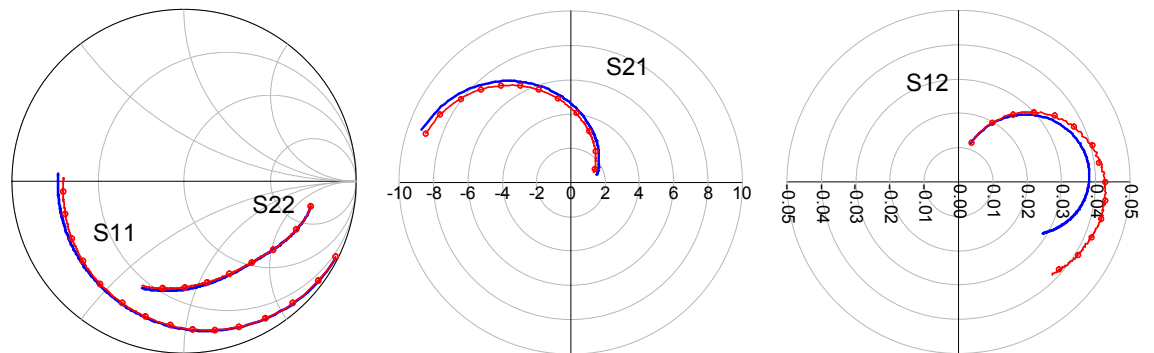
A.1 Small signal model verification at $I_d = 150 \text{ mA/mm}$



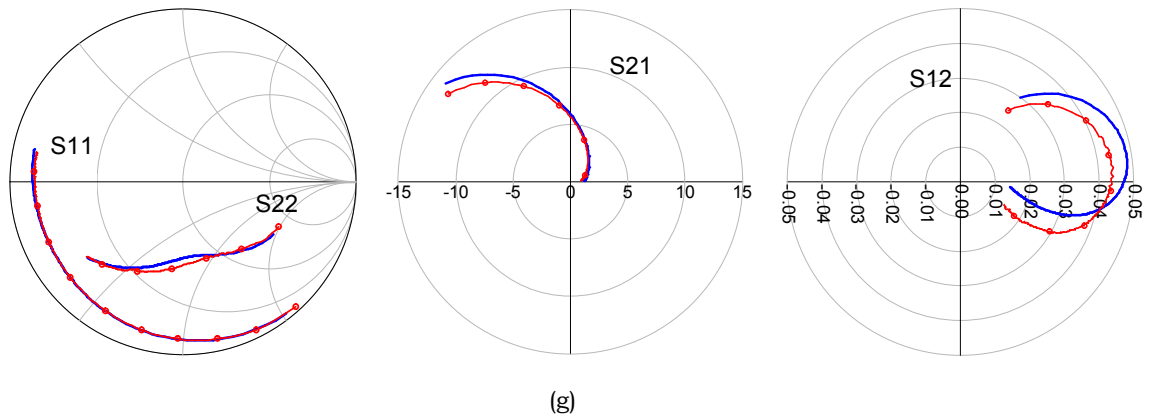
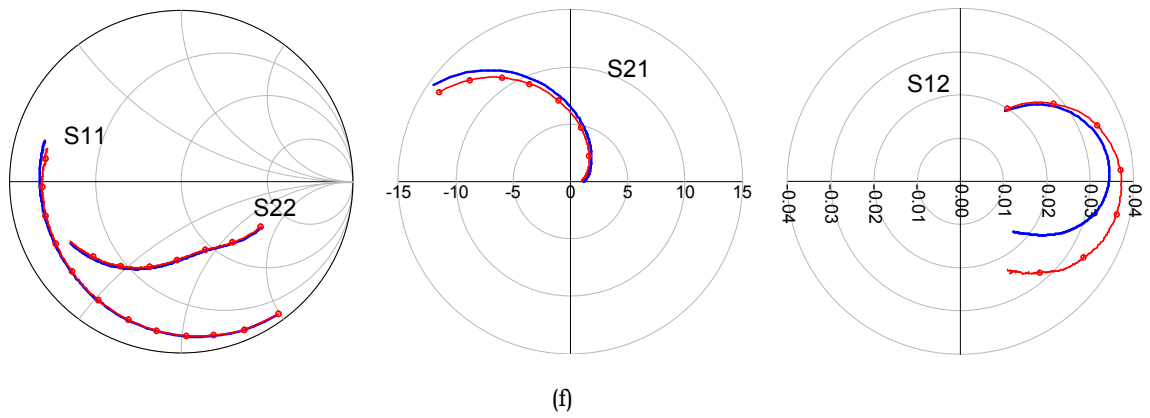
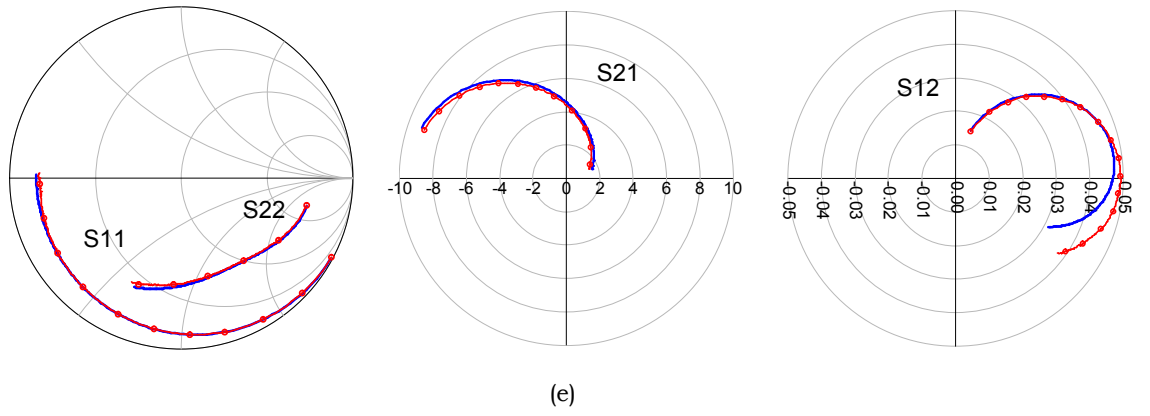
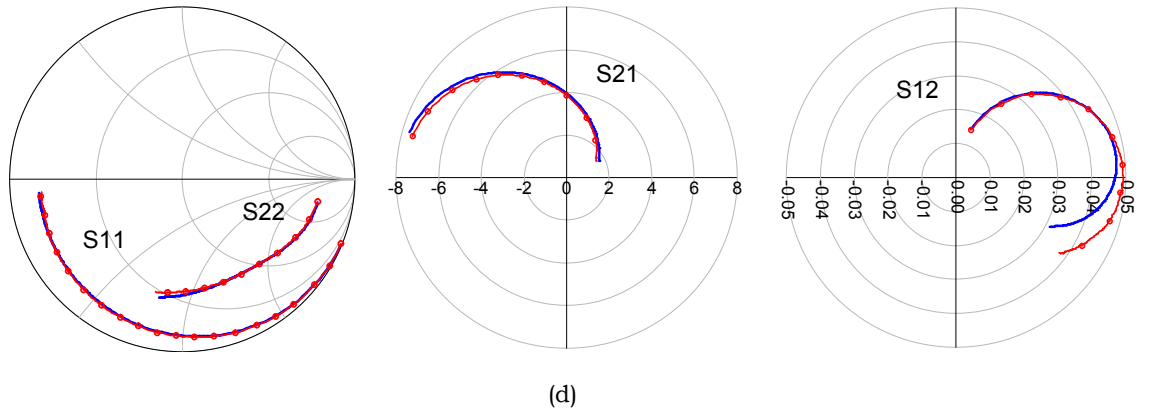
(a)



(b)



(c)



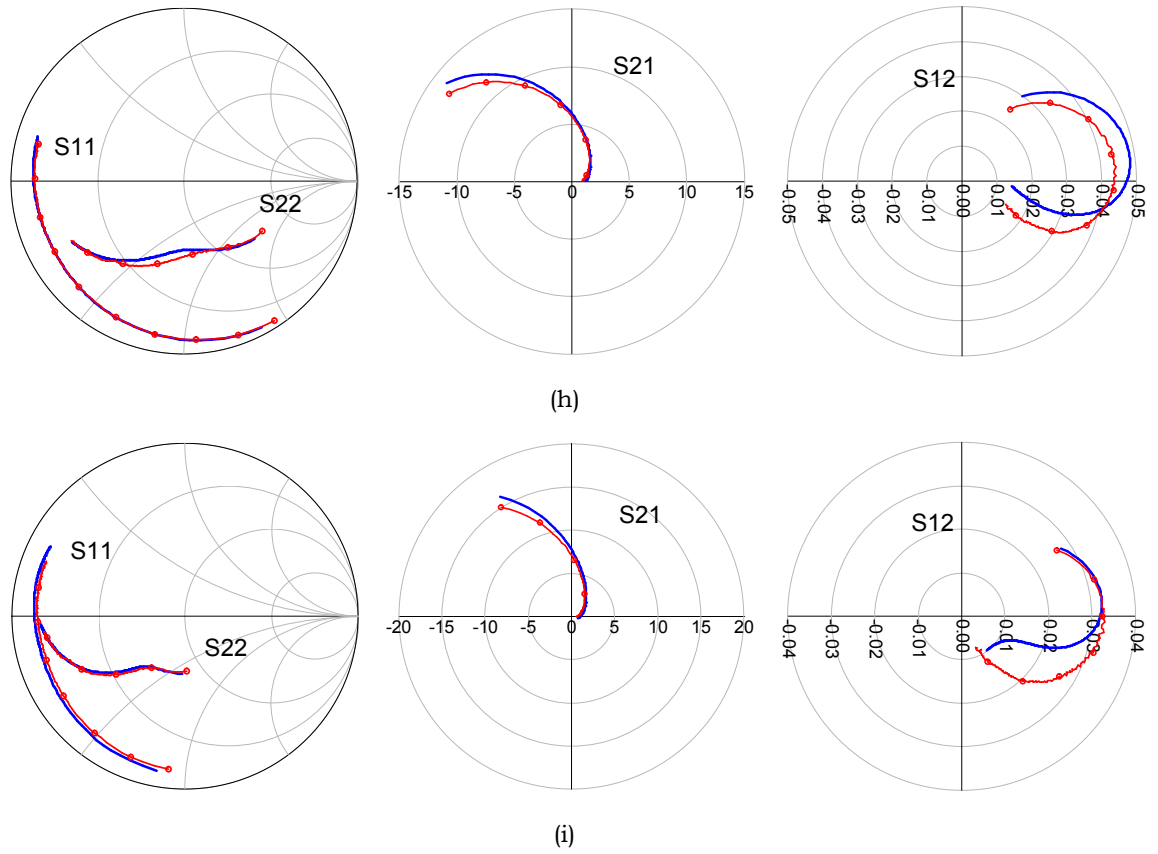
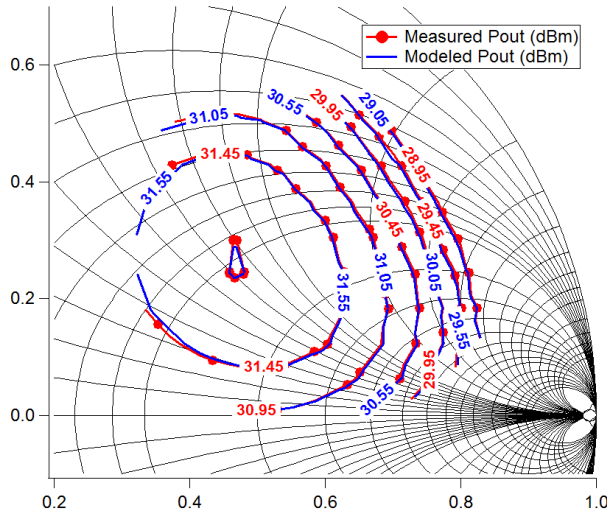


Figure A1-1: Measured versus modelled results of S-parameters from 1 - 20 GHz obtained at $I_d=150$ mA/mm. (a) 2×80 μm device (b) 2×100 μm device (c) 2×200 μm device (d) 4×80 μm device (e) 4×100 μm device (f) 4×200 μm device (g) 8×80 μm device (h) 8×100 μm device (i) 8×200 μm device

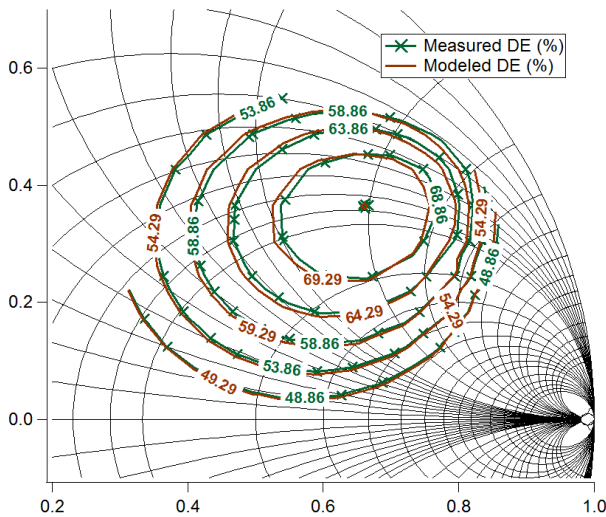
A.2 Scaling by factor of 2



Measured contours - in 0.5 dB steps from maximum of 31.95 dBm.

Modelled contours - in 0.5 dB steps from maximum of 32.05 dBm.

(a)



Measured contours - in 5 % steps from maximum of 73.86 %.

Modelled contours - in 5 % steps from maximum of 74.29 %.

(b)

Figure A2-1: Measured versus modelled P_{out} and Drain Efficiency contours for the $4 \times 80 \mu\text{m}$ device at a $P_{incident}$ of 21.72 dBm. (a) P_{out} contours (b) Drain Efficiency contours.

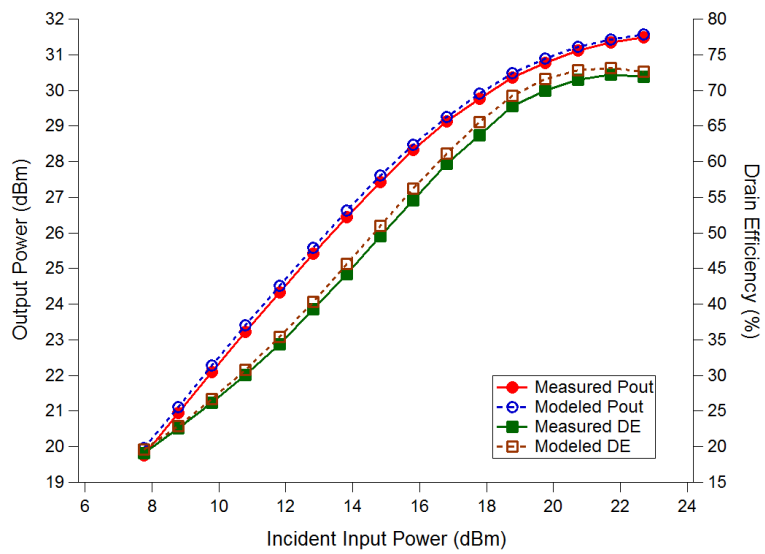


Figure A2-2: Measured versus modelled P_{out} and Drain Efficiency from power sweep at optimum load $\Gamma = 0.599 + j0.305$ for the $4 \times 80 \mu\text{m}$ device

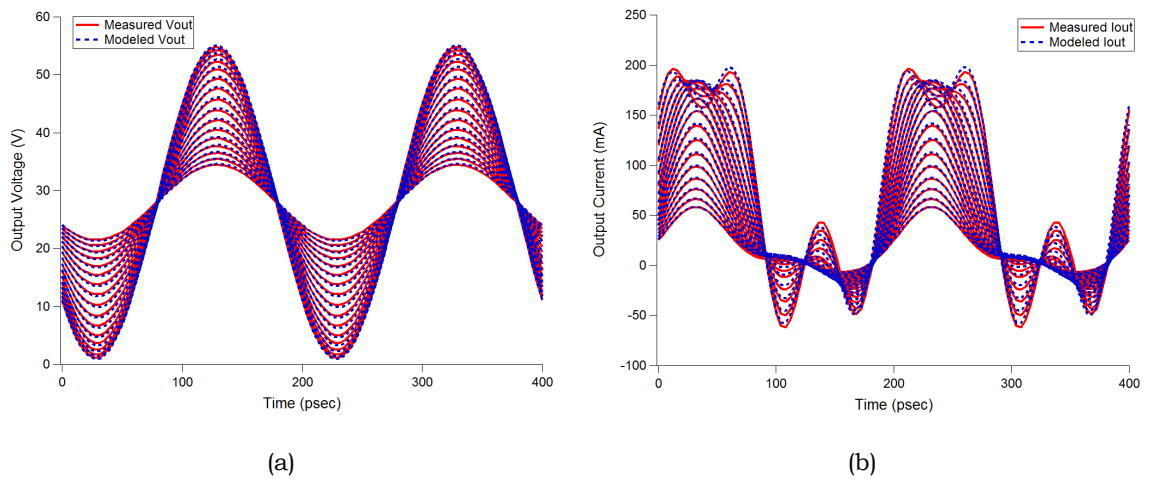
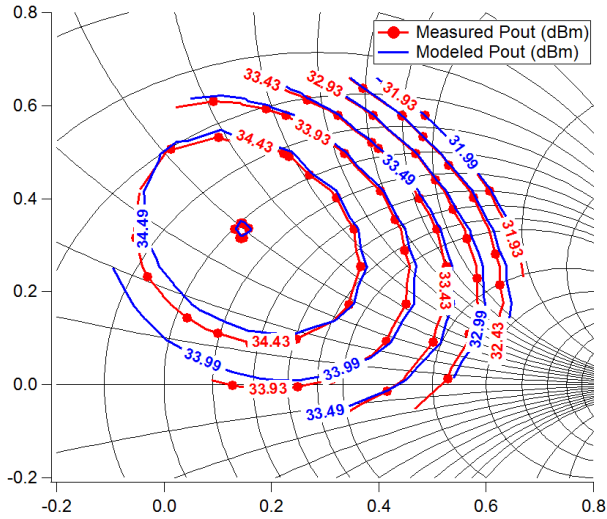


Figure A2-3: Measured versus modelled waveforms from power sweep at optimum load $\Gamma = 0.599 + j0.305$ for the $4 \times 80 \mu\text{m}$ device (a) Output voltage (b) Output current

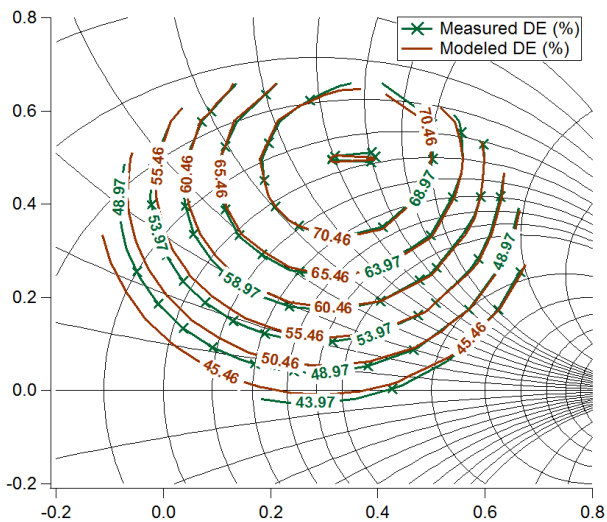
A.3 Scaling by factor of 4



Measured contours - in 0.5 dB steps from maximum of 34.93 dBm.

Modelled contours - in 0.5 dB steps from maximum of 34.99 dBm.

(a)



Measured contours - in 5 % steps from maximum of 73.97 %.

Modelled contours - in 5 % steps from maximum of 75.46 %.

(b)

Figure A3-1: Measured versus modelled P_{out} and Drain Efficiency contours for the $8 \times 80 \mu m$ device at a $P_{incident}$ of 25.26 dBm. (a) P_{out} contours (b) Drain Efficiency contours.

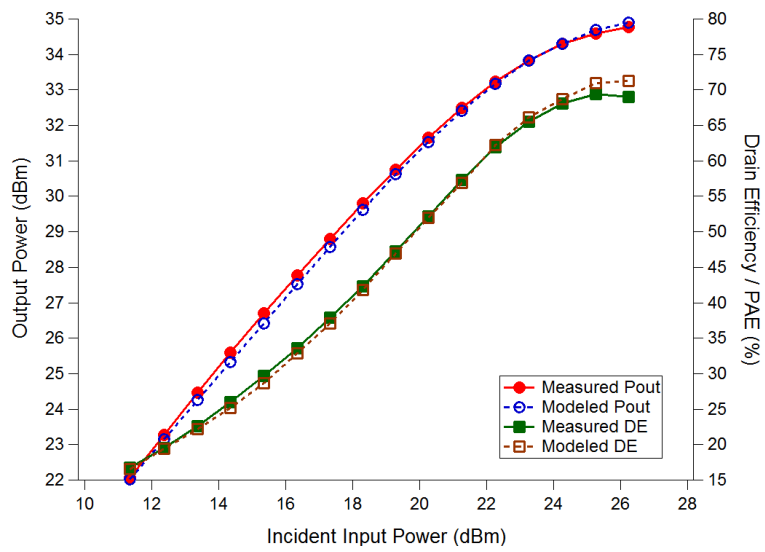


Figure A3-2: Measured versus modelled P_{out} and Drain Efficiency from power sweep at optimum load $\Gamma = 0.321 + j0.335$ for the $4 \times 80 \mu\text{m}$ device

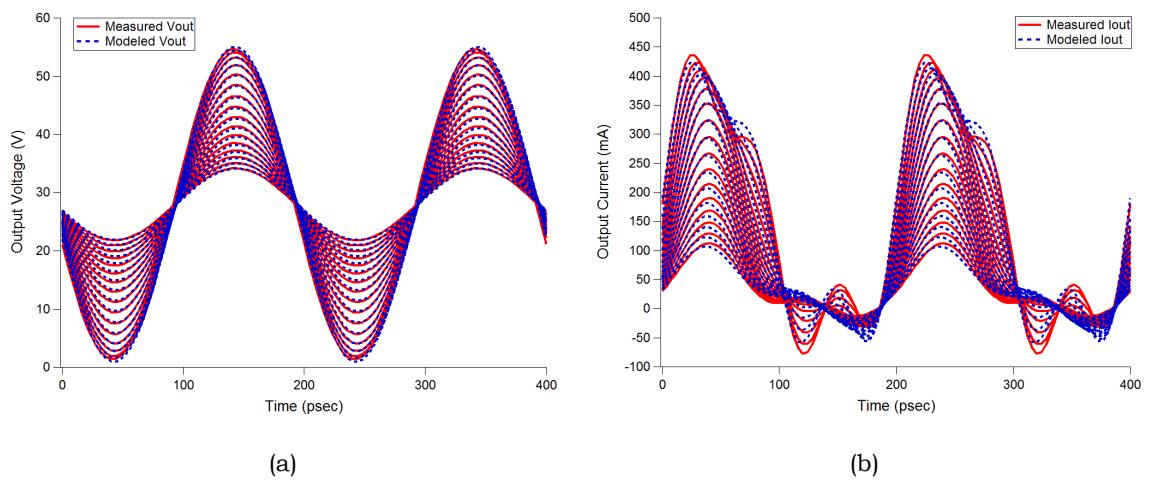
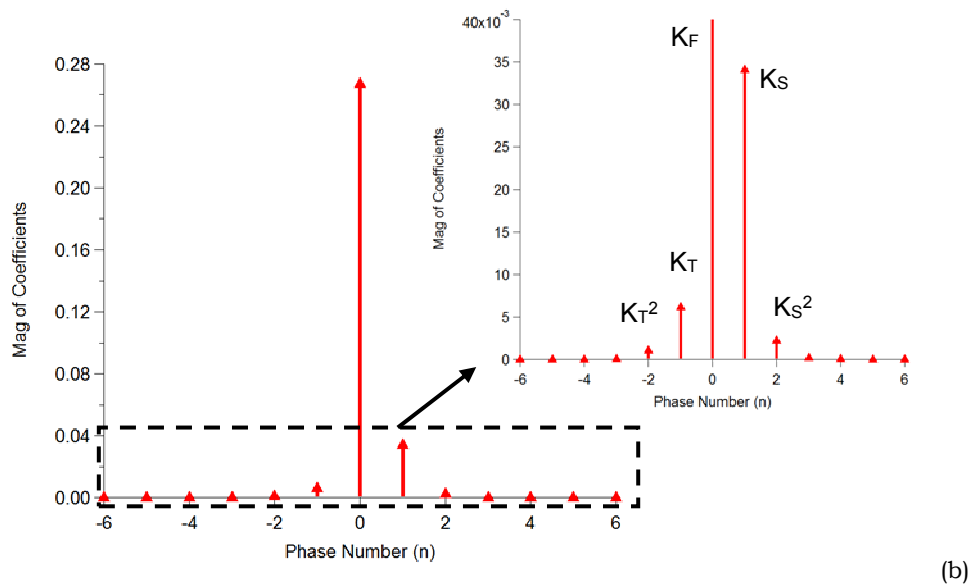
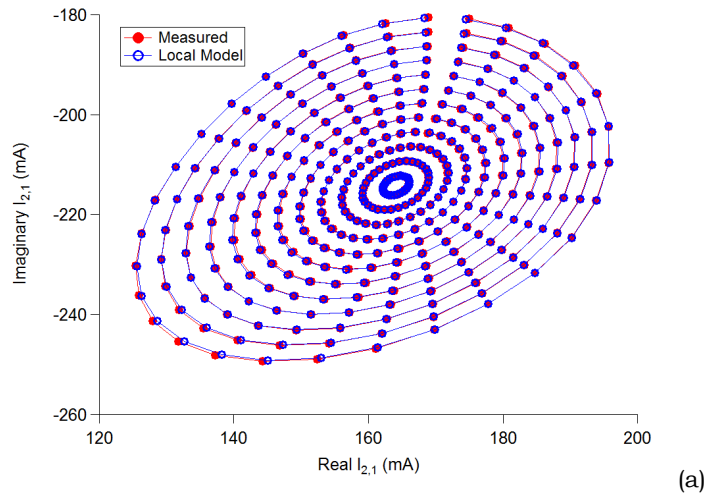


Figure A3-3: Measured versus modelled waveforms from power sweep at optimum load $\Gamma = 0.321 + j0.335$ for the $4 \times 80 \mu\text{m}$ device (a) Output voltage (b) Output current

APPENDIX B

B.1 Admittance Domain Model Coefficients at 8 GHz



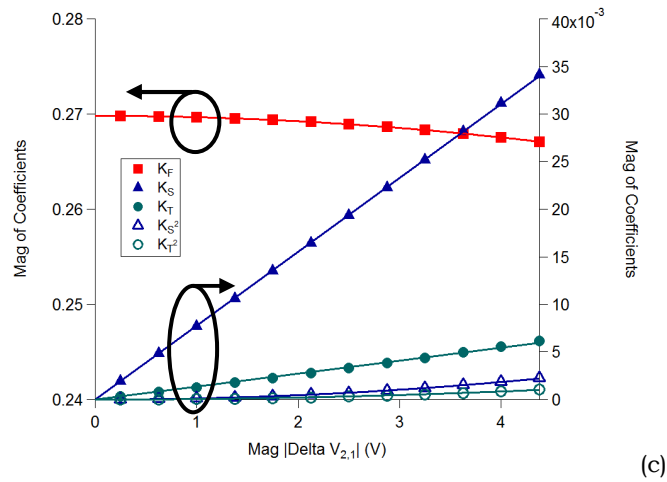
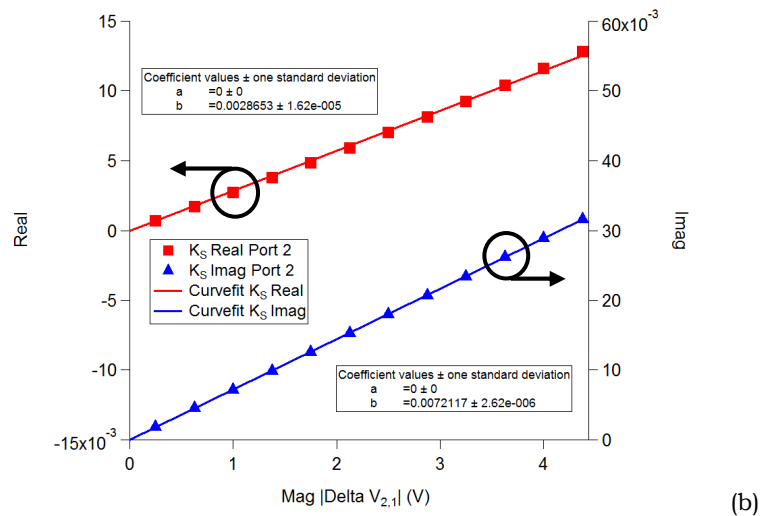
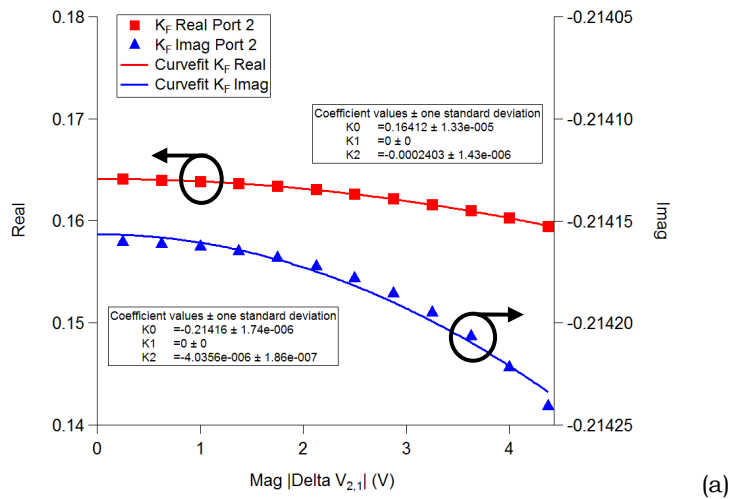
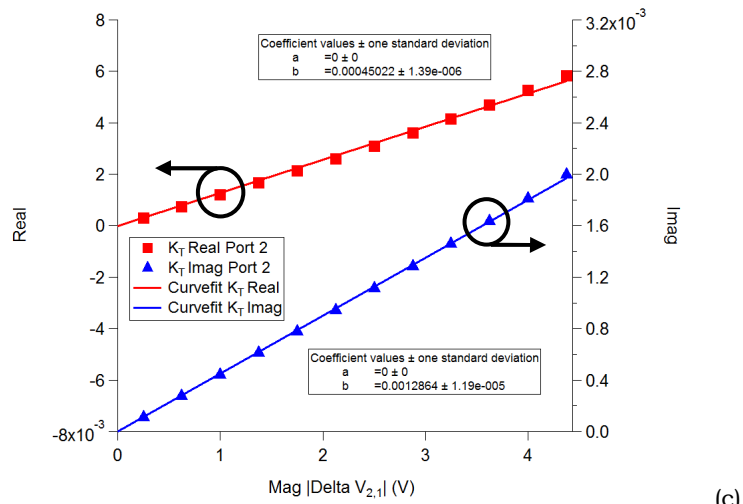
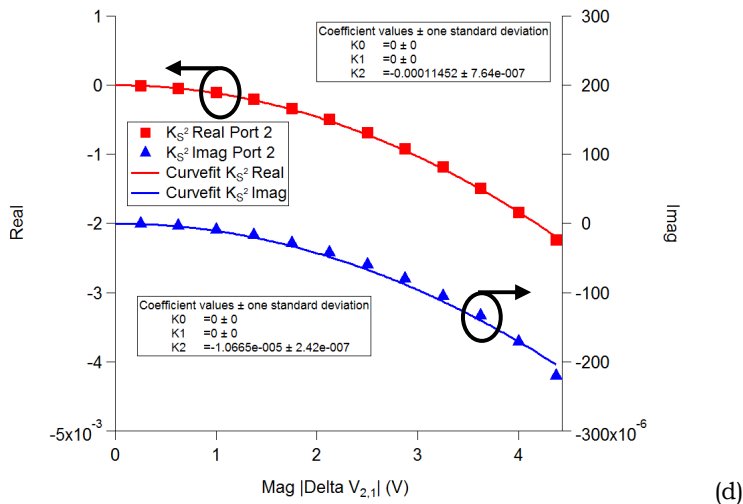


Figure B1-1: Voltage load-pull results performed on the 2x200 μm GaN on SiC transistor at 8 GHz (a) $I_{2,1}(Q_1)$ results (b) Fourier Coefficients of $I_{2,1}$ with $|\Delta V_{2,1}| = 4.375\text{V}$ (c) Fourier Coefficients of $I_{2,1}$ versus $|\Delta V_{2,1}|$

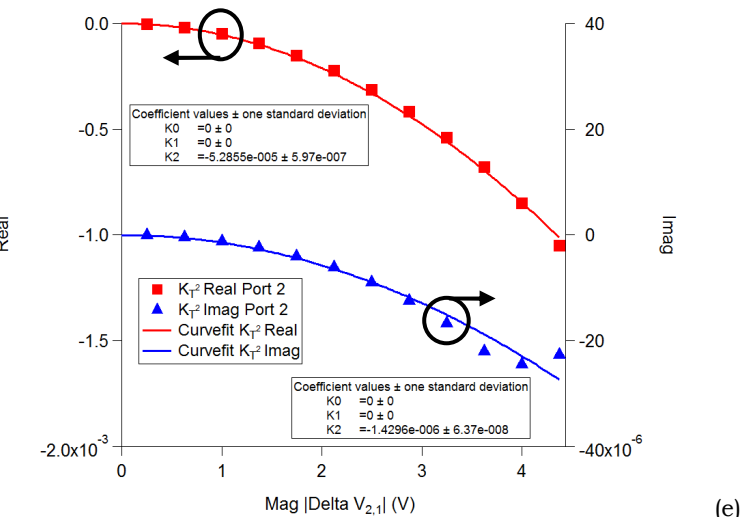




(c)



(d)



(e)

Figure B1-2: Curve fit of coefficients for $I_{2,1}(Q)$ over $|\Delta V_{2,1}|$ to obtain local Y-parameters at 8 GHz

(a) K_F and K_F^2 (b) K_S (c) K_T (d) K_S^2 (e) K_T^2

B.2 Model Results (Using FFT Extraction) at 8 GHz

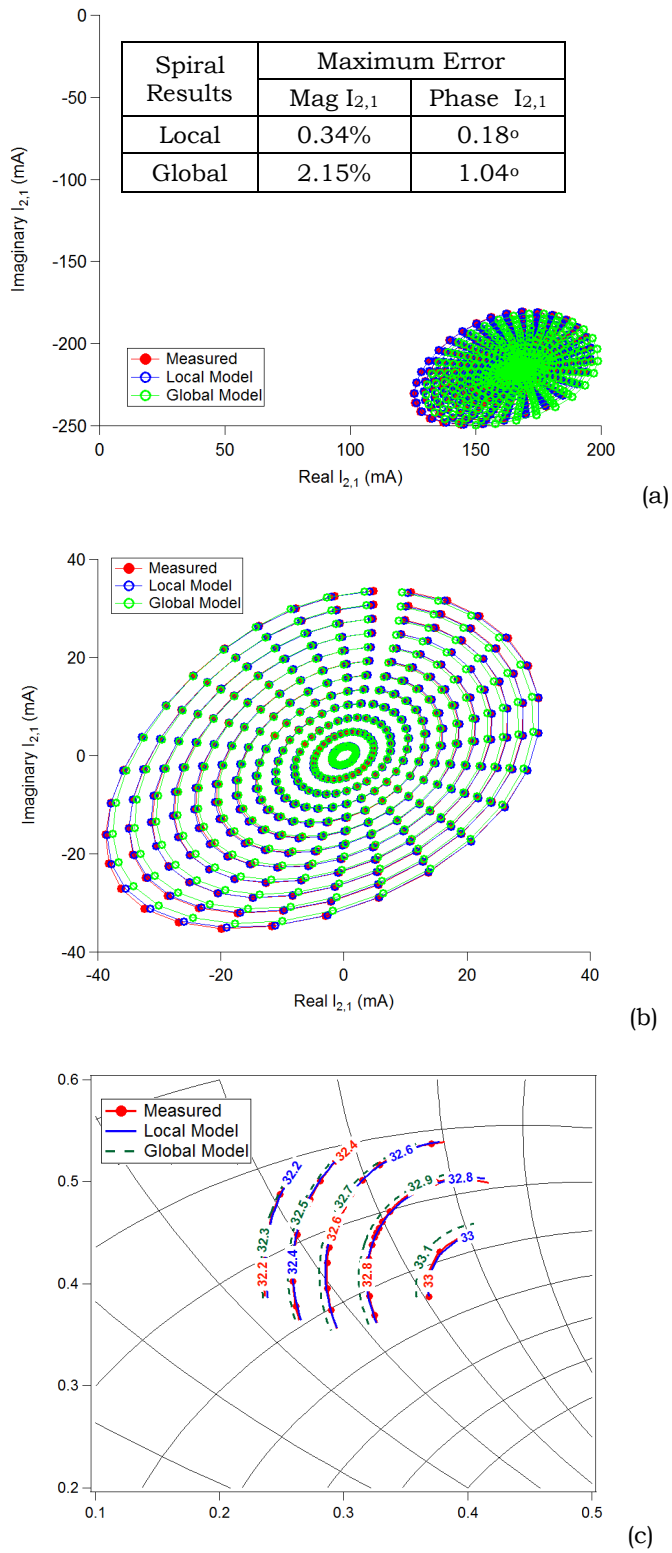


Figure B2-1: Measured and modelled results for 2x200 μm GaN on SiC transistor at 8 GHz (a) $I_{2,1}(Q)$ results (b) $I_{2,1}(Q)$ results without Y_F coefficient (c) Output power contours (in dBm).

B.3 Model Results (Using LMS Extraction) at 8 GHz

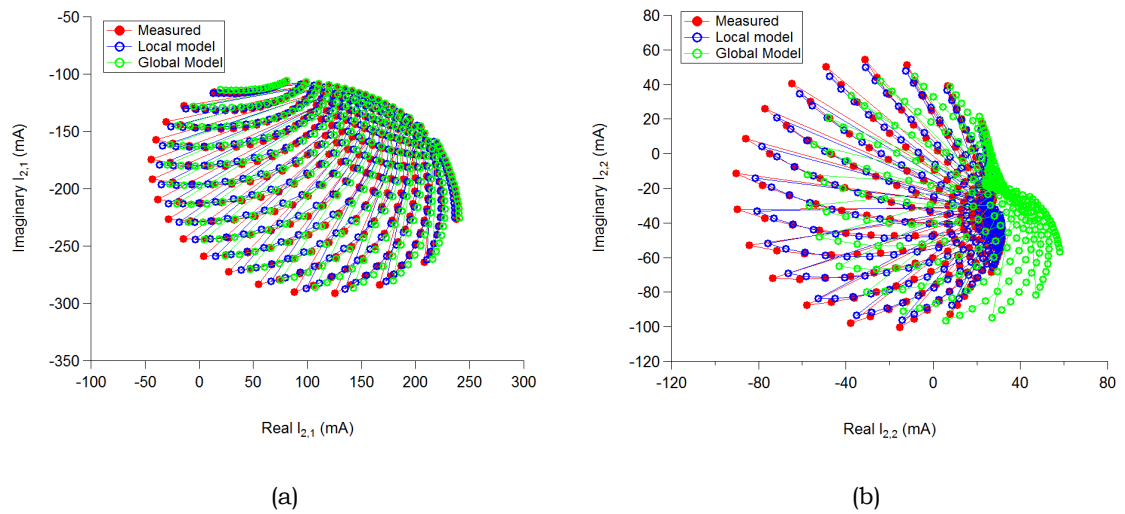
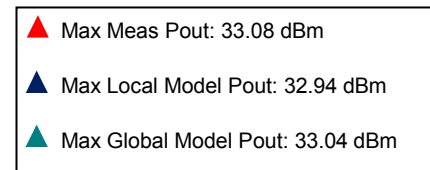
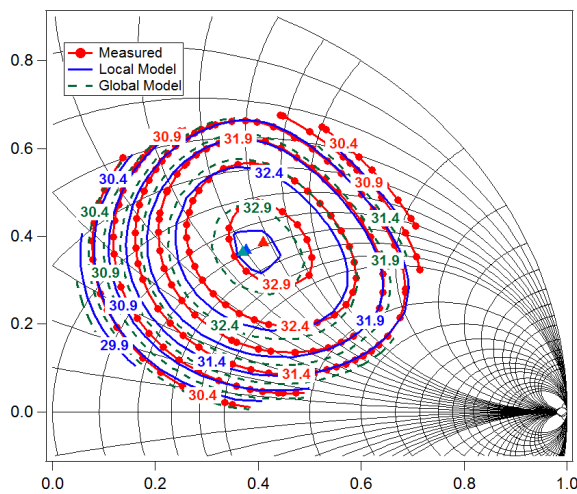
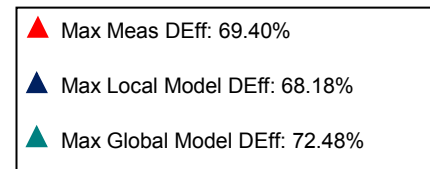
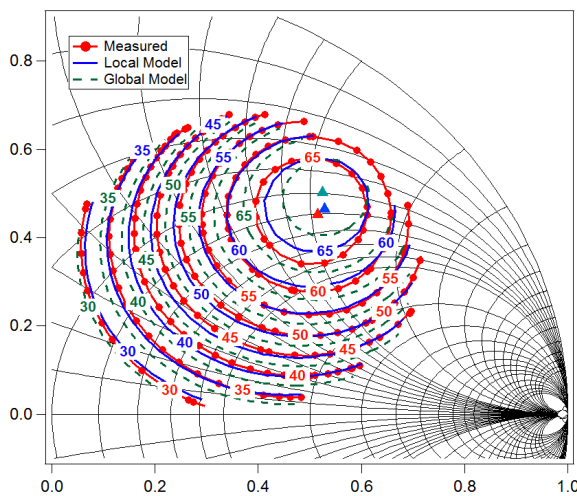


Figure B3-1: LMS results on load-pull data at 8 GHz for (a) $I_{2,1}$ (b) $I_{2,2}$



(a)



(b)

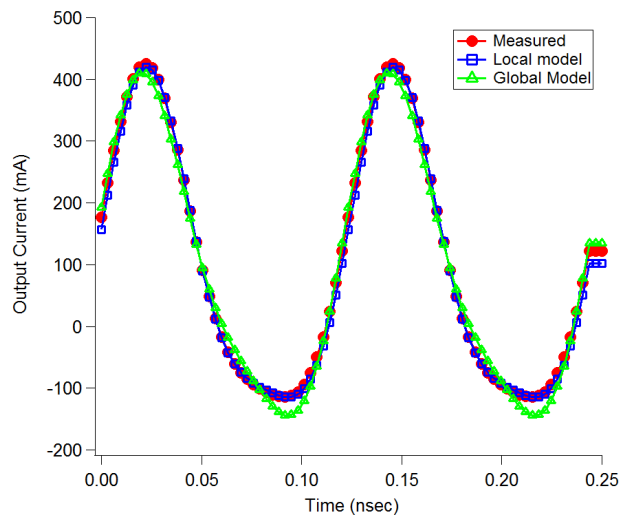


Figure B3-2: LMS results on load-pull data at 8 GHz for (a) P_{out} contour (b) Drain Efficiency contour (b) Output current waveform (at optimum load $\Gamma = 0.46 + j0.47$)