RF-IV Waveform Engineering Inspired MMIC design

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Doctor of Philosophy

By

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ABSTRACT

The research work presented in this thesis sets out to investigate improvements to the power amplifier (PA) design cycle through the use of Waveform Engineering techniques. This is approached using alternative simulation methods with strong links to the data available from time domain based radio frequency waveform measurement and characterisation systems.

One key objective of this work is to improve the overall efficiency of the radio-frequency power amplifier stage by focusing on circuit design. More specifically, the direct utilisation of waveform-engineering techniques in the development of multi-stage amplifiers to improve power added efficiency was targeted.

In developing these power amplifier design methodologies, the techniques are demonstrated and validated using monolithic microwave integrated circuit (MMIC) implementation. This work has also led to an increase in understanding of the operation of the device terminal waveforms which is used to drive an alternative simulation approach.

Through the use of standard computer-aided design (CAD) device models and measured waveform data, a 2-stage MMIC Gallium Nitride power amplifier has been detailed. This amplifier also uses internal node probe points in the interstage matching network, along with a new application of the waveform measurement system, to allow investigation of the terminal waveforms to validate the performance.

This direct implementation of these waveform measurements provides valuable information on the design of the interstage networks to reduce the number of design iterations resulting in a more efficient design process.

Waveform-engineering-based designs completed in this research have been demonstrated with test circuits and the time domain measurement system to demonstrate new modes of operation, as well as complete designs realised as prototype MMIC power amplifiers.

SUMMARY OF ORIGINAL CONTRIBUTION

This work contains three main original contributions during the development of this thesis:

1. The use of voltage source simulation methods to define the correct and appropriate waveforms at the intrinsic nodes of the Device Under Test. The waveforms are defined by the theoretical expressions and used directly in the simulator to force the correct amplifier operating mode on the transistor.

2. A Second harmonic source injection amplifier design strategy is presented. The theoretical waveform sets are presented to define the design space, and this is used in the design of a two stage amplifier. Practical device parameters are considered which detail the performance limits which are achievable.

3. An in-circuit waveform measurement and analysis technique is outlined. This approach uses a standard time domain load pull system in a novel manner. The use of the system creates a high impedance at the fundamental and harmonic frequencies, allowing direct contact measurement at internal circuit nodes, without loading the circuit.

ACKNOWLEDGEMENTS

First and foremost, I would like to thank Professor Paul Tasker for his help and guidance as supervisor during the journey of this PhD. His expertise and knowledge in the field of Microwave Engineering are outstanding and I am grateful for his patience and understanding during our discussions when he tried to explain the concepts to me. I would also like thank my second supervisor Professor Johannes Benedikt for his support and mentoring. It was as a result of some initial discussions with him that led to me pursuing this course of study.

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My thanks also go to Mr Paul Robertson, former head of department at Selex ES Ltd, who encouraged me and supported my request to take this degree. He sadly passed away before the end of this journey but my gratitude will always be with him – Thank you Paul.

Finally, and most importantly, I would like to thank my family. My wife Victoria has been supportive during these long years of study. She has not complained throughout my endless nights in front of the computer screen and the days away at University. She has taken the additional burden of things I have neglected to do in her stride and has always been there for me. I am truly blessed to have her in my life.

I dedicate this thesis to my children Oliver and Daisy.

LIST OF PUBLICATIONS

1. Haynes, Merv; Cripps, Steve C.; Benedikt, Johannes; Tasker, Paul J.; , "PAE improvement using 2nd harmonic source injection at x-band," Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC), 2012 Workshop on , vol., no., pp.1-3, 3-4 Sept. 2012.

   Abstract – Theory and measurements are presented comparing Class B amplifier performance of a 0.5 W GaAs pHEMT driven with (a) a sinusoidal signal or (b) using 2nd harmonic input injection. Engineering the input waveform in this way leads to a class B operating mode requiring 3.4 dB less input drive at 9 GHz. This increases power gain and maintains the output power above 26.4 dBm. The 2nd harmonic injection case shows a 5.9% Power Added Efficiency (PAE) improvement over the class B case.

2. Haynes, M.; Tasker, P.J.; Cripps, S.C., "High Efficiency PA Design Strategy at X-Band," Compound Semiconductor Integrated Circuit Symposium (CSICS), 2013 IEEE , vol., no., pp.1-4, 13-16 Oct. 2013. doi: 10.1109/CSICS.2013.6659232.

   Abstract – There is an growing demand for high efficiency power amplifiers at high frequencies, X-band and above. It is well understood that design strategies targeting high efficiency requires output IV waveform engineering; switching the mode of device operation from the Class A or AB modes to the Class B or C modes. Unfortunately, this mode switch results in a significant reduction in gain, which since the maximum amount of gain at high frequencies is limited, can result in degraded rather than enhanced power added efficiency. An improved design strategy, incorporating input IV waveform engineering, can be used to minimize this gain reduction thus providing for improved power added efficiency.

3. Haynes, M.; Bullen, A; Hone, D; Singh,D; “Overview of GaN Technology applications within Finmeccanica” in Automated RF and Microwave Measurement Society Conference, April 2016.

Abstract – The increased availability of GaN technology over recent years has enabled higher power amplifiers and components but has had a slower take up in military systems. The cost and access of the technology and the performance at the high microwave frequencies has kept this largely in the research domain. Solutions to these barriers are now coming to fruition and this technology is breaking through into products.

The early years used single transistors which provided simple hybrid circuits to demonstrate the practically achievable performance and the positive benefits of this technology. The follow on development, through various EDA programmes (Korrigan and Magnus) plus internal research initiatives, have moved the technology forward into MMIC implementation. This is contrasted against the improvement in availability and performance of COTS transistor components which has kept hybrid microwave solutions alive for military airborne systems.

LIST OF SYMBOLS AND ABBREVIATIONS

ADS	Advanced Design System, CAD tool from Keysight Technologies
AESA	Active Electronically Scanned Array
ALPS	Automatic Load Pull System
C	Capacitance
CAD	Computer-Aided Design
CF	Centre Frequency
C_{j0}	Schottky junction zero bias capacitance
CW	Continuous Wave
DARPA	Defense Advanced Research Projects Agency
d	Dielectric Thickness
dB	Decibels
dBc	Decibels (reference to carrier power)
dBm	Decibels (reference to 1mW)
dc	Direct Current
DRFM	Digital Radio Frequency Memory
DUT	Device-Under-Test
Eg	Energy Gap
EIRP	effective isotropically radiated power
ESCAN	Electronic Scan (Antenna)
EW	Electronic Warfare
eV	Electron Volts
F, pF,fF	Farads, pico-Farads, Femto-Farads, unit of capacitance
FD30	0.3µm gate length GaAs pHEMT MMIC process from Compound Photonics[1]
FET	Field Effect Transistor
Freq., f	Frequency
GaAs	Gallium Arsenide
GaN	Gallium Nitride
$G_{P,A}$	Class A device power gain
$G_{P,B}$	Class B device power gain
GSG	Ground-Signal-Ground, connection type used on MMICs and the probes
H, nH	Henrys, nano-Henrys unit of inductance

[1] Compound Photonics was formerly RFMD(UK) Ltd foundry in Newton Aycliffe, Co Durham.

HPA	high power amplifier
HEMT	High Electron Mobility Transistor
HT	Harmonic tuned
Hz, GHz	Hertz, Giga-Hertz
I, i	Current
Idq	Quiescent Drain Current
Idss	Saturation Drain-Source Current
Ids	Drain-Source Current
Igen	Current-Generator Plane
Igd	Gate-Drain Current
Igs	Gate-Source Current
ISS	Impedance Standard Substrate, as used for measurement calibration
j	Denotes the imaginary component of a complex impedance
L	Inductance
LP	Load-Pull
μm	micro-metres
MAG	Maximum Available Gain
MMIC	Monolithic Microwave Integrated Circuit
Nd	Semiconductor doping concentration
NL	Nonlinear
P	Power
P_{1dB}	Output power at 1dB gain compression
PA	Power Amplifier
PAE	Power-Added Efficiency
PDK	Process Design Kit
PHD	Poly Harmonic Distortion
pHEMT	Pseudomorphic High Electron Mobility Transistor
PUF	Power Utilisation Factor
q	Electronic charge
R	Resistance
RF	Radio Frequency
RF-IV	RF Current-Voltage
RFOW	RF-on-wafer
S-parameters	Scattering Parameters

SiC	Silicon Carbide
SWaP-C	Size, Weight, Power and Cost
TRL	Thru, Reflect, Line – Calibration method
TRM	Transmit-Receive Module
UAV	Unmanned Aerial Vehicle
UGW	Unit Gate Width, of transistor device
V, v	Voltage/Volts
Va	Applied Schottky junction bias
Vbi	Schottky built in potential
Vds	Drain-Source Voltage
Vgd	Gate-Drain Voltage
Vgs	Gate-Source Voltage
Vk	Knee Voltage
Vp	Pinch-off Voltage
VNA	Vector Network Analyser
W, mW	Watts, milli-Watts
X	Reactance
Z	Impedance
ε_r	Relative Dielectric Constant
ε_s	Permittivity
K_{eff}	Effective Dielectric Constant
λ	Wavelength
$\eta_{D,A,ideal}$	Ideal Drain Efficiency, Class A
$\eta_{D,A}$	Drain Efficiency, Class A
$\eta_{D,B}$	Drain Efficiency, Class B
η_G	Gain efficiency factor
η_K	Knee voltage efficiency factor
η_L	Matching loss efficiency factor
η_D	Drain Efficiency
η_{FB}	Feedback Efficiency factor
Ø	Electrical Length
Γ	Reflection Coefficient
Ω	Ohms

CONTENTS

1 INTRODUCTION

The high power amplifier (HPA) is a key building block in many military Radar and Electronic Warfare (EW) systems. Modern radars are realised with Active Electronically Scanned Array (AESA) Antennas [1],[2]. These systems deliver high effective isotropic radiated power (EIRP) by the virtue that the power from many radiating elements are combined. This power addition, together with the array factor (AF) focusses the power in a specific direction.

In these AESA systems the design focus centres on the transmit-receive module (TRM) as they are the crucial building blocks with a dominant impact on performance [3]. The basic block diagram of a typical TRM is shown in Figure 1.1, highlighting the major functions. The focus of this work will concentrate on the HPA.

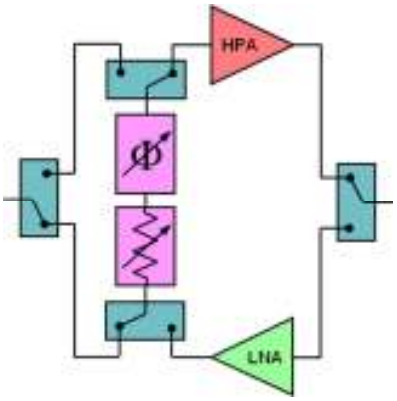


Figure 1.1 Typical 'Common leg' Transmit Receive module architecture

In the transmit path of an 'n' element array, each TRM provides 1/n of the total antenna power, where n ranges from ~10 in lightweight unmanned air vehicle (UAV) systems to ~2000 in large fire-control radars, leading to the requirement of the high power amplifiers (HPAs) to deliver several watts output power to each antenna element.

Airborne electronic warfare (EW) power modules, in contrast, tend to be transmit only, with the receive function performed by the Electronic Support Measures (ESM) part of the equipment. Recent developments in off-board RF decoys however [4], [5] have shown the need for similar transmit-receive functionality in EW applications.

These EW HPAs have similar power output requirements to AESA radar applications but with increased bandwidth.

1.1 Airborne Radar HPA requirements

Airborne ESCAN radars typically operate in X-band for airborne fire-control or surveillance systems, compared to S-band or C-band in the case of naval radars. The electrical requirements are diverse, but specifications for solid-state modules often include the following:-

- In the transmit path each module must provide a typical peak output power of several watts operating with pulse lengths ranging from 500ns to as much as several hundred microseconds.
- Prime generator power is at a premium, especially in fighter aircraft, all the electrical characteristics must be achieved at minimum DC consumption. It should be remembered that cooling, DC-DC conversion, and power switch/circulators dominate the overall efficiency of these RF systems. All these factors demand the availability of highly efficient HPAs.
- Mass is severely constrained in airborne platforms, especially in the case of transmit-receive modules. Because an E-scan antenna may contain 1000-2000 such modules, each gram added to the TRM will immediately increase the antenna mass by 1-2kg, but the problem is compounded by the need for a stronger structure to support a heavier array.
- Cost of the TRM is also a key parameter as the total cost is then scaled by the number of modules. Minimising cost of the key functions is translated into reduced chip area for MMIC components.

The basic system design of power modules is quite elementary, with only simple passive networks to create the desired beam steering and polarisation signals. However the electrical implementation is complex due to the small physical size, wide bandwidths and thermal problems which exist in such modules. In order to get the functionality in the required size, extensive use has been made of GaAs MMIC technology, which allows integration of circuit functions with the required performance across the operating band. Other technologies are emerging which could offer enhanced performance are being considered (e.g. GaN for HPA applications).

1.2 EW HPA requirements

The wide bandwidth and high frequency operation, typically 6-18GHz, of the EW power modules has meant the RF power amplifiers are in the domain of GaAs pHEMT technology and more recently GaN FETs. Operation is generally at CW (or very long pulse lengths) which results in increased power dissipation, as power added efficiencies (PAE) are lower than those for radar bands. Higher channel temperatures result which can adversely affect reliability.

The prime power is also of consideration, especially in the off-board RF decoys systems [4], [5] where this power is derived from battery technology. Less efficient amplifiers will lead to reduced jamming time. In addition these systems have small form factors and cooling is very limited so efficient operation is paramount.

The HPA components need also to be capable of working without some form of output isolation, such as a circulator. These components are difficult to achieve across the EW frequency range. However, without any output isolation it is possible for the amplifiers to see highly mismatched loads producing high voltages at the output of the devices resulting in destructive breakdown.

1.3 MMIC HPAs

During the 1980s MMIC technology was being developed for AESA radar applications, with GaAs as the semiconductor of choice [1]. In spite of much interest in GaAs HBT amplifiers during the 1990s, GaAs pHEMT technology (0.5μm or 0.25μm) now offers good power-added efficiency (>40% at X-band) and is more widely deployed. Although a single MMIC will deliver up to 10W at 10GHz, a balanced pair of HPAs is likely to offer comparable efficiency and better match even when switched off. In radar modules operating at any significant duty cycle the HPA drain-source current dominates the power consumption, and the component is often biased to give Class AB operation rather than Class A. Following fabrication of the MMIC, the wafer is thinned in order to reduce the thermal resistance of the finished die, which will typically be soldered to a thermally conductive plinth.

More recently, the performance requirements for military systems has become more demanding requiring higher power and improved efficiency HPAs. The development of GaN technology is now being pursued for these components.

Table 1.1 summarises some currently available wideband and narrowband HPA GaAs MMICs and the relative performance figures.

Technology	Frequency (GHz)	Power	Size (mm)	PAE	Source	Ref
GaAs pHEMT	6 – 18	>5 W	5.8 x 5.8	~ 22%	BAE Systems	[8]
GaAs pHEMT	6 – 18	5.6 W	5.7 x 4.3	~ 25%	TriQuint	[9]
GaAs HBT	9 – 10	11 W	5 x 3.6	~ 40%	UMS	[10]
GaAs pHEMT	9 – 10	11 W	4.4 x 3.6	43–45 %	MACOM	[11]
GaAs pHEMT	8.5–10.5	~ 8 W	3.5 x 2.6	35 – 42%	TriQuint	[12]

Table 1.1 Sample of commercially available HPA MMICs

The data shows that the X-band power amplifiers have efficiencies around 40% and the wideband amplifiers around 30%.

It is clear from this simple top level view of the radar and EW systems that the power amplifier is the key driver in performance, packaging, cooling and cost. Developing highly efficient power amplifiers addresses several of these important aspects simultaneously. Reduced power dissipation helps more modules to be powered up improving transmit power[2]. This also reduces thermal load on the cooling equipment. It also allows the packaging to be simpler, without having to resort to exotic materials and assembly techniques, thus reducing cost.

1.4 Future system trends

The efficiency of RF PAs is becoming more important for future systems where multi-functionality is to be exploited [6],[7]. In these systems a single antenna can be used for radar, EW and communications. Other systems are optimised to use multiple communication bands in a single unit. These systems can be reconfigurable and the use of bespoke amplifiers for each application is not feasible, however as shown from section 1.3, increasing the operational bandwidth generally leads to a lowering of efficiency.

[2] Modules can be switched off to keep within dc power budgets in the AESA system. Allowing more modules to be active increases the total transmitted power.

The drive for future systems is therefore for reduced size, weight, power and cost (SWaP-C). In this respect there are several high profile research programmes aiming to improve technology and applications to increase efficiency in reduced form factors or to manage the associated thermal management problem.

Improving the efficiency at the circuit level relaxes the thermal consideration and will complement the improvements made under these programmes, and allow higher power operation on standard foundry processes where the exotic materials and processes may not exist.

1.5 High Power Microwave Amplifier Design Process

The typical power amplifier design flow, Figure 1.2 [13] starts with capturing the initial system performance and operational requirements. The active device technology choice and biasing Class follow. In low frequency microwave designs, the device choice is varied but as the frequency increases the technology choice reduces. At X-band frequencies and above, the implementation of power amplifiers in the 1 W to 10 W output power range is dominated by the use of Field Effect Transistor (FET) devices in Gallium Arsenide (GaAs) and, more recently, Gallium Nitride (GaN) semiconductor materials. The work in this thesis will concentrate on these FET devices (and in particular MMIC implementation) but the techniques and approach are technology independent.

The basic amplifier circuit then defines a load impedance space, $Z_L(f)$, for correct operation at the chosen bias point and operating class. These impedances can be identified by various means.

1. Cripps method approximation
2. Simulation using CAD software with device non-linear models
3. Load pull measurements

These processes increase in complexity down the list from the basic theoretical view point to the full measurement based load pull approach.

The output from this process is a defined load impedance space Z_L for the device to deliver the output power and efficiency in accordance with the specification. The design

then becomes a problem of synthesising the network response to deliver these impedances to the device reference plane.

It is interesting to note that during this design flow there is little attention to the device waveforms, even though the underlying theory of the amplifier classes comes from a RF I-V waveform viewpoint. The design task and resulting circuit optimisation are confined to the frequency domain [13]. Furthermore, in the design of multistage amplifier optimisation goals relating to the output power and efficiency are usually defined. Allowing the interstage matching to be varied with these goals is obviously non-optimum as the variables and the goals are uncoupled as the internal load line and operating waveforms are not considered.

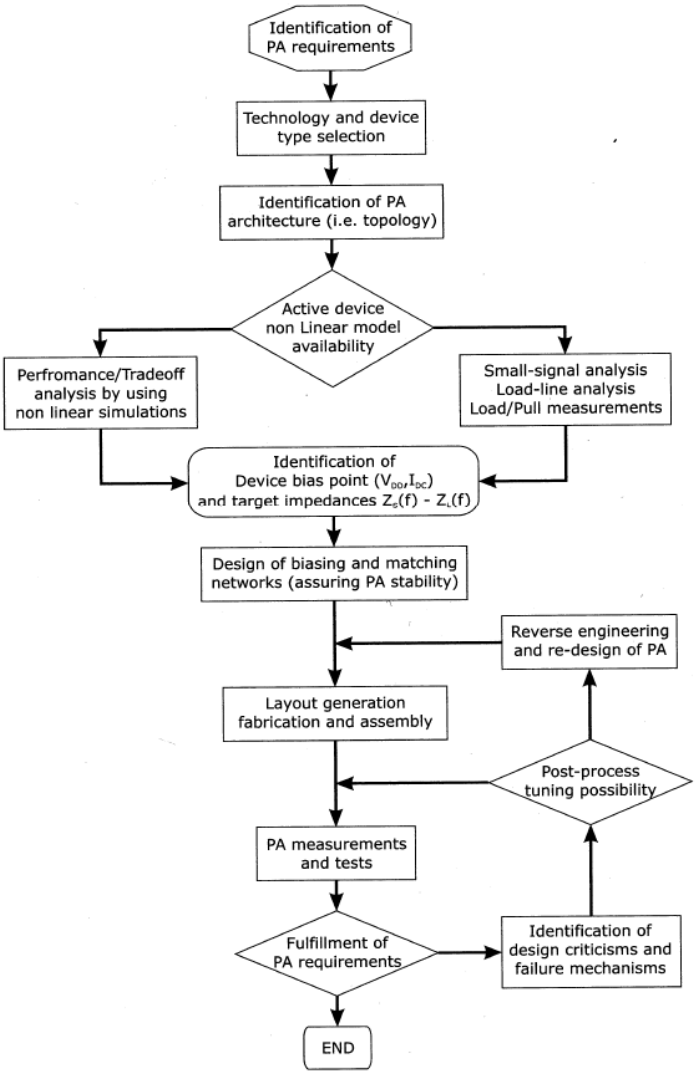


Figure 1.2 Typical HPA design flow [13]

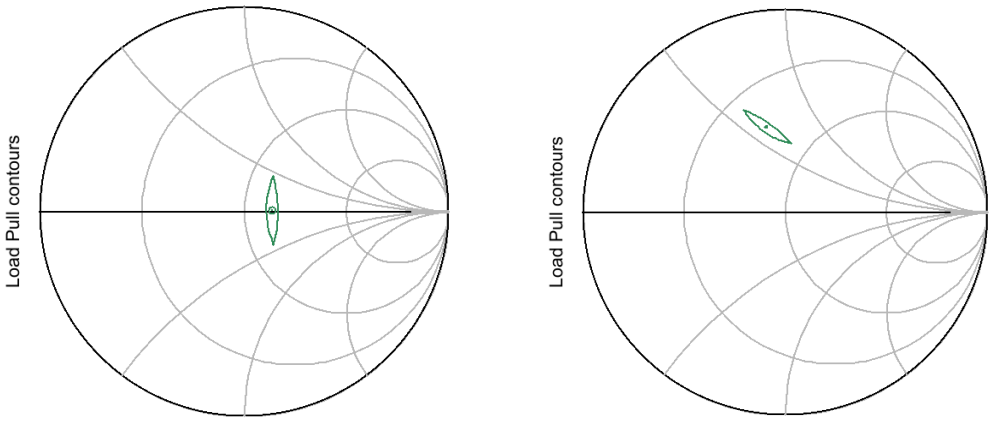
1.5.1 Definition of the load impedances

Power amplifier design and analysis requires knowledge of the large signal performance of the transistor and non-linear effects and design strategies have long been based on load-pull techniques. These allow determination of the optimum impedances which need to be applied to the device at the reference planes. These load impedances can be derived by analysis, using CAD simulation and via measured load pull data.

1.5.1.1 Analysis – The Cripps Load

Cripps [14] demonstrated the shape of the load pull contours is defined by the device RF-IV characteristics. This method is a simple but powerful analytical approach and showed that the impedances to be created need to be referred to the correct reference plane, the current generator. These impedances are modified by the parasitic elements (e.g. packages, bond wires etc.). This allowed the initial amplifier designs to start on a theoretical footing to derive some basic parameters and matching networks.

It can also be used to define a region of the smith chart to reduce the need to fully characterise the impedance plane, resulting in a targeted sweep of the values and reduce the measurement space and hence improving the design time.



(a) Current Generator Plane (b) Extrinsic Plane

Figure 1.3 Cripps load analysis for CP FD30 MMIC process 10x75µm pHEMT device (a) Current generator plane (b) Extrinsic Plane (Frequency=9GHz)

1.5.1.2 CAD Simulation methods

Use of the circuit simulator with non-linear device models can preclude the measurement of the load pull data and can speed up the design process by performing analysis in the CAD tool. A typical response is shown in Figure 1.4 showing close correlation to the Cripps load.

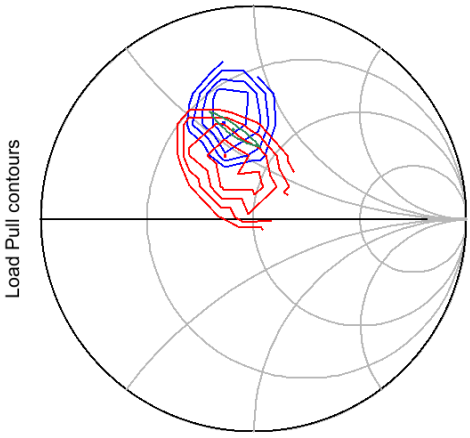


Figure 1.4 Simulated load pull data for CP FD30 MMIC process 10x75µm pHEMT device Power contours (red), PAE contours (blue), Cripps load (green)

This approach requires a non-linear model to be available for the device in question. These are generally compact models (especially through foundry access Process Design Kits) although new behavioural modelling approaches based on measured data are available. This in itself, however, still doesn't give an insight into the waveforms of the amplifier but the simulator allows voltage probes to be included at any node in the circuit for waveform monitoring.

The simulator can also be configured to provide an alternative design strategies which can overcome some of the shortfalls of existing design approaches or to investigate different scenarios.

1.5.1.3 Load Pull measurements

Load Pull is the act of presenting a set of controlled impedances to a device under test (DUT) and measuring a set of parameters at each point. Practical Load Pull measurement systems can be split into passive and active solutions [19] and are shown in block diagram form in Figure 1.5.

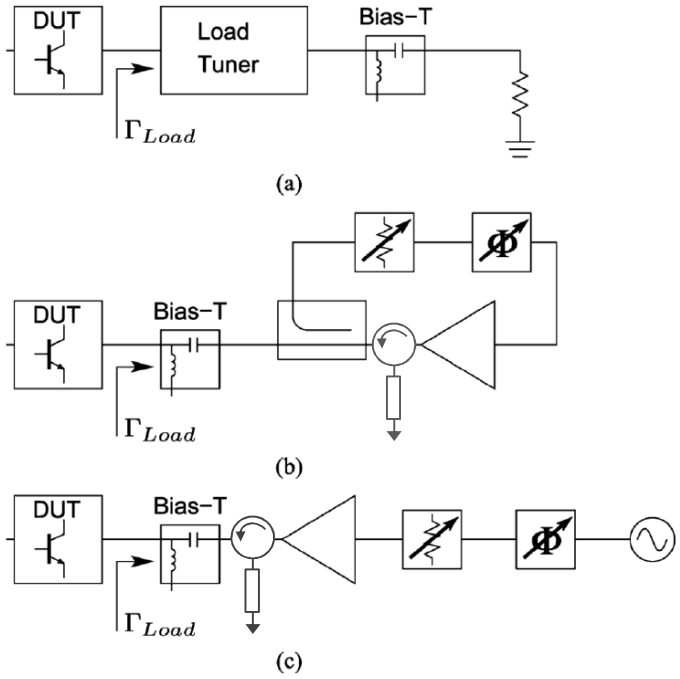


Figure 1.5 Load pull system block diagram (a) Passive load pull, (b) Closed loop Active Load pull and (c) open loop active load pull [19]

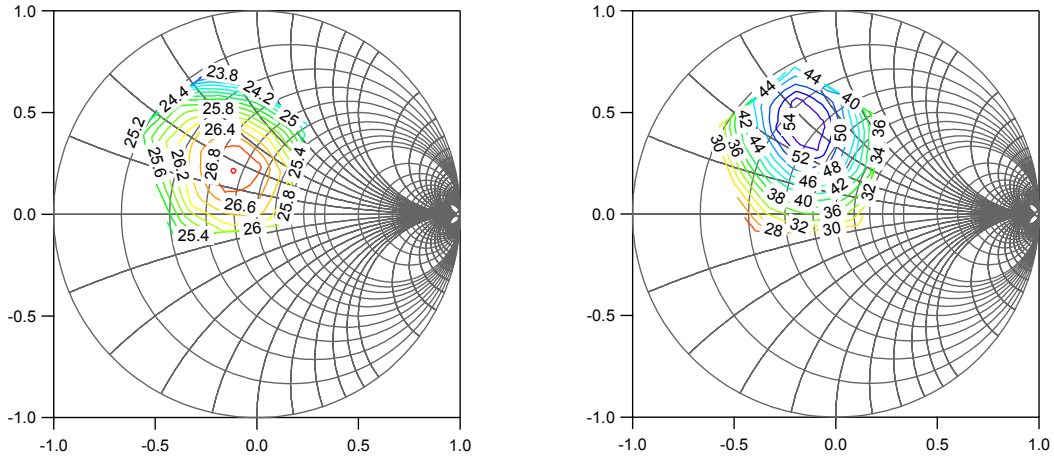
Passive load pull systems, Figure 1.5(a), use passive networks with tuneable elements (moveable stubs etc.) to alter the impedance presented to the device-under test (DUT) [20][21]. These passive systems have limitations with the impedance space that can be covered due to systems losses, that is impedances on the extremities of the Smith chart are unrealisable.

The impedance presented to the DUT is actually the ratio between the reflected and incident waves at the load. By terminating the signal from the DUT and using an injected signal at the output with varying amplitude and phase, an electronically adjustable impedance is created. Active Load Pull systems, Figure 1.5 (b) and (c), therefore measure and terminate the normal amplifier output signal, using an isolator or

circulator and load, then inject a system generated signal to the output of the DUT. This can be performed in open loop or closed loop configurations. The closed loop systems take a portion of the amplifier signal and feed it back to the DUT after varying the amplitude and phase. These systems can become unstable with the feedback network. Open loop systems do not suffer these instabilities as the amplifier signal is sampled and terminated, with an artificial reflection (injection) signal created at the correct amplitude and phase with a signal generator, usually under computer control. Phase shifters and digital attenuators control the injected signal to synthesise the load impedances [23] in both these configurations.

More recently, the active load pull techniques have been configured in time domain systems [24]. These systems allow the direct measurement and analysis of amplifier operating modes with reference to the time domain waveforms. The output data files from these systems can be used for the application for this is the behavioural modelling.

The typical response from these load pull systems is shown in Figure 1.6 mapping output power performance and drain efficiency against load impedance.

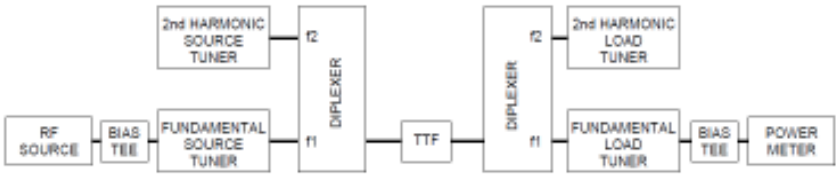


(a) Output Power (b) Drain Efficiency

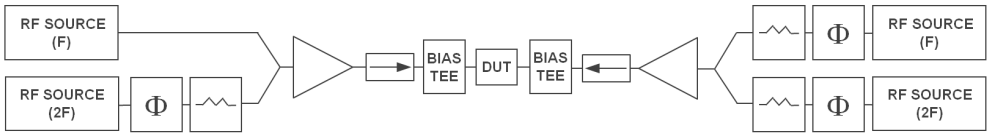
Figure 1.6 Measured load pull data for Compound Photonics FD30 MMIC process 10x75µm pHEMT device (a) Output power contours and (b) Drain Efficiency contour (Frequency=9GHz, Vds=+9V, Vgs=-1.1V)

These systems can be configured to control harmonic impedances as well as the traditional fundamental only set-ups (Figure 1.7). In these systems the signals are split to include fundamental and harmonic frequency paths, with impedance control in each

arm. The signal splitting is either via a diplexer, as in the case of the passive tuner based systems (Figure 1.7(a)), or with a power combiner network feeding a driver amplifier (Figure 1.7(b)).



(a)



(b)

Figure 1.7 Typical Harmonic load pull configurations. (a) Passive system [22] and (b) Active system (after [13]). Control interfaces not shown

1.5.2 Source pull

Source pull is the same as load pull except the input impedance seen by the active device is varied rather than the load impedance. Source impedance strategies are less well defined, with the approaches based solely on measured impedance sweeps [25] as there are no closed form solutions available.

The input harmonic space has been investigated, using the system shown in Figure 1.7(a), providing evidence that there is a significant effect of the second harmonic input terminating impedances on the efficiency of the amplifier [22].

1.5.3 Load Pull Summary

The design of power amplifiers has traditionally started from the impedance space and designing matching networks to deliver a specific set of impedances to the device for a specific operating mode. Cripps explained the shape of the load pull contours and this, coupled with the measurement methods outlined in this section have been used successfully in the design of power amplifiers for many years.

They are also useful to

i. Verify simulation results of a transistor model (model validation) and gather characterization data for model extraction (behavioural model extraction)

ii. Ensure a microwave circuit's ability to perform after being exposed to high mismatch conditions (ruggedness test)

iii. Confirm the stability or performance of a microwave circuit or consumer product under non-ideal VSWR conditions.

The more recent time domain based measurement systems have added an extra dimension to the traditional load pull where the exact operating mode can be determined with reference to the actual device terminal voltage and current waveforms.

1.6 Waveform Engineering

The role of the terminal RF-IV time varying waveforms in improving efficiency and optimising PA performance has been known for many years. Tyler [26] demonstrated this approach in valve technology where flattening the voltage waveforms (class F) was found to be beneficial in efficiency improvement whilst providing higher output power than class C operation, which was the reference approach for high power generation at the time. Snider [28] provided a comprehensive mathematical analysis of this Class F operation, with the optimal loading condition of zero or infinite harmonic impedances, alongside a comparison to Class B. This approach to amplifier design and analysis, involving the ability to modify the time varying terminal waveforms has been described as 'Waveform Engineering' [27]. Waveform engineering is the process of using the device, dc bias operating points and circuit terminating impedance characteristics to generate the specified waveforms for a given class of amplifier.

1.6.1 Output Waveforms

The 'high efficiency' modes of operation (Class F etc.) using this analysis technique have dominated and require properly defined fundamental and the harmonic frequency terminating impedances at the transistor output terminal. This has long been the focus and the mathematical analysis of waveforms has been further developed by Raab [29][30] where the harmonic content of the ideal voltage waveforms have been optimised and analysed. This work has also included an analysis of bandwidth limited operation, i.e. truncating the number of harmonics utilised in the waveforms [31][32]. Rhodes [33] has taken the idealised transistor characteristics and derived an elegant expression for the load impedance network element values in order to create the class F amplifier operating mode, demonstrating the results are dependent on the terminating network impedances and not transistor properties.

The development of these modes has expanded with the operating space by the use of the continuous mode theory [18]. Here the Class B and Class J operation are shown to be points on the same continuum of operation providing the same power and efficiency as class B.

In addition to these classical amplifier modes, there has been an expansion of research in this area involving the manipulation of the harmonic content to adjust the waveforms to optimise PA efficiency [13]. Colantonio et al have studied several options

with various numbers of harmonics being controlled. Initial research targeted amplifiers with second harmonic load terminations [33]. This approach adds a correctly aligned second harmonic component of drain voltage. The theoretical analysis of this design space defines a voltage gain function increasing the fundamental content of the waveform. Further work using higher harmonics [34][35] has been reported by the same research team and has been coined as the "Harmonic Manipulation Technique" [34]. These operating modes were demonstrated by appropriate selection of the harmonic content based on load pull sweeps [36]. Theoretical analysis of the technique has expanded a design space and has shown that the efficiency can be improved by optimising the ratio of the harmonic contents rather than rely on analysing the amplifier under the ideal zero and open circuit load impedances [37].

These methods so far have implemented waveform engineering using passive impedances. Harmonic injection at the output, resulting in active rather than passive load impedances have been investigated [42] and shown to improve the efficiency of the amplifier stages. This implementation requires complex circuitry to split the input signal and double to create the output harmonic injection. This is then manipulated in amplitude and phase before injection at the output port via a diplexer arrangement. It does, however, provide an efficiency improvement even when considering the added power of the auxiliary second harmonic generation circuit and amplifier.

Type	F GHz	DE %	PAE %	Power dBm	G_p dB	Ref
GaAs amp RF board Class F	2.0	-	76	+21	13	[44] 2005
GaAs pHEMT Class F	9.6	50	-	+28	6	[38] 2010
GaN board PA Class J continuum	1.5 -2.5	60-70	-	+39	18	[41] 2009
GaN Board PA Class F, Harm Inj	0.9	74	-	+40	20	[37] 2010
GaAs transistor Class F continuum	0.9	75-82	-	+20.2	20	[39] 2011
GaAs hybrid PA Harmonic tuned	5.0	73.7	60	+25.6	6.5	[34] 2000
GaAs MESFET Harmonic tuned	5	-	55	+25	7	[37] 2003
GaN MMIC PA Class B	8	-	34	+36	10	[40] 2003

Table 1.2 Summary of published single transistor amplifier performance.

A further point on the review of the output waveform engineering results has shown a reliance on presenting drain efficiency results, ignoring any effects of the input drive levels. This is especially true of the low frequency applications (Table 1.2). The work at higher frequencies with full harmonic manipulation methods has made reference to the gain reduction of these modes and the data has been extended to include the PAE of the amplifier [34][37].

It is clear from this review that waveform engineering has been exploited practically (after initial postulation from a theoretical perspective) and that most of the focus is on the impedance environment for implementation. Furthermore, in the majority of these research themes it should be noted that this has been confined almost exclusively to the load impedances and the input side of the circuit has been largely neglected.

1.6.2 Input Waveforms

Investigation into the benefits of input harmonic impedance terminations have been reported in high efficiency amplifier operation [43][44][45][46]. These early works show circuit techniques to present passive input (source) impedances to the transistor device under test (DUT). These circuit modifications improve efficiency by reducing the effects of pHEMT Cgs varactor distortion on the output current conduction angle. White [43] uses capacitive and resonant elements to short circuit the input second harmonic currents arising from the varactor effects, which broaden the gate voltage shape, and hence the output current pulse. This leads to reduced efficiency as there is significant current flow during the output voltage swing. White also demonstrated second harmonic distortion of the gate signal of a pHEMT is more problematic than for a MESFET circuit due to the more severe capacitance-voltage characteristic of the Gate-Source capacitance (Cgs). The result was an impressive 49% – 81% improvement in simulated PAE. This work has recently been extended on by Canning et al [47] demonstrating this efficiency improvement practically and linking this to the intrinsic device waveforms for MMIC implementation. Here the resonant circuit places the harmonic short circuit impedance at the device input intrinsic Cgs plane.

Maeda [45][46] used second harmonic source impedances to create a ‘quasi square wave’ signal at the gate terminal of a FET to minimise the switching time of the transistor waveforms. The waveform is acknowledged to have an ‘increased flat portion

at the maximum of the waveform leading to improved output power. The realised power module showed an efficiency improvement of 6% at 900MHz when adding in the passive source harmonic termination.

Gao [44] again identifies the critical performance of the input circuit and describes a simulation procedure of defining the optimum fundamental and harmonic source impedances. The work demonstrates the strong relationship between efficiency and the second harmonic input termination at 2GHz. The optimum impedance condition is offset by an amount predicted by the author to be related to the simple circuit theory considering the parasitic elements of the package – a similar effect to the Cripps Load at the output.

The work on harmonic tuned amplifiers by Colantonio [34] developed a design methodology for the output load conditions and also included an assessment of the role of the input waveform on the clipping of the output current shape and the corresponding effect on the output terminating impedances and hence voltage waveforms. In this work the design space was mapped using a gain overshoot function (to demonstrate the level of harmonic voltage level required for improved performance and related these to the second and third relative harmonic levels. It is noted that using the 2nd HT PA design method requires additional design efforts related to the control of the input harmonic terminations to properly generate the output harmonic components with appropriate phase relationships. These source impedance strategies are less well defined, with the approaches based solely on measured impedance sweeps as no closed-form expressions can be easily derived for input harmonic impedances [25].

Commercial application of these techniques is also noted. The work by Mitsubishi Electric [48] shows a high efficiency internally matched amplifier approach at 5.8GHz, where the input side second harmonic tuning was noted to have a dominant effect on performance. Although the impedance space was swept using a harmonic load pull system, there was no explanation provided on the strategy or the improvement noted. Subsequently, a C-band 100W GaN HEMT power amplifier was released by Mitsubishi quoting the record PAE of 67% is “enabled by the world’s first harmonic tuning circuit placed in front of each GaN HEMT cell on the substrate” [48].

More recent work has expanded the operating space from the passive source impedances and demonstrated the concepts for active injection techniques Ingruber [50] Ramadan [51], Kusonoki [55] and Fan [56]. Here the input waveform can be shaped by adding a second harmonic contribution to the input signal from an external source.

Ingruber [50] describes an amplifier concept using a second harmonic input injection method at 1.6GHz, named by the author as a "harmonic controlled amplifier". This paper acknowledges the low gain of reduced conduction angle operation and presents this as a method of improving the PAE and intermodulation distortion of the amplifier. The power stage injection signal is created from a driver amplifier stage which splits the signal through separate amplitude and phase shaping paths and injected to a class F power stage via a diplexer arrangement. The circuit has a method for tuning the amplitude and phase of the fundamental and second harmonic drive signal. The paper also mentions optimising the gate bias voltage as a consequence of the synthesised signal. There is no explanation of the interstage matching except there is a phase shifting network to create an optimum waveform shape. Similarly, Ramadan [51] has identified an experimental study demonstrating the injection technique on a discrete GaN transistor device in class F and F^{-1} at 2GHz, creating a clipped sinewave drive signal using test set-up. This is compared with a passive short circuit load condition. The authors present an efficiency improvement and describe the performance being due to the reduced 'on-time' conduction angle of the drain current. Extension of this work by Ramadan [52]has shown the effect of the reduced conduction angle from a second harmonic injection signal has on the output current pulse leading to improve amplifier efficiency, with the Fourier analysis driving the optimum gate voltage. It was noted that this work does highlight the need for any driver stage to be able to create these harmonic components. This approach was developed further [53] in a two stage amplifier designed using the gate voltage waveform shaping at 1.8-2.2GHz. The design basis was to shape the gate waveform to reduce the 'on' time of the current pulse at the drain. No procedure is provided for the interstage matching network and it is clearly evident there is significant tuning of the hybrid circuit to achieve the waveform performance.

Source injection has also been used to improve amplifier linearity. Fan [56] analysed the intermodulation distortion components from a FET device using Volterra

series description of the non-linearities and demonstrated these can be cancelled by controlling the injection signal at the baseband and second harmonic frequencies. Kusonoki et al [55] expanded this work and demonstrated the approach and the additional load impedance dependence of the circuit to optimise the linearization technique. Both these works show a practical circuit implementation of an amplifier stage and a linked second harmonic generator circuit fed in via a diplexer arrangement.

1.7 Research Objective & Thesis Structure

High Power Amplifier theory uses a simplified approach to derive the waveforms and hence performance characteristics of amplifier classes and operating modes. However, the design of power amplifiers has traditionally started from the impedance space and designing matching networks to deliver a specific set of impedances to a device.

This thesis seeks to address the design and development of high efficiency high frequency MMIC PAs using circuit techniques using RF-IV waveform information directly in the design process. Therefore, the first objective is to investigate high efficiency amplifier operating modes looking from a waveform engineering perspective and to understand the drivers affecting efficiency. The second objective is an investigation into methods to overcome these limiting mechanisms, leading to a design strategy suitable for MMIC implementation of high frequency PAs, with the focus of the work concentrated on transistor input driving networks and waveforms.

This thesis first presents the basic amplifier theory and operating modes. It develops this theory further by presenting an analysis on how the input circuit affects amplifier performance. This theory is practically demonstrated using large signal measurements on simple transistor cells leading to a novel concept for harmonic 'source injection'. The theoretical analysis of the source injection mode is presented, followed by validation measurements. The source injection mode is then applied to the design of a 2 stage PA demonstrator implemented in a GaN MMIC process.

Chapter 2 starts with a review on classic Amplifier operating modes looking in detail at PA behaviour from a device terminal current and voltage waveform perspective, along with the factors affecting efficiency.

Chapter 3 outlines the de-embedding processes required in future chapters to find the intrinsic waveforms either from measurements or for use in the circuit simulator to drive the design process. It details the extraction of the device element models and derives the parasitic elements required to effectively de-embed the waveforms.

Chapter 4 reviews the standard microwave amplifier simulation methods and presents a new waveform based approach which define the transistor terminal

waveforms directly, where the impedances are then derived for amplifier implementation.

Chapter 5 analyses the role of the input circuit on amplifier performance and the second harmonic source injection mode is proposed. The theoretical operation is presented and backed up with validation measurements.

Chapter 6 describes the design and evaluation of a two stage GaN MMIC PA demonstrator using the second harmonic source injection technique. The design of the interstage network to generate the required driving voltage waveform is presented.

Finally, Chapter 7 draws conclusions and summarises the thesis. In addition, future work and suggested extensions to this research are also presented.

2 AMPLIFIER OPERATING MODES

2.1 Amplifier operating modes

Amplifier modes are generally categorised by the bias voltage operating point, where the device is assumed to behave as a current source with a sinusoidal input drive e.g. classes A, AB, B and C. This bias point affects the output current conduction angle and differentiates the circuit operation. Further classification is possible by the device operating conditions indicating there are specific matching network conditions for operation e.g. class J and Class F [13] but use a Class B or AB bias point.

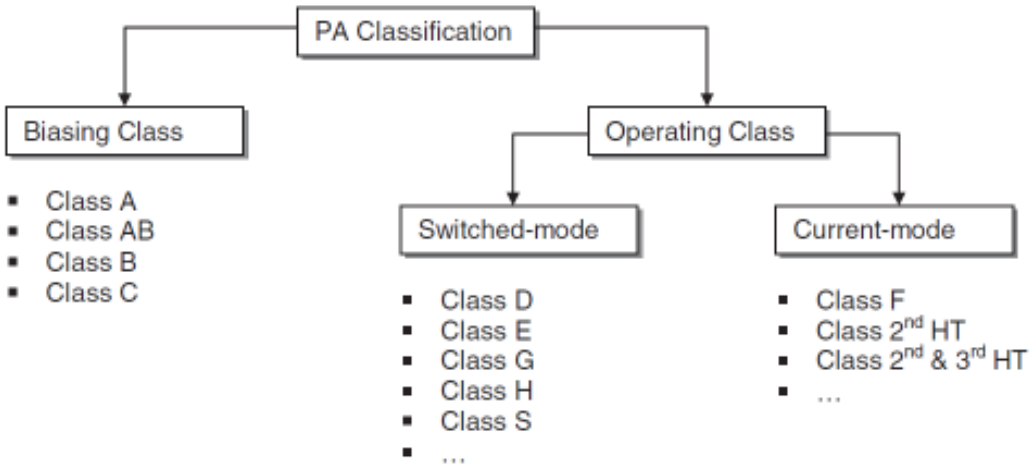


Figure 2.1 Typical PA classification as described by Colantonio et al. [13]

These operating modes can also be further expanded with the continuous mode theory, defining the class BJ continuum (covered later) and the continuous class F mode.

Inverse class amplifiers (e.g. class F^{-1}) are also possible where the voltage and current waveform are swapped.

More specifically the operating modes are described by the RF-IV waveform shapes at the output terminal, which is in part due to the bias point and part operating impedance environment.

2.1.1 Class A Amplifier

This is the simplest class of amplifier and is characterised by biasing a transistor at a quiescent bias point midway between the maximum current and pinch-off. The RF input signal is injected about this bias point. The resulting output current swings up to I_{max} and down to zero (Figure 2.2).

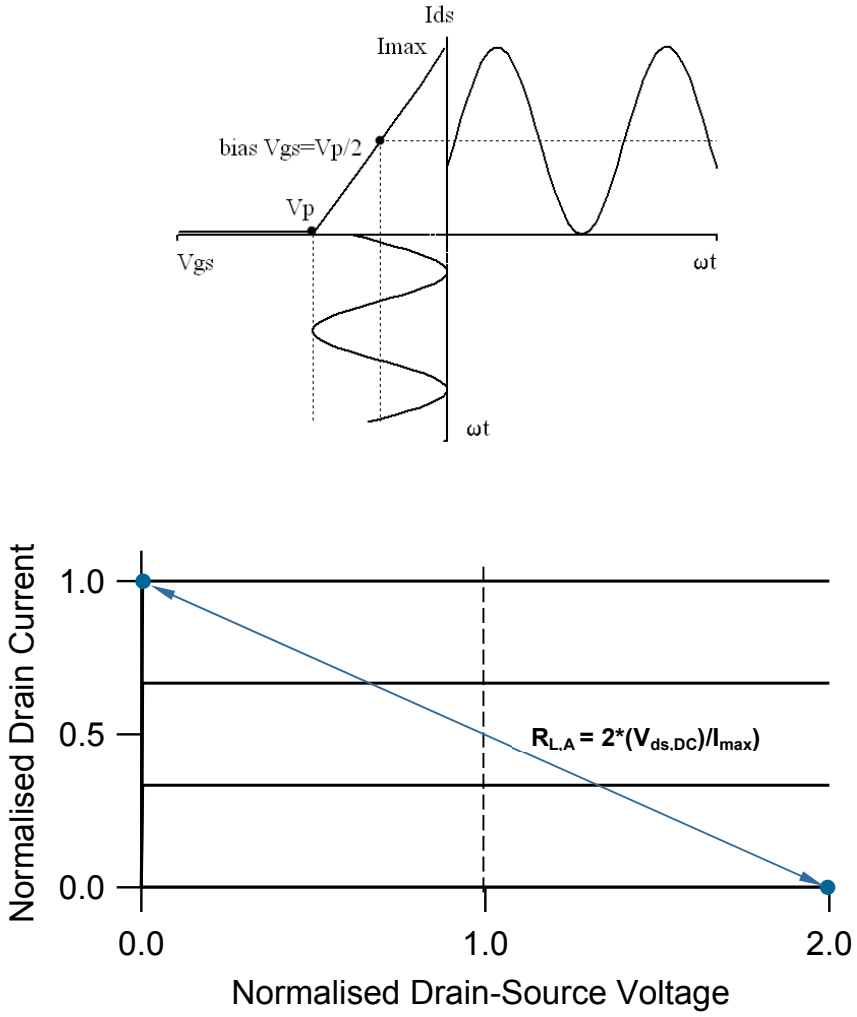


Figure 2.2 Class A operation (a) bias point and waveforms and (b) optimum load line

The ideal load for this configuration has been defined by Cripps [14] and is simply the ratio of the output voltage swing defined by the voltage supply, $V_{ds,DC}$, and the maximum device current, I_{max} (Figure 2.2)

$$R_{L,A,ideal} = \frac{2V_{ds,DC}}{I_{\max}} \qquad 2.1$$

Drain Efficiency, $\eta_{D,}$ is simply the ratio of fundamental RF output power to total DC power.

$$P_{out,RF} = \frac{I_{\max}}{2\sqrt{2}} \frac{V_{ds,DC}}{\sqrt{2}} = \frac{I_{\max} V_{ds,DC}}{4} \qquad 2.2$$

$$P_{DC,A} = \frac{I_{\max} . V_{ds,DC}}{2} \qquad 2.3$$

$$\eta_{D,A,ideal} = \frac{P_{out,RF}}{P_{DC,A}} = \frac{1}{2} \qquad 2.4$$

The maximum drain efficiency for this class of amplifier is 50% at full drive. This is the drawback of Class A configuration as the dc power is independent of drive level and efficiency during back-off is poor.

Another important parameter, often neglected in the literature dealing with amplifier operating modes, is the power gain, G_P. The power gain is defined here as the "available power gain" [15] of the device. The output power is the optimum power available from the transistor, before the amplifier exhibits any compression or non-linear characteristic - which is the basic assumption for linear power amplifier theory. The input power is assumed to be the power available from the source.

The power gain, G_P, for the Class A amplifier is simply the ratio of the output power to the input power, where the input power is assumed to be proportional to the input voltage amplitude, V_{in}^2 [15][16].

$$V_{in} \propto \left(\frac{\frac{1}{2}(V_{gs,\max} - V_P)}{\sqrt{2}} \right)^2 \qquad 2.5$$

$$G_{P,A} = \frac{I_{\max}(1-\beta)V_{ds,DC}}{4} \cdot \frac{1}{\left(\frac{\frac{1}{2}(V_{gs,\max} - V_P)}{\sqrt{2}} \right)^2} = \frac{2I_{\max}(1-\beta)V_{ds,DC}}{(V_{gs,\max} - V_P)^2} \qquad 2.6$$

2.1.2 Class B Amplifier

It is well understood that correct high efficiency power amplifiers design strategy involves the engineering of the output RF current and voltage waveforms. The reference design, Class A, was shown to have sinusoidal current and voltage waveforms (section 2.1.1) providing a theoretical maximum drain efficiency of 50%. To improve efficiency either one or both of these waveforms must be modified by the introduction of harmonics terminated in non-dissipating loads.

The Class B case requires the transistor biased and driven in a manner that provides a half-rectified current waveform. The classical approach to realizing Class B amplifier (sometimes called tuned load) operation [13][17] is achieved by biasing transistors at pinch-off, such that there is no quiescent current flow at the active device output in the absence of any input signal. The input RF signal is then superimposed on this dc bias level causing the active device to conduct during the positive excursions of the input signal, and forcing the device further into pinch–off during the negative cycle of the sinusoidal input signal. The resulting output current waveform is a half wave rectified sinewave (Figure 2.3). Fourier analysis of the current waveform (2.7) provides the detail on the relative amplitudes of the harmonic components.

$$I_{ds}(\omega t) = \frac{I_{\max}}{\pi} + \frac{I_{\max}}{2}\cos(\omega t) + \frac{2I_{\max}}{3\pi}\cos(2\omega t) + \ldots \qquad 2.7$$

The fundamental component of this current waveform is $I_{max}/2$, the same as for the Class A case, and, when terminating all the even harmonic components of this half-rectified output current waveform into short circuits, the output voltage waveform is sinusoidal, as for the Class A case, resulting in the same optimum load impedance and output power as given in (2.1) – (2.3).

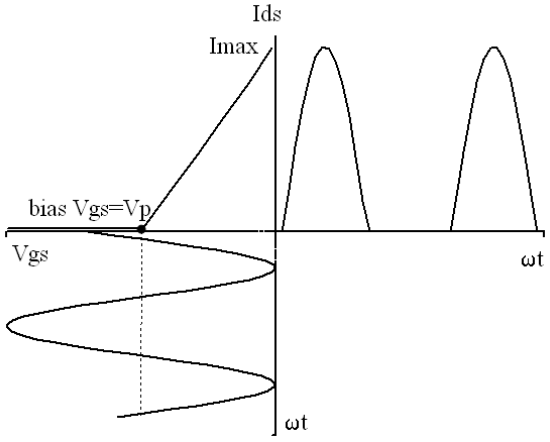


Figure 2.3 Class B operating point and waveforms

The dc component of the current waveform under Class B operation is I_{max}/π, hence the dc power is given by:

$$P_{DC,B,ideal} = \frac{I_{\max}.Vds}{\pi} \qquad 2.8$$

This dc power is lower than under the Class A bias and thus this mode of operation has the benefit of improved drain efficiency, by a factor $\pi/2$ (2.9), over the Class A case with no degradation in output power.

$$\eta_{D,B,ideal} = \frac{P_{out,RF}}{P_{DC,B}} = \frac{I_{\max}Vds/4}{I_{\max}Vds/\pi} = \frac{\pi}{4} = \frac{\pi}{2}\eta_{D,A,ideal} \qquad 2.9$$

Such a waveform has a fundamental current waveform component, and hence output power, identical to Class A but with a drain efficiency increased 78.5%.

This class of amplifier is part of the reduced conduction angle operating region. In between the Class A and Class B end points amplifiers are in Class AB.

2.1.3 Class C amplifier

The class C amplifier follows from an extension of the class A and B cases with the gate bias point reduced further to below the pinch-off voltage. This results in a smaller conduction angle as the gate voltage is above pinch-off for a reduced part of the drive cycle, Figure 2.4

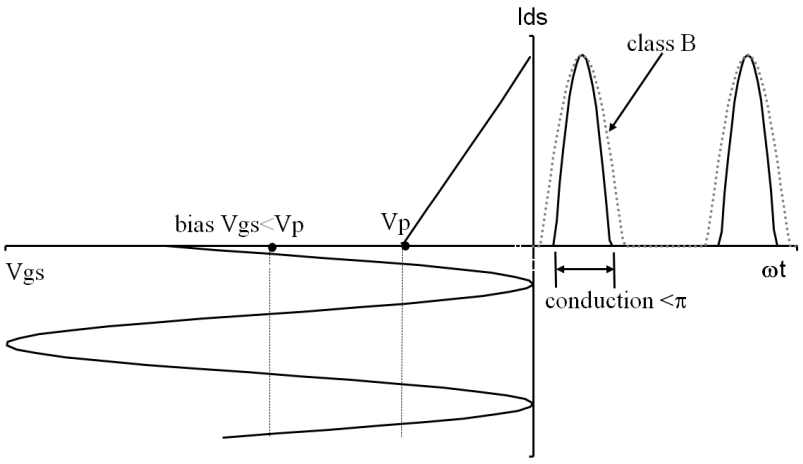


Figure 2.4 Class C operating point and waveforms

Here the current pulse is seen to be smaller than for the class B operating mode, with a conduction angle, α, less than π radians.

The expressions for the fundamental component of the drain current pulse and the dc component can be found from Fourier analysis of this drain current waveform [13][17] and are given by (2.10) and (2.11)

$$I_1 = \frac{I_{\max}}{2\pi}\left[\frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)}\right] \qquad 2.10$$

$$I_{dc} = \frac{I_{\max}}{2\pi}\left[\frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)}\right] \qquad 2.11$$

The efficiency is improved under this operating mode as shown in Figure 2.5, but a consequence of the reduced conduction angle operation is the lower output power achievable, which is discussed in section 2.1.7.

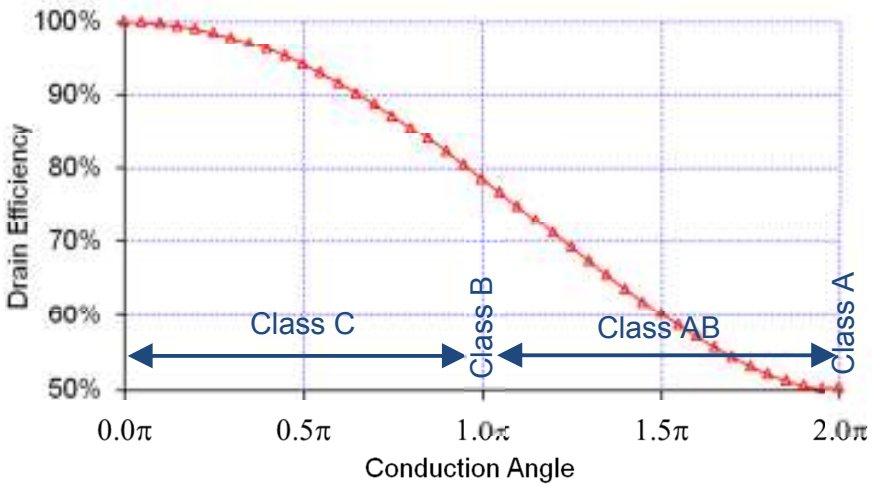


Figure 2.5 Efficiency versus conduction angle for reduced conduction angle operation.

2.1.4 Class J Amplifier and the BJ continuum

Relaxation of the output load harmonic impedances from the Class B short circuit case to include a 2nd harmonic reactive component (generally the device Cds) and a corresponding opposite reactive element to the fundamental load impedance is shown to deliver the same efficiency and power as the Class B operation. This mode of operation has been named Class J [17].

Recent work has expanded this theory leading to the Class BJ continuum [18] showing that the Class B and Class J modes are just the end points in a generalised theory relating the fundamental and second harmonic components at the output.

The waveforms can be simply described by the sum of two harmonics with a phase angle between them and results in the expression

$$V_{BJ}(\theta) = (1 - \beta\cos\theta)(1 - \alpha\sin\theta) \qquad 2.12$$

These waveforms are plotted in Figure 2.6 for varying α from α =-1 (Class J^{-1}) through α =0 (Class B) to α =+1 (Class J)

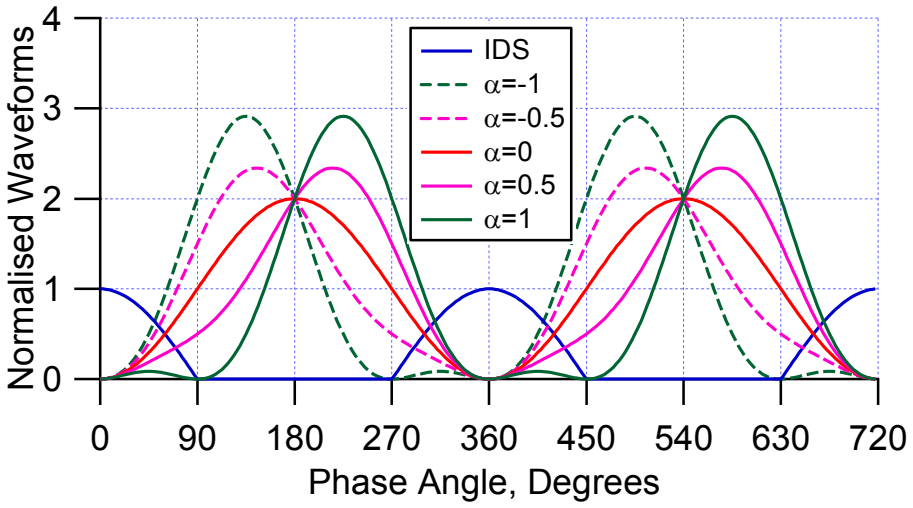


Figure 2.6 Class BJ ideal waveforms from (2.12) for varying α (β=1 in all cases) [18]

All these voltage waveforms, combined with the half sinusoidal current waveform, have the same power and efficiency as the classic Class B sinusoidal derivation. These operating points require different impedances at the fundamental (by including a reactive term) and the addition of a non-zero 2nd harmonic impedance.

The impedances are now defined as the ratio V/I for each of the harmonic components from (2.7) and (2.12) resulting in

$$Z_{Lf0,BJ} = R_L + j\frac{\alpha}{\beta}R_L \qquad 2.13$$

$$Z_{L2f0,BJ} = 0 - j\alpha\frac{3\pi}{8}R_L \qquad 2.14$$

The fundamental real impedance component, R_L, is identical to the Class A and B case. The reactive terms are clearly identified in (2.13) and (2.14) and how they are related to R_L with the Class J parameters α and β.

2.1.5 Class F Amplifier

Reduced conduction angle operation has been shown to improve efficiencies by effectively reducing the time when the current and voltage waveforms overlap (hence minimising dissipation). Further efficiency improvements can be made by selecting the output drain voltage waveform to be a square wave whilst maintaining the half wave current waveform, see Figure 2.7. This mode of operation (Class F) was originally demonstrated by Tyler for valve devices [26] and expanded upon by Snider [28].

In this mode a 100% theoretical efficient amplification can be achieved – but this assumes control of infinite harmonics. Generally the design procedure is considered by controlling the first three harmonics only. Raab has presented several papers reviewing the control of the harmonics for optimum waveforms [29][30][31][32] using a numerical approach.

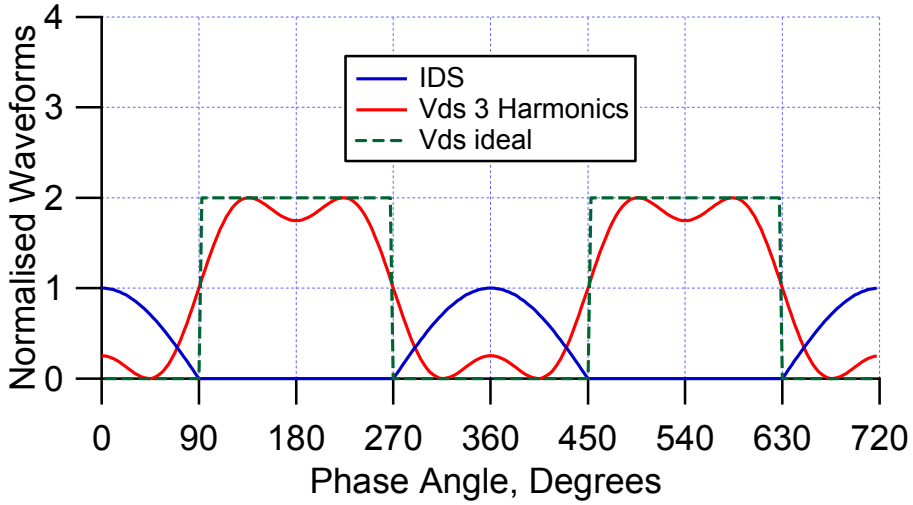


Figure 2.7 Class F ideal waveforms showing optimum square wave voltage and the 3rd harmonic approximation.

This class of operation uses the same basic bias point as Class B, although optimisation during the design procedure moves this point subtly by minimising the even harmonic current content.

The optimum fundamental impedance for the class F is defined by the peak fundamental voltage, which will be larger than the equivalent class B operating point. The value is $R*(4/\pi)$ for an ideal square wave. Practical values range from $1.125*R_{L,A}$

the maximally flat condition to 1.273*$R_{L,A}$ by optimising the voltage waveform shape and the number of harmonics to be controlled.

The harmonic terminating impedances are Z_L=0 for even harmonics and Z_L=∞ for odd harmonics.

Recent research developments on the continuous mode theory [39] have expanded this operating space to allow the use of a larger area of the impedance plane, to remove the need for the open and short circuit harmonic impedances.

2.1.6 Inverse Class F Amplifier

The inverse class F (Class F^{-1}) mode of operation just requires interchanged output waveforms with respect to Class F, i.e. a squared current waveform, containing only odd harmonic components, and a half sinusoidal voltage waveform, having only the fundamental and even harmonic components [13][38], leading to the basic requirement for a short circuit impedance at the odd harmonics and an open circuit at the even harmonics. This mode of operation will maintain the same efficiency as the class F mode.

The drain current waveform shape needs some consideration. In order to achieve the square current waveform, the amplifier needs to be overdriven, such that it causes the saturation condition.

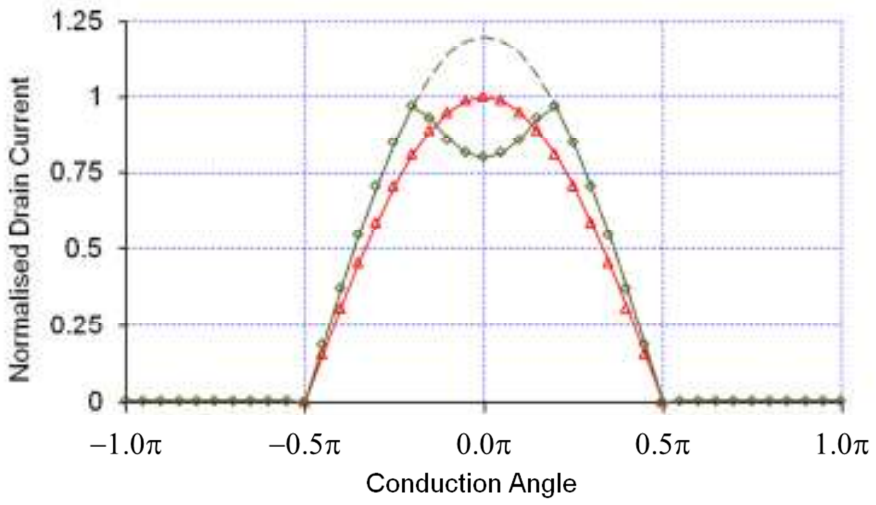


Figure 2.8 Class F^{-1} current waveform from an overdriven transistor.

This overdrive signal causes bifurcation of the drain current pulse at the peak amplitude [38] and, coupled with the pinch-off performance flattening the bottom of the current pulse, a quasi-square current waveform shape is created (Figure 2.8).

2.1.7 Power Utilisation Factor

One of the main, and not widely publicised, effects of reduced conduction angle operation is the varying RF output power. Moving towards Class C operation does indeed improve the efficiency but the output power drops. This is a delicate balance between the requirements for power and the gain of efficiency. A figure of merit, the 'Power Utilisation Factor' (PUF), has been defined [17] to quantify this effect which shows the output power relative to the Class A case. This is shown in Figure 2.9.

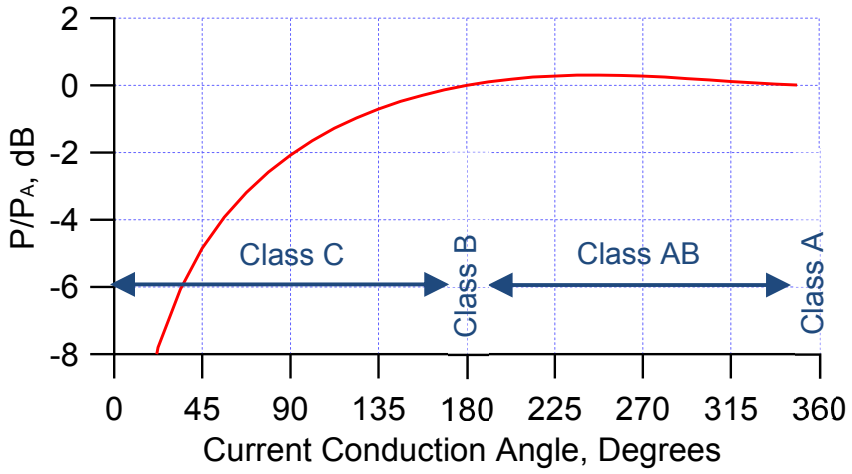


Figure 2.9 Power Utilisation Factor (PUF) for reduced conduction angle operation

The power output is the same for the Class A and Class B bias points and shows the classical increase in power in the Class AB range. The power drops significantly as the Class C operating region is entered.

2.2 Factors affecting Efficiency

The ideal waveforms and operating points discussed in section 2.1 explain basic amplifier operation and provide a basis for comparing the waveform requirements and the resulting efficiency gains, however, real transistor performance deviates from the simple linear theory of sections 2.1.1-2.1.6, and these affect efficiency. This section discusses these factors and identifies methods to reduce or alleviate the effects of these non-idealities.

2.2.1 Knee Voltage

The most notable difference is the inclusion of the knee Voltage, V_k, which modifies the Ids–Vds transfer characteristics (shown in Figure 2.10) to account for the limit on minimum drain voltages in real devices.

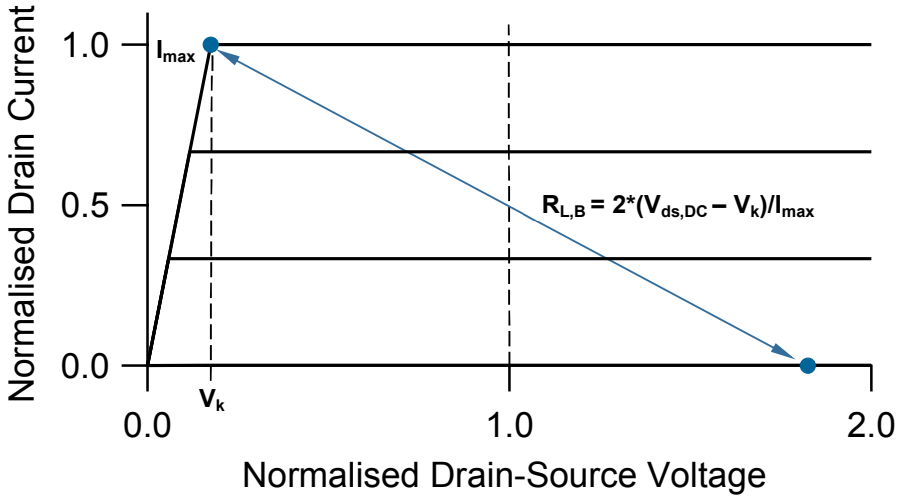


Figure 2.10 Class A operation optimum load line with knee voltage

Rewriting expression (2.1) for Class A load resistance with the knee voltage component gives (2.15).

$$R_{L,A} = \frac{2(V_{ds,DC} - V_k)}{I_{\max}} = \frac{2(1-\beta)V_{ds,DC}}{I_{\max}} \qquad 2.15$$

Where $\beta = V_k/V_{ds,DC}$, the ratio of knee voltage to DC supply voltage.

The RF fundamental voltage swing is correspondingly reduced by the knee voltage, so the fundamental output power is given by

$$P_{out,RF} = \frac{I_{\max}}{2\sqrt{2}} \frac{(1-\beta)V_{ds,DC}}{\sqrt{2}} = \frac{I_{\max}(1-\beta)V_{ds,DC}}{4} \qquad 2.16$$

The expressions for gain and Drain Efficiency, η_D, can be expanded to include this reduced fundamental RF output power. As the input power is unchanged, the knee voltage reduces gain and efficiency by the factor (1-β) as shown by (2.17) and (2.18).

$$G_{P,A} = \frac{I_{\max}(1-\beta)V_{ds,DC}}{4} \cdot \frac{1}{\left(\frac{\frac{1}{2}(V_{gs,\max}-V_P)}{\sqrt{2}}\right)^2} = \frac{2I_{\max}(1-\beta)V_{ds,DC}}{(V_{gs,\max}-V_P)^2} \qquad 2.17$$

$$\eta_{D,A} = \frac{P_{out,RF}}{P_{DC,A}} = \frac{1}{2}(1-\beta) = \eta_{D,A,ideal}\eta_k \qquad 2.18$$

This factor is especially detrimental when low supply voltages are used, as the β term increases towards unity. The response is shown in Figure 2.11.

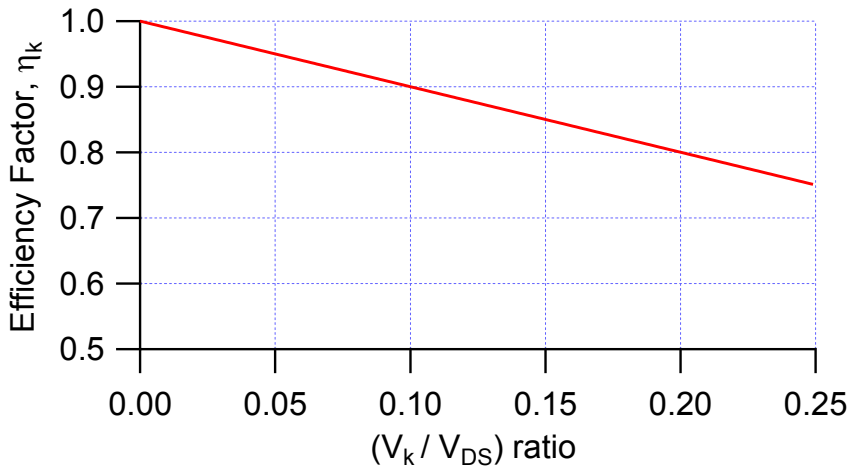


Figure 2.11 Knee voltage efficiency factor versus Knee to supply voltage ratio.

For the Class B case, the efficiency can also be modified to take account of the knee effect and this suffers the same degradation.

$$\eta_{D,B} = \frac{P_{out,RF}}{P_{DC,B}} = \frac{\pi}{4}(1-\beta) = \frac{\pi}{2}\eta_{D,A} \qquad 2.19$$

Gallium Nitride (GaN) has a lower carrier mobility, μ_n, than Gallium Arsenide (GaAs). This translates to the 'knee' voltage, V_k of the DC-IV curves in GaN transistors being higher than that of GaAs HEMTs, by the order of about 5 times. The critical factor in device operation however is ratio of Vmax to Vk allowing higher operating voltages which can compensate for the higher knee.

2.2.2 Device Gain

The discussion and analysis of the amplifier operating modes so far has involved the drain efficiency, η_D, as a measure of performance. An alternative and more relevant definition for efficiency, which also takes account of the device gain, is power added efficiency (PAE). This is the ratio of the total RF output power, less the RF input power, and divided by the total dc input power [7].

$$PAE = \frac{P_{out,RF} - P_{in,RF}}{P_{DC}} = \frac{P_{out,RF}}{P_{DC}}\left(1 - \frac{1}{G_P}\right) = \eta_D\left(1 - \frac{1}{G_P}\right) = \eta_D\eta_G \qquad 2.20$$

Here, the efficiency gain dependency can be clearly seen. For high power gain (G_P>>10), the (1-1/G_P) factor, η_G, has little effect and the PAE is almost equal to the drain efficiency. However, when this power gain value drops to 10dB and below the PAE is affected significantly. For example a 10dB power gain results in a 90% factor of η_D (Figure 2.12).

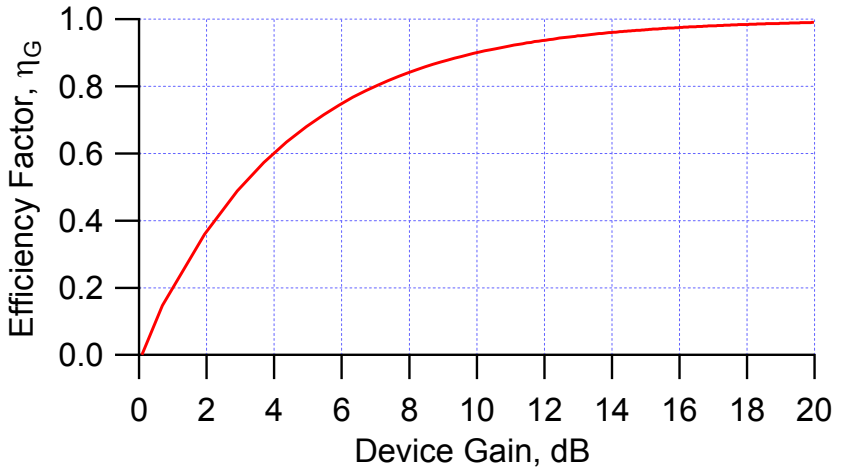


Figure 2.12 η_G (=PAE/Drain efficiency) factor versus device power gain

This factor is a considerable problem at high frequencies, where device gain is lower, and for power amplifier design, where the power gain is further reduced due to the effect of compression, which is more pronounced in the GaN technology.

2.2.3 Matching network loss

The design of any amplifier requires the termination of the fundamental and harmonic components into defined impedances using some form of circuit network. Practical realisation of these matching networks will add some losses, from the resistivity of the conductor metal layers and the dissipation factor (tan δ) of the substrate and capacitor dielectric layers. These losses are often forgotten (or neglected) during the initial design process, where the implementation is described using ideal circuit elements, but their impact on circuit design needs to be considered.

Losses in the output network are more detrimental to efficiency than if they were to appear at the input in PA design. Minimizing of these losses at the output of PAs is therefore key to maintaining high efficiency.

The effect of the losses on the drain efficiency versus output matching network loss is shown in Figure 2.13. As an example, a 0.2dB loss translates to a 96% efficiency factor.

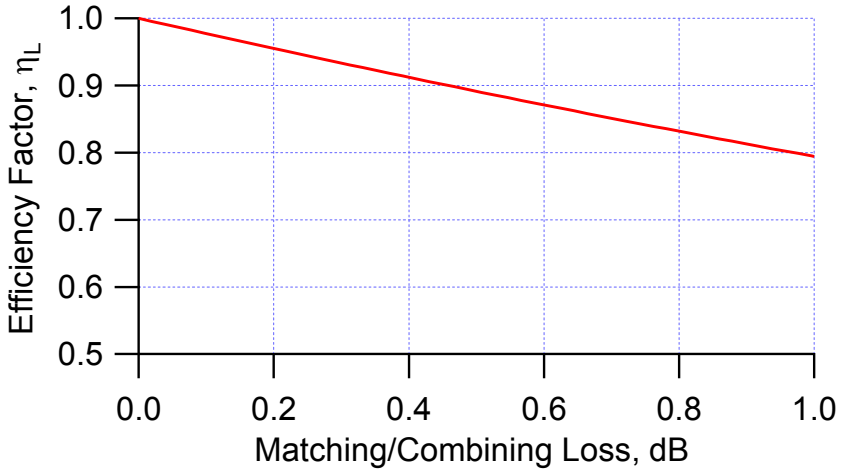


Figure 2.13 Efficiency factor versus output combining losses

2.2.4 Overall impact of efficiency factors

The overall effect of these factors is multiplicative such that the overall realisable efficiency is dramatically reduced from the ideal value. In order to illustrate this some typical values are chosen, for a GaAs process:

Knee voltage 1V for a 9V operation $\Rightarrow \eta_k = 0.89$

Gain = 10dB $\Rightarrow \eta_G = 0.9$

Output Matching circuit loss = 0.2dB $\Rightarrow \eta_L = 0.96$

PAE = $\eta_{ideal.}\ \eta_{k.}\ \eta_{G.}\ \eta_L$

Considering Class B operation with a theoretical efficiency of 78.5%, the actual achievable PAE is (78.5%).(0.89).(0.9).(0.96) = 60.4% which is a significant reduction from the starting point. This illustrates the need to manage these factors in any design approach.

2.3 Multistage amplifiers

The factors described so far are mainly related to individual transistor amplifier stages. Generally high frequency amplifiers involve multiple stages, with the most common approach confined to two stages. Under these conditions the PAE must also account for the dc consumption of the driver stage(s).

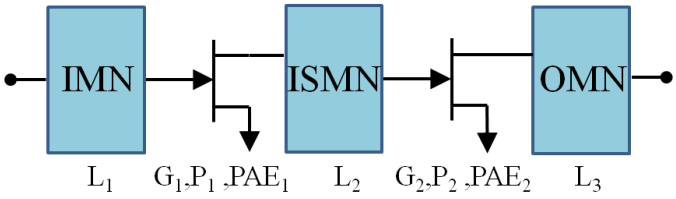


Figure 2.14 Two stage amplifier block diagram showing efficiency contributions.

The amplifier total PAE can be derived from the individual stage performance [58] as shown in (2.21)

$$PAE_{total} = \frac{PAE_1.PAE_2(L_1L_2L_3G_1G_2 - 1)}{PAE_1L_1L_2G_1(G_2 - 1) + PAE_2L_1(G_1 - 1)} \qquad 2.21$$

The response is plotted in Figure 2.15 for the simple case of lossless matching networks (L1,L2,L3=1), fixed and equal amplifier stage gain (G1=G2=10dB) and variable PAE1 and PAE2.

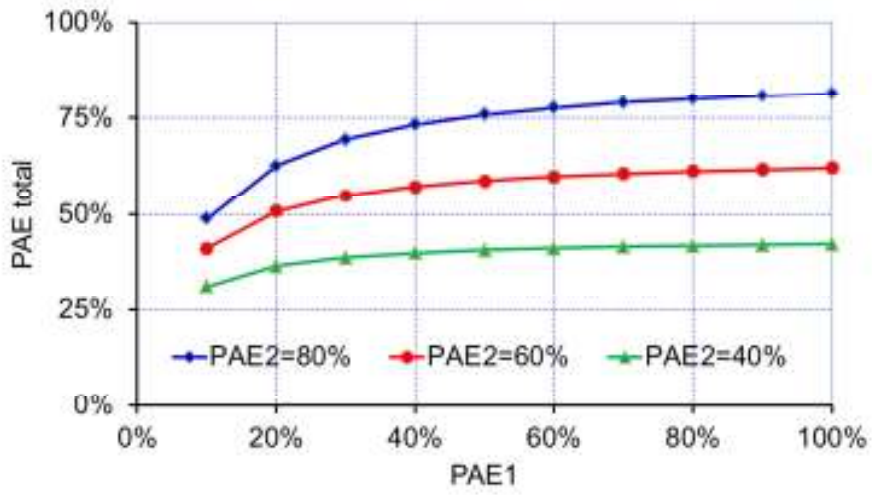


Figure 2.15 Effect of driver amplifier efficiency on overall amplifier PAE for G1=G2=10dB.

2.4 Conclusion

This chapter has described the operating modes of typical amplifiers and outlined the factors which need to be considered to maintain high efficiency, with a particular focus on high frequency operation. High efficiency modes are shown and the demands of the matching network impedances are identified, and it is clear that these modes are defined in terms of the output waveforms only.

The influence of gain on efficiency is obviously evident from the PAE reduction due the device gain and also any losses after the device. This is compounded in the two stage amplifier design, where the overall PAE is a function of both stage efficiencies and gains.

3 WAVEFORM DE-EMBEDDING

The design and analysis of PAs requires knowledge of the RF-IV waveforms as described in chapter 2. These waveforms are all referenced to the 'intrinsic' transistor device planes. That is, the device current generator plane at the output and the gate controlling node at the input (in the case of FET technology). A simple model to describe this situation is shown in Figure 3.1(a) where the main intrinsic device elements are identified. This model has limited usefulness in this form, for example low frequency operation and/or very small unpackaged devices. A better model is required to capture the full performance of the transistor.

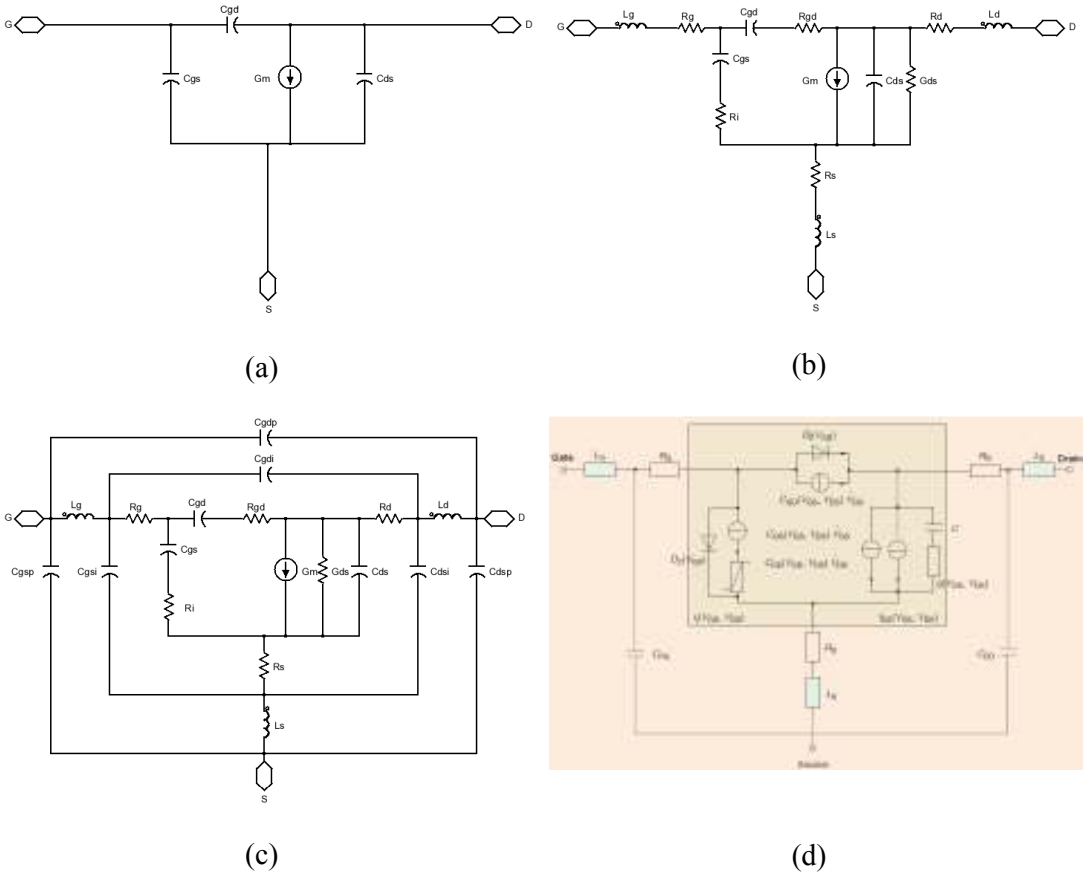


Figure 3.1 equivalent circuit models for FET technology (a) simple low frequency model, (b) basic Small signal model, (c) Improved small signal model to account for distributed effects and (d) non-linear model [59] version of model (c).

Practical devices have this intrinsic transistor structure embedded inside a parasitic 'shell' [59],[60],[61] which includes elements arising from the physical size of the device, and the connection to the outside world by bond pads, bond wire interconnects

and/or packages. A more complete device model, combining the basic extrinsic parasitic elements and the intrinsic core, is shown in Figure 3.1(b)

The device model is further refined by capturing the distributed effects of larger devices by including more parasitic elements. This improved model for a FET based transistor is shown clearly in Figure 3.1 (c) and (d). The origin of these parasitic components is due to the physical geometry and the access structures in the realisation of the devices [62],[63]. The capacitive elements are due to the coupling between the electrodes and metal features on the surface of the semiconductor. The inductance is due to the length of the device interconnects and the resistance is due to the finite interconnect and gate metallisation conductivity and the semiconductor Ohmic contacts. Clearly, as device sizes increase the capacitive coupling and inductance increase in accordance with standard scaling rules but the biggest problem is capturing the emergent distributive effects that appear. This leads to a more complex model.

Understanding these parasitic elements is paramount in defining the voltages at the intrinsic device reference planes by de-embedding any measurements or simulations which will be measured at an external reference plane. It will also be shown to play a role in defining the matching networks to present the correct impedances or voltage waveforms at these intrinsic planes.

The approach discussed in this section will concentrate on the approach and models for GaAs/GaN MMIC applications but the process and theory are equally valid for packaged devices and for different transistor technologies.

3.1 Calibration and de-embedding

Measurement of transistor device RF voltage and current waveforms (or more generally any vector measurements) are typically referenced to a measurement plane. This measurement plane can be calibrated and the resulting measurement is for the Device Under Test (DUT). Depending on how the transistor is connected to the measurement system, a number of calibration steps (tiers) may be required in order to shift the measurement reference plane to the device intrinsic plane [64].

The measurement reference plane is generally the package leads or, for the case of MMIC application, RF-on-Wafer (RFOW) probe pads (Figure 3.2). This is the point at

which measurement systems are calibrated [64] and thus the measurement data are fully error corrected. Methods are available to calibrate to arbitrary reference points up to the Device-Under-Test (DUT) using TRL, SOLT and LRM methods [66],[67],[68],[69]. These methods require the use of specific calibration standards fabricated on the substrate, test fixture or wafer at the same time as the test device or circuit. The remainder of this section will concentrate on the wafer level application.

In the case of this work, using the Cardiff University Active Load Pull system (ALPS) and the Vector Network Analyser s-parameter measurement systems, the RF-on-Wafer measurements are performed on a Cascade Microtech Summit® probe station using standard commercial Ground-Signal-Ground (GSG) probes. Calibration of these systems is performed using LRM 'standards' available from the Impedance Standard Substrate (ISS) [70],[71]. This enables 10-term error corrected measurements upto the Ground-Signal-Ground (GSG) probe tips. The next step is to 'de-embed' these measurements back to the extrinsic device using data for the test transistor GSG probe pads and any interconnection lines, then to further de-embed to the intrinsic reference plane by removing the device parasitic elements.

After calibration, the Cardiff University ALPS [72] allows de-embedding s-parameter files to be uploaded to shift the reference planes to the intrinsic device for real time de-embedded measurements. Alternatively, the de-embedding can be performed offline using a data viewer or CAD tools by manipulating the raw measurement data.

3.2 De-embedding measurement data

The process of de-embedding measured data can be accomplished by manipulating the s-parameters of the DUT and interconnection networks. The test fixture (or embedding network) and the DUT must, therefore, be represented in a convenient form. For this case, the de-embedded measurements can be post-processed from the measurements made on the test fixture and DUT together [73].

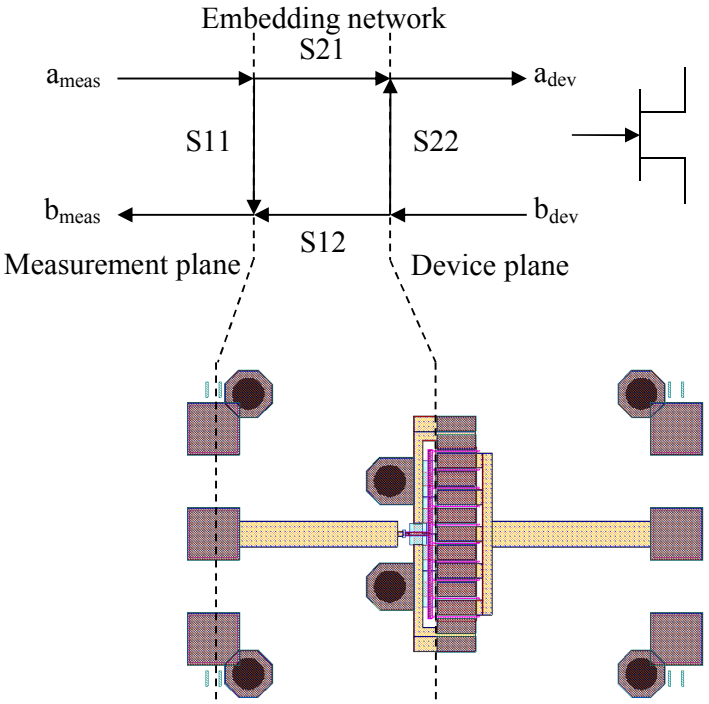


Figure 3.2 Definition of measurement planes and de-embedding networks for measurements on a MMIC circuit. The input circuit is shown explicitly. The output circuit is defined in the same manner.

Using the s-parameters, the a_{meas} and b_{meas} waves are known (measured) at the measurement plane (see Figure 3.2). If the s-parameters of the embedding network are known then it is a simple algebraic method to get back to the device plane a and b waves (a_{dev} and b_{dev}). Here these measurements can be used to find the device s-parameters or to reconstruct the device plane waveforms. In the case of the waveforms, this needs to be performed for the full frequency range, or more precisely, for all the harmonic components of the waveform we will be measuring. This approach is

described by referring to Figure 3.2 which shows an RF-on-Wafer transistor cell embedded between the GSG probe pads and interconnecting transmission line. The probe pads and transmission line are defined by an s-parameter block. The resulting equations define the approach for the input circuit but the output terminal is dealt with in an identical manner. The device a and b waves are shown in (3.1) and (3.2) in terms of the measured data and the embedding network (the GSG pad and transmission line) s-parameters.

$$a_{dev} = a_{meas} S_{21} + b_{dev} S_{22} \tag{3.1}$$

$$b_{meas} = a_{meas} S_{11} + b_{dev} S_{12} \tag{3.2}$$

rearranging 3.2 in terms of b_{dev}

$$b_{dev} = \frac{(b_{meas} - a_{meas} S_{11})}{S_{12}} \tag{3.3}$$

And inserting (3.3) into (3.1) yields

$$a_{dev} = a_{meas} S_{21} + \frac{(b_{meas} - a_{meas} S_{11}) S_{22}}{S_{12}} \tag{3.4}$$

So that the de-embedded waves a_{dev} and b_{dev} are found as a function of the measurement plane a and b waves (or voltage and current waveforms) and the s-parameters of the embedding network.

In the large signal time domain measurement system, the voltage and current waveforms are translated into an s-parameter format at the measurement plane, then each harmonic frequency element is de-embedded as above.

The resulting de-embedded device plane a_{dev} and b_{dev} waves can be converted back to the Voltage and Current waveforms using the standard s-parameter equations [15].

$$a_{dev} = \frac{1}{2\sqrt{R_s}.(V + Z_0 I)} \tag{3.5}$$

$$b_{dev} = \frac{1}{2\sqrt{R_s}.(V - Z_0 I)} \tag{3.6}$$

Rearranging leads to

$$2a_{dev}\sqrt{R_s} = (V + Z_0 I) \quad 3.7$$

$$2b_{dev}\sqrt{R_s} = (V - Z_0 I) \quad 3.8$$

Adding or subtracting 3.7and 3.8 leads to a solution for voltage and current at the device

$$V_{dev} = \sqrt{R_s}(a_{dev} + b_{dev}) \quad 3.9$$

$$I_{dev} = \frac{\sqrt{R_s}(a_{dev} - b_{dev})}{Z_0} \quad 3.10$$

Correct choice of the data to de-embed can, therefore, allow the voltages at the device extrinsic reference plane to be derived easily.

Having knowledge of the transistor parasitic elements, and including them in the de-embedding circuit, allows determination of the intrinsic reference plane waveforms. By including the Drain capacitance Cds and other inductive and resistive parasitic elements from the drain terminal into the de-embedding file the current generator plane response is found. Similarly, the gate resistance and inductance, Rg and Lg, can be included at the input if we want to determine the intrinsic device gate-source controlling node waveforms.

3.3 Determination of de-embedding networks

Because of the variety of substrates, wafers, printed circuit types and general test fixture designs, there are no simple textbook formulations for creating an exact model of the embedding network. Looking at the whole process of de-embedding, the most difficult part is creating an accurate model of the test structure [73].

Inspection of the typical device MMIC test cell structure (Figure 3.2) shows that the transistor is embedded between two GSG probe pads by a length of transmission line at the input and output. On-wafer measurements of these devices will therefore include the parasitic effects of the probe pads and interconnections. In order to extract actual Device Under Test (DUT) parameters from the measurements, several on-wafer calibration test structures such as open, short, and thru are normally required [74]. This

can be accomplished by the methods as stated in section 3.1. This is wasteful of chip area and, when implemented, is usually dedicated to characterisation masks used to define the specific process models. Alternative techniques are available which use a simplified process with a reduced requirement on the number of standards [75],[76],[77].

The process outlined by Cho [76],[77] uses a transmission line thru and an open as the standards to allow a calculation of the phase constant of the line based on the ABCD matrix of the line. The line lengths are then applied to the interconnections to de-embed the input and DUT connecting output lines. A similar approach is taken by Mangan [75] using two 'thru' lines to calculate the phase constant of the transmission lines along with a lumped admittance model for the bond pad to create a model for the embedding lines. This approach has been used also by Cha [74] who creates bond pad and interconnect equivalent circuits to extract the de-embedding network from measured s-parameters using the optimization routines in widely used CAD simulators (e.g. ADS).

The application of this approach for test fixture measurements is detailed in [73] with a model created by optimizing a computer simulation based on a series of measurements made using the actual test fixture. A coax-to-microstrip transition is modelled as a lumped series inductance and shunt capacitance, with the values optimized using the measured results from a straight microstrip thru line placed in the test fixture as shown diagrammatically in Figure 3.3

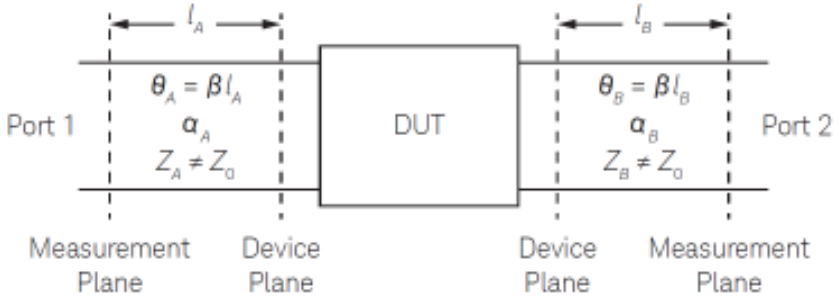


Figure 3.3 De-embedding using lossy transmission line modelling the test fixture [73]

The approach to optimise the transmission line parameters relies on the microstrip line model within the CAD tool (ADS®) rather than solution of the ABCD matrix for the lossy transmission line parameters [75],[76],[77].

A hybrid approach using these two main methods can be taken to define the de-embedding network parameters for the transistor Compound Photonics 10x75 µm test cell shown in Figure 3.4.

Figure 3.4 MMIC test cell photograph from RFMD FD30 mask 58029.0001.001 MM1465A showing a 10x75µm transistor test cell and the RF 'thru' calibration structure.

The transistor is seen to be between two equal length (300µm x 50µm) and symmetrical interconnection lines and GSG pads. Also shown in Figure 3.4 is the 'thru' line, equal to twice the interconnection line length (600µm x 50µm).

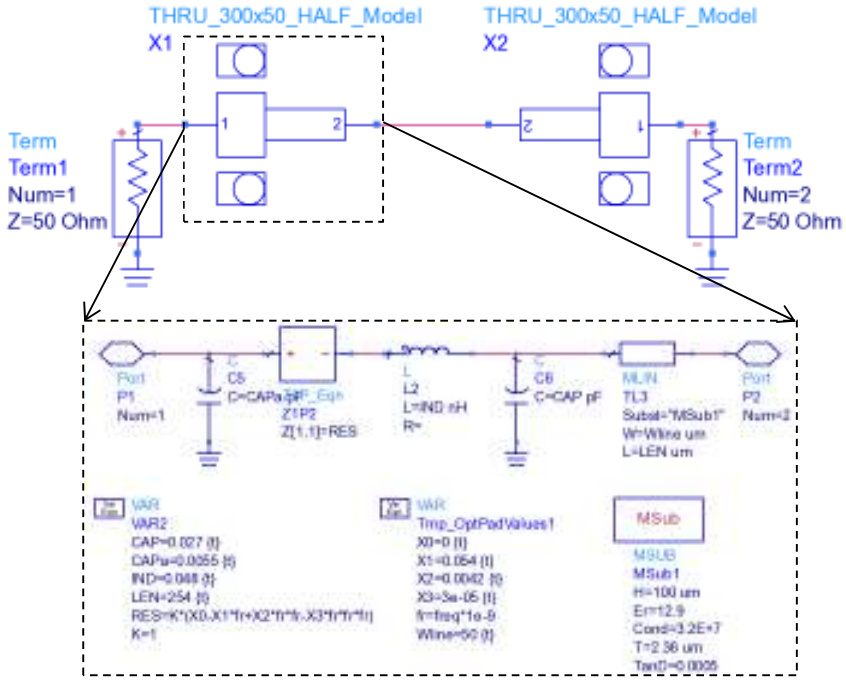


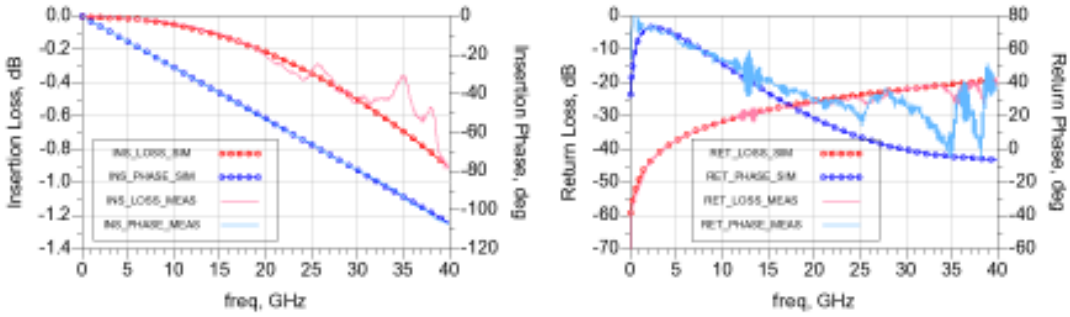
Figure 3.5 Embedding network equivalent circuit showing detail of the 'thru' half circuit.

An equivalent circuit can be constructed based on two back-to-back 'half circuits, comprising a single GSG pad and half the line, which when fitted to the measured data

allows a de-embed file of the input and output connection lines. The GSG probe pad is modelled as an equivalent 'Pi' network and the transmission lines are defined using the CAD tool microstrip line model on GaAs substrate, Figure 3.5. Two of these GSG/line half circuits are connected together and the parameters optimised to match the measured data. The resulting element values show a slight change from the physical line parameters (length of 288µm rather than 300µm) to match the insertion phase correctly.

The resulting response of the equivalent circuit compared to the measurements for the full line is shown in Figure 3.6.

This approach has been shown to deliver excellent results to 20GHz on MOSFET technology [76] and on pHEMT MMIC processes to frequencies above 35GHz [79], allowing the reference plane to be placed in the centre of the back to back line by taking one 'half circuit' for use as the de-embedding file.



(a) (b)

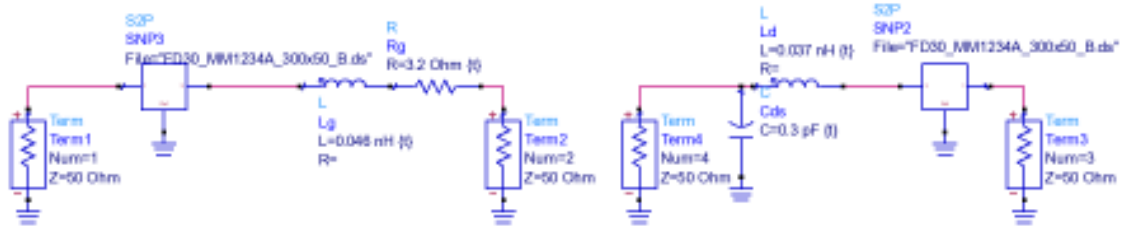
Figure 3.6 Embedding circuit and response (a) Insertion Loss measurement versus equivalent circuit (b) Return Loss measurement versus equivalent circuit

3.4 De-embedding to the intrinsic device plane

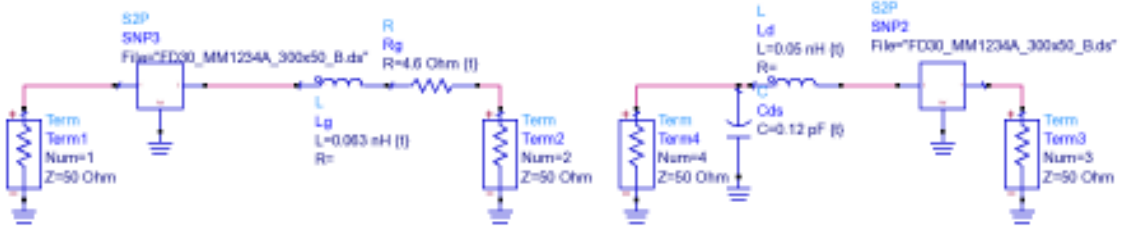
Section 3.3 showed the ability to define a de-embedding network to get to the transistor extrinsic planes, from the transistor test cell, by just removing the interconnection lines and probe pads. If these de-embedding files also include the device parasitic elements, the de-embedding moves to the intrinsic plane.

To perform de-embedding during initial simulations in common CAD tools the extrinsic parasitics can be determined by inspection of the foundry PDK values. These are the only values required in the simulator[3] and will give ideal correction for the device models used. The resultant voltage and current waveforms will then be those at the intrinsic plane.

It should be noted here that at the start of this work this was the only way to obtain the intrinsic waveforms. Subsequently, the increasing use of waveform engineering techniques for the design of amplifiers has shown the need for intrinsic waveforms and device models have recently become available [78] which have nodes allocated to view these waveforms directly in the simulator.



(a)



(b)

Figure 3.7 FD30 device de-embedding to intrinsic reference planes, the input Gate-Source controlling node and the output current generator plane, for (a) 10x75 device and (b) 4x75 device under bias conditions of Vds=+9V, Vgs=-1.1V.

[3] There is no requirement in the simulator to have feed lines and probe pads. The extrinsic plane is defined by the model directly.

Waveform measurements on real devices however require the parasitic elements to be determined fully, so that accurate de-embedding to the intrinsic plane can be performed.

3.4.1 Determination of device parasitic elements

Several methods are available to extract the device small signal model element values, although strictly for application here, the only values actually required for the de-embedding files are the 'extrinsic' elements. For MMIC applications the transistor test cells are included on the wafer in a probeable configuration, for example coplanar connections, or as discussed above, in a transmission line network (Figure 3.4). A model extraction procedure can follow by performing various measurements across a range of bias conditions.

Conventional measurements usually start with a dummy device having only bond pads without the device present. This allows simple Y-parameter subtraction of the pad parasitics and the resulting data are that for the device alone [80].

$$[Y_{device}] = [Y_{DUT}] - [Y_{open}] \qquad 3.11$$

This is adequate for devices which are small or working low enough in frequency such that any series parasitic elements do not have an impact on the performance so that a basic 'π' network can define the DUT and test structure [81]as shown in Figure 3.8.

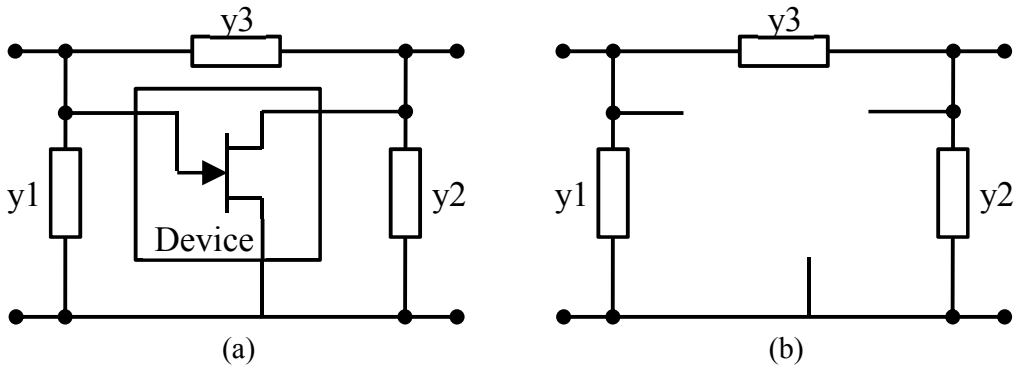


Figure 3.8 Device equivalent circuit model showing parallel parasitics [81]and equivalent circuit for bond pad interconnects.

Improvements in this method to account for the series parasitic elements as well have been used [82]. This takes initial measurements of the probe pads using the dummy 'open' structure which can be removed from the Y-matrix. The resulting network is transformed to a Z-matrix format where measurements of a 'short' standard

are removed. This does require the addition of specific coplanar FETs and for dummy structures to be included on the wafer.

It should be noted that the work in [82][80] was derived using bipolar processes where the active devices are relatively small. Applying this to GaAs or GaN transistor processes is difficult as the device sizes are much larger (especially for power applications) and creation of the short or open structures need to modification of the transistor cells (Figure 3.9) leading to two main problems:

1. Definition of the reference plane. What is removed as a parasitic element and what is part of the transistor and needs to be included in the small signal model.
2. Commercial foundry design rules can make custom FET cells difficult as they are not direct from the library, hence not validated by the process engineers.

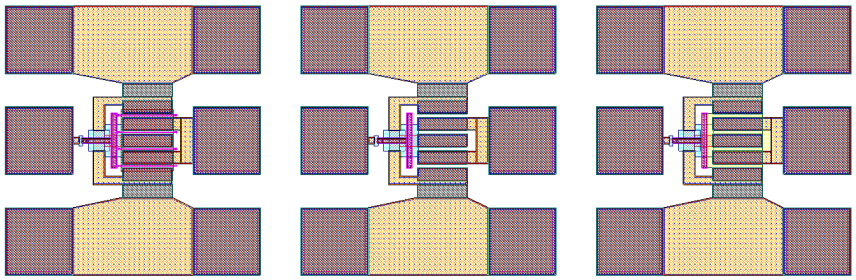


Figure 3.9 Cell layouts for the de-embedding of FET parasitic elements. (a) Full FET layout (b) FET 'open' (all gates removed and (c) FET short (gates shorted to Drain and Source after Koolen [82])

Taking the available test cell devices on the Compound Photonics FD30 GaAs MMIC process, this approach is not possible. Any resulting approach needs to use the feed line arrangement to use for measurements and extract the model parameters.

Extraction of the FET equivalent circuit parameters needs to consider both the constant, bias independent extrinsic elements and the bias dependent intrinsic part. Most extraction strategies is performed in 2 steps, one for each of the parts of the model.

Using the generic equivalent circuit shown in Figure 3.10, the extrinsic parasitic shell and intrinsic core are clearly seen [83]. Extrinsic parameters are grouped into the parasitic 'Y' shell comprising the bond pads and capacitances, the parasitic Z-shell with the series elements and the π-network intrinsic core. This model is for simple FET layouts on wafer and a more complex model is required for either high frequency

operation or large multi-finger devices to capture the distributed effects of the finite size of the device [83][84][86].

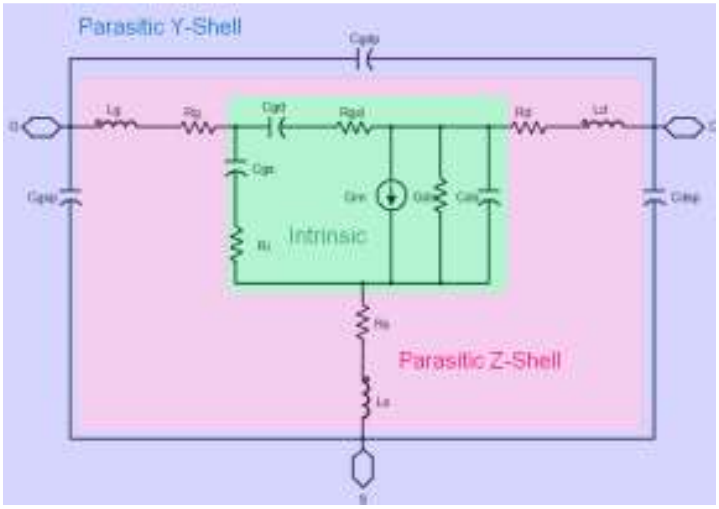


Figure 3.10 FET equivalent circuit showing the extrinsic parasitic shells and the intrinsic core [83]

The model shown in Figure 3.10 shows a modified model with additional parasitic elements more suited to large multi-finger devices.

The determination of the extrinsic parameters such as parasitic resistances and reactances are generally extracted based on 'cold' FET s-parameter measurements [87][88][90], both using reverse gate bias (pinch-off) and forward gate bias. Applying a large negative gate bias in excess of the pinch-off voltage and keeping the drain at 0V Vds, turns the intrinsic device off and the resulting low frequency equivalent circuit is a passive π-network, Figure 3.11.

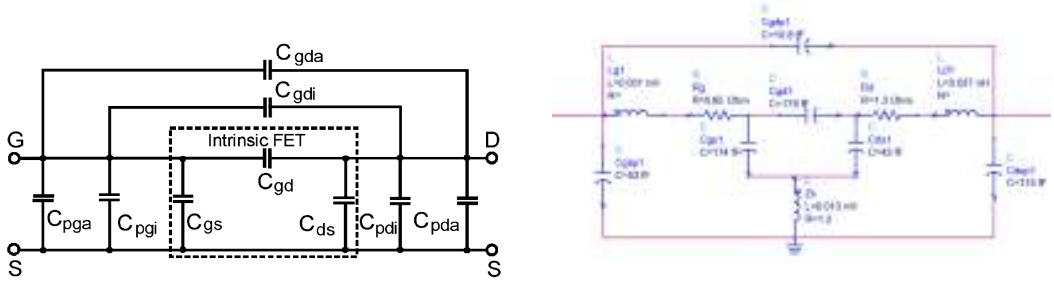


Figure 3.11 Equivalent circuit for the Cold FET (a) low frequency equivalent circuit [85] (b) full circuit.

3.4.2 Parasitic Y shell element extraction

Taking s-parameter measurements in the cold FET bias state, the capacitances can be determined from the resulting low frequency Y-parameters using the definitions shown in Figure 3.12.

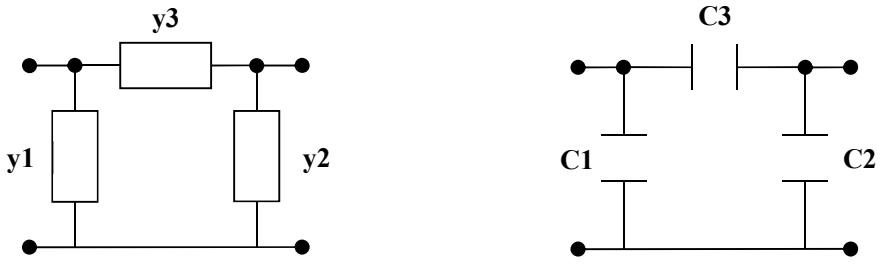


Figure 3.12 Network representation of a cold FET device (a) π circuit equivalent showing admittances (b) π circuit equivalent for capacitive element extraction.

Using the Y-parameter matrix representation of a π section of Y components connected, Figure 3.12(a), can be written as 3.12.

$$[Y_{ext}] = \begin{bmatrix} y1+y3 & -y3 \\ -y3 & y2+y3 \end{bmatrix} \qquad 3.12$$

Where [Yext] is the measured Y-parameter set for the cold fet. Rearranging, the values for y1, y2 and y3 can be determined, hence:

$$y1 = Y_{11ext} + Y_{12ext} \qquad 3.13$$

$$y2 = Y_{22ext} + Y_{21ext} \qquad 3.14$$

$$y3 = -Y_{12ext} = -Y_{21ext} \qquad 3.15$$

And this matrix can be reduced to the simple capacitive form, Figure 3.12(b), for element values (which should be independent of frequency) so that

$$C1 = \frac{imag(y1)}{\omega} \qquad 3.16$$

$$C2 = \frac{imag(y2)}{\omega} \qquad 3.17$$

$$C3 = \frac{imag(y3)}{\omega} \qquad 3.18$$

The device used for investigation is a ten finger, 75 µm Unit Gate Width (UGW) device (10x75µm) from the Compound Photonics FD30 MMIC foundry process. Taking s-parameter measurements under the cold FET bias condition (Vds = 0 V, Vgs = -5 V) and converting into a π-network equivalent circuit as defined by Figure 3.12 and equations (3.12) to (3.18) provides the results shown in Figure 3.15. Using the low frequency (1GHz) data points, the three capacitive elements Cgsp, Cgdp, Cdsp have values of 244 fF, 191 fF and 166 fF respectively.

freq	Cgsp	Cgdp	Cdsp
1.000 GHz	244.4 f	191.7 f	166.5 f

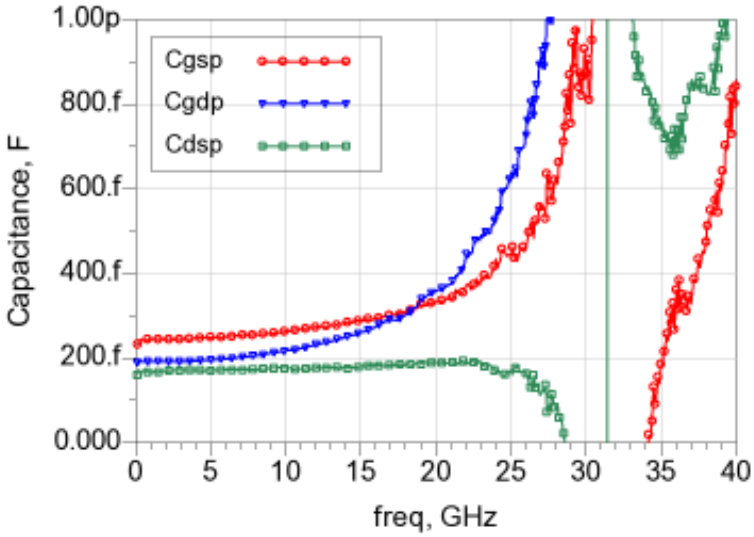


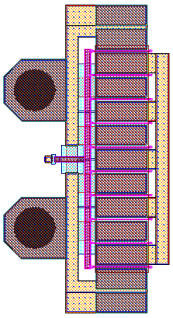
Figure 3.13 Extracted π-capacitance matrix for the 10x75 FD30 COLD pHEMT measurements.

The problem encountered by the extraction technique is to distinguish between the extrinsic capacitances and the intrinsic capacitances of the Cold FET model. Inspection of the cold FET model shown in Figure 3.11 reveals all the capacitances appear in parallel, thus the measurement only provides information on the total capacitance in each branch of the pi network. To overcome this, initial estimates on the ratio of capacitances has been proposed [85] and then the equivalent circuit is optimised to match the measured data with a set of predetermined rules.

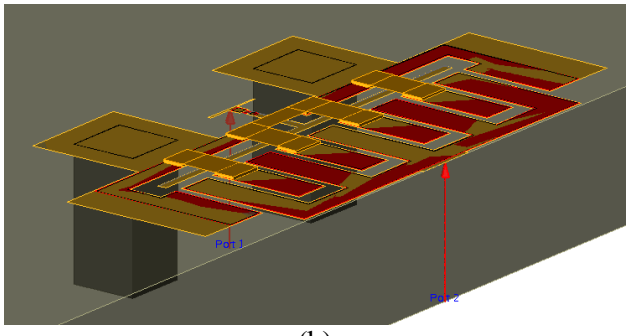
A unit cell approach [91] has been used to model the distributed nature of the device to allow scalability of the model and capture the high frequency effects.

Other researchers have used electromagnetic simulation methods to identify the distributed nature of the transistor and the parasitic structures in the device model [92][93]. These techniques split the transistor across a number of 'elementary intrinsic devices' or across different element groupings according to scaling rules, further reinforcing the distributed nature of the device.

An approach based on electromagnetic simulation is proposed here. This method takes account of the physical dimensions directly and does not require any prior assumption of the element values. The use of Electromagnetic Simulation tools allows the response of arbitrary shaped geometries to be performed. Taking the geometry from the foundry PDK transistor layout artwork and analysing the metallisation allows an accurate estimation of the inter-electrode and metallisation crossover capacitances, which can be used to inform equivalent circuit values.



(a)



(b)

Figure 3.14 FD30 10x75 device geometry artwork and (b) Layout of CP 10x75 device for EM simulation. The gate terminal connection (port1) can clearly be seen as an underpass to the source terminal air bridges. The gate stripe is removed for this simulation.

The device layout for the 10x75µm transistor is shown in Figure 3.14(a). The layout shows the physical dimensions of the metallisation for the source and rain pads

and interconnects, along with the gate feed and airbridge underpass at the input, which are the sources of the parasitic elements.

The gate-to-gate spacing is 35 µm, larger than the standard 25um spacing to allow for thermal management of HPA designs. Via holes, used for grounding the device in the 'Common-Source' amplifier configuration, are also included in the simulation, and also appear in the transistor test cells.

The EM simulation layout is shown in Figure 3.14(b) for use in ADS® momentum software. The gate stripe is removed from the circuit simulation as the contribution from this aspect of the device is part of the intrinsic core.

EM analysis results of the 10x75µm device metallisation without Gate stripe are similarly converted into a π-network equivalent circuit as defined by Figure 3.12 and are shown in Figure 3.15. Using the low frequency data, the capacitances Cgsp, Cgdp, Cdsp can be determined as 55 fF, 11 fF and 115 fF respectively.

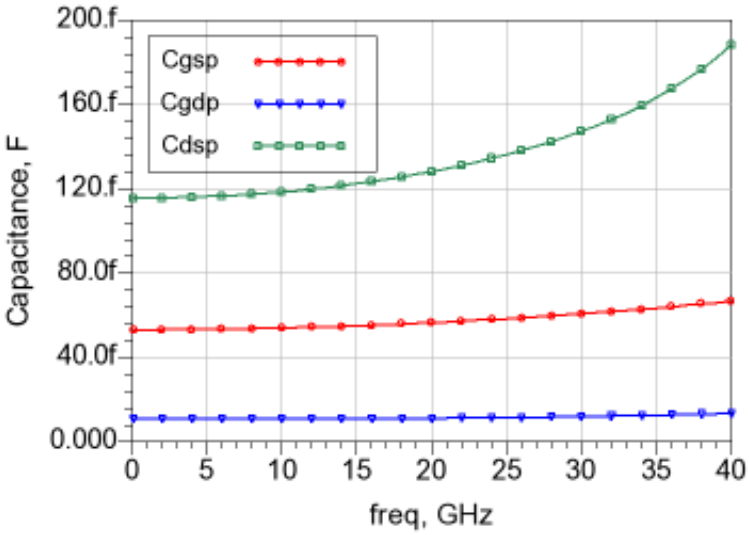


Figure 3.15 EM simulation results of the 10x75 FET structure (No Gate stripe)

These values are split off from the measurement data to provide a circuit implementation with two capacitances per element. The resulting values for the capacitive elements are shown in Table 3.1.

	Cgs (fF)	Cgd (fF)	Cds (fF)
Extrinsic	55	11	115
Intrinsic	189	180	51
Total	244	191	166

Table 3.1 Capacitance values for the FD30 10x75 COLD FET model

The curves in Figure 3.13 and Figure 3.15 both show a non-flat frequency response. If the equivalent circuit was a pure set of capacitances, the curves would be straight lines parallel to the x-axis. This shows that there are some distributed effects apparent and need to be included in the model [89]. This could be inferred from inspection of the layout showing it has a significant size, especially with the larger gate to gate pitch.

The EM extraction of the parasitic capacitance elements for these FETs is the first part in this process. The series elements need defining alongside to create a distributed approximation using the extrinsic (parasitic) and intrinsic elements of the pHEMT and the position they appear to define the frequency response of the network accordingly

3.4.3 Series parasitic Z-shell element extraction

The series elements are found, after removing the parasitic Y-shell, using similar measurements at cold FET bias conditions with the gate in a forward bias state [94][95].

The form of the resulting circuit is similar to the Z-parameter network as shown in Figure 3.16. Translating the forward bias s-parameters into this Z-parameter form enables the impedances to be determined using (3.19) to (3.22), in a similar manner to the parasitic Y-shell extraction process.

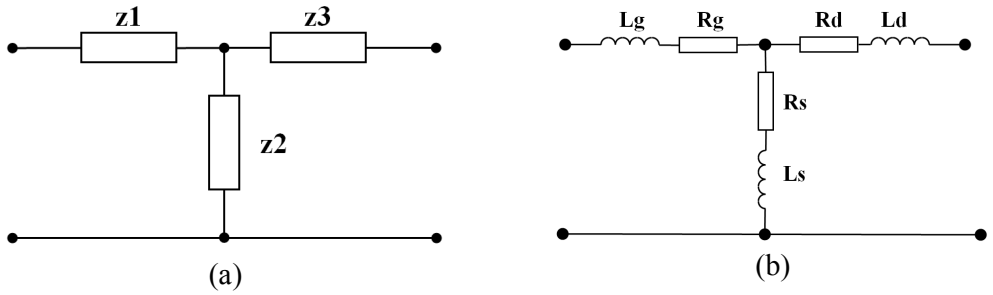


Figure 3.16 Tee configuration equivalent circuit for series element extraction

$$[Z_{ext}] = \begin{bmatrix} z1+z3 & z3 \\ z3 & z2+z3 \end{bmatrix} \quad 3.19$$

Rearranging, the values for z1, z2 and z3 can be determined, hence:

$$z1 = Z_{11\,par} - Z_{12\,par} = Z_g \quad 3.20$$

$$z2 = Z_{22\,par} - Z_{21\,par} = Z_d \quad 3.21$$

$$z3 = Z_{12\,par} = Z_s \quad 3.22$$

Rearranging these expressions, the values for z1, z2 and z3 can be determined and they map into the gate, drain and source impedances. These can be reduced to a simple series RL form for each impedance element. The element values are thus defined by the real and imaginary parts of the impedance such that R_x=Real(Z_x) and L_x=Imag(Z_x)/ω.

The operating point of the device for the series resistance element extraction is under forward bias, cold fet bias conditions – Vd=0V, Vs=0V, with the Gate-Source voltage, Vgs greater than the barrier. The exact value of the Vgs voltage is a variable and is set this by defining a forward Gate current, Ig, value.

Under these forward bias conditions the equivalent circuit for the transistor is shown in Figure 3.17. The circuit shows the extrinsic parasitic components and also the impedance contribution from the channel and the gate Schottky diode which are both a function of voltage.

The channel is equivalent to a distributed RC network and the equivalent circuit can be simplified as shown in Fig. 3. The R_{dy} and C_g are the Schottky resistance and capacitance which characterize the Schottky effects at the gate, while R_{ch} and C_{ds} account for the channel resistor and drain source capacitance.

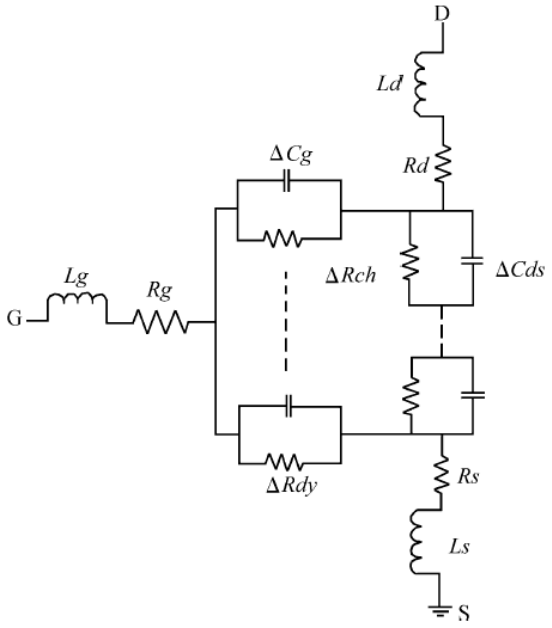


Figure 3.17 Cold FET model under forward bias condition [96], showing the Channel resistance and Schottky diode resistance contributions.

Analysing the region under the gate as a transmission line [96][97], and using a low frequency range such that the Schottky capacitance and drain–source capacitance can be neglected, leads to the expressions for the Z parameters as [87][96]

$$Z_{11} = R_s + R_g + \frac{R_{ch}}{3} + R_{dy} + j\omega(L_s + L_g) \qquad 3.23$$

$$Z_{12} = R_s + \frac{R_{ch}}{2} + j\omega L_s \qquad 3.24$$

$$Z_{22} = R_s + R_d + R_{ch} + j\omega(L_s + L_d) \qquad 3.25$$

The diode resistance R_{dy} is defined by the gate current and takes the form as shown in (3.26).

$$R_{dy} = \frac{nkT}{qI_g} \qquad 3.26$$

A typical strategy here is to choose bias points with a doubling of current for each bias setting. For the FD30 10x75µm (0.75mm periphery) device these are set as 25, 50, 100 and 200 mA/mm.

Bias Point	Gate Current density	Gate current calculated	Actual Gate Current
1	25mA/mm	18.75mA	17.4mA
2	50mA/mm	37.5mA	36.5mA
3	100mA/mm	75mA	79.5mA
4	200mA/mm	150mA	149.7mA

Table 3.2 Forward bias cold FET bias conditions for the Z-shell parameter extraction of FD30 10x75 device.

The extraction of the series resistance and inductance values is determined using the low frequency data to calculate the slope and intercept of the Z-parameters plotted versus (1/Ig) [87][90]. The results of the measurements are shown in Figure 3.18 and Figure 3.19.

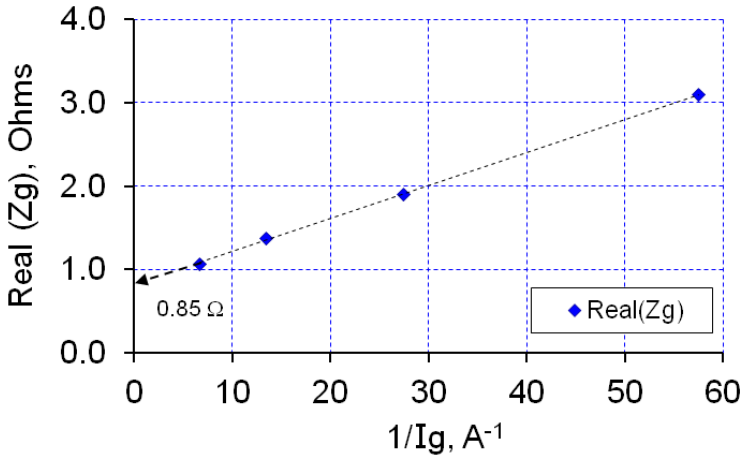


Figure 3.18 Resistance Rg derived from Re{Z_{11}-Z_{12}} measurements, extracted at 1GHz

The determined gate resistance is somewhat dependent on the fitting frequency range [98] but the data used here is extracted at 1GHz. There is an opportunity to optimise these values to fit to the measured s-parameter data in the small signal model.

The resistance values plotted in Figure 3.18 shows the y-axis intercept, which removes the diode bias dependent element (R_{dy}) resulting in the value ($R_g + 0.166R_{ch}$), where the R_{ch} term accounts for the small residual value of the channel resistance from

combining (3.23) and (3.24). This term is ignored at this point in the extraction process which will only result in a slight underestimate for R_g but which can again be optimised over the s-parameter range. In fact, in the model proposed the R_i term (used for the component in the channel) is derived only from the Tau calculation to ensure the delay is correct – it is difficult to differentiate the values Rg and Ri and these are used to ensure the real part of the input match is correct.

The parasitic inductances are extracted in a similar manner by plotting the slope of the imaginary parts of the Z parameters versus frequency (Figure 3.19) and using the expressions (3.23) – (3.25). Here the inductances are found to be, L_s=12pH, L_g=37pH, L_d=43pH.

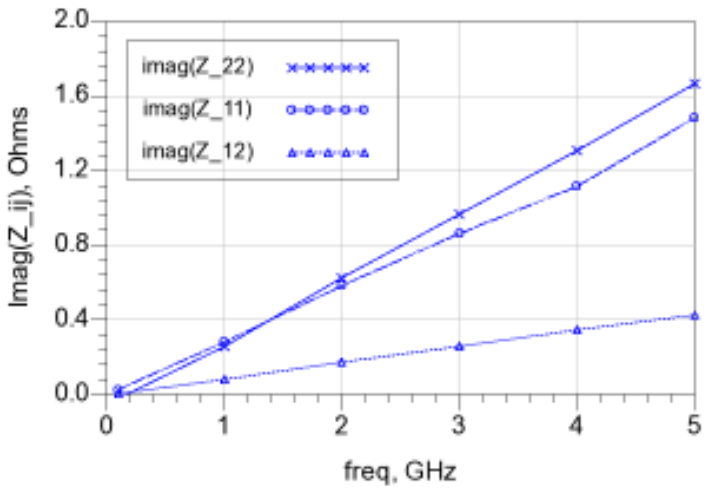


Figure 3.19 Extraction of the parasitic inductances for the 10x75 (MM1234A) device under forward bias conditions. Inductances are defined by the slope of the Z_{ij} response versus frequency.

Combining the series elements with the capacitive pi-network, including the parasitic shell from the EM simulations of the 10x75 device, the model derived for the Cold FET off state is shown in Figure 3.20

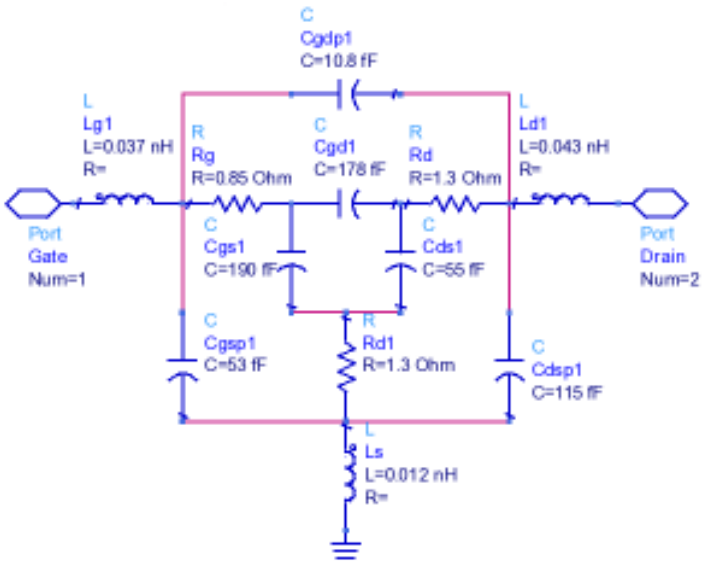


Figure 3.20 Cold FET distributed model. Parasitic capacitances for the pads and feed lines are removed.

Simulating the model and comparing to the measured data under Cold FET bias conditions is shown in Figure 3.21.

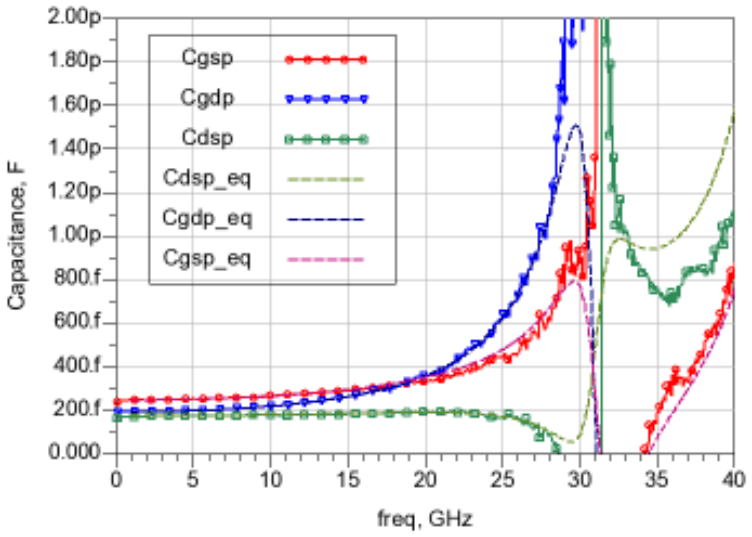


Figure 3.21 The capacitive Pi network with extrinsic capacitances compared to the measured data (58029.0001.MM1465A)

3.4.4 Full pHEMT model extraction

Taking the parasitic extrinsic component values as derived in sections 3.4.1 – 3.4.3, these can be successively stripped from the model and the intrinsic core element values can be derived [85][87], that is, de-embedding the inductance of the Z-parameters first then the parasitic Y-Shell, Cgsp, Cgdp, Cdsp components, resulting from the EM simulation.

Then equivalent circuit component values for the intrinsic device are extracted to fit the model. The full small signal model and elements are shown in Figure 3.22.

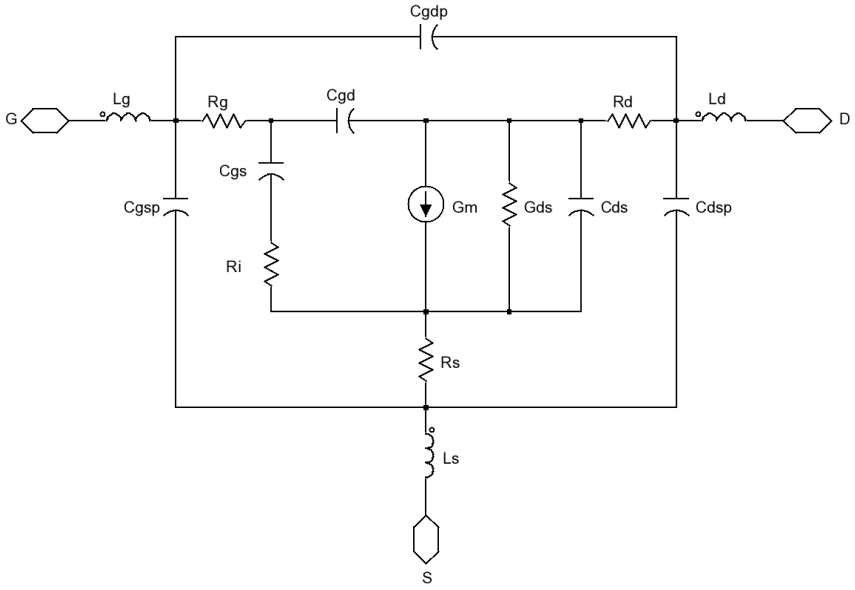


Figure 3.22 The Small Signal HEMT extracted model equivalent circuit

Since the intrinsic core exhibits a π-network topology, the element values are extracted in a manner similar to the cold FET Y-matrix approach. Elements are easily resolved using equations (3.13) – (3.16) for each branch of the network and equating the real and imaginary parts to the elements in Figure 3.23.

The element values are extracted for each bias condition under consideration. Further work can be used at this point on multiple bias conditions and transistor cell sizes to create a parameterised model if required. This step is not covered as it falls

outside the scope of this thesis and not required for the circuit evaluation covered in later sections.

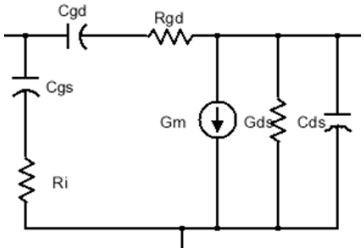


Figure 3.23 FET/HEMT Intrinsic core network element definition

Typical FD30 10x75 µm device extracted parameters are shown in Table 3.3 at a fixed bias voltage (Vds=9V, Vgs=-0.6V) using measurements taken from FD30 wafer 58029.0001.001.MM1465A.

Lg	37 pH	Rg	0.85 Ω
Ld	43 pH	Rd	1.3 Ω
Ls	12 pH	Rs	1.3 Ω
Cgs	2204 fF	Cgsp	53 fF
Cds	58 fF	Cdsp	115 fF
Cgd	59 fF	Cgdp	10.8 fF
Gm	256 mS	Gds	5.46 mS
Ri	0.94 Ω	Tau	3.05 ps

Table 3.3 FD30 10x75 pHEMT Small signal model element values for Vds=9V, Vgs=-0.6V

The typical intrinsic device parameter extraction results are shown in Figure 3.24 and Figure 3.25 for two distinct bias conditions. This data shows some voltage dependence is evident the capacitive elements, Cgd, Cgs (and subsequently on the values of Tau and Ri). This needs to be carefully considered when using the data as this will mean the de-embedding of the waveforms needs to be undertaken using a weighted average over the waveform operating conditions to get an accurate result.

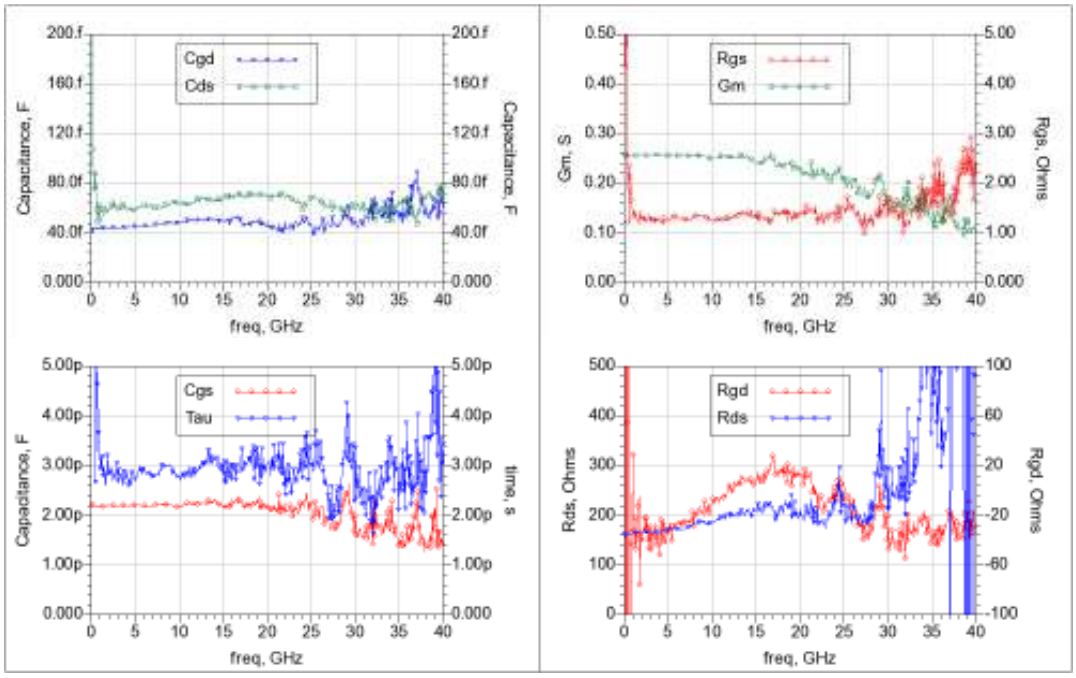


Figure 3.24 Extracted small signal 10x75 model values at 9V, -0.6V

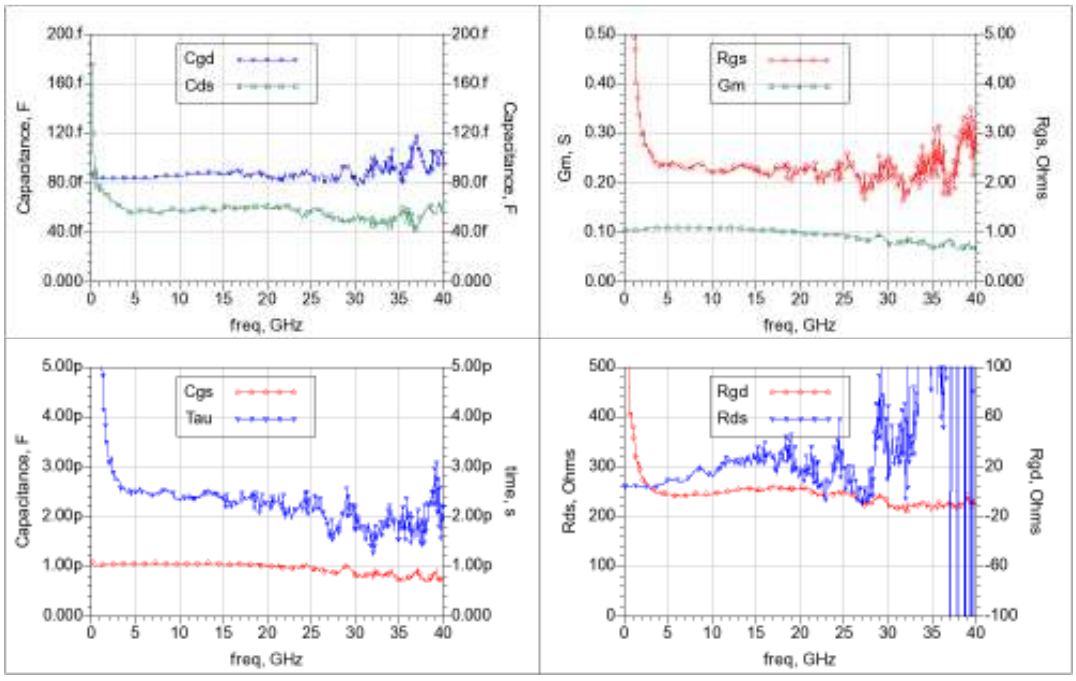


Figure 3.25 Extracted small signal 10x75 model values at 9V, -1.1V (Class B bias)

Following the extraction process, the models were simulated and compared to the measurement data up to 50GHz, Figure 3.26 and Figure 3.27.

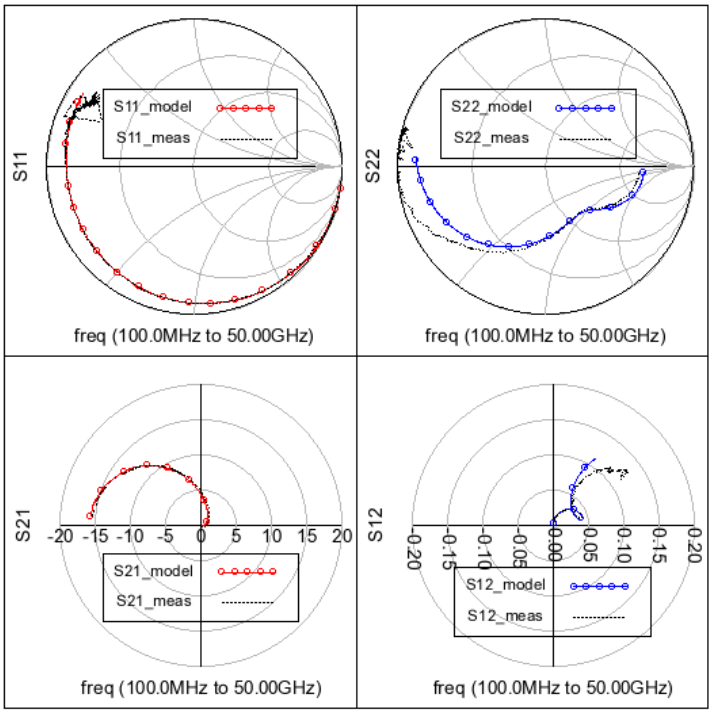


Figure 3.26 S-parameter measured data versus extracted model for FD30 10x75 device, 9V, -0.6V.

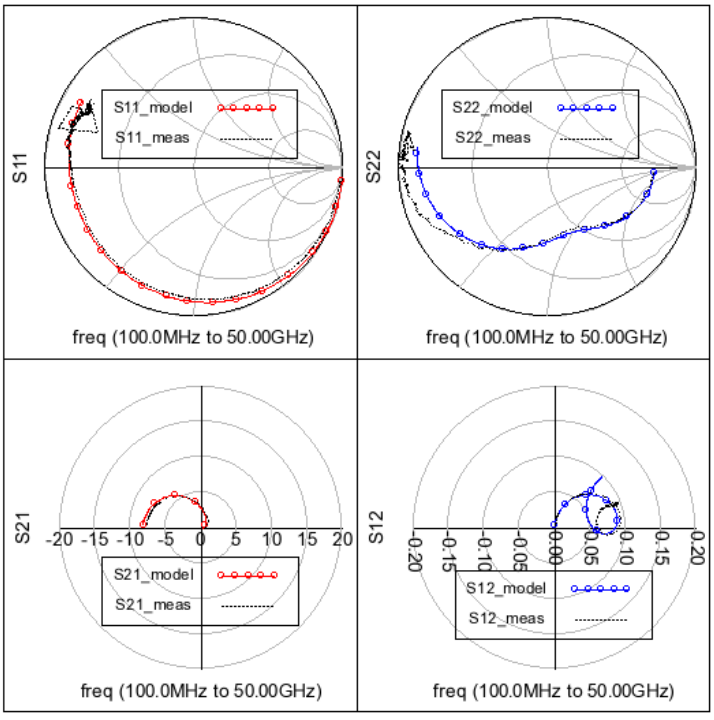


Figure 3.27 S-parameter measured data versus extracted model for FD30 10x75 device, 9V, -1.1V.

The plots show there is good general agreement between the model and measurement data for both class AB and class B bias points. The input match (S11) of the model has excellent correlation to 50GHz, with the biggest error shown in the output match (S22) – but the model correlates well to 36GHz, which is enough to capture 4th harmonic performance of a 9GHz amplifier.

The most important part of this for the work in this thesis is the equivalent circuit networks for the extrinsic parasitic networks at the gate and drain terminals (Figure 3.28). The elements take the values defined in Table 3.3, or as determined using the process outlined for the required bias point.

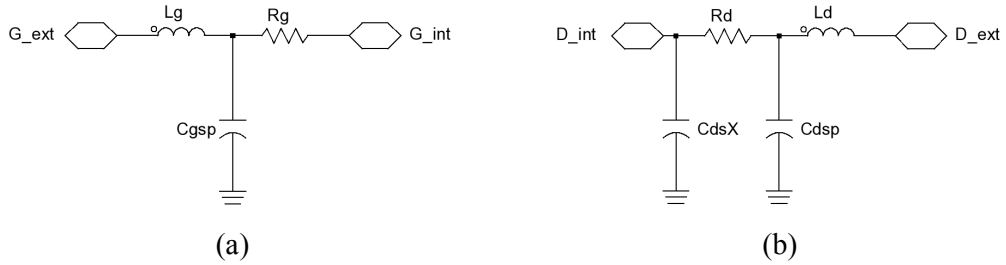


Figure 3.28 Parasitic equivalent circuit networks for FD30 10x75 pHEMT device (a) Gate terminal and (b) drain terminal

These will be used to determine the intrinsic waveforms from the terminal measurements. At the output the series drain inductance and resistance are included along with the drain capacitance, Cds, elements. The Cds capacitance here is a fixed value linear approximation ignoring the voltage dependence.

The input de-embedding file however, only needs to include the series gate inductance and resistance and the parasitic gate capacitance, Cgsp, related to the metallisation and crossover effects. The non-linear gate capacitance, Cgs, is deliberately not de-embedded. This is the circuit node at which the gate voltage waveforms are to be determined, and the gate capacitor will directly affect these waveforms, and hence the drain current pulse, so needs to be included.

3.4.5 De-embedding Limitation

The de-embedding approach outlined so far has shown the use of an equivalent circuit can be determined and the resulting parasitic elements can be removed from the measurements to find the intrinsic reference plane performance. There needs to be a

note of caution in the use of this technique, which confines the use of the model to a physical representation of the device. This is implied in the development of the model from the measured data in this chapter. The circuit elements here are related to the device geometry and de-embedding to the intrinsic planes is simple by negating these parasitics. There are residual errors, as with any model development from measured data into an equivalent circuit, but these can be minimised, and it does not invalidate the approach.

When using CAD models errors may occur where the device model has a non-physical relationship, for example negative capacitances, in the parasitic model representation. In this case, using the series inductor/resistor combination for the terminal access elements will not de-embed to the correct intrinsic plane and the waveforms will be invalid. CAD models with direct access internal nodes will be the ideal solution to this problem.

3.5 Conclusion

This chapter has shown the processes required to de-embed RF measurements of transistor test cells on wafer. The de-embedding allows the reference plane to be moved for s-parameter or waveform measurements allowing insight into the waveforms at the intrinsic control nodes in the transistor and the resulting performance space.

It is clear that access to the internal node waveforms is a requirement for correct analysis of amplifier operating modes. In the CAD simulator it is better, for reasons of accuracy, to have direct access to the internal node in the model rather than deriving a de-embedding network. In the measurement space, however, there will always be errors associated with the de-embedding process due to the extraction of the parasitic elements.

The extrinsic parasitic model parameters critical to this approach have been found and this allows direct inspection of the waveforms at the reference plane allowing a link to the theory of chapter 2. These parameters are also useful in the design phase of a PA. They can be used to place ideal waveforms at the controlling nodes by a novel application of CAD circuit simulators. This can adjust for other parasitic elements (for example the source resistance) to deliver the ideal performance. This is demonstrated in the next chapter.

4 SIMULATION METHODS

Scattering parameter simulation[4] is the main approach for general microwave and RF circuit analysis. This technique is applicable to passive and active circuits but is limited to the small signal regime, that is, where the circuit is considered linear. High power amplifiers cannot effectively be simulated with this approach to predict output power, efficiency and compression, so a different approach is taken.

Traditional large signal simulation methods in CAD environments start with the use of a large signal model for the active device. These device models are generally 'compact' models [62], where the device is approximated by circuit elements and mathematical descriptions of the non-linear components. Behavioural and data based look up models, for example X-parameters® [100] and the Cardiff model [99] are becoming more common as an alternative to the compact models. These models are effectively black box representations of a network providing a response to the input stimulus and load conditions. There are no approximations used and the response of the network is based on a mathematical representation of the network measured port voltages and currents against variable load conditions. This technique does place a large burden on the measurement set-up and number of test points.

For the work in this thesis, the foundry supplied PDK 'compact' models are used, but the techniques outlined are equally valid with any non-linear model implementation.

The test bench used for simulation uses standard techniques within most circuit simulators comprising both a large signal 'stimulus' and 'load' component with the active device model embedded in between.

4.1 Standard Large Signal simulation methods

A simple HPA circuit large signal simulation set-up is shown in Figure 4.1 comprising an active device model embedded in a virtual test bench. The test bench consists of a pair of dc voltage sources for the gate and drain bias, a 50 Ohm Large

[4] The word 'simulation' is used to define the act of finding the theoretical response of circuit in CAD software. It is used in preference to 'modelling' which is reserved for the act of defining a circuit to recreate the performance of a physical network.

Signal power source as the stimulus for the circuit, for example a 'P_1Tone' in Keysight Technologies[5] ADS® simulation tool, and a load impedance.

The output match (or load) in this simulation is initially defined in terms of impedances from a data file, or from a set of equations to be used in a load pull simulation. These theoretical or calculated impedances are later refined into ideal circuit elements and then finally into the practical element models or Electromagnetic (EM) simulation blocks representing the physical implementation of the matching network. This circuit is coupled with a set of voltage, current or power probes at strategic points in the circuit network to define the output power, dc operating conditions and so on.

The simulated large signal waveform response of the circuit is shown in Figure 4.2. These waveforms have been de-embedded using the process detailed in section 3.4, to show the intrinsic plane response. Initial simulations used the standard value of 0.3pF for the Cds drain capacitance element for the de-embedding file (for the 10x75 device). It is clear that the waveforms are far from ideal and can be partially accounted for by an underestimate in the Cds value for de-embedding. The bottom of the Ids current pulse is not flattened out correctly and closer inspection of the dynamic load line (Figure 4.3) shows that there is a significant amount of 'looping' indicative of reactive effects.

[5] Keysight Technologies was formerly known as Agilent Technologies Inc.

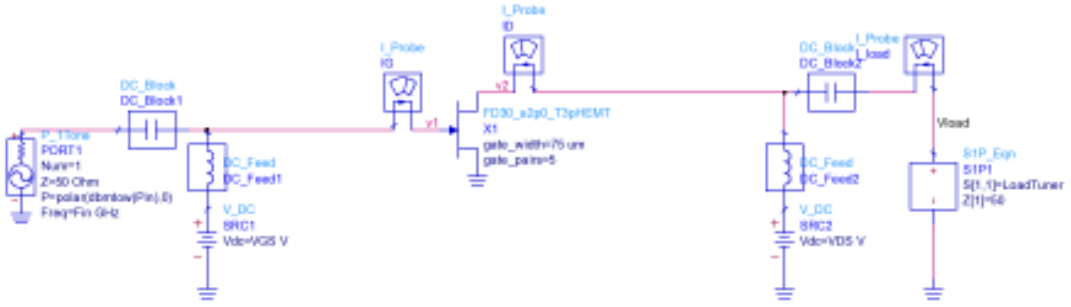


Figure 4.1 Standard Large Signal simulation circuit using the Compound Photonics 10x75 PDK transistor model and a load impedance defined by a datafile.

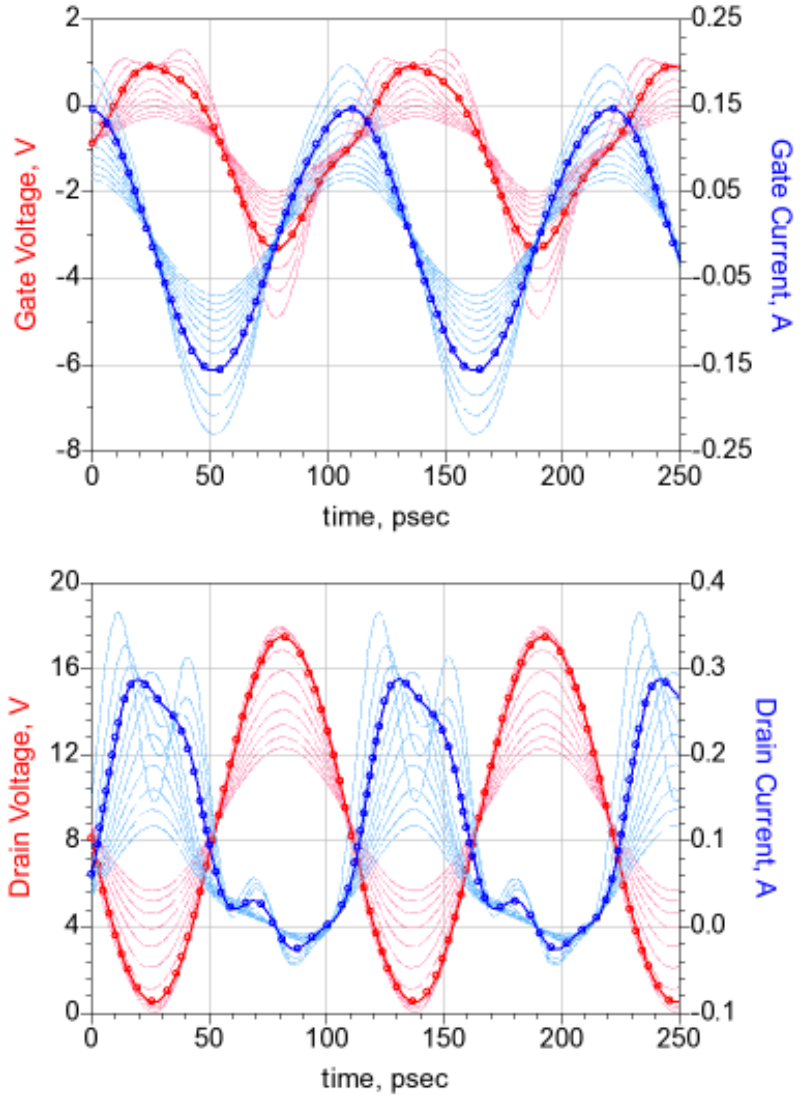


Figure 4.2 Large signal simulation waveform results at 9 GHz using P_1tone for swept input power

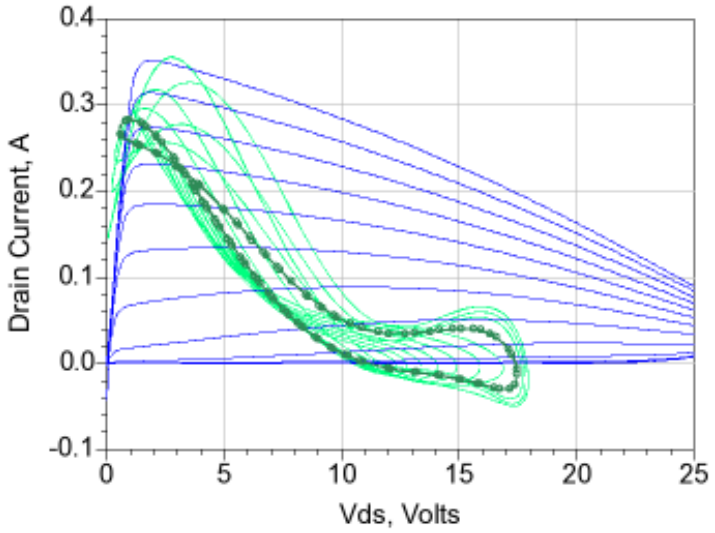


Figure 4.3 Dynamic loadline for the large signal simulation circuit of Figure 4.1 using 0.3pF Cds de-embedding.

Modifying the drain capacitance model to a value of 0.36pF shows are marked improvement on the output current waveform shape but still noting there is some distortion due to the input gate voltage (Figure 4.4).

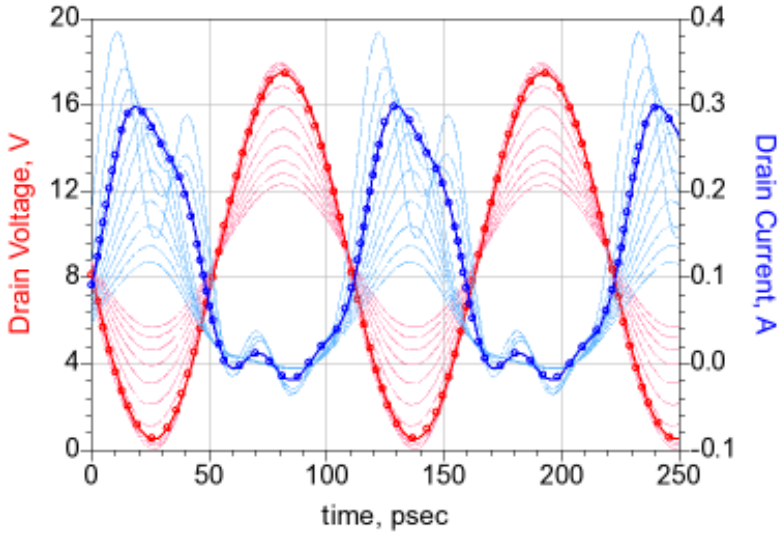


Figure 4.4 Large signal simulation results for the drain waveforms using Cds=0.36pF de-embedding

The response of the circuit shows there is distortion of the waveforms at the intrinsic nodes as there is no direct relationship between the stimulus and load defined by the simulation circuit and the desired waveforms for amplifier operation.

Using voltage sources to define the stimulus would be more representative of the actual amplifier operation. The input stimulus can be replaced with a large signal voltage source and the output load defined as before with a set of equations defining a set of harmonic impedances.

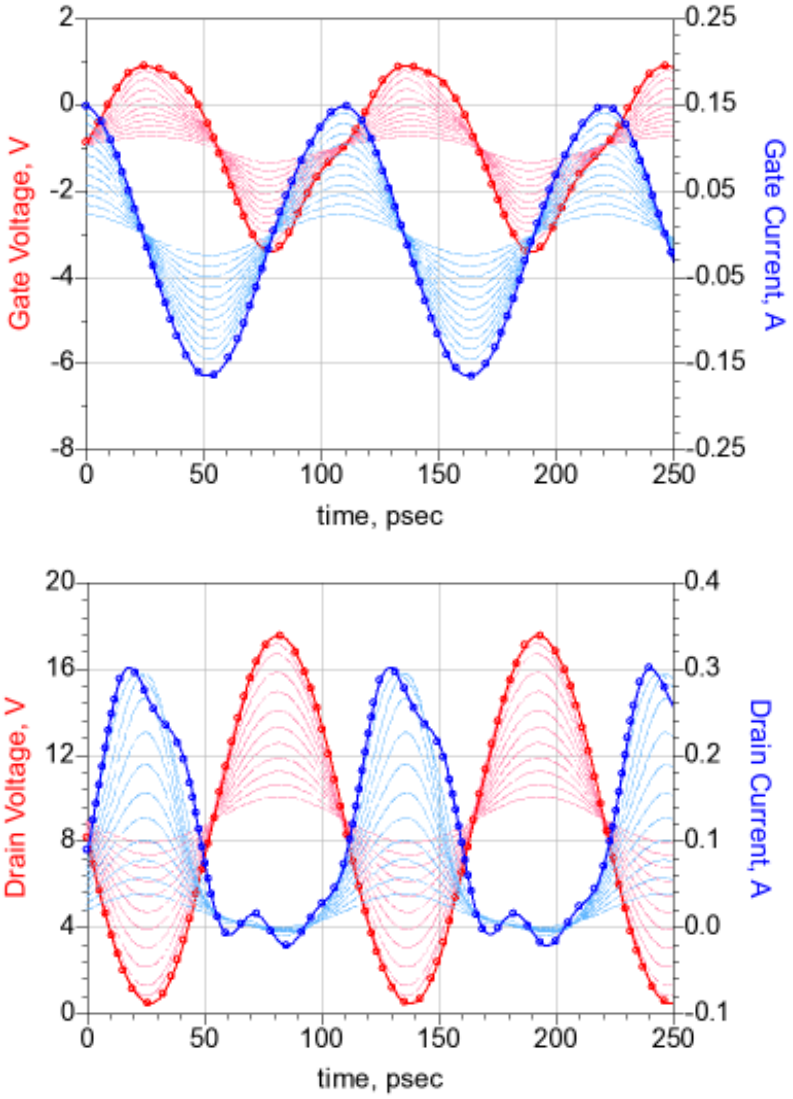


Figure 4.5 Simulation response using voltage sources as the stimulus at 9GHz

There is still significant distortion in the waveforms at the intrinsic plane. The input waveforms when de-embedding past the gate parasitic elements (Rg and Lg) show non-ideal shape due to these parasitic components (Figure 4.5). This is due to the harmonic

currents generated by the input non-linearities flowing through the source and parasitic impedances.

A further point on the waveform distortion results when running the device in a class J or J* mode (rather than the class B condition) as there is a significant 2nd harmonic voltage component at the drain terminal by design. Feedback through the parasitic device elements (Cdg) is now possible and, as previously noted in section 4.1, this can cause a detrimental effect on the input waveforms as the feedback currents flow through the source impedance (e.g. Z_0=50Ω).

Additionally, the output voltage waveforms are dependent on both the input drive signal (which is distorted) and the resulting drain current waveform interacting with the load impedance. A more intuitive approach is to use the desired waveforms directly in the design process and then synthesise the matching networks from the resulting response.

4.2 Voltage source simulation methods

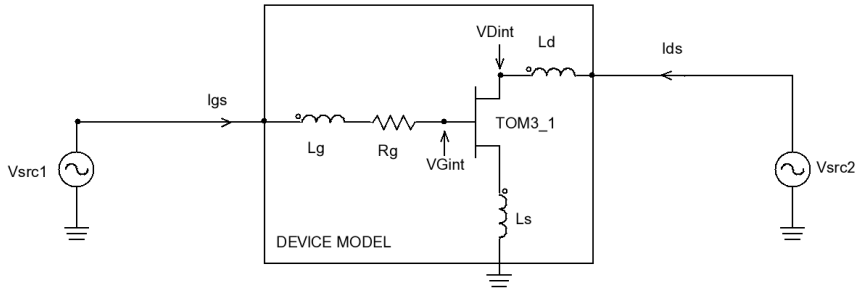
The proposed simulation method is to use a voltage source for the injection and define this as the drive between the intrinsic gate and source nodes. This will allow setting of precise voltages at the controlling node, i.e. the node that controls the output current waveform. Choice of the maximum gate voltage swing is determined that which results in the designed maximum drain current, I_{max} to define the optimum load line. For the CP FD30 process this is chosen to be $V_{gs,max}$=+1V for the maximum current swing. This simulation approach is very similar to the existing method but the voltage drive waveform needs to be applied at the intrinsic plane.

The most significant difference in the modelling method is the way the output load will be determined. Using voltage sources and an appropriate predistortion[6] network, the correct output waveform can be placed at the intrinsic drain node for any amplifier class. In this way the optimum load impedance is ascertained from the ideal drain voltage waveform and the output current shape, which is controlled by the input voltage.

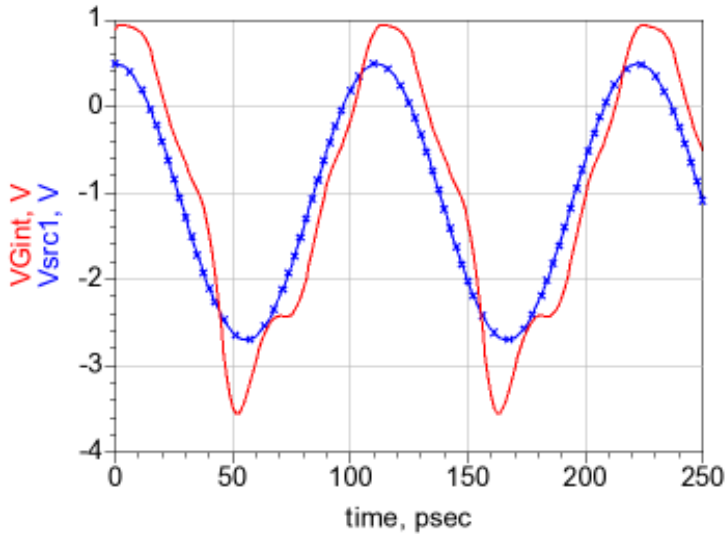
[6] Predistortion is used here to refer to a network that modifies the response of the driving signal prior to use at a specific network node in a simulation circuit and not, as in common literature, about creating a technique used to improve the linearity of Power Amplifiers in communication systems.

4.2.1 Waveform engineering simulation method

Using voltage sources in the CAD simulator, it is possible to create an ideal driving signal for an amplifier by specifying the waveform in terms of fundamental and harmonic components in the time domain. However, referring to Figure 4.6(a), there will be distortion of the waveforms at the intrinsic plane which comes directly from current flow through the parasitic elements of the device and the voltage source driving signal. This includes any harmonic currents generated by the device itself flowing through these elements, which result in even further distortion. These waveforms are shown in Figure 4.6(b). These distorted waveforms degrade the amplifier performance.



(a)



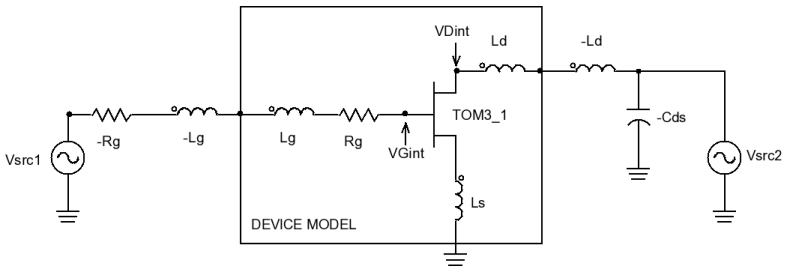
(b)

Figure 4.6 Voltage source simulation method and resulting intrinsic gate waveforms, demonstrating the distortion effects of the parasitic impedances.

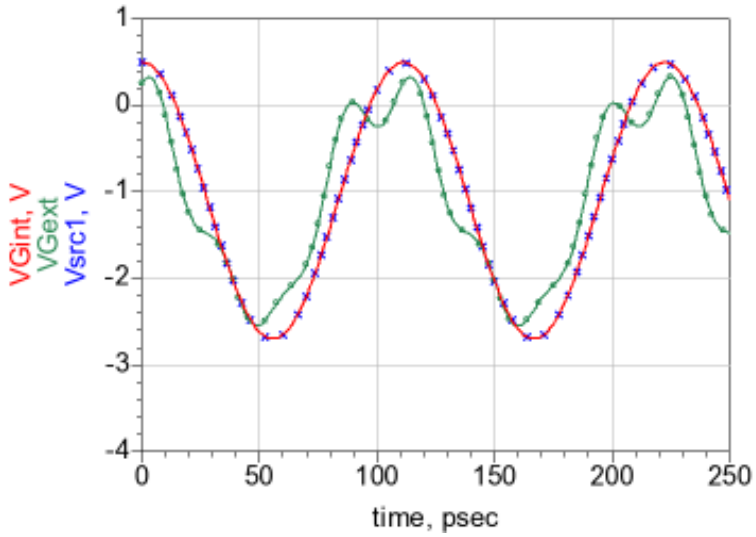
A method is required to define the waveforms at the intrinsic plane. This is possible by using the de-embedding parasitic networks, detailed in section 3.1, in reverse.

If the waveform defined by the large signal voltage source is modified by an appropriate network, which provides the inverse response of the parasitic device shell, the ideal driving source voltage will appear at the intrinsic device plane.

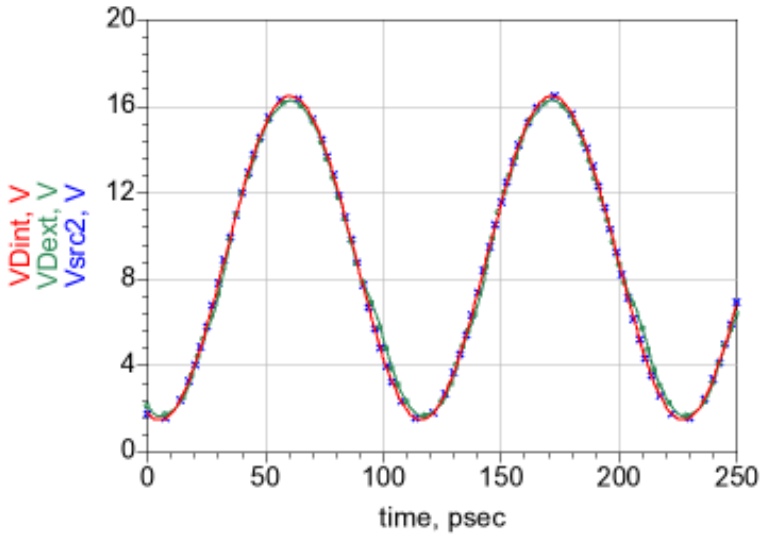
A network which performs this function is simply the negative components of the device parasitic elements. This basic schematic diagram for this circuit is shown in Figure 4.7(a) and shows the order of the elements in the network is key to ensure correct embedding of the voltages. The resulting waveforms are shown in Figure 4.7(b) and (c) for the FD30 10x75 pHEMT device at 9GHz. It is clearly seen that the intrinsic voltages are exactly as defined by the voltage source elements at the source and load. The extrinsic voltages required to define this are also shown as VG_{ext} and VD_{ext} on the plots and it is clear these are significantly distorted. The non-linear effect of the input gate capacitor is clearly noted. There are higher order harmonics evident in the gate waveform, which are generated by the device as the only input stimulus signals are from the fundamental frequency voltage sources.



(a)



(b)

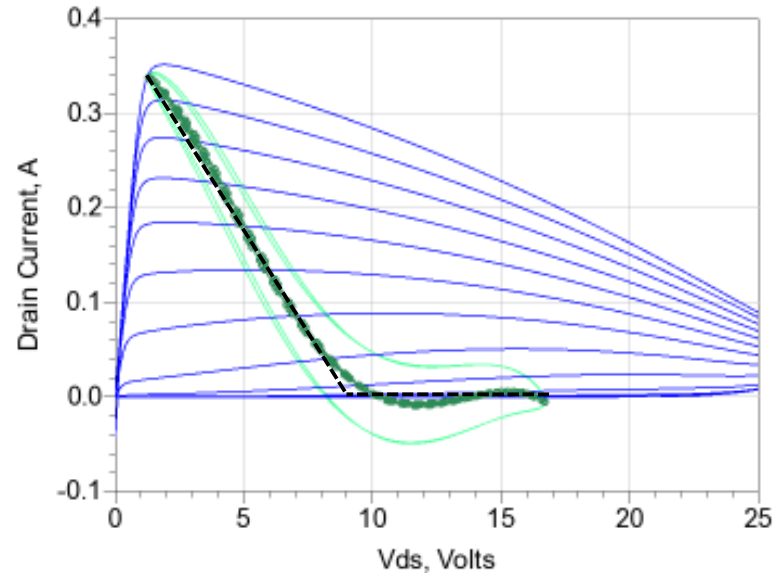


(c)

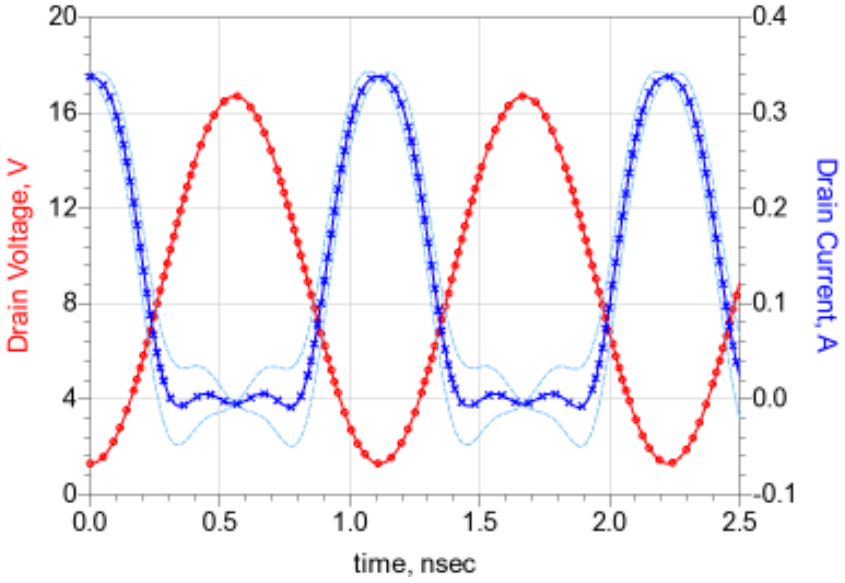
Figure 4.7 Voltage simulation method (a) schematic with predistortion network, (b) resulting gate simulated waveforms and (c) drain waveforms.

4.2.2 Interpretation of the waveforms

Interpretation of the device intrinsic plane waveforms and load line under these de-embedding conditions is outlined below.



(a)



(b)

Figure 4.8 Intrinsic plane (a) load line and (b) waveforms for a transistor. Ideal load line (black dash), correct de-embedding (bold) and the over/undercompensated case (light traces)

The ideal loadline for class B is shown in Figure 4.8 along with a simple model loadline, which is almost identical. The corresponding drain current waveform can be determined from this load line. Starting at the maximum drain voltage, the drain current

will be zero and remains there when traversing along the x-axis. This is the flat bottonm of the current pulse. When the drain supply voltage is reached, the current rises to a peak. The current then follows the same path in reverse along this load line. The current pulse is shown in bold in Figure 4.8(b).

If the de-embedding is incorrectly compensated the load line is modified to a closed loop (Figure 4.8(b)). The trajectory of the loops is traversed in a clockwise or anti-clockwise direction depending on whether the de-embedding is over or under compensated. The related waveforms under these conditions show a non-flattened bottom, with the current going below zero (which gives rise to the looped loadline response).

4.2.3 Class B waveform simulation

Implementation of the waveform simulation approach using ADS is shown in the schematic circuit of Figure 4.9. The use of the negative component values is clearly identified, placing the synthesised waveform at the intrinsic reference plane, along with the equations defining the voltage source waveforms.

The output load is defined by the voltage source creating the required drain terminal waveform. For the case shown in Figure 4.9 this drain voltage has a fundamental component only consistent with the Class B mode of operation.

This drain voltage is scaled with a swing defined by the dc supply (Vds) and the knee voltage (V_k). The representative waveforms from this simulation are shown in Figure 4.10 at a frequency of 0.9GHz. These show the classical Class B waveforms of a clipped sinewave current shape and a dynamic load line sweeping up to Imax. The drain voltage is seen to be clipped at 1.5V, as defined by the knee voltage at the desired operating point and specified in the simulation circuit.

The drawback of this simulation approach, which needs to be overcome, is the need to define the phase relationship between the input and output voltage sources. It is important when using the voltage sources that the delay between the Vgs and Vds waveforms is handled correctly as any phase shift between the waveforms will distort the operation.

Ideally, and at low frequencies, this phase relationship between the input Vgs and the Vds waveforms should be 180°. This is the basis for the plots in Figure 4.10.

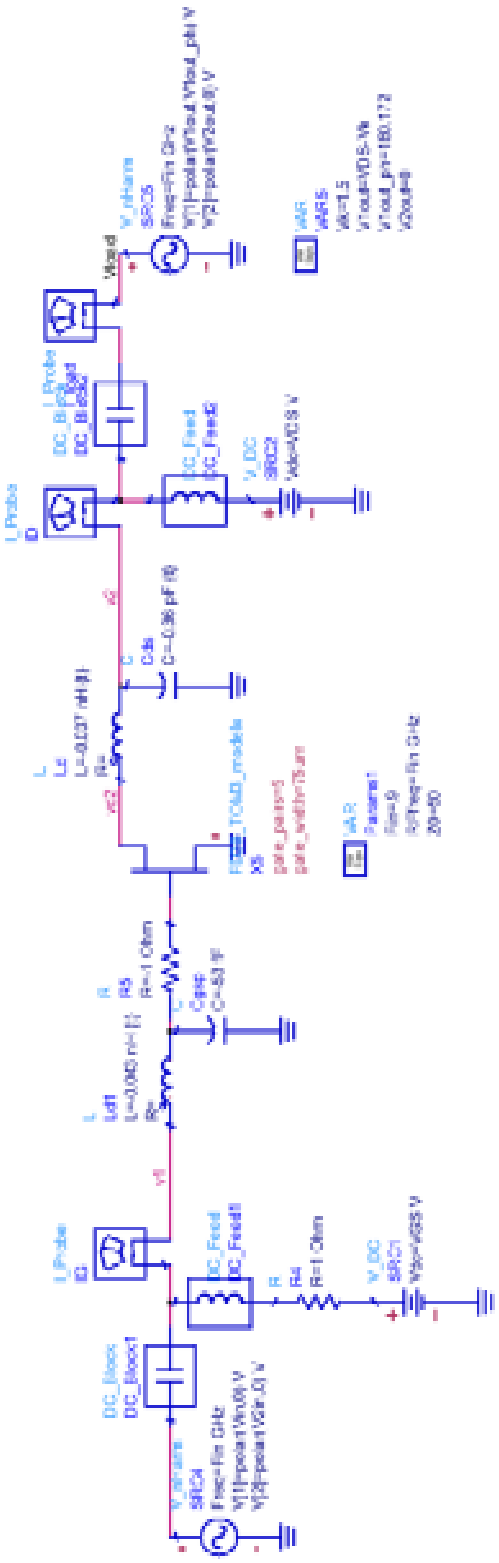


Figure 4.9 Voltage source driven simulation schematic in ADS. Negative element value predistortion shown for Class B analysis at 0.9GHz.

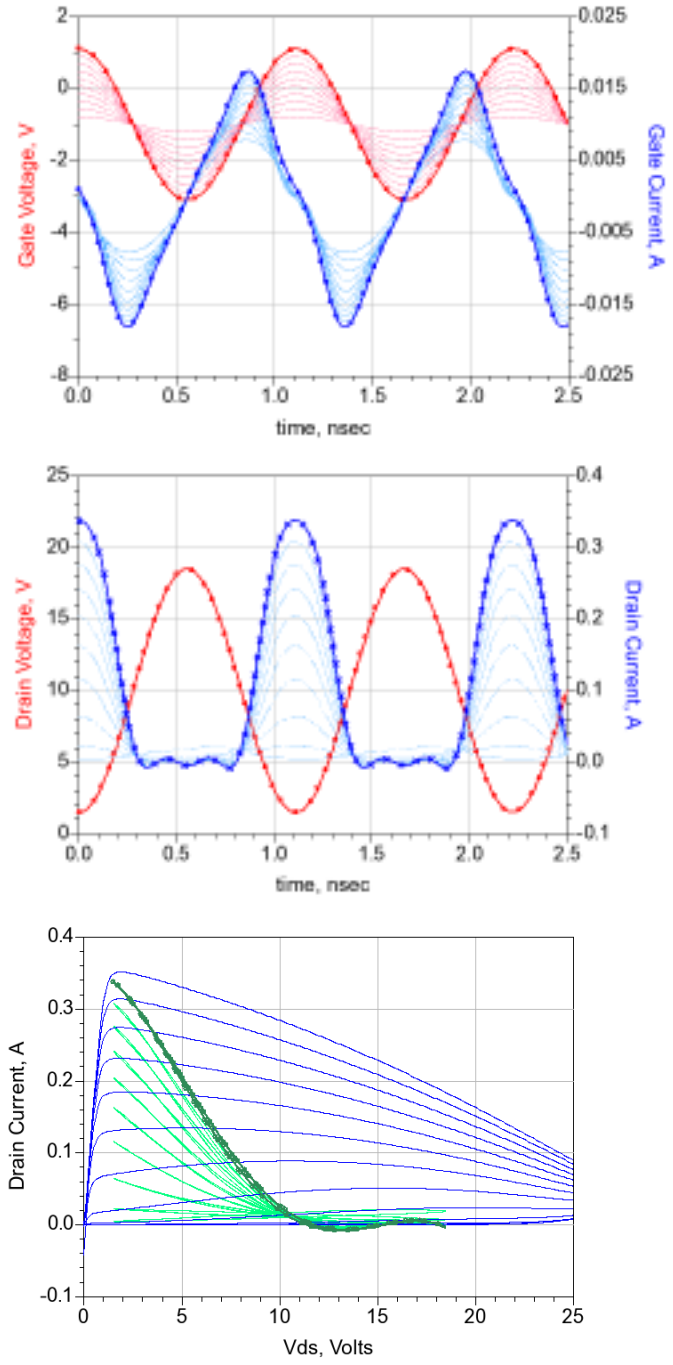


Figure 4.10 Voltage Source driven FD30 10x75 – Class B operation at 0.9GHz (Vgsq=-1.0, Vdsq=9V, Vk=1.5V) Cds=0.3pF, phi=180

Simulating the circuit at 9GHz, the waveforms deviate from the ideal (or low frequency) case. The response for the simulation circuit at this frequency is shown in Figure 4.11.

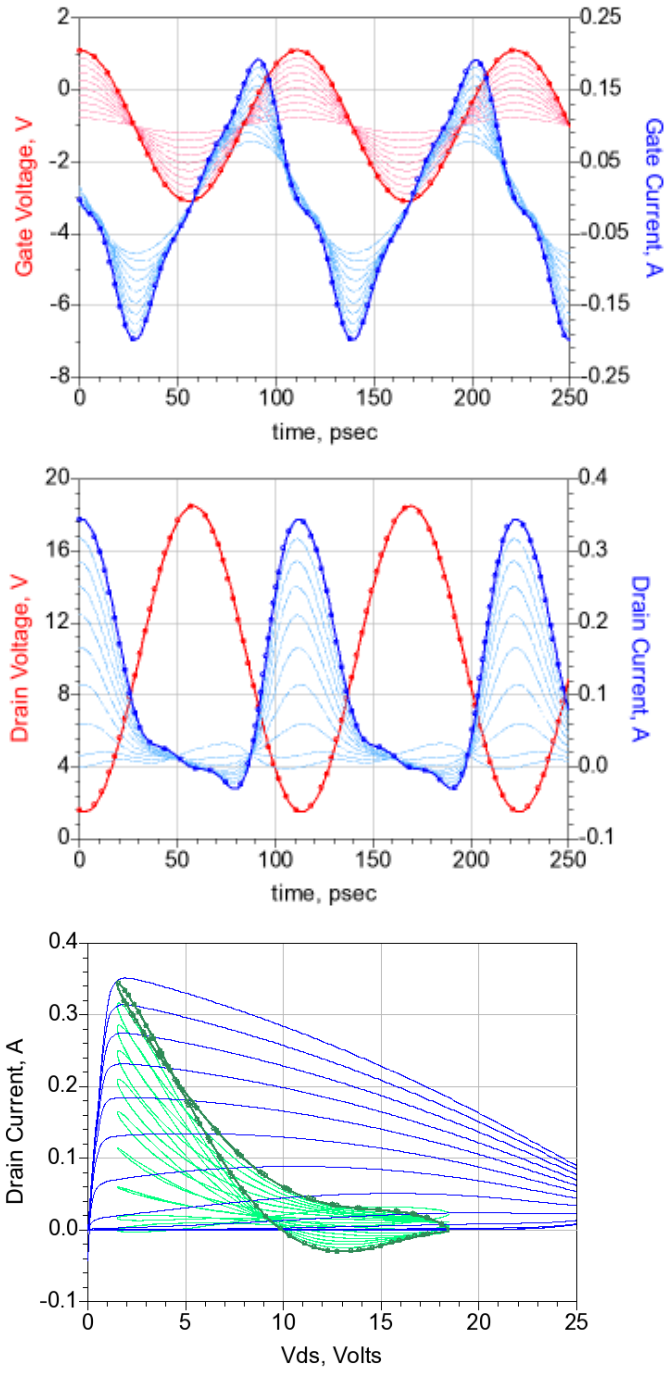


Figure 4.11 Voltage Source driven FD30 10x75 transistor – 9GHz Class B operation (Vgsq=-1.0, Vdsq=9V, Vk=1.5V) Cds=0.3pF, phi=170. Swept gate amplitude 0.1-1.0V, Bold trace at Vg=1.0V

The drain current waveforms do not exhibit the flattened bottom of the current pulse. It is clear the de-embedding is not correct. In fact at the Cds value of 0.3pF, as extracted from the methods in section 3.4, is too small (and was also noted in the usual large signal simulation approach). Furthermore the dynamic load line shows significant

looping (reactive effects). Further inspection of the de-embedding network shows an additional capacitive element is required.

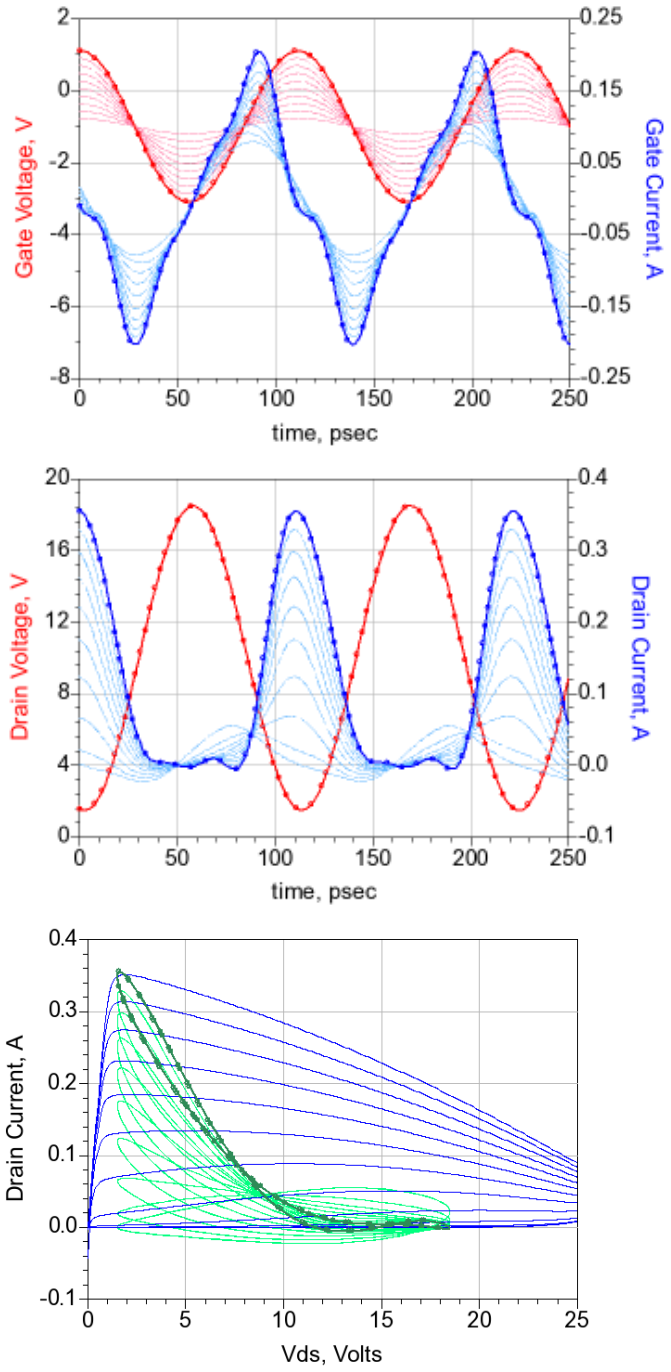


Figure 4.12 Voltage Source driven FD30 10x75 transistor – 9GHz Class B, (Vgsq=-1.0, Vdsq=9V, Vk=1.5V) – Cds=0.36pF, phi=170. Swept gate amplitude 0.1-1.0V, Bold trace at Vg=1.0V

The origin of this element is found from the Miller theorem. This shows that the component is the Cgd element which appears in parallel with the Cds component at the output node, and takes the values as extracted.

Adjusting the de-embedding capacitance to 0.36pF (C_{ds} + C_{dg}) the response is recovered and is in line with the theoretical expectation, as shown in Figure 4.12, and the dynamic load line shows a much reduced amount of looping. Any residual error from the ideal line is due to the simple parasitic model used which has fixed element values (i.e. no bias dependence) and small number of elements.

There is also a contribution from the phase shift through the network in aligning the gate and drain voltage waveforms. At higher frequencies there is a finite phase shift through the device and the 180 degree assumption is in error. Empirically, anything around 180 degrees works at a frequency of 9 GHz, and the voltage and current waveforms seem reasonable. However, on closer inspection there is a varying amount of 'looping' in the dynamic load line.

To reduce this and find the optimum performance, the waveforms used in the simulator need to be related to the start phase for the ADS system, so the gate and drain waveforms align correctly. This, in general, is not a problem in the usual large signal simulation method, when the output voltage is determined during simulation due to the current flowing through the defined load impedance.

The approach taken here is to optimise the phase angle between the gate driving voltage and the output drain voltage manually, using a swept variable. This method was used as there was no closed form solution available within ADS at the time of writing. Recently, a Frequency Defined Device (FDD) modelling approach has been developed which allows the phase to be aligned automatically during the simulation [101] thus simplifying this simulation method.

Sweeping the relative angle Φ, allows the performance of the amplifier to be assessed. This needs to be performed with a defined Cds de-embedding value as the phase shift can also be viewed as additional capacitance at the Cds plane. The Cds value in practice has some weak bias dependence but is defined in this experiment to independent of the gate voltage, Vgs (the Vds voltage waveform is defined to be a fixed

value throughout the simulation space by the very nature of the design process using voltage sources).

The power and efficiency results for swept phase are shown in Figure 4.13 and the waveforms and dynamic load line are shown in Figure 4.14. These results show a phase shift between 165° and 175° is optimum, depending on the chosen target of output power or drain efficiency. At these higher frequencies, this is not 180° due to the phase shift related to the finite physical size, the Unit Gate Width, of the device.

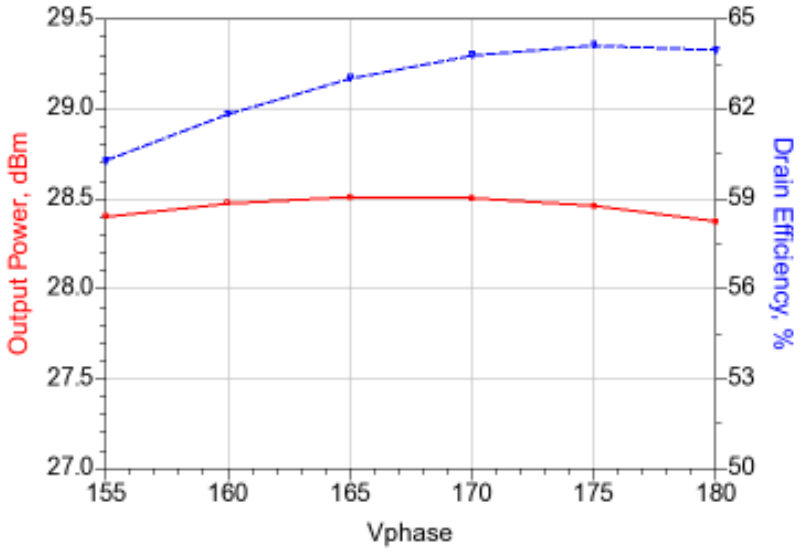


Figure 4.13 Output power and Drain Efficiency for swept phase of Vds fundamental component. Showing Φ=165° – 170° is optimum for Power and Φ=175° is optimum for Efficiency.

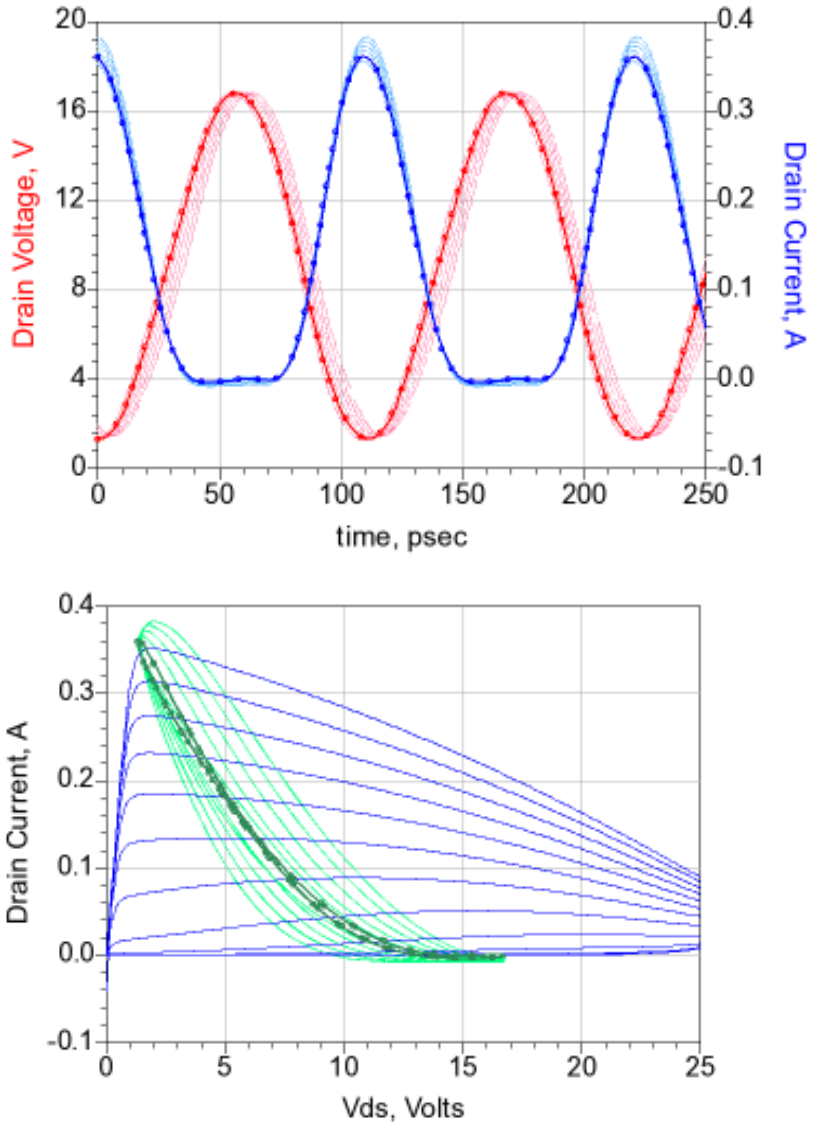


Figure 4.14 Waveforms and dynamic load line for the swept phase condition (155°-180°) – bold trace is at 175°, for the simulation at 9GHz, Class B operation.

It is important to note that the analysis technique demonstrated here has not referenced any impedance during the simulation process, unlike the traditional amplifier design process. These impedances (which are important) can be easily found by taking the ratio of the output voltage to the drain current when it is necessary to implement the actual matching networks.

4.2.4 Waveform engineering Class J simulation

Expanding the voltage source simulation approach, the simulator can also create the ideal class J waveforms (or any other arbitrary waveform set) by adding in the correct reactive fundamental and second harmonic voltage at the output.

The basic Class BJ theory factored waveforms given in equation (2.12) need modification to be used in the ADS simulation software. Expanding the terms out (4.1) clearly shows the three main components of the waveform – the fundamental term the reactive fundamental term and the second harmonic.

$$V_{BJ}(\theta) = (1 - \beta\cos\theta - \alpha\sin\theta + \frac{\alpha\beta}{2}\sin 2\theta) \qquad 4.1$$

This equation provides the normalised voltage waveforms and requires scaling to the full drain voltage levels. Scaling with the dc voltage $V_{ds,DC}$ and shifting for knee voltage, so the waveforms limits at the voltage V_k, leads to the final version (4.2)

$$V_{BJ}(\theta) = V_{ds,DC} + (V_{ds,DC} - V_k)(1 - \beta\cos\theta - \alpha\sin\theta + \frac{\alpha\beta}{2}\sin 2\theta) \qquad 4.2$$

However, using ADS CAD software, the voltage waveforms are all cosine based and the elements need defining accordingly. The –cos θ term is created by cos(180+θ), the –sin θ term is created by cos(90+θ) and the +sin 2θ term is created by cos(-90+2θ).

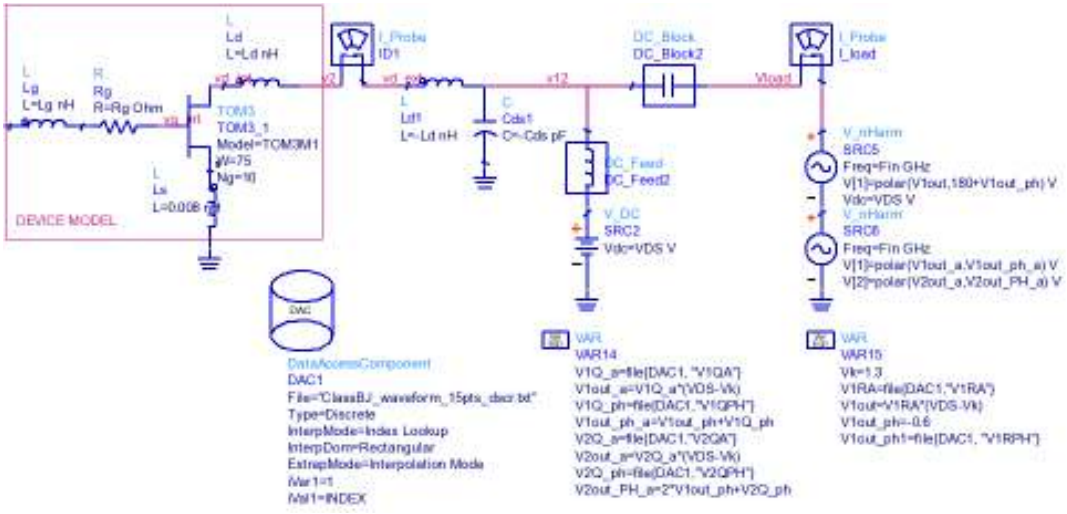


Figure 4.15 Voltage source schematic set-up in ADS used to define the output Class BJ waveforms

The resulting simulation circuit is shown in Figure 4.15 showing the output voltage sources. In the simulation, voltage source values are controlled by a Data Access Component defining discrete steps in the Class J operating space.

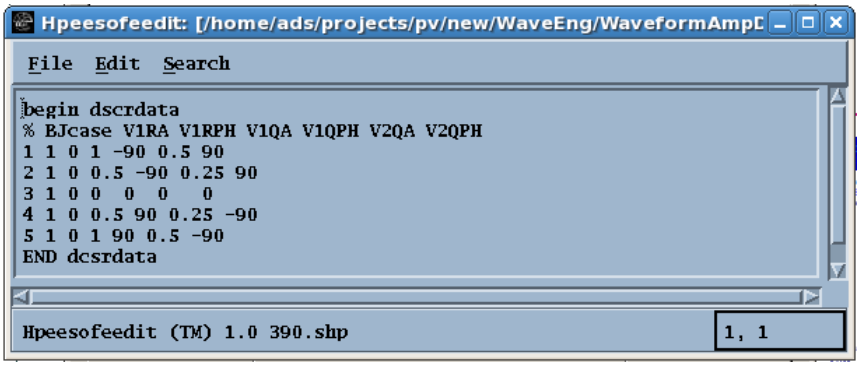


Figure 4.16 Voltage source data file used to read Class BJ waveform coefficients in ADS. Five states are defined for the range -1<α<1.

The resulting simulated waveform set is shown in Figure 4.17 for the simulation circuit and dataset definition detailed in Figure 4.15 and Figure 4.16.

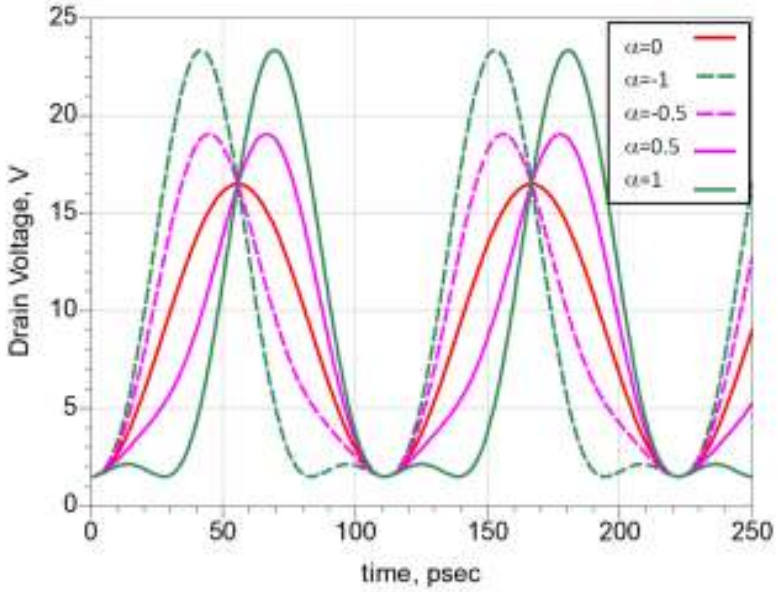


Figure 4.17 Class BJ voltage waveforms (4.2) simulated in ADS using the circuit form Figure 4.15 with V_{ds}=9V, V_k=1.3V, β=1, -1<α<1 at 9GHz

Taking this simulation approach, the fundamental and harmonic impedances can be derived simply from the voltage and current waveforms on the device intrinsic planes

rather than rely on the load pull approach. The design problem then becomes one of simply synthesising the required impedances.

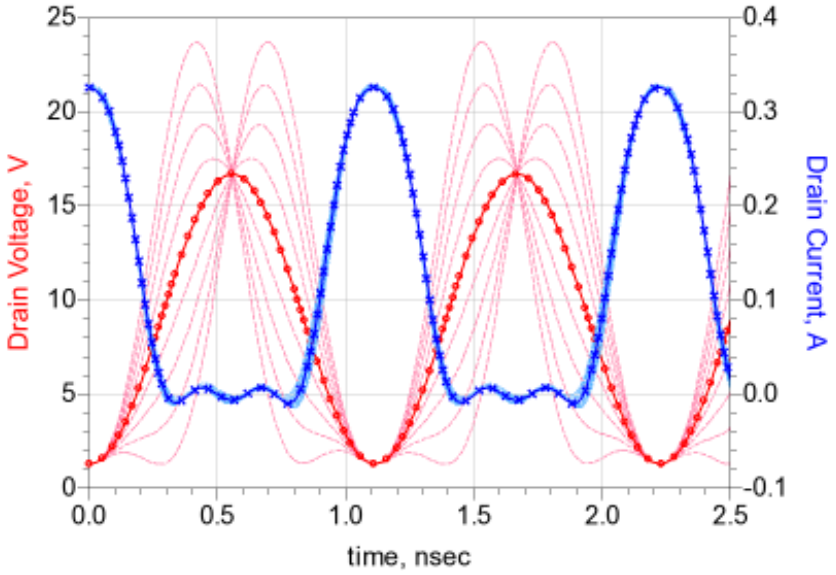


Figure 4.18 Drain waveforms for the FD30 10x75 device driven from voltage sources defining the Class BJ continuum (for the range -1<α<1 in 0.25 steps) at 0.9GHz. Bold trace denotes the classB case, α =0

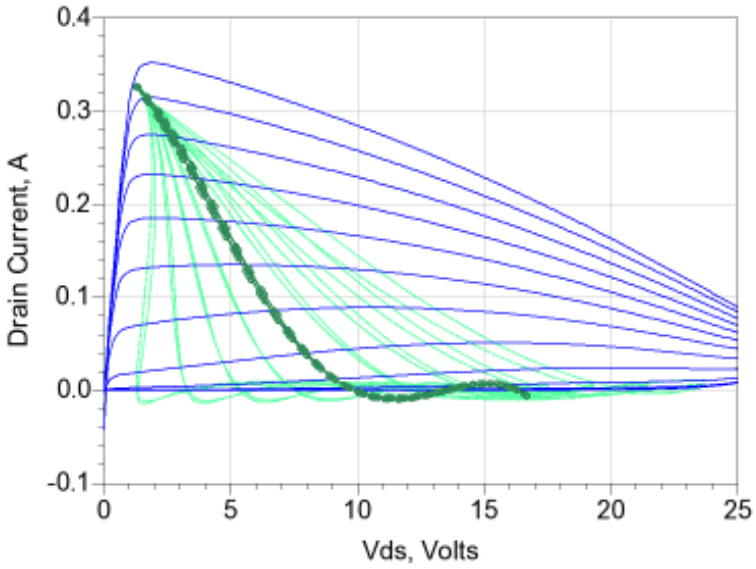


Figure 4.19 Load lines for the Class BJ continuum at 0.9GHz (for the range -1<α<+1 in 0.25 steps) at 0.9GHz. Bold trace denotes the classB case, α =0

The results in Figure 4.18 show the waveforms for the drain current are independent of the drain voltage applied in the BJ continuum.

The impedances described by this waveform set are shown in Figure 4.20. They show close correlation to the ideal impedances but there is some movement away from the edge of the Smith Chart. This is traced to the minor differences in the current pulse shape from the ideal clipped sinewave.

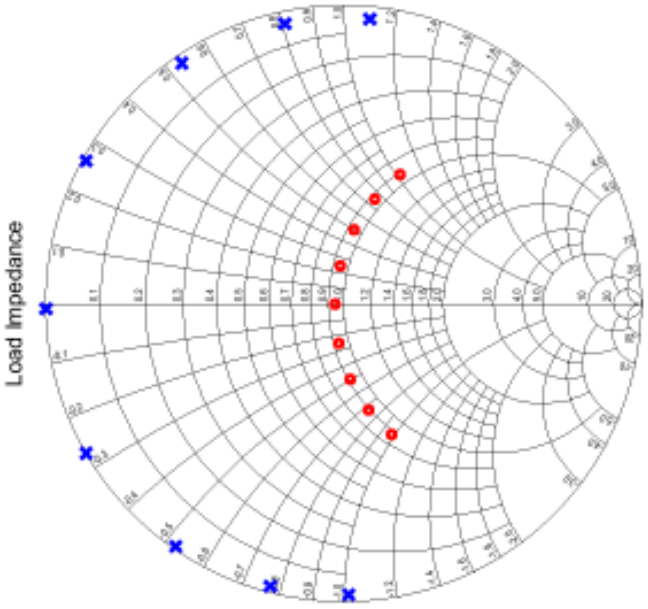


Figure 4.20 Load impedances for the FD30 10x75 simulated circuit at 0.9GHz showing very close correlation to the ideal class J waveform impedances [18].

The waveforms have a further degree of freedom with the phase relationship between the output waveforms and the input drive voltage. These results are shown in Figure 4.21.

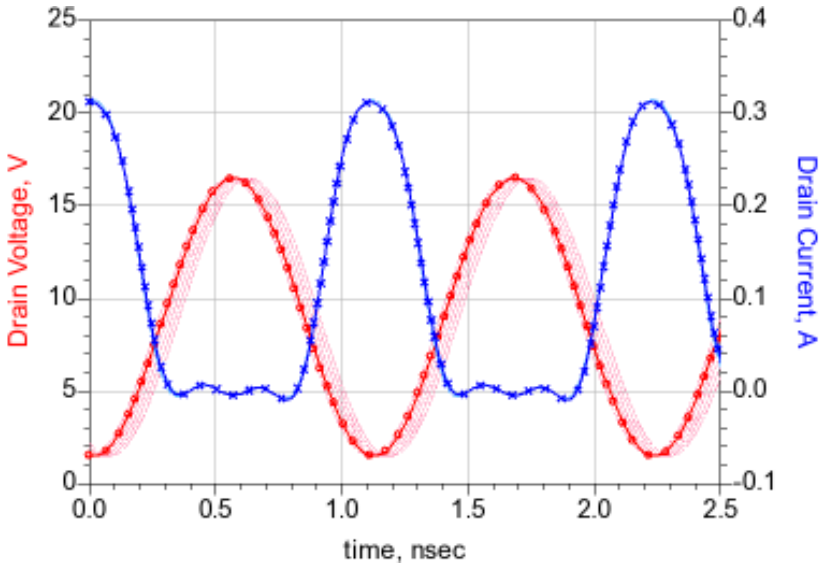


Figure 4.21 Waveforms for swept output voltage phase (170 to 190) at 0.9GHz using Vn source drive.

4.2.5 Waveform simulation method for de-embedding 'in-circuit'

The use of network elements as a 'pre-distortion' network in the previous section has shown that the waveforms for correct operation are known and the excitation can be modified to force the correct internal voltages on the transistor. In a reciprocal method, this technique can be applied to find the intrinsic transistor waveforms from a circuit node without post processing the data to de-embed the waveforms.

During simulation, the voltages and currents at the intrinsic device plane are related to the input driving signals, modified through the extrinsic parasitic shell. Using two dummy networks in series, one with 'positive' element values of the device extrinsic components, followed by a 'negative' value extrinsic network the overall circuit remains unchanged. However, virtual voltage and current probes can be placed between these two dummy networks and the resulting output will represent the effective intrinsic transistor waveforms, as the network with the positive values will replicate the waveform shifts due to the parasitic elements. The negative network removes this effect so the input voltage into the transistor is as desired by the original circuit.

This method is demonstrated in Figure 4.22 and highlights the gate node used as an example. Here the extrinsic values are considered as R_g and L_g, although any network can be used in practice, from the extraction procedures in section 3.3.

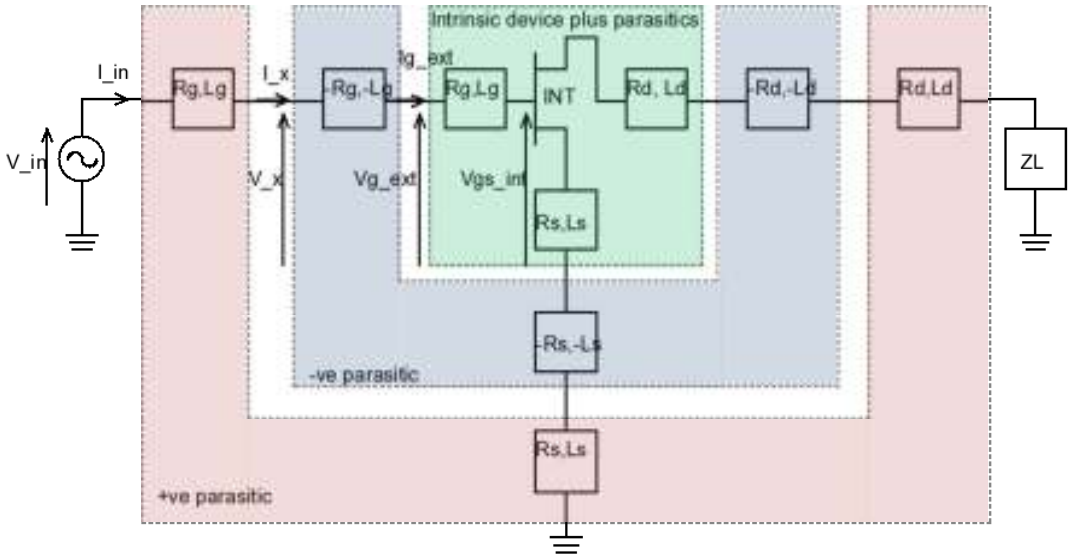


Figure 4.22 Approach to use waveform simulations for de-embedding 'in-circuit'

The voltage into the circuit is here defined by a voltage source (V_in) but this could easily be just the voltage from any other part of a circuit in the design process. The positive Rg/Lg network is followed by a –Rg/–Lg which negates the overall effect of the dummy network, such that the voltage Vg_ext is identical to V_in. The important feature is the internal dummy node between these networks where the probes V_x and I_x are referred. The response defined here will be identical to the intrinsic node values, Vgs_int and Igs_int.

4.3 Conclusion

The use of voltage sources in the simulation circuit has been demonstrated. This allows the correct waveforms to be placed at the intrinsic nodes of the transistor so that any operating mode can be replicated. This removes the effects of the source impedances and any distortion arising from harmonic current flow through these elements.

This mode of operation can be used tom inspect waveforms directly in the simulator by using the inverse approach. This is a simple and elegant technique which allows insight into the operating modes.

5 RF-IV WAVEFORM ENGINEERING

5.1 Strategies for improving Efficiency

The previous sections have shown there are several blocks to achieving high efficiency HPA performance. Methods to overcome these need to be quantified and discussed to formulate an achievable design methodology. It is clear that the reduced conduction angle, harmonic terminated approach to HPA design has been proven to deliver large benefits in performance, so the following discussion will focus on Class B amplifier designs (or Class B-J as the same problems affect this class of amplifier) to illustrate the concepts.

5.1.1 Output Waveform Engineering

It is well understood that the correct high efficiency power amplifier design strategy involves the engineering of the output RF current and voltage waveforms which involves understanding the optimum loads conditions [28]-[32]. These are generally achieved by using load pull techniques, which can be time consuming and costly. Identification of the correct starting point can minimize this effort and provide a very simple way to analyse the performance without the load pull set-up, or even a non-linear CAD model.

In engineering these output waveforms a simple approach is to use the I_{max} and V_{dmax} of the chosen transistor to determine the appropriate fundamental load impedance (Cripps Load [14]).This is the basis of the derivations in section 2.1.1 to section 2.1.5. Even when acknowledging the knee voltage, the optimum load line is assumed to move from the intersection of the linear and saturated region of the straight line approximation to the Vds max point (Figure 2.3). However, in a practical design the strategic engineering of the output waveforms must take into account the realistic knee region of the transistors I-V characteristics and the piecewise linear approximation needs updating. Modifying the theoretical I-V characteristics slightly to use a simple tanh(x) function, the expression given in equation (5.1) is found.

$$I_{ds} = k.I_{\max} \tanh\left(\frac{V_{ds}}{k}\right) \qquad 5.1$$

This is then used to plot the knee characteristics, rather than the linear approximation, and it shows a more familiar response, Figure 5.1(a). This expression is compared to measured data of the CP FD30 pHEMT and is plotted in Figure 5.1(b). Close agreement between the idealised and measured characteristics is noted which will be adequate for the purposes of a qualitative analysis.

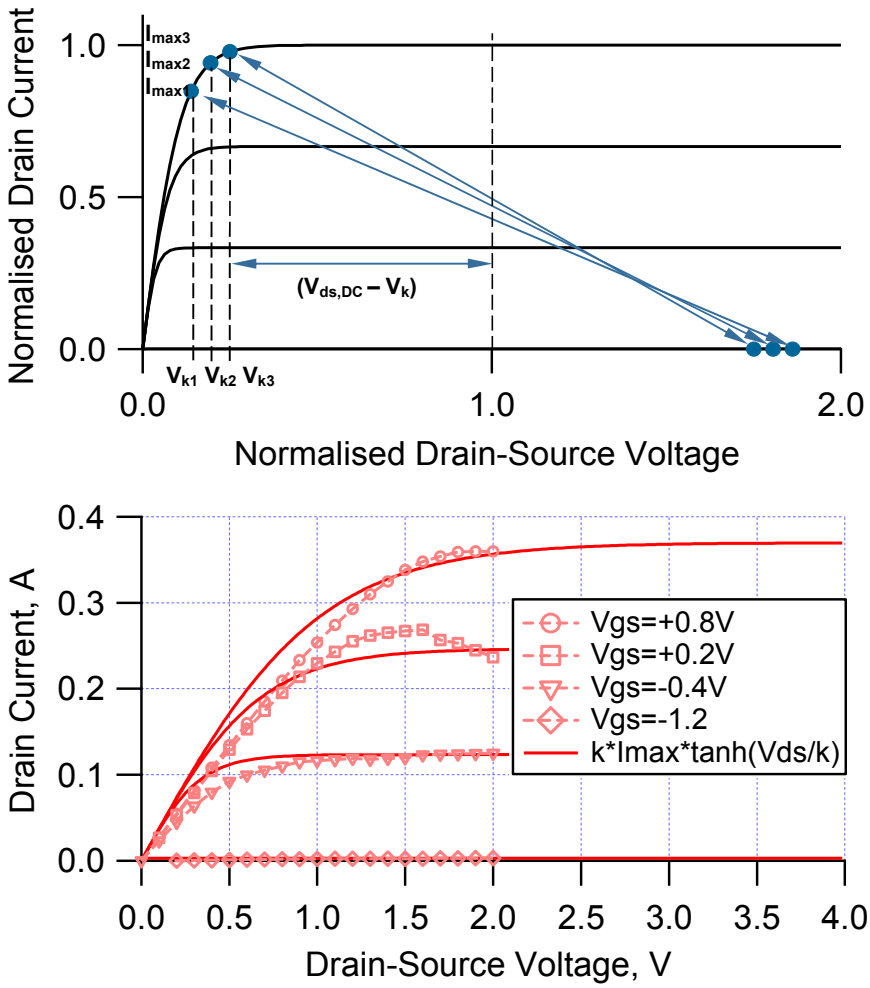


Figure 5.1 FET transfer characteristics (a) Idealised curves using (5.1) and (b) Application of (5.1) to the CP FD30 10x75µm device (58003-09-6948#16 MM1234A J21010)

Using these curves, the choice of knee voltage is now not as clear as the linear approximated case, and the strategy for choice of this load line for efficiency needs more discussion. For example, choice of the operating point within the knee region could be any of the points shown in Figure 5.1(a). Reducing the useable I_{max} minimizes the knee voltage, V_k, and thus improves Drain Efficiency (η_D). The down side of this strategy is that the peak power is reduced. Here the designer must consider the design

aim carefully as choosing an operating point for peak power, for a given rail voltage, is likely to result in significant reduction in the peak drain efficiency due to the knee voltage, irrespective of the operating class of the amplifier. Published work on high efficiency amplifier in the communication bands have shown exceptional efficiencies and power but these are on Gallium Nitride technologies at low (<2GHz) frequencies operating at high >28V rail voltages. This high rail voltage can have the property of reducing the V_k effect. Additionally, the gain is high at these relatively low frequencies meaning the degradation between drain efficiency and power added efficiency (PAE) is minimised. This is not the case at high frequencies, where the both the rail voltage[7] and gain are generally much lower.

A ten finger, 0.75mm (10x75µm) device on the FD30 process was used as a test transistor, with the knee region modeled using (5.1), as shown in Figure 5.1(b). The maximum drain current, I_{max}, of the FD30 process is approximately 450 mA/mm leading to a drain current of 330mA for a 0.75 mm periphery device. Plotting the power output and drain efficiency for different knee voltage end point shows the response in Figure 5.2. This figure shows degradation in efficiency with increasing knee voltage load line end point but this is countered by a relatively constant output power level.

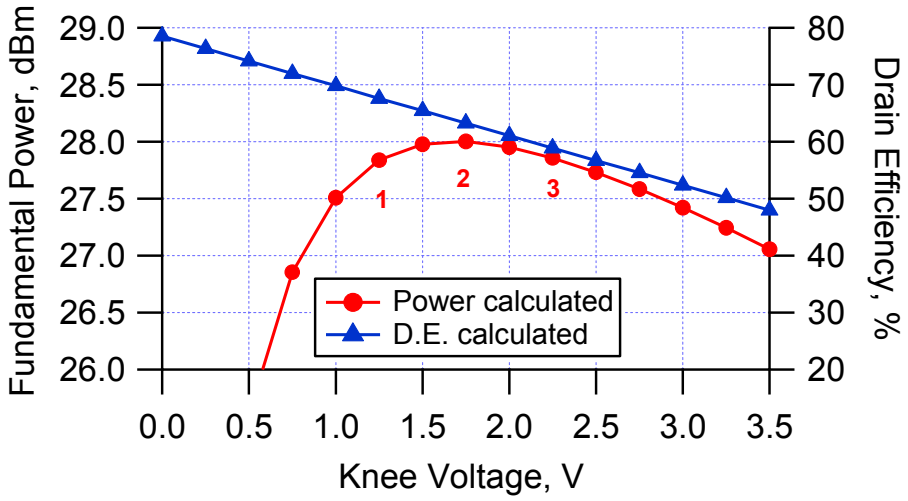


Figure 5.2 Output power and drain efficiency as a function of load line end point knee voltage defined in Figure 5.1(a)

[7] Higher frequency operation can imply a shorter gate length within a device technology and thus a reduction in breakdown voltage hence lowering operating voltages – a more complete assessment of semiconductor technology can be found using the Johnson figure of merit.

Table 5.1 shows the predicted variation in performance resulting from selecting the three different points on the knee region and the transistor set up for Class B operation. While there is a relatively small 0.2 dBm power difference across these loadline endpoints, a significant 8.7% variation in drain efficiency results, providing valuable insight for the designer in the choice of optimum load impedance.

It should be noted that in all cases the efficiency calculated is noticeably less than the theoretical value of 78.5%, highlighting that a ratio $V_k/V_{ds,DC} > 0.1$ causes significant efficiency degradation.

$V_{ds,DC}$=9V, Imax=450mA/mm				
Knee point	**Vk**	**RL**	**Power**	**Drain Efficiency**
Point 1	1.25 V	41.9 Ω	27.8 dBm	67.6%
Point 2	1.75 V	39.2 Ω	28.0 dBm	63.2%
Point 3	2.25 V	36.5 Ω	27.8 dBm	58.9%

Table 5.1 Summary performance of a 10x75 transistor under Class B operation versus knee voltage/Imax load line end point, defined in Figure 5.2

It is obvious from this data that efficiency improvements are, therefore, possible by further reducing the knee voltage. This can be achieved by choosing a lower I_{ds}/V_{ds} curve associated with a reduced peak V_{gs} maximum swing. The drawback of this approach is that the power density available is reduced. This will lead to device up-scaling or require using parallel combining of transistors to deliver the specified RF output power. These solutions both increase the chip area in a MMIC implementation. The second of these options has a dramatic effect on the required chip area as the increased complexity of the combining and matching networks adds an additional chip area penalty. In turn, this larger chip area increase implies a cost increase.

An additional drawback of the increased number of devices relates to the increased loss of the combining network. The improvements possible will therefore be limited by any combining network losses (Figure 2.13) which increase with complexity.

5.2 Power gain under reduced conduction angle operation

In section 2.2.2 power gain was shown to play a key role in maintaining high PAE. Understanding the impact of the device gain is especially important in the case of

reduced conduction angle operation as a less discussed consequence of operating in these amplifier classes is the resulting reduction in gain.

In these operating modes there is an effective reduction of power gain. This can be demonstrated by considering Class B operation. Comparing the input waveforms in Figure 2.2 and Figure 2.3 it is clearly seen that the Class B configuration requires a doubling of the input voltage swing for the same peak output current, Imax, (and hence output power). The drawback of this larger input voltage requirement is it effectively reduces the power gain of the device and results in a degradation of power added efficiency as described by (2.20).

In general, the power gain can be derived as a function of current conduction angle. The fundamental component of output current for reduced conduction angle analysis [13] [17] can be written as:

$$I_1 = \frac{I_{\max}}{2\pi}\left[\frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)}\right] \qquad 5.2$$

Assuming an optimum load condition at the fundamental with the harmonics short circuited, the output voltage will have a fundamental amplitude of ($V_{ds,DC}$–V_k). The output power will therefore be

$$P_{out,AB} = I_1 V_1 = \frac{1}{\sqrt{2}}\frac{I_{\max}}{2\pi}\left[\frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)}\right]\frac{(V_{ds,DC} - V_k)}{\sqrt{2}} \qquad 5.3$$

The expression (5.3) reduces to the Class A case (2.6) when $\alpha=2\pi$.

The input power is related to the fundamental input drive voltage as before (2.5) but modifying for the reduced conduction angle drive it becomes

$$P_{in,AB} \propto V_{gs}^2 = \frac{1}{2}\left[\frac{(V_{gs,\max} - V_P)}{1-\cos(\alpha/2)}\right]^2 \qquad 5.4$$

Thus the power gain for reduced conduction angle operation is given in (5.5) and clearly shows the dependence on conduction angle, α.

$$G_{P,AB} = \left[\frac{P_{out,AB}}{P_{in,AB}}\right] = \frac{I_{\max}}{2\pi}\left[\frac{(\alpha - \sin\alpha)(1-\cos(\alpha/2))}{(V_{gs,\max} - V_P)^2}\right](V_{ds,DC} - V_k) \qquad 5.5$$

Relating the power gain to the Class A condition using (2.6) leads to the following expression for reduced conduction angle gain.

$$\frac{G_{P,AB}}{G_{P,A}} = \frac{I_{\max}}{2\pi}\left[\frac{(\alpha - \sin\alpha)(1-\cos(\alpha/2))}{(V_{gs,\max} - V_P)^2}\right](V_{ds,DC} - V_k)\frac{(V_{gs,\max} - V_P)^2}{2I_{\max}(1-\beta)V_{ds,DC}} \qquad 5.6$$

$$\frac{G_{P,AB}}{G_{P,A}} = \frac{(\alpha - \sin\alpha)(1-\cos(\alpha/2))}{4\pi} \qquad 5.7$$

The expression (5.7) is plotted in Figure 5.3 and shows the effect of the reduced conduction angle operation on gain, showing the often quoted 6dB lower gain at Class B operation (conduction angle=180°) compared to Class A.

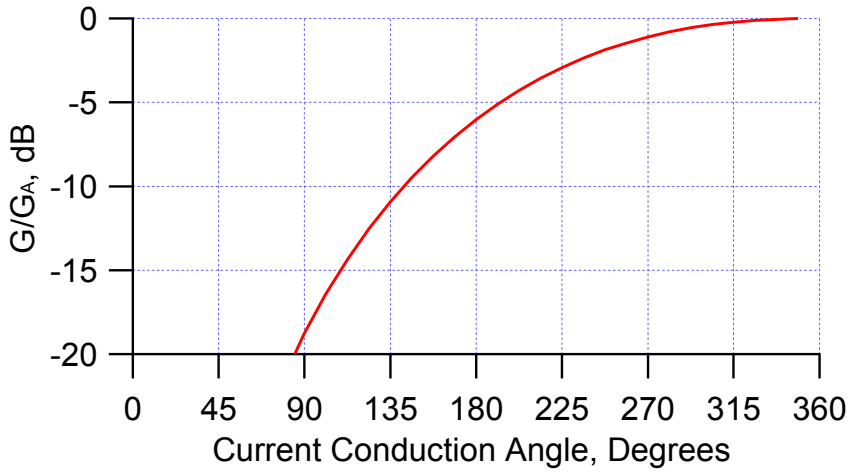


Figure 5.3 Device gain, G, relative to Class A versus current conduction angle (CCA)

This effect is particularly significant where the device gain is limited, for example, at high frequencies relative to the cut-off frequency, f_T, the gain reduces and the power added efficiency suffers, hence the reluctance to use this mode of operation at high frequencies, X-band and above, where the intrinsic device gain limitations can seriously degrade the PAE. For example, typical MMIC processes at above X-band show

transistors with only a modest gain of 6-9 dB, thus any further reduction in gain will have a very detrimental effect on PAE.

This effective reduced gain will be common to all reduced conduction angle operation – including Classes J and F as it is dependent on the input drive constraints and bias point, not the output matching configuration.

It is interesting to note the increased input power requirement for the reduced conduction angle modes (Classes B, J, F etc.) is rarely mentioned in lower frequency amplifier designs, where the device gain is 15dB-20dB or more. In these publications the efficiency quoted is generally limited to Drain Efficiency, η_D and the PAE is not mentioned but this cannot be done in the case of high frequency designs as the PAE is modified significantly with gain.

5.3 Device Input Impedance Effects

The general amplifier theory of section 2.1 shows the classical results derived from some basic assumptions. These simplifications are well understood at the output of the terminals of the transistor. It has also been demonstrated that, with the addition of some minor corrections to the simplistic IV model, e.g. the effect of the knee voltage (section 2.2.1), these equations represent the device well. However, the input side of the transistor is neglected and the resulting equations assume a fixed input impedance which can be seriously in error.

In reality, capacitive effects at the input of the device can seriously undermine the validity of these basic equations and lead to incorrect assumptions on the design of amplifier circuits.

The fixed input analysis of reduction conduction angle operation indicates a 6dB gain reduction[102][103] when biasing in Class B relative to Class A, as shown in Figure 5.3. This is based on the assumptions that the input impedance is:

1. Unchanged with dc bias point (no voltage dependence) and
2. Fixed and constant for the entire input drive voltage swing. In the case of a FET device (MESFET or HEMT), this assumes a fixed capacitance.

Under these conditions, when the fundamental input voltage doubles, as required in Class B by the need to drive from the pinch-off voltage to the maximum gate voltage $V_{gs,max}$, (as opposed to the swing between V_p and $V_{gs,max}$ for Class A) the fundamental input current doubles. This implies a fourfold increase in input power for the same output power i.e. a 6dB reduction in device power gain relative to Class A operation. This gain reduction has a dramatic effect on the power added efficiency (PAE) of an amplifier stage where device gain is inherently low.

In practice, the factors affecting device gain need consideration to give an accurate indication of system performance. This leads to the requirement for a better understanding of the impact of non-ideal device input impedance.

5.3.1 MESFET Gate capacitance

The basic MESFET geometry is shown in Figure 5.4 where A is the active layer (doped semiconductor) thickness, and L_G, the gate length. The gate forms a Schottky junction with the semiconductor (here n-type material) and a depletion region below the gate forms. The gate capacitance of a MESFET transistor can then be derived from the analysis of a simple Metal-Semiconductor (Schottky) junction [104][107]. In fact, the junction capacitance of a MESFET can be approximated to two connected Schottky diode junction across the Gate-Source and Gate-Drain terminals, respectively.

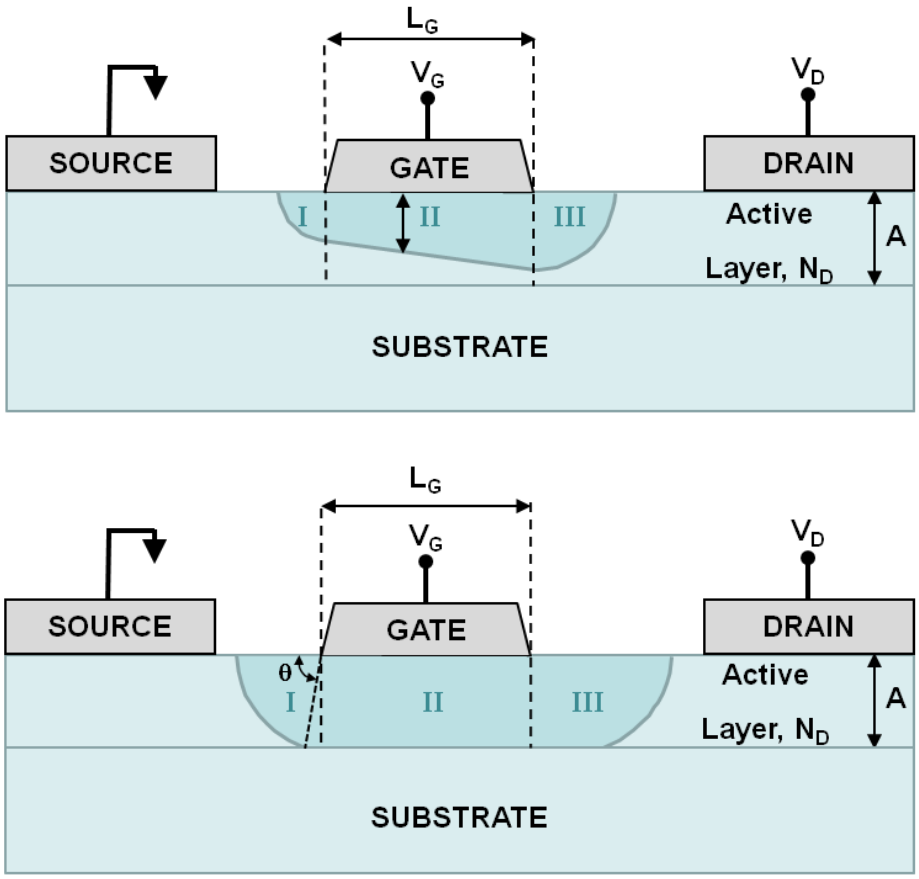


Figure 5.4 Basic MESFET cross section and depletion layer definition for Gate capacitance derivation (a) above pinch-off condition and (b) below pinch-off.

This approach has been used in SPICE simulators [104][108] for the JFET model which has been used successfully to simulate MESFET circuits. The basic model for the Schottky junction capacitance [104] is given by

$$C(V) = \sqrt{\frac{q\varepsilon_s N_d}{2(V_{bi} - V_a)}} = \frac{C_{j0}}{\sqrt{\left(1 - \frac{V_a}{V_{bi}}\right)}} \qquad 5.8$$

where C_{j0} is the zero bias capacitance of the junction and V_a is the applied gate bias voltage. The simplistic model has some modifications due to the asymmetry of the bias voltages on the source and drain terminals and the saturation velocity of carriers, which modify the geometry of the depletion region under the gate. Nevertheless, the form of the capacitance is still defined by the general definition in (5.8). The capacitance can be determined by the amount of charge stored as a function of bias. Under normal amplifier biasing arrangements the (Vgs<0V, Vds>0) there is a change in geometry of the depletion region. In the linear region of operation the charge is obtained by using the gradual channel approximation across the whole gate length, that is, the depletion layer beneath the gate varies linearly along the gate length.

A more important point on the validity of this approximation shows that the resulting expression for the capacitance is wholly inadequate at voltages lower than the threshold voltage i.e. it does not predict the sudden reduction in capacitance at pinch-off. A better model is required.

Below pinch-off the active channel is totally depleted and the depletion layer directly under the gate (see Figure 5.4 region II) advances rapidly into the substrate (as it is much more lightly doped than the active layer). The capacitance is then effectively only defined only by the sidewalls (Figure 5.4 regions I and III), i.e. the extension of the depletion regions beyond the gate [109]. This component varies little with bias and the capacitance remains almost constant at a low value. The overall response is shown in Figure 5.5 and compared to the simple Schottky diode model.

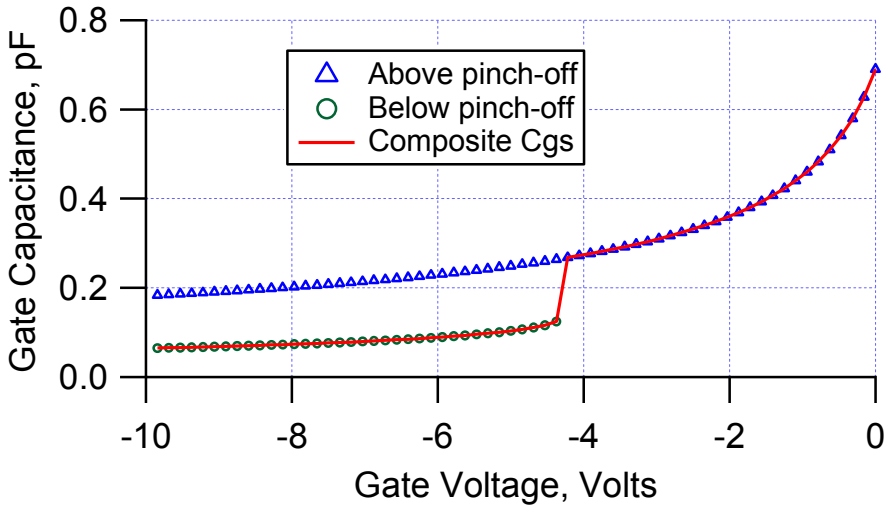


Figure 5.5 Gate-Source capacitance profile of a MESFET derived from Schottky junction capacitance model above pinch-off [104][108][109] and the sidewall capacitance [108][109] below pinch-off

The discontinuity at the pinch-off voltage is less severe in practice as the depletion layer concentration does not change abruptly at the boundary. Figure 5.6 shows the typical response of this model [108]. This does illustrate the wide variation of the input capacitance in MESFET devices and it is clearly not fixed for any large input voltage swing.

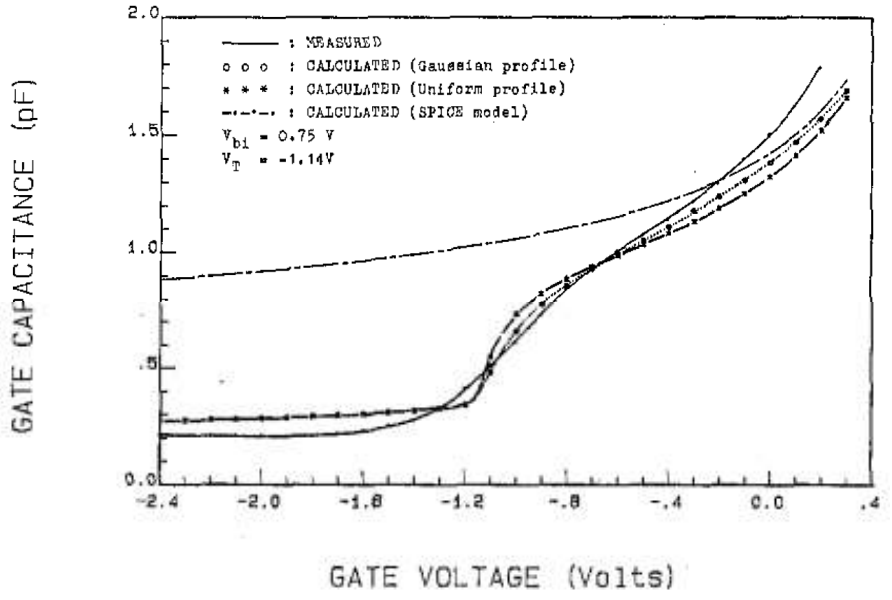


Figure 5.6 Typical response of MESFET Gate capacitance versus the model [108]

5.3.2 HEMT Gate capacitance

The basic structure of a GaAs HEMT is shown in Figure 5.7. The heterojunction between the doped AlGaAs and the undoped GaAs with the spacer layer leads to the formation of a 2-Dimensional Electron Gas (2DEG). The gate capacitance characteristic for the HEMT structure can be analysed using the charge control model [104], which defines the change in concentration of the 2DEG with gate bias, and hence the capacitance profile follows.

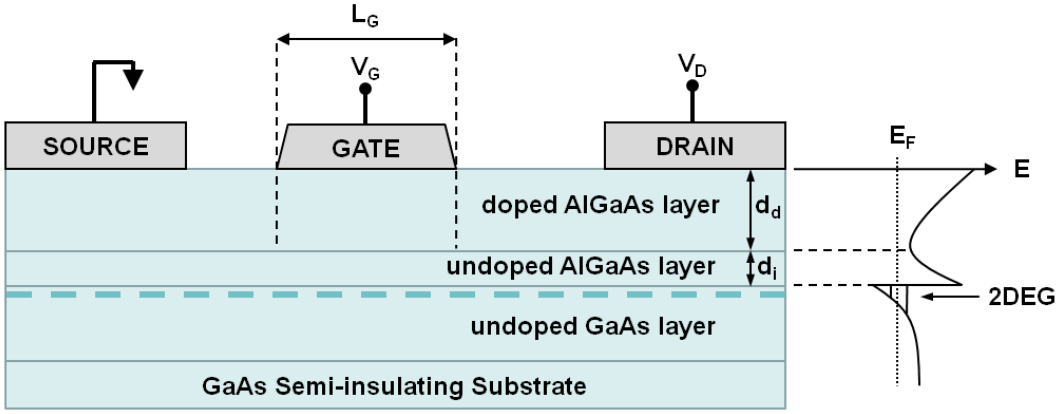


Figure 5.7 GaAs HEMT structure and Energy band diagram.

The carrier concentration for the 2DEG is a function of the bias voltage, and this rises rapidly as the gate bias is increased above pinch-off. This space charge, however, is confined to a specific distance from the Metal-Semiconductor junction, approximately (d_d + d_i) in Figure 5.7, and thus the capacitance remains constant as defined by $C=\varepsilon A/W$, where $W=(d_d + d_i)$.

At reverse bias voltages greater than the pinch-off, the 2DEG disappears and the capacitance drops rapidly, essentially to zero. In reality, the capacitance will reach a low level due to any geometric contribution from the gate-source metal contacts etc.

The combination of these two boundaries on the capacitance defines a step function ranging from 0 below pinch-off to C_0 above pinch-off. This effect is shown in Figure 5.8 for a typical GaAs PHEMT device [104][110].

The model for C-V characteristics is important for understanding the operating principle and the large-signal characteristics of HEMTs.

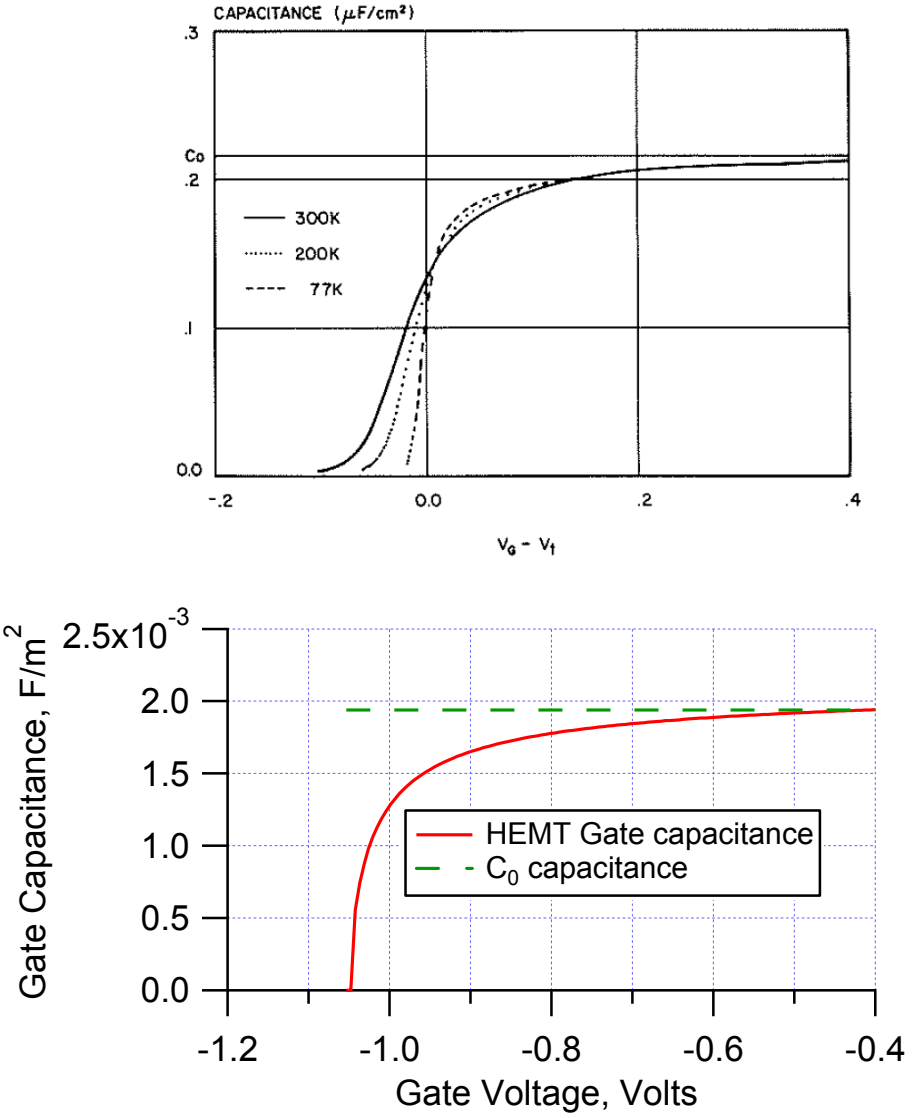


Figure 5.8 Typical C-V characteristics for GaAs HEMT device [104][110]. The capacitance C_0 is the limit defined by the separation of the active layer from the gate.

The gate-source capacitance voltage dependence can cause harmonic generation and these currents flowing through resistances in the circuit cause voltage distortion and affect the linearity of the amplifier at high drive levels when the waveform exercises a large part of the voltage-capacitance characteristic. This is a source of dynamic nonlinearity that creates AM-PM distortion as the phase shift varies with input amplitude.

5.3.3 Gate capacitance effects on device gain

The expressions for the efficiency of the classical amplifier classes (as detailed in sections 2.1.1-2.1.5) now need to be modified to capture the effect of the non-uniform, bias dependent input capacitance of real FET devices.

Taking the example of the HEMT device, a simple model for this bias dependent capacitance would be fixed value, C_0, above pinch-off with a step change at pinch-off from C_0 down to zero, as shown in Figure 5.9. This is a good approximation to the results in Figure 5.8 to allow a qualitative analysis.

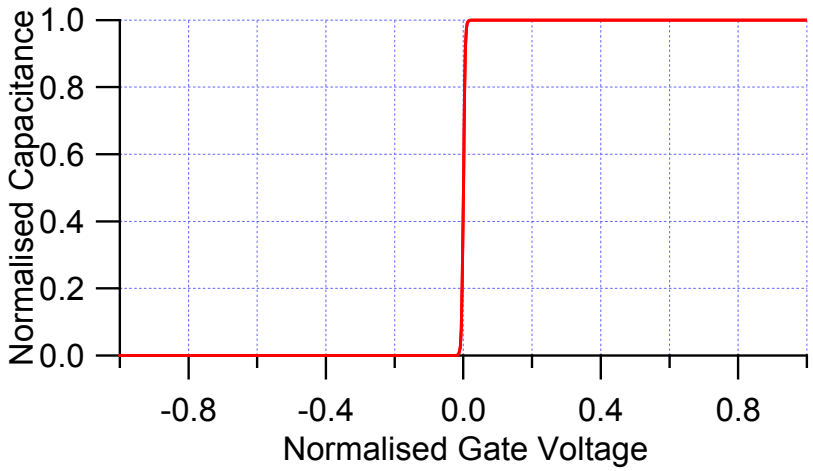


Figure 5.9 Idealised GaAs pHEMT Gate Capacitance model. Pinch-off is defined here as a normalized gate voltage of zero.

This is the ideal case where the off capacitance is zero and hence the ratio C_{off}/C_{on} is also zero. In this case, operating in Class B would result in only 3dB gain reduction relative to Class A, as gate current is only delivered for the voltages above pinch-off. This basic analysis suggests that a reduction in gain between 6 dB (the fixed capacitor assumption) and 3 dB (the ideal stepped capacitor assumption) is expected, the practical value being dependent of the actual C_{off}/C_{on} ratio.

Taking the stepped capacitor model approach and sweeping the C_{off}/C_{on} ratio, shown pictorially in Figure 5.10 (a), the gain response can be plotted.

Figure 5.10 (b) shows gain response and the dependency of the device gain on the actual gate capacitance profile. There is a less obvious point to be considered here in addition to the basic assumption that the use of these reduced conduction angle modes

does reduce gain. The capacitance profile actually places a limit on the gain which can be recovered by circuit techniques or waveform engineering the drive signals.

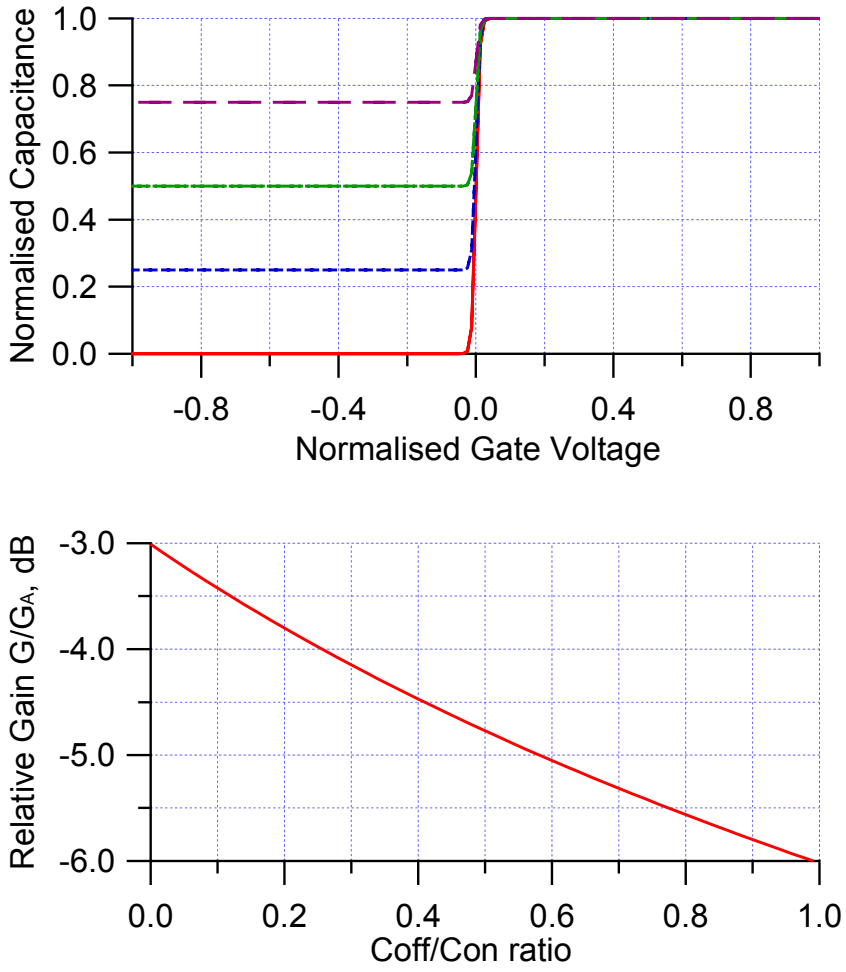


Figure 5.10 Stepped capacitor model showing (a) capacitance C_{off}/C_{on} ratios from 0 to 0.75 and (b) Gain analysis relative to Class A versus gate capacitance ratio under Class B operation.

This approach can be quantified a little more precisely by considering a practical device and refining the analysis.

Measurements were performed on a pHEMT device using the Compound Photonics Ltd FD30 foundry process. The active device was a ten finger transistor with a total gate periphery of 0.75 mm (10x75μm) biased at a drain voltage of 9 V. The gate capacitance of the pHEMT transistor was extracted under large signal drive conditions. The device was operating in Class B and with the optimum fundamental load

impedance and a short circuit at the 2nd and 3rd harmonic frequencies. The extracted gate capacitance results are plotted in Figure 5.11 along with the simple tanh(x) function approximation with a C_{off}/C_{on} ratio of 0.33. This shows good agreement for a very simple approach and can be used to predict the gain profile of the stepped capacitor model.

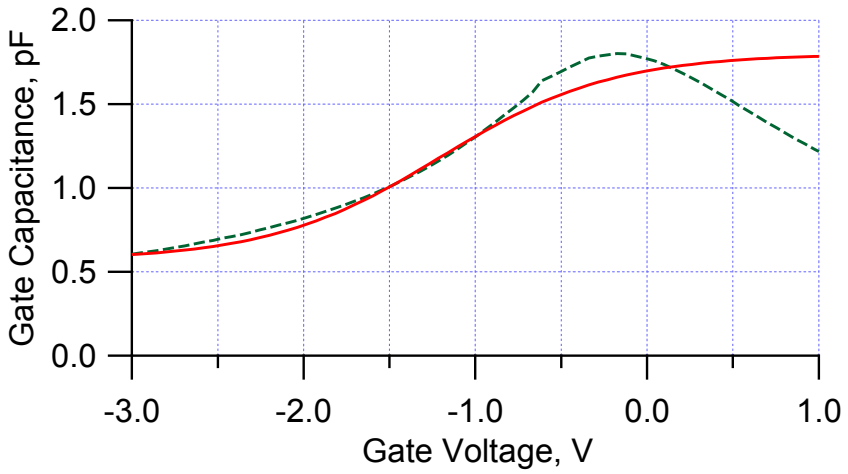


Figure 5.11 Extracted Gate Capacitance for an FD30 10x75 pHEMT (dashed line) and simple tanh(x) approximation with C_{off}/C_{on}=0.33, C_0=1.8pF (solid line)

Using the stepped capacitance model the reduced conduction angle device gain response shown in Figure 5.3 can be updated. The resulting analysis is plotted in Figure 5.12. This shows the classical, fixed capacitor model result (red race) and the ideal stepped capacitor response (green trace) as described by Figure 5.9. These results clearly demonstrate the 6 dB and 3 dB gain reduction predicted at Class B bias (180° conduction angle). More interestingly, the gain profile corresponding to the practical C_{off}/C_{on} ratio of 0.33 (representing the 10x75µm device) is shown, which results in a gain reduction of 4.3 dB at Class B bias.

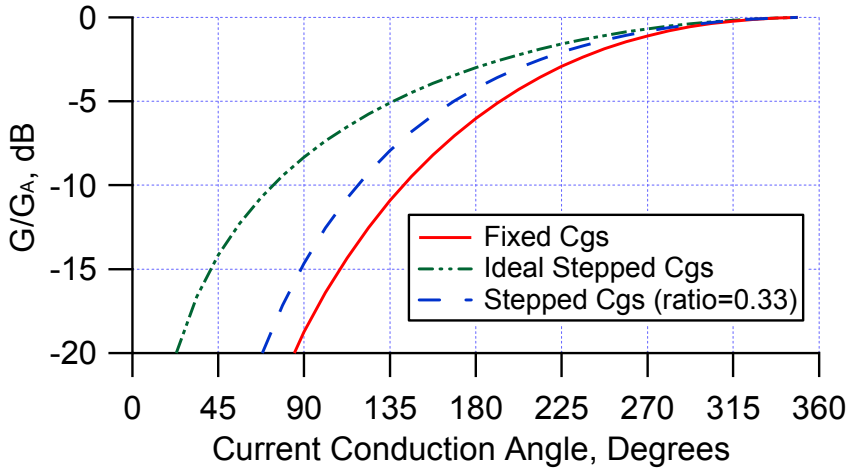


Figure 5.12 Gain relative to Class A versus output current conduction angle (CCA) under sinewave drive for (a) fixed gate capacitor (red trace), and (b) Ideal stepped gate capacitance model (green trace) (c) Stepped Cgs model with Coff ratio=0.33 (blue trace)

These results show that any practical circuit configuration will only be able to recover 4.3dB gain and not the full 6 dB as initially predicted.

5.4 Input Waveform Engineering

Analysis of the waveforms at the input terminal, as described in section 5.3, has shown that it has a direct impact on the gain performance of the amplifier. This aspect of HPA design is largely neglected and the output networks are the main focus of design.

Reviewing the basic assumptions of amplifier operation it can be shown theoretically, any waveform shape below the pinch-off voltage, Vp, can be used without affecting the output drain current shape (Figure 5.13).

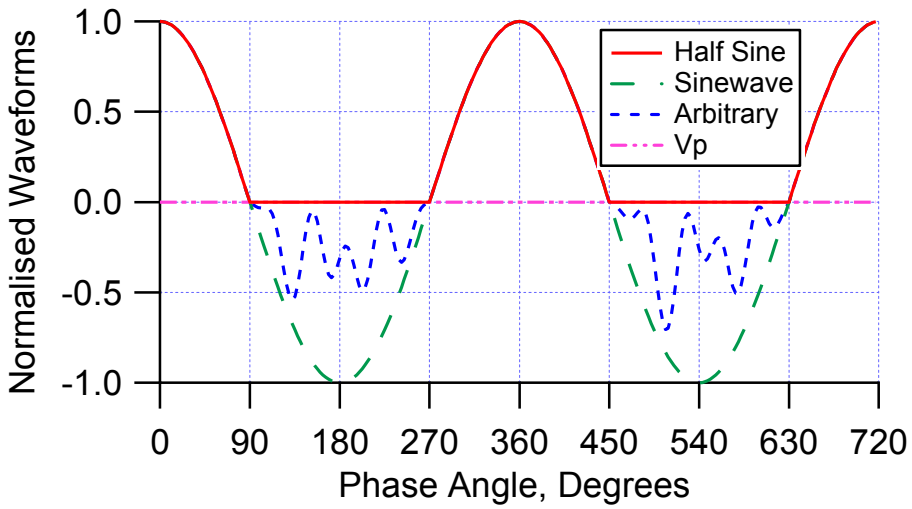


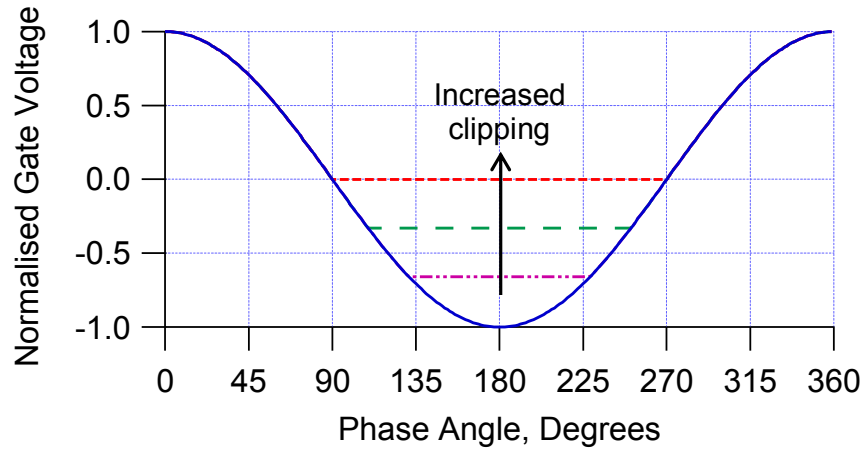
Figure 5.13 Gate waveform shapes delivering the same Drain current shape in a FET device

This is a subtle but obvious point as in the case of the FET devices, the output current follows the gate voltage above pinch-off and is zero below this point.

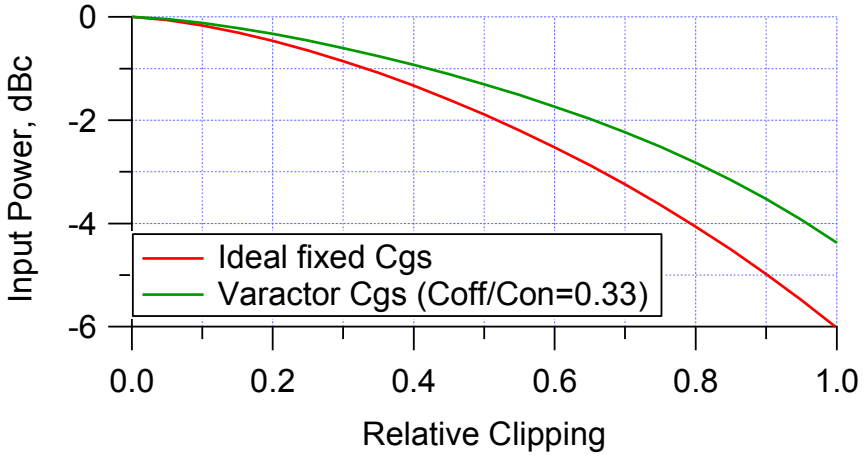
5.4.1 Ideal Waveforms

Taking the simple postulation shown in Figure 5.13 and expanding out with simple waveforms it is obvious that using a sinusoidal input drive signal, with the transistor biased at pinch-off, the negative portion of the input signal can be clipped at any point for an unchanged output current waveform. This is shown in Figure 5.14(a). If the clipping point is moved from zero (unclipped full sinewave) to 1 (half wave rectified drive level) the input fundamental amplitude, and hence input power, can be determined. Sweeping this drive relative clipping point shows that the input signal fundamental component can be reduced relative to Class B (Figure 5.14(b)). As stated

in section 5.3.3, the full 6dB improvement is not possible due to the capacitance ratio of the transistor gate, however, the 4.3dB gain reduction predicted considering a realistic 1:3 Coff/Con ratio can be recovered.



(a)



(b)

Figure 5.14 (a) Input signal showing clipping levels, and (b) drive level requirement relative to Class B with clipped sinewave drive

The use of a clipped sinewave drive is not realistically practical in this form as it implies an infinite bandwidth signal. An alternative approach is required for this method to be practically implemented.

5.4.2 Bandwidth Limited Waveforms

Limiting the bandwidth of the input waveform, the clipped sinewave waveform can be approximated and a useable design approach can be explored.

Using Fourier analysis of an ideal clipped sinewave it is found that the waveform has even harmonic cosine terms. Taking the first two harmonics terms and the a_0 term, a fair approximation of the clipped sinewave drive can be made. The expression (5.9) can be used to describe this system.

$$Vgs(\theta) = A\cos\theta + AK\cos 2\theta + (1 - A - AK) \qquad 5.9$$

The variables A and K can be used to engineer the waveform and maximize performance, where A is the fundamental signal amplitude and K is the relative second harmonic amplitude and the (1-A-AK) term is the dc level. This equation defines the Vgs maximum at unity and the pinch-off at zero. The expression, therefore, only needs to be scaled upto the maximum voltage permissible on the gate, Vgs_{max} and down to the pinch-off voltage, Vp, for the process. This is described by (5.10).

$$Vgs(\theta) = Vgs_{delta}\{A\cos\theta + AK\cos 2\theta + (1 - A - AK)\} + Vp \qquad 5.10$$

where the factor Vgs_{delta}=(Vgs_{max}–Vp) is the difference between the maximum gate voltage Vgs_{max} and the pinch-off voltage, Vp.

Applying the assumption that the drain current follows the gate voltage above pinch-off and setting the transistor current waveforms to zero when the gate voltage falls below Vp, the pinch –off voltage, the Drain current for a transistor driven with a Vgs signal of the form shown in (5.10) is described by (5.11).

$$\left.\begin{array}{ll} ids(\theta) = I_{max}\{A\cos\theta + AK\cos 2\theta + (1 - A - AK)\} & \dfrac{-\alpha}{2} < \theta < \dfrac{+\alpha}{2} \\ ids(\theta) = 0 & \text{elsewhere} \end{array}\right\} \quad 5.11$$

Where α is the conduction angle and is symmetric about the y-axis. The gate voltage and drain current waveforms for these expressions are shown in Figure 5.15.

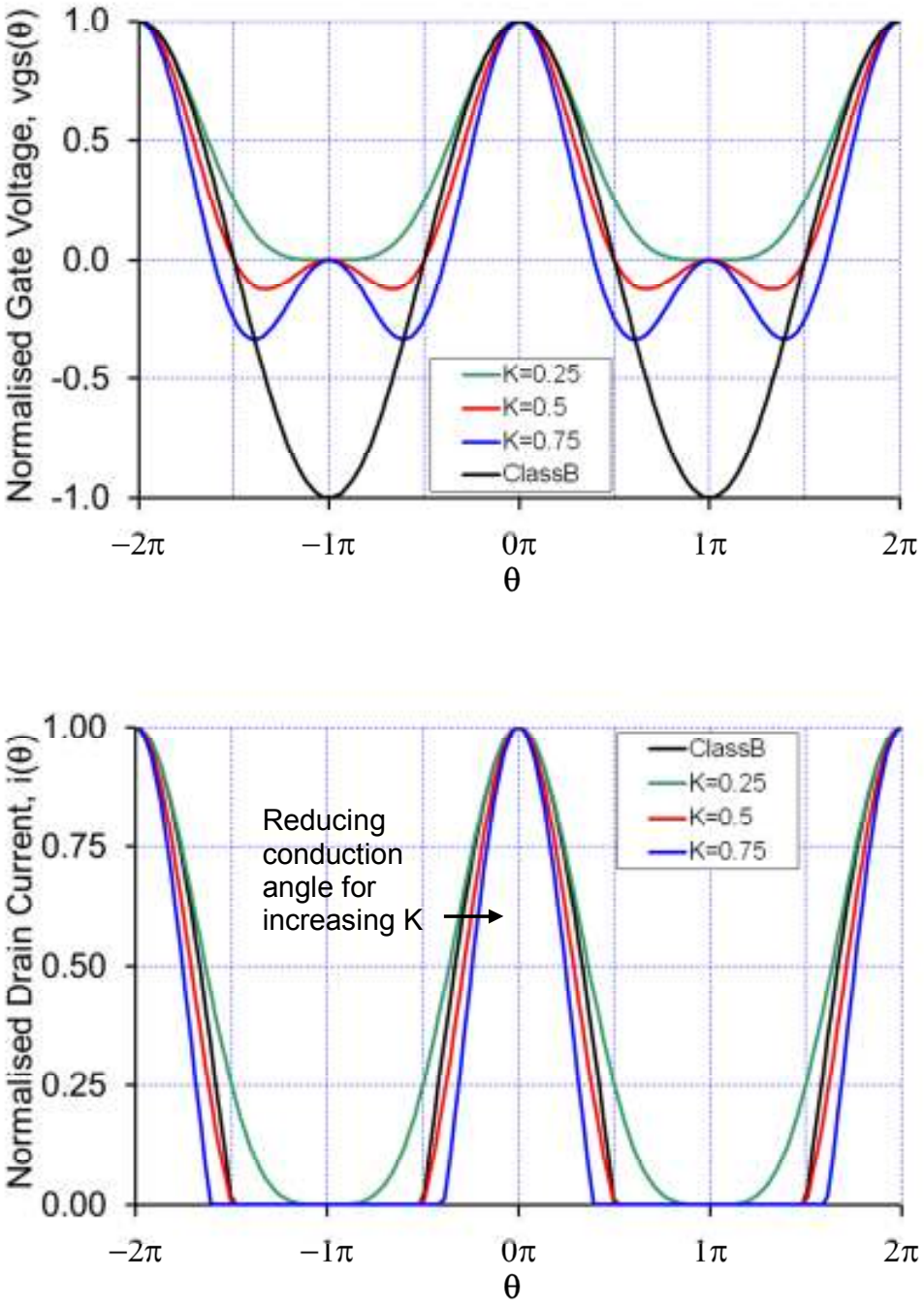


Figure 5.15 Ideal waveform sets (a) Gate voltage from (5.9) and (b) The resulting drain current response resulting from (5.10) showing Ids=0 for negative values of Vgs. (Fixed amplitude A=0.5 and swept K across the range 0.25<K<0.75 and ϕ=0) Plotted also in black is the standard cosθ sinusoidal drive.

There are some interesting features of this voltage waveform (Figure 5.15(a)). Keeping the value of A fixed at a level of 0.5 (as would be the case for the standard Class A amplifier) means the gate voltage swings from Vgs_{max} down to the pinch-off voltage Vp. This is the smallest value of A required to get to pinch-off, which occurs at a phase angle of $\pm\pi$. Adding in the second harmonic shows the current reaches zero at this point even though the function goes negative between these points. It is also the case that the function is always zero at $\pm\pi$ irrespective of the values of K.

Inspection of the waveforms for the current response (Figure 5.15) shows an additional feature. The current pulse is narrower than the usual clipped sinewave, a feature of band limiting the signal to the first two harmonics. Increasing the second harmonic content reduces the current pulse further. This will have an impact in practical amplifier design by effectively requiring an increase in the optimum load impedance for a given voltage swing.

Plotting the response of (5.9) and (5.10) with a fixed second harmonic content and sweeping the fundamental is shown in Figure 5.16. This shows more generally that the value for $Vgs(\theta)$at $\theta=\pi$ is always a constant and defined by the value of A only.

Again, a narrowing of the resulting current pulse observed. This is not as pronounced as the effect of the second harmonic content but still impacts the load impedance optimum.

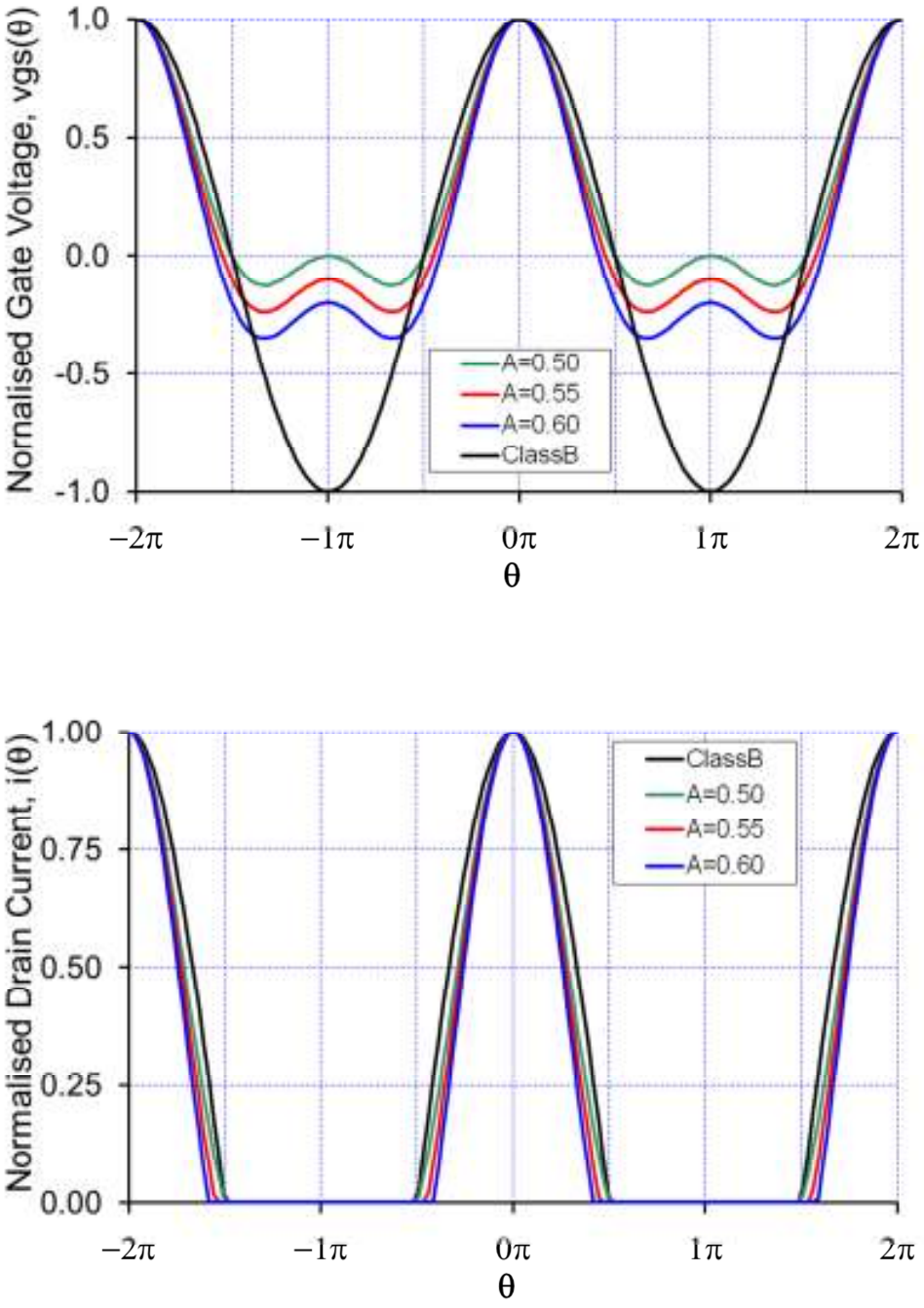


Figure 5.16 Ideal waveform sets (a) Gate voltage from (5.9) and (b) The resulting drain current response resulting from (5.10) showing Ids=0 for negative values of Vgs. (Fixed amplitude K=0.5 and A swept across the range 0.5<A<0.6 and ϕ=0). Plotted also in black is the standard cosθ sinusoidal drive.

Investigation of these drain current waveforms in more detail requires analysis of the harmonic content. The dc level and fundamental of ids(θ) are calculated from the Fourier components, detailed in Appendix A. The dc level is given by (5.12) and the fundamental by (5.13)

$$dc = \frac{I_{\max}}{\pi}\left\{A(\sin\alpha/2) + \frac{AK}{2}\sin\alpha + \frac{(\alpha - \alpha A - \alpha AK)}{2}\right\} \qquad 5.12$$

$$a_1 = \frac{I_{\max}}{\pi}\left\{\frac{A\alpha}{2} + \frac{A}{2}\sin\alpha + AK\sin\left(\frac{3\alpha}{2}\right) + (2 - 2A - AK)\sin\alpha/2\right\} \qquad 5.13$$

From these expressions the drain efficiency, η_D and fundamental output power and optimum load resistance can be determined under the usual assumptions of sinusoidal voltage with all harmonic currents short circuited, for each value of conduction angle.

The value of α, the conduction angle, is a function of A and K and is found by setting (5.11) equal to zero and solving (Appendix A). This provides the zero crossings at ±α/2 and is given by (5.14)

$$(\alpha/2) = \cos^{-1}\left[\frac{-1 \pm \sqrt{(4K+1)^2 - 8\left(\frac{K}{A}\right)}}{4K}\right] \qquad 5.14$$

These equations can now be solved and analysed. The two major variables, A and K, which define the performance can be swept and plotted on a surface which will define the operating space of these waveforms.

The dc component is shown in Figure 5.17. The traditional Class B condition is shown (A=1, K=0) with a value of 0.32 (Imax/π) where Imax here is normalised to 1. It is clear that either increasing the fundamental component or adding in second harmonic content reduces the dc component. If this reduction appears whilst maintaining the fundamental output power, high efficiency operation will result.

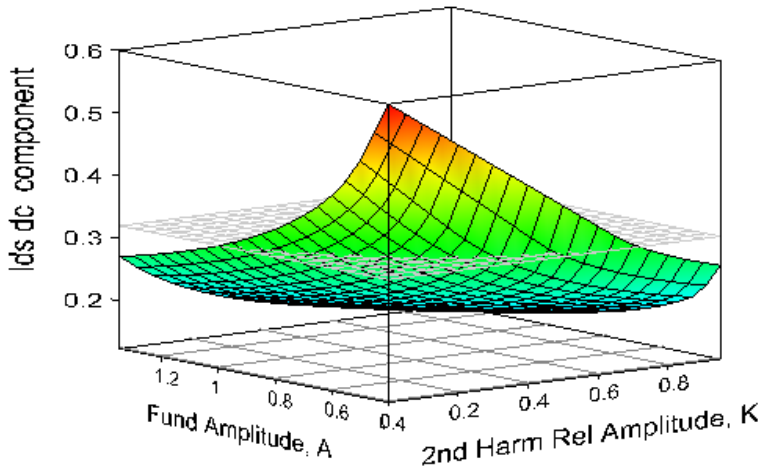


Figure 5.17 DC component – Second harmonic source injection performance, swept A, K. (Reference Class B case also shown)

The fundamental component of current, from (5.13) drives the output power. This result is shown in Figure 5.18. The usual operating space is defined by the bold line at the K=0 axis. This shows the 0.5 fundamental at A=0.5 (Class A) and A=1 (Class B) conditions. It is noted that there is a plateau along the second harmonic amplitude level, along the optimum fundamental amplitude line at of 0.5.

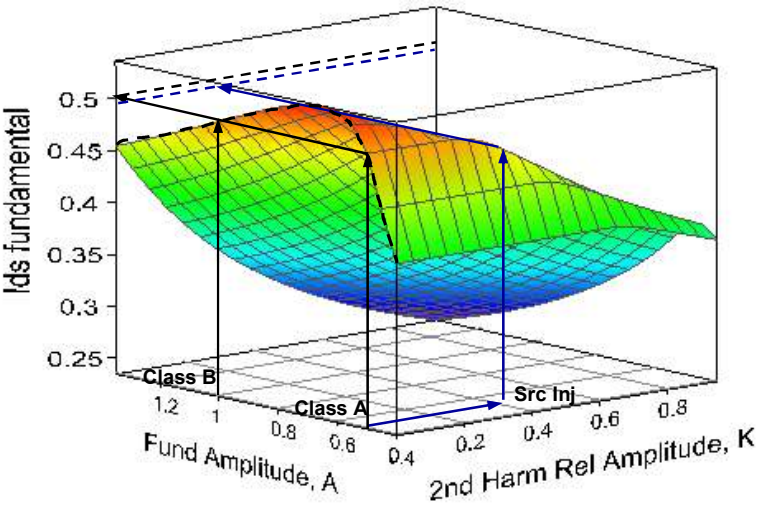


Figure 5.18 Fundamental current component – Second harmonic source injection performance swept A, K showing comparison between Class B and the proposed source injection optimum point (A=0.5, K=0.41)

The drain efficiency can be calculated and plotted as shown in Figure 5.19 with the fixed normalised load impedance of R_L=1 (the class A/class B optimum value).

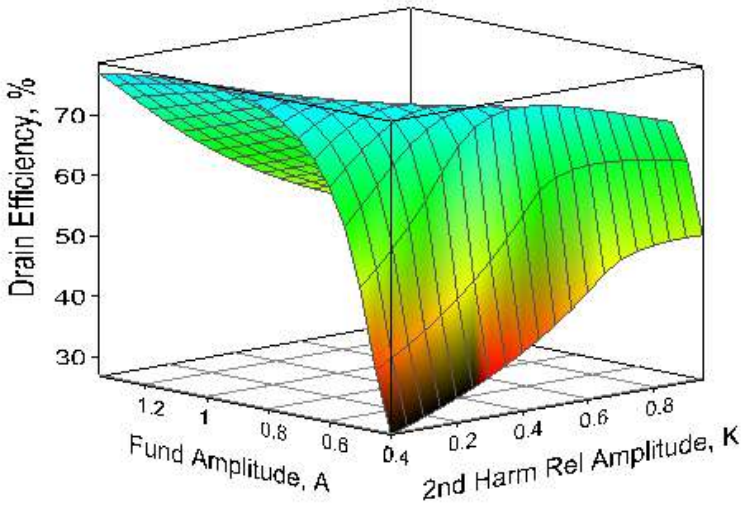


Figure 5.19 Drain Efficiency – Second harmonic source injection performance versus swept A, K – Class B load resistance.

It is clear the efficiency drops off significantly. This is because the load impedance needs optimising to keep the voltage waveform at the maximum value.

The optimum load resistance is calculated and shown in Figure 5.20.

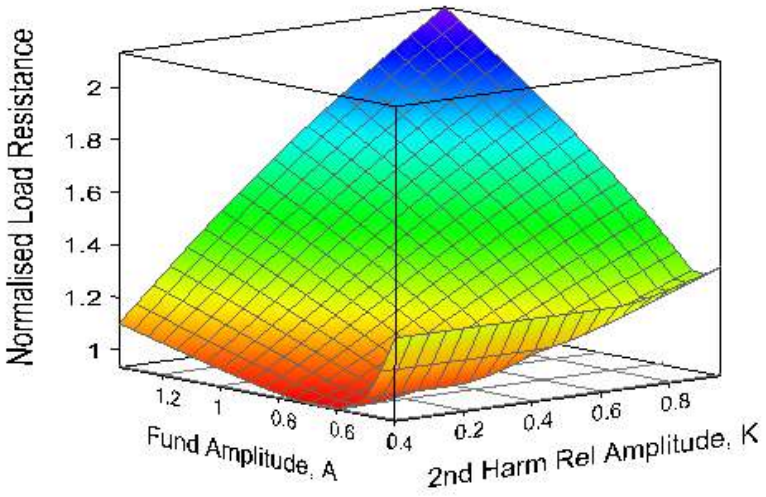


Figure 5.20 Normalised Load resistance to scale Vds to maximum value – Second harmonic source injection performance swept A, K

The classical class AB load resistance is noted along the K=0 axis line. This is plotted here against fundamental amplitude, A, rather than conduction angle as is usually the case [13].

The output power resulting from the fundamental current and optimised load resistance is shown in Figure 5.21 and the Drain efficiency is shown in Figure 5.22.

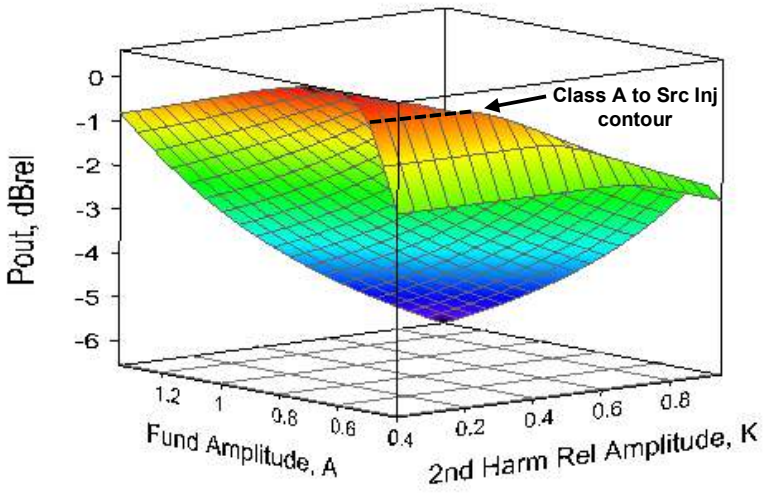


Figure 5.21 Power output relative to class A – Second harmonic source injection performance versus swept A, K – optimised load resistance.

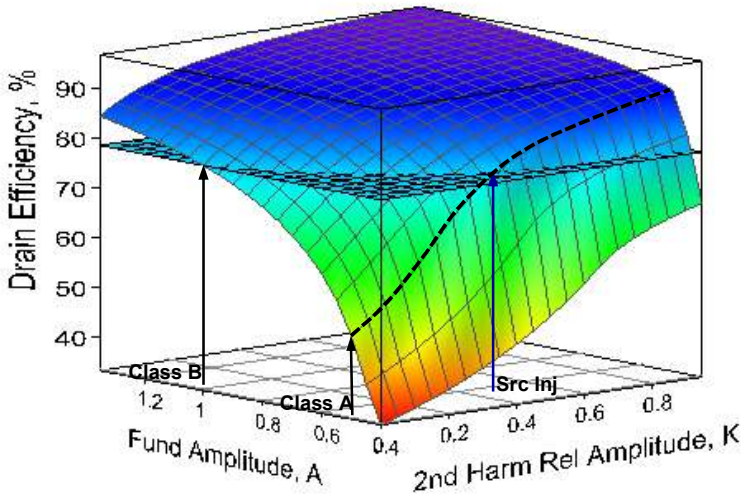


Figure 5.22 Drain Efficiency – Second harmonic source injection performance versus swept A, K – optimised load impedance.

The drain efficiency results, Figure 5.22, show the usual class B operating point and also the optimum source injection mode point, which indicates the drain efficiency can be maintained but with class A fundamental drive levels by the addition of a second harmonic component. . Indeed, there is an improvement noted for any level of second harmonic component identified by the dotted line on the surface plot. This mode of operation therefore has the same power gain as class A along this trajectory.

The efficiency can also be improved significantly, toward 100% for high levels of fundamental amplitude and second harmonic amplitude. This is not surprising as these two cases reduce the conduction angle. This operating mode is similar to moving towards the class C case in traditional theory. The downside of this is the effect on output power which drops (Figure 5.21) rapidly. This surface plot can be considered as the source injection version of the Power Utilisation Factor curve identified in section 2.1.7.

5.4.3 Bandwidth Limited Waveforms with phase offset

Investigating the waveforms more generally and including a phase offset term, the waveform is modified as:

$$\begin{aligned} ids(\theta) &= I_{\max}\{A\cos(\theta)+AK\cos(2\theta+\phi)+(1-A-AK)\} \quad \text{for } \alpha_n < \theta < \alpha_p \\ ids(\theta) &= 0 \quad \text{elsewhere} \end{aligned} \qquad 5.15$$

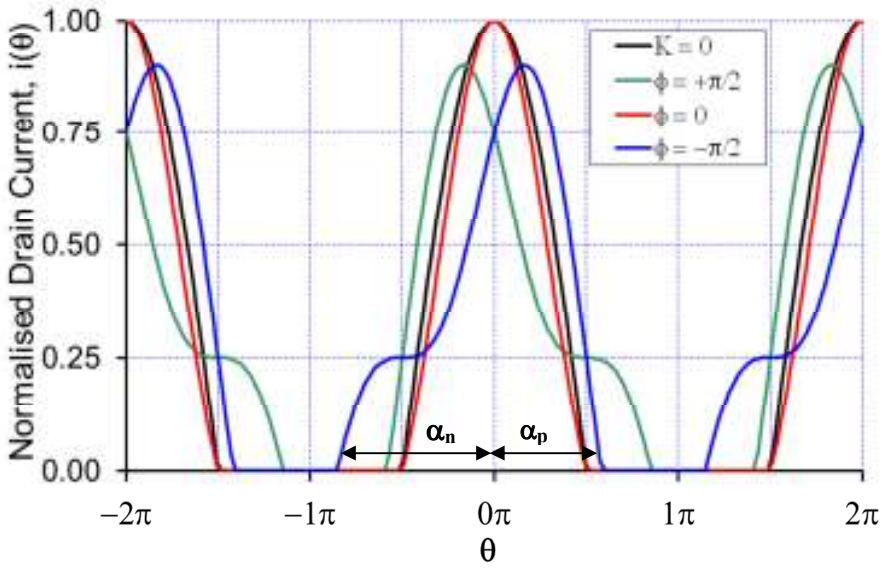


Figure 5.23 Drain current waveforms of the form of (5.15). Fixed amplitude A=0.5 and K=0.5 and ϕ=-90° to +90°. Plotted also in black is the standard cos(θ) current.

The waveforms in Figure 5.23 show that the function is no longer even (the zero crossings each side of zero angle are different) and thus the harmonic components will be comprised of both sine and cosine terms. The corresponding Fourier terms are given by:

$$\begin{aligned} dc = \frac{I_{\max}}{2\pi}\{A(\sin\alpha_p - \sin\alpha_n) + \frac{AK}{2}(\sin(2\alpha_p+\phi) - \sin(2\alpha_n+\phi)) \\ + (1-A-AK)(\alpha_p-\alpha_n)\} \end{aligned} \qquad 5.16$$

The fundamental component of the drain current is given by both a1 and b1 terms:

$$a_1 = \frac{I_{\max}}{\pi}\left\{\begin{array}{l}\frac{A}{4}(\alpha_p - \alpha_n) + \frac{A}{4}(\sin 2\alpha_p - \sin 2\alpha_n) \\ \quad + \frac{AK}{6}(\sin(3\alpha_p + \phi) - \sin(3\alpha_n + \phi)) \\ \quad\quad + \frac{AK}{2}(\sin(\alpha_p + \phi) - \sin(\alpha_n + \phi)) + (1 - A - AK)(\alpha_p + \alpha_n)\end{array}\right\} \qquad 5.17$$

And similarly:

$$b_1 = \frac{I_{\max}}{\pi}\left\{-\frac{A}{4}(\cos 2\alpha_p - \cos 2\alpha_n) - \frac{AK}{6}(\cos(3\alpha_p + \phi) - \cos(3\alpha_n + \phi)) \right. \\ \left. + \frac{AK}{2}(\cos(\alpha_p + \phi) - \cos(\alpha_n + \phi)) - (1 - A - AK)(\cos\alpha_p + \cos\alpha_n)\right\} \qquad 5.18$$

These expressions are complex and little insight is to be gained by looking at the structure. In fact, the expressions (5.16)-(5.18) and the corresponding calculations for the load impedance will just define a family of surfaces (of the form in Figure 5.17 to Figure 5.22) for each value of Φ.

The remainder of this thesis will concentrate on the optimum phase condition (Φ=0) but will reference the effects of relative phase on practical implementation.

5.4.4 Class B amplifier using second harmonic source injection

In order to use this harmonic injection waveform engineering approach in a practical circuit there needs to be some constraints on the actual operating space. There are three variables (A, K, Φ) defined in the dataset. As these sweep, the dc term (and hence biasing level) is also shown to vary. There needs to be some boundaries on the range of these variables for practical implementation in an amplifier circuit. Some simple constraints can be defined based on a basic analysis:

(i) The value of the fundamental should be 0.5<A<1. This covers the operating space from Class A (A=0.5) through Class B (A=1), with a corresponding change to the dc level.

(ii) The relative values of A and K should be defined such that K<1. This defines the second harmonic voltage less than the fundamental.

(iii)The dc level will be fixed for a specific operating condition – and this will be maintained throughout the operating range. Operating in radar and EW systems, adaptive biasing is generally not used, with initial voltages set for the correct operation of the module and held fixed irrespective of the drive power.

Using these basic principles and the voltage simulation method outlined in section 4.2.1, the input drive voltage can be defined in a similar manner to the class BJ output waveform. The voltage sources are used to synthesise the source injection gate waveforms defined by (5.10).

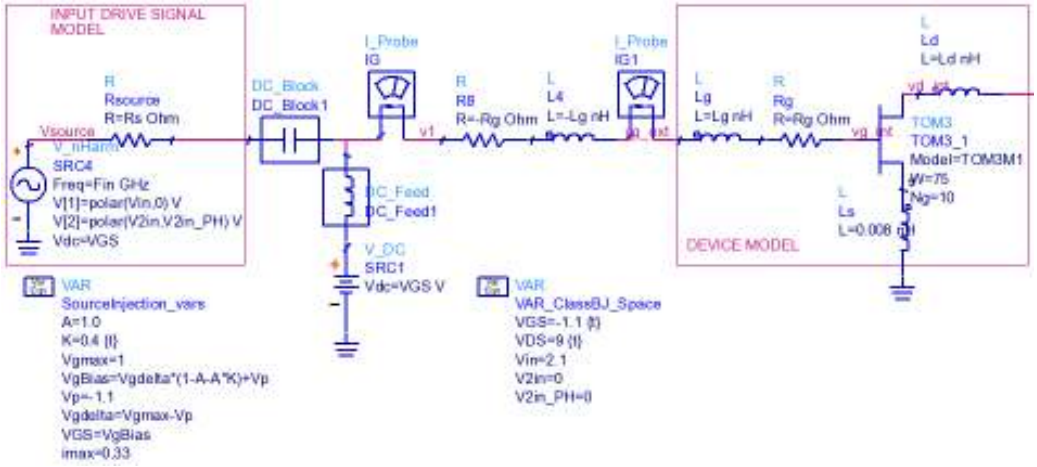


Figure 5.24 Input voltage simulation circuit for the source injection mode of operation, showing the input predistortion network.

The simulation circuit responses are shown in Figure 5.26. Initially the circuit is run at low frequencies (0.9GHz) to minimise the effects of the input-output phase relationship. This Vgs-Vds phase offset is set to 180°, and the waveforms are shown to be close to ideal.

The choice of the low frequency for this analysis was based on the practical viewpoint that there is a factor of 10 between the two cases, allowing a quick and simple direct comparison of the level of the input current waveforms and the time axis by scaling by a factor of 10.

Optimising the phase relationship for 9GHz operation as described in section 4.2.1 gives the results shown in Figure 5.25, requiring the Vgs-Vds phase offset to be set at 170°.

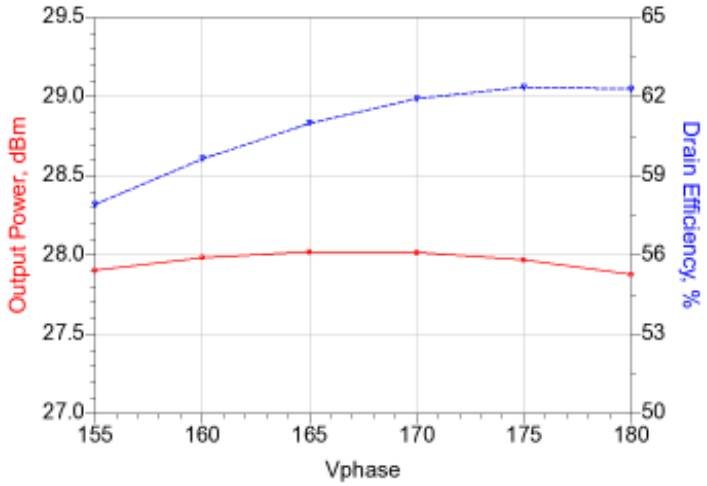
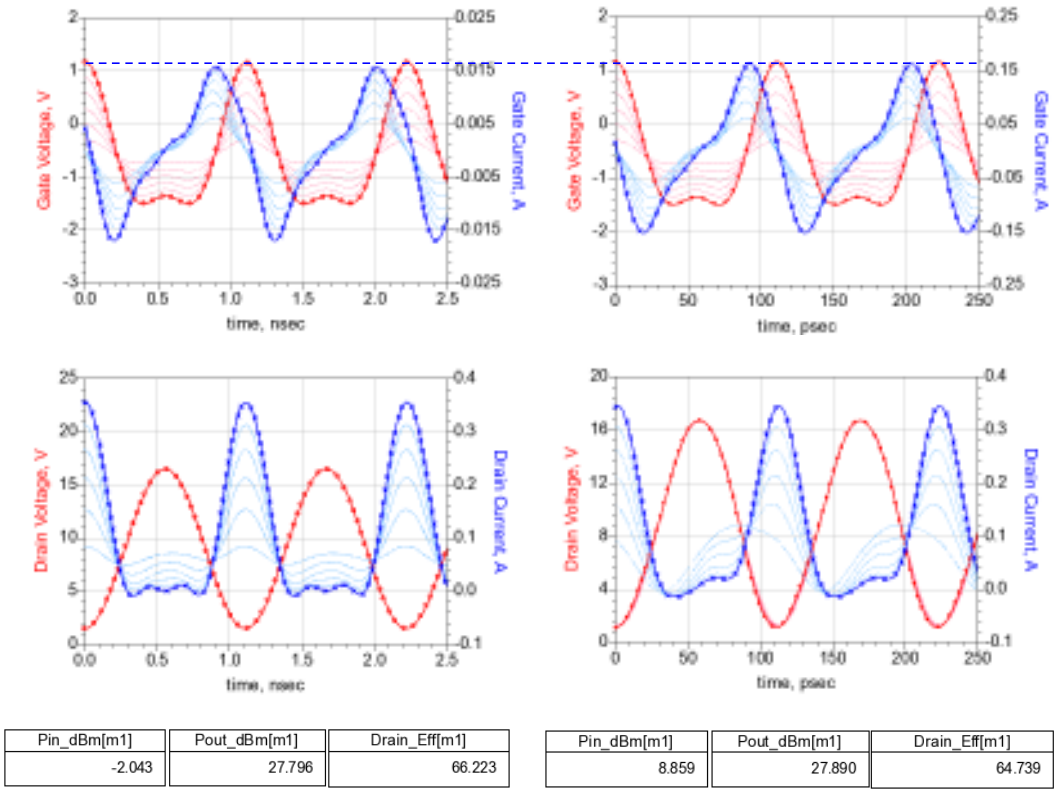


Figure 5.25 Swept operating space for the source injection mode waveforms with phase shift optimising.

Simulating at 9GHz with this optimum phase shift the drain current waveforms are shown to be in error (Figure 5.26(b)). The performance shows the Cds de-embedding to be too aggressive, resulting in the drain current having a slope at the cut-off condition.



Pin_dBm[m1]	Pout_dBm[m1]	Drain_Eff[m1]
-2.043	27.796	66.223

Pin_dBm[m1]	Pout_dBm[m1]	Drain_Eff[m1]
8.859	27.890	64.739

(a) 0.9GHz waveforms (b) 9GHz waveforms

Figure 5.26 Source Injection results for FD30 10x75um transistor driven from a voltage source (swept Vgs_{max} 0.5V to1.0V, bold trace at Vgs_{max}=1V) at 0.9GHz and 9GHz. Cds=0.36pF. This is the intrinsic device plane performance. The waveforms at 9GHz show the de-embedding Cds value is too aggressive.

Using the 2nd Harmonic Source Injection approach the de-embedding capacitance is a different value than the Class B. Initially it seemed the Cgd component – added to de-embed Class B waveforms – is not required in the Source Injection case. Further investigation however showed this to be a result of the different bias condition used for the two operating modes. The gate bias is -0.6V compared to -1.1V for the Class B case and the main non-linear components will be affected. The results of the parameter extraction process of section 3 indicated a bias dependence of the Gate-Drain capacitance as shown in Figure 5.27.

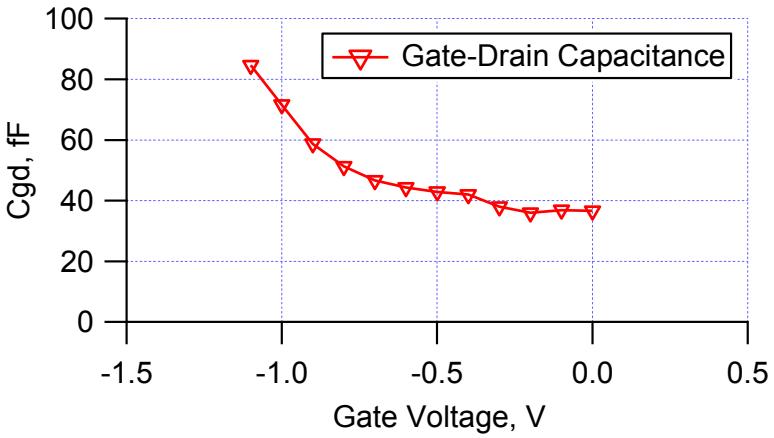
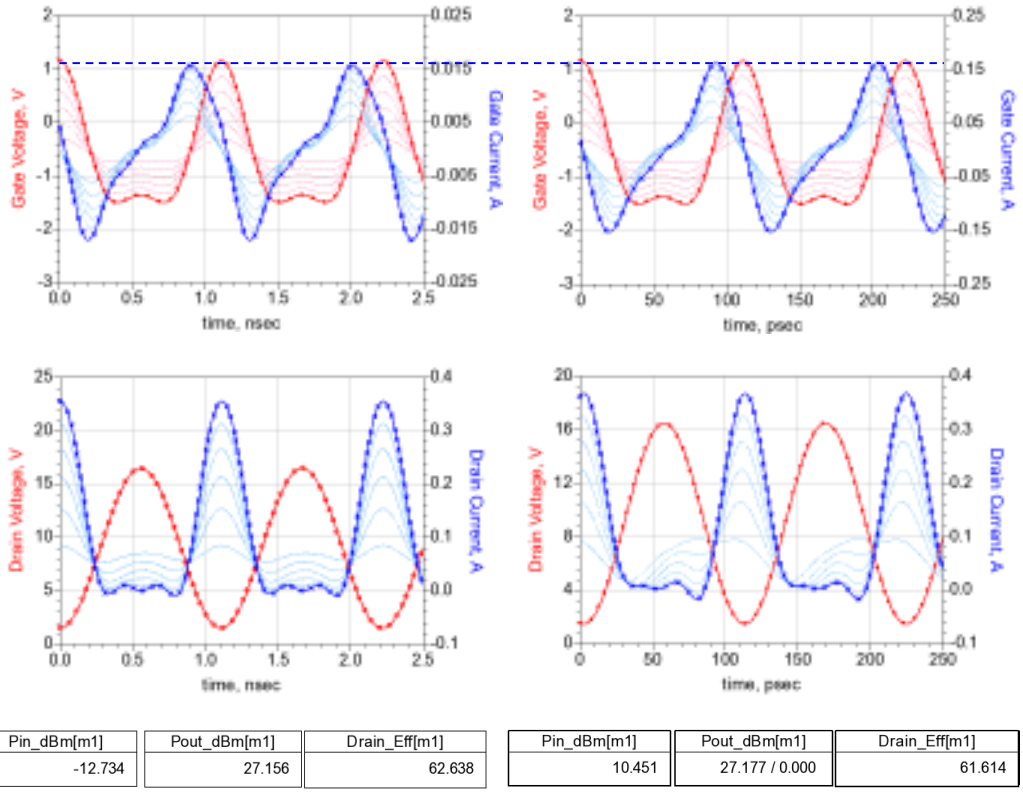


Figure 5.27 FD30 10x75µm device Gate-Drain capacitance versus gate dc bias voltage (Vds=+9V). Data extracted from small signal measurements.



Pin_dBm[m1]	Pout_dBm[m1]	Drain_Eff[m1]
-12.734	27.156	62.638

Pin_dBm[m1]	Pout_dBm[m1]	Drain_Eff[m1]
10.451	27.177 / 0.000	61.614

(a) 0.9GHz waveforms (b) 9GHz waveforms

Figure 5.28 Source Injection results for FD30 10x75um transistor at 0.9GHz and 9GHz, Cds=0.3pF. (swept Vgs_{max} 0.5V to1.0V, bold trace at Vgs_{max}=1V) Here the waveforms are now seen to be largely invariant with frequency.

Reducing the Cds element accordingly shows the resulting output drain current de-embedded waveforms are good, Figure 5.28. There are still some differences which are explained by the other elements in the model which do have some voltage dependence which is not accounted for in the de-embedding model. For example, there is a slight increased Ids peak and some current flow noted in the bottom of the drain current waveform. This is due to the voltage dependence on Cgd and the effect of the harmonic feedback effects which are not present on the class B case.

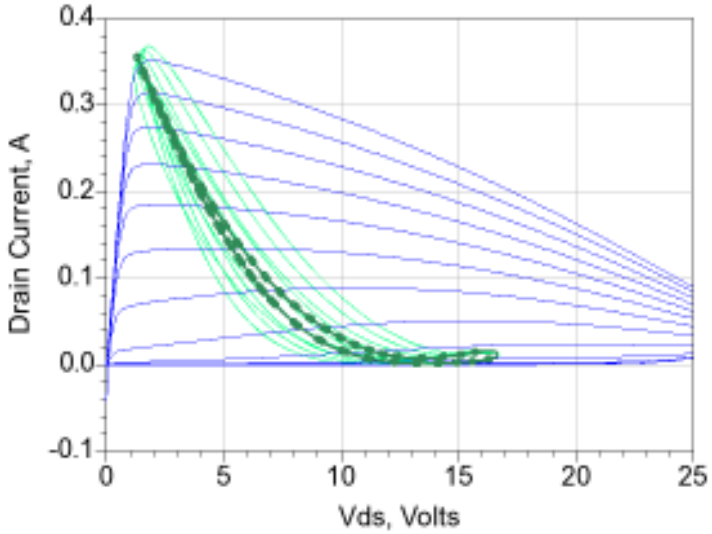
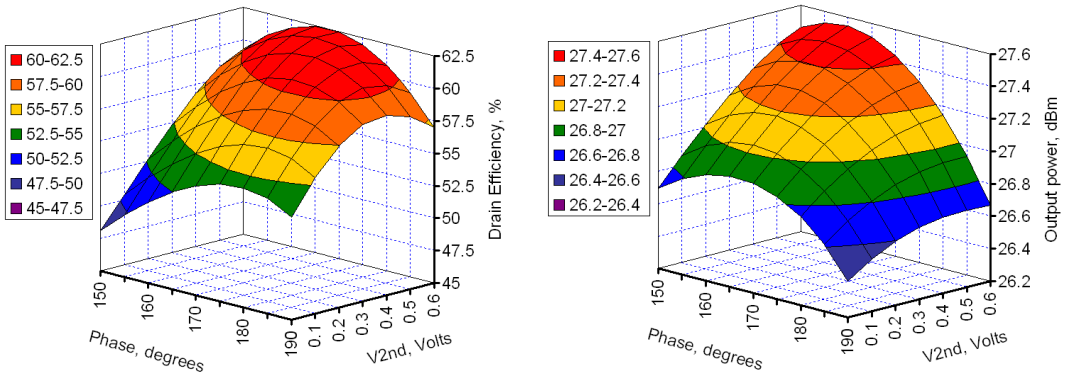


Figure 5.29 Load line for the source injection mode with swept phase shift between Vgs and Vds. Optimum condition (Φ=170°) is shown in bold.

Taking this as the starting point for the simulation, a sensitivity plot for the waveform based approach is created; similar to that outlined in section is used to verify the phase relationship. As previously noted, there are several degrees of freedom when using 2nd harmonic injection is used and the order of the problem increases dramatically. For the simulation, the amplitude of the fundamental, A, is held constant along with the gate bias voltage. The relative level of the 2nd harmonic is stepped whilst sweeping the phase relationship between the fundamental output voltage and the input gate voltage waveforms. This is performed with the defined Cds de-embedding value. The Cds value is a bias dependent parameter and as such is defined in this experiment to be only a

function of Vgs (the Vds voltage waveform is defined to be a fixed value throughout the simulation space by the very nature of the design process using voltage sources).

Initial simulations show the effect of the phase shift at the output (drain) port of the transistor.



(a) Drain Efficiency (b) Output Power

Figure 5.30 FD30 10x75µm transistor driven from a voltage source at 9GHz, Source Injection performance at the intrinsic device plane for swept phase (Fundamental = 1V, Vgs=-0.6V).

These simulations show a compromise of 170° is a good fit across the range of relative 2nd harmonic levels for both power and drain efficiency, and correlates with the simple approach from Figure 5.25.

5.4.5 Experimental Validation of the Source Injection mode

A ten finger, 0.3µm gate length GaAs pHEMT on the CP FD30 process with a periphery of 0.75 mm (10x75µm) is chosen as the test transistor, Figure 5.31.

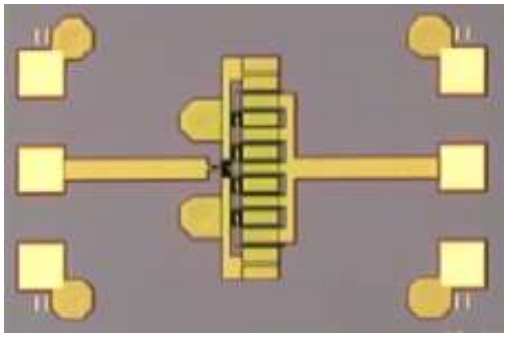


Figure 5.31 Compound Photonics FD30 10x75µm test transistor, (wafer 58003.09.6948.10)

This pHEMT process has a pinch off voltage, V_p, of approximately -1.1 V, a maximum drain current, Imax, typically 480 mA/mm, and a relatively high breakdown voltage suitable for High Power Amplifier applications. The calculated RF load at the fundamental frequency for this transistor is 66 ohms. The 9 GHz optimum load impedances were identified using a load pull sweep around this theoretical point, after de-embedding the data to the device current generator reference plane.

The 18 GHz output 2nd harmonic current was terminated into a short circuit as required for the Class B condition. Both fundamental and 2nd harmonic load impedances were synthesized using the Cardiff active load-pull system [24] shown in Figure 5.32.

The load impedances, Z_{Nf0}, presented to the device, at the intrinsic device reference planes are Zf0 = 68.6+j5.8 Ω for the fundamental and Z2f0 = 3.1+j1.2 Ω for the 2nd harmonic, which is a good short circuit relative to the fundamental impedance. The 27 GHz 3rd and (>36 GHz) higher harmonics were terminated into the system characteristic impedance, with Z3f0 = 4.7 –j19.8 Ω and Z4f0 = 4.5 –j14.7 Ω at the device reference plane. This does not change the validity of the results as this impedance environment is the same for all measurements, but it is noted that these are close to the required short circuit condition.

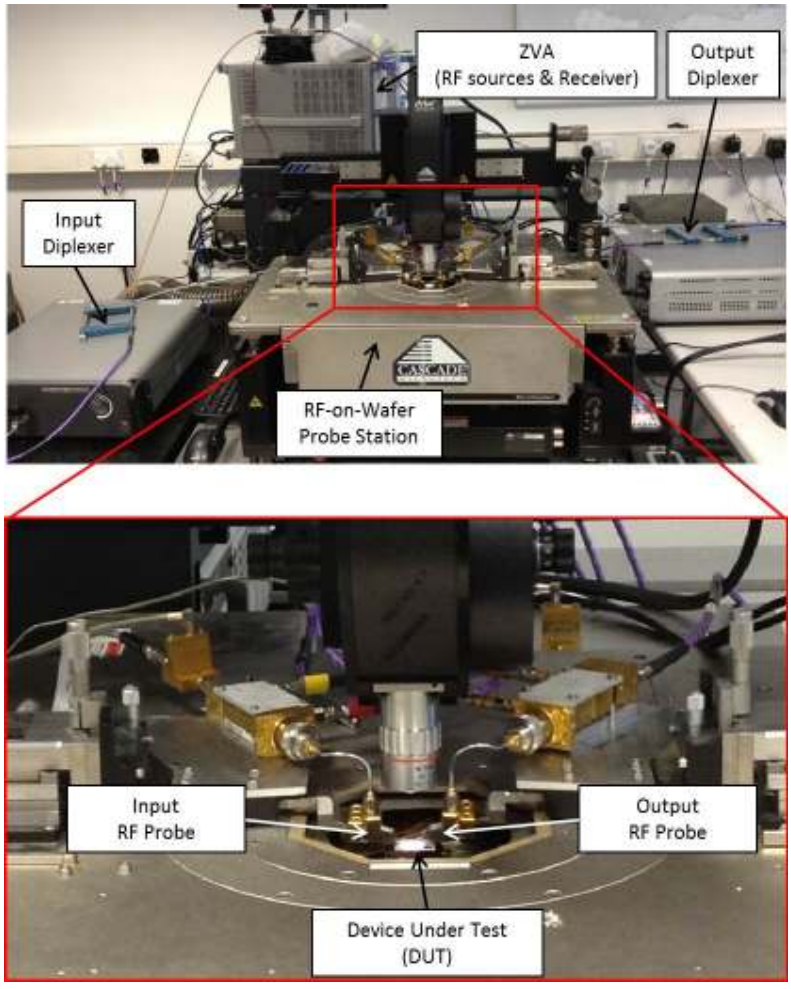


Figure 5.32 Cardiff ALPS configured for RF-on-wafer measurements. Fundamental and second harmonic at source injection and fundamental and second harmonic load control are shown using diplexers.

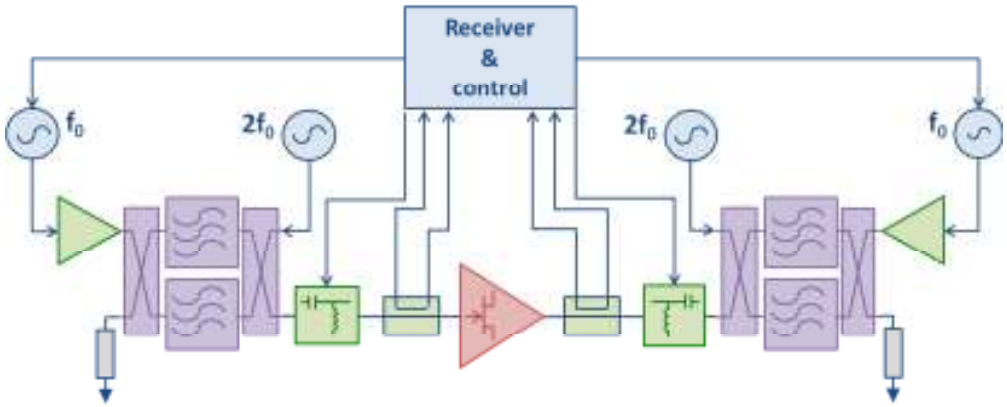


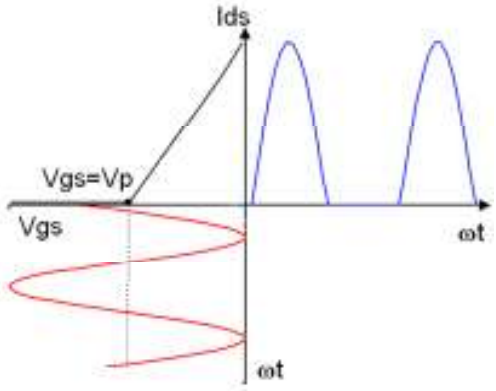
Figure 5.33 Measurement set-up schematic for source injection/Class B investigation.

Measurements were performed RF-on-chip with the device engineered to operate in the two identified states, at Vds=9 V:

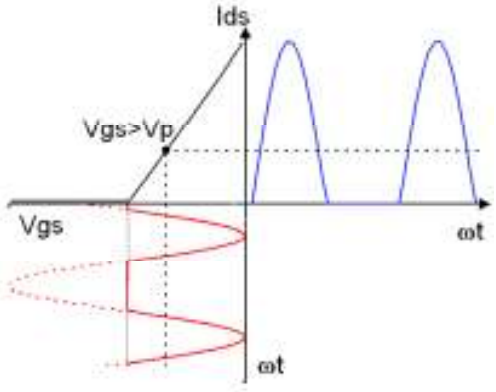
(a) Traditional State: A single tone RF input signal at the classical Class B bias point with gate-source voltage, Vgs= -1.1 V i.e. at pinch-off, and

(b) Improved State: The gate input waveform optimized by adjusting the DC bias condition, Vgs=-0.6 V, and adding a correctly aligned, phase coherent 2nd harmonic signal to the input of the device (see Figure 5.33 for test set-up schematic).

These two states are identified in Figure 5.34 and show the gate dc bias condition must be modified in order to keep the clipped portion of the sinewave at the pinch-off voltage, resulting in a modified quiescent bias point (now more similar to Class AB than Class B) as shown as the bias point in Figure 5.34 (b).



(a)



(b)

Figure 5.34 Idealised PHEMT transfer characteristics showing bias points and waveforms for (a) Class B sinusoidal and (b) clipped sinewave drive conditions.

Input operation was optimized with guidance from the measured RF current and voltage waveforms [24] which are de-embedded to the intrinsic device plane, i.e. the Gate-Source controlling node, and as such establishes a direct link with the fundamental waveform theory.

The resulting optimum input drive for the source injection case is +12.6dBm fundamental signal with a 2nd harmonic amplitude of -6.9 dBc and a -65° phase shift relative to the fundamental.

5.4.6 Measurement Results

Input (gate) measured waveforms for the device are shown in Figure 5.35 for both Class B conditions. The single RF tone Class B drive shows a peak gate voltage of +1 V with the negative cycle that swings down below -4 V.

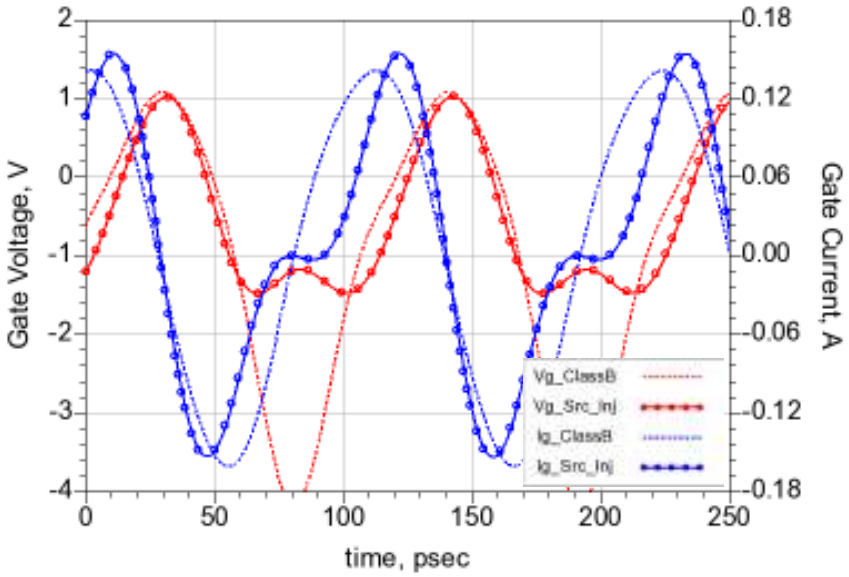


Figure 5.35. Measured 10x75µm GaAs pHEMT Gate voltage and current waveforms under Class B conditions (f0 = 9 GHz, Vds=+9 V).

The voltage waveform is asymmetric about the -1.1 V bias point, due to the gate-source capacitance varactor effect that increases the negative peak voltage excursion and broadens the positive peaks This broadening increases the drain current conduction angle, as evident in Figure 5.36, which has a detrimental effect on efficiency.

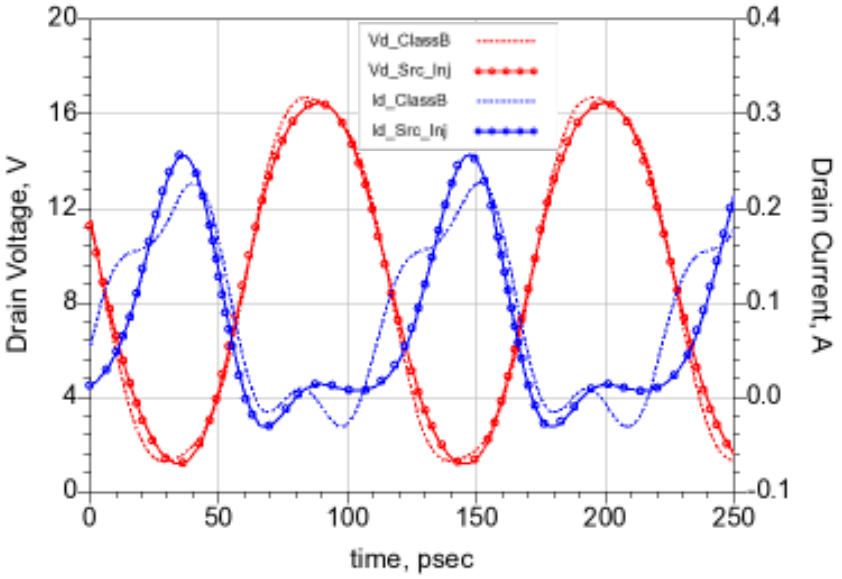


Figure 5.36 Measured 10x75µm GaAs pHEMT Drain voltage and current waveforms under Class B conditions (f0 = 9 GHz, Vds=+9 V).

In contrast, the source-harmonic injection signal case clearly shows a gate voltage waveform with a band limited half wave rectified response. This achieved waveform has the same positive peak voltage of 1V but the negative swing now limits at approximately -1.5 V. This difference in input signal voltage translates to a fundamental signal component of +12.6 dBm for the source injection case, which is 3.4 dB lower than the +16 dBm input required using the traditional Class B case. The gate waveforms between these approaches are very similar above the pinch-off voltage and result in a similar output (drain terminal) current response (Figure 5.36), thus validating the postulation that the input voltage swing below cut-off plays no role in the output waveform shaping. Further investigation of the drain waveforms (Figure 5.34) show the voltages are also almost identical and result in an output power (Table 5.2) which is only 0.4 dB lower at +26.4 dBm for condition (b) compared to +26.8 dBm, for the traditional class B condition (a).

	Pin dBm	Pout dBm	Ids mA	Drain Efficiency, η_D	PAE
(a) Class B	16.0	26.88	82.6	65.6%	60.1%
(b) Src Inj	12.6	26.46	71.4	68.8%	66.0%

Table 5.2 Measured 10X75 PHEMT device 9GHz Performance summary

The differences in the drain current waveforms can be explained by the presence and non-linear behaviour of the device intrinsic capacitive elements (Cgs and Cgd), which are functions of both bias voltages. Hence a beneficial slight reduction is also noted in the conduction angle of the drain current for the 2nd harmonic source injection case. This is a consequence of the narrower positive going gate-source voltage swing achieved when injecting only the 2nd harmonic at the input to create the clipped sinewave signal. The modified input signal is also overcoming some of the detrimental gate-source (Cgs) varactor broadening effects, which are more pronounced in the pHEMT device compared to similar MESFET technologies [43]. As a consequence, it was also noted that the drain efficiency, η_D, of the second harmonic injection case was 3% higher at 68% compared to the sinusoid drive case (η_D = 65%). Furthermore, the lower input drive requirement for the source injection case does translate to increased amplifier power gain and results in significantly improving amplifier PAE to a very high value of 66%, from 60.1% when using the single sinusoidal drive.

The response of the transistor waveforms under the second harmonic source injection case, when varying the phase of the second harmonic input signal (with the amplitude held constant at -7dBc relative to the fundamental) is shown in Figure 5.37.

These waveforms show some additional drain current flow at the extremes of the relative phase excursion, as would be expected from the theory and depicted in Figure 5.23.

The power and efficiency performance of the transistor under these conditions is plotted in Figure 5.38. This response shows there is little impact on output power or drain efficiency if the phase of the second harmonic is maintained to approximately ±10° about the optimum case. Additionally, there is only a small, <3.3%, drain efficiency penalty and <0.17dB power drop with the second harmonic held to within ±20° of the optimum value. This is an important result which shows there is some design margin in the response of the transfer characteristic. This is critical when translating the optimally driven test transistor into a practical amplifier circuit, as this relaxes the requirement of the driver amplifier fundamental and second harmonic response.

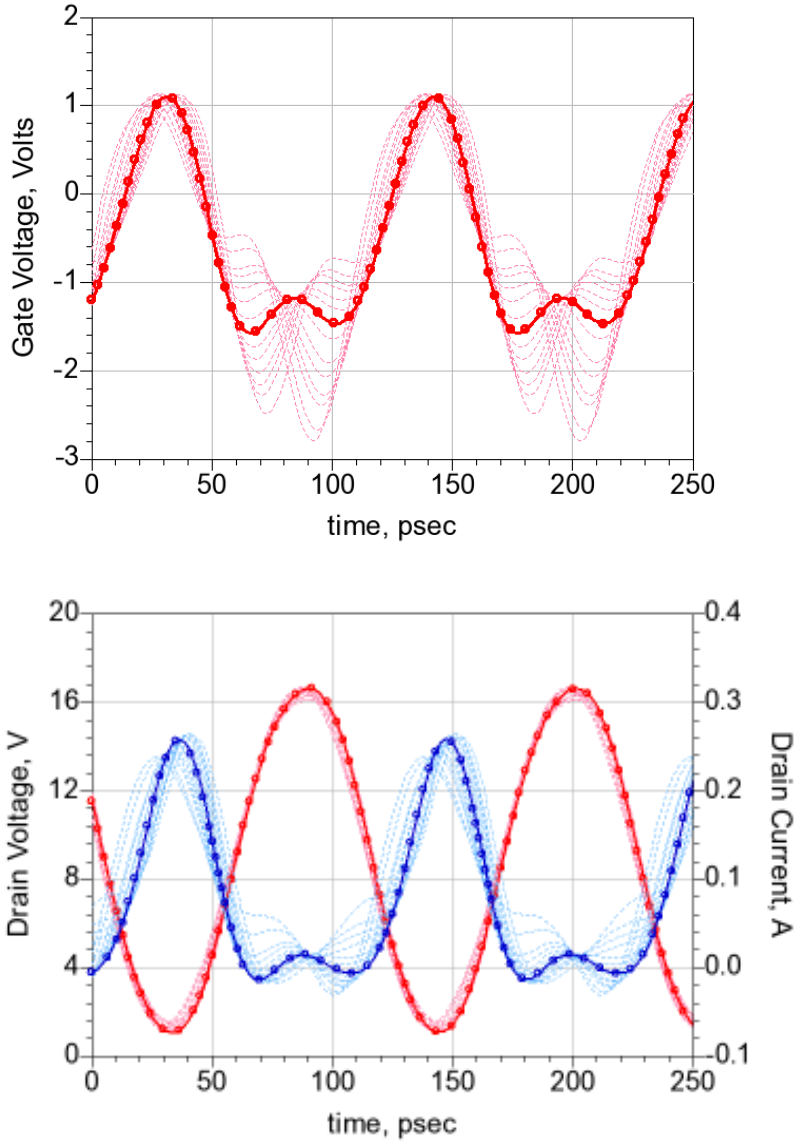


Figure 5.37 Phase sensitivity waveforms for FD30 10x75 device at 9GHz. Phase shift -80° to 80°, bold trace at the optimum condition 0°. Bias conditions Vds=9V, Vgs=-0.6V.

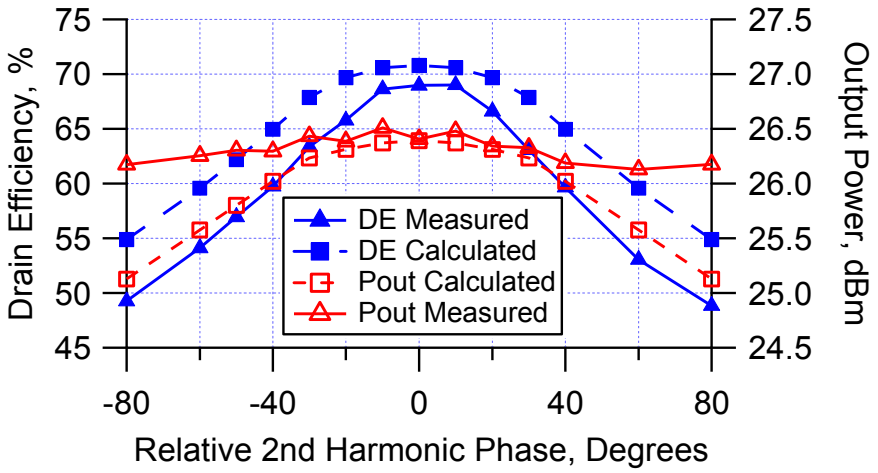


Figure 5.38 Measured 10x75µm GaAs pHEMT output power and Drain Efficiency versus relative phase of 2nd harmonic component (from optimum). Bias conditions Vds=9V, Vgs=-0.6V.

This design approach was expanded and included measurements on a second wafer. The measured performance of the traditional Class B condition shows an input power of 16.5dBm at the 1dB compression point. The reference output power at this point is 27dBm. The measured PAE is only 91% of the drain efficiency figure due to the low power gain of 10.5dB.

The measured response under the swept second harmonic injection condition is shown in Figure 5.39. Under this case the fundamental component is held constant and the second harmonic input power is swept. The input power at 1dB compression is 13.4 dBm under this condition, 3.1dB lower than that required by the traditional Class B case. Even though the output power under this condition is slightly lower, the PAE is higher (94% of the drain efficiency figure) because of the improved power gain.

One of the interesting points to note in the data of Figure 5.39 is the turning point at low 2nd Harmonic drive levels. This is the point at which the self-generated 2nd harmonic created from the fundamental drive, is cancelled by the injected, out of phase second harmonic signal. The measurement system cannot distinguish between these signals so the x-axis references the total second harmonic content.

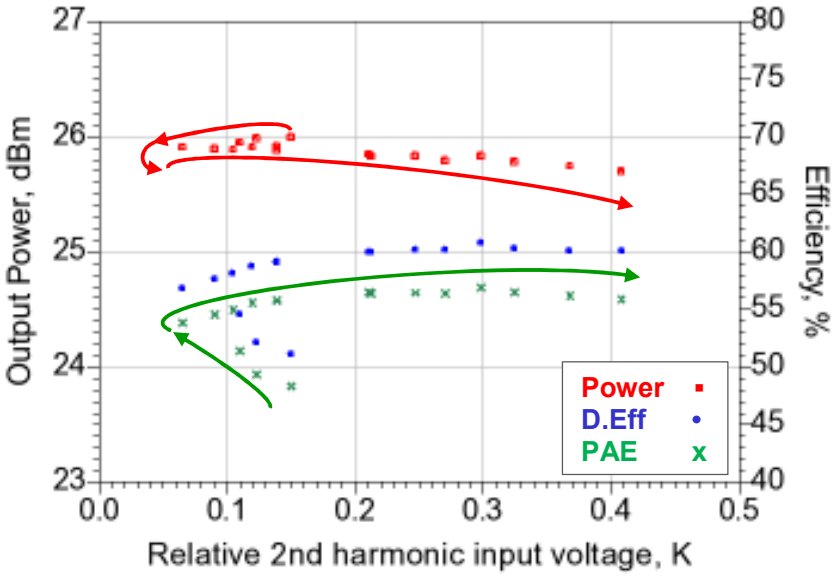


Figure 5.39 Power and efficiency of 10x75µm pHEMT (wafer 58036) (Vds=+9V, Vgs=-0.6V) at 9GHz with varying 2nd Harmonic injection, fundamental held constant. Direction of arrows show increasing injection power.

5.4.7 Measurement Conclusion

Shaping the input waveform using 2nd harmonic injection, to drive a pHEMT into a Class B amplifier mode has been demonstrated at X-band, showing the RF swing past cut-off is not required for successful operation, as postulated. It was shown to deliver similar output performance to the classical Class B operation but with the fundamental input signal requirement that is 3.4 dB lower (i.e. the power gain is 3.4 dB higher than class B). This is a significant improvement over the traditional Class B gain and is found to be in line with the predicted 4.3dB value. The residual difference is linked to the fact that the pinch-off voltage in practical devices is not a defined line but covers a finite band and also has some process variation. Therefore, some input fundamental overdrive, relative to the theoretical minimum, is required to keep Vgs below pinch-off during the clipped portion of the waveform, which will reduce the benefit.

A beneficial reduction of the output current conduction angle was also noted, which relates to the different response of the non-linear transistor capacitance to a different input voltage waveform. Consequently, the reduced input drive resulted in an overall 5.9% improvement in the PAE.

It is important to note that this work has highlighted that this performance improvement is only possible for active injection, previous PA work focusing on passive only approaches are not sufficient. This requirement will necessitate the specific nonlinear design of the driver stage.

These results directly confirm the benefits of harmonically engineering the input signal for Class B amplifier operation. It experimentally establishes a direct link between the proposed input waveforms at the intrinsic device gate-source node and the device performance improvement. By focusing on measuring these input waveforms, it provides important insight in how this approach could be exploited and optimised.

5.5 Design strategy using input waveforms

A design strategy needs to be formulated to explore the available design space with this source injection approach. One solution would be to optimise the variables to keep a constant conduction angle, targeting the ideal theoretical value of π radians, or minimizing the fundamental component.

The resulting output current waveforms are shown in Figure 5.40. Alternatively the input waveforms variables can be engineered to target a constant efficiency or constant power, producing another set of output current waveforms.

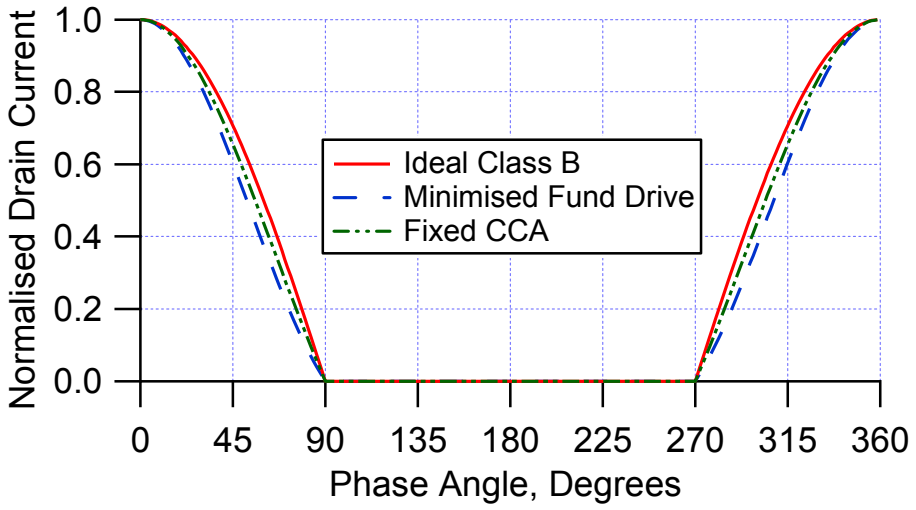


Figure 5.40 Drain current waveforms for the second harmonic injection case using constant conduction angle. Minor changes are noted in the current waveforms

The A-K design space can be further expanded to detail the relative clipping effect Figure 5.41. This clearly shows the class A case (zero clipping and fundamental only) through to the ideal, Fourier clipped sinewave with a relative clipping of unity.

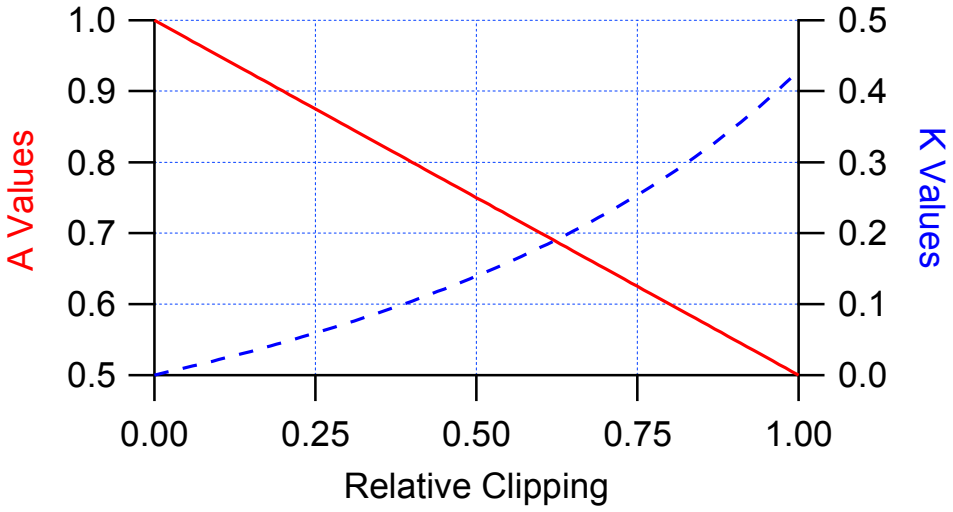


Figure 5.41 The A-K design space versus relative clipping.

The respective associated A-K design space values, with the constant C varied to maintain a constant maximum drive level, are detailed in Figure 5.42 for three design strategies. The trend can be seen that decreasing the 2nd Harmonic content, K, for a given fundamental amplitude, increases power but decreases efficiency and vice versa.

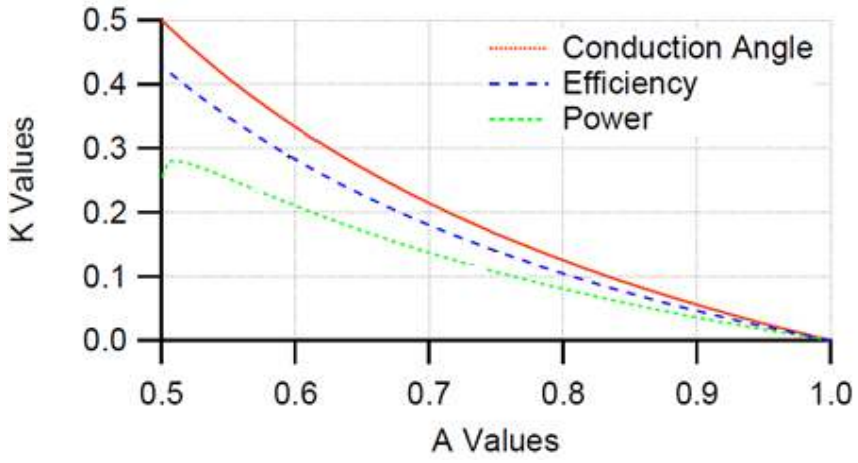


Figure 5.42 Power and efficiency trade-off under three design strategies.

However, in selecting the optimum design trade-off we need to also address the problem of reduced gain at these high frequencies. Targeting solutions, which minimize the fundamental input signal will result in a higher power gain and hence translate to a higher PAE. Using 5.9 and keeping the fundamental at the minimum (A=0.5), the gain

space trade-off can be quantified. Analysis shows the output power remains fairly constant over practical ranges of relative second harmonic level, and thus the power gain is defined by the input power for each test.

Rewriting the input power from 1.16, with a clipped sinewave drive

$$V_{gs,Fund} = \frac{(V_{gs,\max} - V_P)}{2\pi}\left[\frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)}\right] \qquad 5.19$$

$$P_{in,AB} \propto V_{gs}^2 = \frac{1}{2}\left[\frac{(V_{gs,\max} - V_P)(\alpha - \sin\alpha)}{2\pi(1-\cos(\alpha/2))}\right]^2 \qquad 5.20$$

Inserting this into 1.17 and rewriting the relative gain expression leads to

$$\frac{G_{P,AB}}{G_{P,A}} = \frac{\pi(1-\cos(\alpha/2))}{(\alpha - \sin\alpha)} \qquad 5.21$$

This is plotted in Figure 5.43 and demonstrates that the gain remains almost constant throughout the Class AB operating space. In fact, there is an improvement in gain for smaller conduction angles toward the Class C condition. This artefact appears as the required input power increases more slowly than the reduction in output power compared to the classical operating point.

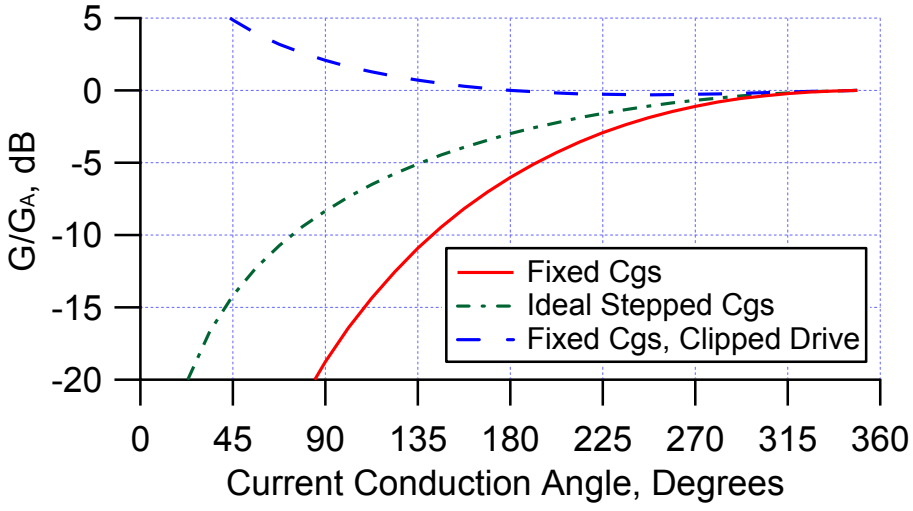


Figure 5.43 Gain relative to Class A versus current conduction angle (CCA) under (a) sinewave drive (red trace), and (b) clipped drive (blue trace)

5.6 Conclusion

This chapter has shown the choice of optimum load line and operating point can drive the design by providing insight into the factors affecting efficiency from a waveform perspective.

The gain response of the reduced conduction angle operation is presented detailing the power gain reduction is significant at class B and beyond, which is a significant drawback.

The role of the non-ideal input impedance was investigated and a method to simplify the circuit performance was presented. The gain response was developed from this approach and demonstrated the simple conduction angle gain response is in error.

The use of alternative input voltage waveforms to recover the gain was shown, with the use of a second harmonic component on the input of a transistor to approximate the ideal clipped sinewave drive.

The theory was validated with measurements on a pHEMT device which showed improvement in efficiency and gain in line with the theory is possible.

6 GAN MMIC AMPLIFIER DESIGN

This chapter details the design of a 2 stage GaN MMIC amplifier fabricated using the Fraunhofer IAF GaN25 MMIC process. The circuit design uses the methods from the previous chapters and will focus on design aspects relating to the intrinsic plane waveforms. It details how the interstage matching networks deliver the correct gate terminal waveforms, to drive the power stage with a clipped sinusoidal waveform which has been shown to improve the PAE of the amplifier stage as discussed in section 5.4.5.

This chapter also shows methods to use these waveform techniques to assess the performance of the circuit implementation.

The target specification for the amplifier is shown in Table 6.1. This is a typical requirement for TR module and includes the additional system level considerations.

Frequency	8.5GHz – 9.5GHz (min) 8GHz – 10GHz (target)
Output Power After TR switch/circulator	> 1.6W (+32 dBm)
Gain Derived from input power drive level to achieve rated output power	> 15dB (power gain)
Efficiency (PAE)	> 50%
Supply voltage	+28V Typically
Chip area	< $2mm^2$

Table 6.1 Cardinal point specification for the Power Amplifier design

The use of second harmonic source injection has been shown to recover device gain under reduced conduction angle operation and lead to an improvement in PAE (section 5.4). These results have been achieved with the use of active load pull test benches to synthesis the correct impedances and engineer the correct input waveforms.

In order for this technique to be useful a design strategy is required to create these waveforms in a practical circuit.

There are different options to create the waveforms

(i) Synthesised input signal from the transmitter source – used with a single transistor amplifier.

(ii) Utilising input circuit non-linearities in the power transistor – can be used with a single transistor circuit.

(iii) Using driver stage non-linearities.

The simplest amplifier design is a single transistor, with a fixed load impedance designed to create the optimum load impedance for a given amplifier class. The input signal can be synthesised (option (i) above), with a second harmonic component included with the correct phase relationship to the fundamental drive signal. This was the basis of the circuit demonstration illustrated in section 5.4.5. The only difference for this approach relative to a traditional amplifier design is the input match is required to support the generation of a 2^{nd} harmonic voltage at the gate terminal. This approach relies on additional system complexity in generating the harmonic signals to synthesise the correct waveform. This is not always possible for radar and EW systems where volume is limited and information of the transmitted signal is not fully known as the signal is a retransmitted pulse replayed from a Digital RF Memory (DRFM) system.

Option (ii) uses the inherent non-linearity of the driver stage input but the waveforms generated add the second harmonic in the opposite phase for positive real impedances. The best performance is found for a short circuit of the second harmonic current, as previously reported in [43] and [47].

Using a second transistor in a driver amplifier stage to create harmonics is defined by option (iii). This at first seems like an increase in complexity but it should be remembered that most amplifiers, especially at high frequencies are actually multi-stage and thus the approach is to harness or adjust the driver amplifier performance to deliver the desired waveform. This is the circuit topology used in this section to demonstrate the concept.

6.1 IAF GaN25 process overview

The amplifier will be implemented on the Fraunhofer IAF GaN25, 0.25µm gate length Gallium Nitride on SiC MMIC process.

The process summary is shown below in Table 6.2, providing the basic electrical operating parameters of the active elements [113]. These are used as the starting point for the amplifier design to estimate the required impedances and the basic performance.

General scalable Parameter	Value	Comment
Id,max	> 800 mA/mm	-
Vbreakdown (VBDS)	> 80 V	-
f_t	33GHz / 50GHz	28V / 20V operation
Operational Bias: (design goal) for X band	≤ 40 V I_{ds} = 50-100 mA/mm	Minimize current for a given gain and V_{DS}
Sat. Power at 10 GHz and 40 V	> 5.2 W/mm	up to 1 mm total gate width (TGW)
max. PAE at 10 GHz and 35 V	> 45 %	up to 1 mm TGW, in Class AB bias and f_0 load tuning to max. PAE
MSG at peak G_m at 10 GHz	> 14 dB	up to 1 mm TGW (MSG range)
Peak Junction Temperature of 100 µm thick SiC	≤ 250 °C	25 K/W mm impedance (K per P_{diss})/ mm gate width

Table 6.2 Fraunhofer IAF GaN25 active device parameters [113]

6.2 Initial PA design analysis

The design requirement shows a 1.6W (+32 dBm) output power after the TR switching network and interface. These switch networks typically have less than 1dB loss so the power stage needs to be capable of delivering +33dBm minimum. This requires the appropriate sized transistor to provide the output power.

Deriving the basic power per unit gate width (UGW) at +28V operation using (1.11) and the data in Table 6.2, shows a typical power density per unit of gate periphery of ~5W/mm, leading to a 0.6mm UGW transistor in the output stage to meet the specification.

6.2.1 Transistor selection

Using readily available FET sizes[8] for the process, with an even number of fingers and standard 50/75/100 µm UGW dimensions, the best choice to achieve a 0.6mm periphery is an 8x75µm FET. The choice of this over a 6x100 µm device was to maintain high gain.

The gain response for UGW can be derived from a simplified model of the gate as a distributed RLC equivalent transmission line. As the gate width increases the phase of the signal varies and results in a reduced gain response. An additional effect is noted from the finite conductivity of the gate metallisation causing attenuation of the signal along the gate width. Using the equivalent circuit of Figure 6.1(a) the expression for the power gain reduction can be derived as a function of the UGW [107] resulting in (6.1) and (6.2) for the case of Rg=0.

$$G_{UGW} = \frac{1}{2W_U}\left[W_U + \frac{\sin(2\beta W_U)}{2\beta}\right] \qquad 6.1$$

$$\beta = \omega C_{gs}\sqrt{\frac{L_g}{2C_{gs}} + \frac{1}{2}\sqrt{\left(\frac{L_g}{C_{gs}}\right)^2 + \left(\frac{R_g}{\omega C_{gs}}\right)^2}} \qquad 6.2$$

Equation (6.1) is plotted in Figure 6.1(b) versus frequency for varying UGW

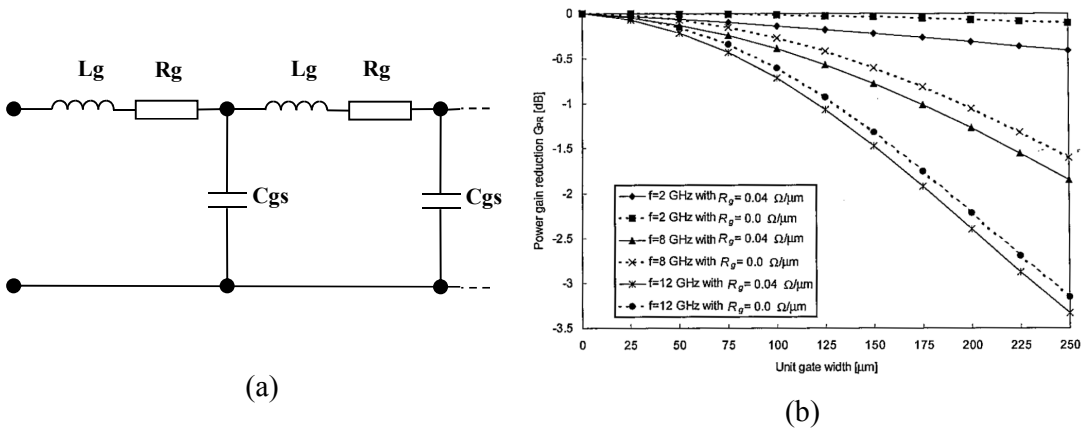


Figure 6.1 Unit gate width effects on gain (a) equivalent gate circuit and (b) application of (6.1) for Cgs= 1.6pF/mm, Lg=6pH/mm, assuming Rg=0.

[8] For a MMIC process the FET UGW dimensions can actually be chosen arbitrarily as long as they are within the foundry layout design rules. However, this puts the emphasis on the designer to create custom models and artworks before design can commence.

The number of fingers can also affect the gain by the same phasing problems across the device width. These are the effects that take the device away from its lumped element approximation and move it into the distributed world. The usual approximation of acceptable dimensions is one sixteenth of the wavelength at the highest frequency of concern.

The standard gate-to-gate pitch of the GaN25 process is 35um so the total distance from the outer to the inner fingers will be 105um or 140um for 6 and 8 fingers respectively. The Wavelength at 18GHz on SiC is ~6.8mm and therefore λ/16~420um. Both these transistor dimension meet this criteria.

6.2.2 Cripps load analysis

As detailed in chapter 2.2.1, the ideal load for a transistor in Class A or Class B operation is defined by equation (2.15) as the ratio of the output fundamental voltage swing and the maximum device current swing, I_{max}.

$$R_{L,A} = \frac{2(1-\beta)V_{ds,DC}}{I_{\max}} \qquad 6.3$$

The resulting impedance may need to be modified slightly during the implementation and optimisation cycle as the drain current shape will vary as discussed in 5.4.2 for a synthesised bandlimited clipped sinewave drive signal.

The Imax is approximately 800mA/mm (Table 6.2) for the Fraunhofer GaN25 process active devices, an 8x75 μm device equates to (800 mA/mm).(0.6 mm) = 480 mA Imax.

Using a simple assumption of the knee voltage at 10% of the dc supply voltage leads to (1-β)=0.9, coupled with the chosen bias point results is a corresponding load line impedance of 105 Ohms.

This simple analysis relates well to the DCIV simulations using the Fraunhofer GaN25 process design kit (PDK) [113] in the Keysight Technologies ADS® CAD tool as shown in Figure 6.2.

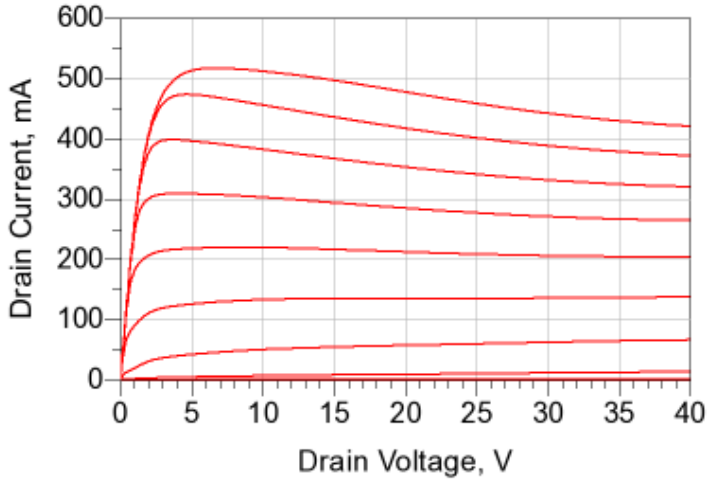


Figure 6.2 Simulated DCIV curves for the IAF GaN25 8x75 device

Using the analysis from 5.1.1, the optimum impedance should be derived from the waveform shapes and the IV curves. Here we assume the RF IV curve boundary is the same as the DCIV and using the process specification from Table 6.2 the performance is shown in Figure 6.3.

Analysing this response, it is seen that the optimum position for power is given at a knee voltage of 4V, but moving to the 3V knee point, a significant efficiency improvement of 3% can be achieved with only a 0.1dB power penalty.

At a drain bias of Vds=+28V and assuming the 3V knee the voltage boundary the RF voltage swing is 25V peak. Taking the actual value of drain current for V_k=3V from the DCIV model results in a value of 453mA. The load line is therefore at an impedance of 110.4 Ohms – very close to the initial estimate.

At this operating point the output power is approximately 3W (+34.8dBm) for a full Class B design, and in line with the initial specification.

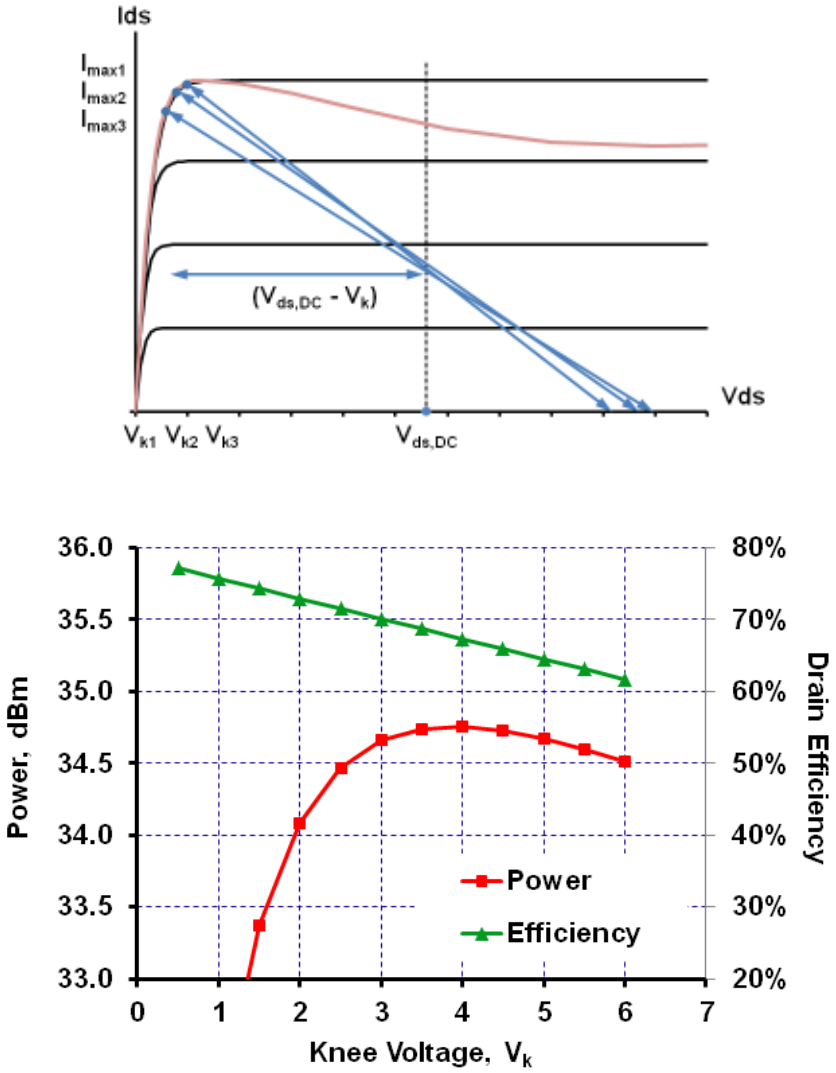


Figure 6.3 Power and efficiency trade-off space (section 5.1.1) for the GaN25 8x75 output matching network design. Showing the idealised and modelled DCIV curves for the 8x75 device.

As a comparison, a load pull simulation was performed on this circuit, along with the Cripps equivalent circuit derived from the load line analysis in Figure 6.3 and using the parasitic elements of C_{ds}=0.24pF and L_d=41pH.

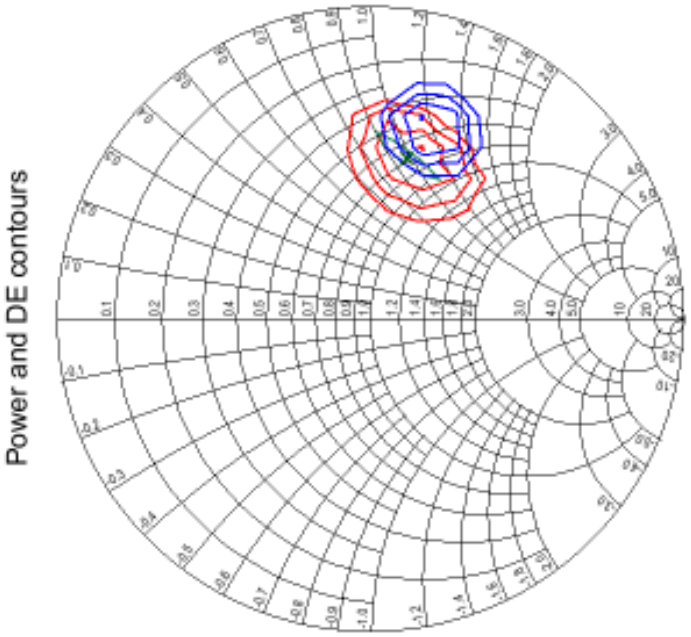


Figure 6.4 Approximated and Simulated load pull contours for the IAF GaN25 8x75µm device at 9GHz. Power contours (red), DE contours (blue), Cripps load [14] (green)

The results for this analysis here are plotted in Figure 6.4, showing the correlation between the classical load pull simulations using ADS and the simplified analysis with the Cripps load. Here the simulated peak power is +33.8dBm and the peak PAE is 51.9% at a drive level of +24.5dBm. The corresponding drain efficiency is 63.6%.

These values correlate favourably with the simple analysis technique. The power gain is around 9.3dB- so the PAE is reduced by a factor (1-1/8.5) = 0.88, with the differences traced to the non-ideal gate voltage waveform creating a larger current pulse.

The analysis has shown that the device is capable of providing the desired specification parameters and will be the basis for the ongoing design, moreover the waveform approach provides more insight into the mechanisms than the load pull simulations alone.

6.3 MMIC Design

Using the basic analysis from section 6.2, the power stage of the amplifier is based on the GaN25 8x75µm device. The design of a 2 stage amplifier using harmonic source injection for the power stage is shown in the following section. This follows the approach outlined in section 5.4.4, but some basic amplifier considerations need to be addressed at the same time.

6.3.1 Amplifier Stability considerations

Stability of an amplifier is an important but often overlooked aspect of the design process. There are two main classes of instability encountered during practical amplifier design.

(i) DC bias (Low frequency) stability – this concerns the impact of the bias and dc feed networks which are required to apply dc power to the active device. This stability measure can be further split into two generic problems.

  (a) The stability of the device operating point caused by poorly defined dc conditions and the operation of the active device. This is especially important if the amplifier is to operate over any expanded temperature range. This is covered in [115][116] and will be assume here that the bias is controlled by an active circuit to keep the current density constant over the operating temperature envelope [116].

  (b) Bias network design causing low frequency oscillations due to loops. This occurs when the feed network inductances reduce to zero at low frequencies and the decoupling capacitors have increasing impedance. When coupled with devices having large dc gain (as in the case of the FETs) out of band can often cause oscillations at low RF frequencies.

(ii) RF stability – this concerns the impact of the terminating impedances of the device and the feedback effects noted in the device or circuit. Again, this stability measure can be further split into two generic problems.

  (a) The transistor can become unstable when placing certain terminating impedances at the device terminals. This arises from the fact that the transistors are, in general, non-unilateral devices as they have internal

feedback, for example the gate-drain capacitance in the case of FET technology. Under certain conditions, a passive terminating impedance at port 2 can cause a reflection coefficient greater than 1 at port 1 and vice-versa. Rollett defined a stability measure, K, of a two port network in terms of the port parameters [111] The theorem states that the transistor (or two port) will be unconditionally stable if the Real part of the port impedance at one port is positive for any passive impedance at the other port. This condition is satisfied if K≥1. The K-factor is actually limited to small signal linear two port networks. Care must be taken to ensure stability is met for the amplifier circuits as they near the non-linear region, as bias conditions differences and drive levels can cause instabilities.

(b) Odd mode oscillations – using a parallel stacked transistor line up for higher output powers any asymmetry in the circuit can cause odd mode oscillations between transistors connected together. This has been analysed by Ohtomo [117]. For the design here a single output transistor is used and this is not valid.

Basic analysis of the transistor building block is critical to get trouble free performance for the amplifier stages. This is performed on each stage individually, with further analysis of the full amplifier following.

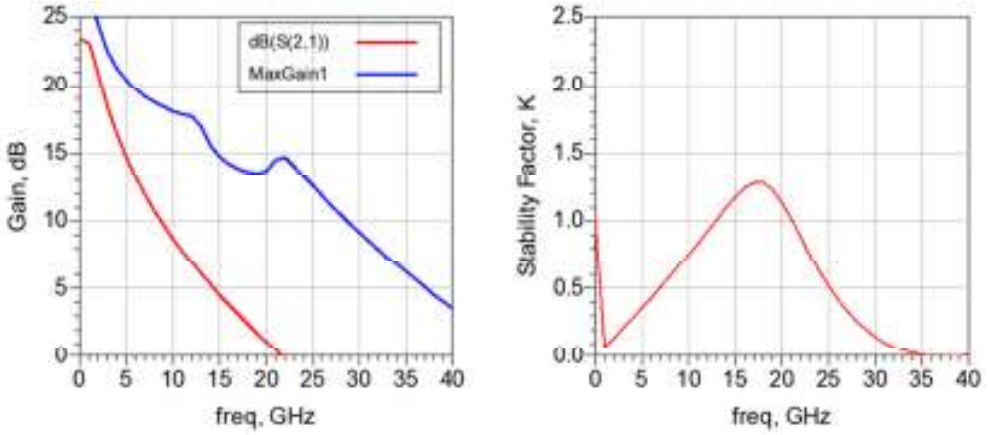


Figure 6.5 The gain and stability of the GaN25 8x75µm device at 28v/-1.6V

For the two stage design identified here, analysis of the s-parameters can identify the stability of the amplifer by inspection of the K factor.

Analysing the GaN25 8x75 device s-parameters at a Class AB bias point (Vds= +28V, Vgs=-1.6V) the response is shown in Figure 6.5, indicating the stability of the 8x75 device is poor, especially at low frequencies.

Transistors, or any active two-port, which are potentially unstable (exhibiting K<1) can be made unconditionally stable by adding a simple series resistor at the input (or output) port as shown in Figure 6.6.

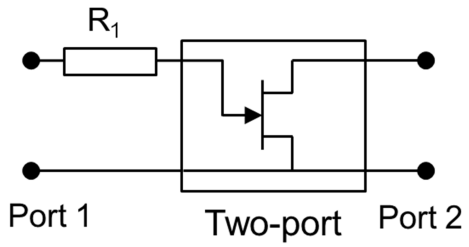


Figure 6.6 Stabilised transistor device using input resistive loading

Analysis of this network in terms of the s-parameters of two cascaded blocks (one for the resistor and one for the transistor) is cumbersome. However, although the stability factor K is usually defined in the literature in terms of s-parameters [15][16], it should be noted that the original paper [111] defines K in terms of any 2 port representation. Inspection of the network in Figure 6.6 shows this to be a series connection and thus better dealt with in terms of the Z-parameters. Using the expression (from Appendix B) the series resistor R_1 can be simply found from the 2-port network Z-parameters of the transistor at each frequency

$$R_1 = \frac{K\left|Z_{12}Z_{21}\right| + \mathrm{Re}(Z_{12}Z_{21})}{2\,\mathrm{Re}(Z_{22})} - \mathrm{Re}(Z_{11}) \qquad 6.4$$

The GaN25 8x75 transistor input series stability resistor results are shown in Table 6.3. This shows that there is a frequency dependent requirement for the resistor.

freq	StabFact1	Rstab
1.000 GHz	0.073	54.248
2.000 GHz	0.144	24.930
3.000 GHz	0.215	15.095
4.000 GHz	0.287	10.147
5.000 GHz	0.360	7.163
6.000 GHz	0.435	5.166
7.000 GHz	0.511	3.739
8.000 GHz	0.588	2.673
9.000 GHz	0.668	1.852
10.00 GHz	0.750	1.207
11.00 GHz	0.834	0.695
12.00 GHz	0.921	0.289
13.00 GHz	1.009	0.000
14.00 GHz	1.095	0.000
15.00 GHz	1.175	0.000
16.00 GHz	1.240	0.000
17.00 GHz	1.278	0.000
18.00 GHz	1.278	0.000
19.00 GHz	1.231	0.000
20.00 GHz	1.141	0.000

Table 6.3 Stability measure for the GaN25 8x75 device at 28v/-1.6V and the resulting series stabilising resistor, R_{stab}, to achieve K=1.

This frequency response can be achieved by using a parallel RC network in series with the gate as shown in Figure 6.7.

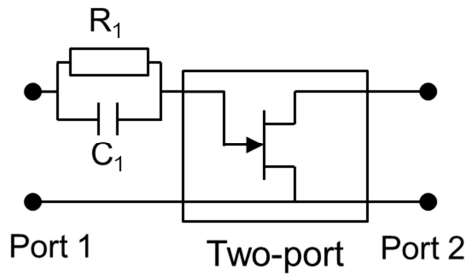


Figure 6.7 RC stabilised transistor cell

The RC network has the property of allowing low frequencies current to flow through the resistor and at higher frequencies more current flows through the capacitor and thus providing a frequency dependant resistive element ideal for the gate of a FET.

The impedance of a parallel RC network is:

$$Z_{in} = \frac{R(1+j\omega CR)}{(1+\omega^2 C^2 R^2)} \Rightarrow \mathrm{Re}(Z_{in}) = \frac{R}{(1+\omega^2 C^2 R^2)} \qquad 6.5$$

Equation (6.5) shows the real part (the resistance) having a frequency dependence. This can be mapped to the R_1 resistor requirement of Table 6.3. This has been used in MMIC designs in a highly integrated form within the transistor structure [112] but for the IAF GaN25 process discrete elements must be used, creating a circuit block attached to the Gate of the transistor.

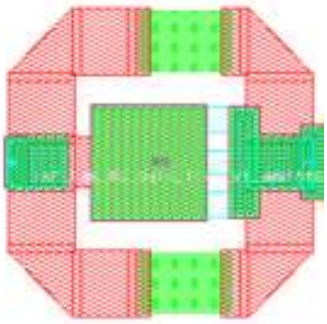


Figure 6.8 RC Stabilisation network MMIC implementation

The response of an ideal network (R_1=100Ω, C_1=1.5pF) is shown against the ideal requirement in Figure 6.9, along with the response of the physical model of the network using MMIC components.

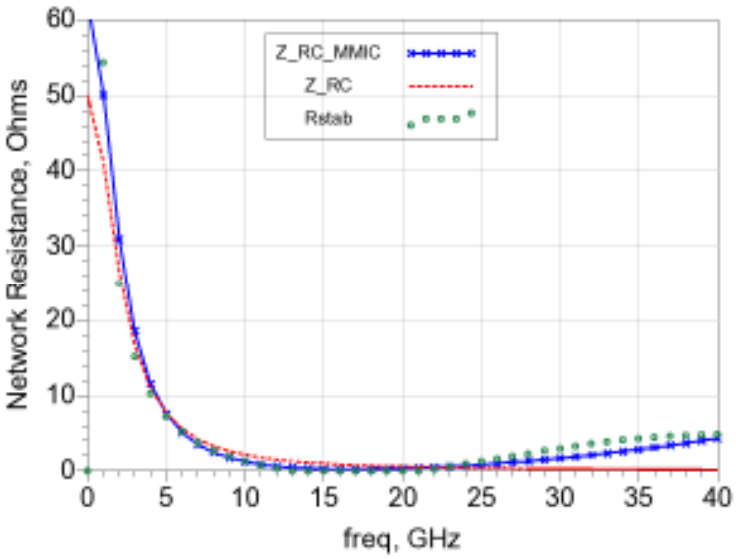


Figure 6.9 The RC stabilising network performance for the 8x75 GaN25 device showing requirements, ideal network and MMIC implementation response.

The stability of the final transistor and integrated RC network is presented in Figure 6.10, showing that it is unconditionally stable to 22GHz, requiring less than 2 Ohms beyond this point to make the circuit stable to 40GHz, but as the impedances at these frequencies are to be controlled, the unstable regions can easily be avoided.

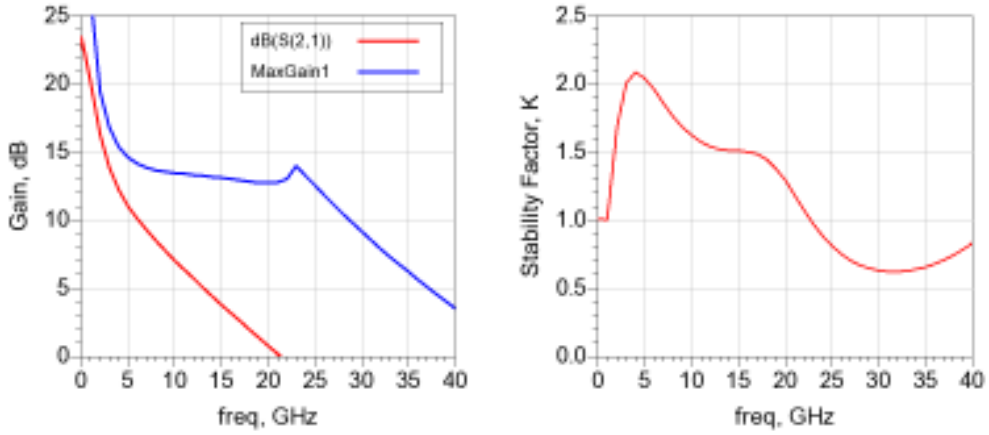


Figure 6.10 The gain and stability of the GaN25 8x75µm device at 28v/-1.6V with series gate RC stabilisation network.

The circuit also needs checking after this network is added to ensure stability with the output load impedance network.

6.3.2 Output Matching Network

The output match is a Class BJ network, designed to provide the optimum match at the fundamental (R_{opt}) at the current generator plane and a short circuit at the second harmonic mid-band. The matching network can be realised by the use of 'L' or 'T' ladder networks [58] and tables or closed form expressions [16]. A simple network is preferred – the effect of adding more elements to the matching network has a diminishing effect and in some cases the increased loss of the networks can eliminate any perceived performance improvement (section 2.2.3).

Using the voltage simulation method and sweeping over a reduced range the impedances are found for the fundamental and second harmonic (). These impedances show close correlation at the fundamental, with some straightening out of the impedance trajectory, and a more pronounced deviation at the second harmonic, due to the current pulse differences with load voltage waveform, even showing the need for an

active load (negative resistance) impedance. However, they are similar to the ideal condition.

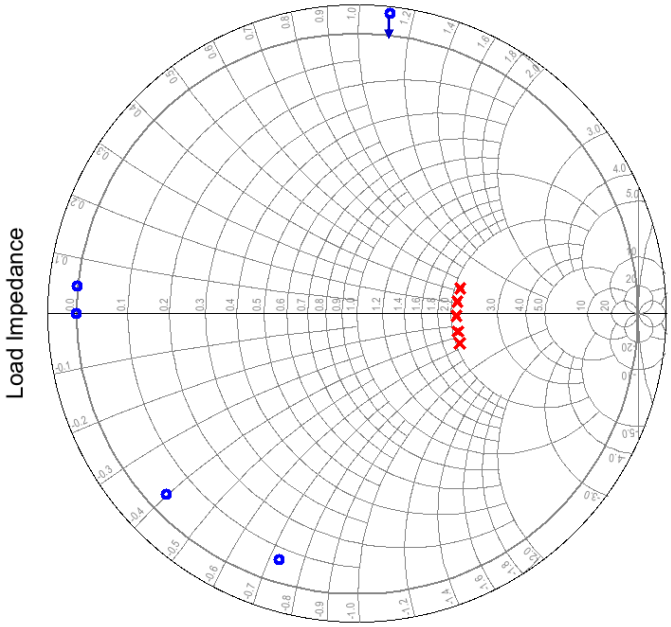
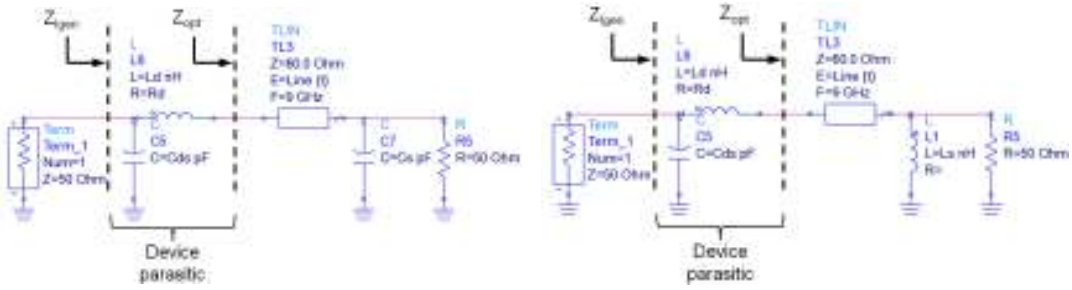


Figure 6.11 Class BJ fundamental and second harmonic impedances at the current generator plane for the IAF GaN25 8x75µm device over the range -0.2<α<+0.2 [18]. Negative resistance impedance shown to be shifted to the passive Smith chart region.

A simple 'Pi' network is chosen to realise the output match, derived from an L section network, with the 3rd element comprised of the transistor parasitic output capacitor, Cds. This approach is called 'parasitic absorption' [15]. Here the drain inductance has been ignored in this initial analysis, as it is very small. This inductive element can be included when implementing the actual circuit, by absorbing or compensating any series transmission lines or inductive elements in the network.

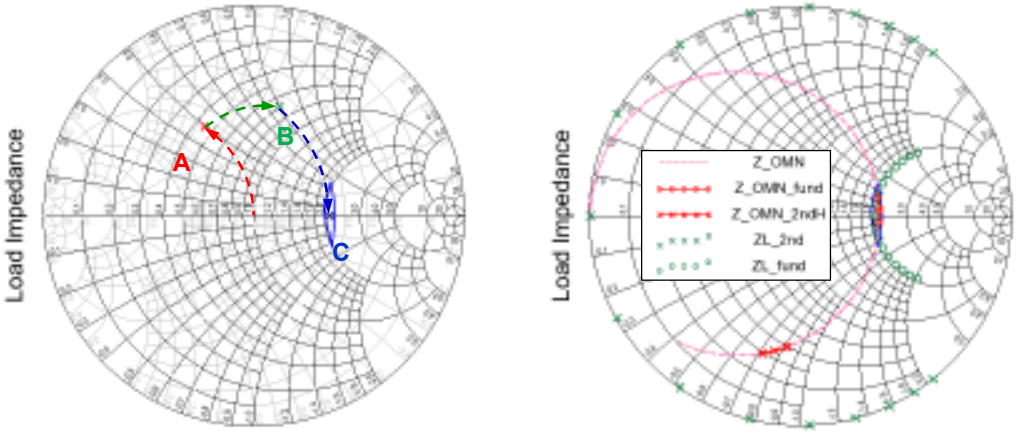
Two basic network options are available as shown in Figure 6.12. A Practical consideration is the discriminator between these two matching networks. The shunt inductor, Ls, in version Figure 6.12(b) is a very useful element as this will allow a dc bias point for the drain supply voltage.



(a) (b)

Figure 6.12 Output matching network topologies for the GaN25 8x75µm Class BJ Load impedance.

The response of the network is developed as shown in Figure 6.13 (a) with the impedance trajectory of the elements at a fixed frequency. The shunt inductor moves to point 'A' from the 50 Ω load impedance. A series transmission line rotates around a fixed circle from 'A' to 'B', which is the optimum impedance, Z_{opt}, for the device. The current generator plane optimum, R_{opt}, is then achieved due the parasitic drain capacitance, Cds, moving the impedance from 'B' to 'C'. The response of the circuit simulated across the full frequency range dc to 40GHz is shown in Figure 6.13(b). Here the fundamental is matched ideally but the harmonic terminations are far from the optimum short circuit.



(a) (b)

Figure 6.13 Output matching network (a) basic derivation and (b) response for the Shunt L–Series Transmission Line–Shunt C network in Figure 6.12 (b).

Refining the circuit requires additional elements in the network (Figure 6.14). Adding in a series resonator in parallel with the Cds element can rotate the harmonic impedances closer to the short circuit optimum, whilst maintaining the fundamental match. Choosing the resonator to be resonant at $2f_0$ provides the short circuit condition. This circuit then has a degree of freedom with the slope parameter for this resonator. This is optimised to allow the second harmonic excursion to extend across the Class BJ space. The circuit was further optimised to use a series inductor in place of the transmission line – this is a subtle modification as the series transmission line is inductive in nature – but the resulting circuit matches the desired impedance trajectory more closely.

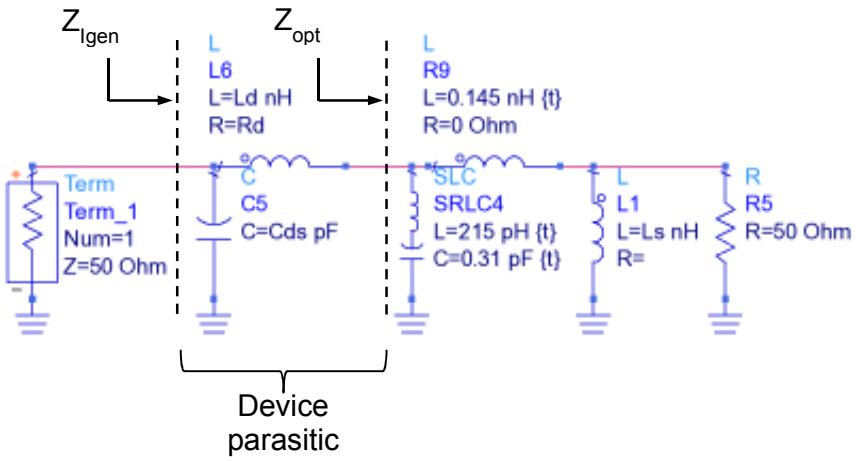


Figure 6.14 Schematic circuit for the ideal output matching network of the GaN25 8x75µm device. Includes a shunt resonator for improved second harmonic response.

The response for the circuit is shown in Figure 6.15. This shows the mapping of the fundamental range as before (Figure 6.13(b)) but now shows the 2nd harmonic impedance closer to the optimum range for the Class BJ design space.

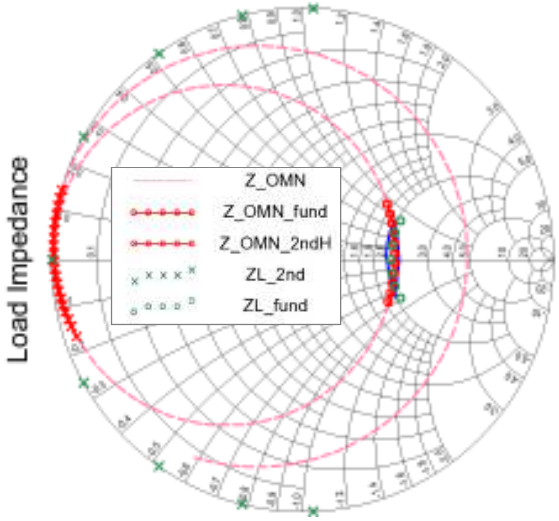


Figure 6.15 Response for the ideal Class BJ matching network from Figure 6.14.

Implementing this circuit in MMIC technology is achieved using lumped element capacitors and distributed transmission line elements for the series inductance. These transmission lines are used in place of spiral inductors on the output network due to their improved current handling capacity.

The resulting matching network schematic is shown in Figure 6.16 (a) with the MMIC implementation layout pictured in Figure 6.16 (b). This incorporates folded transmission lines designed to minimise the overall chip area[9].

The simulated response of the modelled circuit is shown in Figure 6.17

[9] The cost of a MMIC is a simple area ratio for a given functional performance level.

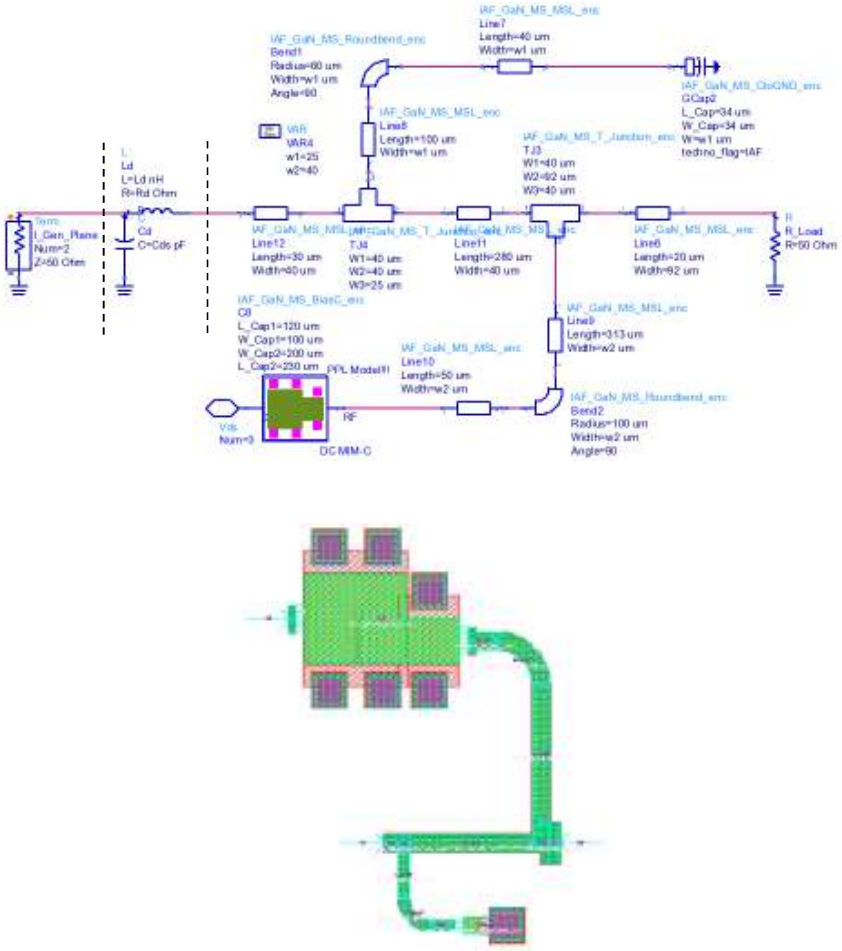


Figure 6.16 Class BJ Output matching network of the GaN 8x75 device (a) schematic and (b) physical layout. MM1586A_8x75_OPMatch_2

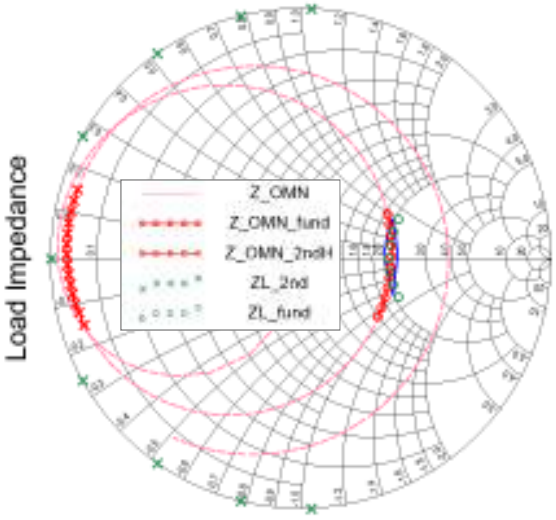


Figure 6.17 Simulated response for the matching network (Figure 6.16). Class BJ impedances also shown (symbols). Fundamental frequency range from 8.5 – 9.5GHz.

6.3.3 Two stage amplifier design

The source injection amplifier design requires the power stage to be driven with a waveform having a properly phased, large second harmonic content.

To define the optimum drive for the power stage, waveform data is required for the design of the matching network. The correct drive voltage is derived from the transfer characteristic, Figure 6.18. Here the pinch-off voltage is seen to be between approximately -2.5 V and -3.0 V.

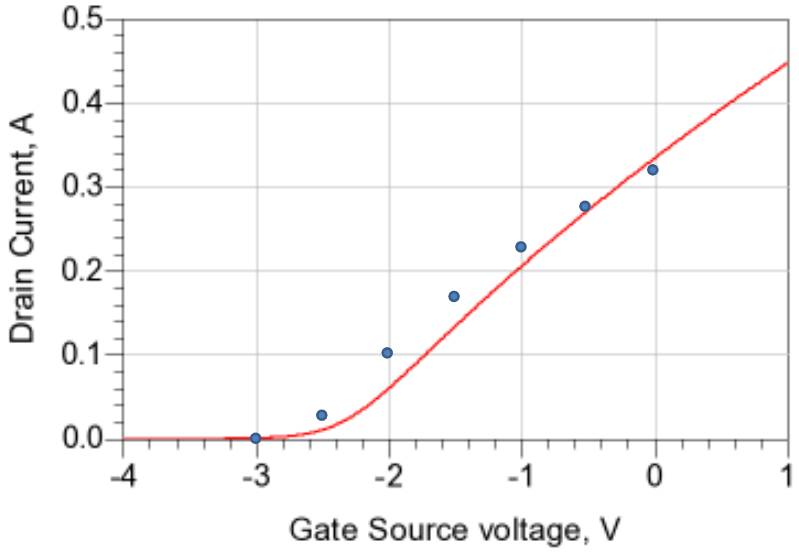


Figure 6.18 Transfer characteristic for the 8x75 GaN25 device at 28V Vds. Here the pinch-off voltage is approximately -3.0V (for 1mA/mm) but the device is essentially 'OFF' for voltages below -2.5V

The analysis in section 5.4.2 has shown the waveforms will need to be driven to make the second harmonic clip at the pinch-off voltage (Figure 6.19). These results are obtained by defining the pinch-off voltage at -2.5V and scaling the voltage accordingly for a Vgs,max of +1V. The dc voltage from the Fourier analysis is found to be -1.6V, a bias condition in Class AB but close to Class A. This will vary slightly depending on the second harmonic content and the device pinch-off voltage.

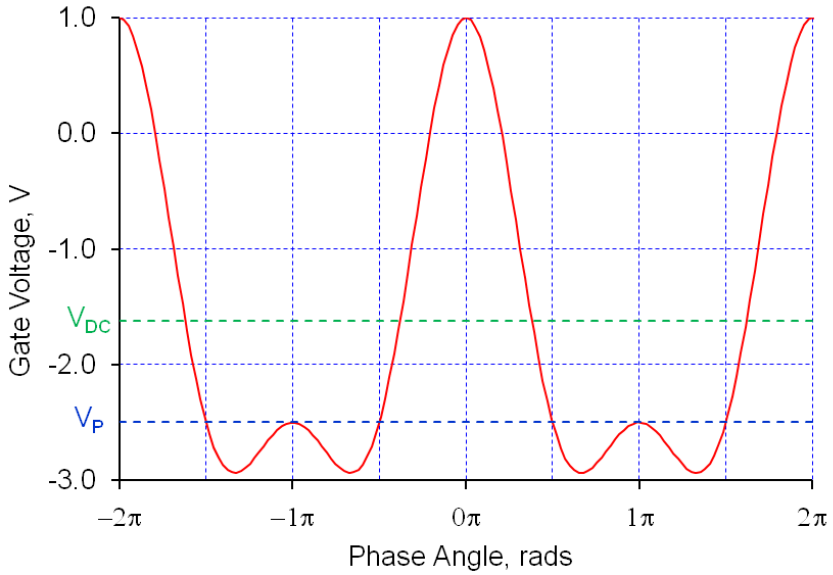


Figure 6.19 Waveform design using Vp=-2.5V, Vgs_{max}=+1.0V, resulting Vdc=-1.6V assuming optimum 2nd harmonic voltage drive level =0.5

This is the optimum condition and the drive level will need to be adjusted to ensure the pinch-off state is achieved. This is an important point when translating the postulated ideal analysis to practical devices and amplifier implementation. It is clear from the transfer characteristic in Figure 6.19 that the pinch-off is not a discrete point and can be defined anywhere around -3V. Thus driving the gate with a normalised amplitude of say 0.55 (as defined in Figure 5.16) which ensures the whole lower portion of the waveform is below pinch-off.

A design flow can to be constructed to detail the phases for the driver stage design in order to create the desired waveform (Figure 6.20). The initial starting point is the choice of conduction angle, chosen to have a second harmonic content. The flow then allows the design of the interstage matching network at the fundamental, with assessment and optimisation of the second harmonic performance. A decision point is included to modify the conduction angle and repeat the flow if the waveforms are not acceptable.

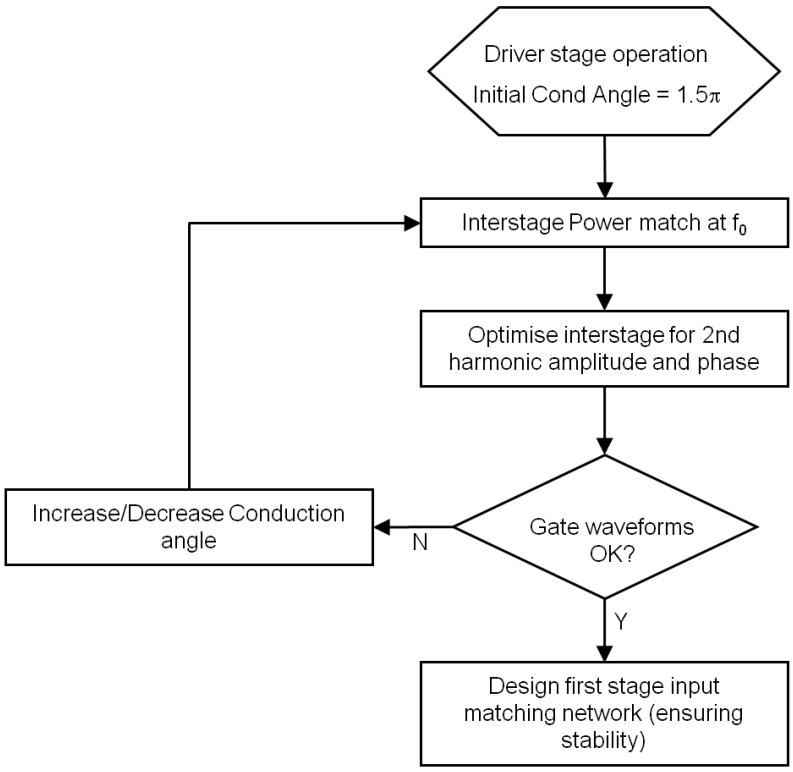


Figure 6.20 Driver amplifier design flow in a 2 stage amplifier.

6.3.4 Driver stage design

The driver stage amplifier transistor size needs to be ascertained. There are some published works that suggest a 1:4 device ratio at X-band is a useful guide. A more optimum solution can be derived using a simple power analysis. The power stage requires a drive of +24dBm to deliver the rated output. Adding 1dB each to take account of the matching network loss and the matching efficiency[10] of the interstage network requires a device capable of providing +26dBm output power. Remembering that the output power of the process, at 28V drain supply, is 5W/mm (section 6.2) translates to a device periphery 11dB (12.5 times) smaller than 1mm. However, the smallest supported device in the foundry library is a 4x50 (200μm) transistor. It must also be remembered that the smaller devices have a higher optimum output impedance (a result of the smaller drain current) so a larger device is preferred as matching networks with large transformation ratios are difficult to realise.

[10] Matching efficiency is the factor which accounts for the accuracy the actual network can approximate the optimum impedance. This effectively adds design margin into the circuit.

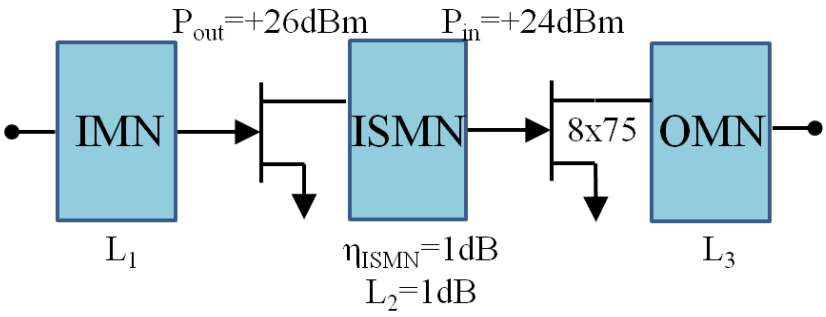


Figure 6.21 Power analysis derivation of the driver amplifier device size.

The full scaling can however be achieved by reducing the voltage of operation accordingly. A drain bias of 9V coupled with a 4x75µm device provides the necessary driver stage requirements.

A further consideration of the driver stage requirements is the need to create a second harmonic voltage component for the power stage. This drive voltage can be achieved by using a device biased in Class B, which provides a second harmonic current and can be manipulated by the impedances to define the voltage. This is not ideal as the gain is reduced, as previously highlighted for the power stage. The bias can be modified slightly to a Class AB condition which keeps a high second harmonic current content and also maintains the device gain [17]. The usual condition for Class B amplification is to provide a second harmonic short circuit impedance at the current generator plane. However, for the application here there is a requirement for a second harmonic voltage.

Investigating the bias conditions shows a 10% Idss bias condition requires a gate bias voltage of -2.2V.

The matching network options can be summarised as:

- The design of the matching network could be achieved by resonating the Cds of the driver stage with an inductor at the second harmonic creating a high impedance. Using a second resonator circuit (series resonant) at the 3rd harmonic would create a short circuit (as required by the ClassB condition). It may be possible also to use the driver stage in Class BJ configuration which would shift the phase of the 2nd harmonic content and could

consequently be offset against the inherent phase shift in the matching network, allowing the correct phase relationship across a larger bandwidth. This is a complicated procedure.

- Recreating the drive level as per Ramadan [53] using a Class F^{-1} driver configuration. In this configuration the circuit was designed using a distributed matching network and this is unsuitable for MMIC implemented.
- Resistive Class B operation [17] which will create the required waveform (180 degrees out of phase) at the driver drain terminal. This has the simplest network terminating impedances with no requirement for open or short circuits at any harmonic frequencies. In this configuration the matching network will be required to provide a 180° phase shift between fundamental and second harmonic.

Using the resistive Class B condition the waveforms can clearly be seen in Figure 6.22. The voltage waveform is a clipped sinewave and a matching network can be designed to modify the waveform already created. This option requires the matching network to do two operations, impedance matching and also phase shifting.

The optimum load impedance to the driver stage needs consideration. It has already been postulated that the driver will be operating in a reduced conduction angle mode, thus providing a second harmonic current waveform. The use of a resistive Class B design will actually provide the required output. The resulting drain voltage has the ideal clipped voltage waveform, albeit shifted in phase, Figure 6.22.

The performance of this for a driver stage is adequate with a relatively high efficiency which will not impact the overall PAE, as described in section 2.3.

Keeping the driver stage gain at around 10dB and 50% efficient will maintain overall PAE within a few percent.

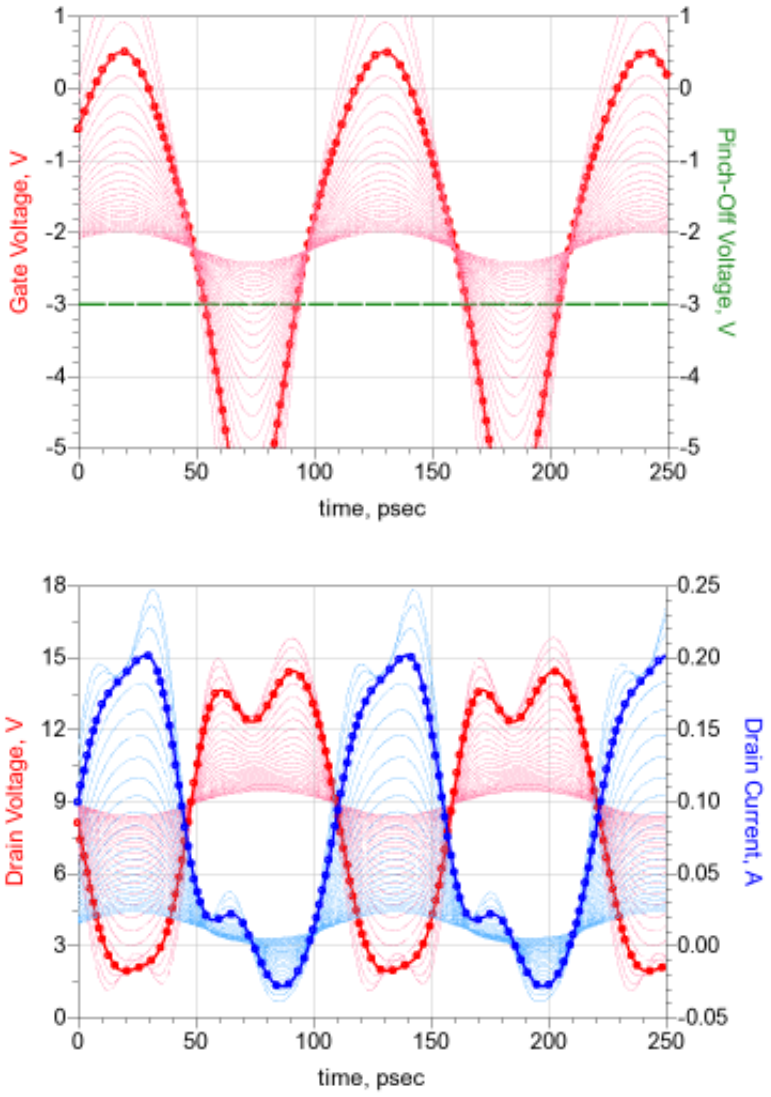


Figure 6.22 Ideal resistive load waveforms for 4x75 GaN25 driver stage shown at the intrinsic plane. The drain waveform is shown to have a good resistive Class B waveform with 2nd harmonic content. (Vds=9V, Vgs=-2.2V Class AB condition)

freq	v2[m5,1::1]	freq	v2[m5,2::2]
9.000 GHz	5.947 / 102.314	18.00 GHz	1.441 / 35.747

6.3.5 Interstage matching network design

The matching network is defined as the interstage between the driver and the power stage. The usual design procedure for the interstage matching requires obtaining the correct impedance across the desired bandwidth between these two terminating networks. This network is also often used as a parameter to flatten the overall gain response of multi-stage amplifiers [15][16] through direct synthesis techniques or by

optimisation. Interstage matching networks for MMIC implementation are treated comprehensively in [58].

In the case of HPA design the driver amplifier terminating impedance, presented by the network, needs to be close to the optimum power match condition to deliver adequate the power to the final stage. So the load line between the devices needs some consideration. This area of matching network design is difficult due to the mismatched load impedances at each end of the network. The driver stage presents a parallel RC network at the output, the device current generator optimum resistance plus the parasitic capacitance, Cds. The input to the Power stage Gate is a series RC network (plus parasitic elements) which is often a low impedance point.

The design of the matching network is further complicated by the simultaneous requirements for the power match of the driver stage to deliver the fundamental drive level to the transistor and the need for a specific 2nd harmonic relationship the fundamental.

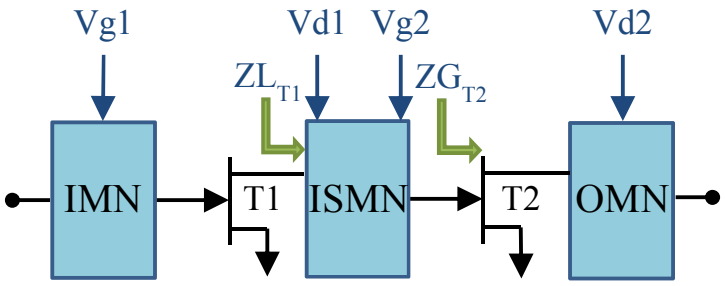


Figure 6.23 Typical two stage amplifier block diagram detailing the matching network definition.

The first step is to define the matching network terminating impedances. Referring to Figure 6.23, the load impedance presented to the driver device, ZL_{T1}, needs to be resistive (in parallel with the transistor Cds) when loaded with the power stage transistor gate impedance, ZG_{T2}.

The input impedance of the power stage is determined by simulating the 8x75µm device at the bias condition of the source injection configuration – with the output match (determined in section 6.3.2) included. This circuit is shown in Figure 6.24, which also includes the gate stabilising RC network. A further transmission line (Line1) element is also included as this is used to take account of an internal circuit probe point for future analysis.

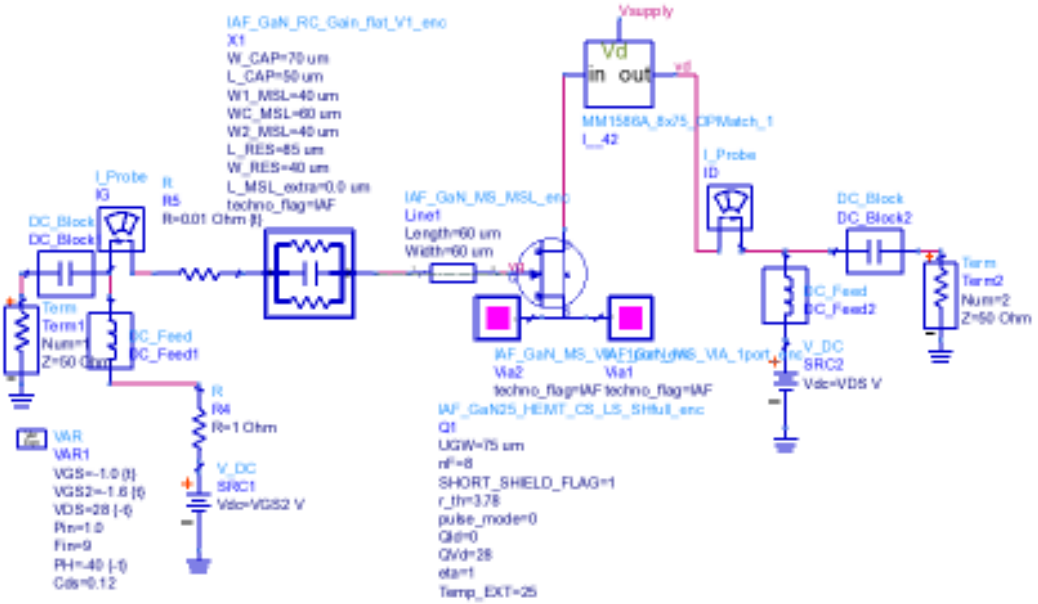


Figure 6.24 Simulation circuit and results for the input match (ZG_{T2}) for the 8x75 power stage device (Vds=28V, Vgs=-1.6V)

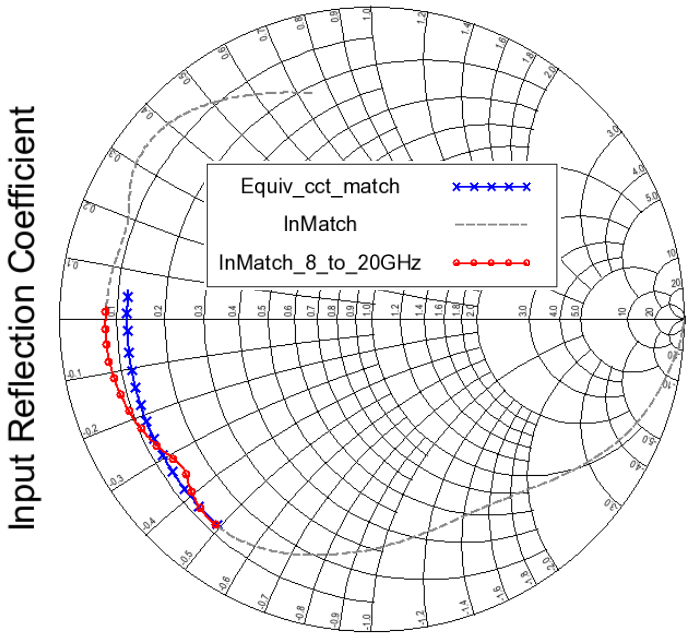


Figure 6.25 Simulation results for the input match for the 8x75 power stage device (Vds=28V, Vgs=-1.6V)

The results shown in Figure 6.25 show the input impedance of the power stage and an equivalent circuit representation for use in the initial interstage design. The equivalent network is a series RLC circuit (6.5Ω/0.12nH/0.6pF). This network is optimised over the fundamental band, 8 GHz to 10 GHz, but is valid across the fundamental and second harmonic frequency range, 8 GHz to 20 GHz. This simplification is an intermediate step to generate solutions for the matching network in a more easily manageable form than s-parameter datasets.

This input impedance needs to be transformed to the load impedance of the driver stage. In this case the driver is based on a 4x75µm device. The load line was optimised by reducing the bias voltage to 9V, a by-product of the device scaling requirement.

Using a drain bias of +9V, the knee voltage, Vk=3V and using the 800mA/mm current density, so Ids= (800*0.3) mA= 240mA, the current generator plane resistive load will be R_L= V/I = 2*(9V-3V)/0.24A ~50 Ohms. This is in parallel with the drain capacitance of 0.16pF.

The matching network requirement is therefore shown diagrammatically in Figure 6.26.

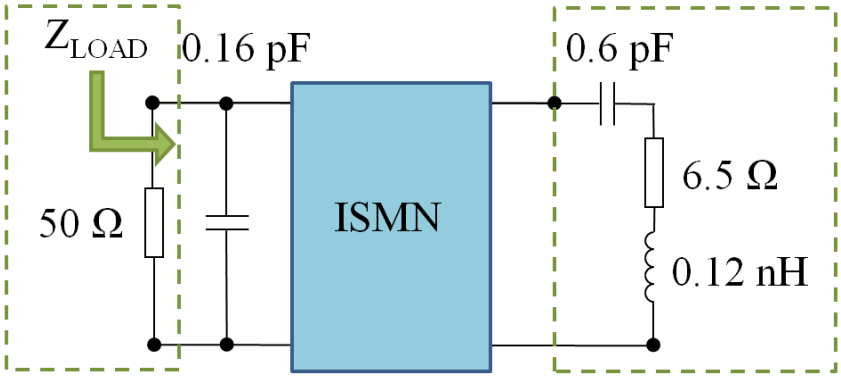


Figure 6.26 Interstage matching network definition between 4x75 driver stage (omitting Rd and Lg series elements) and 8x75 power stage using equivalent circuit terminating impedances. The optimum current generator plane impedance is shown as Z_{LOAD}.

This is the first criteria for the interstage matching network, with the network presenting a load impedance to the driver stage allowing optimum output power under the chosen operating class.

The second criterion for the ISMN relates to the phase shift through the network. This phase shift is required to take the driver stage output voltage waveform and translate this to obtain the correct phase relationship between fundamental and second harmonic at the gate terminal of the power stage.

The implementation of the interstage matching network needs another slight modification from the usual design process. In a traditional approach, the matching network will be designed across the fundamental frequency range only. To enable a voltage waveform engineered solution the network needs to be capable of supporting the second harmonic signal as well as the fundamental. The requirement for this design is to cover 8.5GHz to 9.5GHz, so the matching network is calculated to cover 8-20GHz, which allows margin for a guard band across both the fundamental and second harmonic frequency range.

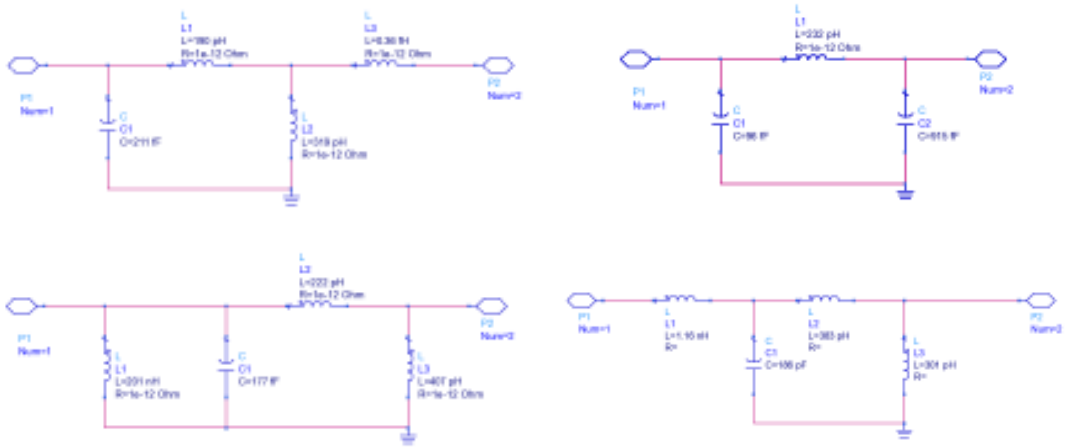


Figure 6.27 Interstage match options for 4x75µm output to the 8x75µm device. Using match 56/0.08p -> 6.5/.15n/0p6 across the frequency range 8-20GHz.

The final matching network consideration (and one that is easily overlooked) is that to ensure the network is capable of providing the required connectivity for the bias voltages and to isolate the dc levels between the two stages. To this end, a shunt inductor element would help for the drain side, allowing an easy access point for the high current drain feed.

Similarly, for the gate bias feed an inductor would be advantageous. In fact, the power stage gate voltage, V_{G2}, can be applied via a large resistor and need not impact the network design as this can be added almost any point as the impedance will not load the circuit. The value of this resistor is still needs consideration as high values will drop a significant voltage as the gate current flow increases under large signal drive conditions. This voltage drop will move the dc bias point of the power stage.

Finally, there needs to be a dc blocking capacitor in the network to isolate the gate and drain bias voltages. This can be added as a relatively small capacitor and absorbed in the network, as at these frequencies only a few Pico Farads is required for this.

Using the network in Figure 6.27(d) and simulating the driver circuit waveforms are shown in Figure 6.28. The output power at this condition is +24.5 dBm and the phase relationships are given in Table 6.4.

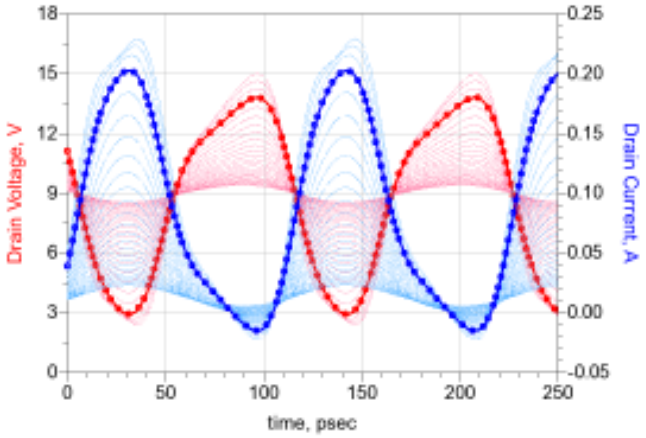


Figure 6.28 Extrinsic plane characteristic using 50 ohm load. Has the same 2nd harmonic content but shifted in phase.

freq	v2[m5,1::1]	freq	v2[m5,2::2]
9.000 GHz	5.341 / 78.877	18.00 GHz	1.120 / 11.320

Table 6.4 Phase relationship of the extrinsic drain voltages under resistive Class B operation.

The second harmonic content can be adjusted slightly by optimising the gate voltage further in the class AB bias range (Figure 6.29). Increasing the harmonic means moving towards the class B bias point but this will be to the detriment of the device gain which we require to keep as high as possible to maintain PAE.

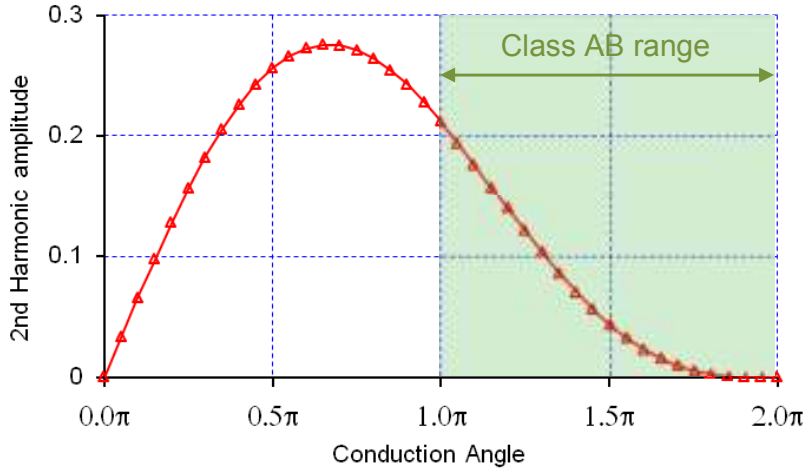


Figure 6.29 Second harmonic current component versus conduction angle, highlighting the operational class AB range.

Investigation of these voltage waveforms at the extrinsic[11] node (Figure 6.28) shows that there is approximately a 20% second harmonic content and phase shifts of 78.8° and 11.3° at the fundamental and second harmonic respectively (Table 6.4). This phase needs to now be manipulated by the matching network to provide the optimum relative phasing of 0° (or n*360°) at the intrinsic gate node of the power stage transistor.

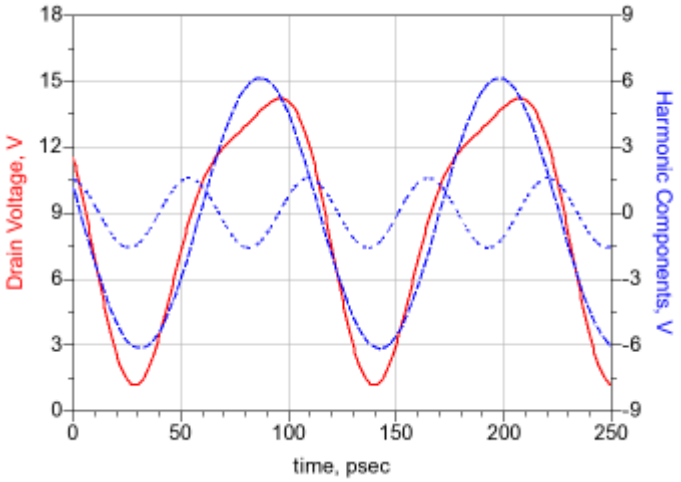


Figure 6.30 Idealised drain voltage waveform from Figure 6.28 considering just the first 2 harmonics and showing the relative phase relationship.

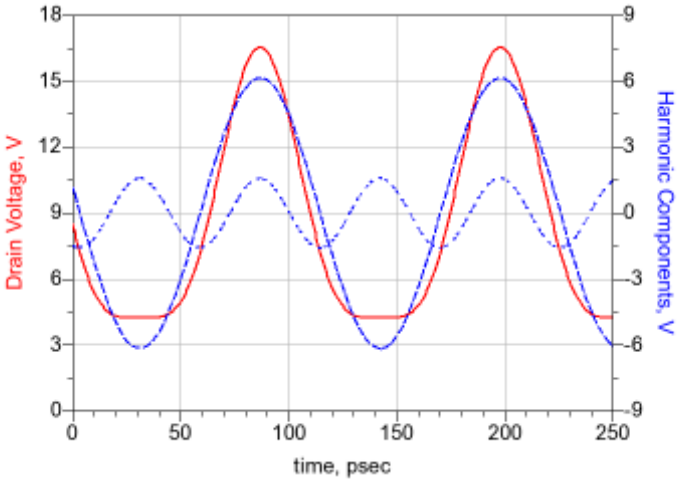


Figure 6.31 Response when the second harmonic component is shifted by -213.7°.

[11] It is valid here to consider the extrinsic node as this is the voltage which will be at the output of the transistor metallisation and connected to the next circuit element in the MMIC.

To maintain the correct phasing of the signals the second Harmonic needs shifting by twice the fundamental phase, to keep in synchronisation. So the second harmonic needs shifting by 2*78.8° = 157.6° but is already 11.3° so the total phase shift required is (157.6° - 11.3°) = 146.3° or -213.7°. This is demonstrated in Figure 6.31.

It is clear from this simple example that the matching network design and optimisation will need careful consideration, especially as any real network (even with ideal components) will have a phase shift at the fundamental and therefore the differential phase to the second harmonic will also move. It is not sufficient to define a relative phase shift between the two harmonic components, as the required second harmonic phase relationship is also influenced by any additional fundamental phase shift.

It must also be remembered that the phase shift needs to be defined at the intrinsic gate node, so that the terminating impedance (as defined by the equivalent circuit in Figure 6.26) is not the reference plane for the waveforms. Therefore the phase shift due to the device parasitic elements needs to be included in the analysis.

There are several other elements that also need including in this analysis of the matching network so that the total path phase shift is included. These include the RC stabilisation network, any interconnecting line (including the probe point in the interstage network in this design) and the dc blocking capacitors and bias interconnection points.

The phase shift through the RC network and the interconnecting line (used as the GSG probe contact point in the design) is shown in Figure 6.32. This shows a differential transmission phase shift of 18° (3° at 9GHz and 22° at 18GHz), so is significant.

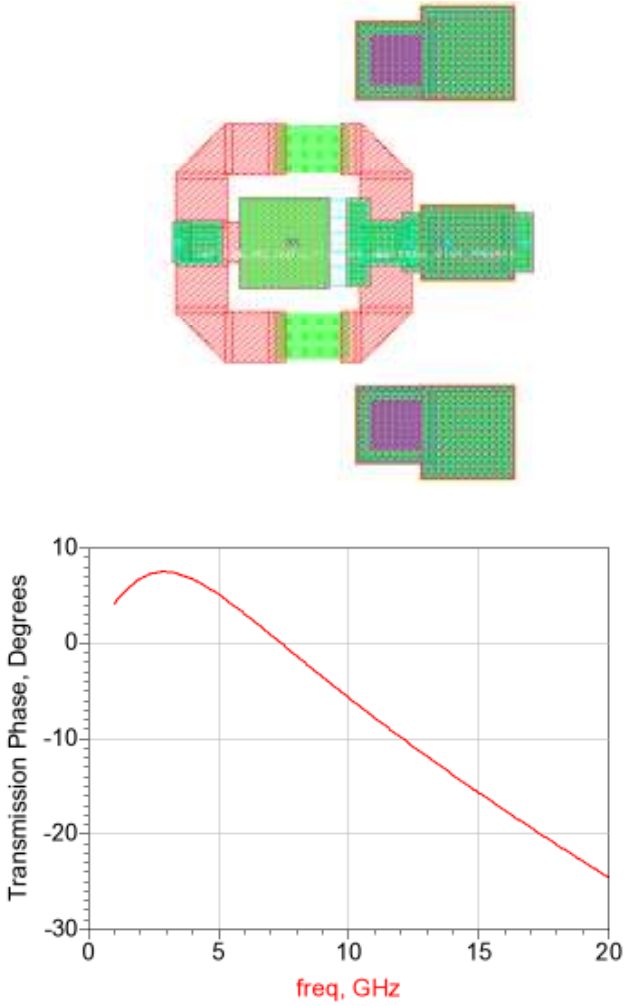


Figure 6.32 Response for the 8x75 GaN25 RC stabilisation network showing the differential phase shift between fundamental and second harmonic frequencies.

Initial design strategy here chose to concentrate on the matching network topology in order to include the response required at the second harmonic frequency. This is generally not addressed (or considered) in the traditional matching network design [16]. Where this is addressed it has largely been confined to additional harmonic 'tank' circuits to short out harmonic content to reduce the conduction angle widening caused by the varactor effect of the gate capacitance [43][47] or during the optimisation process with source pull data.

The initial assessment of the matching networks included one with the approximate phase shift response, included a shunt inductive element for the bias feed point and had element values ideally suited to MMIC implementation, Figure 6.33.

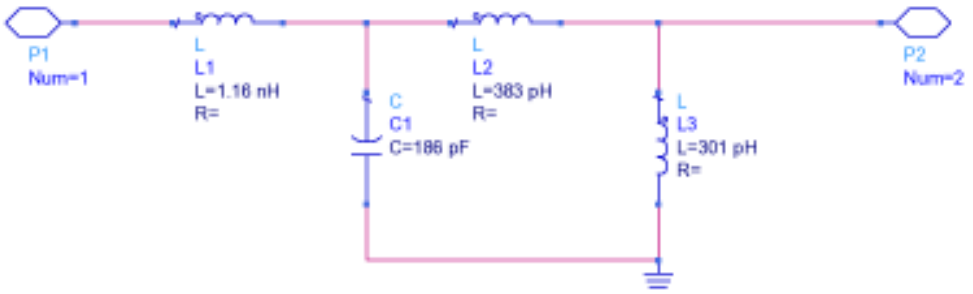


Figure 6.33 Ideal interstage matching network design for the 4x75 output impedance to the 8x75 GaN25 input device with RC stability network.

The phase shift of the ideal element matching network is shown in Figure 6.34. The fundamental phase shift is +11° and the second harmonic phase is -119°

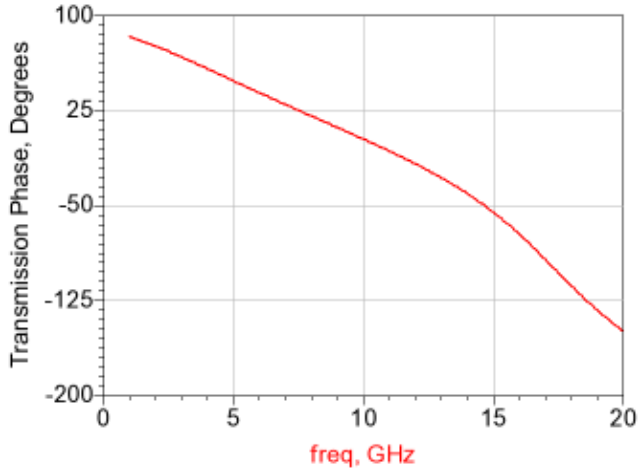


Figure 6.34 Transmission Phase shift of the ideal interstage matching network.

Translating the circuit topology into MMIC implementation is relatively straight forward as lumped element components are available in the PDK library. Some translations of the elements into distributed elements has been used to allow the optimisation of inductance and capacitance and include interconnects between the components.

The phase shift response through the resulting MMIC circuit is shown in Figure 6.35 which is close to the required phase shift to successfully create the ideal waveforms, Figure 6.36.

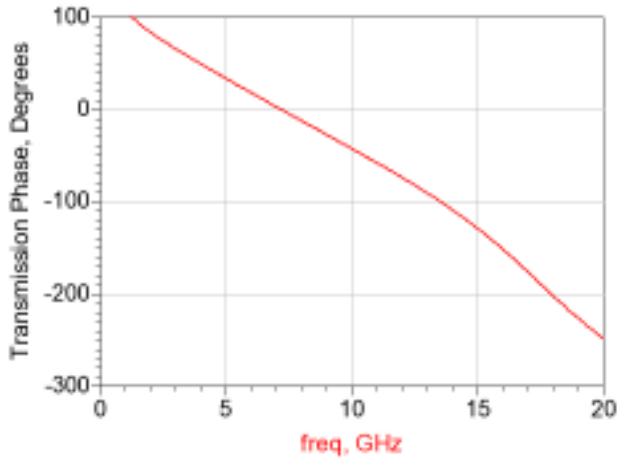


Figure 6.35 Phase shift through MMIC interstage network including dc blocking components and parasitic elements.

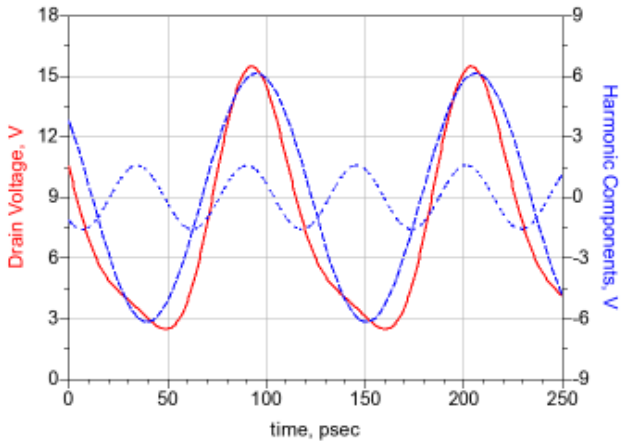


Figure 6.36 Approximated waveform by modifying the driver stage harmonic components with the MMIC matching phase response.

Including this network in the amplifier design schematic, the response of the overall simulated circuit is shown in Figure 6.37. The gate voltage is seen to have a small amount of second harmonic content and the phase difference is close to the required zero degrees and reflects the simple analysis of Figure 6.36. This response is, however, not ideal and some tuning or optimisation is required.

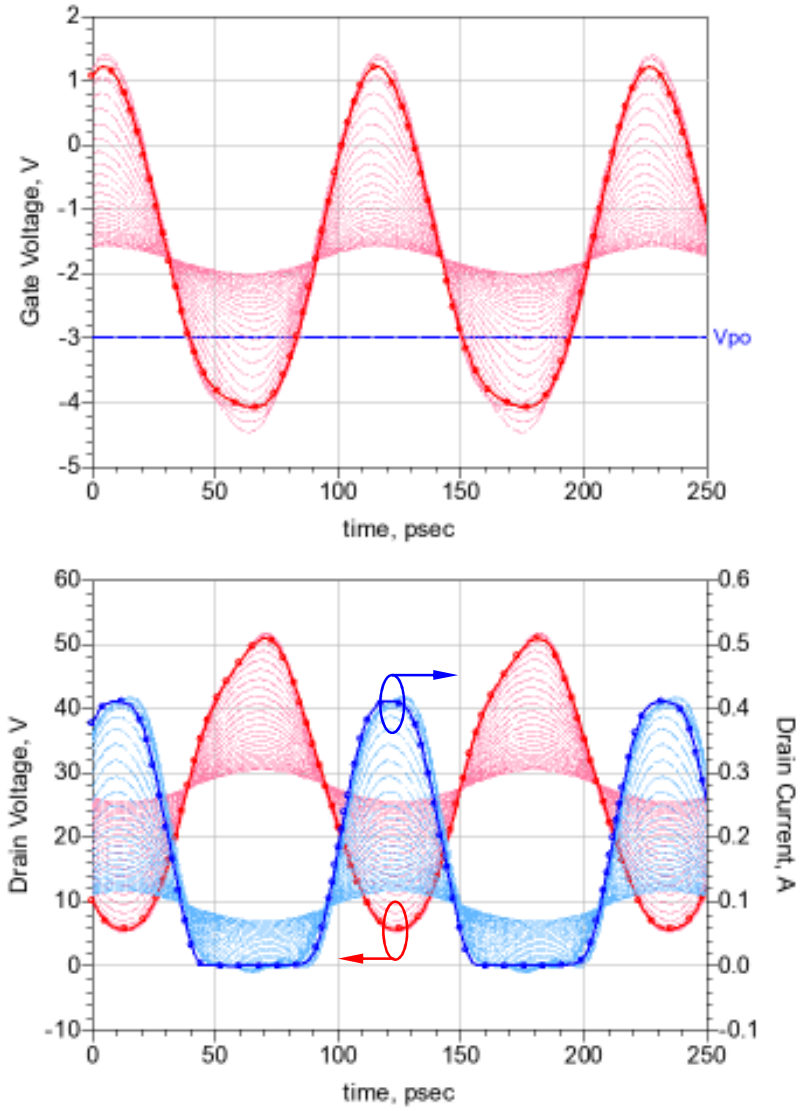


Figure 6.37 Simulation results of the basic 2 stage 'source injection' amplifier circuit. Input drive signal swept 0 to 20dBm.

Optimisation of HPA circuits has usually concentrated on the input and output criteria of the amplifier. As previously mentioned this is acceptable for single transistor circuits and amplifiers. This approach, however, does not address the specific problem of multi-stage amplifiers where the internal circuit elements are optimised based on input and output criteria only. This use of external node parameters (e.g. output power, efficiency etc.) to drive the decision process for the indirectly coupled elements in the internal nodes of a circuit is questionable.

The method taken here is to not focus on the output power or efficiency as the optimisation goal but to use the internal voltage node waveforms to drive the interstage circuit tuning. Optimising these waveforms to have the correct amplitude and phase relationship at the intrinsic gate terminal of the power stage transistor will result in the optimum output current waveforms and hence the output power and efficiency will follow.

The optimisation is set up by firstly placing a voltage and current probe at the internal interstage node. In this way the intrinsic gate voltages can be determined either by de-embedding the resulting voltage response or by placing the voltage node between the positive/negative de-embedding 'predistortion' network as defined in section 4.2 and using the voltage value directly.

Then the optimisation goal is defined by choosing the fundamental amplitude to reach $V_{g,max}$, a second harmonic amplitude (optimum of 0.414*fundamental) and a second harmonic relative phase of 0°. The weighting of the optimisation goals is targeted more towards the phase shift rather than amplitude of the second harmonic. It was concluded in section 5.4.2 that any second harmonic component will improve efficiency but the phase alignment should be maintained (section 5.4.6). The optimisation goals used in the simulation circuit are shown in Figure 6.38, with the relative phase weighted twice as high as the amplitude response. The fundamental and second harmonic are targeted toward the optimum ratio.

Figure 6.38 Optimisation goals for the 2 stage GaN MMIC

The Large signal performance of the optimised circuit is shown in Figure 6.39. The intrinsic node voltage now shows the clipped sinewave form more closely. Also included is the probe point voltage waveform. This is the waveform that would be measured at this node in the circuit. It is clear this is distorted slightly but the second harmonic content can be seen.

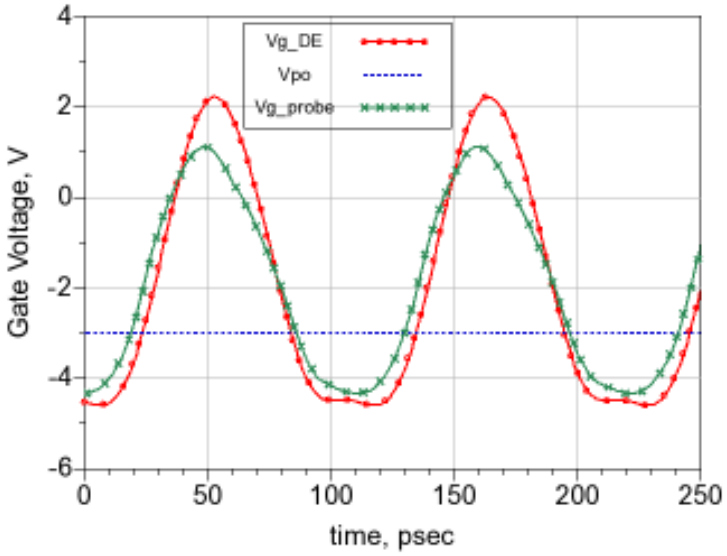


Figure 6.39 Large signal performance after optimisation – intrinsic gate voltage and probe voltage waveforms.

The second harmonic relative amplitude and phase response is shown in Figure 6.40 versus fundamental input power. This plot also shows the offset between the probe point and intrinsic waveforms. The intrinsic waveforms define the performance and the phase relationship is zero for a drive level of approximately +18dBm.

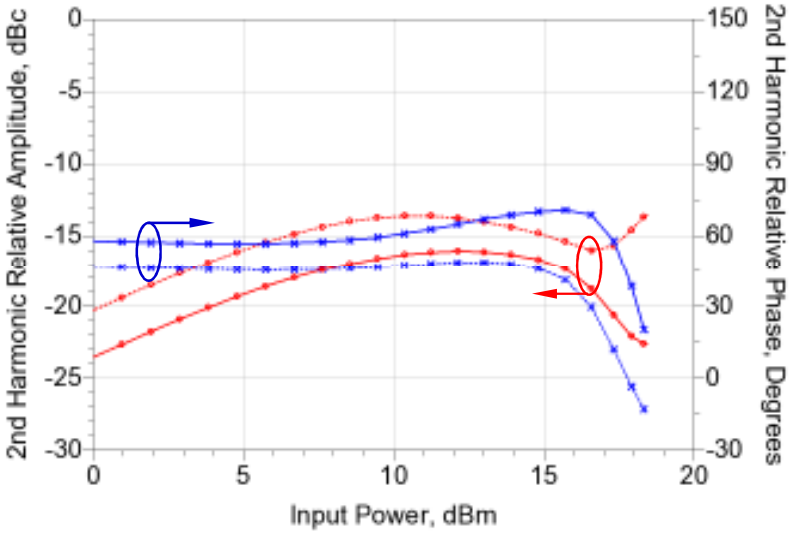


Figure 6.40 Simulated response for the circuit FXX003GE showing probe point measurement plane response (solid) and intrinsic Cgs plane response (dashed) at 9GHz.

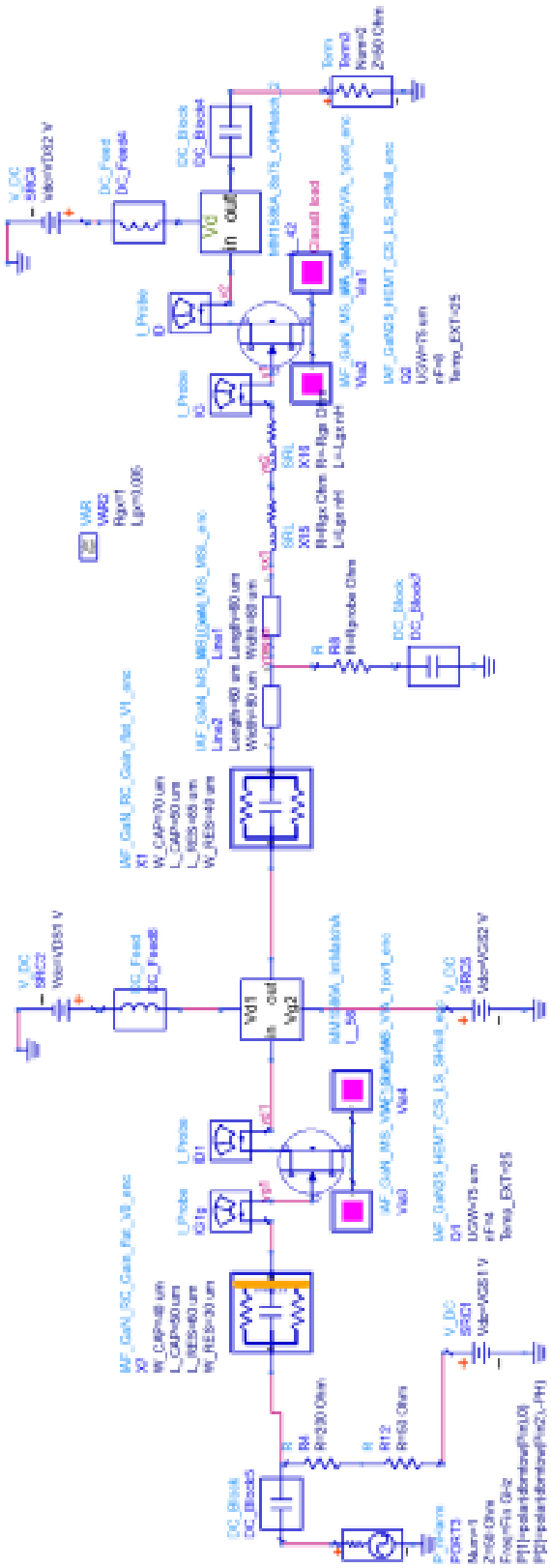


Figure 6.41 Simulation circuit for GaN two stage amplifier MMIC MM1586A

The small signal gain response for the amplifier cells is shown below in Figure 6.42. This shows that there is indeed a reduction in the gain when using the Class B bias condition, which is offset using the source injection.

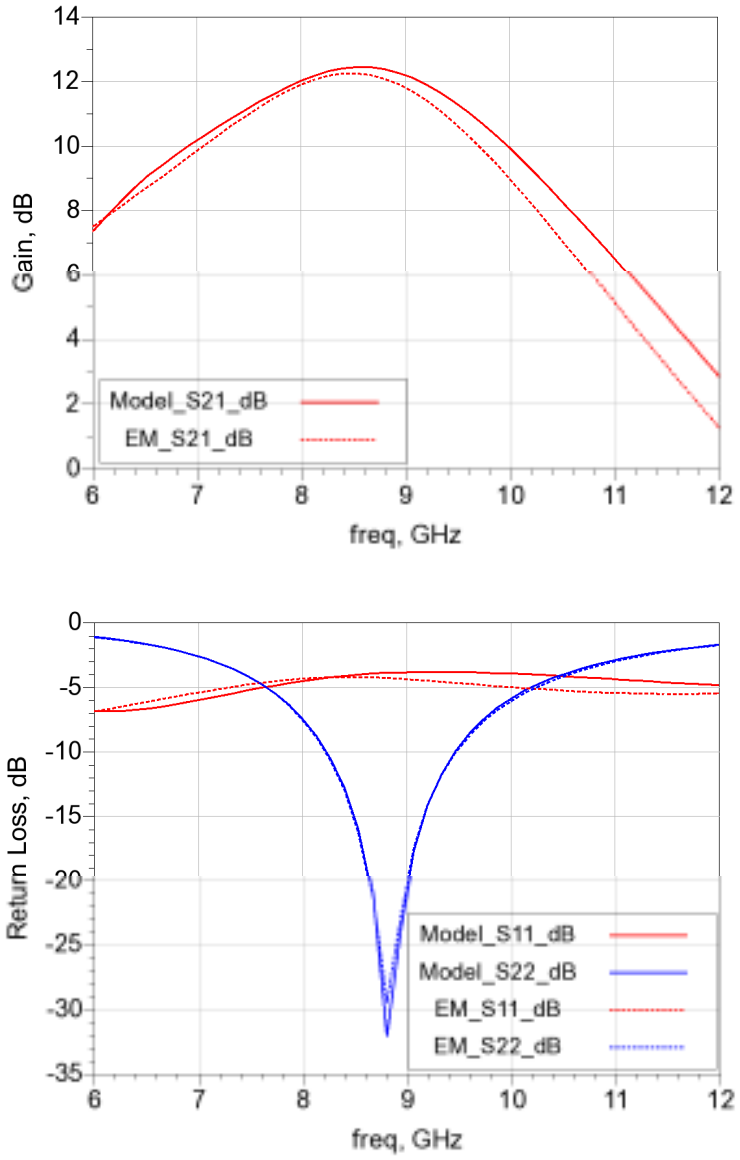


Figure 6.42 Simulated S-parameters for the GaN25 2 stage amplifier MM1586A. Bias conditions: Vd1=+9V (12.7mA), Vg1= -2.1V, Vd2=28V (92mA), Vg2=-1.8V.

6.3.6 MMIC Design layout

The GaN25 two stage MMIC amplifier design, MM1586A_TSP_A9, is shown in Figure 6.43 below with the matching networks and the test cells for the power stage and matching network are shown in Figure 6.44 as cell reference MM1599A_TSP_A9.

The MMICs were fabricated on mask IAF1072 and 20 devices of each chip were delivered for evaluation. The photographs for the amplifier cells are also shown in Figure 6.43.

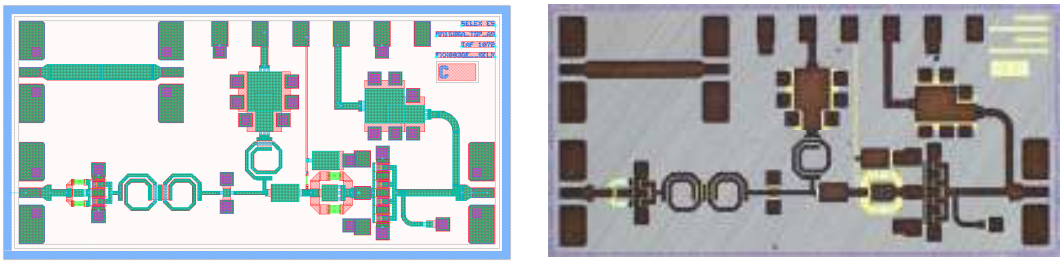


Figure 6.43 MMIC artwork and photograph for 2stage amplifier MM1586A_TSP_A9 (IAF reference FX003GE) from wafer IAF1072. Also included is a GaN25 TRL thru line.

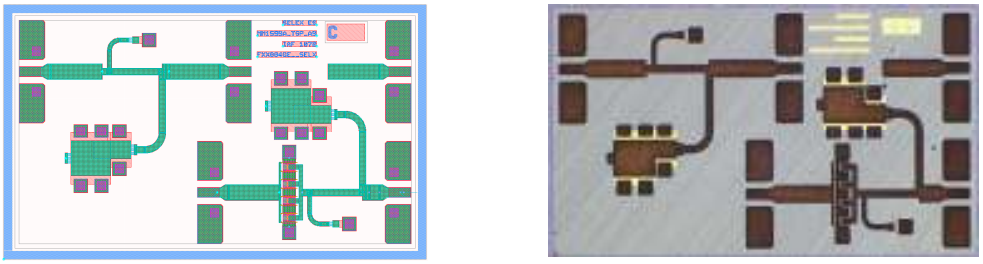


Figure 6.44 MMIC artwork and photograph for GaN25 8x75µm transistor test cell MM1599A_TSP_A9 (IAF reference FX004GE) from wafer IAF1072. Class BJ matching network and TRL 'open' are also shown.

6.4 Interstage Waveform Measurement

The design of the matching networks has shown that the driver stage waveform can be modified by the matching network by considering the second harmonic content, to drive the power stage transistor into a source injection mode of operation. These waveforms will need to be verified after fabrication to confirm that the proposed operating point is actually realised.

The measurement of the interstage waveforms is not straight forward unlike a simple 2 port (single stage) amplifier, where the input and output ports are easily accessible and the measurement system at Cardiff University [72] uses these for full transistor characterisation.

There are two generic options for measuring the internal waveforms

(i) Non-contact measurement – Using an E-field probe, where the measurement probe does not come into physical contact with the circuit.

(ii) Direct contact measurement – Using a probe connected to the circuit to sample the voltages and currents.

6.4.1 Non-contact measurement

The use of the E-field probe is a non-intrusive measurement technique and has been demonstrated by Dehghan [118][119]. The application has been used to identify the waveforms across the multiple bond wire connections between the package and die at low microwave frequencies. The drawback of this approach is the sensitivity of the probe at the power levels present in this current circuit – the initial application space proposed for this technique is probing the fields across the Gate nodes of 100W transistors in Doherty PAs.

Here the power level at the interstage is only around 100mW and there are no bond wires in this current circuit configuration as it is a monolithic construction. The sensitivity of the probe given these two constraints leads this approach not being pursued. Additionally, the frequency range is much higher, requiring field probe bandwidths in excess of 18GHz to capture any meaningful waveform data, which makes this approach difficult to use.

6.4.2 Direct contact measurement

Traditional use of a direct measurement probe has a drawback of loading the circuit under test if used in an internal circuit position. This is undesirable so careful consideration of the probing point and signal sampling network is required to ensure the circuit performance is not modified when the probe is or is not connected to the circuit.

Measurements using a calibrated probe have been proposed [120] but no consideration was presented on the loading effects on the measurements. Some internal probe points are low impedance and thus the probing network (if in a 50Ω environment) looks high impedance and has little effect on the measurements.

The bandwidth of the signal is also an important consideration. The network is required to support the harmonic content of the waveform with sufficient dynamic range.

Proposed use of the Cardiff ALPS for an interstage voltage node measurement is defined. Using 2 identical circuits initial measurements can be performed between the input and output of the amplifier, Figure 6.45(a), across a defined range of bias voltages and power levels.

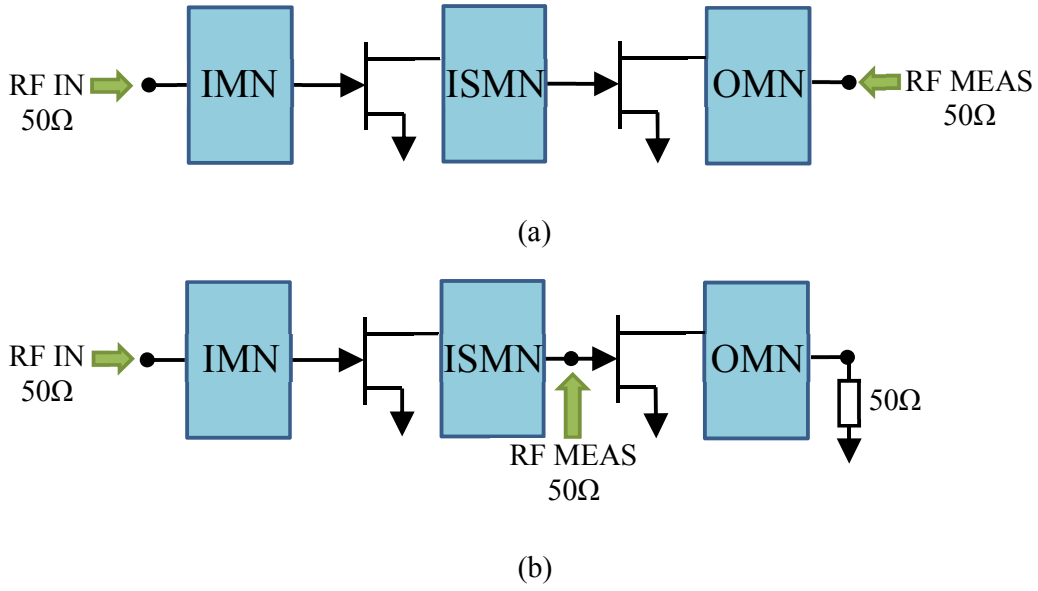


Figure 6.45 Proposed measurement set-up for interstage voltage probing (a) overall amplifier measurements input to output (b) Output loaded amplifier with interstage probe measurements.

A second circuit requires the amplifier terminated in a matched load, Figure 6.45(b). This is used to enable placement of the output measurement probe in the centre of the interstage matching network. Measurements are performed across the same bias conditions and power levels as before, and the data merged to define a full dataset of input power versus output power and internal voltage waveforms.

The benefit of using the Cardiff ALPS for this measurement is that the full capability on harmonic load pull can be utilized. In fact using this system the fundamental, second and third harmonic impedances can be defined on the 'output'[12] port2 measurement probe.

[12] Port 2 is traditionally defined as the output port, however, in this set-up it is used for measuring an internal circuit node response. The 'output' reference will still be used to define this port in this work.

6.5 MMIC Measurements

The GaN25 MMICs, MM1586A – FXX003GE and MM1599A – FXX004GE, need to be mounted to a suitable fixture for testing. This fixture needs to handle the power dissipation and maintain a suitable device junction temperature for reliable operation. It is also required to provide the bias connections to the chip.

The test jig assembly consisted of a 0.5 mm thick Copper-Tungsten (CuW) carrier with the GaN chips mounted using Eutectic Gold Tin (Au80Sn20) solder and a flux less, void free solder attachment method developed in Selex ES Ltd. The ancillary dc bias bypass capacitors were mounted using conductive silver epoxy Abelstik 84-1 LMI [121]. The MMIC/capacitor circuit assembly was gold wire bonded using 17um diameter gold wire, with double wires used for high current carrying drain supply lines. The resulting carrier assembly was mounted in a general purpose Kovar based package using high thermal conductivity silver epoxy, EPO-TEK H20E [123]. The package has dc connector glass-to-metal seal pins in the sidewall to allow easy biasing using soldered wires connected to standard power supply equipment.

Connections to the test circuit assembly from the feedthrough pins was made using 0.003” x 25um Gold ribbon for improved mechanical ruggedness and current handling over long distances[13]. The full test package assembly is shown in Figure 6.46, along with the individual circuit details.

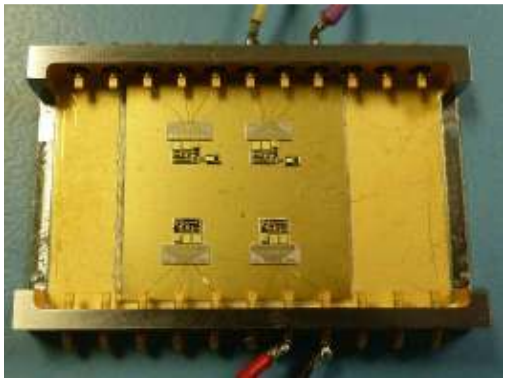
RF connections and measurements are performed on chip by using Cascade ACP40-GSG-200 probes calibrated using the ISS substrate [70] on a Cascade® 12000 probe station.

The circuits were measured under small signal and large signal operating conditions. Small signal s-parameter measurements were performed using a Keysight Technologies PNA-X Vector Network Analyser (VNA).

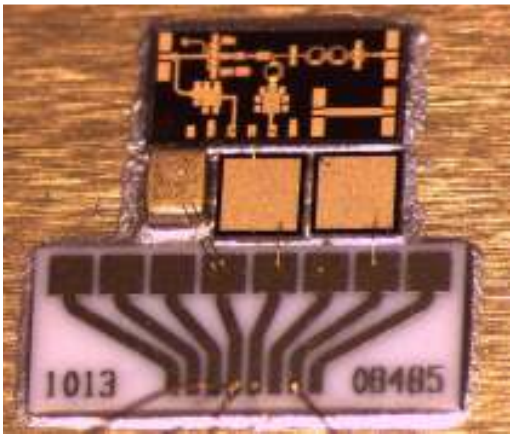
The large signal characterisation was performed using both with conventional scalar power meter test configurations, for power in/power out measurements, and the Cardiff ALPS where waveform information is required.

The amplifiers were measured across a range of bias voltages.

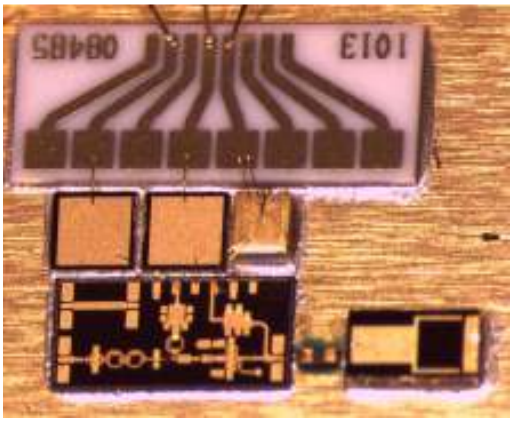
[13] The current handling capacity of bond wires is a function of length as well as cross-section.



(a) Test fixture



(b) Two stage amplifier GaN MMIC assembly detail

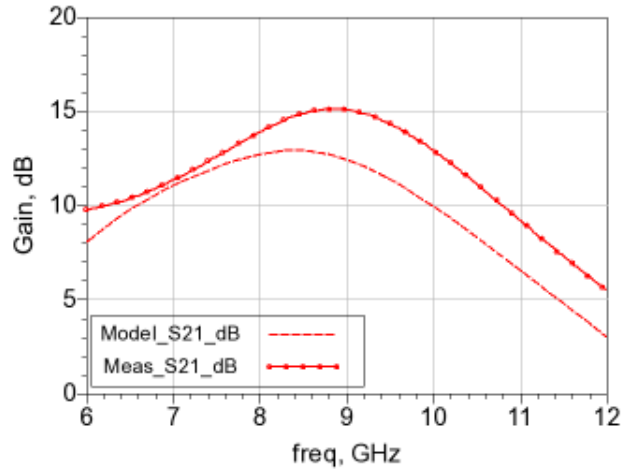


(c) Two stage amplifier GaN MMIC assembly detail for interstage probing

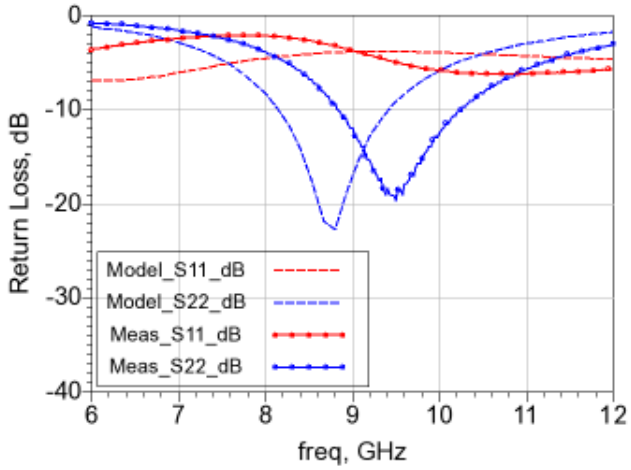
Figure 6.46 FXX003GE.1072 GaN amplifier assembly (a) test jig mounting showing 4 circuits (b) GaN chip assembly for RF-on-chip power measurements and (c) GaN chip assembly for interstage voltage measurements – the diamond 50 ohm termination on the amplifier output is clearly seen on the RHS.

6.5.1 S-parameter measurements

The overall two stage amplifier circuit MM1586A_TSP_A9 was measured in the test fixture (Figure 6.46(b)) under small signal conditions. The measured s-parameters are shown in Figure 6.47, along with the simulated data.



(a)



(b)

Figure 6.47 MM1586A_TSP_A9, chip reference FXX003GE.1072.C10 s-parameter measurements. (a) Gain response and (b) return loss response. Bias conditions: Vg1=-2.2, Vd1=9V (10mA), Vg2=-1.8V, Vd2=25V (108mA)

There is more gain measured than predicted by the PDK large signal model – even when adjusting to achieve the same bias current density. Further improvement in gain is also noted when modifying the bias voltages (Figure 6.48) of the driver stage or increasing the first stage current.

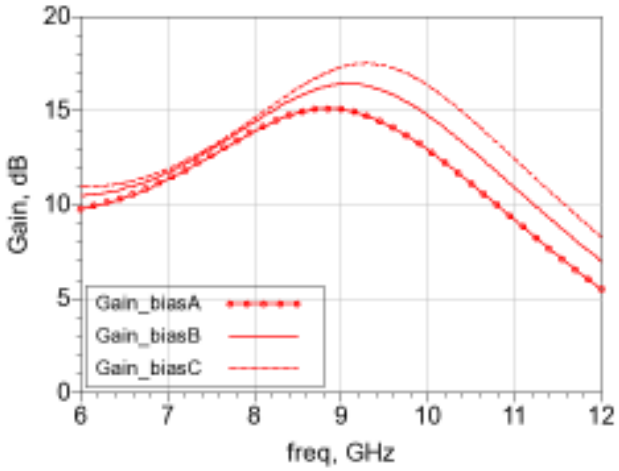


Figure 6.48 Measured gain response for varying first stage bias voltage Vd1 A=9V, B=12V, C=15V. Vg1=-2.5, Vg2=-1.8V, Vd2=25V (108mA)

It is also noted from Figure 6.47 that the output match is centered higher than expected, above the operating frequency, suggesting the output match is not optimally aligned. Further s-parameter measurements were performed on the output matching network (Figure 6.49) using chip MM1599A_TSP_A9. The response shows reasonable agreement to the simulation, with a slight shift up in frequency for the optimum Class B impedance to 9.5 GHz from 9 GHz, as indicated in the overall amplifier s-parameters.

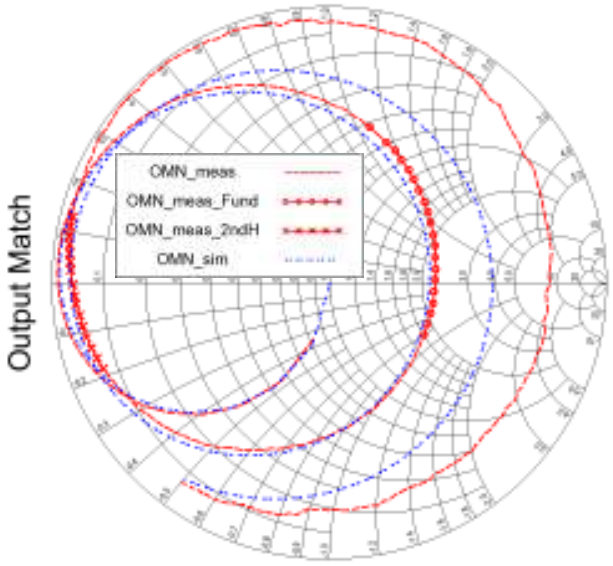


Figure 6.49 Output matching network measurements for test cell MM1586A_TSP_A9 (FXX004GE.1072.C11). Symbols mark the fundamental and 2nd Harmonic ranges.

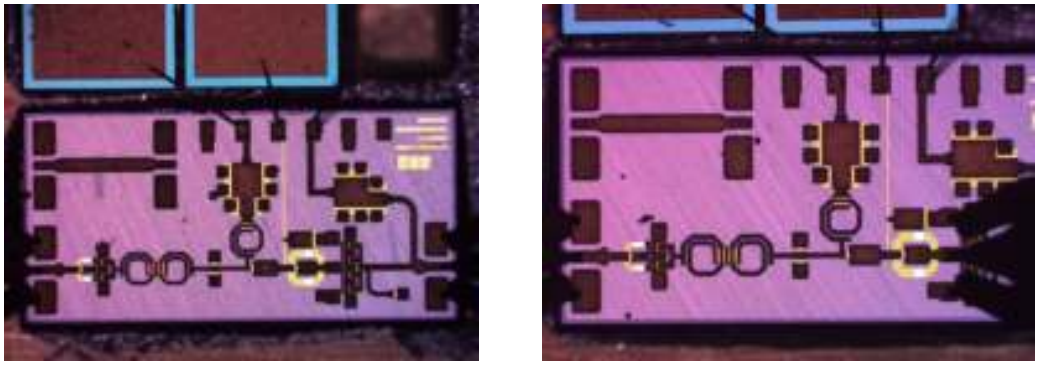
6.5.2 Large Signal measurements.

Large signal measurements follow the approach outlined in section 6.4.2, using two measurement datasets, one for each of the probe positions.

i. Input1 – Output2 to measure the overall two stage amplifier performance. This configuration is shown in Figure 6.50(a) with RF GSG probes.

ii. Input1 – Input2 to measure the interstage waveforms appearing at the power stage gate terminal, Figure 6.50(b), with the full circuit detailed in Figure 6.51.

The same measurements are performed on both circuits and the datasets correlated to provide an overall picture of the 2 stage amplifier performance.



(a) (b)

Figure 6.50 FXX003GE GaN amplifier assembly showing measurement probes (a) for the full amplifier and (b) detail of the interstage probe points

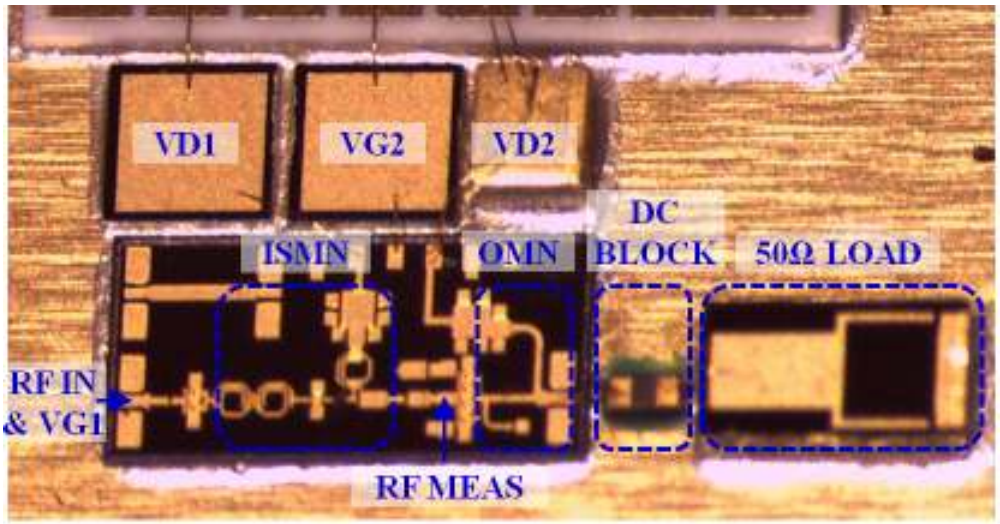
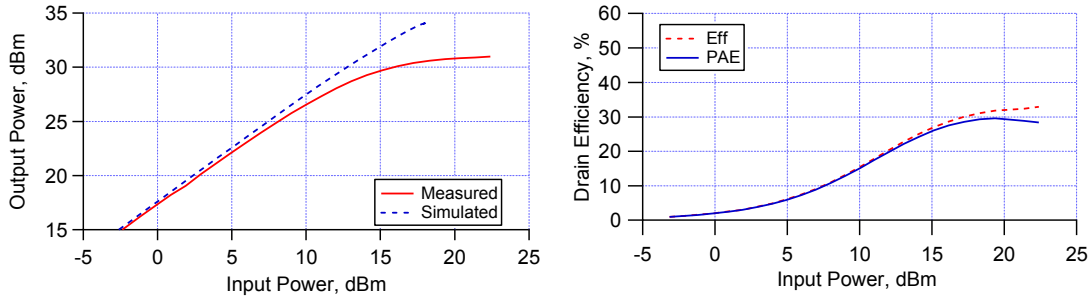


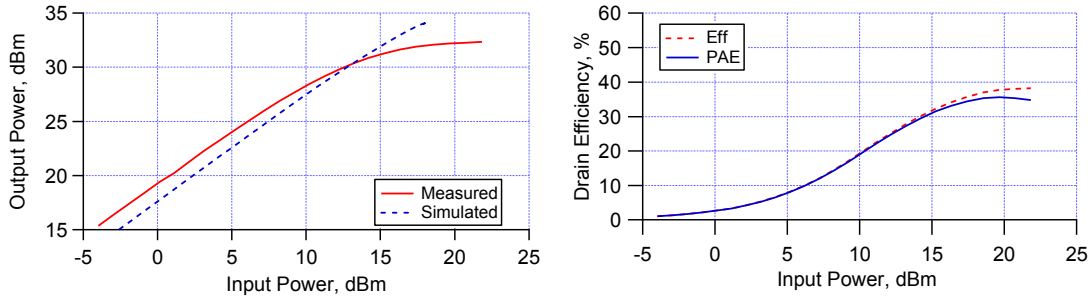
Figure 6.51 Photograph of the test circuit detailing the interstage voltage measurement. This is the practical implementation of the schematic in Figure 6.45(b)

6.5.2.1 Initial measurements

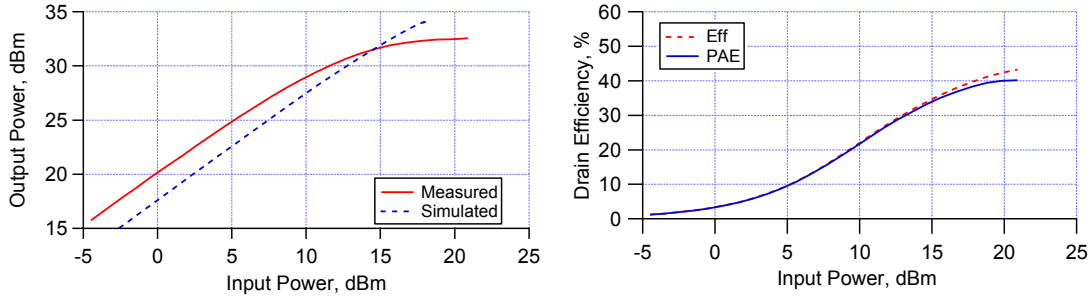
The initial GaN MMIC amplifier test cell measurements, based on the Cardiff active load pull system [72], are shown in Figure 6.52. It can be see that the power gain at low power is consistent with that from the s-parameter measurements, however the saturated power characteristics limit at approximately +32.5 dBm, compared to the predicted +35 dBm at the designed bias point of Vds=+28V.



(a) id25686 9GHz, Vg1=-2.2, Vd1=9V, Vg2=-1.8V, Vd2=28V



(b) id25700 9GHz, Vg1=-2.2, Vd1=12V, Vg2=-1.8V, Vd2=28V



(c) id25706 9GHz, Vg1=-2.2, Vd1=15V, Vg2=-1.8V, Vd2=28V

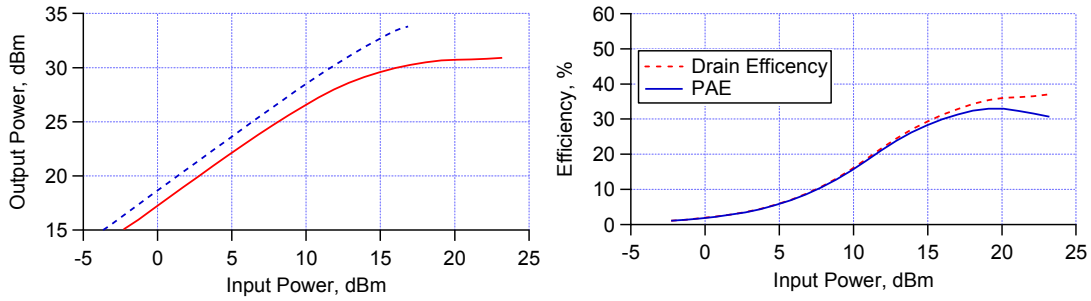
Figure 6.52 FXX003GE.1072.C10 GaN amplifier assembly measured performance and simulated response (Vg1=-2.2, Vd1=swept, Vg2=-1.8V, Vd2=28V)

The measurements at 28V show that the amplifier efficiencies are rather poor. All bias voltages were varied to improve the performance. The driver stage gate voltage was increased towards class A to improve gain, the source injection bias voltage was adjusted and the driver stage drain supply increased from 9V to 15V.

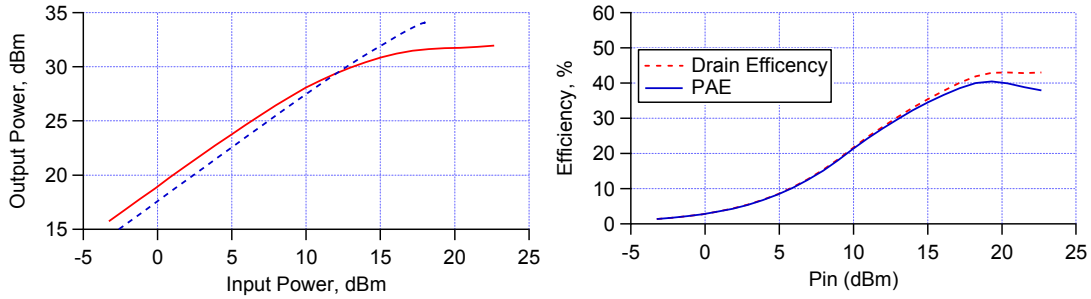
The increase in the drain supply of the driver stage showed improved performance, however, the peak PAE achieved was still only 40.2%.

The improvement in performance with driver stage supply indicates the stage is not powerful enough at driving the output stage into compression. This affects efficiency considerably. A lower drain voltage supply for the power stage operation can mitigate this effect somewhat by improving the efficiency whilst having a minimal effect on the output power.

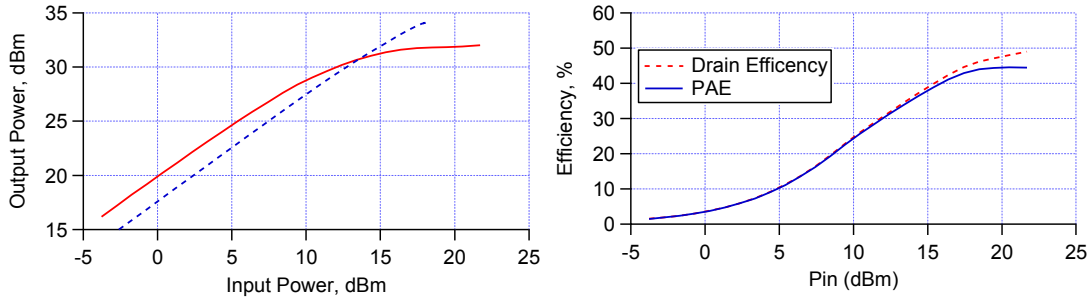
Repeating the measurements at the lower drain bias point of 25V, the basic measurements for the 2 stage GaN amplifier are shown on Figure 6.53 and Figure 6.54, for a variable first stage drain supply at 9 GHz. This is included as the driver stage shows signs of poor power output such that the power stage is not driven adequately.



id25719 9GHz, Vg1=-2.2, Vd1=9V, Vg2=-1.8V, Vd2=25V

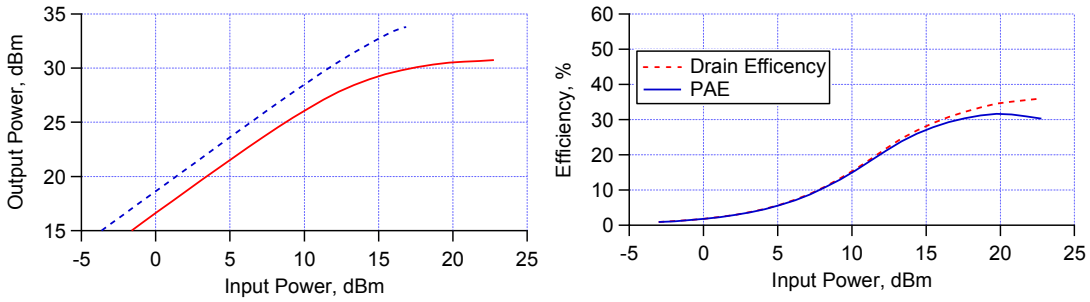


id25720 9GHz, Vg1=-2.2, Vd1=12V, Vg2=-1.8V, Vd2=25V

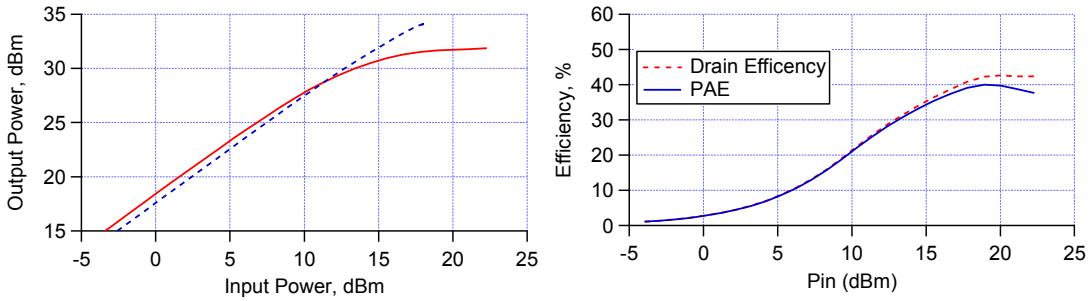


id25721 9GHz, Vg1=-2.2, Vd1=15V, Vg2=-1.8V, Vd2=25V

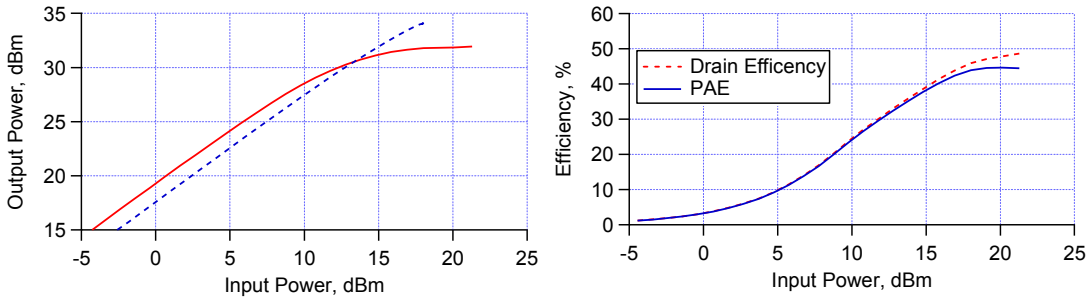
Figure 6.53 Power and Efficiency measurement results for FXX003GE.1072.C10 GaN amplifier assembly. Variable first stage drain bias, Vd1. (Vg1=-2.2, Vd1=Swept, Vg2=-1.8V, Vd2=25V)



id25724 9GHz, Vg1=-2.5, Vd1=9V, Vg2=-1.8V, Vd2=25V



id25723 9GHz, Vg1=-2.5, Vd1=12V, Vg2=-1.8V, Vd2=25V



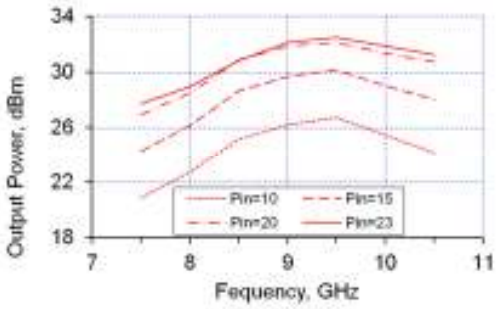
id25722 9GHz, Vg1=-2.5, Vd1=15V, Vg2=-1.8V, Vd2=25V

Figure 6.54 Power and Efficiency measurement results for FXX003GE.1072.C10 GaN amplifier assembly. Variable first stage drain bias, Vd1. (Vg1=-2.5, Vd1=Swept, Vg2=-1.8V, Vd2=25V)

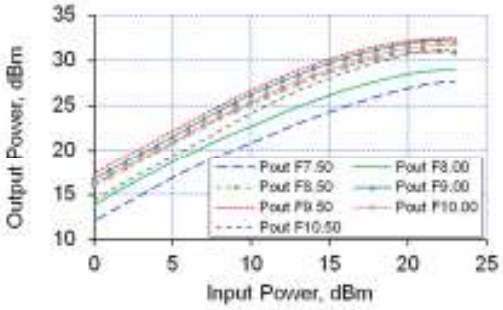
Under these modified bias conditions the efficiency is improved by more than 5% across these cases and the saturated output power level drops only marginally from +32.5dBm to +31.8 dBm.

6.5.2.2 Swept frequency measurements

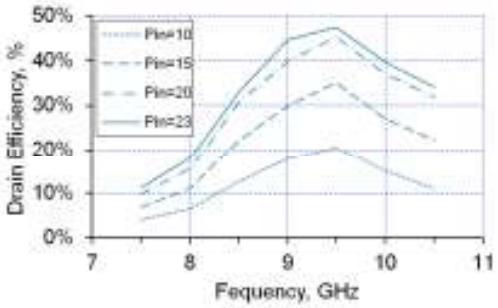
Using standard scalar power measurement techniques, the circuits were measured across a range of input powers and frequencies, at the bias conditions indicated from the analysis of section 6.5.2.1.



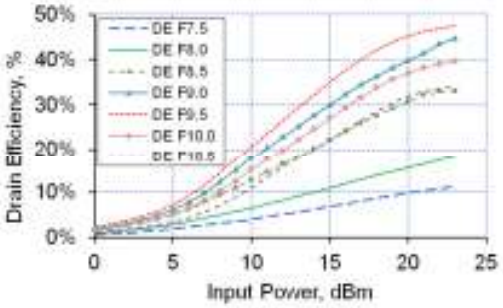
(a) Output Power versus Frequency



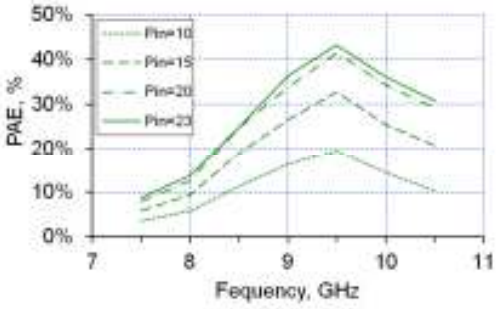
(b) Output Power versus Pin



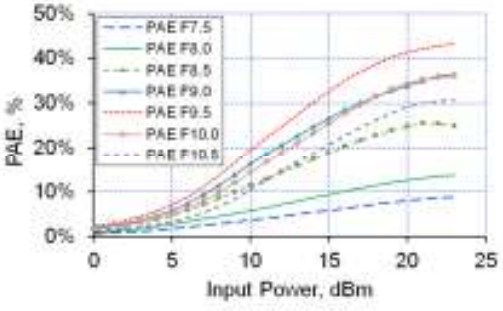
(c) Drain Efficiency versus Frequency



(d) Drain Efficiency versus Pin

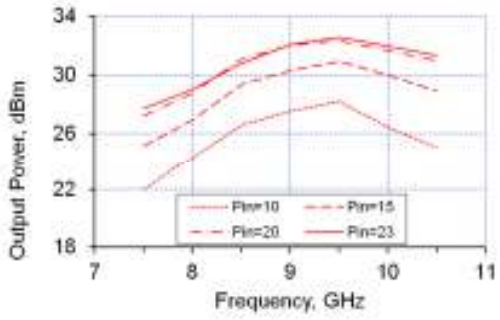


(e) PAE versus Frequency

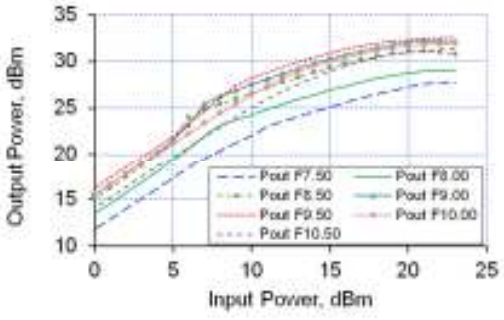


(f) PAE versus Pin

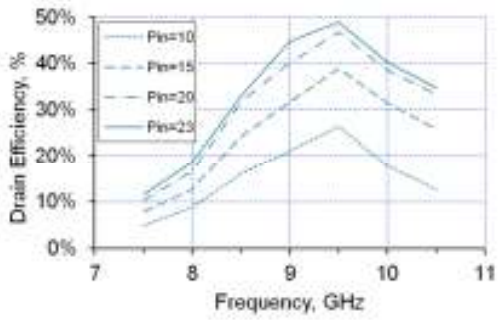
Figure 6.55 FXX003GE.1072.C10 measurements (Vg1=-2.5, Vd1=15V, Vg2=-1.8V, Vd2=25V) with various input power levels.



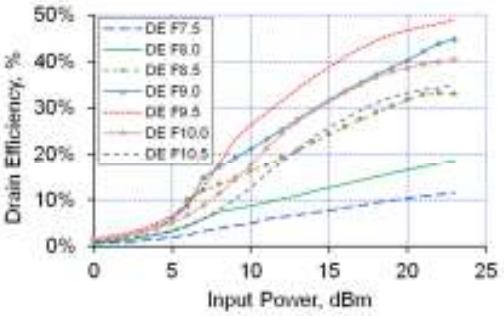
(a) Output Power versus Frequency



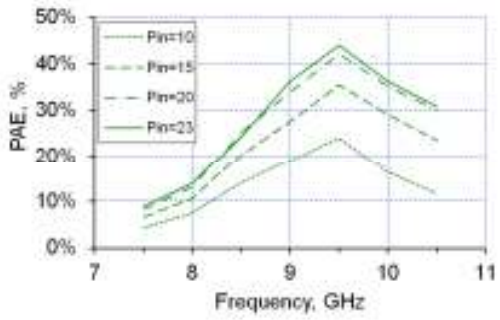
(b) Output Power versus Pin



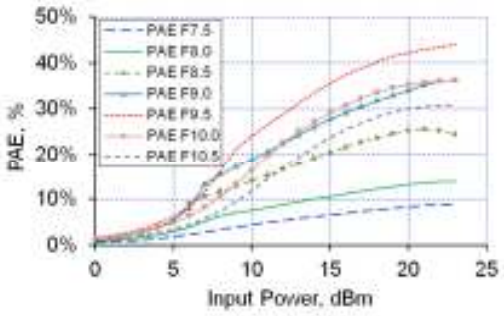
(c) Drain Efficiency versus Frequency



(d) Drain Efficiency versus Pin



(e) PAE versus Frequency



(f) PAE versus Pin

Figure 6.56 FXX003GE.1072.C10 measurements (Vg1=-2.2, Vd1=15V, Vg2=-1.8V, Vd2=25V) with various input power levels.

These measurements for the overall 2 stage circuit confirm the power performance response is shifted up in frequency slightly (as the s-parameter data indicated). The performance does not reach the intended efficiency and power output goals. The internal interstage waveforms need to be inspected to identify the reason for this shortfall in performance.

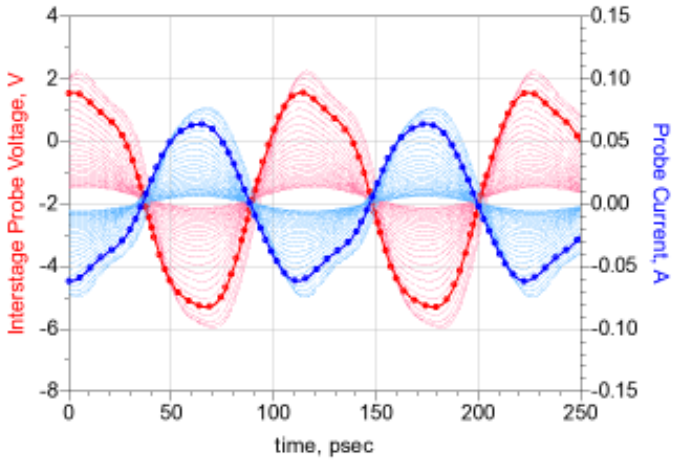
6.5.2.3 Interstage waveform measurements

Using the internal GSG probe point waveform measurements were taken. These were performed under different RF loading conditions, to ensure the measurements were not affected by the additional interaction between the probe and circuit, as was highlighted in section 6.4.2.

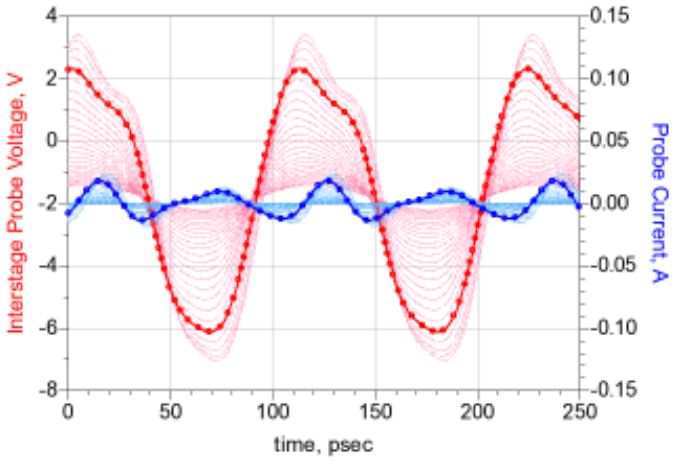
These results are shown in Figure 6.57. The response with the GSG probe set to the system characteristic impedance of 50Ω the gate waveform is seen to have a large amount of probe current suggesting that, although this point is a low impedance part of the circuit, the 50Ω probe impedance is not high enough and some loading occurs.

Setting the load pull system to generate an 'open circuit' fundamental impedance reduces the amount of probe current flowing and the shows the result in Figure 6.57(b). Taking this further with both the fundamental and second harmonic impedances set to open circuit conditions (Figure 6.57(c)) shows little difference in performance and only a small amount of third harmonic probe current flowing.

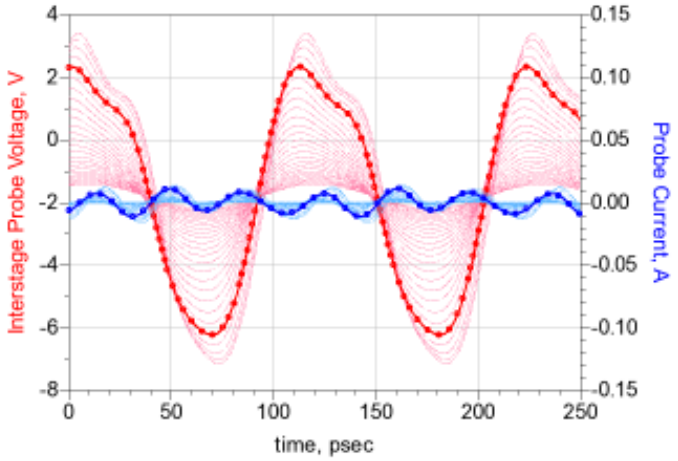
The most important point in this analysis is the fact that although the results show a second harmonic voltage component is evident, the phase relationship between the fundamental and second harmonic is incorrect, with the clipping appearing at the positive peak. This needs to be analysed against the intrinsic voltage waveforms, or the simulated probe point response.



(a) id25743 9GHz, Interstage Waveforms 50Ω probe



(b) id25746 9GHz, Interstage Waveforms f0 O/C



(c) id25775 9GHz, Interstage Waveforms f0, 2f0 O/C

Figure 6.57 Interstage voltage measurements of FXX003GE.1072.C09 (Vg1=-2.2, Vd1=15V, Vg2=-1.8V, Vd2=25V) under different RF loading conditions, (a) Probe at 50Ω, (b) probe fundamental='open circuit' and 2nd harmonic load=50Ω and (c) probe fundamental and second harmonic='open circuit'

Comparing these measurements to the simulated response for the interstage voltage probe point is shown in Figure 6.58. This shows there is clearly a mismatch between the desired response and the measured values.

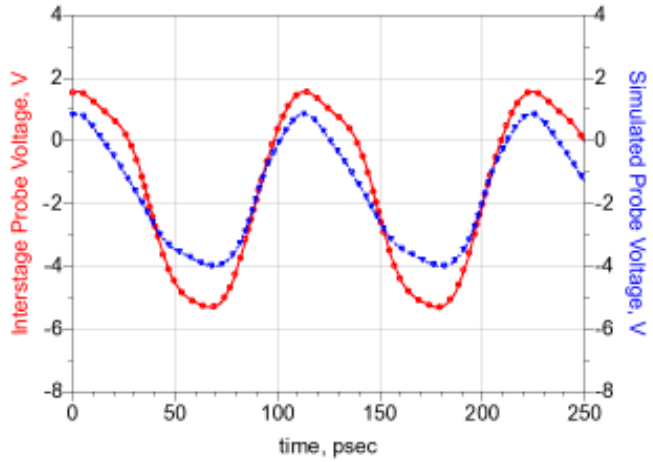


Figure 6.58 Measured (id25743) vs simulated interstage probe point voltage waveforms Showing waveform shape differences (Pin=+18dBm)

Analysing the response to validate the amplitude and phase relationship is shown in Figure 6.59. Here the measured and simulated response at the probe point is compared.

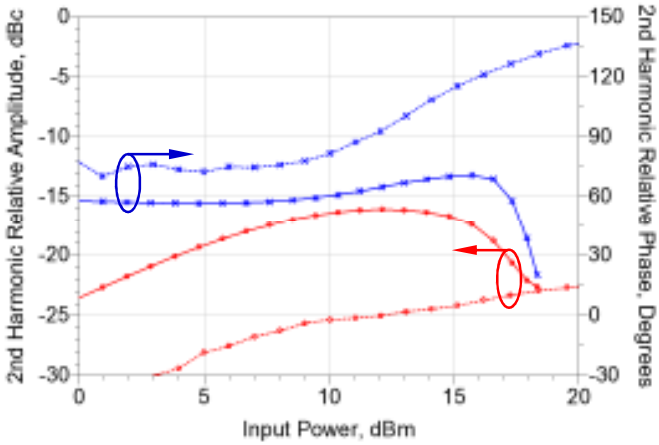


Figure 6.59 Measured response of MMIC (dashed) (dataset id25744) compared to the simulated response (solid) at the interstage probe pad measurement plane.

The amplitude response is different in the two cases, but there is a significant divergence in the phase response at high RF input power drive levels.

6.6 MMIC Circuit Reverse Engineering

The response of the measured amplifier does not align well with the simulated or intended performance. The analysis of the probe point voltages shows that there is a significant difference between the simulations and measurement, especially the phase response. Investigation into the reason for this is required.

There are possible causes that could affect the outcome.

i. The probe point. When the device is probed at the interstage node, the physical probe (unlike a virtual probe in the simulator) may cause coupling which provides an incorrect response. This is an area which has been ignored in the analysis but can be modelled by full 3D EM if required.

ii. The circuit design is fundamentally incorrect.

iii. Errors in the implementation of the amplifier from the schematic to physical translation.

iv. Device model inaccuracies. This is valid for both the passive and active models, however, the active device is the most complex component to characterise and this circuit technique requires specific amplitude and phase relationships with the harmonic components. Any errors here could cause poor performance.

6.6.1 Simulated analysis for the probe point

The initial simulations used a simple linear transmission line model to analyse the interstage waveforms. The impedance of the probe was adjustable using a fixed ideal resistor at the mid-point of the probe pad. It was evident during the simulations that the value of this element had only a small effect on the circuit performance, once above 50Ω.

The probe point was analysed again in more detail using Electromagnetic Simulation tools (ADS® Momentum). The EM layer substrate definition for the GaN25 MMIC process is shown pictorially in Figure 6.60.

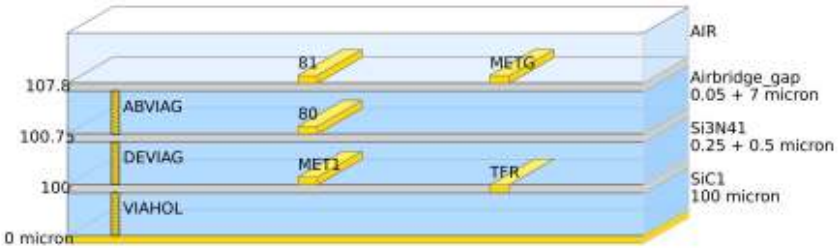


Figure 6.60 Keysight ADS momentum® substrate definition (with dummy layers) for the GaN25 IAF process

The resulting simulation circuit is provided in Figure 6.61 with the probe points for connection between the circuit elements on MMIC and the internal node (port3) where the GSG probe will contact. The results from this were almost identical to the small signal closed form model.

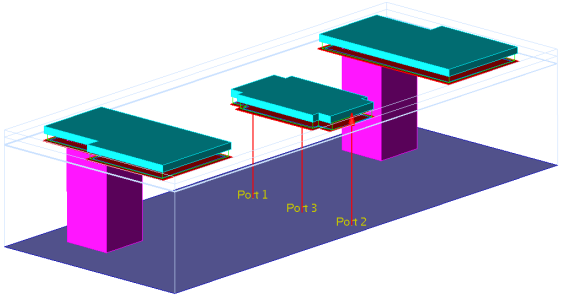


Figure 6.61 Momentum simulation circuit for the interstage probe network

Further analysis of the interstage network elements is required to find the cause of the difference.

6.6.2 Simulated analysis for the Interstage network

Simulations for the individual components (the RC stabilisation network and capacitors) follow a similar pattern to the probe point analysis in that the response between the linear models and the EM simulation results are very close.

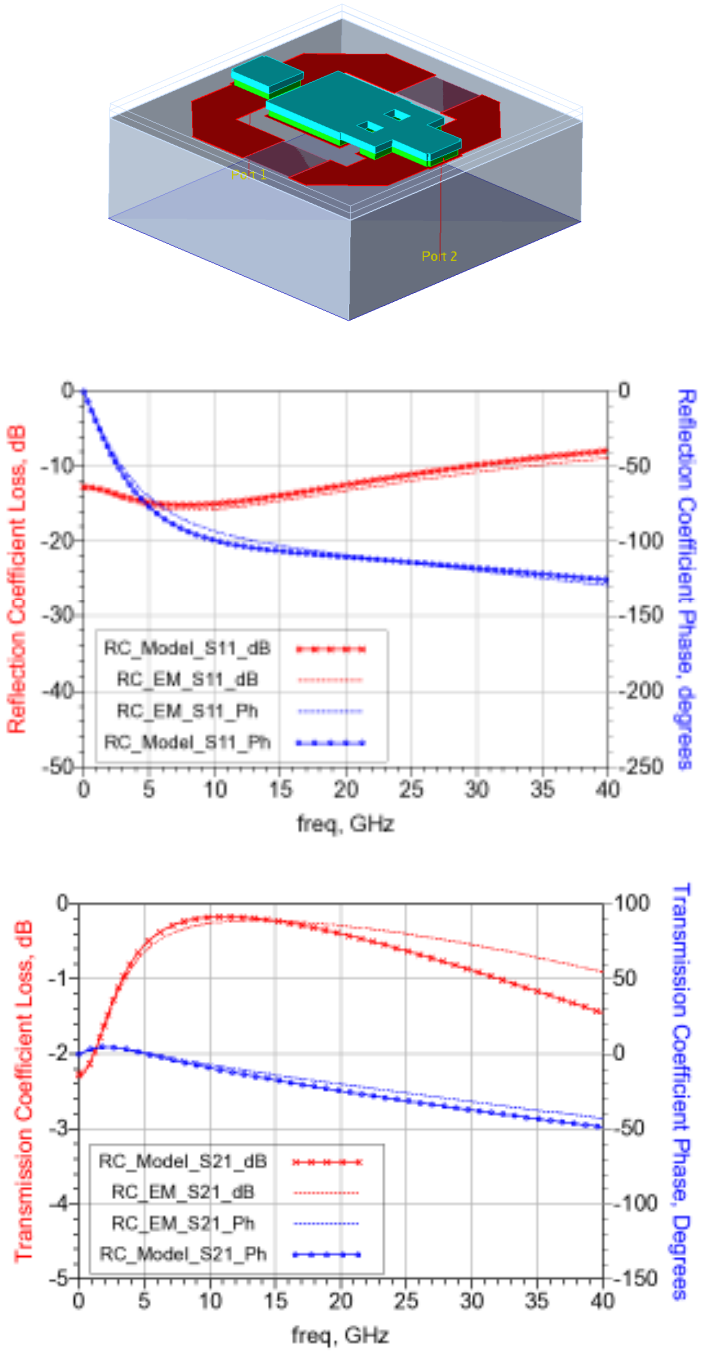


Figure 6.62 Simulation results for the RC network. EM simulation using Keysight ADS® (dashed line) and linear foundry model (symbols)

The capacitor EM circuits and responses are given in Figure 6.63and Figure 6.64, showing the similarity in response to the linear circuit representations.

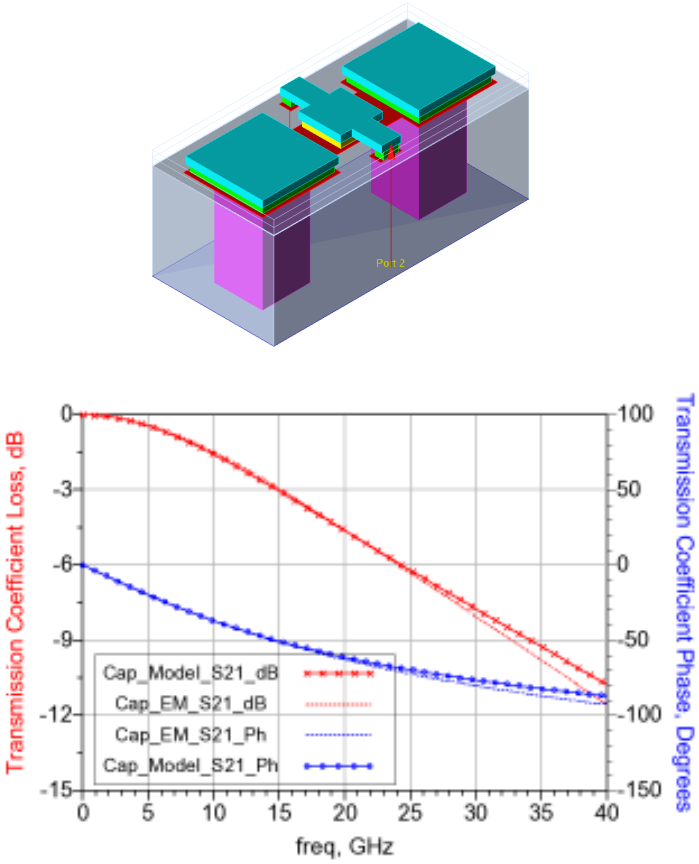


Figure 6.63 Shunt capacitor (40µm x 40µm) model and simulated response. EM simulation using Keysight ADS® (dashed line) and linear foundry model (symbols)

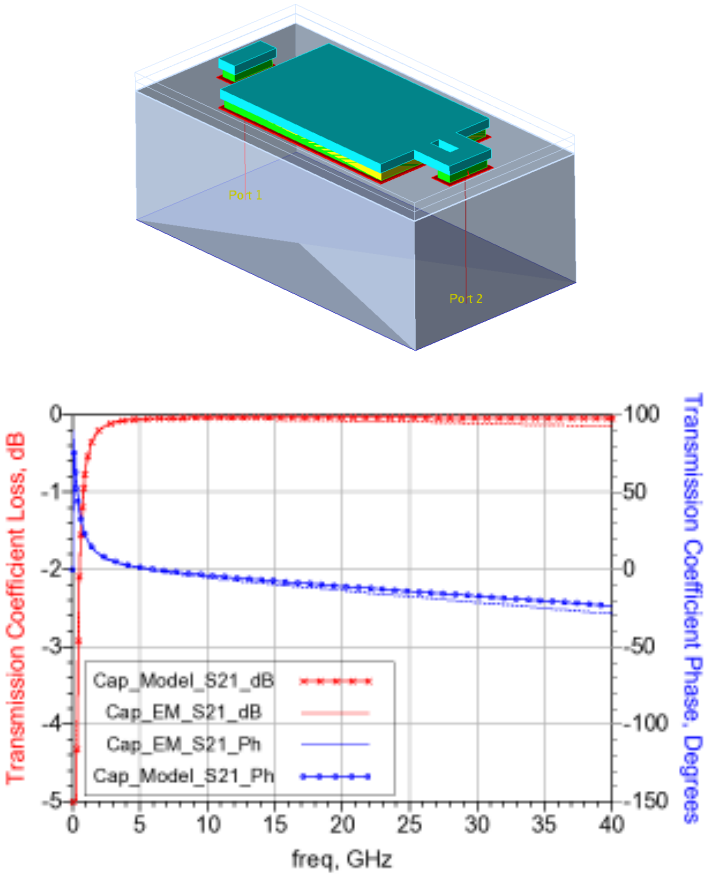


Figure 6.64 Series capacitor (100 µm x 160µm) simulated response. EM simulation using Keysight ADS® (dashed line) and linear foundry model (symbols)

The simulation circuit for the inductors shows significant difference in the transmission (S21) phase between the fundamental and 2nd harmonics. The foundry model seems to have a larger error than expected. A single 1.5 turn inductor deviates from the model as shown in Figure 6.65. This may be the main reason to explain the poor waveform shape noted by the probed measurements.

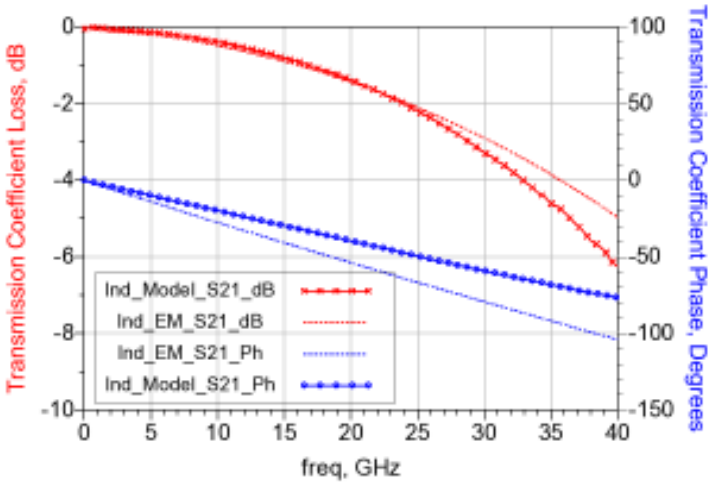


Figure 6.65 Single GaN25 1.5turn spiral inductor simulated results. EM simulation using Keysight ADS® (dashed line) and linear foundry model (symbols)

Cascading the inductors (Figure 6.66) as in the matching network compounds this error. The simulation results of the two 'back-to-back' inductors are shown in Figure 6.67.

These results show that there are significant differences between the linear models and the full 2.5D EM simulations, generally when there are two or more components close to each other.

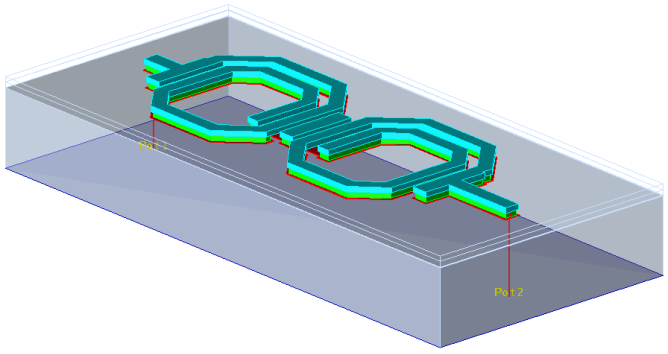


Figure 6.66 EM simulation for reverse engineering the interstage inductor matching network. This considers two back to back spiral inductors.

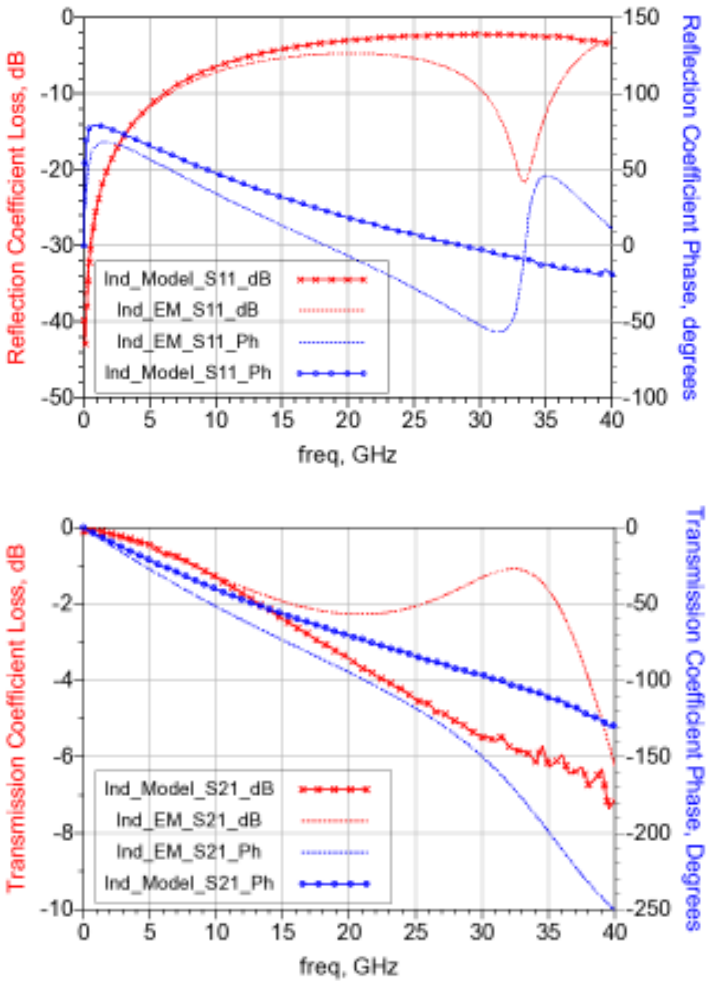


Figure 6.67 Interstage matching network, two series Back to back inductors, simulated results. EM simulation using Keysight ADS® (dashed line) and linear foundry model (symbols)

This is unsurprising in many ways since the component models are extracted from measurements of the components in isolation and the field patterns and modes are in steady state and settled. This is not the case when two structures are move closer together – this assumption breaks down as the fields are still perturbed from the first 'discontinuity' before encountering the second structure.

The full interstage matching network was included in a single EM simulation file and analysed to capture any interactions. This file includes the bias feeds and the drain supply decoupling capacitor to ensure bias related effects are also captured. These results are shown in Figure 6.68.

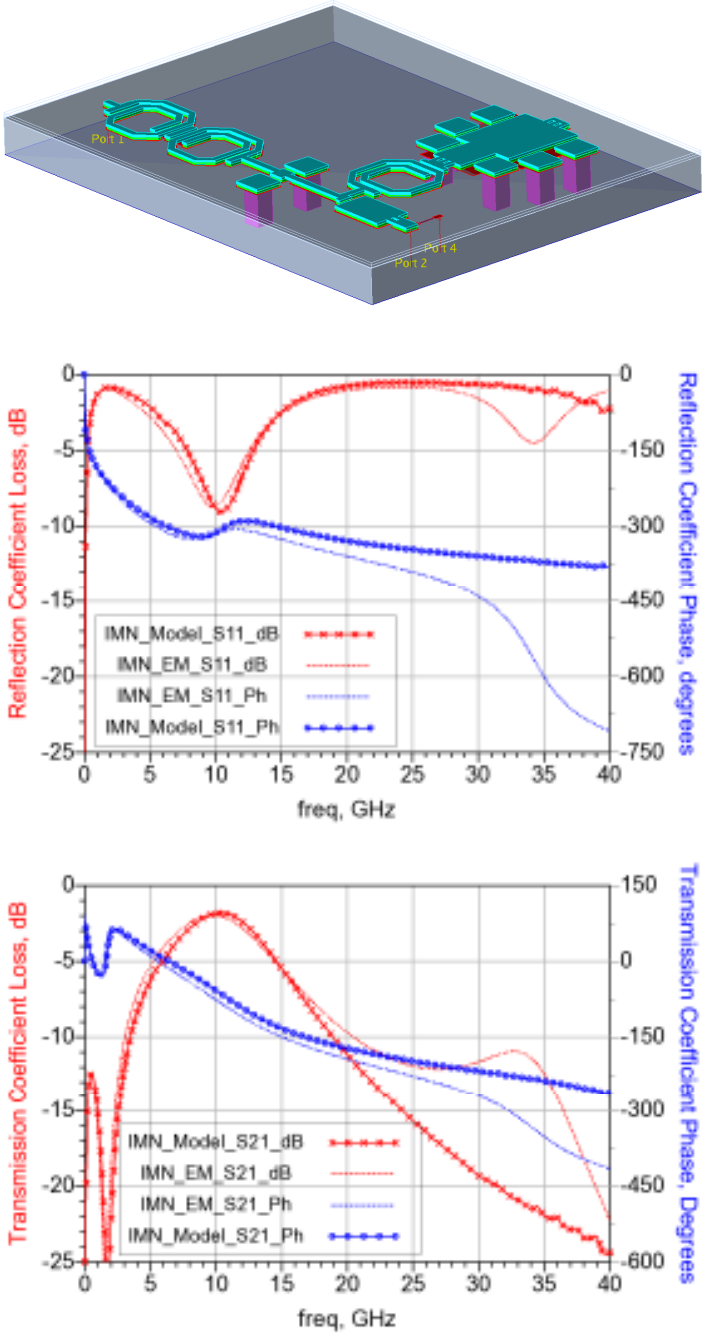


Figure 6.68 Interstage matching network EM model and simulated response. EM simulation using Keysight ADS® Momentum (dashed line) and linear simulation using foundry model (symbols)

Using the EM datasets for the interstage network in the overall simulation circuit the effect of these phase errors can be seen in the response.

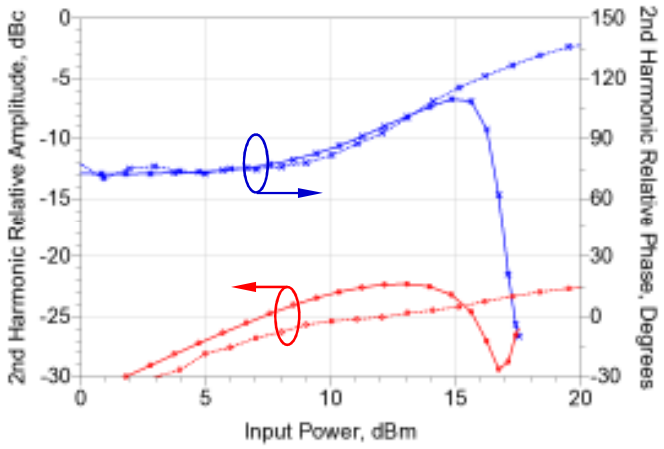


Figure 6.69 Circuit simulation using EM modelled interstage matching network data (solid lines) compared to measured data (dotted lines). The simulations follow the actual measured results closely for low power levels.

The tracking between these reverse engineered simulations and the measurement data is now very close for most of the simulation power range. This points to the implementation of the circuit design being poor, not the underlying theory and operating principle.

However, there is still a significant divergence in the performance at high drive levels, where the model predicts a turn-over in the phase response but this is not seen in the measurement data.

7 CONCLUSIONS AND FURTHER WORK

7.1 Conclusions

The role of waveform engineering has shown significant acceptance and has been adopted more in recent years to improve amplifier efficiency, with the main focus on the output matching conditions. This work has expanded the operating space to include the effects of the input circuit. Key to this 'Waveform Engineering' method is ensuring the results are referred to the intrinsic device plane and so knowledge of the device parasitic elements is required. The standard de-embedding and device modelling approaches have been expanded in this thesis to use new methods in the extraction of these parasitic values to allow determination of the intrinsic waveforms.

A new approach to the design, simulation and optimisation using a direct waveform method has been demonstrated. This is based on using voltage sources to place the optimum waveforms on the device reference planes, and deriving the impedances directly, rather than via load pull techniques. This method, in conjunction with the parasitic element extraction, can be used to inspect the circuit node waveforms directly in the simulator, without the need to post process the results.

The theoretical conditions for PAE improvement by engineering the input waveform have been presented. It has been found that this requires harmonic power injected into the device. This 'Source Injection' mode has been validated with measurements on transistor test cells. These measurements have demonstrated gain is recovered by the addition of the second harmonic content and that there is a limit on this gain recovery due the device input impedance.

This second harmonic injection mode is ideally suited to multistage amplifiers, where the driver stage can deliver the required second harmonic into the power transistor. This harmonic signal is usually present in these amplifiers and this property was used to design a MMIC amplifier in the 'Source Injection' mode.

Novel use of the load pull system to measure interstage waveforms have been used to include probe points in a MMIC design to validate the theoretical postulation.

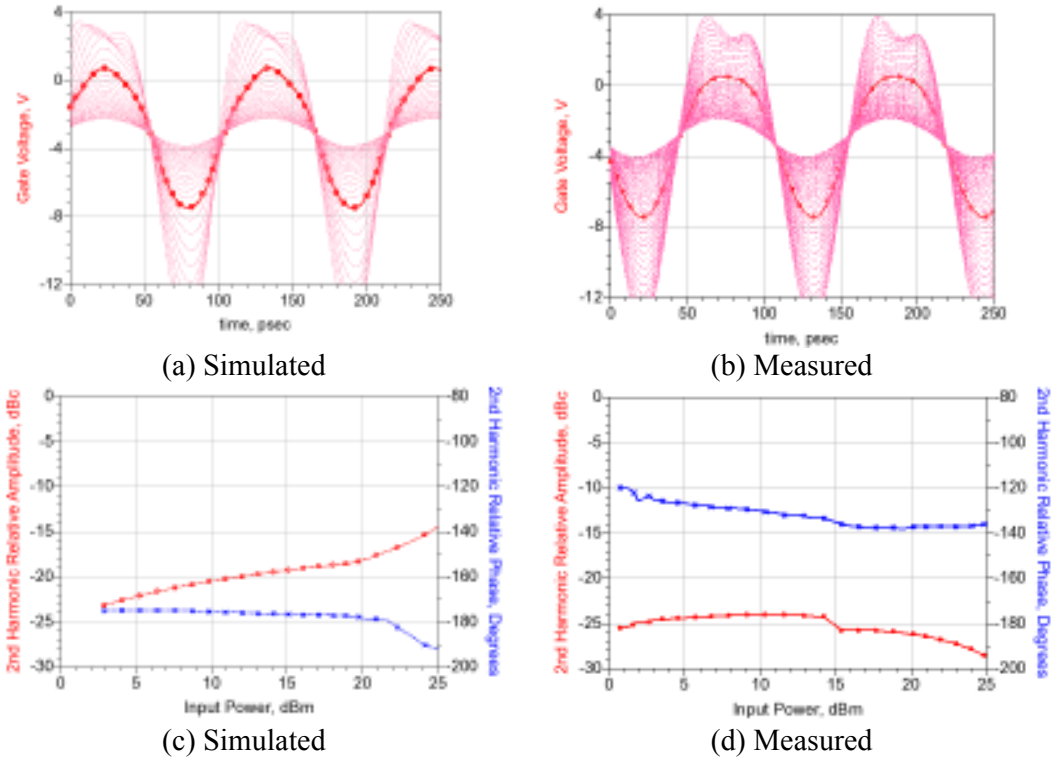
The implementation of the design process was shown to be problematic and the full potential, although demonstrated on individual devices, was not replicated in a two

stage MMIC amplifier. Waveform measurements have confirmed that the source injection mode is not achieved. This is an area for further development.

7.2 Further Work

7.2.1 Modelling approach

The reverse engineering of the MMIC circuit showed a major divergence to the measured performance at high input powers, which significantly impacted the expected circuit performance. The resulting reverse engineering exercise (section 6.6) showed that performance can be modelled successfully at lower power levels but there is a significant deviation between the model and the actual circuit at high drive levels.



(a) Simulated (b) Measured

(c) Simulated (d) Measured

Figure 7.1 Large signal measurement comparison for test cell FX004GE under class B bias point (a) and (b) waveforms, (c) and (d) second harmonic relative amplitude and phase.

Simulations and measurements for the individual transistor test cell, FX004GE, (Figure 6.44) were performed to explore this effect further. The use of this cell is chosen to remove any interactions between the two active devices and focus on the power stage only. The results are shown in Figure 7.1 and show a significant difference between the measured and simulated results, especially in the relative amplitude and phase response,

Figure 7.1(c) and Figure 7.1(d). There is a fixed phase offset of approximately 40° between measurement and simulation across the input power range. Also of note is the simulated dip in phase of the second harmonic under higher drive levels Figure 7.1(c). This is not shown in the measured data, Figure 7.1(d).

The input circuit is not generally the focus on the modelling activities and this may well account for this discrepancy. The compact model validation process does not place much attention on the input circuit response. The bulk of the effort is to align the small signal response to the real transistor measurements and then to verify the large signal output performance by means of load pull measurements

The use of alternative methods for modelling may be helpful in this regard.

7.2.1.1 Poly Harmonic Distortion (PHD) modelling approach

The PHD framework makes use of the principle of harmonic superposition to model a nonlinear system. Similar to S-Parameters, the PHD model describes response waves as the superposition of scaled and delayed incident waves at each of the component ports. However, unlike S-Parameters, the PHD model also maps the impact of incident waves between harmonics. The nonlinear representation of the component is valid at and around a region of the reference state, and can be configured to respond to fundamental and harmonic input signals. In this case the model does not rely on a fit to a circuit representation but it is a direct representation of the circuit black box response and the effects at the input can be captured directly.

X-parameters (from Keysight Technologies) and also the Cardiff model use variations of this approach to create behavioural models which can be used for this application.

The ‘Cardiff model’ uses the frequency domain representations of the measured device plane RF-Waveforms for a selection of loading conditions, and a minimal amount of processing to generate a table that can be imported into CAD software and used in as a model.

X-parameters are a restructuring of the Poly-Harmonic-Distortion model which simplifies the terminology used providing a more commercial framework.

7.2.2 Application of source injection topology

The harmonic source injection methods in the literature and highlighted in this thesis can be summarised in two main classes:

i. Those that include some kind of input duplexing arrangement to allow signal injection (section 1.6.2). This is the main application space in the literature at present.

ii. The use of alternative matching options to create the desired gate waveforms in a multistage amplifier. This was the main focus of the strategy and culminated in the amplifier design is section 6.

There are alternative options in the application for the source injection theory, with one of the most interesting being the use of a balanced amplifier topology [122].

The standard balanced amplifier configuration is shown in Figure 7.2 showing the input port and output port, which present a theoretically ideal input match as the two terminations on the isolated coupler ports, absorb any reflections from the amplifier stages.

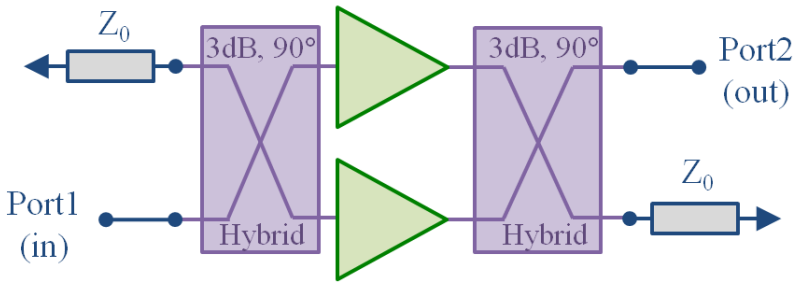


Figure 7.2 The balanced amplifier configuration.

Balanced amplifiers have had a slight resurgence lately where the quadrature coupler isolated port, generally terminated in the system characteristic impedance Z_0, is actually used to provide a convenient point to inject signals into the amplifier network. This method has been used to provide separation between receive and transmit paths of Transmit-Receive modules [124] and, more recently, has been exploited for amplifier efficiency improvement with output injection by Shepphard et al [125] with the 'Load Modulated Balanced Amplifier' showing improved performance at significant power back-off.

A similar approach can be considered for the second harmonic source injection amplifier concept, where the input quadrature coupler isolated port is used to inject the second harmonic component (Figure 7.3), which can come from either the fundamental path or from a separate signal source depending on application.

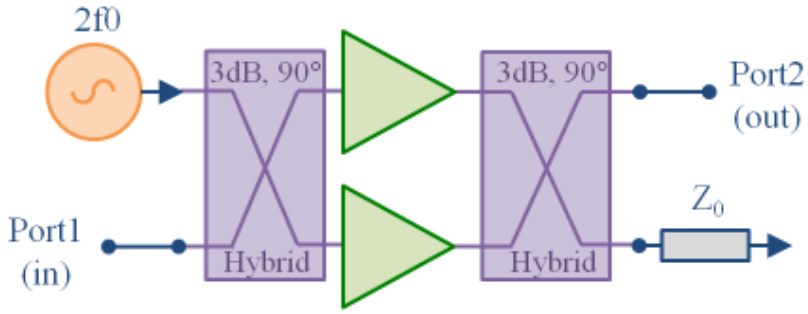


Figure 7.3 Balanced amplifier configured for harmonic injection.

Analysis of a balanced amplifier for the purposes of 2nd H source injection shows that injecting via the isolated port does not have the correct phase response for each of the amplifiers.

Figure 7.4 shows the simulation schematic of the balanced amplifier architecture (using Lange couplers) with 2nd harmonic injection into the isolated input port.

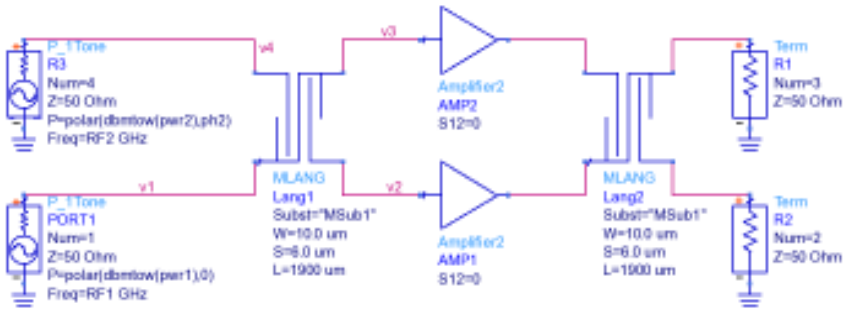


Figure 7.4 Balanced amplifier configuration with 2nd harmonic injection

The response of this circuit is shown in Figure 7.5, after normalising for the intrinsic phase shift through the network which, was not included in the basic formulation of the hybrid analysis.

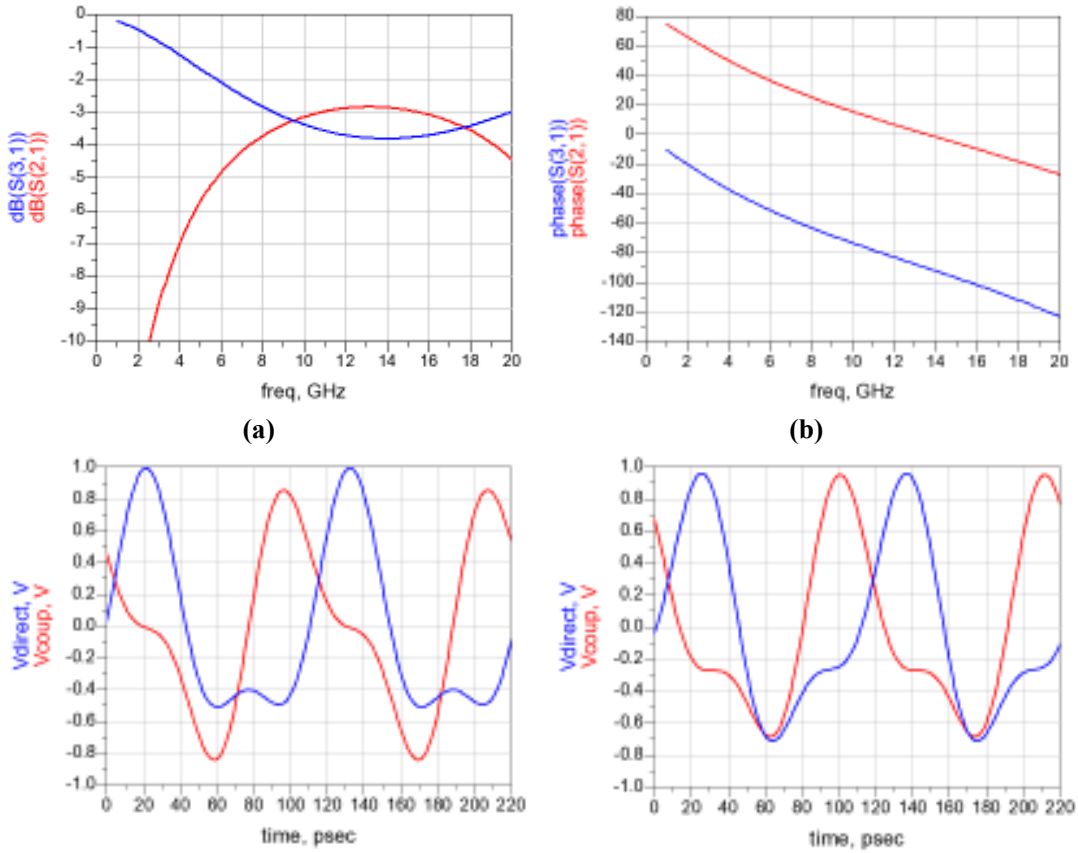


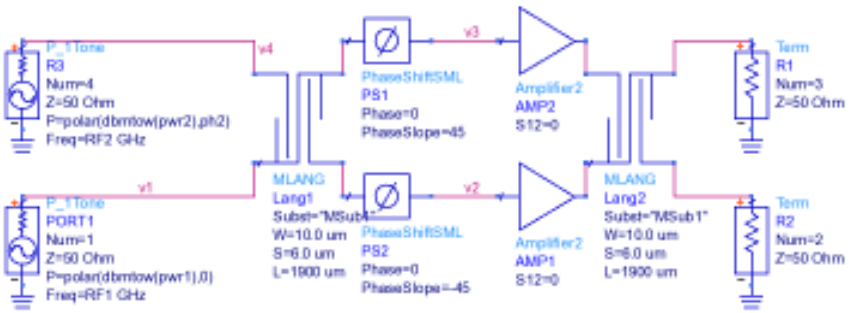
Figure 7.5 Balanced amplifier source injection circuit simulation results (a) Lange coupler amplitude response, (b) Lange coupler phase response (c) and (d) voltage waveforms into ideal 50Ohm input amplifier impedance with second harmonic phse shift. Fund power=+10dBm, 2ndH -7dBc.

Figure 7.5(a) and (b) shows the simulated response of a GaAs MMIC Lange coupler. The waveforms available when injecting in both input ports of a Lange as per the architecture are shown in Figure 7.5(c) aligning the phase for the direct arm. This however shows the input into the coupled amplifier is now not correct due to the 90° split in the Lange coupler.

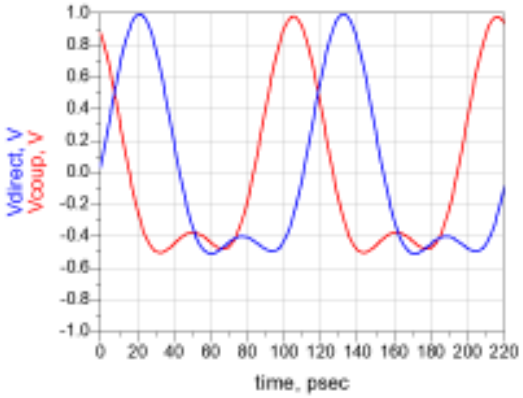
Optimising the 2nd harmonic relative phase to get a better response between the two arms of the balanced amplifier shows ideally a 135° (3π/4) is the best compromise (adjusted here to 195° to account for the 60° differential phase shift of the practical Lange implementation). The response is shown in Figure 7.5(d).

This is not optimum for either amplifier and really the arms would need an additional phase shift of +45° and -45° for arms 1 and 2 respectively – without affecting the fundamental phase shifts (or a single 90 shift in one of the arms – but again with a

0° differential shift at the fundamental.) Figure 7.6 shows the schematic and response of this architecture.



(a) Schematic with additional phase shifts



(b) ϕv_2= -45° and ϕv_3= +45°

Figure 7.6 Balanced amplifier schematic and input voltage waveforms with source injection. (Fund power=+10dBm, 2ndH -7dBc, ϕ2=195)

These results show that this approach is possible, but careful consideration of the additional circuit complexity and benefits need to be undertaken. This is however a useful additional architecture worthy of further research.

7.2.3 Waveform Engineering for improved robustness and reliability

The work presented so far in this thesis has concentrated on injection of the second harmonic signal to improve the amplifier performance with a negatively clipped sinewave to reduce the conduction angle in PAs whilst maintaining power gain. Other applications of this technique are possible by utilising the clipped sinewave positive peaks.

Robust LNA configurations in the literature are limited mainly to GaN technology and the improved survivability is generally attributed to the wide bandgap material properties rather than any circuit techniques [126] - [130]. Chen [131] shows a study of InP and GaAs devices where the HEMT device size and matching can make a difference to the survivability. The notable exceptions to this are the papers by Rudolph et. al. [131][132][133] who state the failure mechanism in GaN devices is due to forward gate current rather than voltage breakdown effects, and thus an improvement in survivability is possible by the use of dc feedback in the gate bias circuit. This dc feedback trades gate forward current for lower (more negative) gate bias voltage as the power increases. This is possible as there is significant headroom between the bias voltage and the device breakdown limits.

This forward gate current limit can also be a failure mechanism for the input power overload in GaAs power processes (e.g the FD30 pHEMT process) where high breakdown voltages are maintained.

In low noise amplifier applications the forward gate current can be problematic for reliability under large signal drive. Clipping the positive peaks of the input waveform can reduce the forward current and improve reliability, although care needs to be taken so that the negative peak (which increases under this method) does not enter the voltage breakdown region.

The use of series feedback in the transistor source terminal is a standard circuit technique and can improve power handling and flatten gain. This is generally a frequency independent network. In LNA design the use of inductive feedback is used to improve the input match and optimum noise point. Using this technique to provide second harmonic feedback can provide the injection point to allow clipping of positive peaks.

The networks in Figure 7.7 show the implementation of these source feedback circuits, with the simulated responses given in Figure 7.8.

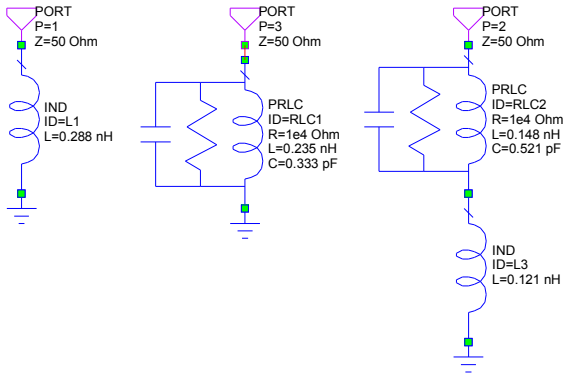


Figure 7.7 Source feedback configurations (a) inductive, reference state for low noise design, (b) parallel resonant circuit and (c) LC-L network controlling 3 harmonics.

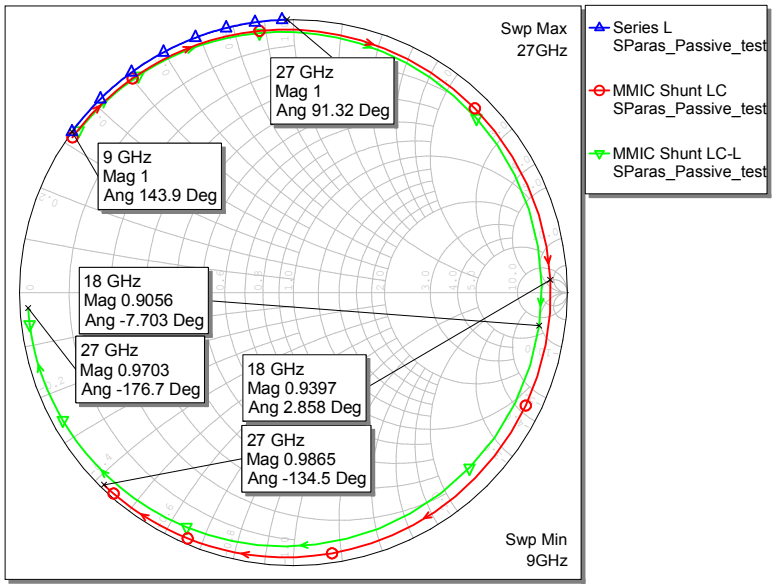


Figure 7.8 Simulated responses for the series feedback networks in figure, using MMIC components. The impedance at the signal fundamental frequency is constant for all cases.

The networks show the same (inductive) impedance at the 9GHz fundamental frequency, chosen to be the optimum value for low noise operation. The response shows a high impedance for the second harmonic, leading to the correct phasing for clipped sinewave operation.

The waveforms at the gate-source nodes are shown in Figure 7.9. The input drive level is sinusoidal and the source voltage shows a large second harmonic content resulting in the correct Vgs clipped sinewave drive.

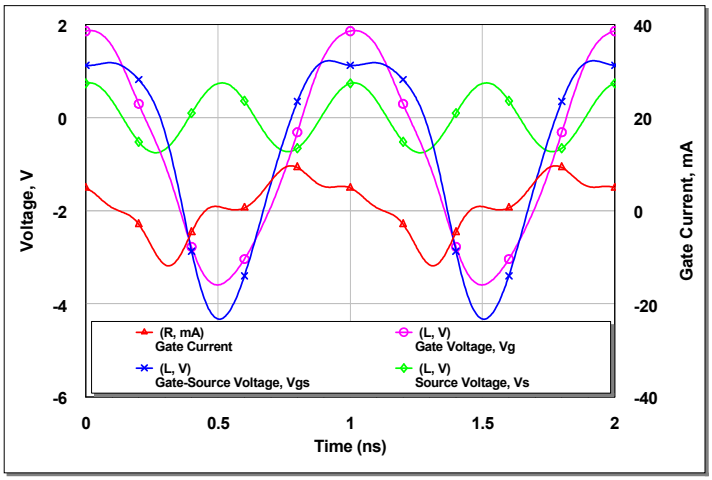


Figure 7.9 Simulated waveforms for a 4x75 FD30 pHEMT using LC-L harmonic series feedback network at 1GHz.

Using this approach in an amplifier circuit has been simulated and the circuit responses are given in Figure 7.10. The raw amplifier performance is shown to be almost identical at the fundamental in all three cases. A reference source grounded version is shown as a comparison.

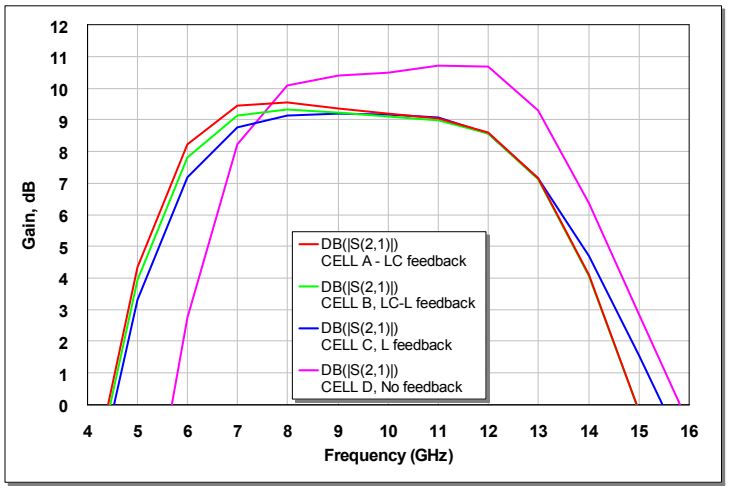


Figure 7.10 MMIC amplifier simulated small signal gain using series-source feedback.

These designs have been simulated under large signal drive to monitor the dc gate current. The results in Figure 7.11shows the benefit of the clipped sinewave drive allowing a 4dB larger input signal for the same gate current.

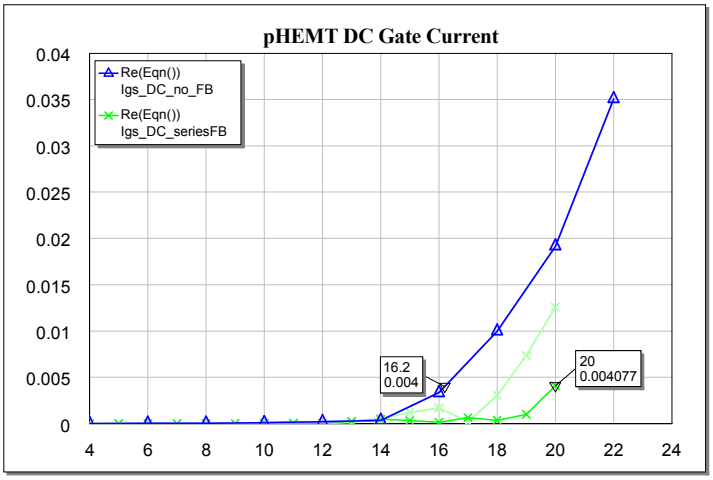
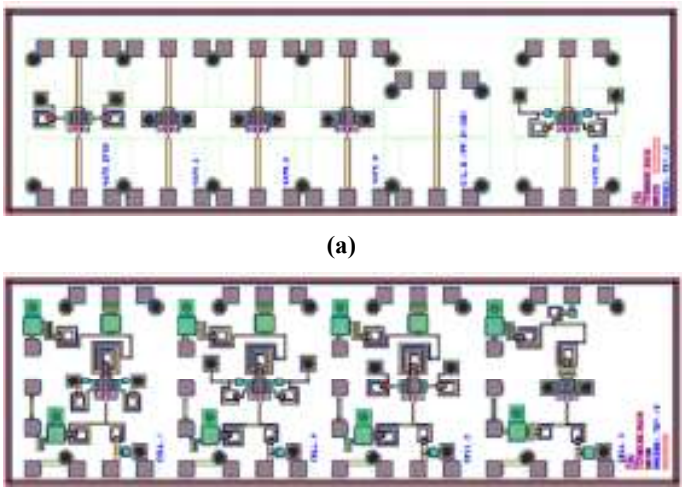


Figure 7.11 MMIC LNA dc gate current simulation results for Series feedback (a) no feedback (blue), (b)LC feedback (light green), (c)LC-L feedback (bold green)

Layouts for the proposed test cells and amplifier circuits are shown in Figure 7.12. The amplifiers have identical input and output matching networks, and the only difference is the source feedback elements.



(a)

(b)

Figure 7.12 MMIC implementation of proposed Robust LNA circuits (a) Transistor test cells with series feedback only and (b) MMIC amplifier designs.

7.2.4 Interstage voltage measurement

The methods outlined in section 6.4 show that the interstage voltage can be measured without loading the circuit by the use of active load pull systems, configured to provide high impedance at the fundamental and harmonic signal frequencies. The methods to perform this function without impacting the circuit function or chip area need assessing to expand this approach in practical amplifier MMIC designs.

The increasing use of novel hybrid circuit assemblies for PA design [134] allow access to these interstage node more readily as the circuits naturally have GSG bond pads in the design at the MMIC chip edges (Figure 7.13). Interestingly this can also open up the possibility of using the E-field probe approach and the bond wire interconnection point, if the probe bandwidth and sensitivity limitations are addressed.

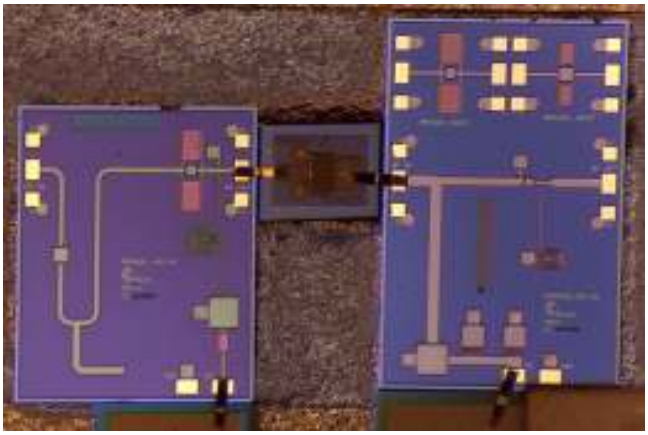


Figure 7.13 GaAs/GaN hybrid HPA test circuit using GaAs input and output passive matching networks around the discrete GaN transistor [133]. MMIC probe/interconnection points are clearly identified.

7.2.5 Expanding the operating voltage space

The measurements of the transistor test cells under source injection mode showed a 2.5 V reduction in the gate-source negative swing, which coincides with the peak drain voltage (Figure 5.35). This can be beneficial for reliability considerations, where the gate-drain voltage breakdown is a failure mechanism, as there is a reduced applied gate-drain voltage. Alternatively, keeping the gate-drain voltage constant under this operating mode may allow the drain bias voltage to be increased to provide for an increase in RF output power.

7.2.6 Summary

This thesis has outlined the theory and operation of conventional microwave amplifier classes. It has identified the role waveform engineering has played in the improvement of efficiency in these amplifiers and discussed the factors which affect the efficiency in relation to these reduced conduction angle classes.

The importance of the intrinsic nodes in defining the operating modes was presented along with methods to extract parasitic elements for modelling and de-embedding of measurements.

A new approach to the design, simulation and optimisation using a direct waveform method has been demonstrated. This is based on using voltage sources to force the optimum waveforms on the device reference planes, and deriving the impedances directly, rather than via load pull techniques. This method, in conjunction with the parasitic element extraction, can be used to inspect the circuit node waveforms directly in the simulator, without the need to post process the results.

These simulation techniques have been used in conjunction with the theory for the input waveform engineering to define an amplifier design strategy for a second harmonic source injection operating mode. This was demonstrated the realisation of a two stage GaN MMIC amplifier.

The performance of the amplifier was not optimum and the results were analysed and the importance of the models in utilising this mode of operation was demonstrated.

The application space using source injected second harmonic for other applications has been presented, using balanced amplifier topologies and to improve RF robustness of LNAs.

8 APPENDICES

8.1 Appendix A

Approximation of the clipped sinewave drive can be made with a fundamental sinewave and second harmonic component with the correct relative phase relationship to the fundamental. The expression (A1) can be used to describe this system.

$$Vgs(\theta) = A\{\cos\theta + K.\cos(2\theta + \phi) + C\} \qquad \text{A1}$$

Solving at the boundary conditions Vgs(0) = 1, the constant (or dc voltage) is found as C=(1–A–AK)

$$Vgs(\theta) = A\cos\theta + AK\cos 2\theta + (1 - A - AK) \qquad \text{A2}$$

Where A is the fundamental signal amplitude and K is the relative second harmonic amplitude. This equation defines a normalised waveform, with the Vgs maximum at unity and the pinch-off at zero. To describe real transistor behaviour it needs to be scaled upto the maximum voltage permissible on the gate, Vgs_{max}, and down to the pinch-off voltage, Vp, for the process.

$$Vgs(\theta) = (Vgs_{\max} - Vp)\{A\cos\theta + AK\cos 2\theta + (1 - A - AK)\} + Vp \qquad \text{A3}$$

The Drain current for a transistor driven with a Vgs signal of the form shown in Eqn A3 is then given by:

$$ids(\theta) = I_{\max}\{A\cos\theta + AK\cos 2\theta + (1 - A - AK)\} \quad \text{for} \quad \frac{-\alpha}{2} < \theta < \frac{+\alpha}{2} \qquad \text{A4(a)}$$

$$ids(\theta) = 0 \qquad \text{elsewhere} \qquad \text{A4(b)}$$

Where $\alpha/2$ is the conduction angle and is symmetric about the y-axis.

Using Fourier analysis, the dc level and fundamental of ids(θ) can be calculated. Noting that the waveform is an even function, only a_n terms are present and defined as:

$$a_0 = \frac{2I_{\max}}{\pi}\int_0^{\alpha/2}\{A\cos\theta + AK\cos 2\theta + (1 - A - AK)\}d\theta \qquad \text{A5}$$

And the dc term is related to a_0:

$$dc = \frac{a_0}{2} = \frac{I_{\max}}{\pi}\int_0^{\alpha/2}\{A\cos\theta + AK\cos 2\theta + (1-A-AK)\}d\theta \qquad \text{A6}$$

$$dc = \frac{I_{\max}}{2\pi}\left\{\left[A\sin\theta\right]_0^{\alpha/2} + \left[\frac{AK}{2}\sin(2\theta+\phi)\right]_0^{\alpha/2} + \left[(1-A-AK)\theta\right]_0^{\alpha/2}\right\} \qquad \text{A7}$$

$$dc = \frac{I_{\max}}{\pi}\left\{A(\sin\alpha/2) + \frac{AK}{2}\sin\alpha + \frac{(\alpha - \alpha A - \alpha AK))}{2}\right\} \qquad \text{A8}$$

The fundamental component of current is defined by the a1 term:

$$a_1 = \frac{2I_{\max}}{\pi}\int_0^{\alpha/2}\{A\cos\theta + AK\cos 2\theta + (1-A-AK)\}\cos\theta d\theta \qquad \text{A9}$$

$$a_1 = \frac{2I_{\max}}{\pi}\int_0^{\alpha/2} A\cos^2\theta + AK\cos 2\theta\cos\theta + (1-A-AK)\cos\theta d\theta \qquad \text{A10}$$

$$a_1 = \frac{2I_{\max}}{\pi}\left\{\begin{array}{l}\left[\frac{A\theta}{2}\right]_0^{\alpha/2} + \left[\frac{A}{4}\sin 2\theta\right]_0^{\alpha/2} + \left[\frac{AK}{6}\sin 3\theta\right]_0^{\alpha/2} \\ \qquad + \left[\frac{AK}{2}\sin\theta\right]_0^{\alpha/2} + \left[(1-A-AK)\sin\theta\right]_0^{\alpha/2}\end{array}\right\} \qquad \text{A11}$$

$$a_1 = \frac{I_{\max}}{\pi}\left\{\frac{A\alpha}{2} + \frac{A}{2}\sin\alpha + AK\sin\left(\frac{3\alpha}{2}\right) + (2-2A-AK)\sin\alpha/2\right\} \qquad \text{A12}$$

Further calculations require the knowledge of the conduction angle, α, which can be found by setting A4(a) equal to zero.

$$ids(\theta) = I_{\max}\{A\cos\theta + AK\cos 2\theta + (1-A-AK)\} = 0 \qquad \text{A13(a)}$$

$$A\cos\theta + AK\cos 2\theta + (1-A-AK) = 0 \qquad \text{A13(b)}$$

$$A\cos\theta + AK(2\cos^2\theta - 1) + (1-A-AK)\} = 0 \qquad \text{A13(c)}$$

$$2AK\cos^2\theta + A\cos\theta + (1-A-2AK) = 0 \qquad \text{A13(d)}$$

This expression, A13(d) is a quadratic in cosθ and can be solved as

$$\cos\theta = \frac{-1 \pm \sqrt{(4K+1)^2 - 8\left(\frac{K}{A}\right)}}{4K} \qquad \text{A14}$$

The zero crossings are defined at an angle α/2

$$\cos(\alpha/2) = \frac{-1 \pm \sqrt{(4K+1)^2 - 8\left(\frac{K}{A}\right)}}{4K} \qquad \text{A15}$$

$$(\alpha/2) = \cos^{-1}\left[\frac{-1 \pm \sqrt{(4K+1)^2 - 8\left(\frac{K}{A}\right)}}{4K}\right] \qquad \text{A16}$$

Investigating the waveforms more generally and including a phase offset term, the waveform is modified as:

$$ids(\theta) = I_{max}\{A\cos(\theta) + AK\cos(2\theta+\phi) + (1-A-AK)\} \quad \text{for} \quad \alpha_n < \theta < \alpha_p \qquad \text{A17(a)}$$

$$ids(\theta) = 0 \qquad \text{elsewhere} \qquad \text{A17(b)}$$

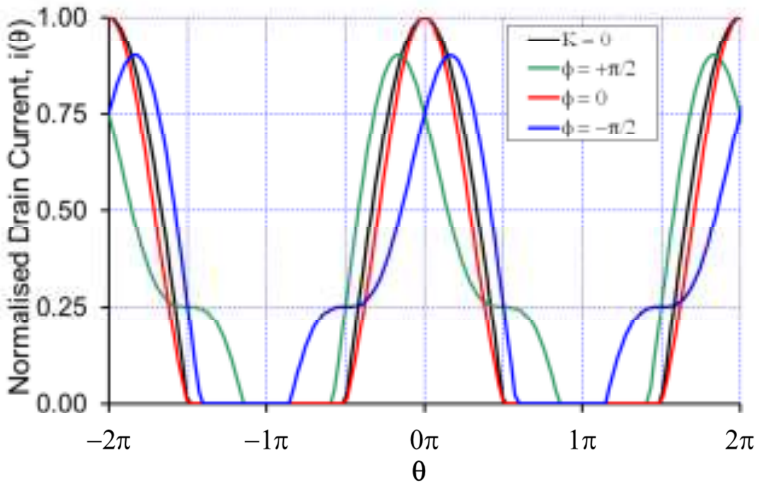


Figure A1: Drain current waveforms of the form equation A17. Fixed amplitude A=0.5 and K=0.5 and ϕ=-90° to +90°. Plotted also in black is the standard cos(θ) current.

The waveforms in Figure A1 show that the function is no longer even (the zero crossings each side of zero angle are different) and thus the harmonic components will be comprised of both sine and cosine terms.

The corresponding Fourier terms are given by:

$$dc = \frac{a_0}{2} = \frac{I_{\max}}{\pi}\int_{\alpha_n}^{\alpha_p}\{A\cos\theta + AK\cos(2\theta+\phi) + (1-A-AK)\}d\theta \qquad \text{A18}$$

$$dc = \frac{I_{\max}}{2\pi}\left\{\left[A\sin\theta\right]_{\alpha_n}^{\alpha_p} + \left[\frac{AK}{2}\sin(2\theta+\phi)\right]_{\alpha_n}^{\alpha_p} + \left[(1-A-AK)\theta\right]_{\alpha_n}^{\alpha_p}\right\} \qquad \text{A19}$$

$$dc = \frac{I_{\max}}{2\pi}\left\{\begin{array}{r} A(\sin\alpha_p - \sin\alpha_n) + \frac{AK}{2}(\sin(2\alpha_p+\phi) \\ -\sin(2\alpha_n+\phi)) + (1-A-AK)(\alpha_p-\alpha_n)\end{array}\right\} \qquad \text{A20}$$

And the fundamental component is now given by both a1 and b1 terms:

$$a_1 = \frac{I_{\max}}{\pi}\int_{\alpha_n}^{\alpha_p}\{A\cos\theta + AK\cos(2\theta+\phi) + (1-A-AK)\}\cos\theta.d\theta \qquad \text{A21}$$

$$b_1 = \frac{I_{\max}}{\pi}\int_{\alpha_n}^{\alpha_p}\{A\cos\theta + AK\cos(2\theta+\phi) + (1-A-AK)\}\sin\theta.d\theta \qquad \text{A22}$$

The a1 and b1 terms need to be expanded and trig identities used to get these in an easily integrateable form:

$$a_1 = \frac{I_{\max}}{\pi}\int_{\alpha_n}^{\alpha_p} A\cos^2\theta + AK\cos\theta\cos(2\theta+\phi) + (1-A-AK)\cos\theta.d\theta \qquad \text{A23}$$

$$a_1 = \frac{I_{\max}}{\pi}\int_{\alpha_n}^{\alpha_p}\frac{A}{2}(1+\cos 2\theta) + \frac{AK}{2}(\cos(3\theta+\phi)+\cos(\theta+\phi)) + (1-A-AK)\cos\theta.d\theta \qquad \text{A24}$$

$$a_1 = \frac{I_{\max}}{\pi}\left\{\left[\frac{A\theta}{2}\right]_{\alpha_n}^{\alpha_p} + \left[\frac{A}{4}\sin 2\theta\right]_{\alpha_n}^{\alpha_p} + \left[\frac{AK}{6}\sin(3\theta+\phi)\right]_{\alpha_n}^{\alpha_p} + \left[\frac{AK}{2}\sin(\theta+\phi)\right]_{\alpha_n}^{\alpha_p} + \left[(1-A-AK)\theta\right]_{\alpha_n}^{\alpha_p}\right\} \qquad \text{A25}$$

$$a_1 = \frac{I_{\max}}{\pi}\left\{\begin{array}{l}\frac{A}{4}(\alpha_p - \alpha_n) + \frac{A}{4}(\sin 2\alpha_p - \sin 2\alpha_n) \\ \quad + \frac{AK}{6}(\sin(3\alpha_p + \phi) - \sin(3\alpha_n + \phi)) + \frac{AK}{2}(\sin(\alpha_p + \phi) \\ \qquad - \sin(\alpha_n + \phi)) + (1 - A - AK)(\alpha_p + \alpha_n)\end{array}\right\} \quad \text{A26}$$

And similarly:

$$b_1 = \frac{I_{\max}}{\pi}\int_{\alpha_n}^{\alpha_p} A\sin\theta\cos\theta + AK\sin\theta\cos(2\theta+\phi) + (1 - A - AK)\sin\theta.d\theta \quad \text{A27}$$

$$b_1 = \frac{I_{\max}}{\pi}\int_{\alpha_n}^{\alpha_p} \frac{A}{2}\sin 2\theta + \frac{AK}{2}(\sin(3\theta+\phi) - \sin(\theta+\phi)) + (1 - A - AK)\sin\theta.d\theta \quad \text{A28}$$

$$b_1 = \frac{I_{\max}}{\pi}\left\{-\left[\frac{A}{4}\cos 2\theta\right]_{\alpha_n}^{\alpha_p} - \left[\frac{AK}{6}\cos(3\theta+\phi)\right]_{\alpha_n}^{\alpha_p} + \left[\frac{AK}{2}\cos(\theta+\phi)\right]_{\alpha_n}^{\alpha_p} - \left[(1 - A - AK)\cos\theta\right]_{\alpha_n}^{\alpha_p}\right\} \quad \text{A29}$$

$$b_1 = \frac{I_{\max}}{\pi}\left\{-\frac{A}{4}(\cos 2\alpha_p - \cos 2\alpha_n) - \frac{AK}{6}(\cos(3\alpha_p+\phi) - \cos(3\alpha_n+\phi)) + \frac{AK}{2}(\cos(\alpha_p+\phi) - \cos(\alpha_n+\phi)) - (1 - A - AK)(\cos\alpha_p + \cos\alpha_n)\right\} \quad \text{A30}$$

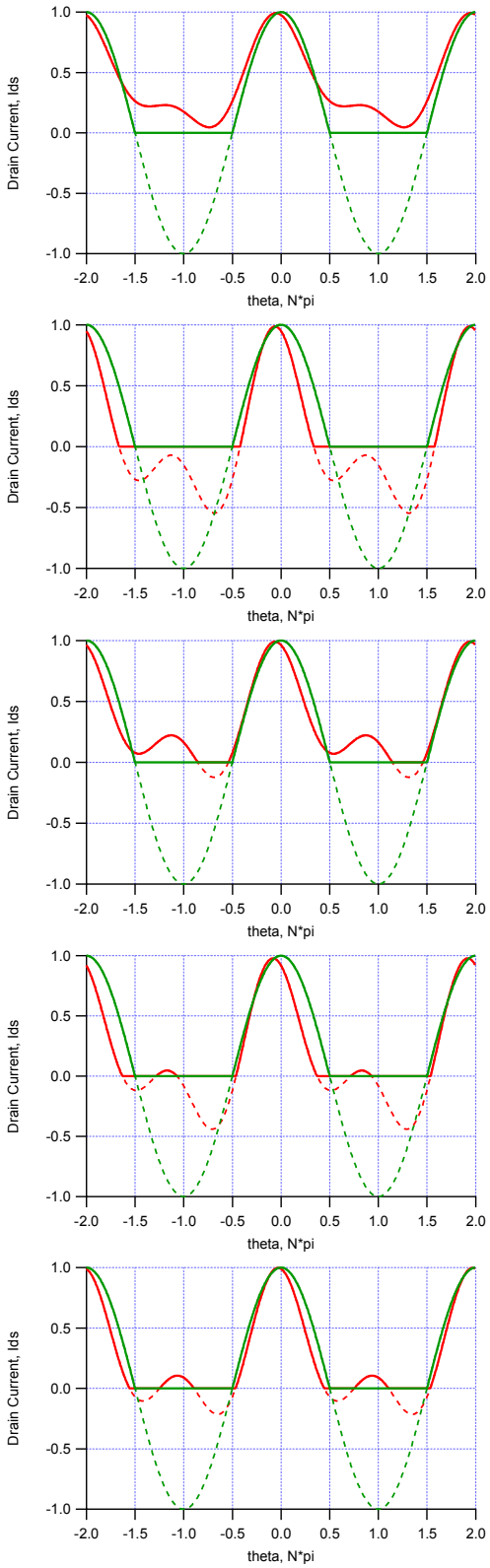
In order for these expressions to be solved, the zero crossing angles α_p and α_n need to be identified to set the integration limits. However, this is now no longer a simple quadratic equation and numerical techniques are required to find the zero crossing angles. The situation is also more complex as this waveform can also have up to 4 zero crossings in any -π to +π period. This complicates the analysis, unless the component amplitudes, A and K and phase offset, ϕ are constrained.

(1) zero crossings –π to α1, α2 to α3, α4 to +π

(2) zero crossings α1 to α2, α3 to α4

(3) zero crossings α1 to α2, α3 to α4

(4) zero crossings α1 to α2



(a) Case1 N=0, phi=30, A=0.4, K=0.45

Range
No Zero crossings

(b)Case2a N=2, phi=30, A=0.55, K=0.7

Range
α_1 to α_2

Case2b N=2, phi=30, A=0.4, K=0.7

Range
$-\pi$ to α_1
α_2 to $+\pi$

Case3a N=4, phi=45, A=0.5, K=0.7

Range
α_1 to α_2
α_3 to α_4

Case3b N=4, phi=15, A=0.45, K=0.7

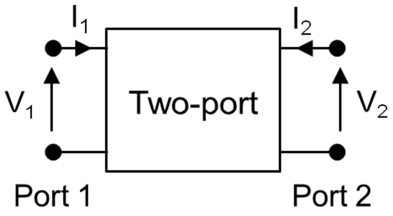
Range
$-\pi$ to α_1
α_2 to α_3
α_4 to $+\pi$

Figure A2 Possible Drain current waveforms created using A5(a)

8.2 Appendix B

Derivation of the optimum input network series resistor for transistor stabilisation.

Consider a two-port network as shown in figure B.1.



(a)

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

(b)

Figure B1 Two port definition (a) schematic and (b) Z-parameter description

Rollett [111] defined a stability factor K for the two-port network, and, although this is generally presented in terms of s-parameters, it is in fact valid for any two-port representation. Defining K using the Z parameter set, which is more suited to series configured circuits.

$$K = \frac{2\,\mathrm{Re}(Z_{11})\,\mathrm{Re}(Z_{22}) - \mathrm{Re}(Z_{12}Z_{21})}{\left|Z_{12}Z_{21}\right|} \qquad \text{B1}$$

The value of K must be greater than 1 for unconditional stability if $\mathrm{Re}(Z_{11})$ and $\mathrm{Re}(Z_{22})$ are positive.

If external impedances are added to the two-port they can be considered as part of the network for the stability criteria. Now the expression for K can be rewritten as:

$$K = \frac{2(\mathrm{Re}(Z_{11}) + R_1)(\mathrm{Re}(Z_{22}) + R_2) - \mathrm{Re}(Z_{12}Z_{21})}{\left|Z_{12}Z_{21}\right|} \qquad \text{B2}$$

Where R_1 and R_2 are the real parts of the impedances added at ports 1 and 2 respectively.

In general, using resistor at port 2 for a power amplifier would not be considered due to the power dissipation problems and the resulting delivery of power to the rest of the system. Similarly, the use of a resistor at the input would not be used for a low noise amplifier (LNA) due to the detrimental effect on the noise figure [122].

Considering only a series resistance, R_1 at the input (port 1) as this is useful for a power amplifier design (see Figure B.2).

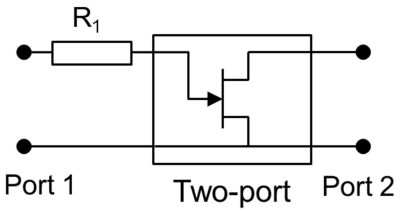


Figure B2 Two port network of the transistor plus series input stabilising resistor R_1

Setting resistance at port 2 to zero (R_2=0), the stability expression can be simplified and rearranged to solve for R_1

$$R_1 = \frac{K\left|Z_{12}Z_{21}\right| + \mathrm{Re}(Z_{12}Z_{21})}{2\,\mathrm{Re}(Z_{22})} - \mathrm{Re}(Z_{11}) \qquad \text{B3}$$

The value of R1 can now be solved for a given stability measure K. Taking the boundary condition of K=1 provides the minimum resistance of R_1 for unconditional stability.

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