Protection Strategy for Multi-terminal DC Networks with Fault Current Blocking Capability of Converters

R. Dantas*, J. Liang*, C. E. Ugalde-Loo*, A. Adamczyk†, C. Barker†, R. Whitehouse†

** Cardiff University, Cardiff, CF24 3AA, UK. (e-mail: DantasR, LiangJ1, Ugalde-LooC{@cardiff.ac.uk})*
† GE's Grid Solutions, Stafford, ST17 4LX, UK. (e-mail: Andrzej.Adamczyk, Carl.Barker1, robert.whitehouse {@ge.com},)

Keywords: High Voltage DC Protection, Fault Blocking Converters, Fault Detection, Fault Discrimination.

Abstract

High voltage dc networks are a promising technology to flexibly transmit power over long distances. However, dc grid protection is still a major challenge. DC fault clearance can be mainly achieved with three devices. These are ac circuit breakers (ACCBs), dc circuit breakers (DCCBs) and converters with fault current blocking (FB) capability. In spite of their great operational advantages, FB converters have attracted less attention than ACCBs or DCCBs in dc protection research. To bridge this gap, this paper investigates a protection strategy for a multi-terminal dc (MTDC) network equipped with FB converters and fast dc disconnectors. A novel minimum opening protection approach fully based on local data is proposed. Digital simulations are carried out using PSCAD/EMTDC. Simulation results show that only the two fast dc disconnectors placed in a faulty link operate following a dc fault. These results have verified proposed ideas for the protection of MTDC networks.

1 Introduction

High voltage dc (HVDC) transmission has emerged as a reliable alternative for high power transfer over long distances [1]. Among the different available technologies, deployment of modular multi-level converters (MMCs) for power conversion between ac and dc systems has reached a mature stage [2]. MMCs offer the advantages of achieving high controllability, scalable power and voltage ratings, high efficiency, and an easy integration to form multi-terminal dc (MTDC) networks.

The design of MMC submodules is mainly based on half-bridge or full-bridge configurations [3]. Half-bridge converters incur lower power losses in comparison to full-bridge submodules and are more economic. However, in the case of a dc fault, current flows uncontrollably through the free-wheel diodes. Conversely, full-bridge submodules are able to quickly interrupt the converter dc fault current contribution [4]. Due to this, converters employing full-bridge submodules fall in the category of fault current blocking (FB) converters. Other advantages of the FB converter include dc voltage controllability and flexibility, *i.e.* possibility of a smooth voltage ramp up, voltage level reduction to mitigate atmospheric conditions and voltage polarity reversal for fast de-ionisation of the arc [5].

The fault current interruption capability of the FB MMC is a very important feature [6]. This could also be achieved with traditional ac circuit breakers (ACCBs) or with dc circuit breakers (DCCBs). The use of ACCBs is economical but may be impractical due to their long operation times, which may cause a long outage time of an MTDC grid [7]. The latter option is preferable, although DCCBs are not commercially available yet and will appear in the market at a high cost [8].

Fault detection and discrimination (selectivity) for dc networks is a subject undergoing intense study within HVDC research. Various fast and selective algorithms have been proposed in the literature [7]. Among these, communication-based methods achieve good results in terms of selectivity [9] at the expense of incurring communication delays, potential communication channel failure and a higher system cost. On the other hand, methods based on local data have the advantage of a fast decision-making.

Recent work has addressed the use of selective algorithms based on current or voltage derivatives [10]–[12]. However, derivative methods have been tested in MTDC grids composed by cables only. Their application for overhead lines (OHLs) is more complex due to the low distributed capacity, fast propagation delay and atmospheric disturbances. In addition, the derivative approach is sensitive to the fault impedance and to the size of link inductors. These inductors are placed at the end of each dc link and are commonly referred to as current rate limiting devices. A dc fault causes a positive rate of change of current in many dc relays. On the links in the vicinity of the fault, the rate of change of current is reduced due to the limiting function of inductors. Hence, using the derivative methods, dc faults can be classified as internal or external by comparing the derivative values with pre-defined thresholds.

Even if the commercial availability of DCCBs poses important restrictions, the practical realisation of MTDC networks may be achieved by incorporating alternative protection devices. A feasible option is to employ converters capable of blocking fault current. To the knowledge of the authors, only one protection strategy for MTDC grids using FB converters has been reported in the literature [13] and, in spite of its potential, constitutes an under-researched topic that should be carefully analysed. To bridge this research gap, a protection strategy for MTDC grids equipped with FB converters is proposed in this paper. The scheme is based on a fault detection and a novel fault discrimination algorithm.

Quick selectivity is achieved through a minimum opening approach. Simulations are carried out using PSCAD/ EMTDC. Results show that the strategy is robust to changes in grid configuration and that it is capable of discriminating faults within a wide impedance range.

2 Protection Strategy

Protection strategies consist of fault detection and fault discrimination algorithms. These initiate the operation of fault clearance and fault isolation devices. Grid operation resumes following fault isolation and once no overvoltage is ensured. In the protection strategy proposed in this paper, fault clearance is facilitated by the blocking action of the FB converters, whereas fault isolation is achieved by the opening of fast dc disconnectors (FDs).

It should be emphasised that the proposed protection strategy is a minimum opening approach. This means that ideally only the FDs placed in the faulty link operate.

2.1 Fault Detection

Fault detection algorithms continuously monitor and analyse dc current and dc voltage. In the study carried out in this work, the detection criteria include overcurrent, under-voltage and current derivative algorithms.

The overcurrent algorithm is based on the transgression of a predefined threshold, which has been set as 120% of the nominal dc current capability. The undervoltage criterion is based on a similar principle, with the threshold being set as 85% of the nominal dc pole-to-ground voltage.

On the other hand, the current derivative algorithm is implemented using an adaptive threshold. This criterion exploits sensitivity and speed requirements, where a lower current derivative threshold leads to fast detection flags. The threshold is based on maximum noise detection over a period of time. Hence, it corresponds to a safety factor (assumed as two) multiplied by the noise peak value of a moving window (of 20 ms). A transgression of this threshold for two consecutive time samples implies that a fault has taken place. Since the threshold should comply with set-point changes and operational events, a minimum value or holding time should be considered.

Figure 1 shows an example of the steady-state dc current noise captured by signal ‘didt’. As it can be observed, the maximum peak ‘didt_pk’ is updated once the noise peak is captured in the time-moving window.

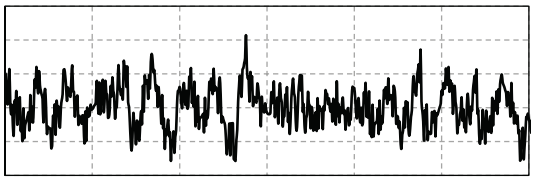

Figure 1: DC current derivative with detection threshold.

A fault is detected if any of the previously described criteria transgresses their respective detection thresholds. Typically, fault detection times are of a few time samples to 1 ms following the arrival of the transient waves.

2.2 FB Converter Blocking

The blocking of FB submodules leads to a quick dc current interruption. In this work, the blocking order consists of the removal of firing pulses to the electronic switches.

HVDC converters are typically protected against overcurrent [1]. In case of an overcurrent event (assuming a 1.2 pu threshold) a blocking order is generated with an assumed processing delay of 0.1 ms. A blocking order is also generated in the case of fault detection in a busbar unit (see Section 3), where a delay of 2 ms is assumed. The blocking criteria, whilst ensuring a safe operation of the converter, is made deliberately slow to allow sufficient time for the analysis of the dc current fault profile in the discrimination algorithm.

Once a converter is blocked, dc current starts to decay to zero. Thus, dc fault energy E_{dc} is absorbed by the arm submodules:

$$E_{dc} = \tfrac{1}{2}\, L_{eq}\, I_{pk}^{\,2} \qquad (1)$$

where

$$L_{eq} = L_{dc} + 2/3\, L_{arm} \qquad (2)$$

$$I_{pk} = I_0 + (V_{dc} T_{blk} / L_{eq}) \qquad (3)$$

In equations (1)–(3), L_{eq} is the equivalent inductance, L_{arm} the converter arm inductance, L_{dc} the equivalent link inductance, I_{pk} the approximated peak dc current at blocking time, I_0 the pre-fault dc current, V_{dc} the pole-to-pole dc voltage, and T_{blk} the time from the arrival of a transient fault current until the converter blocking instant. The FB blocking mode generates a dc voltage equal to $-V_{dc}$. Hence, the approximate time $T_{fall\,0}$ for the dc current to decay to zero is given by

$$T_{fall0} = \tfrac{1}{2}\, I_{pk}\, (L_{eq} / V_{dc}) \qquad (4)$$

The decay time to zero T_{fall0} depends on T_{blk} and L_{eq}. Selecting low values for these protection related parameters is important as they would reflect on a faster current interruption and lower energy absorption by the FB converter. Hence, as fast fault clearance is already ensured by the FB converter blocking action, current limiting devices may be required at a reduced rating (or even avoided). As a disadvantage, fault discrimination algorithms based on the current derivative may not be applicable for grids equipped with FB converters.

2.3 Fault Discrimination

Fault discrimination uses local dc current to determine the faulty dc link. It starts with the fault detection and terminates once the converter associated with that protection relay is blocked. As the blocking operation quickly alters the dc current and dc voltage profiles, discrimination decisions must be taken before the blocking instant. The discrimination algorithm used in this paper is composed by a current direction algorithm and by a novel current comparison of rate of change (CCRC) algorithm.

The current direction algorithm analyses the sign of the current change at the instant of fault detection. Therefore, if the change of current is positive, the fault is classified as potentially internal to a dc link. This can be expressed as

$$dI/dt\ (t_{det}) > 0 \qquad (5)$$

where dI/dt is the current derivative and t_{det} the fault detection instant. Conversely, if the rate of change of current is negative, then the fault is determined as external. It should be emphasised that the previous statements are valid for a dc current sensor oriented for positive current flow from a busbar to a dc link. Due to its simplicity, the current direction algorithm is recommended to form part of dc discrimination algorithms; however, it should be borne in mind that on its own it only achieves partial discrimination.

The CCRC criterion is based on the comparison of the peaks of a second current derivative signal, which is triggered when the incident peak amplitude exceeds a minimum threshold The voltage step caused by a dc fault leads to an increase in dc current. However, the voltage drop is not instantaneous as it is supported by link capacitance and converters operating in voltage control mode. A converter blocking action results in a loss of voltage and, thereafter, a further voltage drop appears which affects the dc current increase rate.

Figure 2 shows the dc fault current of a dc relay external to a faulty link. At approximately 0.011 s the fault induced current wave arrives to the relay location and fault detection is quickly achieved. From this instant, the current increases at a given rate of change (period 1). Shortly after, it continues to increase from 0.012 s but at a different rate (period 2). The difference in slopes occurs as the converters located in the vicinity of the fault block earlier than those at remote locations. Consequently, the voltage drop caused by this blocking action propagates to non-faulty links and results in a super-imposed current with a positive value. This current waveform has a larger rate of change compared to that of the fault induced transient wave.

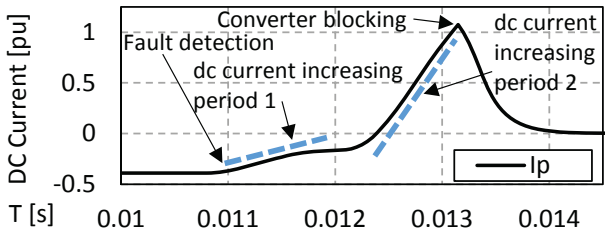

Figure 2: DC current profile on an external fault link.

Figure 3 shows the dc fault current of a dc relay internal to a faulty link. After fault detection, the rate of change of the increasing dc current is captured. The rate of change in period 1, marked after the fault induced wave, has a higher slope than in period 2. This comparison forms the basis of fault discrimination.

Changes in current may be captured by a second order derivative function. A filter is applied to reduce susceptibility to measurement noise. The first incident wave is processed in such a way that its peak is captured and compared with the peaks of the following incident waves. Hence, a fault is discriminated by the CCRC criterion if:

$$pk1 > pk2 \qquad (6)$$

$$pk1 > thr_{min} \qquad (7)$$

where $pk1$ is the amplitude of the captured incident wave, $pk2$ the maximum amplitude of the reflected waves, and thr_{min} a minimum threshold (set as 0.2 pu/ms^2).

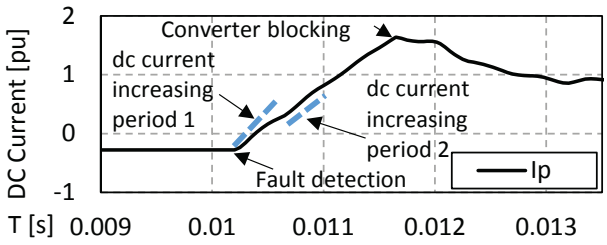

Figure 3: DC current profile for an internal fault link.

If all conditions given by Equations (5)–(7) are satisfied, the fault is classified as internal. If any of those conditions is not complied with, the fault is then external.

It should be noted that this fault discrimination method can also be effectively utilised in a DC grid consisting of different converter topologies, including the converters without the ability to block DC fault current.

2.4 Overvoltage and Voltage Unbalance Suppression

A pole-to-ground (P2Gnd) fault taking place in a symmetrical monopole topology causes a voltage shift. The voltage at the faulty pole collapses, while it typically doubles at the non-faulty pole. This event creates an overvoltage which must be removed quickly to avoid damage to the links and the insulation. Although the overvoltage may decay naturally, this process takes a long time and is highly dependent of the grounding reference –which is commonly used on the ac side of the system [14]. In addition, the start-up of a monopole dc link with a voltage unbalance may lead to asymmetric operating voltages. Hence, not only the overvoltage must be suppressed prior to grid restoration but also the voltage unbalance.

A method to quickly supress the overvoltage and voltage unbalance is here proposed. P2Gnd fault detection is achieved within 2 ms if only one pole experiences an undervoltage event. This can be expressed as

$$V_p > 0.45 \text{ pu and } |V_n| < 0.45 \text{ pu or} \qquad (8)$$

$$V_p < 0.45 \text{ pu and } |V_n| > 0.45 \text{ pu}$$

where V_p is the positive and V_n the negative dc pole voltage.

After a P2Gnd fault detection, the submodules of one phase of the FB converter are temporarily bypassed. This results in a connection of the positive pole with the negative pole through the insulated-gate bipolar transistors (IGBTs) and arm reactors of the submodule. In addition, this implies connecting the ac to the dc side; thus, an overcurrent is expected, which could be sustained if the FB converter is blocked. If an overcurrent occurs, the converter blocks for 1

ms, which leads to a decay of the dc current. The overvoltage suppression operation is resumed after the blocking period. This way, the IGBTs remain in a safe region of operation.

Figure 4 illustrates the voltage profile after a positive-P2Gnd fault at the terminals of a converter. As it can be observed, the application of the overvoltage suppression method greatly limits the duration of the overvoltage period when compared to the case when it is not employed.

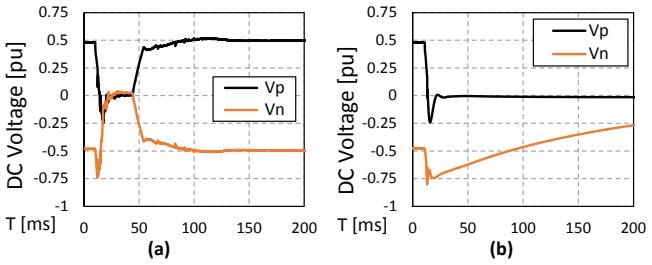

Figure 4: Voltage profile (a) with overvoltage suppression strategy and (b) natural overvoltage decay.

The overvoltage suppression operation terminates once the voltages on both poles are residual (below a threshold of 0.05 pu). The P2Gnd fault isolation occurs after overvoltage and voltage unbalance suppression actions. It should be noted that this overvoltage suppression method could be also used with any other converter topology that allows creating a low impedance path between the DC transmission system poles, such as half-bridge MMC.

2.5 Fault Isolation

The opening of FDs leads to fault isolation. The FDs associated with the faulty link, as determined by the discrimination algorithm, are the devices that receive an opening order.

2.6 Grid Restoration

At this stage, FB converters receive a de-blocking order and restore dc voltage and power in the network. The de-blocking order is given if any of the following conditions is met:

1. Opening operation of a discriminated FD, if existing, with a safety delay of 5 ms (only for rectifiers);
2. Link voltage restoration (e.g. 0.4 pu) on both poles;
3. Maximum blocking time (40 ms set, only for rectifiers).

The opening of FDs placed in non-faulty links is unlikely but might occur. In this case, their reclosing operation is ensured through a voltage recovery criterion.

2.7 Benefits of the Proposed Strategy

The main benefits of the proposed protection strategy include:

1. A limitation of dc fault current level due to the fast clearance action of FB converters. This leads to a reduced rating of current limiting devices at the link ends as the dc current increasing period is very short.
2. A discrimination criterion for a minimum opening approach. The CCRC algorithm is based on the pattern of dc fault currents and thus, pre-defined thresholds are not required. Conversely, local discriminative methods found in the open literature are mainly based on current derivative approaches with pre-defined thresholds. Hence, the presented method represents a novel alternative to discriminate dc faults.
3. A method for fast overvoltage and voltage unbalance suppression which leads to a quick grid recovery after P2Gnd faults. In spite of the low voltage level, the voltage symmetry is an important factor as it enables voltage restoration to nominal values on both positive and negative poles. Without this symmetry, the voltage of one pole would decrease to an undervoltage level while the other would rise to an overvoltage level.

It should be highlighted that the proposed protection strategy is suitable for dc grids equipped with either dc cables or OHLs, or a combination of both.

3 Grid Modelling

An MTDC network has been designed in PSCAD/EMTDC to test the protection strategy presented in Section 2. The grid comprises four FB converters in a meshed/radial configuration, as observed in Figure 5. A symmetrical monopole topology is considered as it is the most widely used [8]. The network dc voltage is ± 200 kV. The converters are based on the detailed equivalent model from Manitoba HVDC Research Centre. The model has 200 submodules per arm and a 29 mH arm inductance. Converter C2 operates in a voltage control mode while the others in power control mode.

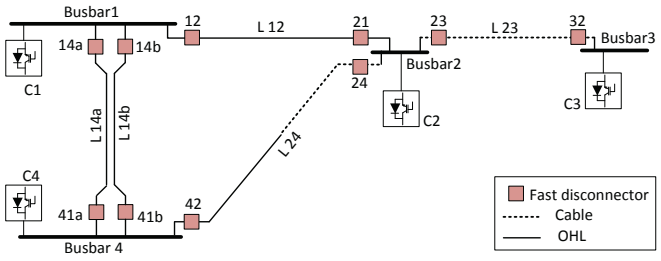

Figure 5: Four-terminal MTDC network.

The cables and OHLs are frequency dependent (phase) models and have been scaled from [15] [16]. The links length is 200km (L12 and L14), 100km (L24) and 50km (L23). A 10 mH link end inductance is considered. The FDs have a 10 ms operation delay and no appreciable current interruption capabilities. The FDs are placed at each link end and are associated with dc relays, which have dc current and dc voltage sensors. The data processing is performed at the busbar units. These are logical units that receive data from all the HVDC line relays and any converter station that are connected to the same bus to issue protection orders. The protection strategy is coded in each busbar unit. All data is analysed locally as there is no communication between the

logic units. The data exchange between a busbar unit and the converter station incurs a delay of 2 ms.

4 Simulation Results

To demonstrate the effectiveness of the proposed strategy, simulations are carried out using the MTDC grid in Figure 5. A P2Gnd fault with a 50 Ω impedance is applied at 10 ms on the positive pole at the middle of Link L23. This causes a voltage collapse at the positive pole and a short oscillation of current in most dc relays. Fault detection is achieved within a few time samples following the arrival of the transient waves by using the undervoltage and current derivative criteria. The discrimination algorithm is initiated at this point and a blocking order is sent to the converter stations.

Fault discrimination is based on a combination of the dc current direction and the CCRC criteria. The current direction criterion is illustrated in Figure 6, which shows the dc current of the positive pole at busbars 1 and 2. Busbar unit 1 exhibits an increased dc current 'Ip12', while dc currents 'Ip14a' and 'Ip14b' initially decrease. Hence, if the fault is located in a link associated with busbar unit 1, it is more likely to be at Link L12 –associated to 'Ip12'. With regards to busbar unit 2, the dc current 'Ip23' increases with the arrival of the transient waves. Hence, it is concluded that Link L23 may potentially be the faulty link.

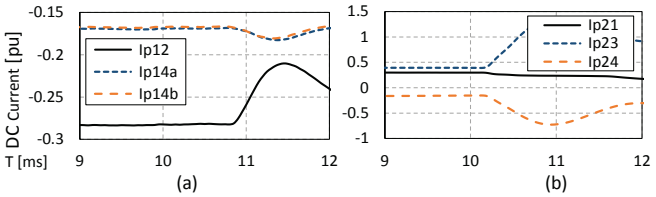

Figure 6: DC current from busbar units (a) 1 and (b) 2.

After the application of the current direction criterion in each busbar unit, the FDs classified as potentially internal to the faulty link are:

- FD 12, FD 23, FD 32 and FD 42.

Notice that the information obtained up to now is non-conclusive as the current direction algorithm offers partial discrimination only. The list of potential FDs may be further reduced with the application of the CCRC criterion.

The CCRC peak comparison criterion is analysed in Figure 7, which illustrates the dc current for a relay to the faulty link and for a relay external to the faulty link. The derivative function block has been applied with a lag of 1 ms to capture quick variations on the dc fault current behaviour. For visual clarity, only the positive values of the current derivative waves are shown. The peak detection is performed on the second order derivative signal. As mentioned previously, the discrimination algorithm starts with fault detection and ends with a converter blocking signal.

Fault discrimination is achieved by comparing the relative peaks of signals 'pk1_32' with 'pk2_32', where 'pk1_32 stands for the peak of the incident wave measured on the dc relay 32 and 'pk2_32' for the peak of the following reflected waves upon the local converter (C3) blocking instant. As 'pk1_32' has the largest peak, the fault is classified as internal to the associated link (L23). Similarly, signal 'pk1_42' is compared with 'pk2_42' where 'pk1_42' stands for the peak of the incident wave and 'pk2_42' for the peak of the reflected waves measured on the dc relay 42. In this case, the peak of the incident wave 'pk1_42' is smaller than the peak of the reflected waves. This occurs due to the dc current rising behaviour following the voltage drop caused by a converter located closer to the dc fault. Converter C2 blocks earlier than C4 due to link propagation and fault detection delays.

The blocking operation of C2 modifies the rates of change of voltage and current on the relays downstream the fault location. Hence, the peak of 'pk2_42' is captured at a higher value than that of 'pk1_42'. The peak comparison leads to classify relay 42 as external to the faulty link. At the end of the discrimination criteria, the FDs classified as internal to the faulty link are:

- FD 23 and FD 32.

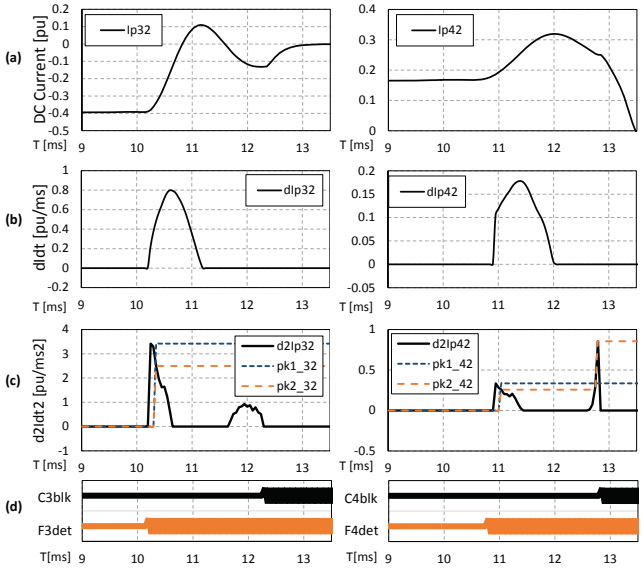

Figure 7: Data considered by the CCRC for internal relay 32 (right) and external relay 42 (left): (a) DC positive pole current, (b) current derivative, (c) second order derivative and (d) converter blocking and fault detection flags.

Figure 8 illustrates the overvoltage suppression strategy. The voltage and one phase current (upper and lower arm) of converter C2 are shown. Figure 8(c) shows the IGBT firing orders for a single submodule. It should be noted that for the adopted submodule switch numeration, the bypass state is achieved by switching on IGBTs T2 and T4, or T1 and T4. T2 and T4 switch on during the overvoltage suppression. A current above a threshold of 2 kA generates a blocking period of 1 ms. After this time, the IGBTs are switched on again. This operation is repeated until the dc voltage decays to a low and symmetrical value for a duration of 2 ms.

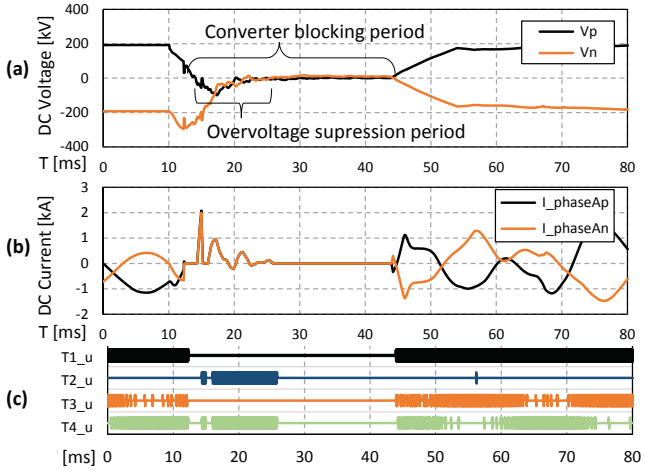

Figure 8: Overvoltage suppression approach on converter 2. (a) DC voltage, (b) phase A arm current and (c) firing orders to the IGBTs at a random submodule.

The ground reference is provided by an ac side reference and the dc fault itself. Once the overvoltage suppression operation ends, the discriminated FDs receive opening orders.

Figure 9 illustrates the closed and open states of the FDs within the MTDC network. As it can be observed, the opening operation of FDs 23 and 32 occurs 10 ms after the opening orders. At this stage the dc fault has been isolated. The following actions include the de-blocking of converters (Figure 10) and power restoration in the dc network.

It should be emphasised that P2P faults (not discussed in this paper) do not require overvoltage suppression actions which would lead to an earlier FD opening operation.

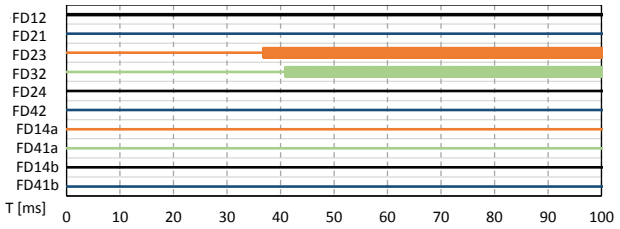

Figure 9: FD state (thick lines represent open state).

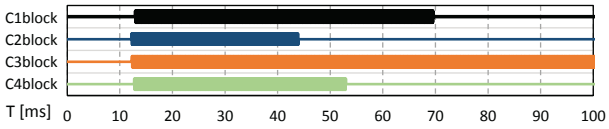

Figure 10: Converter blocking state during the P2Gnd fault.

5 Conclusions

This paper has presented a protection strategy for MTDC grids by using FB MMC and fast dc disconnectors. The fault discrimination algorithm is based on local dc current direction and on the comparison of rate of change of current. The comparison criterion has the advantage of not relying on fixed thresholds as other algorithms in the literature. Those thresholds are captured online and are the peaks of travelling waves, which vary with the fault impedance. Hence, even for a large fault impedance, the protection algorithm is able to discriminate internal or external dc faults. The protection algorithm uses local dc current data from a time window up to 2 ms. Hence, fault discrimination is quickly achieved.

FB converters are able to block dc fault currents. Therefore, the use of ACCBs or DCCBs may not be necessary to protect an MTDC grid that is constructed with FB converters. For instance, when the proposed protection strategy is adopted for the system under study, the grid outage time is restricted to a few tens of milliseconds. This includes the dc fault current decay period, the operation delay of fast disconnectors, and the voltage restoration period. The grid outage time is relatively short and, thus, impacts on the ac system operation can be reduced.

References

[1] V. Akhmatov, M. Callavik, C. M. Franck, S. E. Rye, T. Ahndorf, M. K. Bucher, H. Müller, F. Schettler, and R. Wiget, "Technical Guidelines and Prestandardization Work for First HVDC Grids," *IEEE Trans. Power Deliv.*, vol. 29, no. 1, pp. 327–335, 2014.

[2] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, 2015.

[3] G. P. Adam and B. W. Williams, "Half and Full-Bridge Modular Multilevel Converter Models for Simulations of Full-Scale HVDC Links and Multi-terminal DC grids," *Emerg. Sel. Top. Power Electron. IEEE J.*, vol. 2, no. 4, pp. 1089–1109, 2014.

[4] C. Petino, M. Heidemann, D. Eichhoff, M. Stumpe, E. Spahic, and F. Schettler, "Application of multilevel full bridge converters in HVDC multiterminal systems," *IET Power Electron.*, vol. 9, no. 2, pp. 297–304, 2016.

[5] A. Nami, A. Hassanpoor, and Y. Häfner, "Theory to Practical Implementation of Full-bridge Modular Multilevel Converter for HVDC Applications," in *2016 IEEE International Conference on Industrial Technology (ICIT)*, 2016, pp. 378–383.

[6] C. D. Barker, A. Adamczyk, R. Gupta, G. Fintzos, R. S. Whitehouse, D. R. Trainer, and N. M. Kirby, "Fault Clearing on Overhead HVDC Transmission Lines," in *CIGRÉ Canada Conference*, 2014.

[7] M. Monadi, M. A. Zamani, J. I. Candela, A. Luna, and P. Rodriguez, "Protection of AC and DC distribution systems Embedding distributed energy resources: A comparative review and analysis," *Renew. Sustain. Energy Rev.*, vol. 51, pp. 1578–1593, 2015.

[8] CIGRE B4.52 Working Group, "HVDC grid feasibility study," 2013.

[9] J. Descloux, P. Rault, S. Nguefeu, J. Curis, X. Guillaud, F. Colas, and B. Raison, "HVDC meshed grid: Control and protection of a multi-terminal HVDC system," in *CIGRE 2012, B4-308*, 2012.

[10] J. Sneath and A. D. Rajapakse, "Fault Detection and Interruption in an Earthed HVDC Grid using ROCOV and Hybrid DC Breakers," *IEEE Trans. Power Deliv.*, vol. 31, no. 3, pp. 973–981, 2016.

[11] W. Leterme, J. Beerten, and D. Van Hertem, "Nonunit Protection of HVDC Grids With Inductive DC Cable Termination," *IEEE Trans. Power Deliv.*, vol. 31, no. 2, pp. 820–829, 2016.

[12] J. Descloux, J.-B. Curis, and B. Raison, "Protection algorithm based on differential voltage measurement for MTDC grids," in *12th IET International Conference on Developments in Power System Protection (DPSP 2014)*, 2014, pp. 1–5.

[13] A. Adamczyk, C. D. Barker, and H. Ha, "Fault Detection and Branch Identification for HVDC Grids," in *12th IET International Conference on Developments in Power System Protection*, 2014, pp. 1–6.

[14] H. Wang, G. Tang, Z. He, and J. Yang, "Efficient Grounding for Modular Multilevel HVDC Converters (MMC) on the AC Side," *IEEE Trans. Power Deliv.*, vol. 29, no. 3, pp. 1262–1272, 2014.

[15] F. Mura, C. Meyer, and R. W. De Doncker, "Stability Analysis of High-Power DC Grids," *IEEE Trans. Ind. Appl.*, vol. 46, no. 2, pp. 584–592, 2010.

[16] ABB, "HVDC Light ® Cables - Submarine and land power cables." Technical Brochure, 2006.