SERIES CURRENT FLOW CONTROLLERS FOR HIGH VOLTAGE DIRECT CURRENT TRANSMISSION GRIDS

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To Nageshwari, Annamma, Rajaratnam and Kandiah...

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Abstract

Large scale grid integration of renewables and cross country border energy exchange may be facilitated by multi-terminal high-voltage direct-current (MTdc) grids. However, as the number of terminals and dc lines increases, power flow management between dc nodes becomes a major challenge. The current carrying capability of dc lines is limited by their thermal and electric stress limits. Thus, the line current must be maintained within the permissible operational region to protect the lines from damages. This thesis addresses this fundamental issue through the introduction of inter-line current flow controllers (CFCs) into MTdc grids. An inter-line CFC is a low power rated controllable voltage source that can enhance system performance by suitably redirecting the current flow at the point of connection. It enables regulation of the dc line current flow by changing the voltage at the dc terminals where it is inserted. The research work presented in this thesis is aimed to realise the most feasible CFC topologies to facilitate flexible power flow between dc nodes. The main contributions of this research work comprise of four parts, namely, (1) design and development of dc CFC topologies, (2) prototyping of the proposed CFCs (3) implementations of centralised and communication free control schemes for densely meshed dc grids, and (4) protection of inter-line CFCs.

In the first phase, the characteristics, control and operation for five configurations of inter-line CFCs are studied, namely, resistive, RC circuit, capacitive, dual H-bridge, and single H-bridge based CFCs. A multi-port CFC is proposed to facilitate current regulation on multiple lines simultaneously. An experimental platform consisting of a three-terminal dc grid and small scale prototypes of the proposed CFCs have been developed to validate the concepts. It is clearly shown through experiments and time-domain simulations that all devices are capable of improving the system performance.

A centralised hierarchical control system is proposed to coordinate the operation between multiple CFCs. A novel voltage sharing control scheme is demonstrated. It is shown that such

scheme reduces the workload on a single CFC by sharing the required control voltage between multiple CFCs, and, additionally, can be used to avoid control conflicts among active CFCs during communication failure. New protection methodologies are implemented to protect the CFC during internal failures and dc faults. Small-scale dc circuit breakers have been developed to study the performances of 1B and 2B-CFCs under a pole-to-pole fault.

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Abbreviations

1B-CFC	Single H-bridge Current Flow Controller
2B-CFC	Dual H-bridge Current Flow Controller
C-CFC	Capacitive Current Flow Controller
CB	Circuit Breaker
CC	Current Control
CFC	Current Flow Controller
DCCB	Direct Current Circuit Breaker
FACTS	Flexible Alternating Current Transmission Systems
FB-MMC	Full-Bridge Multi-modular Converter
HB-MMC	Half-Bridge Multi-modular Converter
HVdc	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
LC	Local Controller
LCC	Line-Commutated Converter
LCS	Load Commutating Switch
p.u.	Per-Unit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MMC	Multi-modular Converter
MTdc	Multi-terminal Direct Current
OHL	Over head line

PWM	Pulse Width Modulation
R-CFC	Resistive Current Flow Controller
RC-CFC	Resistive Capacitive Current Flow Controller
RCC	Remote Control Centre
UFD	Ultra Fast Disconnector
VC	Voltage Control
VSC	Voltage Source Converter
VSM	Voltage Sharing Mode

1 Introduction

1.1 Background

As the world moves towards a low carbon energy production, a large amount of renewable energy needs to be integrated into the electricity system. One of the major potential contributors among the existing RESs is offshore wind energy due to its capability of offering clean and eco-friendly energy [1]. Large offshore wind farms are generally located far away from shore, making power transmission challenging. Ac transmission is not suitable for distances longer than 50 km [2]. It is widely recognised that wind integration using voltage source converter (VSC) based high-voltage direct-current (HVdc) links offer a high efficiency, reliability and bulk power transmission over long distances [3, 4, 5, 6]. Fig. 1.1 shows the existing and proposed HVdc inter-connectors in Europe. Projections indicate that the amount of wind energy in Northern Europe will raise to ≈126 GW by 2030 [1].

The delivery of steady and reliable power to onshore ac grids may be ensured by connecting existing HVdc link terminals to additional VSCs to form multi-terminal HVdc (MTdc) grids [8]. An MTdc system will enable cross country border energy exchanges where the excess energy can be transferred between countries, increasing the functionality and reliability of the network [9]. The formation of MTdc grids through the interconnection of existing HVdc links is currently impeded by technical challenges, such as fast dc grid protection, grid standardisation and flexible power flow control between dc nodes [10, 11, 12]. Among the aforementioned challenges, this thesis address the power flow management issues in meshed dc grids.

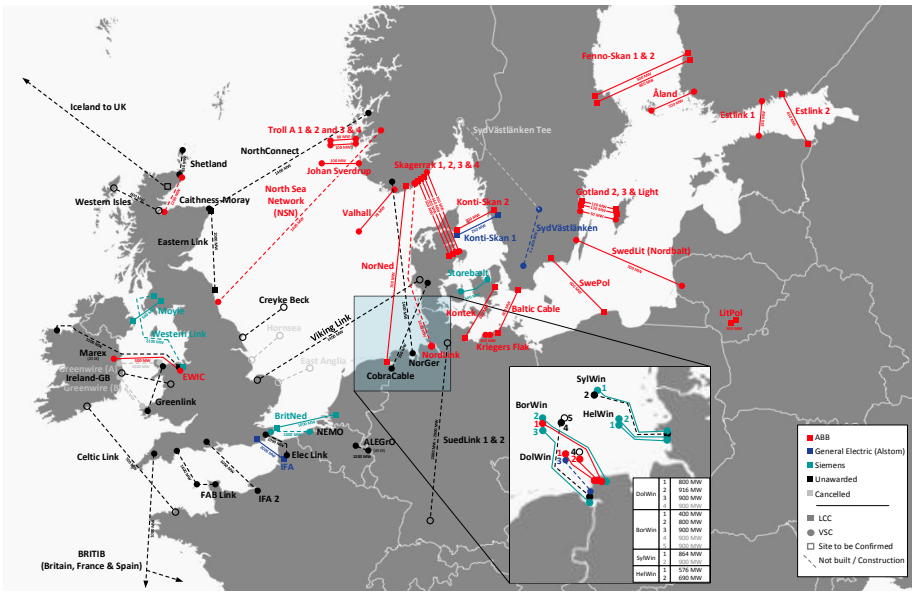


Figure 1.1: HVdc links in Europe [7].

The power transfer capability within a dc grid is not fully controlled and limited by its admittance matrix and cable thermal ratings. In addition, flexible power flow between dc nodes poses significant challenges as the system increases in complexity. In a simple grid, power flow control can be precisely achieved by adjusting the voltage set points of each converter [13, 14, 15]. However, this preciseness decreases with an increase of terminals and branches. Poor grid power flow management could lead to transmission bottlenecks, undesirable power losses and branch overloading (exceeding thermal ratings) [16]. A continuous operation under these conditions could cause dc line breakdowns. Thus, power flow should be rescheduled flexibly between terminals to improve the reliability and efficiency of the dc grid [17].

The previous issues can be relieved by using current flow controllers (CFCs) [18] –inspired by flexible ac transmission systems (FACTS) devices. FACTS equipment is used to regulate key power system parameters by incorporating power electronics-controlled devices into the high-voltage side of ac networks to make it electronically-controllable [19]. The flexibility afforded by FACTS devices comes with the possibility to manage active and reactive power. Although there is no reactive power to be compensated in a dc grid, a CFC may be employed to regulate active power flows within the dc network [20]. This way, a CFC may enable the operation of dc lines/cables within their thermal rating, a flexible power flow between different systems

connected to the dc grid, and an increase/decrease in the amount of power transferred between networks. For instance, a CFC may be used to export excess power from one point of the dc grid to another by changing the grid's admittance matrix.

In recent years, substantial research has been dedicated to power flow control in dc grids using dc-dc converters [21, 22, 23, 24, 25]. The dc-dc converters play a pivotal role in the formation of dc grids by interconnecting dc systems with different voltage levels [26]. However use of a dc-dc converter exclusively for power flow control is not a viable solution in terms of operational and capital costs. Conversely, series-connected CFCs, as proposed in [18] and [27], have lower losses, maintenance and installation costs than their shunt counterpart. Although, this makes them a promising solution for MTdc grid power control, there is still room for improvement with respect to cost and footprint as these CFCs require a large step-down isolation ac transformer. In this thesis, the challenges associated with ac side tapping are eliminated by introducing dc CFCs.

1.2 Objectives and Scope of the Research Work

This thesis investigates the power flow management in meshed dc grids using dc CFCs. The main objectives of this research work are summarised as:

- Define the feasible CFC topologies in terms of control flexibility, power losses, cost and footprint to facilitate current control in meshed dc grids.
- Design local controllers to accomplish smooth transition from by-pass mode to current control mode during steady-state and line overloading conditions.
- Coordinate the operation between multiple CFCs through optimizing the required series dc voltage for current control.
- Eliminate imbalance between dc poles that occurs due to different cable degradation rate or asymmetrical tapping of dc cable.
- Experimentally validate the function and operational concept of CFC.

- Implement protection methodologies for inter-line CFCs to protect the device against any dc fault and internal failure.

1.3 Contributions of the Research Work

The main contributions of this thesis can be summarised as follows:

- **Operation and control of dc CFCs:** To enable current control in dc grids, five different types of CFCs have been proposed, namely, resistive (R-CFC), RC circuit (RC-CFC), capacitive (C-CFC), dual H-bridge (2B-CFC), and single H-bridge (1B-CFC) based CFCs. An RC-CFC is proposed to improve the controllability of a R-CFC. The power losses caused on R-CFC and RC-CFC are eliminated by introducing a C-CFC. Although, C-CFC exhibits lower power losses compared to R-CFC and RC-CFC, its operation range is limited to two quadrants. To relieve the shortcoming of C-CFC, a 2B-CFC and 1B-CFC are introduced.

- **Design of local controllers:** A single modulation controller is proposed to control CFCs without a controllable voltage source element such as in the C-CFC. The controller performance is further enhanced by adopting a compensator based voltage controller. A dual modulation controller is proposed to independently regulate the line current and CFC capacitor voltage.

- **Design of a hierarchical control scheme to coordinate the operation between multiple CFCs:** A novel centralised hierarchical control scheme is proposed to coordinate the operation between multiple CFCs. Moreover, a new control strategy called voltage sharing method is proposed to increase the grid control flexibility during CFC overloading and absence of communications.

- **Pole balancing:** CFCs are used to provide an auxiliary pole balancing support during an imbalance condition by injecting dc voltages in series with dc lines.

- **Prototyping of CFCs:** To prove the function and operational concept of a CFC, small scale reconfigurable CFC modules are designed and developed to adopt all the proposed CFC topologies. The impact of semiconductor voltage drops on line current flow is extensively

analysed to determine the module specifications. Start-up and shut-down procedures for the experimental test-rig and CFCs are implemented to ensure the safety of CFC modules.

- **Prototyping of dc circuit breakers (DCCBs):** Small-scale solid-state based DCCBs are developed to study the performances of 1B and 2B-CFCs under a pole-to-pole dc fault. Protection methodologies are implemented to protect the CFCs against any overvoltage or overcurrent during dc faults.

1.4 Thesis Overview

- **Chapter 2** address the challenges in achieving flexible power flow control between dc nodes in meshed dc grids and provide a review on the existing CFC topologies and their merits and drawbacks.

- **Chapter 3** presents the operation and control of three different types of CFCs, namely, R-CFC, RC-CFC and C-CFC. The performances of the CFCs are evaluated under line overloading condition on a three terminal meshed HVdc test-rig. In addition, a RC-CFC is used to provide current nulling on the compensated line to ease the maintenance.

- **Chapter 4** presents the operation and control of a 2B-CFC. The operation of the CFC is analysed under current control mode and voltage control mode. A compensator based dual modulation scheme is proposed to control the CFC. The performance of the CFC is evaluated under steady state and line overloading conditions using a three terminal meshed HVdc test-rig. Furthermore, the impact of semiconductor voltage drops on line current flow is discussed.

- **Chapter 5** derives a new CFC topology (1B-CFC) by replacing the capacitor of a C-CFC with a controllable voltage source element. Thus, operational limitations imposed by a C-CFC are eliminated. A single modulation control strategy is proposed to control the CFC. This modulation technique regulates the line current via adjusting the voltage across the CFC capacitor. The concept of 1B-CFC is extended to multi-port CFC to increase the control flexibility and reliability. The concepts are experimentally validated on a HVdc test rig.

- **Chapter 6** introduces a centralised hierarchical control scheme to coordinate the operation between multiple CFCs. A novel voltage sharing method is implemented improve the system performance during communication failure or CFC overloading by sharing the required capacitor voltage among CFCs. The effectiveness of the proposed voltage sharing method scheme is experimentally verified on a three-terminal HVdc test-rig. Besides current regulation, CFCs are used to provide auxiliary pole balancing services during pole imbalance conditions. Furthermore, protection methodologies are implemented to protect the CFC during internal failure and system failure. Fault performances of the 1B and 2B-CFCs are experimentally assessed under a pole-pole fault. For completeness, the changes in dc side harmonics due to CFC switching are analysed.

2 Flexible Power Flow Control Between DC Nodes in Meshed HVdc Grids

2.1 Introduction

The breakthrough in the development of solid-state semiconductor valves in the 1970s has led to the installation of numerous point-to-point HVdc links around the globe. HVdc links are suitable for bulk power transmission over long distances due to their lower losses and costs compared to ac links [4]. Particularly, voltage source converter (VSC) based HVdc links have been widely adopted over line-commutated converters (LCCs) based links due to their decoupled power flow control, black-start capability, control flexibility and reduced footprint [9, 28, 29, 30, 31]. Although the VSC performs better in many aspects, the LCC is still attractive due to its higher power handling capabilities and fault sustainability [9]. The conventional 2-level based VSC exhibits 1.7 % power losses due to high frequency hard-switching [32]. To minimise the power losses and harmonics, multi-modular converters (MMCs) were introduced in 2003 [33]. MMCs consist of series connected sub-modules and generates sinusodial ac waveforms at the converter output by inserting or by-passing these sub-modules in series with the arm. As the number of sub-modules increases, the switching frequency and the harmonics can be reduced. Thus, the power losses are minimised [34].

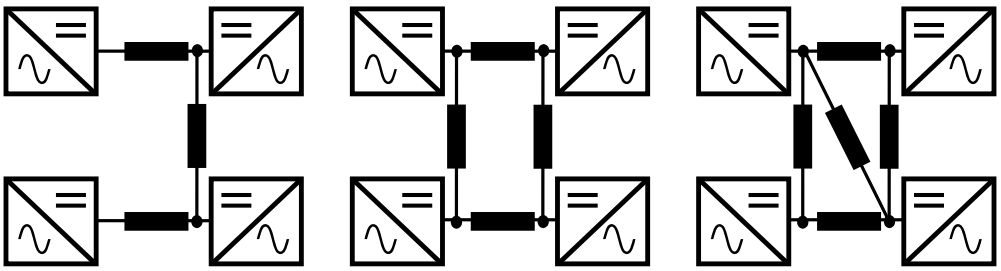
Ever since the installation of first VSC based HVdc link in 1997, multi-terminal dc (MTdc) grids have been the point of interest to facilitate cross border energy exchange [3]. Since the VSC exhibit a constant voltage on the dc side, multiple converter terminals can be interconnected on the dc side via dc lines to formulate a dc grid. The formation of a dc grid can improve the grid

reliability and stability by providing more steady and reliable power transfer through averaging the available wind power [8, 11]. With increasing power demand and generation, an additional number of dc terminals and dc lines in an MTdc grid will be required. As the system becomes more complex, power flow management becomes a major challenge.

In this chapter the concept of dc current flow controllers (CFCs) is introduced to manage power flow in meshed HVdc grids. The characteristics, control and operation of an IGBT and thyristor based series-connected CFCs are studied. The time-domain simulations are carried out to demonstrate the performance of the proposed devices on grid power flow. Through critically analysing the merits and drawbacks of the proposed CFCs in the literature, the concept of inter-line CFC is proposed to overcome the shortcomings.

2.2 State of the Art of Multi-terminal HVdc (MTdc) Grids

As shown in Fig. 2.1 three types of dc grid topologies can be realised, namely, radial, ring and mesh [35, 36, 37]. In a radial configuration, power flow between two terminals is carried out through one unique transmission path. Thus, failure of one of the dc lines could interrupt the power flow between terminals. In the case of ring or mesh configurations, there are more than one transmission paths available between two terminals. Hence, these topologies provide N-1 contingency in the event of a line disconnection [35]. The mesh topology provides a better solution in terms of power losses, reliability and flexibility for power exchange. On the other hand, the investment costs are highly elevated as result of more dc lines [36].



(a) Radial (b) Ring (c) Mesh

Figure 2.1: DC grid topologies

MTdc grids are still in a conceptual stage as their development is hindered by technical challenges, such as grid protection, standardisation and power flow control [10, 11, 12]. There

have been many recent research activities in the development of DCCBs and dc grid protection strategies. DCCBs projected to be an integral part of the dc grid protection system, which should break the fast-rising transient fault currents in a few milliseconds to maintain the grid stability and to protect the converters against any overvoltage or overcurrent [38, 39, 40, 41, 42]. Among the proposed DCCBs in the literature, hybrid DCCBs exhibit high efficiency and an acceptable interruption time. In hybrid DCCBs, the losses during the normal operation are minimised through use of a ultra fast disconnecter (UFD) and a load commutating switch (LCS) [40, 41]. During normal operation, the main circuit breaker branch is bypassed via activating the UFD and the LCS. The breaking time of the hybrid breakers is mainly determined by response time of the UFD. In 2011, ABB has demonstrated the operation of a 80 kV hybrid DCCB with a breaking capabilities of 9 kA [39]. Following this line, in 2013, Alstom grid has developed a 120 kV hybrid DCCB prototype which is capable of interrupting a prospective fault current of 3 kA within 2.5 ms [43]. In [44], a 200kV hybrid DCCB has been used to break a fault current of 15 kA within 3ms. Alternatively, full-bridge (FB) based MMCs are being considered as a feasible solution for a meshed dc grid due to their dc fault blocking capability. Unlike half-bridge (HB) MMC, the FB-MMC eliminates the need of DCCBs to isolate dc faults [45, 46]. By incorporating these developments in the area of MMCs and DCCBs, numerous protection strategies have been proposed to isolate the dc fault and to achieve quick grid restoration [47, 48, 49, 50, 51]. Moreover, some research activities have been focused on protection strategies using AC circuit breakers [48, 50, 52].

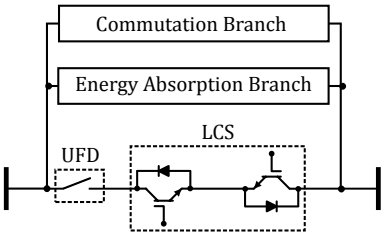


Figure 2.2: Hybrid DCCB.

Existing HVdc links have different voltage levels as they were specially designed for a specific application. Hence, these links cannot be directly interconnected to form a dc grid. This can be overcome by introducing a dc-dc converter (Fig. 2.3). In addition to dc voltage matching, the dc-dc converter can be used to isolate the dc fault by dividing the dc grid into different

protection zones. Although use of dc-dc converters resolve the issue, they are expensive and exhibit similar level of power losses as a VSC [8]. On the other hand need of dc-dc converters can be eliminated through determining a standard dc voltage level among the suppliers.

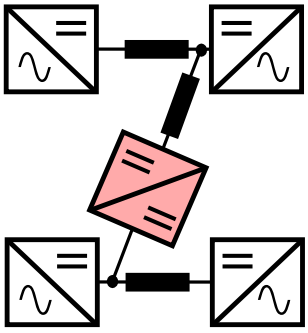


Figure 2.3: MTdc grid formation using dc-dc converter.

2.3 Power Flow Control in HVdc grids

In HVdc systems, dc power are transmitted via overhead lines (OHLs) or cables. Although cables are inherently suitable for underground or sub-sea transmission and pose a reduced visual and environmental impact compared to OHLs, OHLs are attractive owing to their high voltage and high power handling capabilities and lower cost [53],[54]. However, both dc cables and OHLs have intrinsic operational limits over the amount of power that can be transferred. These limits are determined by thermal and electric stress characteristics [55],[56]. The behaviour of thermal and electric stress limit curves in relation to voltage and currents are shown in Fig. 2.4. The electrical stress on dc cables shows a parabolic behaviour while the thermal limitation is fixed [56]. The operation of a dc cable in regions A1 and A2 could damage the cable. The feasible operational region is shown as area A3, where the permissible line current is below the thermal and electric stress limits.

In a very dense MTdc grid, power flow cannot be regulated independently as it is passively determined by the resistance between dc nodes. Since the line current distribution is uncontrolled, some lines may carry excess current while the remaining ones may be under-utilized. To manage the power flow in dc grids, various control schemes such as master-slave control [3], droop control [57, 58, 59, 60] and autonomous converter control [61] have been proposed.

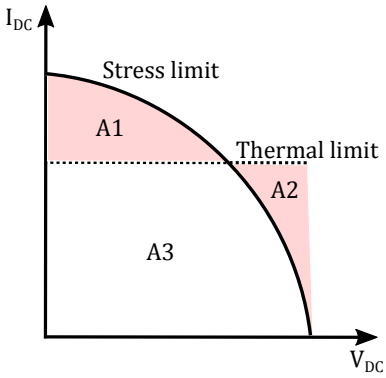


Figure 2.4: DC cable operating regions.

In a system with n number of converters, the proposed control schemes are capable of regulating the current flow in n-1 lines through altering the converter voltage set points. However, the level of preciseness decreases with increasing number of dc lines and converter terminals. System operation beyond thermal and stress limits could damage OHLs and cables and lead to cascaded failure. In a system with high power demand, such a transmission interruption could be very costly. This problem may be relieved through the installation of auxiliary lines, but at the expense of high capital and environmental costs. Moreover, an effective line current control can only be achieved with the inclusion of additional control structures to the system.

2.4 Current Flow Controllers

Power flow controllers (CFCs) are power electronics based devices capable of providing dc line current control in MTdc grids [62]. Since the dc line resistance is low, a small change in dc voltage generates a significant dc current variation which can change the direction of power flow. The CFCs can either be a controllable voltage source or resistor. Based on their connection type, CFCs can be classified as series or shunt-connected (Fig. 2.5) [18].

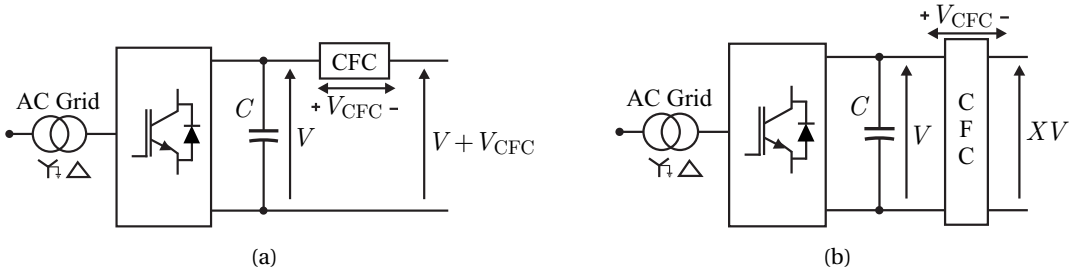


Figure 2.5: Types of CFC: (a) Series-connected; (b) shunt-connected.

2.4.1 Shunt CFCs

The shunt-connected CFC is essentially a dc-dc transformer with step up/down characteristics. The dc-dc transformers can exert dc grid power flow control through regulating both positive and negative pole nodal voltages simultaneously. Its output voltage (XV) is 95-105% of the rated dc line voltage (V), making the power rating of the device 100% under full line current [62]. Although a dc-dc transformer has a great controllability over line power flow and eliminates the need of DCCBs by isolating the dc line, their primary use in a dc grid is to interconnect two systems with different dc voltages and/or operating strategies [26]. Therefore, the operation of a dc-dc transformer around the stepping ratio of 1 for the sole purpose of current flow control is not feasible as these converters exhibit high losses and installation cost. This can be overcome by placing small power rated series controllers at each pole. A series-connected CFC has lower losses, maintenance and installation costs than its shunt counterpart, thus making it a promising solution for MTdc grid power control.

2.4.2 Series CFCs

Series-connected CFCs can either be a controllable voltage source or resistor. Although the most straightforward way to control dc line current is through the inclusion of a controlled series variable resistor [62], this approach offers a limited controllability and causes high power losses. In recent years, several controllable voltage source based CFCs have been proposed to eliminate the shortcomings of a resistive-based solution. The series voltage injection generates a positive resistance effect which increases the dc line current flow –or alternatively, a negative resistance decreasing line current flow.

2.5 Topologies of Series CFCs

2.5.1 Thyristor CFC

A thyristor is a unidirectional device carrying current only in one direction (from anode to cathode). This restricts the operation of thyristor-based three-phase converters to two quadrants (Q1 and Q4), where a change in the direction of the current requires a voltage polarity reversal.

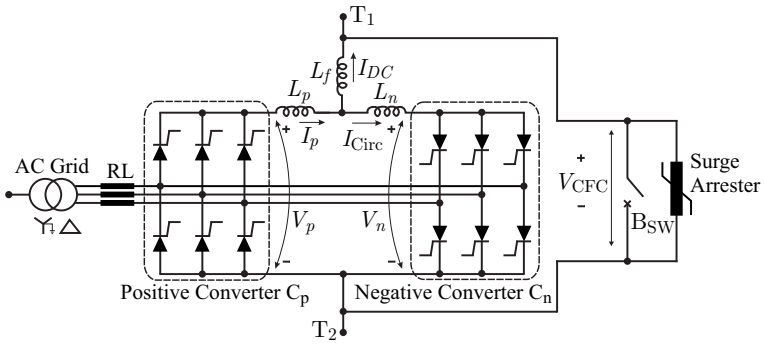


Figure 2.6: Topology of a thyristor-based CFC.

Fig. 2.6 shows a thyristor-based CFC. It consists of two three-phase thyristor-based converters connected in anti-parallel to ensure a four-quadrant operation. The CFC may be powered up using a single-phase ac connection, although this may lead to an unbalanced ac system. This imposes a higher stress on the CFC which could lead to failure. However, since the required dc voltage and thus dc power transfer does not change, the total power from the ac system remains the same.

The firing angles of the converters are related so that both produce the same terminal voltage [63]. While one converter operates as a rectifier, the other acts as an inverter, with

$$\alpha_p + \alpha_n = \pi \tag{2.1}$$

where α_p, α_n are the firing angles of the positive and negative converters, respectively. The CFC's dc side voltages are given by

$$\begin{aligned} V_p &= \frac{3\sqrt{2}}{\pi} V_{s,\max} \cos(\alpha_p) \\ V_n &= \frac{3\sqrt{2}}{\pi} V_{s,\max} \cos(\alpha_n) \end{aligned} \tag{2.2}$$

where $V_{s,\max}$ is the ac line-to-line voltage and V_p, V_n the positive and negative terminal voltages. During current control, only one converter receives firing pulses at any time, with the other being blocked due to the polarity of the current. The positive converter receives pulses only if the line current is positive and above the threshold value. If the line current is negative and

below the threshold value only the negative converter receives firing pulses. When the dc line current falls below the threshold values (Fig. 2.7) both converters receive firing pulses to enable a smooth change in the direction of the current. Thus, a discontinuous dc line current below the threshold value may exist [64]. In this case, the instantaneous voltage difference between converters causes a circulating current, whose magnitude may be limited via inductors L_p, L_n. This has to be done with care as it may increase power losses due to the large dc line current flow through the inductor. Alternatively, the circulating current can be regulated as proposed in [65]. In this work, the control structure shown in Fig. 2.8 is used. An angle β is generated so that

$$\begin{aligned} \alpha_p + \alpha_n &= \pi - \beta, \\ \alpha_{p,\text{new}} &= \alpha_p - \beta/2, \\ \alpha_{n,\text{new}} &= \alpha_n - \beta/2. \end{aligned} \tag{2.3}$$

Where $\alpha_{p,\text{new}}$ and $\alpha_{n,\text{new}}$ represent the new firing angles of positive and negative converters, respectively, with circulating current controller.

The circulating current controller activates only if the dc line current falls below threshold values $I_{\text{DC,th+}}$ and $I_{\text{DC,th-}}$ as shown in Fig. 2.7.

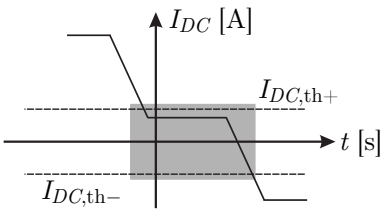


Figure 2.7: DC line current threshold limits.

The thyristor-based CFC controller structure employs nested control loops based on PI controllers. This is shown in Fig. 2.8. An inner control loop is used to regulate the output voltage of the CFC, controlling the firing angle of the thyristor bridge. The outer control loop is designed to regulate the dc line current and generates the reference signal for the inner loop.

Fig. 2.9 illustrates the effect of the circulating current regulator (shown in Fig. 2.8). For this

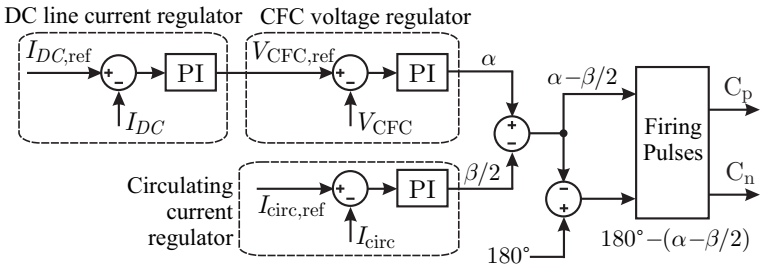


Figure 2.8: Controller structure of a thyristor-based CFC.

example, the dc current reference has been set below a defined threshold to cause a circulating current between the positive and negative converters. As it can be observed, this current contains both ac and dc components. It can be noticed that its magnitude is considerably larger when the controller is not active. Thus, an uncontrolled circulating current could lead to additional power losses than when it is regulated.

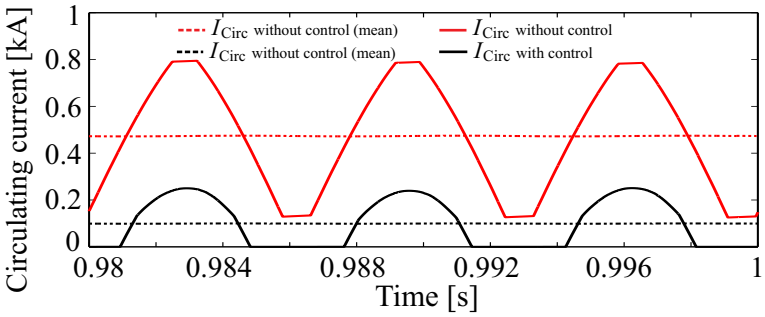


Figure 2.9: Circulating current profile with and without regulation.

2.5.2 H-bridge CFC

An H-bridge CFC consists of a three-phase two-level PWM controlled converter and a four-quadrant chopper –with switching modules consisting of anti-parallel connected IGBTs and diodes. This arrangement ensures a bidirectional capability. The CFC is connected to an ac system through a phase reactor and a step-down galvanic isolation transformer (see Fig. 2.10). On the dc side, the device terminals T_1 and T_2 are connected in series with a dc line and in parallel to a solid-state bypass switch B_{SW} and a surge arrester. This way, if the CFC is not active it is bypassed via B_{SW}. The surge arrester protects the CFC in case of a dc fault, where high fault currents could lead to overvoltages. The output dc voltage V_{CFC} and the capacitor voltage V_C

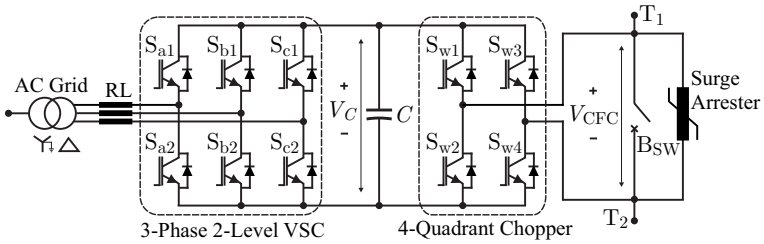


Figure 2.10: Topology of the H-bridge CFC.

are related as [66]

$$\begin{aligned} V_{\text{CFC}} &= (2D-1)V_C, \\ -V_C &\le V_{\text{CFC}} \le V_C, \end{aligned} \tag{2.4}$$

where D is the duty cycle of the chopper and $0 \le D \le 1$. The two-level converter maintains a constant capacitor voltage while the H-bridge regulates the dc line current by generating a variable mean dc voltage in series with the dc line.

The capacitor voltage controller, shown in Fig. 2.11, is similar to synchronous reference frame-based VSC control schemes with PI controllers. It consists of an inner current control loop cascaded with an outer capacitor voltage control loop. Import and export of reactive power are avoided by setting the q-axis reference to zero. The H-bridge controller (Fig. 2.12) consists of two cascaded control loops; namely, the dc line current controller (outer loop) and the V_{CFC} controller (inner loop). The outer loop regulates the dc line current by generating a reference signal $V_{\text{CFC,ref}}$ to the inner voltage controller.

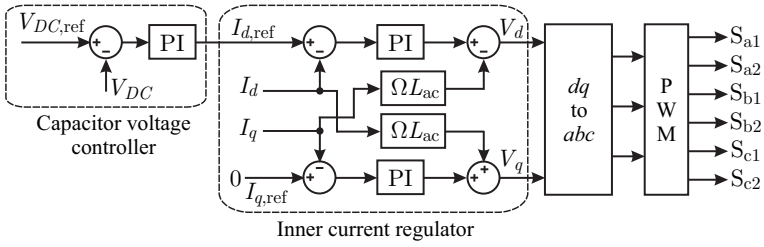


Figure 2.11: Controller structure of three-phase two-level converter.

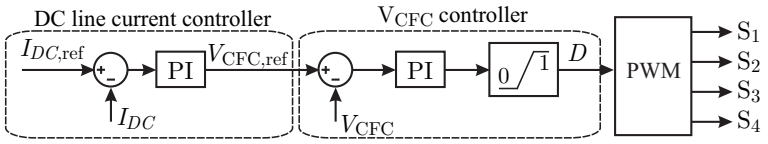


Figure 2.12: H-bridge controller.

2.6 Simulation Results

2.6.1 Test MTdc Network Configuration

A four terminal VSC-based MTdc grid has been configured to demonstrate the dynamics, control and operation of the CFCs presented in Sections 2.5.1 and 2.5.2. The system under study is shown in Fig. 2.13(a). The four terminal system has been adapted from the one presented in [13], which emulates a hypothetical North Sea based meshed dc grid where Grids 1-4 represent, respectively, Scotland, RG Nordic, England, and RG continental Europe [35, 67]. All converters have been modeled as switching type (IGBT-based) two-level symmetrical monopoles [Fig. 2.13(b)]. The location of the thyristor and H-bridge based CFCs is shown in Fig. 2.13(c). A pole-to-pole dc voltage rating of ±320 kV and a power rating of 1 GW have been used. Each converter is connected to an ac system with a phase reactor and a transformer. A single tuned filter is deployed on the valve side (transformer secondary) to eliminate harmonics due to converter switching.

For the system under study [Fig. 2.13(a)], terminals T_1, T_3 and T_4 are operated under a constant power control mode whereas T_2 acts as a slack busbar that maintains grid power balance (constant dc voltage). The initial reference values are given in Appendix A. A positive power flow is represented by the arrows in Fig. 2.13(a). The dc lines have been modeled as PI sections [68, 69]. The dc line parameters are given in in Appendix A, where the electrical parameters have been taken from a cable manufacturer [70] and line lengths adapted from [13].

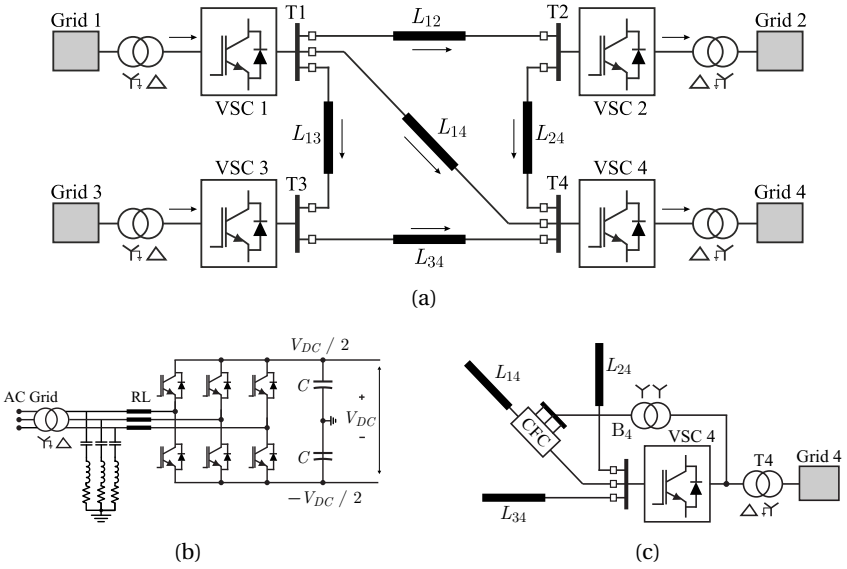


Figure 2.13: (a) Four-terminal VSC-based MTdc grid. (b) Configuration of each terminal converter. (c) Location of thyristor-based and H-bridge CFCs.

2.6.2 Results and Analysis

2.6.2.1 Controllability

The controllability of a CFC is defined as the change in the dc line current with respect to the control ratio, where control ratio represent the magnitude of the inserted voltage with respect to CFC voltage rating. A control ratio of 1 represents the maximum dc voltage generation, with 0 representing 0 V. To evaluate controllability, the capacitor voltage of the H-bridge CFC has been set to 5 kV. The reference values for the converters are provided in Table A.3. The thyristor and H-bridge CFCs have been connected in series with line L_{14} (shown in Fig. 2.13). The initial line current without an active CFC has been defined as I_0 = 432 A. Fig. 2.14 shows the change in dc line current with the control ratio of each device. As shown, the control ratio is proportional to the inserted dc voltage in thyristor and H-bridge CFCs.

The controllability plot (Fig. 2.14) is divided in two regions. Region 1 is the area above I_0, where the inserted voltage in series with the dc line L_{14} is positive; Region 2 is the area below I_0, where the inserted voltage is negative. The plot clearly shows that both thyristor and H-bridge CFCs exhibit similar level of controllability.

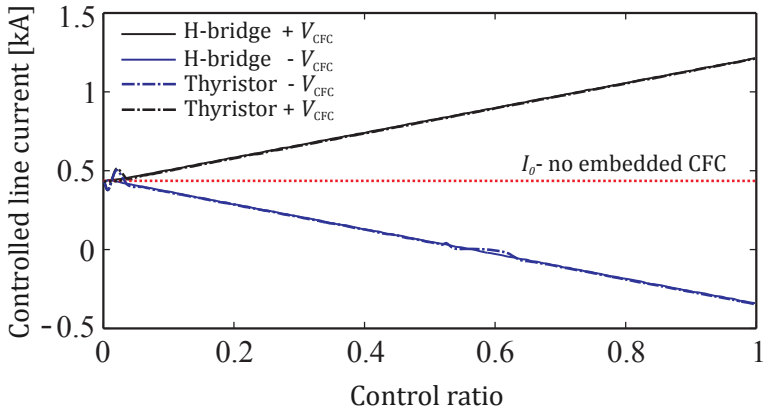


Figure 2.14: Controllability of thyristor and IGBT based CFCs.

2.6.2.2 Line current control

2.6.2.2.1 Thyristor based CFC: The results for this device are shown in Fig. 2.15. The CFC generates a constant dc voltage rather than a pulsating dc voltage [Fig. 2.15(a)]. Pulses for the negative and the positive converters are blocked initially. At $t = 1$ s the positive converter is fired to regulate the dc current of L_{14} to 600 A. At the same time the negative converter is blocked and thus the current through the positive converter equals that of the dc line [Fig. 2.15(b)]. During the current reversal period the current of L_{14} falls below the threshold value [Fig. 2.15(c)]. Thus, for a short period both converters receive pulses and a circulating current flows between them due to an instantaneous voltage difference. The magnitude of this current is limited to ±100 A by the circulating current controller and inductances L_p, L_n. This allows a smooth dc line current reversal. As shown in Fig. 2.15(b), once the dc line current passes the negative threshold it is no longer provided by the positive converter (becoming zero for it) but by the negative one. After the reference power of the VSCs changes at $t = 4$ s and $t = 4.5$ s [Fig. 2.15(e)], the dc line currents and terminal dc voltages [Figs. 2.15(c)-(d)] reach new steady state values while the controlled line current has remained constant at −200 A. However the required dc voltage has increased due to the new line current distribution.

2.6.2.2.2 H- bridge CFC Fig. 2.16 shows the simulation results for this device. The capacitor voltage is maintained at 5 kV during the simulation [Fig. 2.16(a)]. To increase the dc line current of L_{14} to 600 A [Fig. 2.16(d)], the CFC generates a positive mean dc voltage V_{CFC} between converters 1 and 2 [Fig. 2.16(b)]. As shown in Fig. 2.16(e), the converters have adjusted their

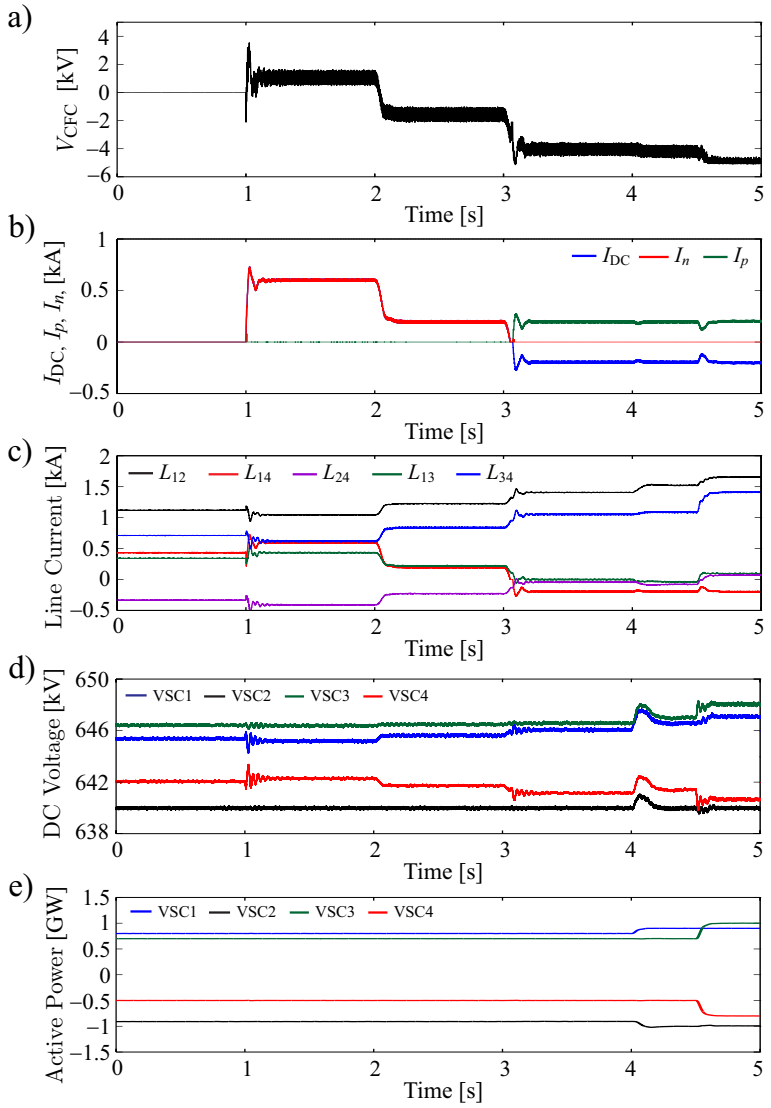


Figure 2.15: Dynamics of the thyristor-based CFC: (a) CFC inserted voltage; (b) CFC dc current profile; (c) dc line current profile; (d) VSC voltage; (e) VSC power.

dc voltages to maintain a constant dc power. For this condition power is exported from the dc grid to the ac side [Fig. 2.16(c)]. At $t = 2$ s, the CFC reference is set to 200 A –lower than the initial value $I_0 = 432$ A. A negative mean dc voltage is applied between the terminals to decrease the current flow. Since the current is positive and the applied voltage has changed its polarity, power is imported from the ac side to the dc grid. It can be seen that the CFC is able to carry out a current reversal (−200 A) at $t = 3$ s and that the desired line current is achieved by further increasing the voltage magnitude. To maintain the line current constant at −200 A after a positive step change in power at $t = 4$ s [Fig. 2.16(f)], the magnitude of the inserted dc voltage

is increased further [Fig. 2.16(e)]. Following the power step changes at $t = 4.5$ s, the device has almost reached its maximum operating point.

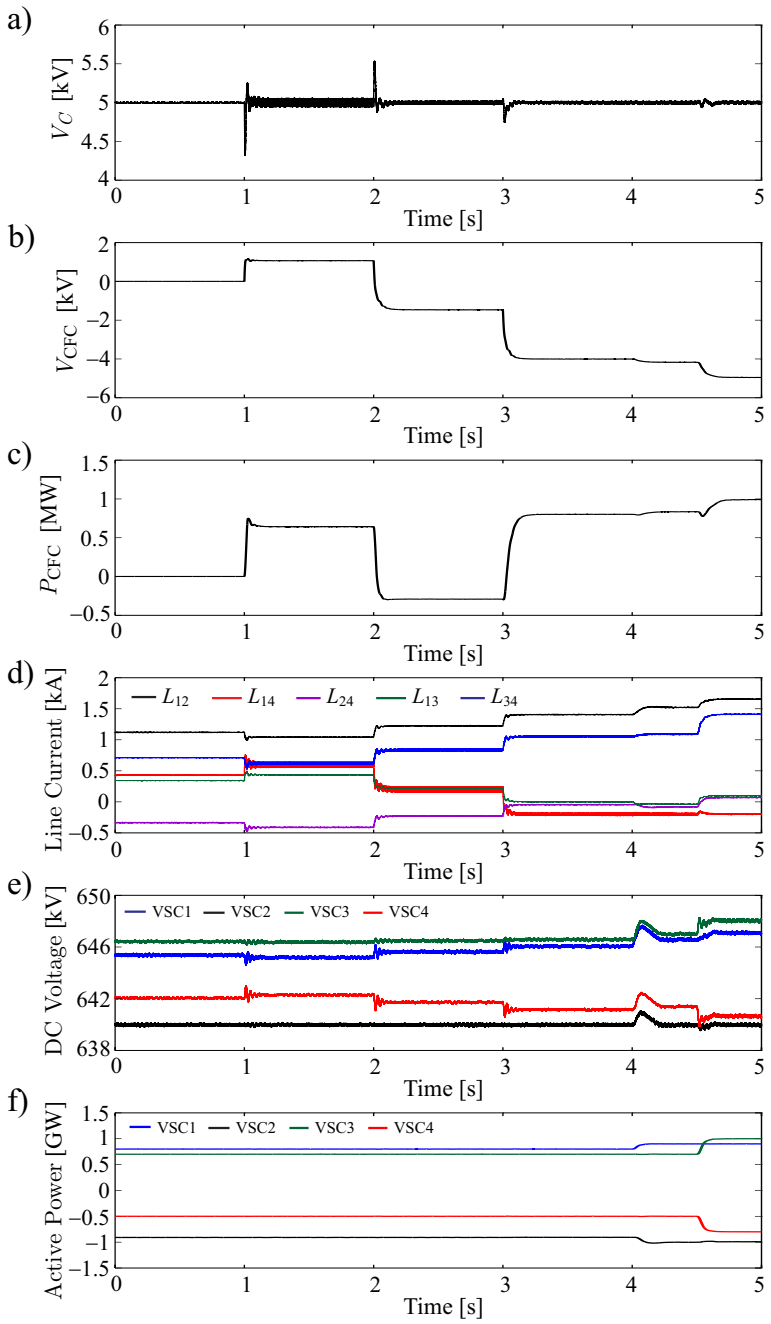


Figure 2.16: Dynamics of the H-bridge CFC: (a) CFC capacitor voltage; (b) inserted dc voltage; (c) CFC dc power; (d) dc line current; (e) VSC voltage; (f) VSC power.

2.7 Inter-line Current Flow Controllers

The results reported in section 2.6.2.2.1 and 2.6.2.2.2 have shown that both CFCs offer similar level of control flexibility over grid current flow control. However, only device control flexibility cannot be used to assess its performance as switching losses, power rating, reliability and cost are essential factors (and constraints) to consider for a practical CFC. Since a power electronics device cannot fulfill all of these characteristics simultaneously, a trade-off between them is required to build a good device.

In thyristor and IGBT based CFCs, the ac connection is established through a step-down transformer. Since these CFCs are electrically coupled to the dc side, the voltage difference between the transformer windings and the ground is equal to the rated dc voltage. Therefore, additional insulation is essential to decrease the capacitance between the windings and ground, but this may in turn increase the transformer size and winding resistance.–implying a higher insulation which increases cost. A large (offshore) installation platform is likely to be needed. Hence, the construction and maintenance of these devices will be more expensive [71]. In addition, a thyristor-based CFC will require large smoothing inductors rated for high dc currents (L_n, L_p, L_f in Fig. 2.6). To achieve this, a number of series connected inductors may be required [72]. These inductors must be installed at least 1.5 to 1.7D away from their centre to provide a minimum magnetic clearance, where D is the diameter of the inductor [73, 74]. Thus, a large platform will be required, with an impact on cost. It should be emphasized that power losses on these inductors and isolation transformer could be extremely higher than the switching losses. In addition, both CFCs generate significant current harmonics in the valve winding, leading to further power losses.

To overcome the aforementioned challenges the device has to be powered inside the dc grid [71, 75]. The dc grid powered device is commonly referred to as an inter-line CFC. The CFC achieves the current control via transferring power between dc lines/nodes.

2.8 Conclusions

In a highly dense meshed dc grid, current flow in each cable cannot be interdependently controlled below its thermal and electrical limits through converter control. In this chapter the concept of CFC is introduced to achieve flexible power flow between dc nodes. The time-domain simulation results show that regardless of the adopted configuration the controllability of the MTdc grid may be increased by a CFC that regulates and redistributes line currents.

As power flow exchange in H-bridge and thyristor-based CFCs occurs between ac and dc points, an ac connection to power up the devices is required –with major cost implications. Such a shortcoming may be relieved by employing an inter-line CFC as it is powered inside the dc grid; thus achieving power flow control through a power exchange between dc points.

3 Resistive and Capacitive based CFC

3.1 Introduction

In HVDC systems, a shunt connected controllable resistance, also called chopper or dynamic breaking resistor, can be used in an event of an overvoltage to maintain the dc voltage within a safe margin by dissipating the excess energy [76, 77, 78]. The same strategy can be adopted to avoid overcurrent in a dc cable by introducing a series connected controllable resistance. In [79], a series impedance modulator is proposed to control the power flow and avoid overheating or overloading of the AC network components. Since there is no reactive power to be compensated in a dc grid, the inclusion of a resistor in series with a dc line generates a voltage drop sufficient to exert the grid power flow. This is shown in Fig. 3.1 where the inserted voltage V_{CFC} is determined by the resistance size. For a resistive CFC with n number of resistor modules (Fig. 3.1), the effective inserted resistance can be controlled at k number of different values by either shorting or inserting each resistor module using a mechanical switch (S_1) where k is given by :

$$k = \sum_{m=1}^{n} \frac{n!}{m!\,(n-m)!} \tag{3.1}$$

Therefore, line current can be controlled at k (eq.3.1) number of different values. It should be highlighted that since these resistors are formed of fixed value resistors, the line current cannot be regulated at a specific value. The mechanical switch, S_n, can be realised with resonance type mechanical CB [20].

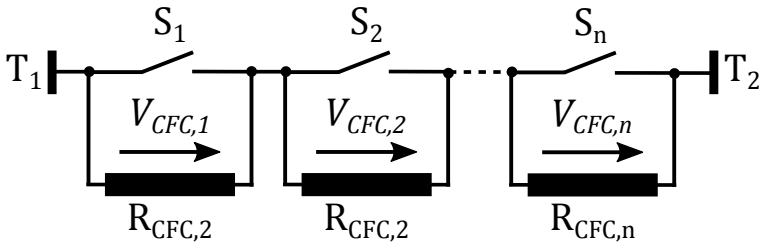


Figure 3.1: Mechanical CB based resistive CFC.

In this chapter, a variable resistor based CFC (R-CFC) is introduced to increase the control flexibility over line current control compared to a fixed value resistor based CFC. An RC circuit based CFC (RC-CFC) is proposed to further improve the controllability. A capacitive based CFC (C-CFC) is derived from the RC-CFC to eliminate the power losses caused by the CFC resistor. In addition, a hybrid CFC circuit arrangement, consisting of the capacitive and RC circuit CFCs, is proposed to expand the operational region of the devices. Small scaled prototypes are designed and developed to validate the operation and control of the proposed CFCs. The Performance of the proposed CFCs is studied under steady-state and transient conditions using a three-terminal meshed connected dc grid.

3.2 Series variable resistor CFC (R-CFC)

Fig. 3.2 shows the solid state arrangement of an R-CFC. The device consists of a power electronic switch, B_1, in parallel with a resistor (R_{CFC}). Switch B_1 is realised with two anti-series connected IGBT switches to ensure bi-directional current flow. A surge arrester must be connected across the bypass switch (see Fig. 3.2) to protect the CFC in case of dc faults, where high fault currents could lead to overvoltages. More details on surge arrester placement and CFC protection requirements are reported in Chapter 6. Let the current be flowing from terminal T_1 to T_2. The device operational modes and corresponding switching waveforms are presented in Figs. 3.3 and 3.4, respectively. The device can be operated under two different operational modes, namely, by-pass mode and current control (CC) mode. When the required current reduction/increment is zero, the CFC is continuously operated in the by-pass mode (Fig. 3.3(a)) by setting the duty cycle of the active switch S_{11} to 1. Since the on state resistance of the IGBT is much smaller than R_{CFC}, most of the line current flows through switch S_{11} and diode D_{12}. During the CC mode,

switch S_{11} is modulated between the on and off switching states, Figs. 3.3(a) and 3.3(b). This continuous modulation generates a mean resistance, R_{eq}, between terminals T_1 and T_2. The value of R_{eq} can be changed via adjusting the duty cycle D. The mean resistance, R_{eq}, can be given by the following equation:

$$R_{eq} = \frac{R_{CFC} \cdot T_{off}}{T_s}$$
$$R_{eq} = R_{CFC}(1 - D) \tag{3.2}$$

Insertion of a mean resistance in series with a dc line increases the effective line resistance, decreases the line current, changes the admittance matrix of the grid and changes the grid power flow.

A PI controller, as depicted in Fig. 3.5, is used to regulate the line current by adjusting the duty cycle of the controlled switch. A first order filter with a cut-off frequency of 200 Hz is used to eliminate the noise and high frequency components from the measured line current.

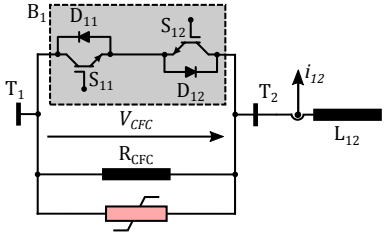
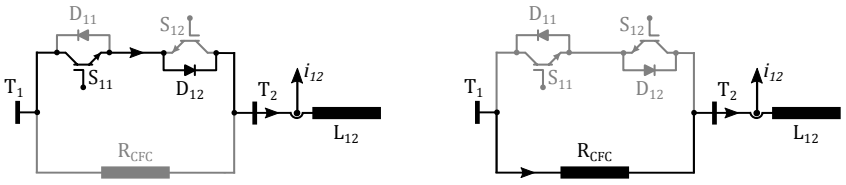


Figure 3.2: Topology of a variable resistor-based CFC.



(a) On-state (b) Off-state

Figure 3.3: Operational states of resistive CFC.

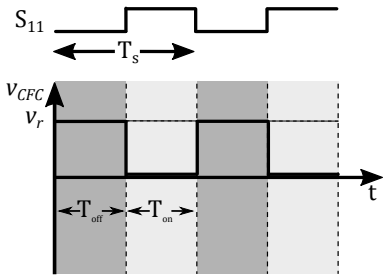


Figure 3.4: Switching waveforms.

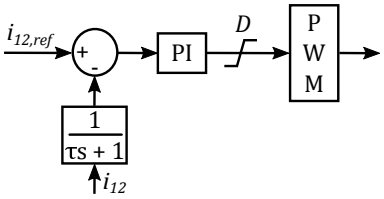


Figure 3.5: Resistive CFC line current controller.

3.3 Series Resistive Capacitive CFC (RC-CFC)

The controllability of a R-CFC is determined by the size of the resistance, and a large resistance increases the device power rating. In order to achieve a zero line current the resistance should be theoretically infinity. On the other hand, the zero line current can be achieved by introducing a capacitive element in series with a finite resistance. To this end, an RC circuit based CFC is shown in Fig. 3.6. The device consists of a power electronic switch, B_1, in parallel with an RC circuit. The switch B_1 comprises two anti-series connected IGBT switches.

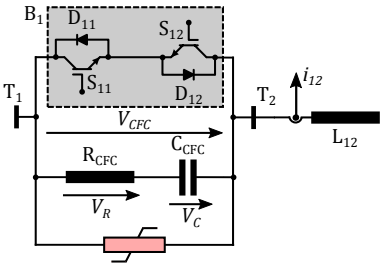


Figure 3.6: Topology of a RC circuit based CFC.

3.3.1 By-pass mode

Lets assume that current flows from T_1 to T_2. As shown in Fig. 3.7, during the by-pass mode , duty cycle of S_{11} is set to 1 to provide zero dc voltage injection.

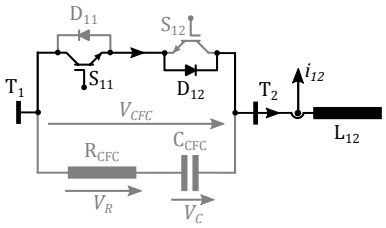
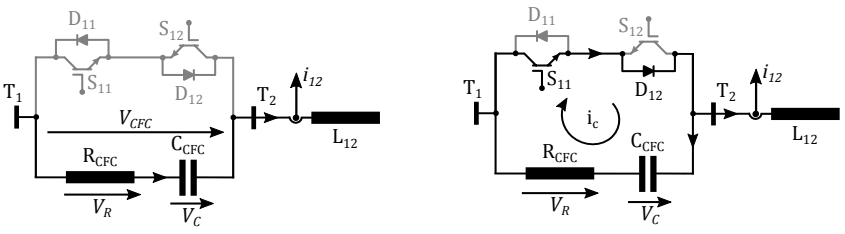


Figure 3.7: RC-CFC under by-pass mode.

3.3.2 Current control mode

In the CC mode, switch S_{11} is modulated to provide the required series dc voltage for current control. The operational modes and switching waveforms of the RC-CFC during the CC mode are shown in Figs. 3.8 and 3.9, respectively. When switch S_{11} is off, as shown in Fig. 3.8(a), the line current flows through the RC circuit and charges the capacitor. During this period a positive voltage is inserted between terminals T_1 and T_2. Thus, line current i_{12} decreases. When switch S_{11} is on, as shown in Fig. 3.8(b), the line current follows through switch S_{11} and diode D_{12}, where the inserted voltage is zero. As a result of capacitor discharge, a circulating current, i_c, flows between the RC circuit and switch B_1 during this period. The capacitor voltage V_C and the inserted voltage V_{CFC} can be represented by the following equations.



(a) Off-state (b) On-state

Figure 3.8: Operational stages of RC-CFC under CC mode.

When switch S_{11} is off:

$$V_{\text{CFC,off}} = (\overline{V}_{\text{C}} + V_{\text{R,off}}) = \overline{V}_{\text{C}} + i_{12} \cdot R_{\text{CFC}} \tag{3.3}$$

where $V_{\text{R,off}} = i_{12} \cdot R_{\text{CFC}}$; and $\overline{V}_{\text{C}}$ is the average value of capacitor voltage V_{C}.

When switch S_{11} is on:

$$\begin{aligned} V_{\text{CFC,on}} &= 0 \\ i_{c,on} &= \frac{\overline{V}_{\text{C}}}{R_{CFC}} \end{aligned} \tag{3.4}$$

Therefore, the average inserted dc voltage $\overline{V}_{\text{CFC}}$:

$$\begin{aligned} \overline{V}_{\text{CFC}} &= \frac{V_{\text{CFC,off}} \cdot T_{\text{off}} + V_{\text{CFC,on}} \cdot T_{\text{on}}}{T_{\text{s}}} \\ \overline{V}_{\text{CFC}} &= \frac{(\overline{V}_{\text{C}} + i_{12} \cdot R_{\text{CFC}}) T_{\text{off}}}{T_{\text{s}}} \\ \overline{V}_{\text{CFC}} &= (\overline{V}_{\text{C}} + i_{12} \cdot R_{\text{CFC}})(1 - D) \end{aligned} \tag{3.5}$$

where D is the duty cycle of switch S_{11} and $D = \frac{T_{\text{on}}}{T_{\text{s}}}$.

During the steady state operation, the capacitor charge and discharge voltages must be equal. Therefore:

$$\begin{aligned} \frac{i_{12} \cdot T_{\text{off}}}{C_{\text{CFC}}} &= \frac{i_{c,on} \cdot T_{\text{on}}}{C_{\text{CFC}}} \\ i_{12}(1 - D) &= i_{c,on} \cdot D \end{aligned} \tag{3.6}$$

$$\begin{aligned} i_{12}(1 - D) &= \frac{\overline{V}_{\text{C}}}{R_{\text{CFC}}} \cdot D \\ \overline{V}_{\text{C}} &= i_{12} \cdot R_{\text{CFC}} \cdot \frac{(1 - D)}{D} \end{aligned} \tag{3.7}$$

where $V_R = i_{12} \cdot R_{CFC}$

By substituting $i_{12} \cdot R_{CFC}$ from eq. (3.7) into eq. (3.5):

$$\begin{aligned} \overline{V}_{CFC} &= (\overline{V}_C + \frac{\overline{V}_C \cdot D}{1-D})(1-D) \\ \overline{V}_{CFC} &= \overline{V}_C \end{aligned} \tag{3.8}$$

Therefore, in steady state, the inserted average series dc voltage $\overline{V}_{CFC}$ is equal to average capacitor voltage $\overline{V}_C$.

The peak-to-peak capacitor ripple voltage Δ_p can be calculated as follows:

$$\begin{aligned} \Delta_p &= i_{12} \cdot \frac{T_{off}}{C_{CFC}} \\ &= \frac{\overline{V}_C}{R_{CFC}} \cdot T_{on} \end{aligned} \tag{3.9}$$

As shown in eq. (3.9), the ripple on the CFC capacitor voltage is determined by the sizes of the capacitor C_{CFC}, resistor R_{CFC} and the switching frequency. The ripple can be reduced by increasing the size of either C_{CFC} or R_{CFC}. However, the use of a large resistor could increase the device voltage rating whereas the use of a large capacitor could lead to slower current control. Alternately, ripple can be reduced by increasing the switching frequency (i.e. reducing T_s). At higher switching frequencies, the power losses increase due to larger number of constant-energy-switching events per time. The ripple magnitude can be optimised by doing a trade-off between C_{CFC}, R_{CFC} and the switching frequency.

Fig. 3.10 presents the control system of the RC-CFC. The output of the current controller generates the duty cycle of the controlled switch. A first order filter with a cut-off frequency of 200 Hz is employed to eliminate the noise and high frequency components from the measured line current. The required capacitor voltage is determined by the amount of current reduction or increment required. Since the initial voltage across the capacitor is zero, the PI controller would adjust the initial duty cycle of switch S_{11} to zero. This could lead to overvolatge across the capacitor as the line current flows through it and rapidly charges it. A feedback compensation loop with a gain of K_f is used to limit the overshoot in capacitor voltage during the start-up by adjusting the initial duty cycle above zero.

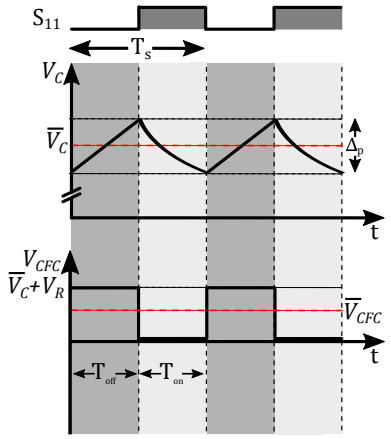


Figure 3.9: Switching waveforms.

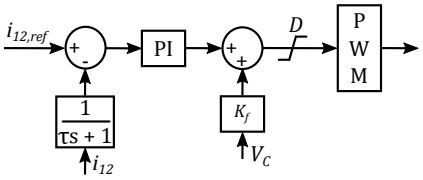


Figure 3.10: RC-CFC line current controller.

3.4 Capacitive based CFC (C-CFC)

R-CFC and RC-CFC exhibit higher power losses as the current control is provided through energy dissipation on a series connected resistor. Alternatively, the power losses can be minimised via exchanging the energy between dc lines. Fig. 3.11 shows the solid state switches arrangement of a capacitive CFC (C-CFC) derived from a RC-CFC. The device comprises two power electronic switches (B_1 and B_2) and a capacitor. Capacitor, C_{CFC}, is electrically coupled between switches B_1 and B_2. A dc voltage is established on the capacitor in order to provide a voltage source for the current flow control.

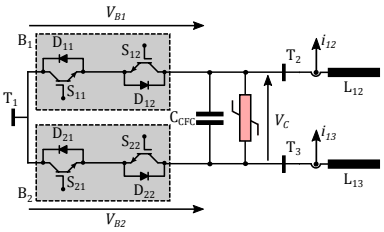


Figure 3.11: Capacitive based CFC.

3.4.1 By-pass mode

Let assume that current flows from T_1 to T_2 and from T_1 to T_3. As shown in Fig. 3.12, when the required current adjustment is zero, the CFC is by-passed through activating switches S_{11} of B_1 and S_{21} of B_2.

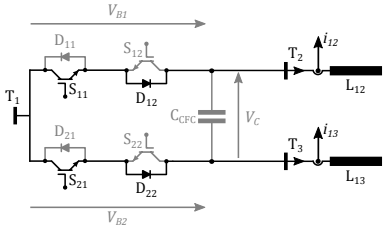


Figure 3.12: C-CFC under by-pass mode.

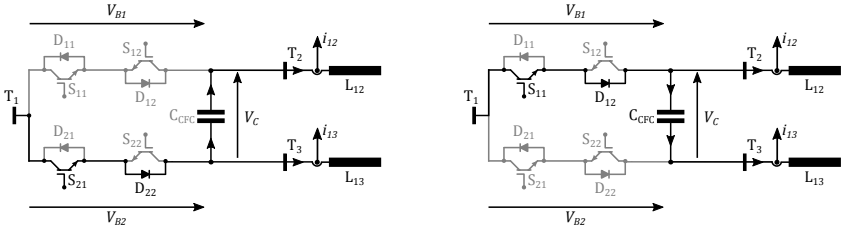
3.4.2 CC mode

During the CC mode, as shown in Figs. 3.13(a) and 3.13(b), the CFC is switched between two different operational modes. Switches S_{11} and S_{21} must be switched complementarily to avoid any discontinuity in line current. When switch S_{11} is off (i.e. S_{21} is on), a part of the converter current flows through the capacitor and charges it rapidly. Thus, a positive voltage V_C is inserted in series with dc line L_{12} (see Fig. 3.14). Since switch B_2 is in by-pass mode, the inserted voltage in series with line L_{13} is equal to zero. In order to maintain the power balance, the stored energy on the capacitor must be discharged into line L_{12} by turning on switch S_{11}. As a result of a negative voltage insertion $-V_C$ in series with line L_{13}, current i_{12} decreases while i_{13} increases to maintain the power balance. As shown in Fig. 3.14, continuous switching of S_{11} and S_{21} generates mean positive (V_{B1}) and negative (V_{B2}) dc voltages across the CFC terminals T_1 and T_2, and T_1 and T_3, respectively. This increases i_{13} and also decreases i_{12}.

During the CC mode, inserted dc voltages V_{B1}, and V_{B2} can be defined by the following equations:

When switch S_{11} is off:

$$\begin{aligned} V_{\text{B1,off}} &= \overline{V}_{\text{C}} \\ V_{\text{B2,off}} &= 0 \end{aligned} \tag{3.10}$$



(a) Charge (b) Discharge

Figure 3.13: Operational stages of C-CFC under CC mode.

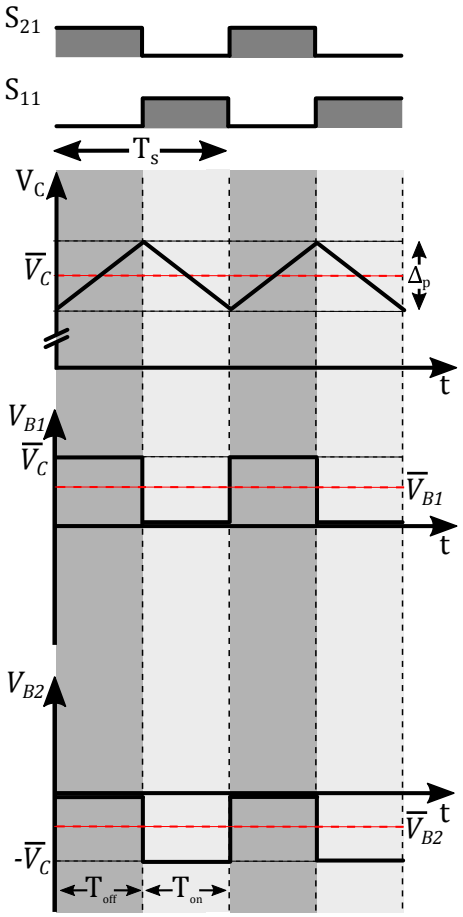


Figure 3.14: Switching waveforms.

When switch S_{11} is on:

$$\begin{aligned} V_{\mathrm{B1,on}} &= 0 \\ V_{\mathrm{B2,on}} &= -\overline{V}_{\mathrm{C}} \end{aligned} \tag{3.11}$$

The average values of bridge voltages V_{B1} and V_{B2} can be given by the following equations:

$$\begin{aligned} \overline{V}_{\mathrm{B1}} &= \frac{V_{\mathrm{B1,off}} \cdot T_{\mathrm{off}} + V_{\mathrm{B1,on}} \cdot T_{\mathrm{on}}}{T_{\mathrm{s}}} \\ \overline{V}_{\mathrm{B1}} &= \frac{\overline{V}_{\mathrm{C}} \cdot T_{\mathrm{off}}}{T_{\mathrm{s}}} = \overline{V}_{\mathrm{C}}(1-D) \end{aligned} \tag{3.12}$$

$$\begin{aligned} \overline{V}_{\mathrm{B2}} &= \frac{V_{\mathrm{B2,off}} \cdot T_{\mathrm{off}} + V_{\mathrm{B2,on}} \cdot T_{\mathrm{on}}}{T_{\mathrm{s}}} \\ \overline{V}_{\mathrm{B2}} &= \frac{-\overline{V}_{\mathrm{C}} \cdot T_{\mathrm{on}}}{T_{\mathrm{s}}} = -\overline{V}_{\mathrm{C}} \cdot D \end{aligned}$$

where D is the duty cycle of switch S_{11} and $D = \frac{T_{\mathrm{on}}}{T_{\mathrm{s}}}$.

In this configuration, the power taken from one line is equal to the power added to the other line. The power balancing between switches B_1 and B_2 can be represented by the following equations:

$$\begin{aligned} \overline{V}_{\mathrm{B1}} \cdot i_{12} + \overline{V}_{\mathrm{B2}} \cdot i_{13} &= 0 \\ s \cdot \overline{V}_{\mathrm{C}}(1-D) i_{12} - s \cdot \overline{V}_{\mathrm{C}} \cdot D \cdot i_{13} &= 0 \end{aligned} \tag{3.13}$$

where $s = \begin{cases} 1 \\ -1 \end{cases}$

In eq. (3.13), s determine the polarity of the injected series voltages where their polarities should be opposite to maintain the power balance.

The peak-to-peak capacitor ripple voltage Δ_p can be expressed as follows:

$$\begin{aligned} \Delta_p &= i_{12} \cdot \frac{T_{\mathrm{off}}}{C_{\mathrm{CFC}}} \\ &= i_{13} \cdot \frac{T_{\mathrm{on}}}{C_{\mathrm{CFC}}} \end{aligned} \tag{3.14}$$

Unlike in the R-CFC and RC-CFC, the voltage across the capacitor in a C-CFC must be limited as the capacitor charges and discharges periods are solely determined by small a dc line impedance. The main control objective is to regulate the line current via maintaining the voltage across the capacitor within a safer limit. Therefore, employment of a single loop current controller could

result in an overvoltage across the CFC capacitor. This can be resolved by introducing a nested control scheme as shown in Fig. 3.15. The nested control system consists of an inner-loop voltage controller and an outer-loop current controller. The outer current controller regulates the line current via setting the required capacitor voltage value. A low pass filter with a cut-off frequency of 200 Hz is employed to eliminate the noises from the measurements.

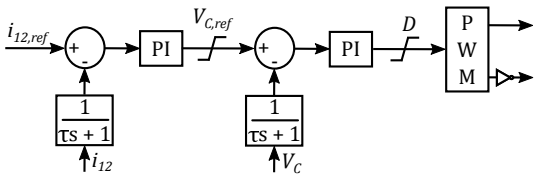


Figure 3.15: C-CFC line current controller.

Fig. 3.16 shows the switching combination of switches B_1 and B_2 under current control. Switching patterns are provided for four quadrant operation, where the quadrants are defined by the direction of the line currents.

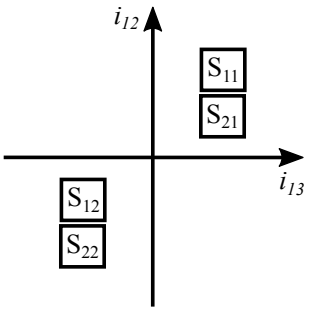


Figure 3.16: C-CFC switching selection.

The operation of a C-CFC is limited to two quadrants (1 and 3) as capacitor discharge is unattainable when line currents are in opposite directions. Therefore, the device cannot be operated in quadrants 2 and 4 as capacitor discharge is only achievable through turning on both switches B_1 and B_2 which results in a short circuit.

When currents through CFC bypass switches are in opposite direction, the CFC will be bypassed to protect the modules against short circuit current. In an event of cable overloading in quadrants 2 and 4, the C-CFC cannot be used to maintain the cable current below its thermal limit. The lack of controllability of the C-CFC may be relieved by the installation of multiple devices

Table 3.1: Coordination of multiple CFCs

i_{12}	i_{13}	i_{23}	CFC 1	CFC 2	CFC 3
p	p	p	C	C	NC
n	n	n	C	C	NC
p	p	n	C	NC	C
n	n	p	C	NC	C
p	n	p	NC	C	C
n	p	n	NC	C	C

which may be afforded due to its low cost and small footprint. Fig. 3.17 shows the schematic diagram of a three-terminal meshed dc grid with three C-CFCs. The current flow reference directions are shown by the black arrows. Table 3.1 summarises the state of each CFC with respect to the changes in line current directions (p-positive and n-negative). The notations 'C' and 'NC' in Table 3.1 represent control and no-control states, respectively. For each line current combination, at least one CFC is available to provide the required current control.

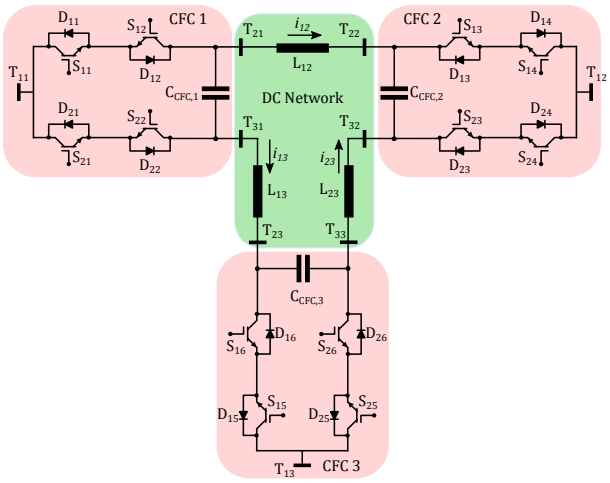
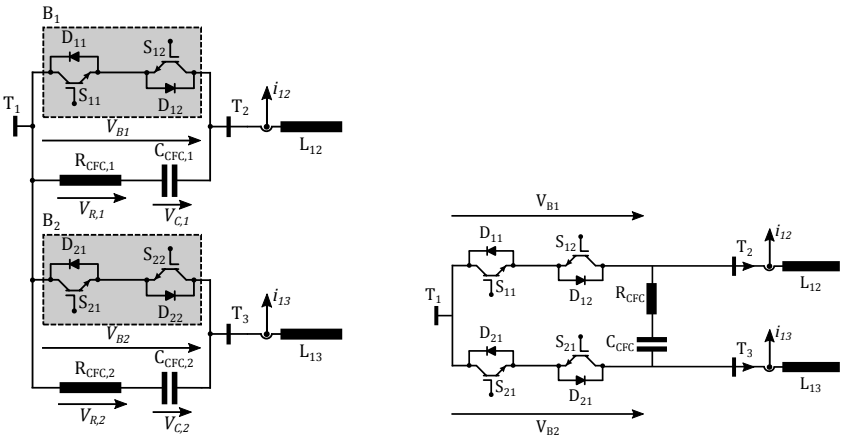


Figure 3.17: DC grid with multiple CFCs.

3.4.3 Hybrid CFCs

3.4.3.1 RC based hybrid CFC

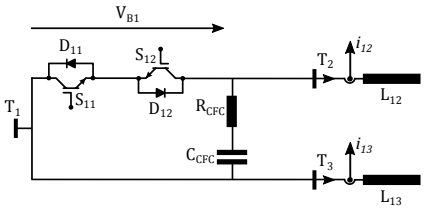
A C-CFC can be used to either increase or decrease dc line current. Conversely, R or RC-CFCs are only capable of achieving line current reduction. To overcome this issue, each line must be employed with a CFC. In the arrangement, as shown in Fig. 3.18(a), current on i_{12} can be increased by decreasing the current on i_{13} or vice versa. The RC circuits ends of CFCs 1 and 2 are connected to a common terminal (T_1) whereas their other ends are connected to terminals T_2 and T_3, respectively. Since only a single CFC is active at a given point of time, the CFCs could share a common RC circuit. This is shown in Fig. 3.18(b). In this configuration, a RC-CFC can be inserted in series with lines L_{12} (Fig. 3.19(a)) or L_{13} (Fig. 3.19(b)) by turning on switches B_1 or B_2, respectively.



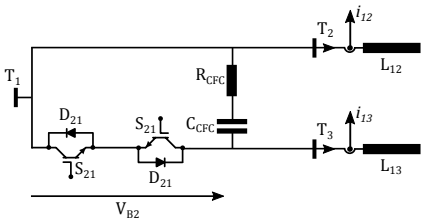
(a) Two de-coupled RC-CFCs (b) Two coupled CFCs

Figure 3.18: Reduced RC CFC.

As discussed before, a RC-CFC offers four quadrant operation at the expense of high power losses. On the other hand, a C-CFC offers lower power losses but lacks the four quadrant operation capability. To utilise the best of both CFC configurations, a hybrid CFC is proposed (Fig. 3.20). The device consists of two electrically coupled anti-series connected IGBTs and a RC circuit. The device can be operated as a C-CFC in quadrants 1 and 3 through by-passing resistor R_{CFC} using a bidirectional switch T_s. Thus, power losses are minimised. The switch T_s can be realised through two anti-parallel connected integrated gate-commutated thyristor (IGCT) switches



(a) voltage injection in series to line L_{12}



(b) voltage injection in series to line L_{13}

Figure 3.19: Voltage injections in coupled RC CFC.

which offer lower conduction losses compared to IGBTs. The CFC operation can be extended to quadrants 2 and 4, through transforming the C-CFC into a RC-CFC by blocking switch T_s.

Fig. 3.21 shows the states of CFC switches under current control. Switching patterns are provided for four quadrant operation, where the quadrants are defined by the direction of the line currents.

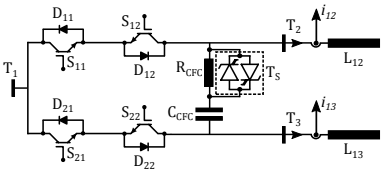


Figure 3.20: Hybrid CFC.

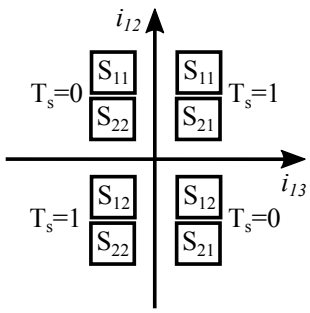


Figure 3.21: Hybrid CFC switching selection.

3.4.3.2 DCCB based hybrid CFC

As discussed in Chapter 2, a FB-MMC has the inherent advantage of blocking the dc fault compared to a HB-MMC. However, the FB-MMC exhibits twice the power losses of a HB-MMC in normal operation due to additional solid state switches. Therefore, HB-MMCs offer a better solution in terms of power losses and investment cost compared to FB MMCs. In presence of HB-MMC converters, DCCBs are required to isolate a dc fault. In recent years, there have been many research activities on the design and development of HVdc DCCBs. Among the proposed DCCB topologies, a hybrid CFC can be realised using either a solid state DCCB or hybrid DCCB as they consist semiconductor switches. However, the use of solid state breaker is not economical as it exhibit high on state power losses [80]. In contrast, the hybrid DCCB offers a better solution compared to solid state DCCB as the conduction losses are minimised through the use of a ultrafast disconnector (UFD) [39]. However, they are expensive than solid state breakers. It must be emphasized that the mechanical DCCB presented in [38], cannot be used to realise a hybrid CFC due to the absence of semiconductor switches such as LCS branch or main circuit breaker branch.

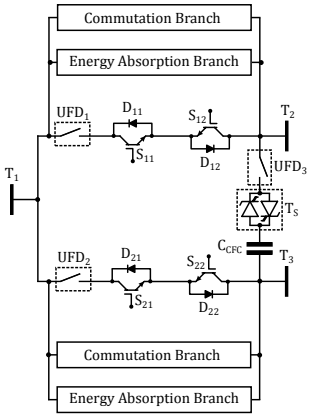


Figure 3.22: Hybrid DCCB based CFC.

Fig. 3.22 shows an alternative CFC topology where the DCCB's load commutation switches are utilised to provide current control. A branch of a capacitor in series with a bi-directional switch (T_s) and an ultrafast disconnector (UFD_3) is connected between the DCCBs. In this configuration, switch T_s is realised through two anti-parallel connected IGCT switches to minimise the conduction losses. They are assumed to have similar turn-on and turn-off speeds as IGBTs.

During a fault, switch T_s and disconnector UFD_3 electrically decouple the DCCBs and block the fault current through the CFC capacitor. Switch T_s and disconnector UFD_3 should have the same power ratings as their breaker counter parts, where UFD_3 must able to withstand the potential difference of pole to ground voltage. It must be highlighted that since LCSs are utilized for control purpose, continuous modulation of these switches could reduce their expected life cycle.

In this chapter, only the concept of hybrid CFC is introduced. A detailed study on operation and control of hybrid CFCs are non-trivial tasks which goes beyond the scope of this thesis. This is considered as a potential future work.

3.5 Simulation and Experimental Validation

The performance of R, RC and C-CFCs have been validated through simulations and experiments using a hardware platform. The three-terminal dc grid equipped with CFCs has been modeled in Simulink/SimPowerSystems.

3.5.1 MTdc Control and Configuration

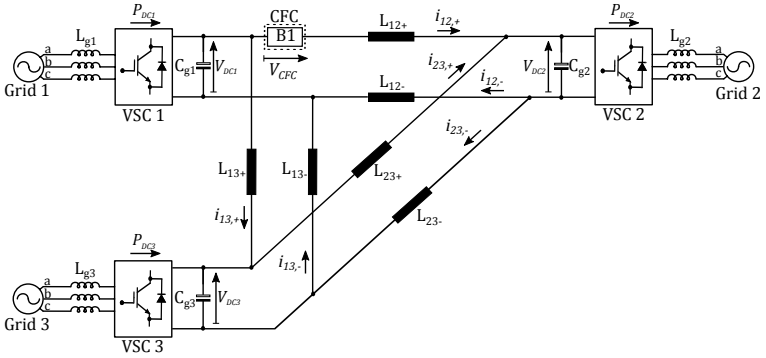
The three-terminal meshed MTdc grid shown in Fig. 3.23 is used to validate the operation and control of the proposed CFCs. The VSC terminals have been arranged in a symmetrical monopole configuration and rated at ±125 V and 2 kW. The location of the R and RC-CFCs is shown in Fig. 3.23(a) and of the C-CFC in Fig. 3.23(b). The C-CFC modules B_1 and B_2 are installed in series with the positive pole of lines L_{12} and L_{13}, respectively. A master-slave control scheme for VSCs has been adopted to maintain the grid power balance [3]. Fig. 3.24 shows the VSC control strategy. It uses a classical *dq* reference frame scheme to regulate the dc voltage or active and reactive power.

3.5.2 Experimental Set-up

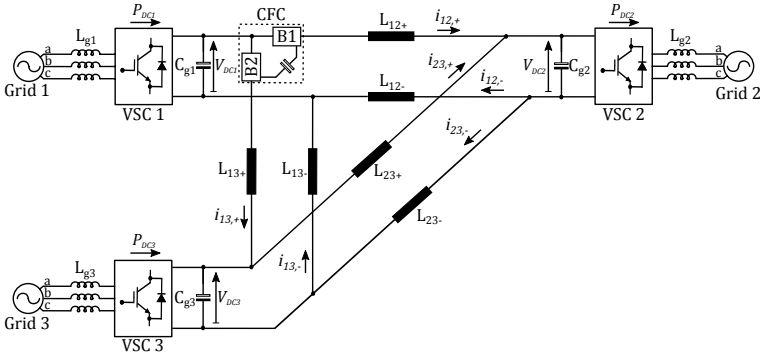
Fig. 3.25 shows the experimental setup of the MTdc test-rig with embedded CFC modules. Each VSC is connected to an ac system through a phase reactor and a transformer. Autotransformers connected to the 415 V ac power supply represent the ac grids. The dc cables are represented by emulated RL sections. A dSPACE DS1005 system is used to control the test-rig. Simulink-based real-time interface control blocks are used to implement the control scheme. Real-time operation is enabled through the ControlDesk 3.2 graphical user interface. The specifications and parameters for the test-rig and the CFCs are provided in Tables 3.2 and 3.3.

3.5.3 Results and Analysis

The results in this section are expressed in per unit considering the following power, voltage and current bases: 2 kW, 125 V, and 8 A. VSCs 1 and 3 are initially set to inject 0.8 and 0.2 p.u. into the MTdc grid, whereas VSC 2 has been designated as a slack busbar that maintains the grid power



(a) MTdc with embedded R/RC CFC

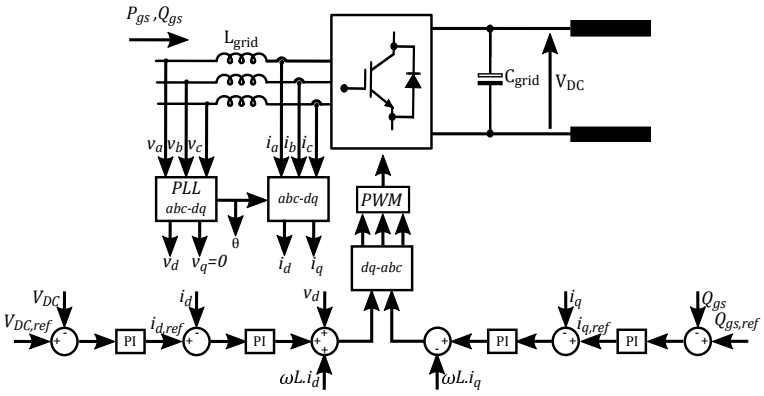


(b) MTdc with embedded C CFC

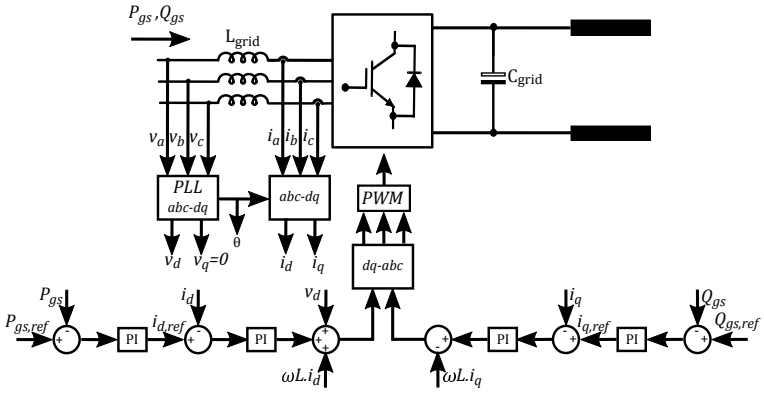
Figure 3.23: 3-terminal test system with embedded CFC module.

Table 3.2: Specifications and parameters of the test-rig

Devices	Specifications	Operating Rating
VSCs	Rated power	2 kW
	Rated ac voltage	140 V
	Rated dc voltage	250 V
	Topology	Two-level symmetrical monopole
AC inductors	L_{g1}, L_{g2}, L_{g3}	2.2 mH
DC lines	L_{12}	2.4 mH
	L_{13}	5.8 mH
	L_{23}	11.8 mH
	Equivalent R_{12}	0.045 Ω
	Equivalent R_{13}	0.68 Ω
	Equivalent R_{23}	0.18 Ω
DC capacitors	C_{g1}, C_{g2}, C_{g3}	1020 μF
Control system	dSPACE DS1005 / ControlDesk 3.2(Simulink interface)	



(a) Master control



(b) Slave control

Figure 3.24: Master-slave control scheme.

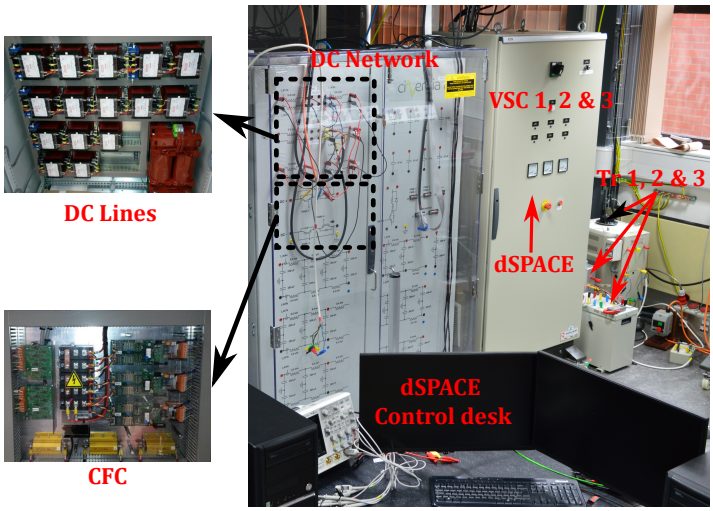


Figure 3.25: Experimental setup.

Table 3.3: Specifications and parameters of CFCs

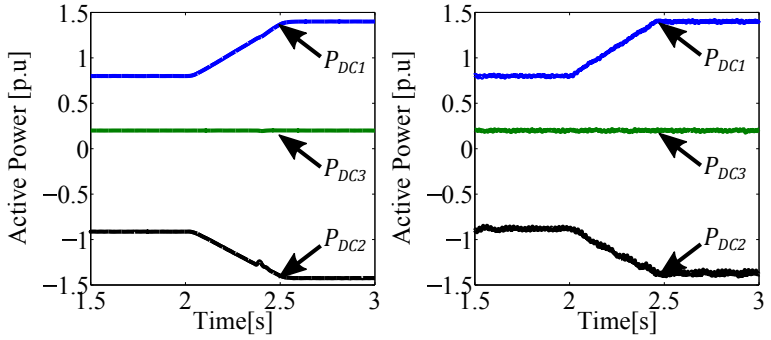
Devices	Specifications	Operating rating
CFC	rated power rated dc voltage topology	120W 15 V R-CFC, RC-CFC and C-CFC
DC capacitor	C_{CFC}	4400 μF
Resistor	R_{CFC}	1.2 Ω
Switching frequency	f_{sw}	2000 Hz
Control system	dSPACE DS 1005 / ControlDesk 3.2(SIMULINK interface)	

balance (*i.e.*, maintains a constant dc voltage).

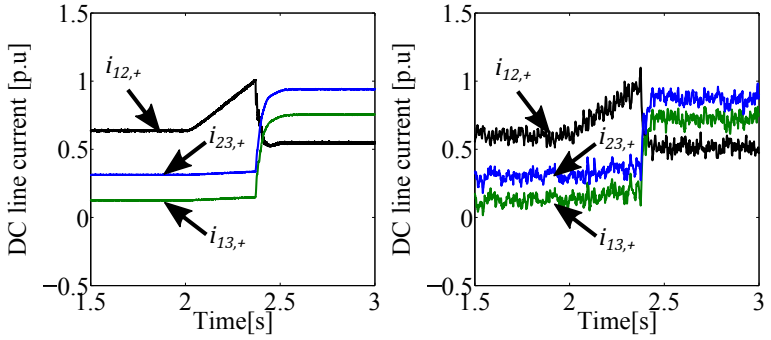
3.5.3.1 Line overload elimination using R-CFC

This test case evaluates the performance of a R-CFC under a line overloading condition. A 1.2Ω resistor is used to provide the required series dc voltage injection. Initially, the CFC is by-passed by setting the duty cycle of switch B_1 to 1. The simulation (left) and experimental results (right) of the dc response and CFC dynamics are shown in Figs. 3.26 and 3.27. At $t = 2$ s, as a result of an increase in grid 2 power demand , VSC 1 is requested to inject an additional power of 0.6 p.u. into the dc grid. This has led dc line L_{12} to carry excess current and become overloaded. A control system, as shown in Fig. 3.28, is designed to provide the series voltage injection only if the line current where the CFC is installed is above 1 p.u. (i_{th}). The local measurements are used to detect the line overload. Following the overload detection, the CFC is requested to bring down line current i_{12} to 0.5 p.u ($i_{12,ref}$) to achieve a better line current distribution. During the CC mode, the CFC has reached its maximum control limit; i.e. duty cycle of 0 before achieving the requested current reduction. As it can be seen from Fig. 3.26(b), line current $i_{12,+}$ has reached a new steady state value of 0.55 p.u., which is 0.05 p.u. above the reference point. A constant dc voltage, as shown in Fig. 3.27, is observed across the CFC terminals in contrast of pulsed dc voltage as the CFC reaches its maximum control limit.

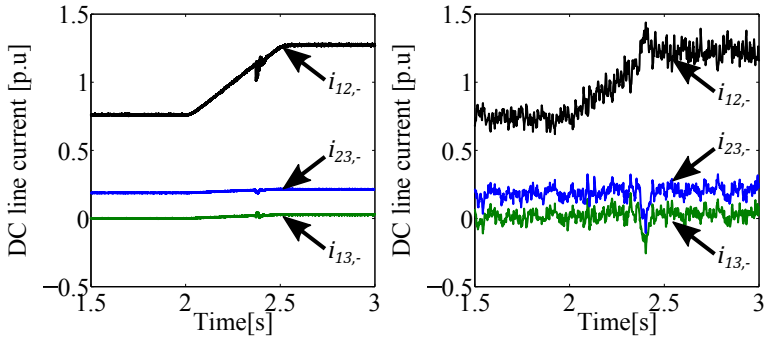
In this test cases, the CFC current reference is set to 0.5 p.u. In general, a CFC is used to maintain the line current of a given line at or below the 1 p.u. mark. However, it should be highlighted that in scaled systems such as in the experimental test-rig shown in Fig. 3.23(a), the forward voltage



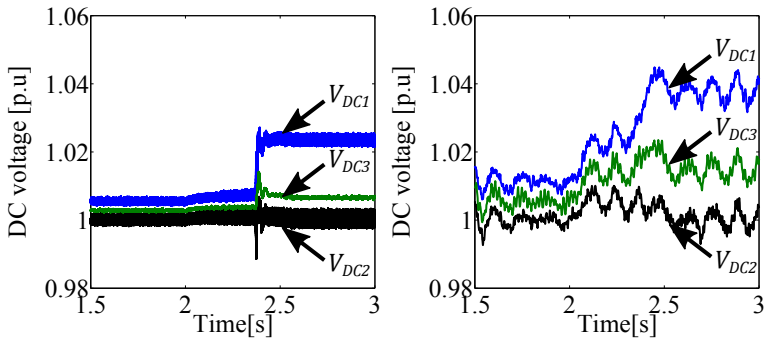
(a) VSC active power



(b) DC line current (positive pole)



(c) DC line current (negative pole)



(d) DC terminal voltage

Figure 3.26: DC grid response for a ramp change in power with embedded R-CFC: Simulation (left) and experimental (right) results

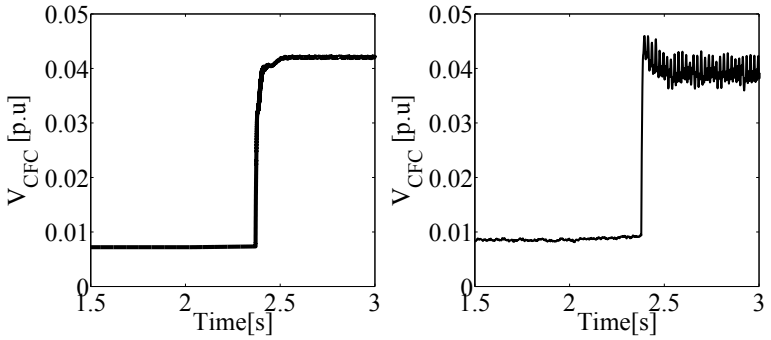


Figure 3.27: Response of the R-CFC located at the positive pole for a ramp change in power: Simulation (left) and experimental (right) results

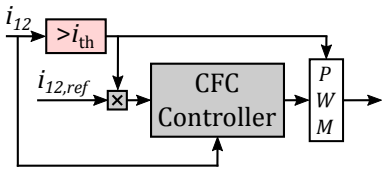


Figure 3.28: Overload detection controller.

drop on semiconductor switches affects the current flow between electrical nodes. For example, during the capacitor charging and discharging modes of a C-CFC, a diode with a forward voltage drop between 0.8-1 V, is inserted into the conduction path. The capacitor voltage required to achieve an optimum line current distribution may be very small and of a magnitude similar to the diode's forward voltage drop. Therefore, to build enough voltage across the capacitor and to experimentally demonstrate the CFC performance, a large current reduction must be achieved. To maintain the consistency between test cases, current references are set to 0.5 p.u. in all test cases, but this value may be just below 1 p.u. mark in a real system. For example, Fig. 3.29 shows the overload elimination on line L_{12} in a real system. Between $t = 1.5-2$ s, the line is overloaded. Following the overload detection via a control system as shown Fig. 3.28, line current, i_{12}, is reduced to 1 p.u. It must be emphasized that the remote control centre as proposed in Chapter 6 could be used to determine the optimal CFC current references to achieve the best line current distribution in complex dc grids so that grid power losses are minimized.

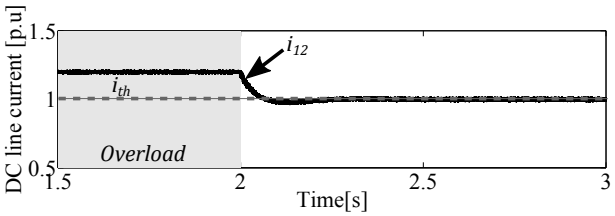
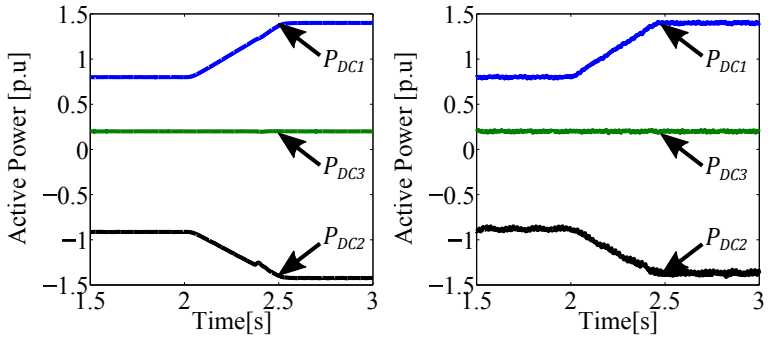


Figure 3.29: Overload elimination in real system.

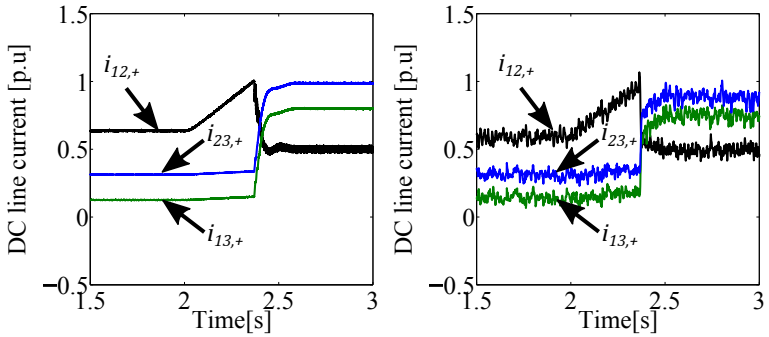
3.5.3.2 Line overload elimination using RC-CFC

A 4.4 mF capacitor is connected in series with the 1.2 Ω resistor to increase the controllability. The device line overload detection and elimination capability is demonstrated under the same condition as the R-CFC. The CFC is placed in series with line L_{12}. Initially the CFC is bypassed through switch S_{11} and diode D_{12} of B_1. As shown in Fig. 3.30(b), after the ramp power change (Fig. 3.30(a)) at $t = 2$ s, line current i_{12} has surpassed the maximum thermal current limit of 1 p.u. In order to protect the cable from thermal break down and to achieve a better line current distribution, the CFC is requested to bring down the line current to 0.5 p.u. The required series dc voltage for current control is provided by the RC circuit by generating a positive mean dc voltage (Fig. 3.31(b)) in series with line L_{12}. During the CC mode, a positive dc voltage, V_C, as shown in Fig. 3.31(a), is observed across the capacitor with small ripples. The introduction of a series capacitor has increased the controllability of the R-CFC by providing the additional series dc voltage for current control.

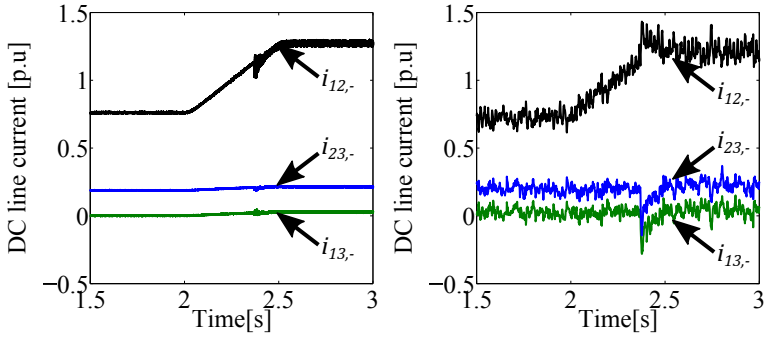
The controllability of R and RC-CFCs is further investigated by ramping down the duty cycle from 1 to 0. Fig. 3.32 shows the amount of line current reduction as a function of the control ratio for R-CFC and RC-CFC. A control ratio of 1 (duty cycle of 0) represents the maximum series dc voltage injection where the device is saturated. A control ratio of 0 (duty cycle of 1) stands for zero dc voltage injection where the CFC is by-passed. The addition of a series capacitor has increased the controllability of the R-CFC by a factor Δ_1 =0.685 p.u where the capacitor is used to provide the additional series voltage injection.



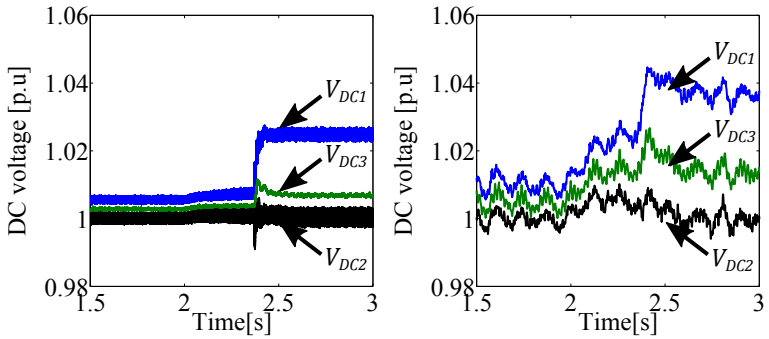
(a) VSC active power



(b) DC line current (positive pole)

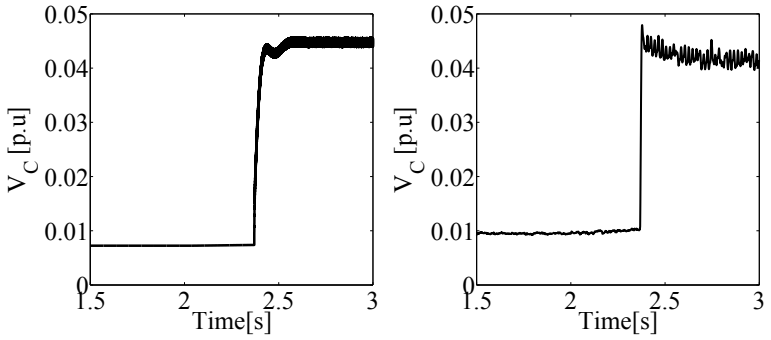


(c) DC line current (negative pole)

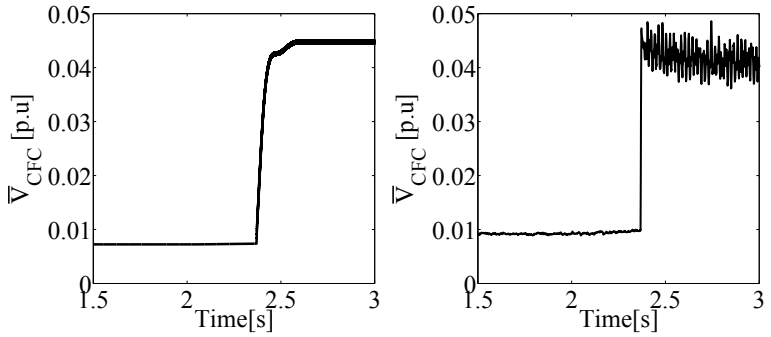


(d) DC terminal voltage

Figure 3.30: DC grid response for a ramp change in power with embedded RC-CFC: Simulation (left) and experimental (right) results



(a) Capacitor voltage



(b) Inserted mean dc voltages

Figure 3.31: Response of the RC-CFC located at the positive pole for a ramp change in power: Simulation (left) and experimental (right) results

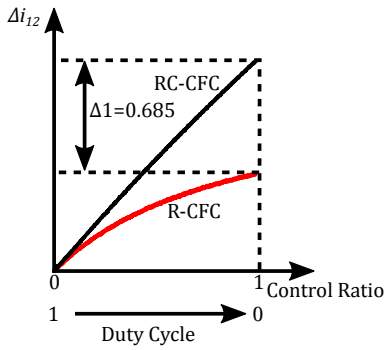


Figure 3.32: R-CFC and RC-CFC controllability.

3.5.3.3 Line overload elimination using C-CFC

In this test case, a C-CFC is used to avoid line overloading following a ramp change in power. Initially, the CFC is by-passed through stetting the duty cycles of switches B_1 and B_2 to 1. The overloading condition is achieved through changing the power reference of VSC 1 from 0.8 p.u. to 1.4 p.u. at $t = 2$ s. The dc grid responses are shown in Fig. 3.33. As a result of additional

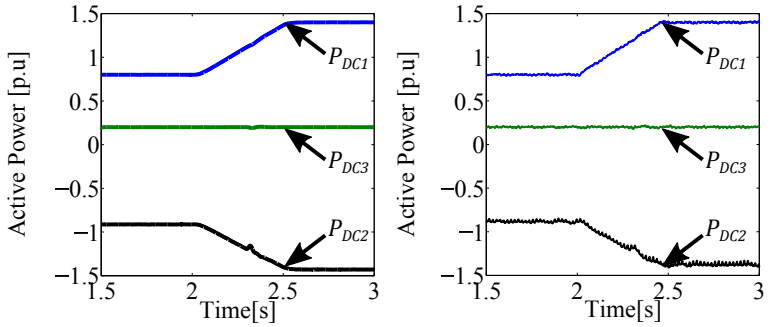
power injection, line currents i_{12+} and i_{12-} have surpassed the permissible thermal line current threshold. The line current i_{12+} is brought down to a safer level i.e. 0.5 p.u. by enabling the CFC. It must be noted that since there is no CFC on the negative pole, as shown in Fig. 3.33(c), line $L_{12,-}$ remains overloaded. During the CC mode, as shown in Fig. 3.33(d), VSCs 1 and 3 have adjusted their terminal voltages to compensate for the effects of CFCs while terminal 2 voltage remains constant.

During the current reduction, capacitor voltage V_C is maintained at 0.04 p.u. As shown in Fig. 3.34(b), mean dc voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$, are inserted in series with lines L_{12} and L_{13}, respectively. The actual inserted pulsed dc voltages are shown in Fig. 3.35. Unlike R and RC-CFCs, during CC mode, power is transferred from line L_{12} to L_{13}.

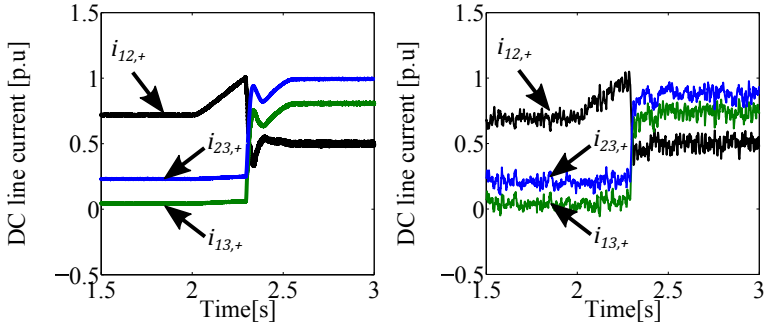
3.5.3.4 DC line isolation

In HVdc grids, the dc cables or OHLs must be periodically examined and maintained to avoid deterioration. During the maintenance or decommissioning of a dc cable, the cable must be isolated from rest of the grid. This can be achieved by opening the DCCBs and mechanical isolation switches of the line which must be isolated. However, in presence of FB-MMC based dc grids, all converters must be blocked to isolate a dc line as they lack the ability to isolate dc lines individually. Therefore, dc line maintenance by blocking converters is not only expensive but could jeopardise grid stability. Alternatively, a line can be isolated by reducing the line current to zero using a CFC and opening the mechanical isolation switches. To achieve zero line current, the CFC must have a capacitive element such as RC or C-CFCs.

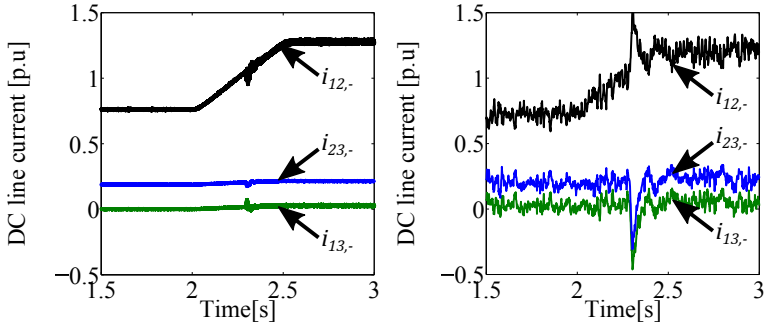
In this test case, an RC-CFC is adopted to isolate the dc line. Figs. 3.36 and 3.37 show the dc grid response and the CFC voltage profiles, respectively. Initially, the CFC is by-passed via activating switch B_1. At $t = 2$ s, the CFC is requested to isolate line L_{12} by turning off switch S_{11}. During the CC mode, i_{12} has reached zero while line currents i_{13} and i_{23} have increased to maintain the grid power balance. The voltage observed across the capacitor (or CFC) is equal to the voltage difference between VSCs 1 and 2. The results have proved that a CFC with series connected capacitive element can be used to isolate a particular dc line without interrupting dc grid operation.



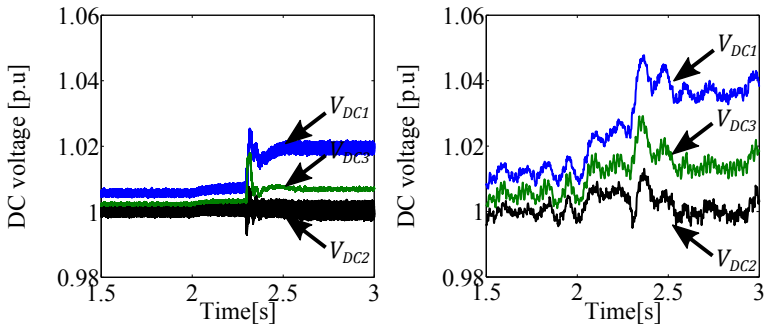
(a) VSC active power



(b) DC line current (positive pole)

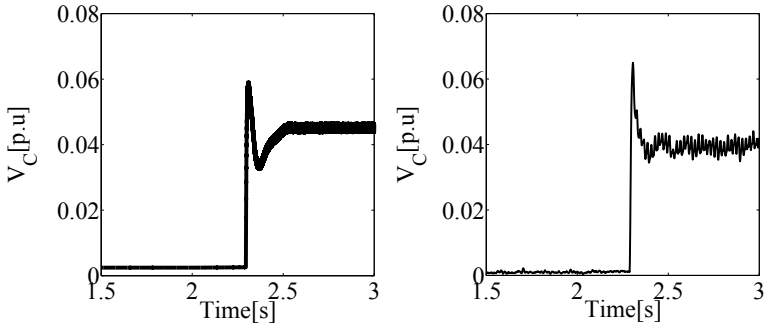


(c) DC line current (negative pole)

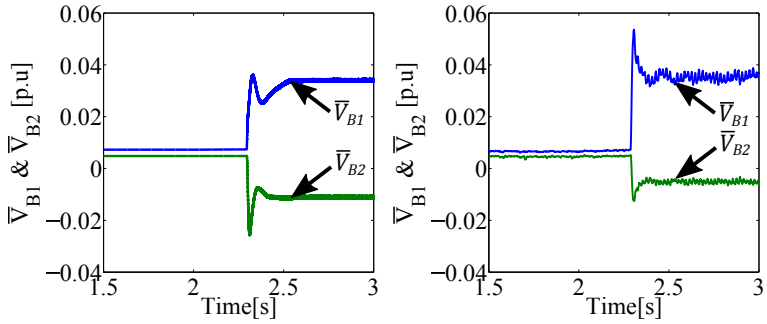


(d) DC terminal voltage

Figure 3.33: DC grid response for a ramp change in power with embedded C-CFC: Simulation (left) and experimental (right) results



(a) Capacitor voltage



(b) Inserted mean dc voltages

Figure 3.34: Response of the C-CFC located at the positive pole for a ramp change in power: Simulation (left) and experimental (right) results

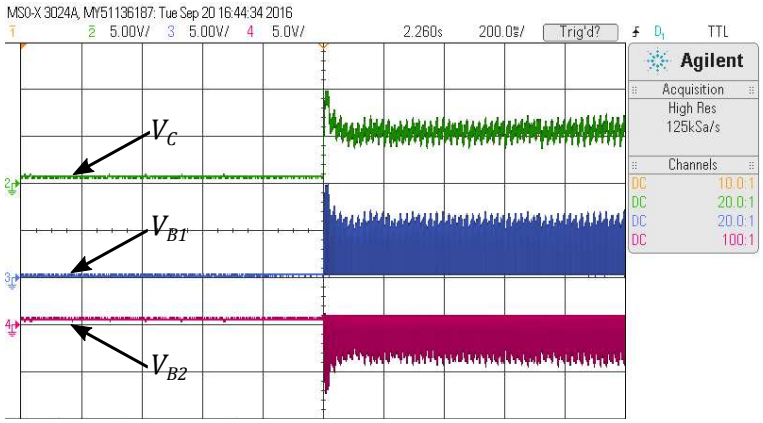
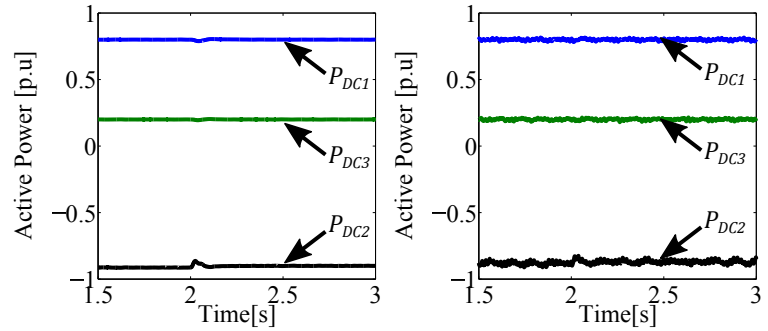
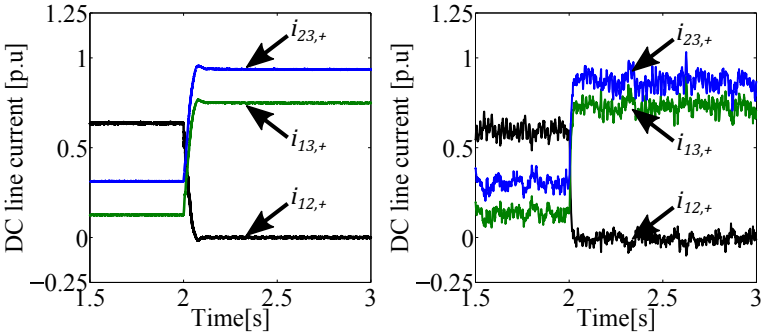


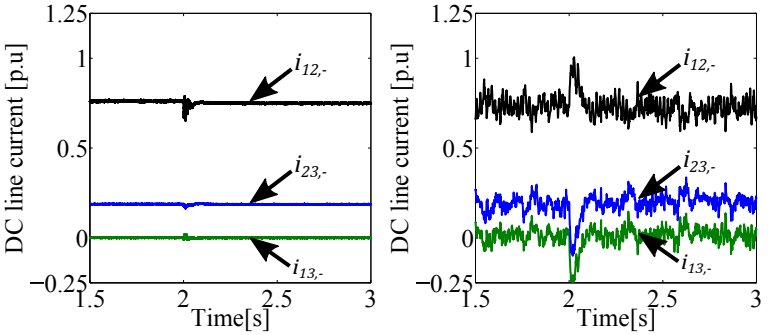
Figure 3.35: C-CFC dynamics under positive ramp power change (voltage axis is 5 V/division and the time axis is 200 ms/division).



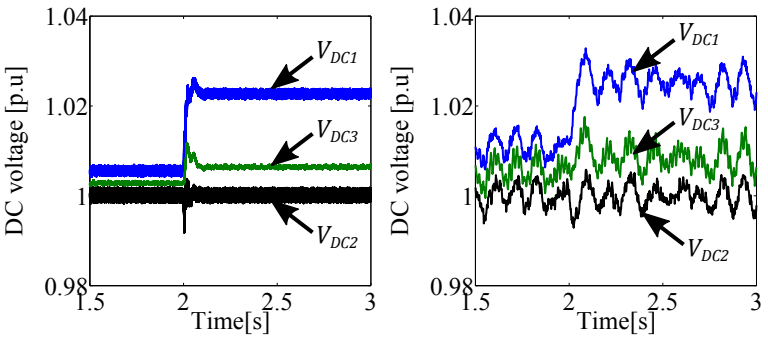
(a) VSC active power



(b) DC line current (positive pole)

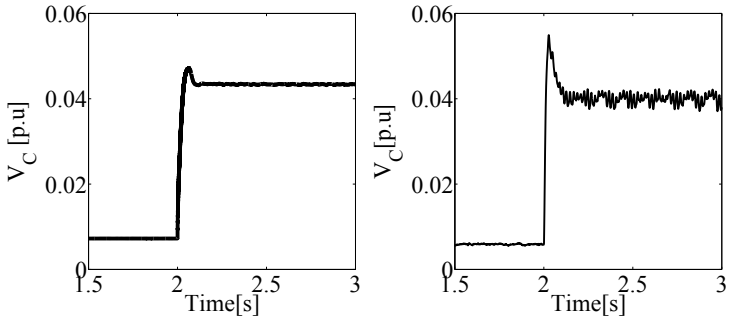


(c) DC line current (negative pole)

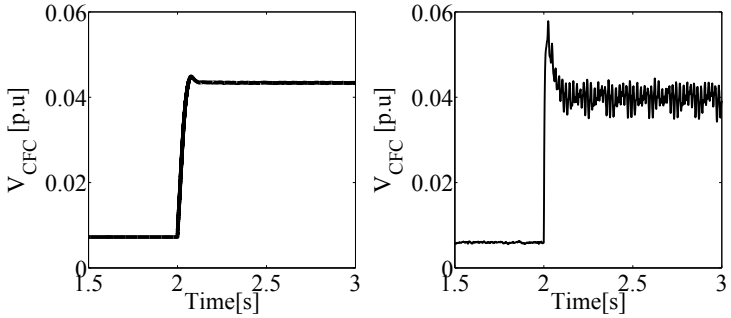


(d) DC terminal voltage

Figure 3.36: DC grid response under dc line isolation: Simulation (left) and experimental (right) results



(a) Capacitor voltage



(b) Inserted mean dc voltages

Figure 3.37: Response of the CFC located at the positive pole under dc line isolation: Simulation (left) and experimental (right) results

3.6 Conclusions

This chapter has discussed the operation and control of R, RC and C-CFCs. The performance of the proposed devices has been validated on an experimental three terminal mesh connected HVdc test-rig. A good agreement has been observed between the experimental and simulation results, which demonstrate that a CFC can be used to improve the grid reliability by limiting the line currents below thermal limits.

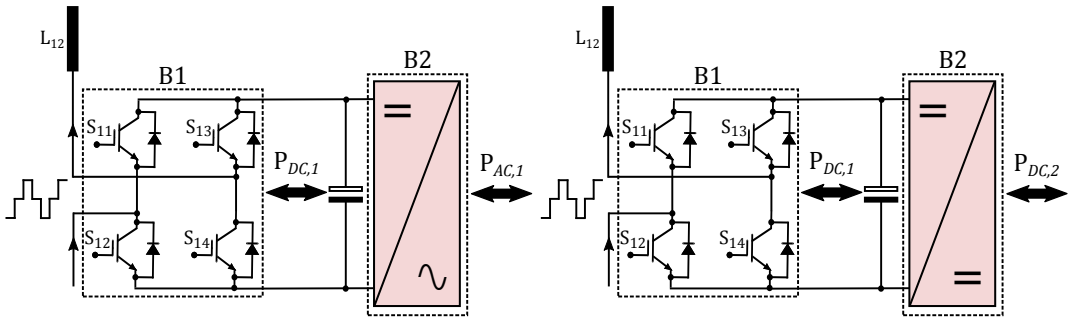
The controllability of the R-CFC can be improved by introducing a capacitor in series with the resistor to form an RC-CFC. The addition of the series capacitor significantly reduces the CFC power rating by eliminating the necessity of a large resistor. The C-CFC provides a better solution in terms of power losses compared R and RC-CFCs. The operational range of C-CFC is limited to two quadrants as the capacitor discharge is unattainable when line currents are in opposite directions. This could be relieved by either employing multiple CFCs or a hybrid CFC. In addition, a CFC with a series connected capacitor (RC or C-CFC) can be used to reduce the stress on FB-MMCs during maintenance by isolating a specific dc line.

4 Dual H-bridge CFC (2B-CFC)

4.1 Introduction

In an IGBT based CFC, as shown in Fig. 4.1(a), an ac/dc converter B_2 is used to establish a constant dc voltage across the capacitor whereas a dc/dc converter B_1 is used to generate the required series dc voltage by chopping the capacitor voltage. The dc/dc converter B_2 can be realised with H-bridge modules due to their four quadrant operational capability. The switch arrangement of an H-bridge module allows controlling the direction of current flowing through the dc side capacitor. Thus, the inserted series dc voltage can be either positive or negative regardless of current direction. If losses are neglected, the power $P_{DC,1}$ added to (subtracted from) the dc branch equals to the power $P_{AC,1}$ subtracted from (added to) the ac side. Alternatively, as discussed in Chapter 3, current control can be achieved via transferring power between dc lines/nodes. As shown in Fig. 4.1(b), an inter dc grid CFC can be realised by replacing the ac/dc converter B_2 in Fig. 4.1(a) with a dc/dc converter (H-bridge) connected in series with a neighbouring dc line.

As discussed in Chapter 3, the operation of a C-CFC is limited to quadrants 1 and 3 as the capacitor discharge is not possible when dc line currents directions are opposite. In this chapter, a dual H-bridge CFC (2B-CFC) is introduced to overcome the shortcomings of a C-CFC. The operation and control of the 2B-CFC are discussed under current control (CC) and voltage control (VC) modes. A dual modulation control scheme is proposed to regulate the CFC capacitor voltage and line current independently. An experimental platform consisting on a three-terminal dc grid and



(a) AC-DC nodes (b) DC-DC nodes

Figure 4.1: Types of CFC power exchange.

small scale 2B-CFC prototypes has been developed to validate the concepts. The performance of the CFC is evaluated under steady state and line overloading conditions. Furthermore, the impact of semiconductor voltage drops on line current flow is explored.

4.2 Solid State Arrangement

A 2B-CFC consists of two back-to-back H-bridges connected in series with dc lines (see Fig. 4.2, where H-bridges B_1 and B_2 are connected with lines L_{12} and L_{13}, respectively). Switches Q_1 and Q_2 are connected in parallel with B_1 and B_2, respectively, to by-pass the bridges when current control is not required. Switches Q_1 and Q_2 consist of two anti-series connected IGBTs. A dc voltage is established on the capacitor in order to provide a voltage source for the current flow control.

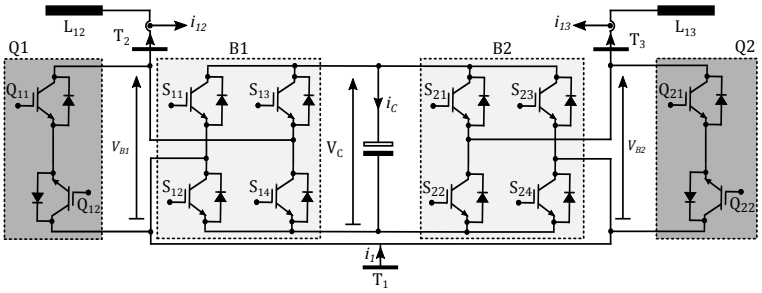


Figure 4.2: Topology of a 2B-CFC.

4.3 Operation and Control

4.3.1 Operation

4.3.1.1 By-pass mode

In this mode of operation, the required line current reduction or increment is zero and thus the series dc voltage injection is zero. Therefore, Q_1 and Q_2 must be bypassed. As shown in Fig. 4.3, this is achieved by turning switches Q_1 and Q_2 on.

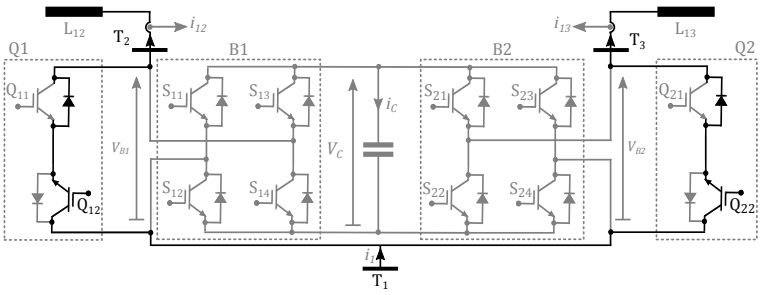


Figure 4.3: Operation under the by-pass mode.

4.3.1.2 Current Control Mode

A required line current control is achieved in this mode by providing a negative or positive dc voltage injection in series to the controlled dc line. The magnitude of the inserted dc voltage is regulated by switching the H-bridge voltage. For instance, consider that current flows from terminals T_1 to T_2 and from T_1 to T_3. In this scenario, switches S_{12} of B_1 and S_{21} of B_2 are modulated to reduce the current on line L_{12}, while all other switches (S_{11}, S_{13}, S_{14}, S_{22}, S_{23} and S_{24}) remain off.

The operational stages of the CFC during the CC mode are shown in Fig. 4.4. The switching states of the controlled switches and the corresponding changes on the bridge voltages are shown in Fig. 4.5. When switches S_{12} and S_{21} are off (Fig. 4.4(a)), the line currents flow through the naturally commutated diodes and charge the capacitor rapidly. The voltages across terminals T_1 and T_2, and T_1 and T_3, are equal to V_C. This decreases currents i_{12} and i_{13}. As illustrated in Fig. 4.4(b), when S_{21} is on and S_{12} is off, bridge B_2 is shorted and B_1 charges the dc capacitor.

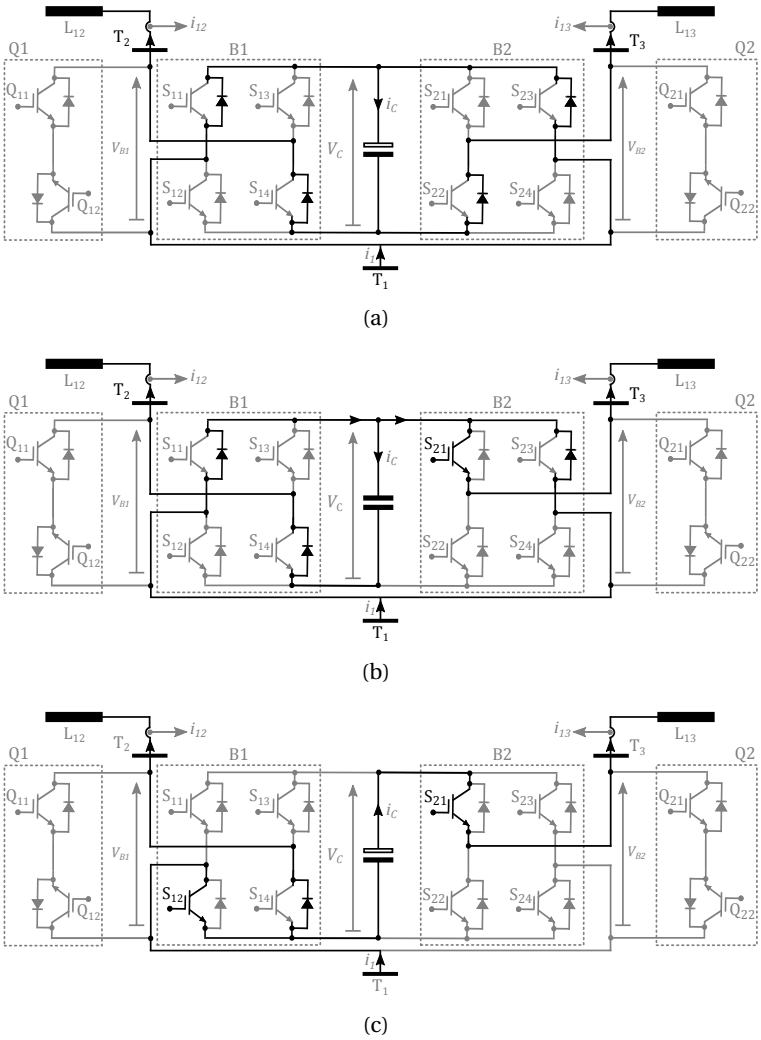


Figure 4.4: Operational stages of a 2B-CFC under the CC mode: (a) Charge mode 1; (b) charge mode 2; (c) discharge mode.

As a result of a positive voltage injection in series with line L_{12}, current i_{12} decreases while i_{13} increases to maintain the power balance (see Fig. 4.5). Conversely, a negative voltage must be inserted in series with L_{13} to increase line current i_{13}. This can be achieved by switching on both S_{12} and S_{21} (see Fig. 4.4(c)). During this period the capacitor is discharged into L_{13}. As shown in Fig. 4.5, continuous switching of S_{12} and S_{21} generates mean positive ($\overline{V}_{B1}$) and negative ($\overline{V}_{B2}$) dc voltages across the CFC terminals T_1 and T_2, and T_1 and T_3, respectively. This increases i_{13} and also decreases i_{12}.

In the CC mode, the inserted dc voltages V_{B1} and V_{B2} can be expressed by the following equations:

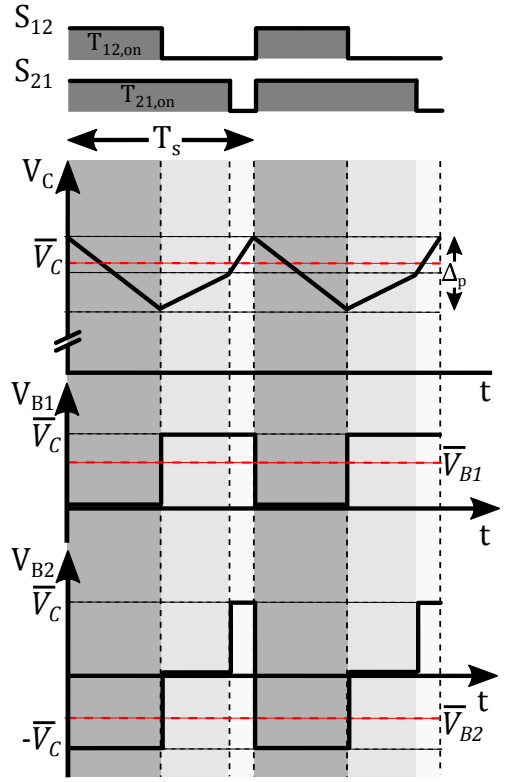


Figure 4.5: Switching waveforms for the CC mode.

When S_{12} and S_{21} are off:

$$\begin{aligned} V_{B1,a} &= \overline{V}_{\mathrm{C}} \\ V_{B2,a} &= \overline{V}_{\mathrm{C}} \end{aligned} \tag{4.1}$$

where $\overline{V}_{\mathrm{C}}$ is the average value of capacitor voltage V_{C}.

When S_{12} is off and S_{21} is on:

$$\begin{aligned} V_{B1,b} &= \overline{V}_{\mathrm{C}} \\ V_{B2,b} &= 0 \end{aligned} \tag{4.2}$$

When S_{12} and S_{21} are on:

$$\begin{aligned} V_{B1,c} &= 0 \\ V_{B2,c} &= -\overline{V}_{\mathrm{C}} \end{aligned} \tag{4.3}$$

From eqs. (4.1), (4.2) and (4.3), the average values of bridge voltages V_{B1} and V_{B2} can be derived as follows:

$$\begin{aligned}\overline{V}_{B1} &= \frac{V_{B1,a}\cdot T_{\text{off},21} + V_{B1,b}\cdot (T_{\text{on},21} - T_{\text{on},12})}{T_\text{s}} \\ &= \frac{\overline{V}_\text{C}\cdot T_{\text{off},21} + \overline{V}_\text{C}\cdot (T_{\text{on},21} - T_{\text{on},12})}{T_\text{s}} \\ &= \overline{V}_\text{C}(1-D_1)\end{aligned} \tag{4.4}$$

$$\begin{aligned}\overline{V}_{B2} &= \frac{V_{B2,a}\cdot T_{\text{off},21} + V_{B2,c}\cdot T_{\text{on},12}}{T_\text{s}} \\ &= \frac{\overline{V}_\text{C}\cdot T_{\text{off},21} - \overline{V}_\text{C}\cdot T_{\text{on},12}}{T_\text{s}} \\ &= \overline{V}_\text{C}(1-D_1-D_2)\end{aligned} \tag{4.5}$$

where D_1 and D_2 are the duty cycle of switches S_{12} and S_{21}, respectively ; $D_1 = \frac{T_{\text{on},12}}{T_\text{s}}$ and $D_2 = \frac{T_{\text{on},21}}{T_\text{s}}$.

In this configuration, the power taken from L_{12} is equal to power added to L_{13} or vice versa. The relationship between the inserted bridge voltages $\overline{V}_{B1}$, $\overline{V}_{B2}$, and line currents i_{12}, i_{13}, can be represented by:

$$\begin{aligned} P_{B1} &= P_{B2} \\ \overline{V}_{B1}\cdot i_{12} &= \overline{V}_{B2}\cdot i_{13}\end{aligned} \tag{4.6}$$

where P_{B1}, P_{B2} are the powers of H-bridges B_1 and B_2, respectively.

In steady state, the ripple on capacitor voltage V_C can be estimated by the following equations:

$$\begin{aligned}\Delta_p &= i_{12}\cdot\frac{(T_{\text{on},21} - T_{\text{on},12})}{C_\text{CFC}} + (i_{12} + i_{13})\frac{T_{\text{off},21}}{C_\text{CFC}} \\ \Delta_p &= i_{13}\cdot\frac{T_{\text{on},12}}{C_\text{CFC}}\end{aligned} \tag{4.7}$$

Fig. 4.6 shows the switching combination of bridges B_1 and B_2 under the CC mode. Switching patterns are provided for four quadrant operation, where the quadrants are defined by the direction of the line currents. The switching sequence is determined by the direction of i_{12}, i_{13}

and i_1. The increment and decrement in bridge currents are represented by the arrow direction.

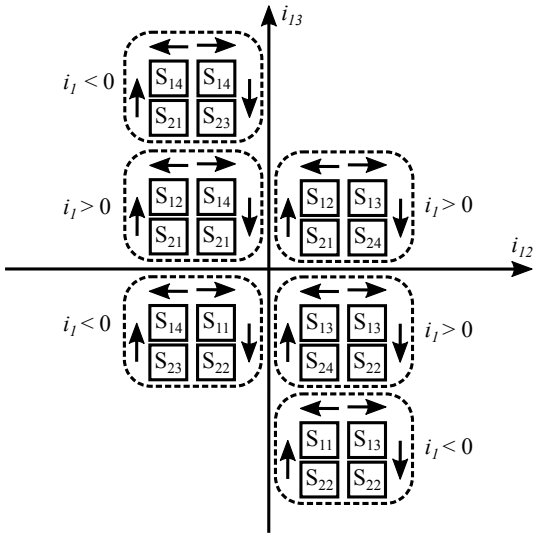


Figure 4.6: 2B-CFC switch selection in CC mode

4.3.1.3 Voltage Control Mode

In this mode the capacitor voltage is regulated regardless of the line current value. To achieve this, the duty cycle of switch S_{21} must be set to 1 while switch S_{12} adjusts its duty cycle so that the voltage is maintained constant. Since one of the switches is always on, the CFC takes only two switching states (see Figs. 4.4(b) and 4.4(c)). This mode of operation usually takes place under the voltage sharing method presented later in Chapter 6. The switching combinations of bridges B_1 and B_2 under the VC mode are provided in Fig. 4.7.

4.3.2 Controller design

A master-slave (dual modulation) control scheme is proposed to control the 2B-CFC connected with L_{12} and L_{13} (see Fig. 4.2). The capacitor voltage V_C and line current i_{13} are controlled independently by modulating switches S_{12} and S_{21}, respectively. The CFC capacitor voltage control loop is depicted in Fig. 4.8. The dynamics of the dc lines are represented by transfer

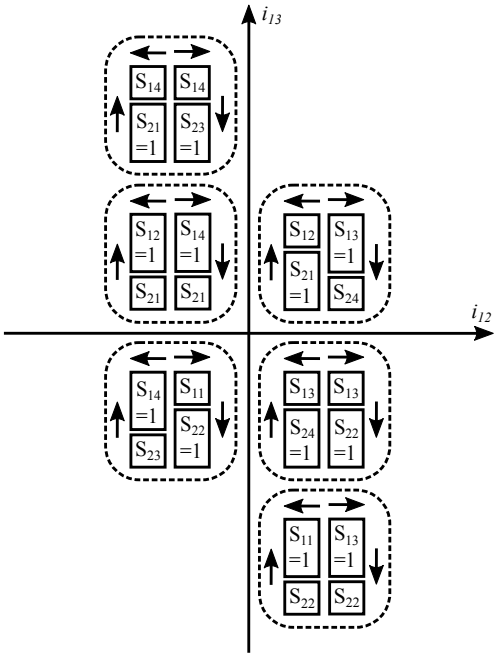


Figure 4.7: 2B-CFC switch selection in VC mode.

functions $G_{p1}(s)$ and $G_{p2}(s)$:

$$G_{p1}(s) = \frac{1}{L_{12}s + R_{12}},$$
$$G_{p2}(s) = \frac{1}{L_{13}s + R_{13}}. \tag{4.8}$$

DC terminal voltages V_{DC1}, V_{DC2} and V_{DC3} are signals which affect the capacitor voltage dynamics in open loop. For control system design, these dc voltages are assumed as disturbances. By applying block diagram reduction techniques, the overall plant transfer function $G_v(s)$ relating the capacitor voltage V_C (output) to the duty cycle D_1 is obtained:

$$G_v(s) = K_c\left(\frac{(L_{12}+L_{13})s + (R_{12}+R_{13})}{L_{12}s + R_{12}}\right)\cdot\left(\frac{1}{L_{13}Cs^2 + R_{13}Cs + 1}\right) \tag{4.9}$$

A controller $G_k(s)$ is proposed to ensure an adequate closed-loop performance:

$$G_k(s) = K\left(\frac{s+z_c}{s+p_c}\right)\left(\frac{s+z_p}{s}\right) \tag{4.10}$$

Controller G_k(s) in (4.10) consists of a proportional-integral (PI) structure cascaded with a lead compensator, where z_p is the zero of the PI controller, z_c and p_c are the zero and pole of the lead compensator, and K is the overall controller gain. Such a control structure, if designed properly, is sufficient to provide high stability margins, eliminate the steady-state error and reject disturbances.

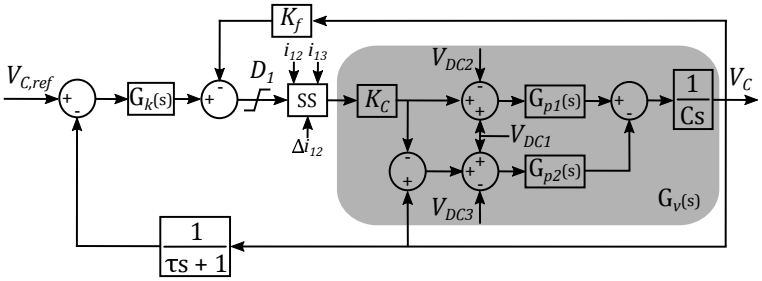


Figure 4.8: Capacitor voltage controller.

Let the parameters in $G_{p1}(s)$, $G_{p2}(s)$, and $G_v(s)$ be defined as in Table 3.2 of Chapter 3. Fig. 4.9 shows the open loop frequency response of $G_v(s)$. The bandwidth of the uncompensated system is 1000 rad/s and this value is kept when $G_k(s)$ is used. It can be also observed in Fig. 4.9 that the uncompensated system exhibits a poor phase margin ($\approx$ 4 deg). While the PI controller is used to achieve a zero steady-state error, the lead compensator significantly improves the phase margin to $\approx$ 68 deg to ensure a good performance during transients and solid-state switching (or quadrant selection). Additionally, the CFC capacitor voltage loop considers a feedback loop with a proportional gain K_f to limit the initial overshoot in the capacitor voltage (see Fig. 4.8).

Fig. 4.10 shows the line current control loop. Since plant $G_i(s)$ is a first order function, a PI controller is used. It should be highlighted that a first order filter with a cut-off frequency of 200 Hz has been employed with the voltage and current controllers to eliminate measurement noise. The CFC control parameters can be found in Appendix B. A logic controller, as shown in Fig. 4.11, is used to activate both current and capacitor voltage controllers during an overloading conditions. The signal S_{CFC} is used as a force trigger to operate the CFC in CCM under operating conditions other than line overloading.

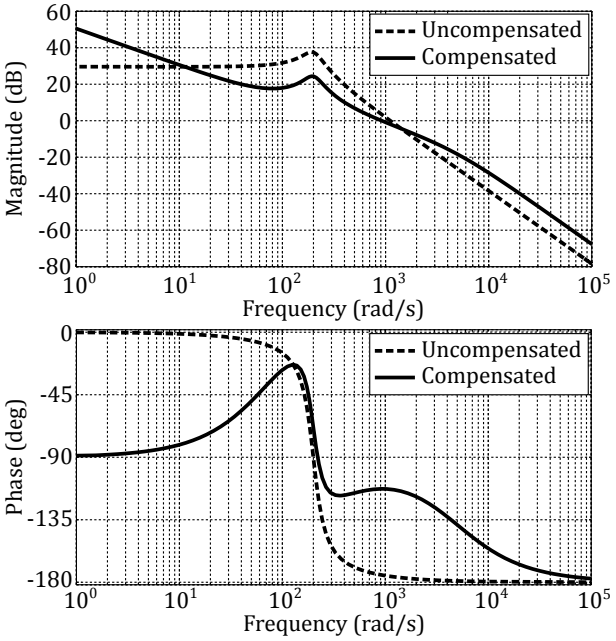


Figure 4.9: System open loop frequency response (Bode plot):Uncompensated system $G_v(s)$ and compensated system $G_k(s)G_v(s)$.

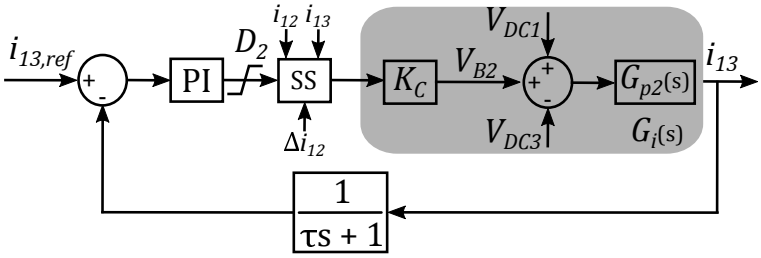


Figure 4.10: Line current controller.

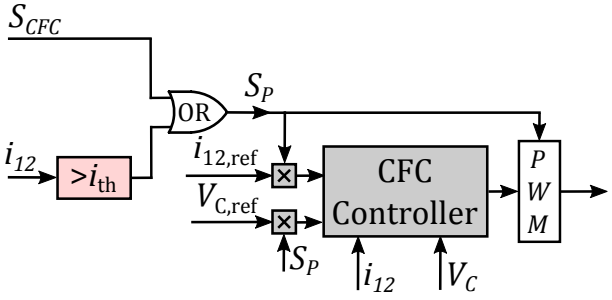


Figure 4.11: 2B-CFC triggering controller.

4.3.3 Reduced 2B-CFC Model

In Fig. 4.12, switches S_{12}, S_{24} are connected between the capacitor positive terminal and T_1 whereas switches S_{11}, S_{23} are connected between capacitor negative terminal and T_1. Therefore,

S_{23} and S_{24} are dispensable as they are connected in parallel to switches S_{11} and S_{12}, respectively. Fig. 4.13 shows the reduced CFC model after the removal of switches S_{23} and S_{24} from bridge B_2. The electrical nodes T_1, T_2 and T_3 are connected to the mid-points of half-bridges B_0, B_1 and B_3, respectively, to form a CFC. The reduced model comprises less number of IGBTs and has a smaller footprint. On the contrary, elimination of switches S_{23} and S_{24} could reduce the reliability level.

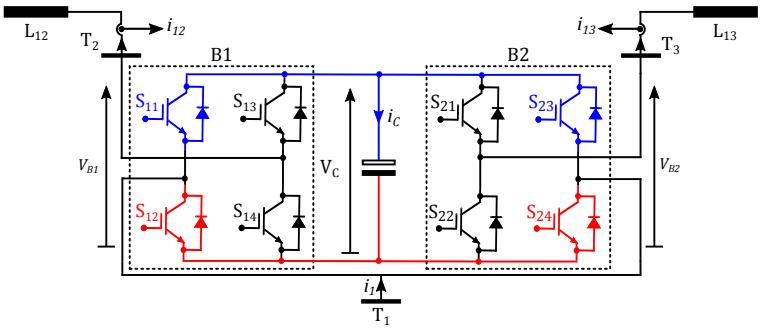


Figure 4.12: Swicthes connected between same potential points.

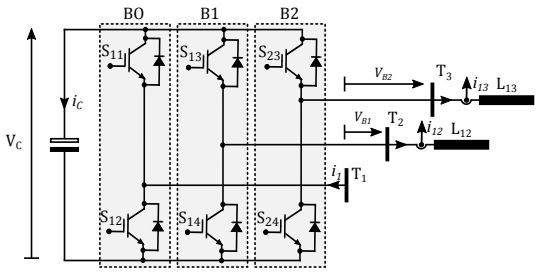


Figure 4.13: Reduced 2B-CFC model.

4.4 Experimental Setup

The three-terminal meshed MTdc grid shown in Fig. 4.14 is used to validate the operation and control of 2B-CFCs. The VSC terminals have been arranged in a symmetrical monopole configuration and rated at ±125 V and 2 kW. Fig. 4.15 shows two types of CFC circuit arrangement on a dc grid, namely, uni-pole (Fig. 4.15(a)) and bi-pole (Fig. 4.15(b)). The uni-pole operation is implemented by placing a CFC either at positive pole or negative pole. In Chapter 3, during the uni-pole operation, the positive pole currents are redistributed to avoid the current overload where the negative pole remains overloaded. In order to avoid imbalances between poles and to

increase the grid reliability, CFCs must be placed at both positive and negative poles (bi-pole). It must be emphasised that a uni-pole operation can be implemented using bi-pole circuit arrangement through by-passing one of the CFCs.

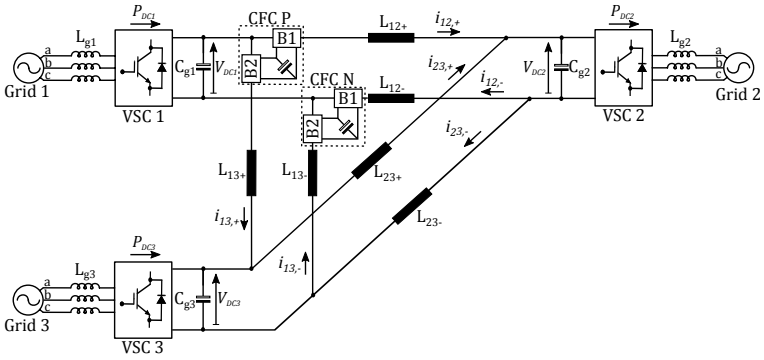
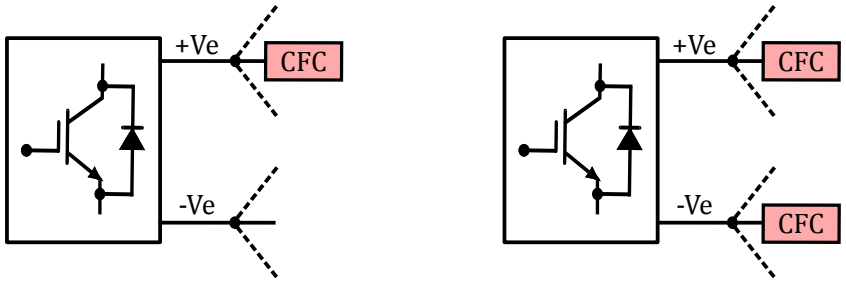


Figure 4.14: Three-terminal MTdc grid with embedded CFCs.



(a) Uni-pole (b) Bi-pole

Figure 4.15: Types of CFC operation.

To establish a bi-pole operation, CFC modules P and N are installed in series with both the positive and negative poles of lines L_{12} and L_{13}. A master-slave control scheme for VSCs as described in Chapter 3 has been adopted to maintain the grid power balance. It uses a classical *dq* reference frame scheme to regulate the dc voltage or active and reactive power.

Fig. 4.16 shows the experimental setup of the MTdc test-rig with embedded 2B-CFC prototypes. A dSPACE DS1005 system is used to control the test-rig. Simulink-based real-time interface control blocks are used to implement the control scheme. The test-rig specifications are provided in Table 3.2 of Chapter 3.

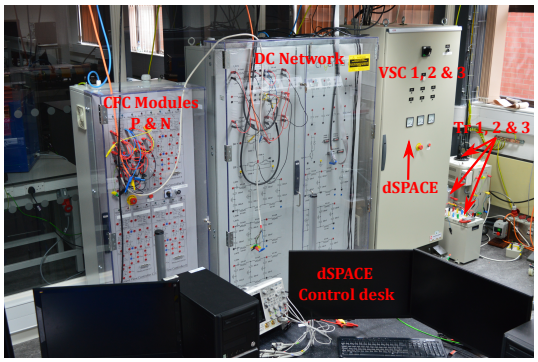


Figure 4.16: Experimental setup.

4.4.1 Impact of semiconductor voltage drops on line current control

Generally, a series dc voltage injection of 1 to 2% (of system rated voltage) is large enough to exert the power flow in dc grids. Following this line, an injection of 2.5 V should be adequate to regulate line currents in the scaled system. However, in a scaled system, the required dc voltage is affected by the forward voltage drop of semiconductor switches as they affect the current flow between electrical nodes. Therefore, these voltage drops must be taken into consideration to find a optimum operating point.

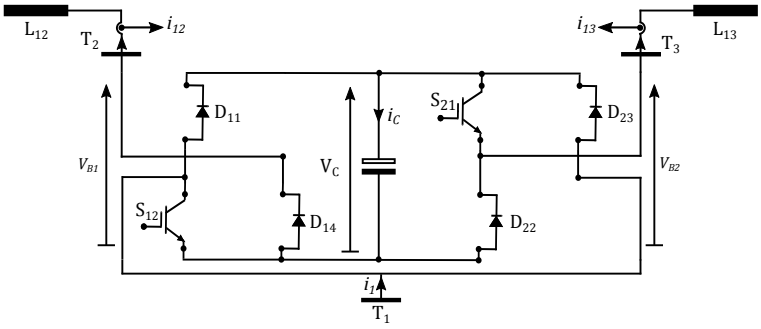


Figure 4.17: Active elements of 2B-CFC during CC mode.

The active elements of 2B-CFC during CC mode are shown in Fig. 4.17. Only one IGBT per bridge is active during operation, which is decided by the line current direction. When current flows from terminals T_1 to T_2 and T_1 to T_3, switches S_{12} of bridge B_1 and S_{21} of B_2 are active, while other switches are bypassed through naturally commuted diodes. The switching states of the controlled switches and the corresponding changes on the bridge voltages are shown in Fig. 4.18. By considering the voltage drops on the active semiconductor elements, the average

bridge voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$ from eqs. (4.4) and (4.5) can be modified as follows:

$$\begin{aligned} \overline{V}_{B1} &= V_{f1} - D_1(V_{f1} - V_{f2}), \\ \overline{V}_{B2} &= V_{f3} + D_1(V_{f5} - V_{f4}) + D_2(V_{f4} - V_{f3}), \end{aligned} \tag{4.11}$$

where

$$\begin{aligned} V_{f2} &= V_{D14} + V_{S12}, \\ V_{f1} &= V_{D11} + V_{D14} + \overline{V}_C, \\ V_{f3} &= V_{D22} + V_{D23} + \overline{V}_C, \\ V_{f4} &= V_{D23} + V_{S21}, \\ V_{f5} &= -\overline{V}_C + V_{S12} + V_{S21}, \end{aligned} \tag{4.12}$$

V_{D11}, V_{D22}, V_{D23} and V_{D14} are the forward voltage drops on diodes D_{11}, D_{22}, D_{23} and D_{14}, respectively; V_{S12} and V_{S21} are the on state voltage drops of switches S_{12} and S_{21}, respectively.

The rectified waveforms of V_{B1} and V_{B2} are shown in Fig. 4.18. Typically, the power diodes exhibit an on state forward voltage drop of 0.7-1 V and the IGBTs exhibit an on state voltage drop of around 1-2 V. Since these voltages are in the magnitude order of 1-2% of the system voltage, these voltage drops are sufficient to exert grid power flow. Thus, the required amount of capacitor voltage to achieve an optimum line current distribution could be very small.

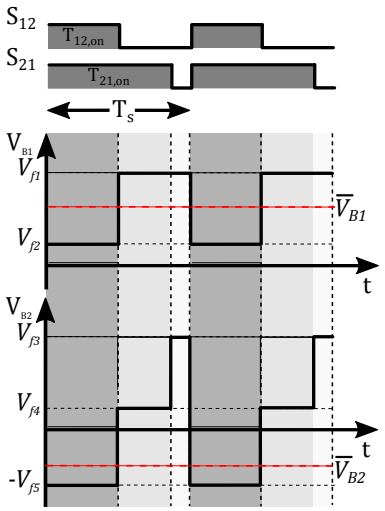


Figure 4.18: Impact of semiconductors voltage drops on bridge voltages in CC mode

In order to improve this issue, MOSFETs are used to develop the scaled CFC modules as they exhibit lower forward voltage drops and power losses than IGBTs. Specially, MOSFETs have a very small on-state voltage drop due to small current in the scaled system. If we assume this value is zero, then:

$$\overline{V}_{B1} = V_{D11} + V_{D14} + \overline{V}_C - D_1(V_{D11} + \overline{V}_C) \tag{4.13}$$

$$\overline{V}_{B2} = V_{D22} + V_{D23} + \overline{V}_C - D_1(\overline{V}_C + V_{D23}) - D_2(V_{D22} + \overline{V}_C) \tag{4.14}$$

Eq. (4.13) shows that $\overline{V}_{B1}$ is always greater than zero for the given point of operation. On the contrary, $\overline{V}_{B2}$ could either be positive or negative. If we assume the voltage drops across the MOSFETs body diode are fixed to V_d regardless of line current magnitude, then eq. 4.14 can be reformulated as follows :

$$\overline{V}_{B2} = \overline{V}_C(1 - D_1 - D_2) + V_d(2 - D_1 - D_2), \tag{4.15}$$

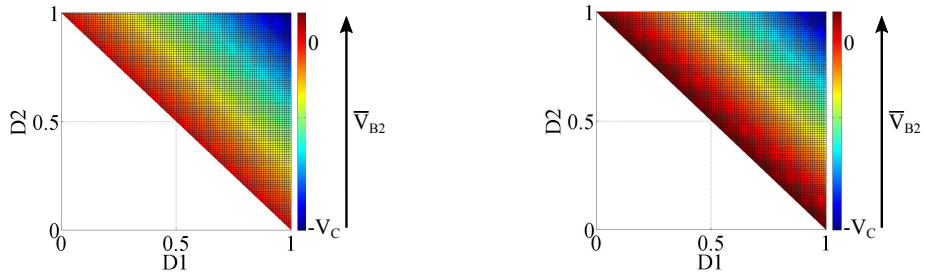


Figure 4.19: $\overline{V}_{B2}$ voltage distribution: (a) ideal (b) diode voltage drop.

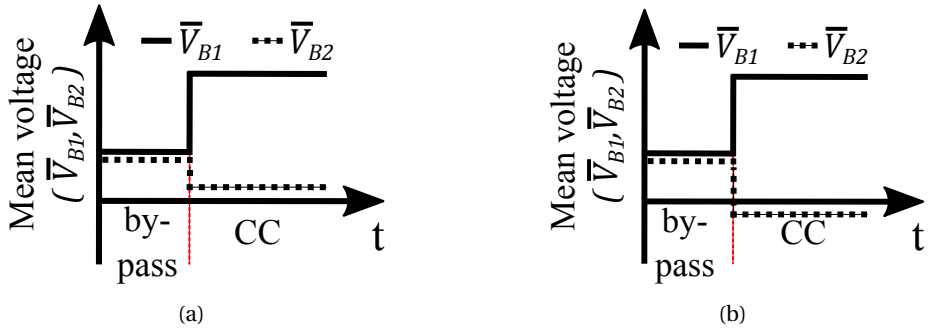


Figure 4.20: Inserted mean voltage in CC mode: (a) positive voltage injections (b) complementary injection.

Table 4.1: Specifications and parameters: 2B-CFCs

Devices	Specifications	Operating rating
CFC	Rated power Rated dc voltage	40W 10 V
DC capacitor	C	4400 μF
Switching frequency	f_{sw}	2000 Hz
MOSFET	Model: PSMN3R8-100BS typical V_d=0.8 V	

Figs. 4.19(a) (eq. 4.15) and 4.19(b) (eq. 4.14) show the changes in the average bridge voltage $\overline{V}_{B2}$ with respect to changes in duty cycles D_1 and D_2, respectively, for ideal and non-ideal conditions. Theoretically if the diode voltage drop is zero (neglected in a high voltage system), when current flows from T_1 to T_2 and T_1 to T_3 i.e. currents i_{12} and i_{13} are positive, inserted dc voltages should have opposite polarities to satisfy the power balance between the bridges where $\overline{V}_{B1} \geq 0$ and $\overline{V}_{B2} \leq 0$ (Fig. 4.19(a)). However, in scaled systems, during the CC mode, $\overline{V}_{B2}$ changes between V_d and -$\overline{V}_C$ as result of diode voltage drop (see Fig. 4.19(b)). Thus, the inserted voltages could either have the same polarity or an opposite polarity (Fig. 4.20).

The scaled CFC module is shown in Fig. 4.21. The module specifications are provided in Table 4.1. MOSFET model PSMN3R8-100BS is used to develop the scaled CFC modules due to their lower forward voltage drop and power losses characteristics compared to IGBTs. A switching frequency of 2000 Hz is adopted to modulate the CFC.

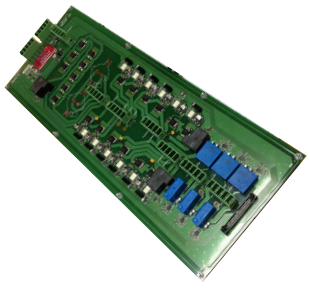


Figure 4.21: CFC PCB module.

4.5 Experimental Validation

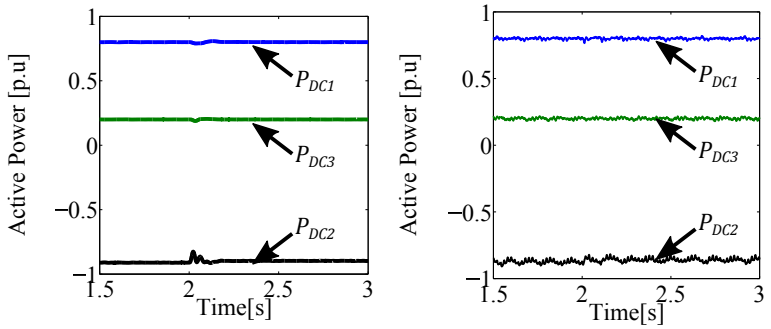
The results in this section are expressed in per unit considering the following power, voltage and current bases: 2 kW, 125 V, and 8 A. VSCs 1 and 3 are initially set to inject 0.8 and 0.2 p.u. into the MTdc grid, whereas VSC 2 has been designated as a slack busbar that maintains the grid power balance (*i.e.*, maintains a constant dc voltage).

4.5.1 By-pass mode to CC mode transition

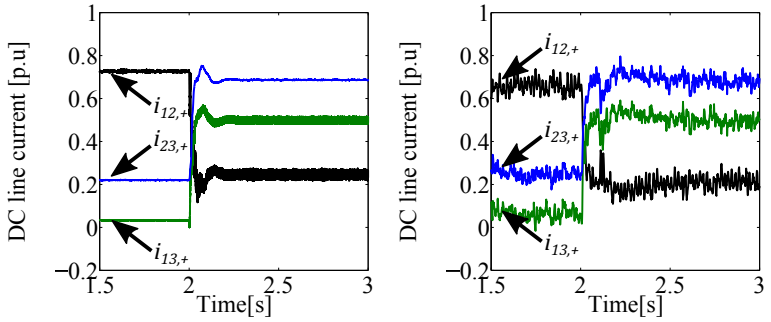
In this test case, performance of 2B-CFC is evaluated during the soft transition from the by-pass mode to the CC mode. The CFCs are placed at the positive and negative poles of lines L_{12} and L_{13}. The simulation (left) and experimental results (right) are shown in Figs. 4.22 to 4.24. Initially, both positive and negative CFCs are bypassed through Q_1 and Q_2. At $t = 2$ s, CFCs are enabled and are requested to control the line current i_{13} at 0.5 p.u. In the CC mode, switches S_{12} and S_{21} of positive pole CFC and switches S_{11} and S_{22} of negative pole CFC are modulated. During the CC mode, as shown in Fig. 4.22(d), VSCs 1 and 3 have adjusted their terminal voltages to compensate for the effects of CFCs while terminal 2 voltage remains constant.

Figs. 4.23 and 4.24 provide the voltage profiles of positive and negative poles CFCs, respectively. For both simulation and experiment, the capacitor voltages are maintained at 0.04 p.u., as shown by Figs. 4.23(a) and 4.24(a). During the CC mode, mean dc voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$ are inserted in series with lines L_{12+} and L_{13+}, respectively. This is shown in Fig. 4.23(b). Since the line current flows in an opposite direction, the signs of the inserted dc voltages in series with L_{12-} and L_{13-} (see Fig. 4.24(b)) are opposite with respect to those shown in Fig. 4.23(b). During the CC mode, power is transferred from B_1 to B_2.

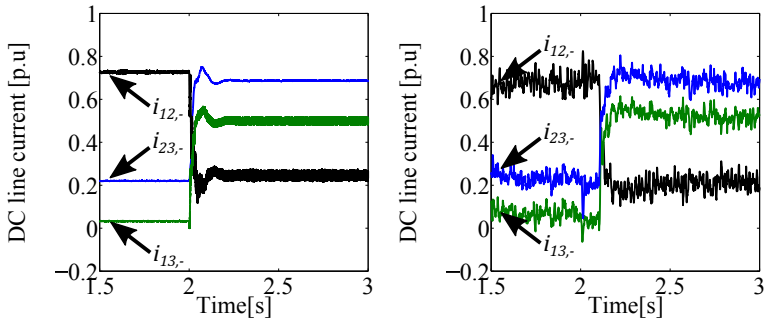
It should be noticed that a small mismatch occurs between the line current distribution of the simulation and experimental results. This is due to forward voltage drops in diodes and converter power losses in the experimental platform. Conversely, these voltage drops are fixed to 0.8 V in the simulation, with converter switching losses being neglected.



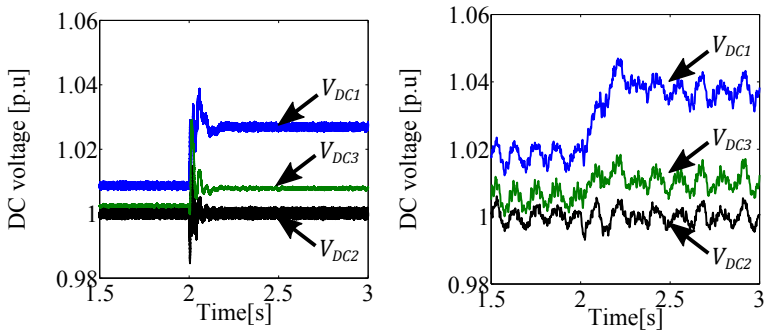
(a) VSC active power



(b) DC line current (positive pole)

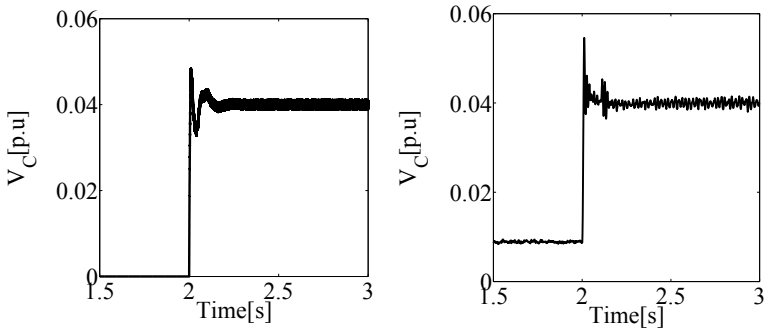


(c) DC line current (negative pole)

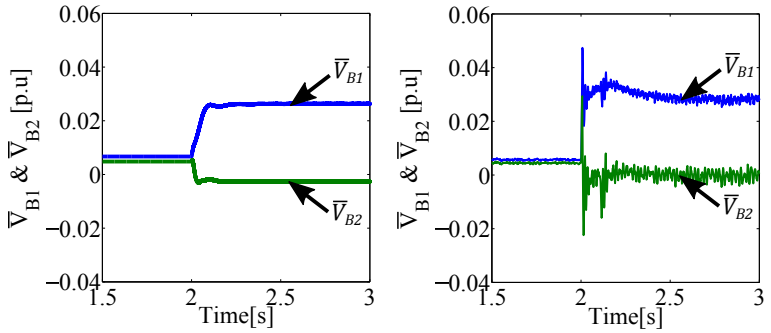


(d) DC terminal voltage

Figure 4.22: DC grid response during by-pass mode to CC mode transition of the 2B-CFC: Simulation (left) and experimental (right) results.

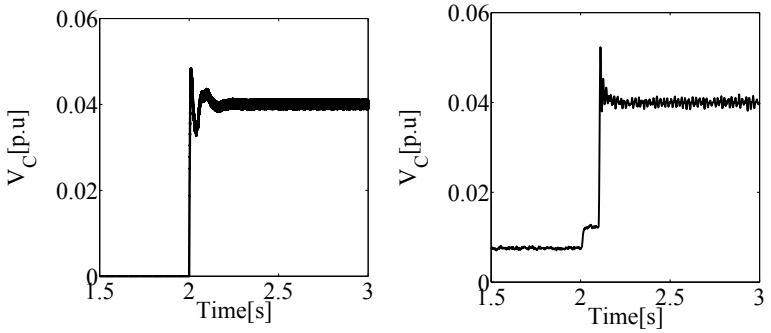


(a) capacitor voltage

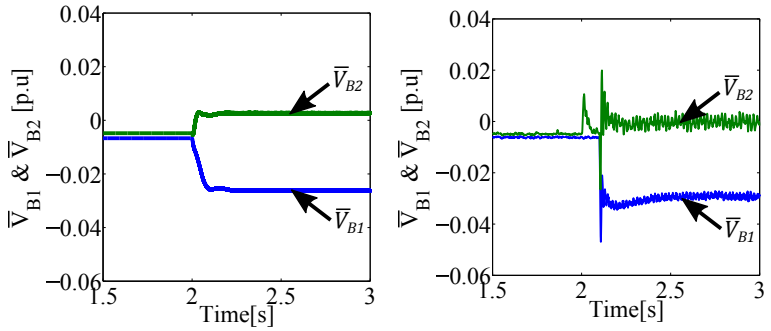


(b) inserted mean dc voltages

Figure 4.23: Response of the 2B-CFC located at the positive pole during by-pass mode to CC mode transition: Simulation (left) and experimental (right) results.



(a) capacitor voltage



(b) inserted mean dc voltages

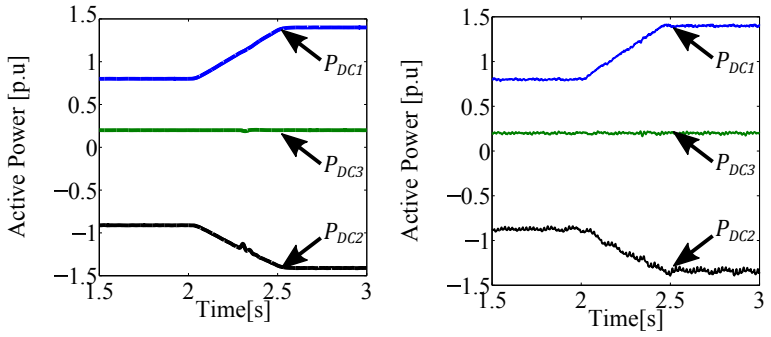
Figure 4.24: Response of the 2B-CFC located at the negative pole during by-pass mode to CC mode transition: Simulation (left) and experimental (right) results.

4.5.2 Line overload elimination

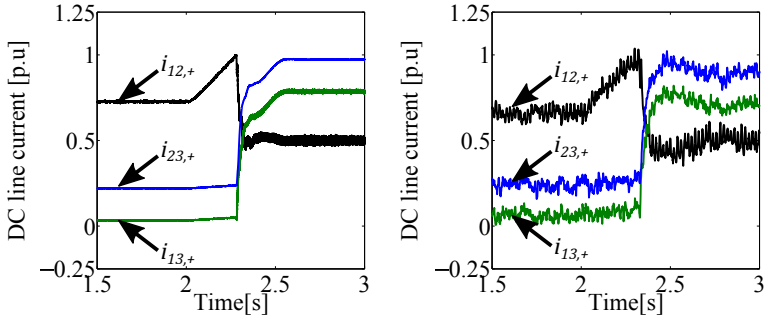
In this test case, 2B-CFCs are used to avoid line overloading following a ramp change in power. Initially, both CFCs operate in a by-pass mode, with switches Q_1 and Q_2 being turned on. At $t = 2$ s, the power reference of VSC 1 is ramped up from 0.8 to 1.4 p.u. (see Fig. 4.25(a)). As it can be observed in Figs. 4.25(b) and 4.25(c), line currents i_{12+} and i_{12-} surpass the maximum thermal current limit (of 1 p.u.). Following the overload detection, the CFCs are enabled to bring down both positive and negative poles currents i_{12+} and i_{12-}, respectively, to 0.5 p.u. to achieve a better line current distribution. As a result, the converters adjust their terminal voltages to maintain the grid power balance (Fig. 4.25(d)). Switches S_{12} and S_{21} of positive pole CFC and switches S_{11} and S_{22} of negative pole CFC are modulated during CC mode.

Figs. 4.26 and 4.27 provide the voltage profiles of positive and negative poles CFCs, respectively, during line overloading elimination. Both positive and negative poles CFCs capacitor voltages are regulated at 0.04 p.u. It has been observed that as a result of a greater current reduction, the amount of required series dc voltage injections (Figs. 4.26(b) and 4.27(b)) have increased compared to the previous test case (Figs. 4.23(b) and 4.24(b)).

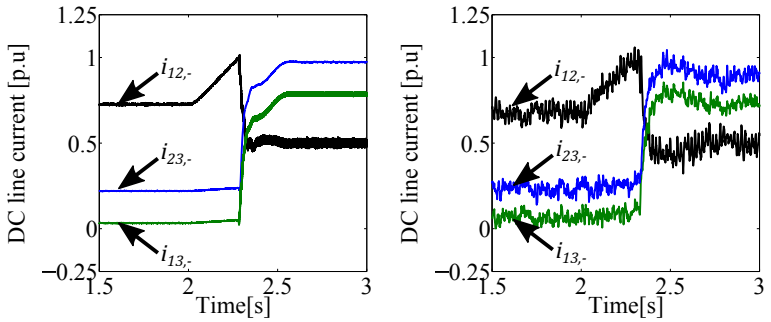
It must be emphasized that in this case the current reference is set to 0.5 p.u. to minimize the impact of diode voltage drop on CFC performance. However, in a real system, the line current will be controlled just below or at 1 p.u. mark as demonstrated in Chapter 3.



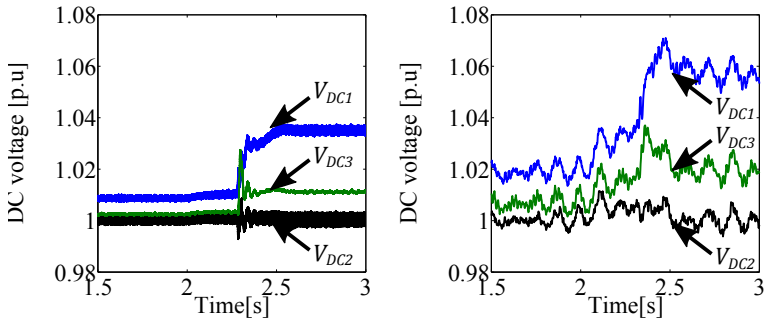
(a) VSC active power



(b) DC line current (positive pole)

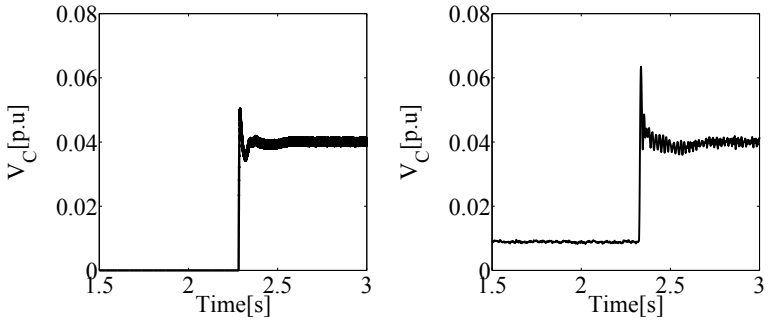


(c) DC line current (negative pole

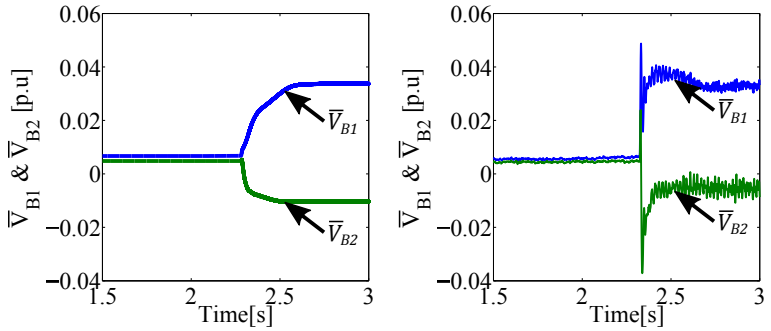


(d) DC terminal voltage

Figure 4.25: DC grid response for a ramp change in power with embedded 2B-CFCs: Simulation (left) and experimental (right) results.

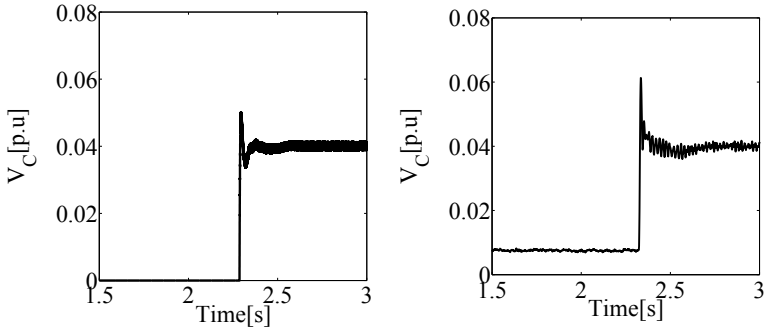


(a) capacitor voltage

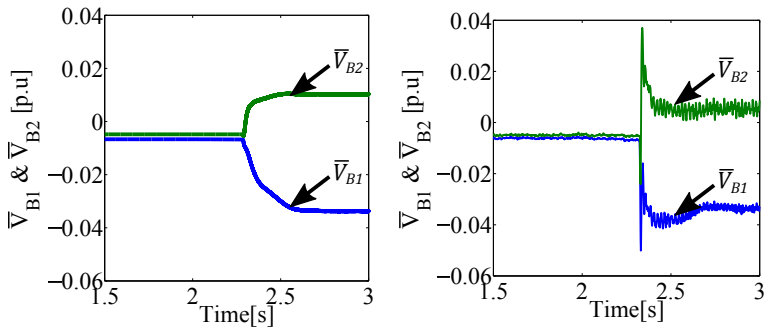


(b) inserted mean dc voltages

Figure 4.26: Response of the 2B-CFC located at the positive pole for a ramp change in power: Simulation (left) and experimental (right) results.



(a) capacitor voltage



(b) inserted mean dc voltages

Figure 4.27: Response of the 2B-CFC located at the negative pole for a ramp change in power: Simulation (left) and experimental (right) results.

4.6 Impact of CFC Switching on DC Side Harmonics

The injection of pulsed dc voltages, as shown in Fig. 6.33, increases the harmonics (magnitude of the peak-to-peak line current ripple) on dc line currents. Thus, dc grids feature significant external power losses on the dc lines due to harmonics. Table 4.2 summarizes the total harmonic distortion (THD) on dc line currents with respect to CFC switching frequency f_{sw}. The impact of CFC switching has been analysed under three different switching frequencies; 500 Hz, 1000 Hz and 2000 Hz (Fig. 4.28). In Table 4.2, the harmonic content on dc line currents decreases with an increase in switching frequency. The results have been expressed as a percentage of the fundamental current magnitude. It has been observed that in all test cases, the harmonics on lines L_{13} and L_{12} where the CFC is located is high compared to line L_{23} due to switching.

Table 4.2: Change of dc harmonics of test-rig dc line currents

Line Current	Switching Frequency (Hz)		
	500	1000	2000
i_{12}	18.1	4.8	1.5
i_{13}	20.1	7.5	1.8
i_{23}	11.6	3.3	1.1

These results suggest that CFCs should be implemented with filters to minimise their harmonic contribution (and hence power losses). However, the addition of passive components should be done with care as these will influence the selection of the switching frequency and the sizing of the CFC capacitor –in addition to cost implications if the installation is carried out offshore.

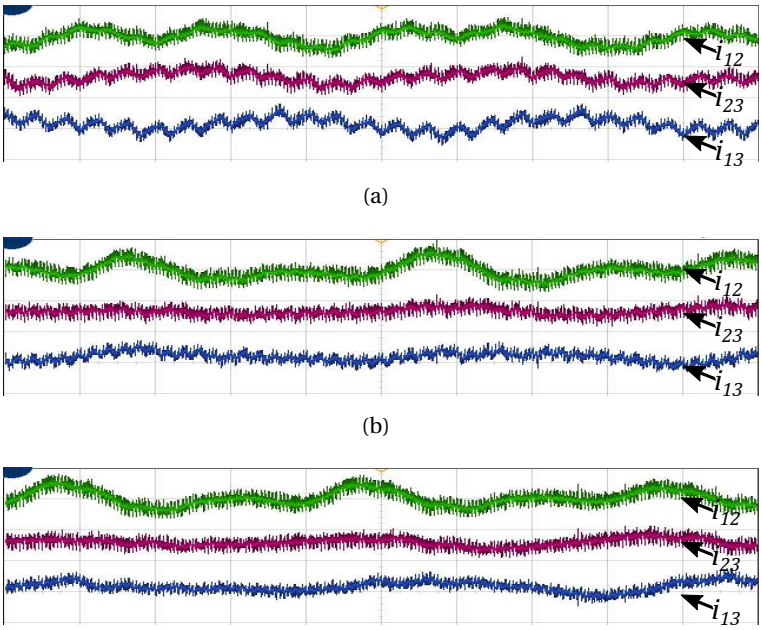


Figure 4.28: Impact of CFC switching frequency on line current ripple (a) f_{sw}=500 Hz; (b) f_{sw}=1000 Hz; (c) f_{sw}=2000 Hz.

4.7 Conclusions

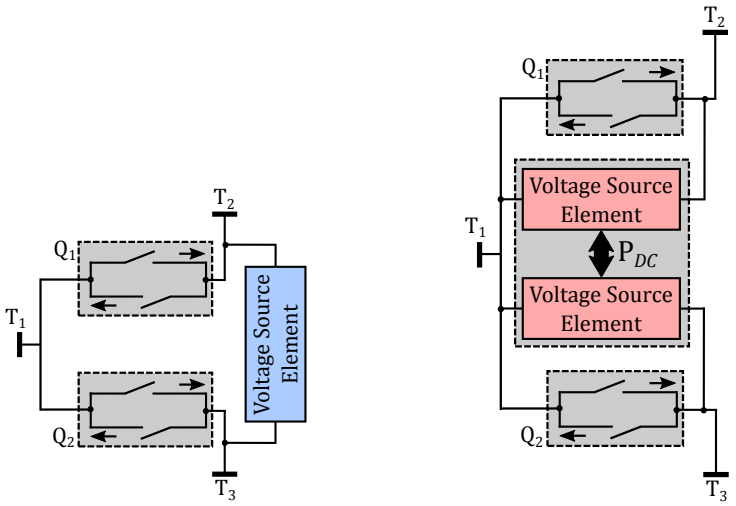
In this chapter, the operation and control of a 2B-CFC have been discussed. The operation has been analysed under two different control modes, namely, CC and VC modes. A dual modulation control strategy has been proposed to regulate line current and capacitor voltages independently. A cascaded PI and lead compensator based controller has been proposed to improve the CFC transient performance during the transition. The performance of the CFC has been evaluated under steady state and a ramp power change on a three-terminal meshed dc grid through simulations and with the experiment platform. The results demonstrate that a 2B-CFC can be used to improve the grid controllability by rescheduling the grid power flow and limiting the line currents below thermal limits. A good agreement has been observed between the experimental and simulation results.

The impact of semiconductor on state voltage drop on CFC performance has been studied. It has been observed that in scaled systems, semiconductor on state voltage drop affects the dc grid power flow significantly. In the experimental platform, the impact of voltage drop has been minimised through using MOSFETs.

For completeness, the impact of CFC switching on dc side harmonics has been analysed. It has been observed that inclusion of CFC has increased the dc harmonic content, specially of the dc lines where CFC is installed.

5 Single H-bridge CFC (1B-CFC)

An inter-line CFC comprises two elements, namely, a by-pass element and a voltage source element. Fig. 5.1 shows two types of CFC arrangements having such a configuration. Type I consists of a voltage source element and two by-pass elements whereas Type II consists of two electrically coupled voltage source elements and two by-pass elements.



(a) Type I (b) Type II

Figure 5.1: Inter-line CFC module arrangements.

In Chapter 4, a Type II based CFC (2B-CFC) has been used to provide current regulation in a meshed dc grid. By-pass elements Q_1 and Q_2 are solely used to by-pass the voltage source elements when the required series dc voltage injections are zero. In Chapter 3, a capacitive based

CFC (Type-I) has been proposed which utilises the by-pass elements to provide the required series dc voltage injection. However, due to absence of a controllable voltage source element such as an H-bridge, the device operation is limited to two quadrants. This can be relieved by adding an H-bridge between the by-pass switches.

In this chapter, a new CFC topology (single H-bridge CFC or 1B-CFC) is derived to eliminate the operational limitations imposed by the C-CFC by adding an H-bridge based voltage source element between the by-pass elements of C-CFC. The characteristics, control and operation of the 1B-CFC are studied under a single modulation control. This concept is extended to multi-port CFC. The operation and control of a multi-port CFC with 3 ports are studied under a dual modulation control. Small scale prototypes of 1B and multi-port CFCs are designed and developed to experimentally study their impact on 3-terminal meshed HVdc grid operation. The performances the CFCs are evaluated a under line overloading condition.

5.1 Solid State Arrangement

Fig. 5.2 shows the switch arrangement of a 1B-CFC (Type I). The device consists of two by-pass switches (Q_1, Q_2) and a voltage source element (B_1). Switches Q_1 and Q_2 are realised with anti-series connected IGBT switches. The voltage source element B_1 comprises a capacitor and an H bridge which are electrically coupled. The H-bridge input terminals are connected to switches Q_1 and Q_2. A dc voltage is established on the capacitor in order to provide a voltage source for the current flow control.

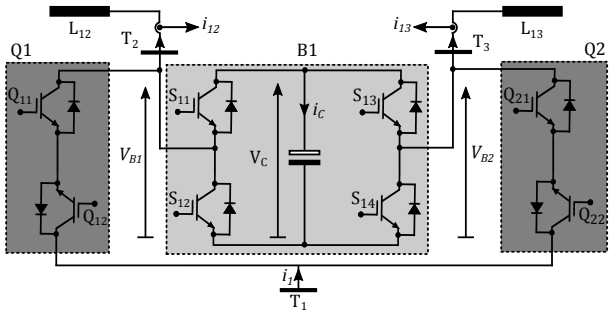


Figure 5.2: Topology of a 1B-CFC.

5.2 Operation and Control

5.2.1 Switching States

5.2.1.1 By-pass Mode

In this mode, B_1 is by-passed via setting the duty cycles of Q_1 and Q_2 to 1 (see Fig. 5.3). During this mode of operation, the inserted dc voltages in series with dc lines L_{12} and L_{13} are zero.

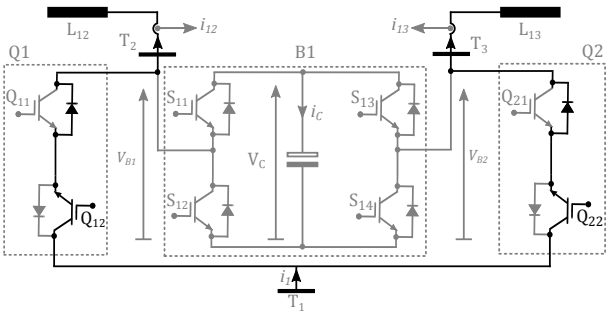
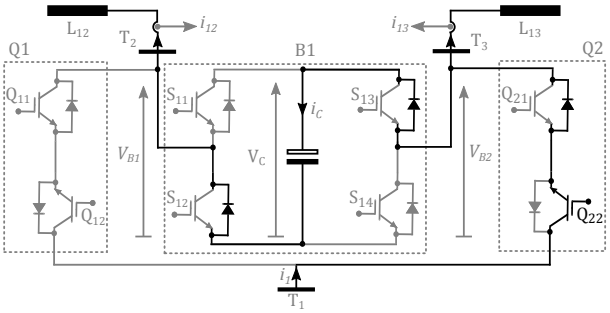


Figure 5.3: 1B under by-pass mode.

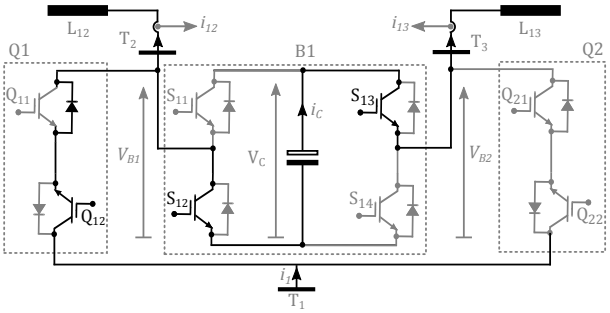
5.2.1.2 Current Control (CC) Mode

In CC mode, both by-pass switches Q_1 and Q_2 and the H-bridge are modulated to provide the required dc voltage injections in series with the congested lines, aiming to virtually increase or decrease their impedances and consequently alter their current flow. The active switches of Q_1 and Q_2 and H-bridge are selected depending on the line current direction and control objective. Let us assume that current flows from terminals T_1 to T_2 and from T_1 to T_3 and that it is desired to reduce the current flow in line L_{12}. In this scenario, switches Q_{12} of Q_1 , Q_{22} of Q_2, and S_{12} and S_{13} of bridge B1 are modulated, while all other switches (Q_{11}, Q_{21}, S_{11} and S_{14}) remain turned off. Q_{12} and Q_{22} are modulated complementarily to avoid any interruption in the current flow i_1 of the converter.

The operational stages of the CFC during the CC mode are shown in Fig. 5.4. The switching states of the controlled switches and the corresponding changes on the bridge voltages are shown in Fig. 5.5. When switches Q_{12}, S_{12} and S_{13} are off (i.e Q_{22} is on), the line current i_{12} flows through switch Q_2 and the naturally commutated diodes of bridge B1 and charges the capacitor



(a) Charging mode



(b) Discharging mode

Figure 5.4: Operational stages of 1B CFC in CC mode.

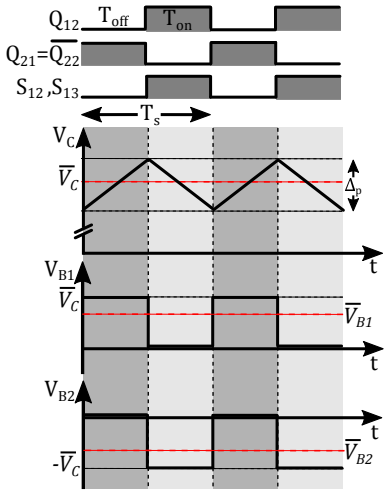


Figure 5.5: Switching waveforms of 1B under CC mode.

rapidly. During this period, the voltage across terminals T_1 and T_2 is V_C and zero across T_1 and T_3. Thus, current i_{12} decreases. Since there are no changes in power demand or voltage references, the total current out of T_1 remains same. This implies that the current on the other line, L_{12}, must increase to maintain the current balance. During this period the inserted dc

voltages V_{B1} and V_{B2} can be expressed as follows:

$$\begin{aligned} V_{\mathrm{B1,off}} &= \overline{V}_{\mathrm{C}} \\ V_{\mathrm{B2,off}} &= 0 \end{aligned} \tag{5.1}$$

where $\overline{V}_{\mathrm{C}}$ is the average value of capacitor voltage V_{C}.

A negative voltage must be inserted in series with L_{13} to increase line current i_{13}. This can be achieved by switching on Q_{12}, S_{12} and S_{13} (see Fig. 5.4(b)). During this period the capacitor is discharged into L_{13}. The inserted dc voltages V_{B1} and V_{B2} can be given by the following equations:

$$\begin{aligned} V_{\mathrm{B1,on}} &= 0 \\ V_{\mathrm{B2,on}} &= -\overline{V}_{\mathrm{C}} \end{aligned} \tag{5.2}$$

As shown in Fig. 5.5, continuous switching of by-pass modules and H-bridge generates pulsed positive (V_{B1}) and negative (V_{B2}) dc voltages across the CFC terminals T_1 and T_2, and T_1 and T_3, respectively. This increases i_{13} and decreases i_{12}. The average values of inserted dc voltages V_{B1} and V_{B2} can be given by the following equations:

$$\begin{aligned} \overline{V}_{\mathrm{B1}} &= \frac{V_{\mathrm{B1,off}} \cdot T_{\mathrm{off}} + V_{\mathrm{B1,on}} \cdot T_{\mathrm{on}}}{T_{\mathrm{s}}} \\ &= \frac{\overline{V}_{\mathrm{C}} \cdot T_{\mathrm{off}}}{T_{\mathrm{s}}} \\ &= \overline{V}_{\mathrm{C}}(1-D) \end{aligned} \tag{5.3}$$

$$\begin{aligned} \overline{V}_{\mathrm{B2}} &= \frac{V_{\mathrm{B2,off}} \cdot T_{\mathrm{off}} + V_{\mathrm{B2,on}} \cdot T_{\mathrm{on}}}{T_{\mathrm{s}}} \\ &= \frac{-\overline{V}_{\mathrm{C}} \cdot T_{\mathrm{on}}}{T_{\mathrm{s}}} \\ &= -\overline{V}_{\mathrm{C}} \cdot D \end{aligned} \tag{5.4}$$

In steady state, the peak-to-peak ripple Δ_p on capacitor voltage V_C can be estimated by the

following equation:

$$\begin{aligned}\Delta_p &= i_{12} \cdot \frac{T_{\text{off}}}{C_{\text{CFC}}} \\ &= i_{13} \cdot \frac{T_{\text{on}}}{C_{\text{CFC}}}\end{aligned} \tag{5.5}$$

In this configuration, the power taken from one line is equal to the power added to the other line. The power balancing between switches Q_1 and Q_2 can be represented by the following equation:

$$\begin{aligned}\overline{V}_{\text{B1}} \cdot i_{12} + \overline{V}_{\text{B2}} \cdot i_{13} = 0 \\ \overline{V}_{\text{C}}(1-D) i_{12} - \overline{V}_{\text{C}} \cdot D \cdot i_{13} = 0\end{aligned} \tag{5.6}$$

5.2.2 Controller design

A single modulation controller, shown in Fig. 5.6, is proposed to control the 1B-CFC. It consists of an inner capacitor voltage control loop cascaded with an outer line current control loop. The outer loop regulates the dc line current by generating a reference signal $V_{\text{C,ref}}$ to the inner voltage controller. As discussed in Chapter 4, the uncompensated system, $G_v(s)$, exhibits a poor phase margin. Therefore, to improve the phase margin and to ensure a good performance during transients, a compensator based capacitor voltage controller $G_k(s)$ is proposed. The $G_k(s)$ and system $G_v(s)$ can be expressed by the following transfer functions:

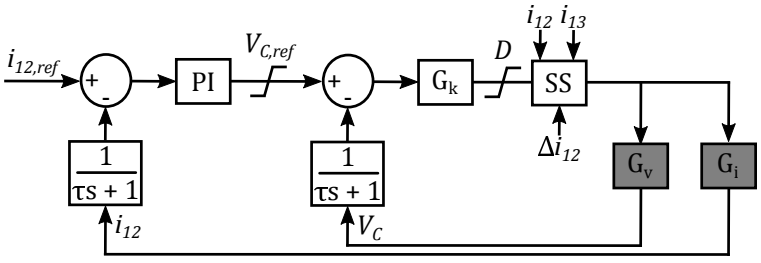


Figure 5.6: 1B-CFC controller.

$$G_v(s) = K_c \left(\frac{(L_{12}+L_{13})s + (R_{12}+R_{13})}{L_{12}s + R_{12}} \right) \cdot \left(\frac{1}{L_{13}Cs^2 + R_{13}Cs + 1} \right) \tag{5.7}$$

$$G_k(s) = K\left(\frac{s+z_c}{s+p_c}\right)\left(\frac{s+z_p}{s}\right) \tag{5.8}$$

where L_{12} and R_{12} represent the inductive and resistive parts of line 12; L_{13} and R_{13} represent the inductive and resistive parts of line 13; C represent CFC capacitor. G_k(s) in (5.8) consists of a PI structure cascaded with a lead compensator, where z_p is the zero of the PI controller, z_c and p_c are the zero and pole of the lead compensator, and K is the overall controller gain.

By assuming the current controller open loop response time is ten times slower than the response time of voltage controller, the inner-loop can be represented by a gain of 1. Thus, the outer loop plant can be simplified to a first order function $G_i(s)$. The transfer function $G_i(s)$ can be represented by:

$$G_i(s) = \frac{1}{L_{12}s + R_{12}} \tag{5.9}$$

Therefore, a PI controller is sufficient to regulate the line current to achieve a good control performance. It should be highlighted that a first order filter with a cut-off frequency of 200 Hz has been employed with the aforementioned voltage and current controllers to eliminate measurement noise. The control parameters can be found in Appendix B. It must be emphasised that a 1B-CFC can be employed with a dual modulation controller as it comprises a controllable voltage element where both line current and capacitor voltage can be independently controlled. This is demonstrated in Section 5.3 by adopting a dual modulation controller to control a 1B based multi-port CFC.

Fig. 5.7 shows the switch section of 1B CFC under the single modulation control. Switching patterns are provided for four quadrant operation, where the quadrants are defined by the direction of the line currents. The switching sequence is determined by the direction of currents i_{12}, i_{13} and i_1. The increment and decrement in bridge currents are represented by the arrow direction. During CC mode, four switches are modulated to provide the current control. For instance, when currents i_{12}, i_{13} and i_1 are positive, to decrease the current flow on line L_{12}, switches Q_{12} of Q_1 , Q_{21} of Q_2 and S_{12} and S_{13} of bridge B1 must be modulated. Under single modulation, Q_{12}, S_{12} and S_{13} are switched simultaneously whereas a complementary gating

pulse is used to trigger Q_{21}.

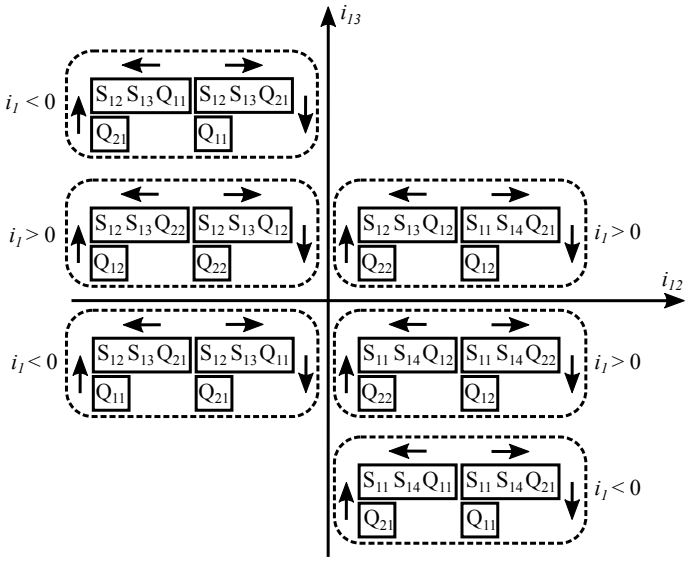


Figure 5.7: 1B-CFC switch selection in CC mode

5.3 Multi-port CFC

The operation of inter-line power flow controllers can be affected by dc cable outage and internal failures. As discussed in previous chapters, the installation of a CFC could reduce the cable failure rate by avoiding the operation of dc cables above their thermal or electric stress limits. However, a failure of an HVdc cable or an overhead line is very is influenced by many aspects such as cable degradation and natural disasters. Additional important factors affecting the operation of the CFC are internal failures in semiconductor modules, gate drivers and mechanical failures.

In presence of more than two lines, a 2-port CFC as discussed in Section 5.2 is capable of adjusting the current flow through an uncompensated line . However, failure of a port or dc line where the CFC is installed could force the device go offline, which may lead to unregulated line currents. Under such conditions, a multi-port CFC could be better solution in terms of control flexibility, reliability and cost.

5.3.1 Solid State Arrangement

Fig. 5.8 depicts the schematic diagram of a 1B based multi-port system with n ports. The device consists of n number of by-pass switches ($Q_1 \rightarrow Q_n$), n number of half bridges ($B_1 \rightarrow B_n$) and a capacitor. The by-pass switches are realised with anti-series connected IGBTs. Device terminal T_1 is connected to a VSC whereas other terminals are connected to dc lines.

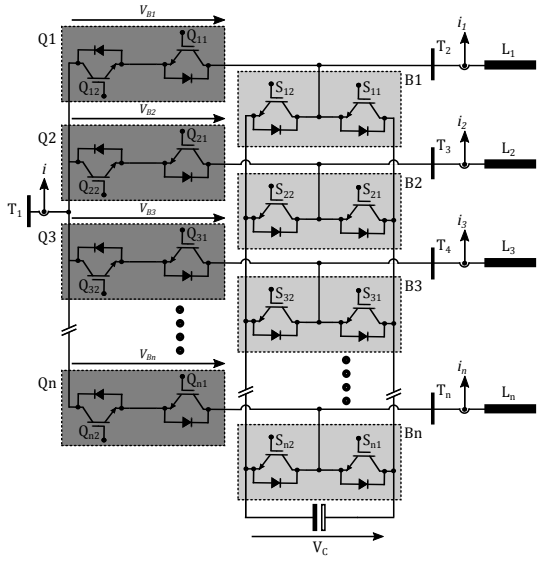


Figure 5.8: Multi-port CFC

An n-port CFC can be used regulate $n-1$ dc line currents simultaneously or individually whereas the remaining port acts as a master port which compensates the net change in other line currents magnitudes. A three port 1B-CFC, as shown in Fig. 5.9, is used here to study the operation and

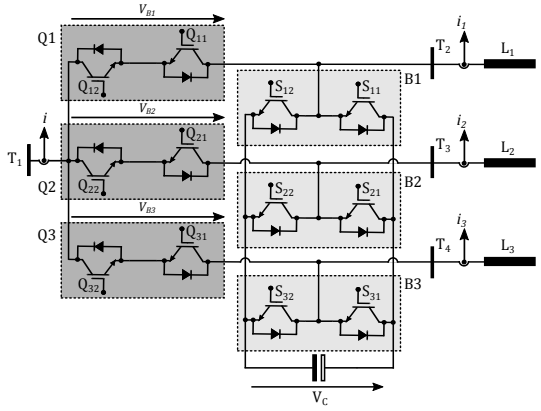


Figure 5.9: Topology of a 3-port based multi-port.

control of a multi-port CFC. The device consists of three by-pass switches (Q_1, Q_2, Q_3), three half bridges (B_1, B_2, B_3) and a capacitor. Q_1, Q_2 and Q_3 are connected in series with lines L_1, L_2 and L_3, respectively. Terminal T_1 is connected to a VSC whereas T_2, T_3 and T_4 are connected to dc lines L_1, L_2 and L_3, respectively.

5.3.2 Operation

5.3.2.1 By-pass mode

This mode of operation is adopted when the required line current reduction or increment is zero. During this period, the voltage source element is by-passed by turning on switches Q_1, Q_2 and Q_3 (Fig. 5.10).

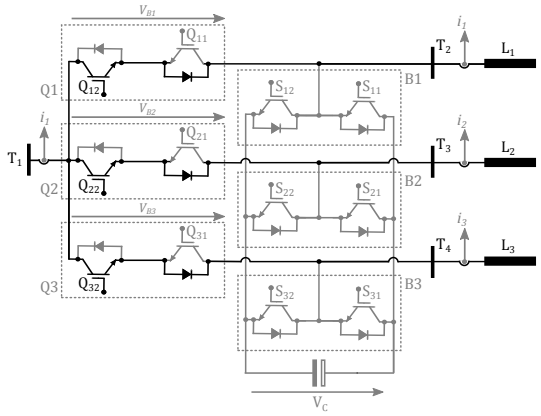


Figure 5.10: Multi-port CFC in by-pass mode.

5.3.2.2 Current control (CC) mode

A dual modulation controller as proposed in Chapter 4 is adopted to control the multi-port CFC. The line currents and capacitor voltages are regulated independently by modulating the by-pass elements (Q_1, Q_2 and Q_3) and voltage source element (B_1, B_2 and B_3), respectively. Since there are 3-ports, currents on two dc lines can be independently controlled. Fig. 5.11 shows the switching states of the multi-port CFC for current flows from terminals T_1 to T_2, from T_1 to T_3 and from T_1 to T_4. The switching states of the controlled switches and the corresponding changes on the bridge voltages are shown in Fig. 5.12. In this case, the CFC is requested to decrease current in line L_1 and increases the current in line L_2. Switches Q_{12} of Q_1 and Q_{22} of

Q_2 are modulated to control line currents i_1 and i_2, respectively. Switch Q_{32} of Q_3 is set be on to avoid any interruption to converter current i when both switches Q_{12} and Q_{22} are off. Switches S_{12}, S_{21} and S_{31} of half bridge modules B_1, B_2 and B_3, respectively, are modulated to control the capacitor voltage.

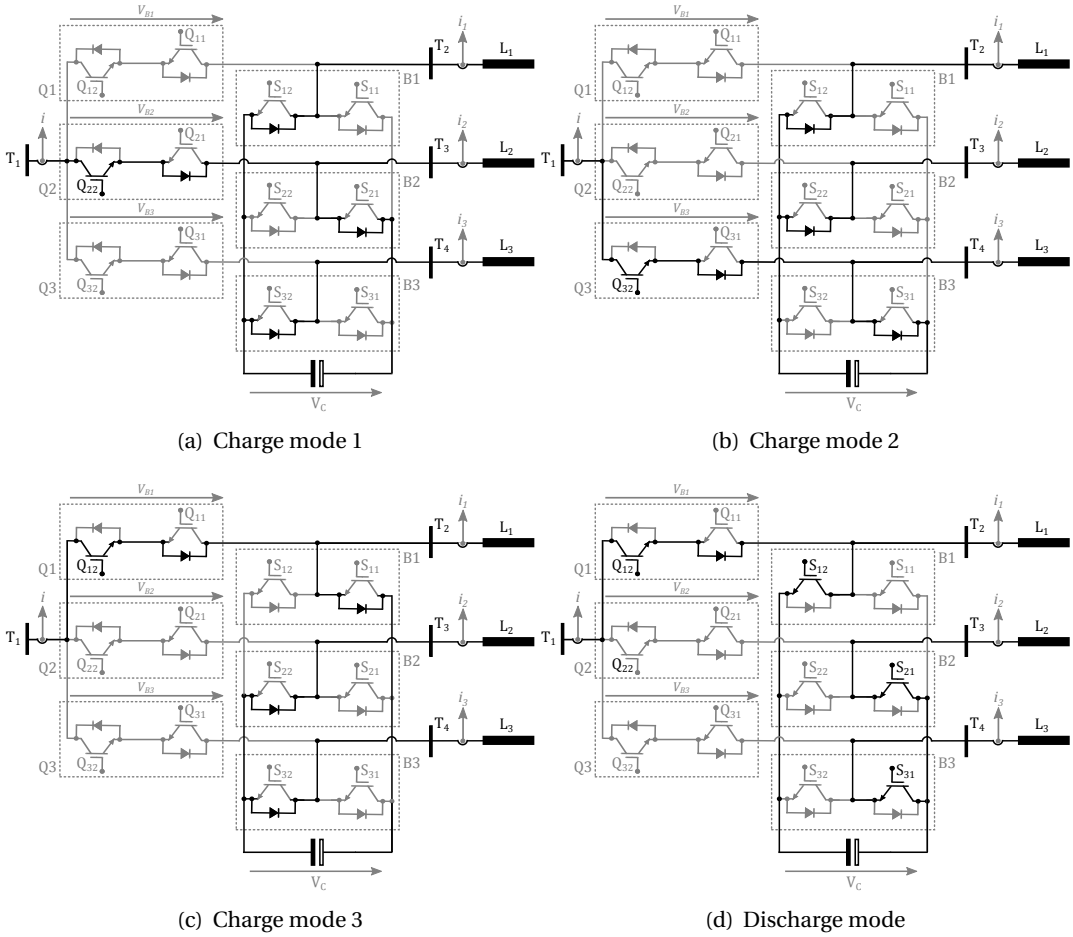


Figure 5.11: Operational stages of multi-port CFC under CCM.

When Q_{22} is in an on state and other switches are turned off, as showed in Fig. 5.11(a), the line currents flow through Q_2 and the naturally commutated diodes of the half-bridges, which charges the capacitor. During this interval inserted series dc voltages can be given by:

$$\begin{aligned} V_{B1,a} &= \overline{V}_{\mathrm{C}} \\ V_{B2,a} &= 0 \\ V_{B3,a} &= \overline{V}_{\mathrm{C}} \end{aligned} \tag{5.10}$$

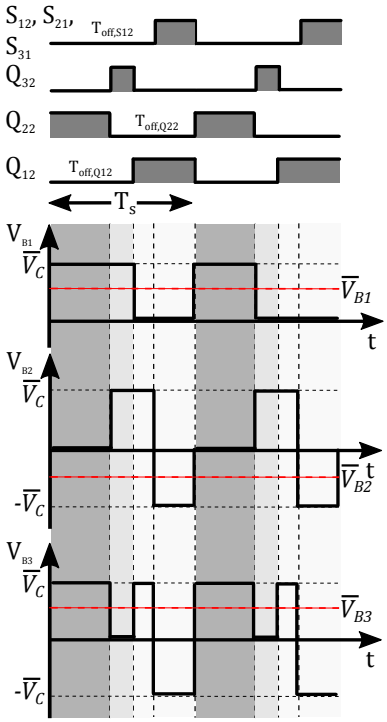


Figure 5.12: Switching waveforms.

As shown in Fig. 5.11(b), when Q_{32} is turned on and the other switches are off, the line currents flow through Q_3 and the naturally commutated diodes of the half-bridges and charge the capacitor rapidly. During this period, the inserted series dc voltages can be given by:

$$\begin{aligned} V_{B1,b} &= \overline{V}_{\mathrm{C}} \\ V_{B2,b} &= \overline{V}_{\mathrm{C}} \\ V_{B3,b} &= 0 \end{aligned} \tag{5.11}$$

When Q_{12} is on and other switches are off (Fig. 5.11(c)), the line currents flow through Q_1 and through the naturally commutated diodes of the half-bridges and this charges the capacitor rapidly. During this period, the inserted series dc voltages can be given by:

$$\begin{aligned} V_{B1,c} &= 0 \\ V_{B2,c} &= \overline{V}_{\mathrm{C}} \\ V_{B3,c} &= \overline{V}_{\mathrm{C}} \end{aligned} \tag{5.12}$$

To maintain the power balance, the capacitor must be discharged into at least one of the dc lines. In this case, the capacitor is discharged into L_2 and L_3 by turning on Q_{12}, S_{12}, S_{21} and S_{31} (Fig. 5.11(d)). During this period, the inserted series dc voltages can be given by:

$$\begin{aligned} V_{B1,d} &= 0 \\ V_{B2,d} &= -\overline{V}_{\mathrm{C}} \\ V_{B3,d} &= -\overline{V}_{\mathrm{C}} \end{aligned} \tag{5.13}$$

From eqs. (5.10) to (5.13), the average values of bridge voltages V_{B1}, V_{B2} and V_{B3} can be derived as follows:

$$\begin{aligned} \overline{V}_{B1} &= \frac{V_{B1,a}\cdot T_{\mathrm{on,Q22}} + V_{B1,b}(T_{\mathrm{off,Q12}} - T_{\mathrm{on,Q22}}) + V_{B1,c}(T_{\mathrm{on,Q12}} - T_{\mathrm{on,S12}}) + V_{B1,d}\cdot T_{\mathrm{on,S12}}}{T_{\mathrm{s}}} \\ &= \frac{\overline{V}_{\mathrm{C}}\cdot T_{\mathrm{on,Q22}} + \overline{V}_{\mathrm{C}}(T_{\mathrm{off,Q12}} - T_{\mathrm{on,Q22}})}{T_{\mathrm{s}}} \\ &= \overline{V}_{\mathrm{C}}(1-D_1) \end{aligned} \tag{5.14}$$

$$\begin{aligned} \overline{V}_{B2} &= \frac{V_{B2,a}\cdot T_{\mathrm{on,Q22}} + V_{B2,b}(T_{\mathrm{off,Q12}} - T_{\mathrm{on,Q22}}) + V_{B2,c}(T_{\mathrm{on,Q12}} - T_{\mathrm{on,S12}}) + V_{B2,d}\cdot T_{\mathrm{on,S12}}}{T_{\mathrm{s}}} \\ &= \frac{\overline{V}_{\mathrm{C}}(T_{\mathrm{off,Q12}} - T_{\mathrm{on,Q22}}) + \overline{V}_{\mathrm{C}}(T_{\mathrm{on,Q12}} - T_{\mathrm{on,S12}}) - \overline{V}_{\mathrm{C}}\cdot T_{\mathrm{on,S12}}}{T_{\mathrm{s}}} \\ &= \overline{V}_{\mathrm{C}}(1-D_2-2\cdot D_3) \end{aligned} \tag{5.15}$$

$$\begin{aligned} \overline{V}_{B3} &= \frac{V_{B3,a}\cdot T_{\mathrm{on,Q22}} + V_{B3,b}(T_{\mathrm{off,Q12}} - T_{\mathrm{on,Q22}}) + V_{B3,c}(T_{\mathrm{on,Q12}} - T_{\mathrm{on,S12}}) + V_{B3,d}\cdot T_{\mathrm{on,S12}}}{T_{\mathrm{s}}} \\ &= \frac{\overline{V}_{\mathrm{C}}\cdot T_{\mathrm{on,Q22}} + \overline{V}_{\mathrm{C}}(T_{\mathrm{on,Q12}} - T_{\mathrm{on,S12}}) - \overline{V}_{\mathrm{C}}\cdot T_{\mathrm{on,S12}}}{T_{\mathrm{s}}} \\ &= \overline{V}_{\mathrm{C}}(D_1+D_2-2\cdot D_3) \end{aligned} \tag{5.16}$$

where D_1, D_2 and D_3 are duty cycle of switches Q_{12}, Q_{22} and S_{12}/ S_{21}/ S_{31}; with $D_1 = \frac{T_{\text{on,Q12}}}{T_\text{s}}$, $D_2 = \frac{T_{\text{on,Q22}}}{T_\text{s}}$ and $D_3 = \frac{T_{\text{on,S12}}}{T_\text{s}}$.

The power balance between the bridges can be represented by the following equation:

$$\begin{aligned} \overline{V}_{B1} \cdot i_1 + \overline{V}_{B2} \cdot i_2 + \overline{V}_{B3} \cdot i_3 &= 0 \\ \overline{V}_\text{C}(1-D_1) i_1 + \overline{V}_\text{C}(1-D_2-2\cdot D_3) i_2 + \overline{V}_\text{C}(D_1+D_2-2\cdot D_3) i_3 &= 0 \end{aligned} \tag{5.17}$$

According to Kirchhoff's current law, the current entering and leaving the CFC must be equal to zero. Therefore, a change in one line current must be equal to the net change in other dc line currents. For example, let assume that i, i_1, i_2 and i_3 are > 0 and a current reduction of Δi is requested on line L_1. The new line current, $i_{1,new}$, through port 1 can be given by the following equation:

$$i_{1,new} = i_1 - \Delta i \tag{5.18}$$

Since the total current entering and leaving the CFC must be equal, net change in currents through port 2 and port 3 must be equal to Δi. Therefore, the new currents, $i_{2,new}$ and $i_{3,new}$ through ports 2 and 3 can be given by the following equations:

$$\begin{aligned} i_{2,new} &= i_2 + n\Delta i \\ i_{3,new} &= i_3 + (1-n)\Delta i \end{aligned} \tag{5.19}$$

Where n determine the current sharing between ports 2 and 3. Currents through ports 2 and 3 can be reversed by setting $n < 0$ and $n > 1$, respectively.

It must highlighted that only selected switching states are presented under CC mode. The CFC could take different switching states besides the aforementioned ones depending on control objective, system parameters and operating point.

5.4 Controller Design

5.4.1 Voltage controller

Fig. 5.13 depicts the capacitor voltage controller. Controller $G_k(s)$ is formed by a cascaded PI controller and lead compensator as proposed in Section 5.2.2. The controller maintains a constant voltage across the capacitor by adjusting the duty cycle D_3 of switches S_{12}, S_{21} and S_{31} of bridges $B1$, $B2$, and $B3$, respectively. Thus, during CC mode, all three switches receive the same PWM signal. A low pass filter with a cut-off frequency of 200 Hz is used to remove the noise and high frequency components from the measured capacitor voltage.

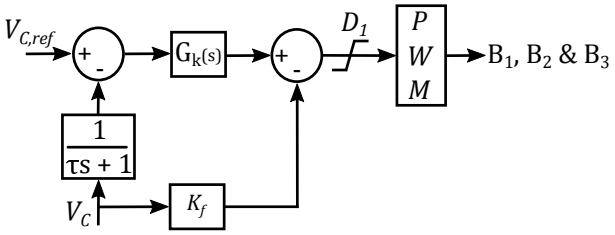


Figure 5.13: CFC capacitor voltage controller

5.4.2 Current controller

Fig. 5.14 shows the control block diagram of line current controller. Line currents i_1 and i_2 are independently regulated using PI controllers. A NOR logic gate is used to generate the gating pulse for switch Q_{32}. The gate pluses of switches Q_{12} and Q_{22} are used as inputs to the NOR gate. This ensures uninterrupted converter current, i, flow during the CC mode.

5.5 Simulation and Experimental Validation

5.5.1 Experimental Set-up

The 3-terminal meshed MTdc grid shown in Fig. 5.15 is used to validate the operation and control of 1B-CFCs. The VSC terminals have been arranged in a symmetrical monopole configuration and rated at ±125 V and 2 kW. To establish a bipole operation, CFC modules P and N are installed in series with both the positive and negative poles of lines L_{12} and L_{13}. The test-rig specifications

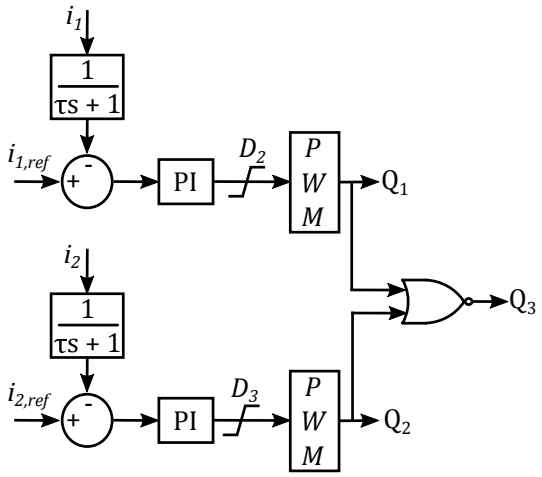


Figure 5.14: Line current controller

are provided in Table 3.2 of Chapter 3. The module specifications are provided in Table 5.1. The MOSFETs are used as counterpart of IGBTs to minimise the impact of forward voltage drop on current control. A switching frequency of 2000 Hz is adopted to modulate the switches CFC.

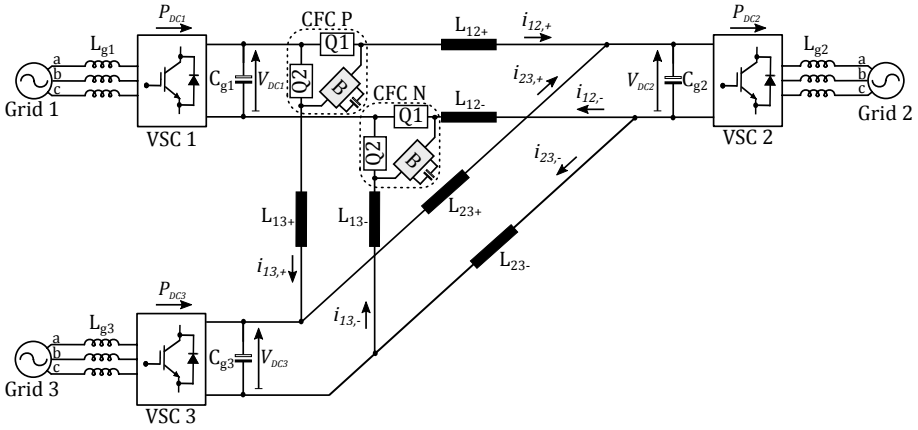


Figure 5.15: Three-terminal MTdc grid with embedded 1B-CFCs.

5.6 Validation

The results in this section are expressed in per unit considering the following power, voltage and current bases: 2 kW, 125 V, and 8 A. VSCs 1 and 3 are initially set to inject 0.8 and 0.2 p.u. into the MTdc grid, whereas VSC 2 has been designated as a slack busbar that maintains the grid power balance (*i.e.*, maintains a constant dc voltage).

Table 5.1: Specifications and parameters: 1B-CFCs

Devices	Specifications	Operating rating
CFC	Rated power Rated dc voltage	40W 10 V
DC capacitor	C_{CFC}	4400 μF
Switching frequency	f_{sw}	2000 Hz
MOSFET	Model: PSMN3R8-100BS typical V_d=0.8 V	

5.6.1 Line overload elimination using 1B-CFC

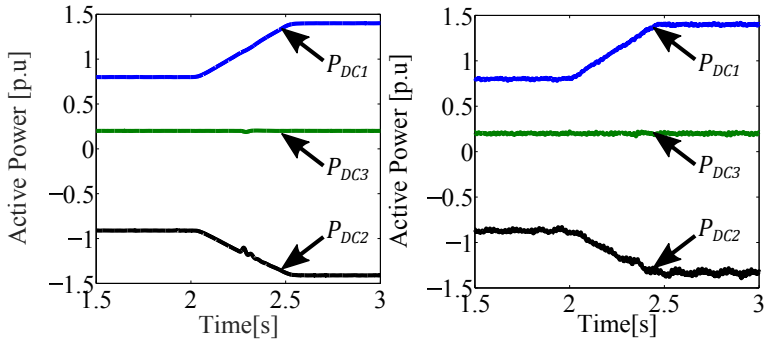
The performance of 1B-CFCs is assessed by means of a simulation and an experiment following a ramp power change through VSC 1. The simulation has been carried out using Simulink/SimPowerSystems block sets. The CFCs are placed at the positive and negative poles of lines L_{12} and L_{13} to enable bi-pole operation.

The simulation (left) and experimental results (right) are shown in Figs. 5.16 to 5.18. Initially, the voltage source element is by-passed via turning on switches Q_1 and Q_2. At $t = 2$ s, a positive ramp power change of 0.6 p.u. is applied though VSC 1 (Figs. 5.16(a)) by adjusting power reference set point from 0.8 to 1.4 p.u. The additional power injection causes the converter current i_1 to increase. Thus, line currents $i_{12,+}$ (Figs. 5.16(b)) and $i_{13,-}$ (Figs. 5.16(c)) exceed the maximum thermal current limit of 1 p.u. Following the overload detection, the CFCs are requested to reduce the line current to 0.5 p.u. Since converters 1 and 3 are in power control mode (see Fig. 3.24(b) of Chapter 3), their terminal voltages have increased further to maintain the grid power balance (Fig. 5.16(d)). It can be observed both in simulation and experimental results that the terminal voltage of the master converter (V_{DC2}) deviates from its reference value to prevent the VSCs from entering into over-modulation.

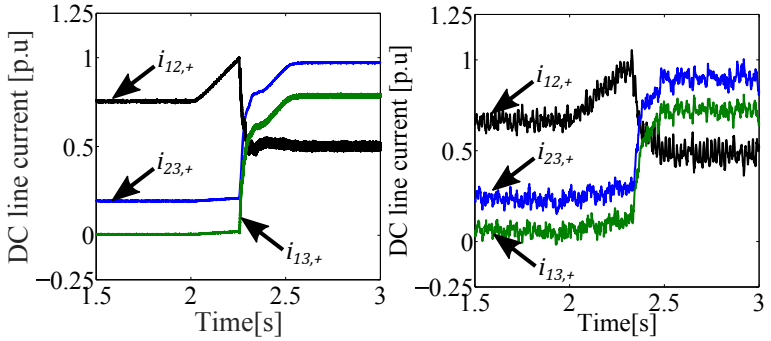
Figs. 5.17 and 5.18 provide the voltage profiles of the positive pole and negative pole CFCs, respectively. The required capacitor voltages are determined by the outer current control. For the experiment, the capacitor voltages are maintained at 0.035 p.u., as shown by Figs. 5.17(a)and 5.18(a), whereas in the simulation the capacitor voltages are maintained at 0.039 p.u. The observed mismatches are caused by forward voltage drops in diodes and converter power losses

in the experimental platform. The impact of semiconductor voltage drop on line current control has been analysed in Chapter 4. The inserted mean dc voltages of positive and negative CFCs are shown in Fig. 5.17(b) and Fig. 5.18(b), respectively.

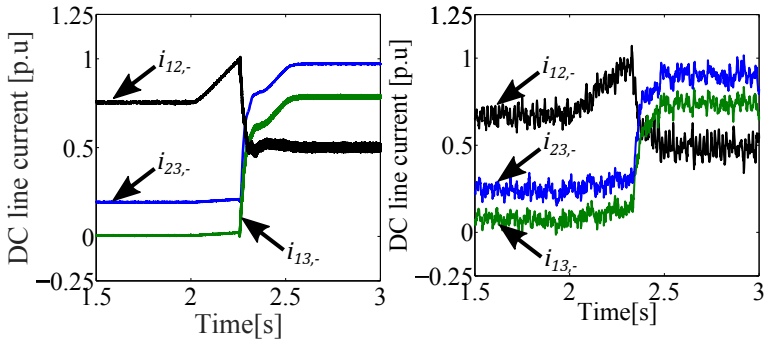
It must be highlighted that since the system under study is a lightly meshed dc grid, in the experimental platform, line overloading can only be achieved through setting the converter power to 1.4 p.u. Therefore, it is assumed that converters can with stand a power injection of 1.4 p.u. However, it must be emphasized that in a densely meshed dc grid, dc lines could surpass their thermal limit while the converters are within their power ratings.



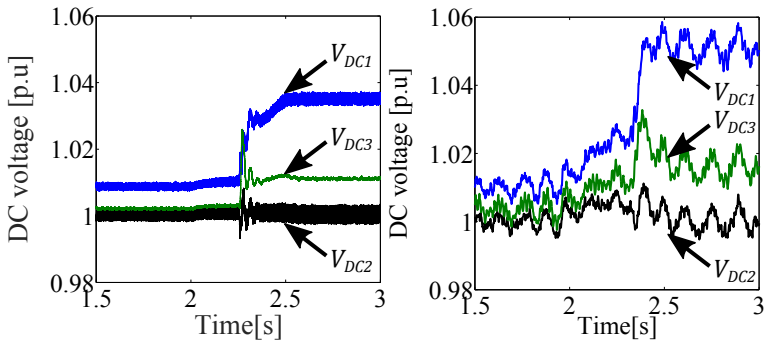
(a) VSC active power



(b) DC line current (positive pole)

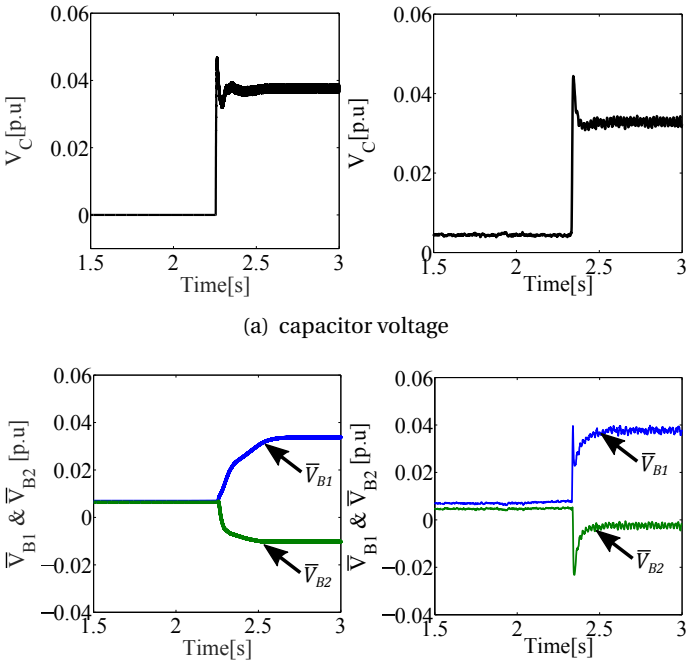


(c) DC line current (negative pole



(d) DC terminal voltage

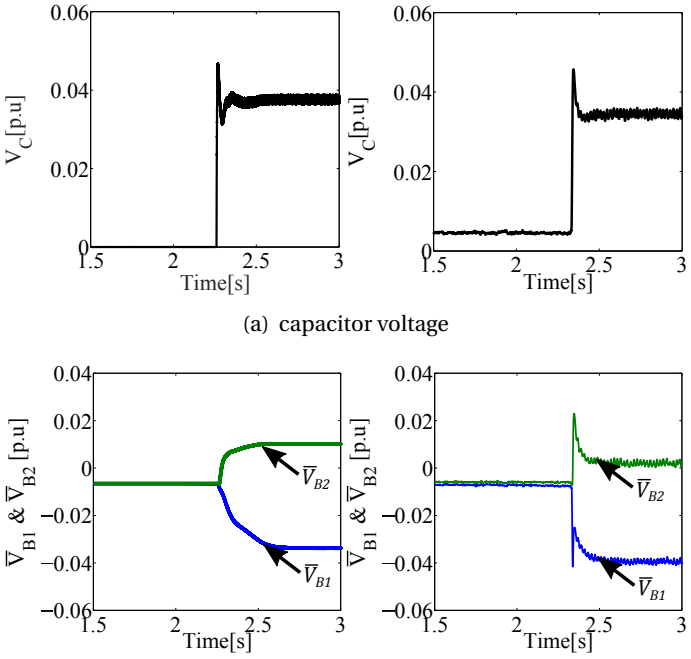
Figure 5.16: DC grid response for a ramp change in power with embedded 1B-CFCs. Simulation (left) and experimental (right) results.



(a) capacitor voltage

(b) inserted mean dc voltages

Figure 5.17: Response of the 1B-CFC located at the positive pole for a ramp change in power. Simulation (left) and experimental (right) results.



(a) capacitor voltage

(b) inserted mean dc voltages

Figure 5.18: Response of the 1B-CFC located at the negative pole for a ramp change in power. Simulation (left) and experimental (right) results.

5.6.2 Line overload elimination using multi-port CFC

The performance of the multi-port CFC is assessed on a point-point network, as shown Fig. 5.19, following a ramp change in power. The dc network is formed by three parallel connected dc lines with different line impedances. The CFC by-pass elements Q_1, Q_2 and Q_3 are connected in series with lines $L_{1,+}$, $L_{2,+}$ and $L_{3,+}$, respectively. The module specifications provided in Table 5.1 are used to develop the multi-port prototype. The dc lines and converter parameters are provided in Table B.1 of Appendix B. Initially, VSC 1 is set to inject 1 p.u. , whereas VSC 2 has been assigned as the master converter.

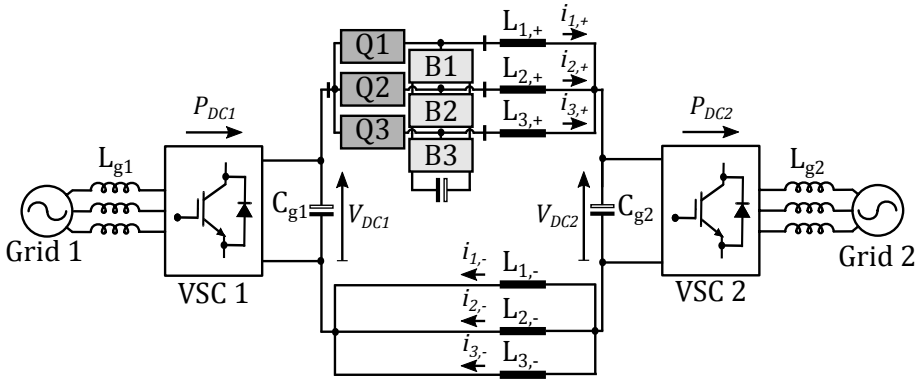
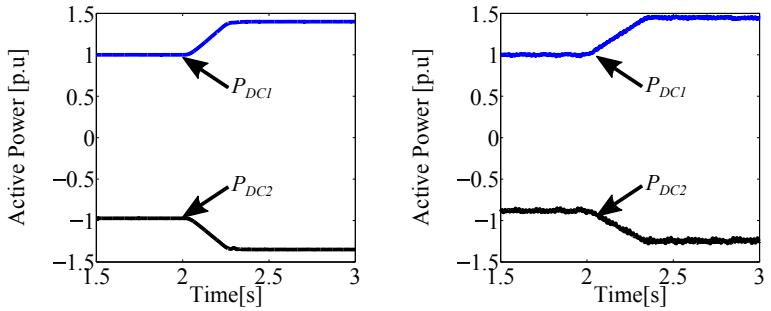
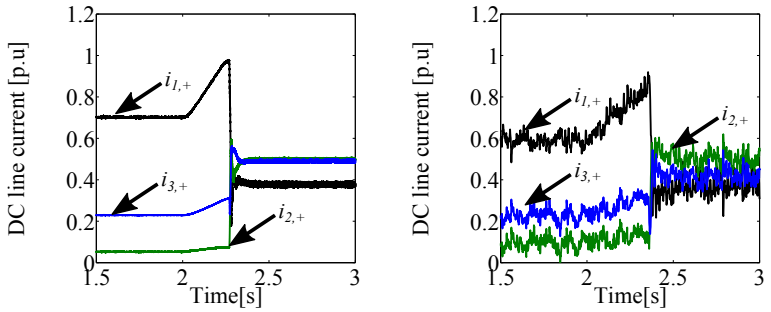


Figure 5.19: 3-terminal MTdc with embedded CFCs

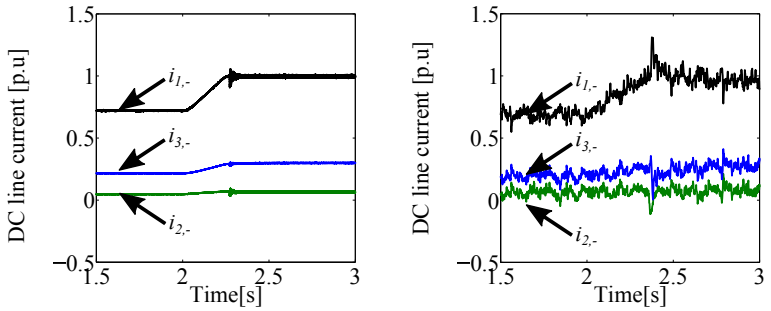
The dc grid responses and CFC voltage profiles are shown in Fig. 5.20 and Fig. 5.21, respectively. At $t = 2$ s, power through VSC 1 is set to increase from 1 to 1.4 p.u. (Figs. 5.20(a)). Following the ramp change, line currents start increasing where most part of the converter current flows through line L_1 due to low line impedance. In by-pass mode, line $L_{1,-}$ carries more current than line $L_{1,+}$ as the positive pole current distribution is affected by diode forward voltage drop. After the ramp power change, current on line $L_{1,-}$ exceeds 1 p.u. whereas maximum current on line $L_{1,+}$ is limited below 1 p.u. Hence, to demonstrate the performance of a multi-port CFC under a line overloading condition, the thermal limit threshold is reduced from 1 p.u. to 0.9 p.u. Following the overload detection, the CFC is enabled to reduce line current $i_{1,+}$ to 0.375 p.u. while it is requested increase $i_{2,+}$ to 0.5 p.u. In the CC mode, the capacitor voltage, V_C is maintained at 0.04 p.u. The mean dc voltages $\overline{V}_{B1}$, $\overline{V}_{B2}$ and $\overline{V}_{B3}$ are inserted in series with dc lines $L_{1,+}$, $L_{2,+}$ and $L_{3,+}$, respectively.



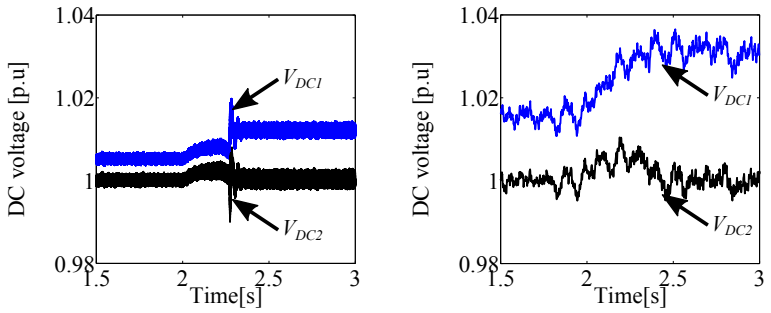
(a) VSC active power



(b) DC line current (positive pole)

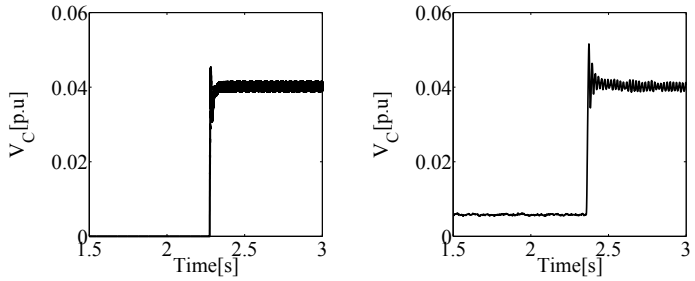


(c) DC line current (negative pole

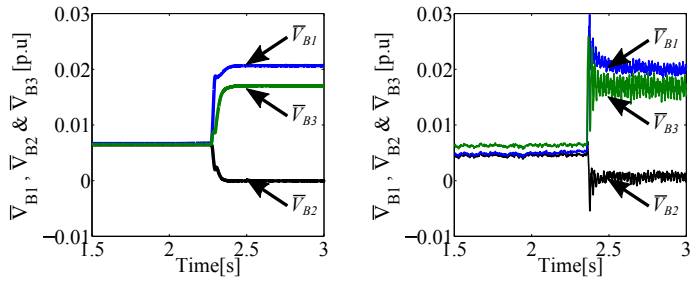


(d) DC terminal voltage

Figure 5.20: DC grid response for a ramp change in power with embedded multi-port CFC. Simulation (left) and experimental (right) results.



(a) capacitor voltage



(b) inserted mean dc voltages

Figure 5.21: Response of the multi-port CFC located at the positive pole for a ramp change in power. Simulation (left) and experimental (right) results.

5.7 Conclusions

In this chapter, 1B-CFC have been introduced to overcome the shortcoming of a C-CFC. The operation and control of a 1B-CFC have been studied under single modulation control. The concept has been experimentally validated in a meshed MTdc grid test-rig against simulation results. A multi-port CFC has been derived from the 1B-CFC to increase the control flexibility and to eliminate contingencies arising from the failure of a single or multiple ports. Furthermore, the operation and control of a multi-port CFC has been experimentally validated. A dual modulation control scheme has been adopted to control the multi-port CFC. The results demonstrate that a multi-port CFC can be used to simultaneously regulate multiple dc line currents.

6 Hierarchical Control and Protection of CFCs in MTdc Grids

In previous chapters, the CFCs have been controlled using local measurements and the references are set locally. In a large network and in presence of multiple CFCs, use of communication free control schemes solely based on local control measurements could lead to conflict between CFCs. The required amount of series dc voltage compensation for current control is affected by the location of a CFC. When more than one CFCs are available for current control, a CFC with low dc voltage requirement must be selected to reduce the system losses and stress level on the device. Therefore, a hierarchical control system is essential to enhance the dc grid reliability and performance by coordinating the operation between CFCs by optimising the required dc voltage compensation.

In this chapter, a novel centralised hierarchical control scheme is designed to coordinate the operation between multiple CFCs. Moreover, a new control strategy is proposed to increase the grid control flexibility during CFC overloading and absence of communications, with the CFC performance being assessed under such conditions. The proposed methodologies are validated through both simulation and experimental results. Furthermore, the performances of 1B and 2B CFC topologies under dc faults are presented. Such an assessment provides an insight into device protection aiming towards improving the existing configurations to ensure the reliability of a dc grid. Small-scale solid-state DCCBs have been implemented to assess the performances of 1B and 2B CFCs under pole-to-pole dc faults, with the interaction between the DCCB and the CFC during fault conditions being analysed. Impact of CFC switching on dc side harmonics is analysed.

6.1 CFC Hierarchical Control Layout

In a complex dc grid, flexible current regulation might not be achieved with a single CFC. This shortcoming can be relieved by installing CFCs at different locations. Under such a scenario, a centralised control scheme is essential to coordinate the operation among the devices. Fig. 6.1 illustrates the hierarchical control system when multiple CFCs are employed in a meshed-connected MTdc system. The control system consists of a centralised remote control centre (RCC) along with multiple local controllers (LCs). Each CFC is assigned to an LC.

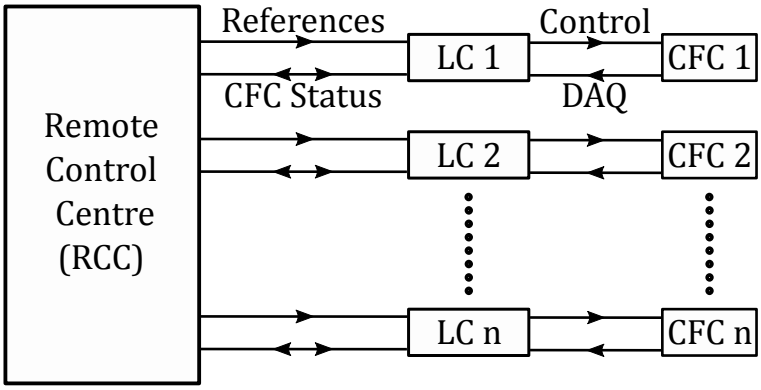


Figure 6.1: CFC Hierarchical control

6.1.1 Remote Control Centre

The RCC monitors the grid power flow and calculates the required voltage and current reference values prior to scheduled power changes, energy trade or system maintenance (for instance, involving the disconnection of a dc cable). In General, the Newton-Raphson algorithm is used to solve power flows in power systems [81, 82, 83]. The Newton-Raphson algorithm could become slower when system becomes more complex or the perturbation is poorly chosen [84]. However, dc grids require an algorithm which should be faster. This issue can be overcome by using the Broyden algorithm. The Broyden is a quasi-Newton based algorithm which is faster than the Newton Raphson method and exhibits less sensitiveness towards the perturbation [84, 85, 86]. Although Broyden method is faster than Newton-Raphson method, it requires more iterations than Newton-Raphson to reach the final solution as its uses a superliner convergence instead of a quadratic convergence [85]. Furthermore, the Broyden algorithm does not self-correct whereas

the Newton-Raphson algorithm rounds-off the error with successive iterations [87]. This result in small deviations in the iterations compared to Newton-Raphson method. The algorithm calculates the required capacitor voltage of each CFC prior to any changes in demands. A CFC with a minimum capacitor voltage will be assigned to control the line current since a small capacitor voltage implies lower power losses due to smaller current ripple.

6.1.2 Local Controller

The LCs are composed of four control layers, namely, system control layer, application control layer, CFC control layer and firing control layer. The system control layer establishes a secure bi-directional data transmission link with the remote control centre. In addition, it monitors the status of each control layer and sends the status details back to the RCC. The application control layer accepts the voltage and current reference values set by RCC and pass the reference values to CFC control layer through a set of limiters. However, when the transmission link fails, the application control layer uses the local measurements and look-up tables to set the reference values.

The CFC control layer is implemented as an array of PI controllers and various control blocks which provides the duty cycle to the firing control layer by processing the references and local measurements. The firing control layer generates the firing pulses to the individual semiconductor valves.

6.2 Coordinated Control of multiple CFCs

6.2.1 Voltage Sharing Mode - CFC Overloading

The operational range of a CFC can be maximised by increasing the capacitor voltage level. However, such an approach could in turn increase the device footprint and cost. This issue can be overcome by sharing the required dc voltage between multiple CFCs.

Fig. 6.2 shows an upgraded dc network with a single CFC and with two CFCs. If a single CFC is used (Fig. 6.2(a)), dc voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$ are required in series with lines L_{ij} and L_{ik} to achieve the desired current on line L_{ij}. Let $\overline{V}_{B1} > V_{C,\max}$, where $V_{C,\max}$ is the maximum voltage allowed

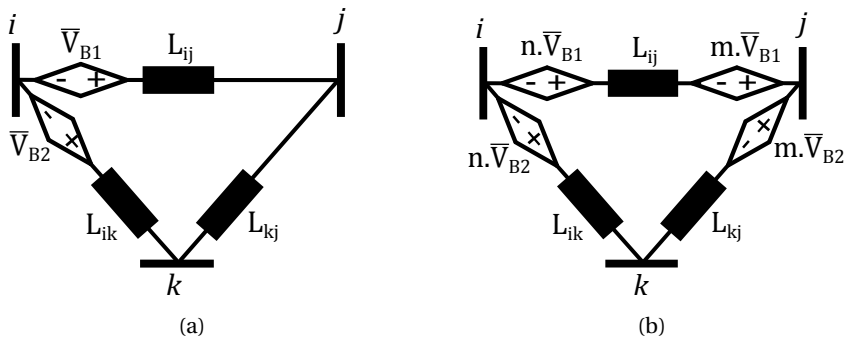


Figure 6.2: Voltage sharing: (a) Single CFC; (b) Multiple CFCs.

across the CFC capacitor. For this scenario, the required line current reduction or increment cannot be achieved. However, when two CFCs are included into the dc network (Fig. 6.2(b)), the required capacitor voltage can be shared between the CFCs in an $n:m$ ratio. The relationships between the required series dc voltages and the capacitor voltage are given by:

$$n(\overline{V}_{B1} + \overline{V}_{B2}) \leq V_{C,\max} \tag{6.1}$$

$$m(\overline{V}_{B1} + \overline{V}_{B2}) \leq V_{C,\max} \tag{6.2}$$

where $n \leq 1$ and $m \leq 1$, with $n + m = 1$.

When more than one CFC is deployed in a common dc line, the control objectives must be established carefully to avoid potential conflicts. Only a single CFC in CC mode is permitted at any given load condition; however, operation of multiple CFCs in VC mode is allowed.

6.2.2 Voltage Sharing Mode - Communication Failure

In HVdc systems, fibre optic and power line communication are widely employed for data acquisition and to dispatch control signals. As a result of technological advancements, these communication modalities have become faster and more reliable in recent years. However, a dc grid cannot just rely on wired-based communication links as they are vulnerable to natural disasters [91, 92, 93] and human errors [94].

An MTdc grid should remain operational in case of any communication failure. Although the RCC sets the references for each CFC (and their status), the LCs should be designed to detect

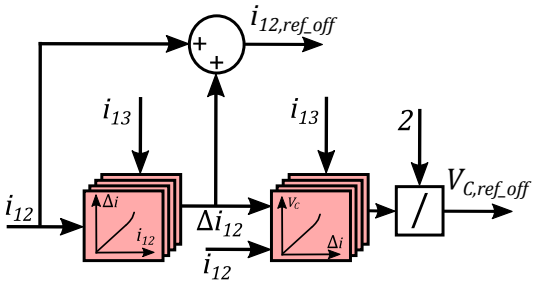


Figure 6.3: Offline voltage and current reference calculation.

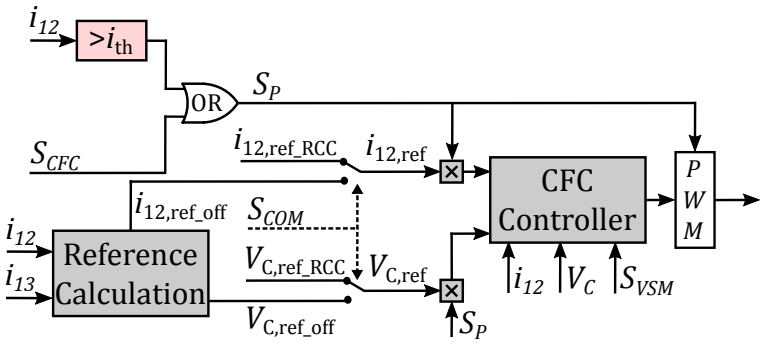


Figure 6.4: CFC triggering control.

overloading conditions and to trigger the CFCs accordingly when communication is lost. In this case, local measurements should be employed. As highlighted previously, preassigned control objectives (*i.e.*, modes of operation) must be established carefully among the active CFCs – with a single CFC acting in CC mode only. Current and voltage references are calculated offline using look-up tables, as shown in Fig. 6.3, where the dc line currents are used as inputs. For instance, if two CFCs are used, the CFC in a VC mode contributes half of the required capacitor voltage while the other half is approximately provided by CFC in CC mode. Fig. 6.4 shows a high level control diagram which is used to determine the references and status of the CFC. In the event of communication failure, signal S_{COM} becomes 0 and the references are determined locally by the off-line controller as shown in Fig. 6.3. The control mode of CFC is set by signal S_{VSM} where 0 and 1 represent CC and VC modes, respectively.

6.3 Pole Imbalance Control

Pole-current imbalances in an HVdc transmission system can be classified into two types: fast transient and slow drift [88]. Fast transients could be caused due to severe cable damage, which

requires a fast acting DCCB. On the other hand, slow drifts occur due to several reasons, such as the different degradation rates between positive and negative poles' cables, converter neutral current due to floating potential point, and asymmetrical tapping of small loads. If an imbalance is caused by an asymmetrical load tapping or cable degradation, a star-point reactor, as reported in [88, 89, 90], can be installed on the AC side to balance the positive and negative dc voltages by suppressing the neutral current. However, the low impedance characteristic of these reactors could introduce constraints on the voltage margins of the MMC by affecting the third-harmonic voltage injection [88]. In [31], a dc-dc converter has been used to provide pole balancing in presence of an unbalanced shunt load on negative pole. Alternatively, a CFC can be used to eliminate the pole-imbalance caused by slow drifts.

The imbalance i_m between dc poles can be calculated as follows:

$$i_m = (i_{12,+} - i_{12,-})100\% \tag{6.3}$$

where $i_{12,+}$ and $i_{12,-}$ are per-unit values of positive and negative pole line currents, respectively.

The current imbalance ratio Δ_i in the dc poles shall be calculated as:

$$\Delta_i = \frac{i_m}{2} \tag{6.4}$$

To achieve pole balancing, both positive and negative poles currents must be compensated $-\Delta_i$ and Δ_i, respectively.

6.3.1 Experimental Validation

The 3-terminal meshed MTdc grid shown in Fig. 6.5 is used to verify the proposed control methodologies. The CFC modules P and N are installed in series with both the positive and negative poles of lines L_{12} and L_{13}. A master-slave control strategy has been adopted to maintain the grid power balance. Fig. 6.6 shows the experimental setup of the MTdc test-rig with embedded CFC modules. A dSPACE DS1005 system is used to control the test-rig. The test-rig specifications are provided in Table 3.2 of chapter 3. A switching frequency of 2000 Hz is adopted to modulate the CFC.

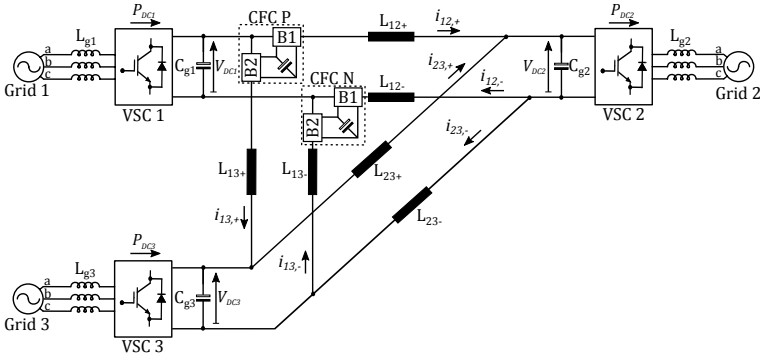


Figure 6.5: Three-terminal MTdc grid with embedded CFCs.

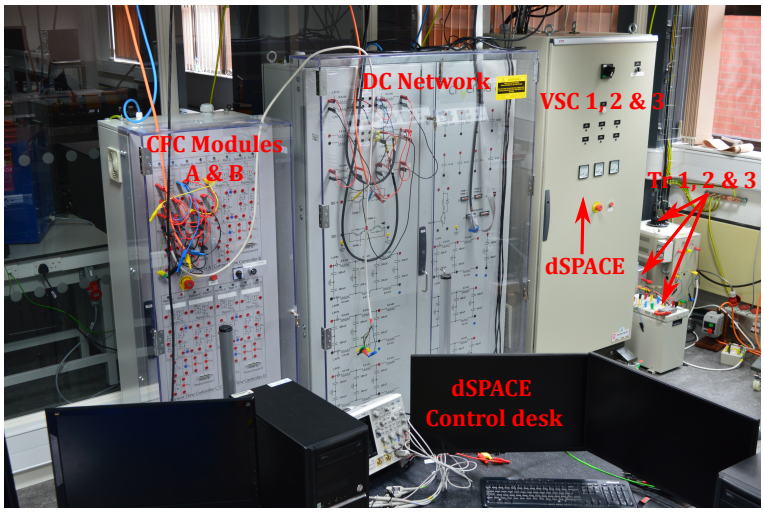


Figure 6.6: Experimental setup.

The proposed methodologies are validated only using 2B-CFCs. However, it must be highlighted that both 1B and C-CFCs can be adopted to provide pole balancing or voltage sharing services. The results in this section are expressed in per unit considering the following power, voltage and current bases: 2 kW, 125 V, and 8 A. VSCs 1 and 3 are initially set to inject 0.8 and 0.2 p.u. into the MTdc grid, whereas VSC 2 has been designated as a slack busbar that maintains the grid power balance (*i.e.*, maintains a constant dc voltage).

6.3.1.1 Current redistribution during line overloading

A test to assess the performance of 2B-CFCs following ramp changes in power is carried out both through a simulation and with the experiment platform. To this end, the 3-terminal dc grid

equipped with CFCs has been modeled in Simulink/SimPowerSystems. The CFCs are placed at the positive and negative poles of lines L_{12} and L_{13}. CFC operation is coordinated using an RCC and each CFC is equipped with an LC. The RCC determines the state of each CFC by calculating the required CFC capacitor voltage to maintain the line current at a desired value.

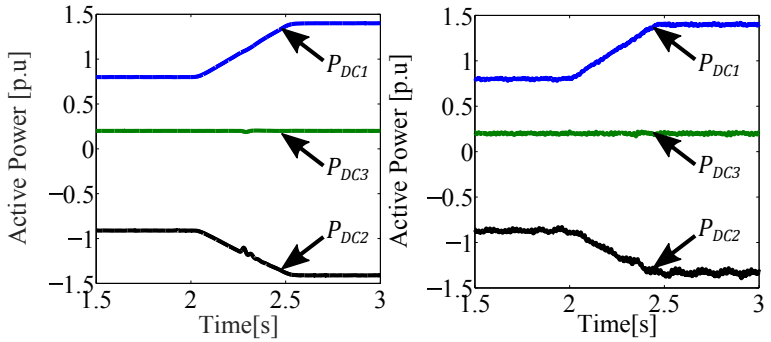
In general, the RCC would determine the optimal current references to achieve the best line current distribution in order minimise the grid power losses. However, it should be highlighted that in scaled systems (such as in the experimental test-rig in Fig. 3.25) the forward voltage drop on the semiconductor switches affects the current flow between electrical nodes. Thus, the required amount of capacitor voltage to achieve an optimum line current distribution should be very small (closer to the diode forward voltage drop). Therefore, to build enough voltage across the capacitor and to demonstrate the CFC performance, a large current reduction must be achieved. In this case the current reference is set to 0.5 p.u. which would be just below 1 p.u. mark in a real system.

Simulation (left) and experimental results (right) are shown in Figs. 6.7 to 6.9. Initially, both CFCs operate in a by-pass mode, with switches Q_1 and Q_2 being turned on. At $t = 2$ s, the power reference of VSC 1 is ramped up from 0.8 to 1.4 p.u. (see Fig. 6.7(a)). As it can be observed in Figs. 6.7(b) and 6.7(c), line currents i_{12+} and i_{12-} surpass the maximum thermal current limit (of 1 p.u.). Following the overload detection, the LCs are activated to decrease the currents to 0.5 p.u. to achieve a better line current distribution. As a result, the converters adjust their terminal voltages to maintain the grid power balance (Fig. 6.7(d)).

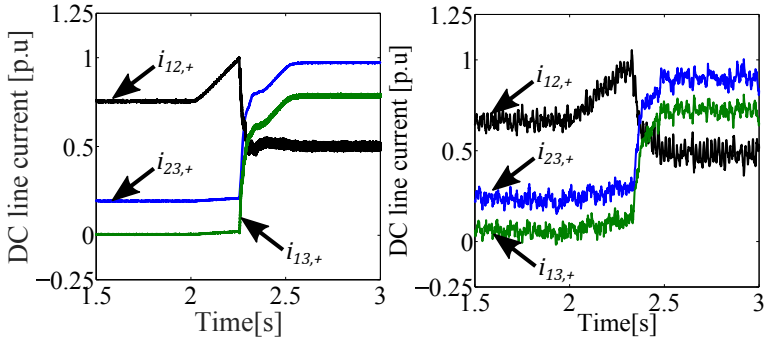
It should be noticed that a small mismatch occurs between the line current distribution of the simulation and experimental results. This is due to forward voltage drops in diodes and converter power losses in the experimental platform. Conversely, these voltage drops are fixed to 0.8 V in the simulation, with converter switching losses being neglected.

Figs. 6.8 and 6.9 provide the voltage profiles of the CFCs. For the experiment, the capacitor voltages are maintained at 0.035 p.u., as shown by Figs. 6.8(a)and 6.9(a). Such voltage value is determined by the RCC. However, the required capacitor voltage is 0.004 p.u. higher for the simulation as a result of the grid's initial current distribution and voltage profile (the RCC uses instantaneous grid measurements to determine the capacitor voltage). During the CC mode,

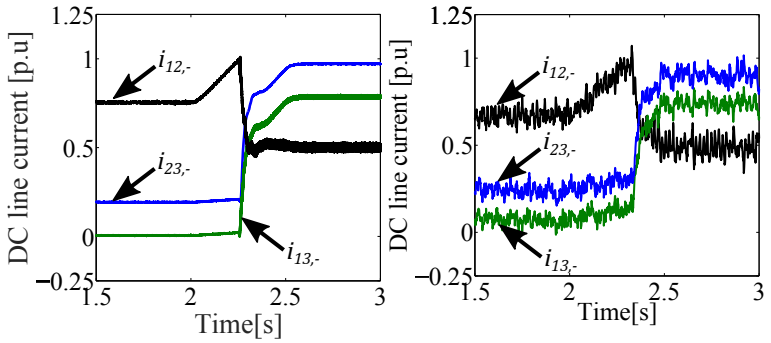
mean dc voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$ are inserted in series with lines L_{12+} and L_{13+}, respectively. This is shown in Fig. 6.8(b). Since the line current flows in an opposite direction, the signs of the inserted dc voltages in series with L_{12-} and L_{13-} (see Fig. 6.9(b)) are opposite with respect to those shown in Fig. 6.8(b).



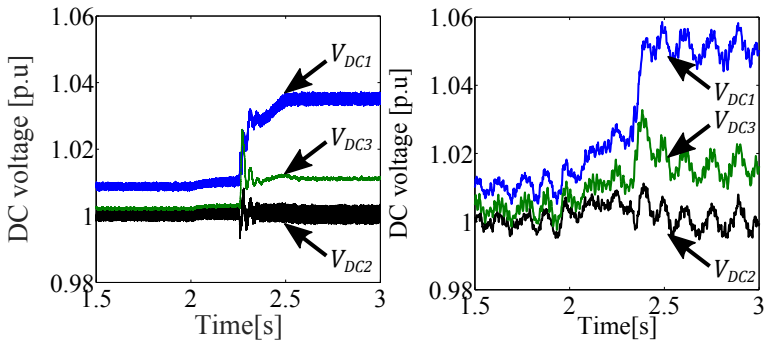
(a) VSC active power



(b) DC line current (positive pole)

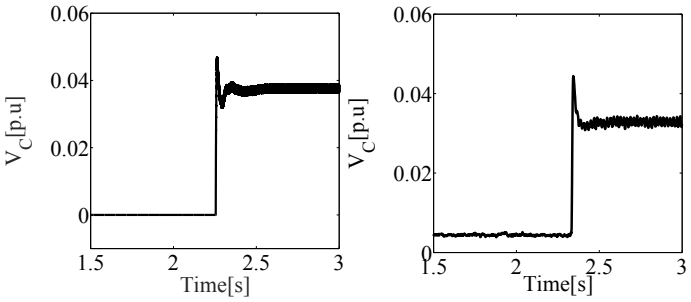


(c) DC line current (negative pole)

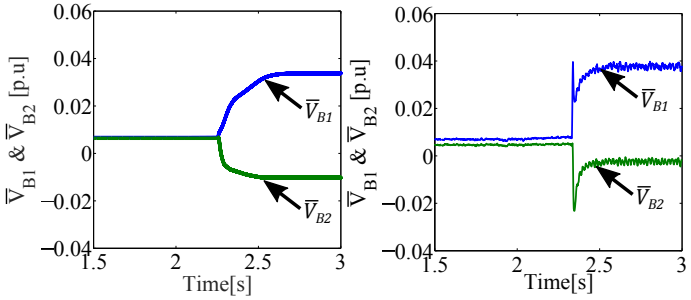


(d) DC terminal voltage

Figure 6.7: DC grid response for a ramp change in power: Simulation (left) and experimental (right) results.

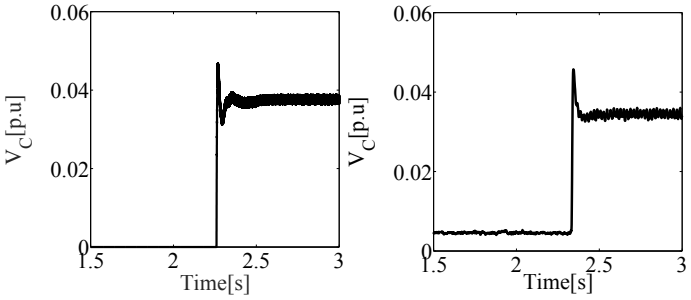


(a) Capacitor voltage

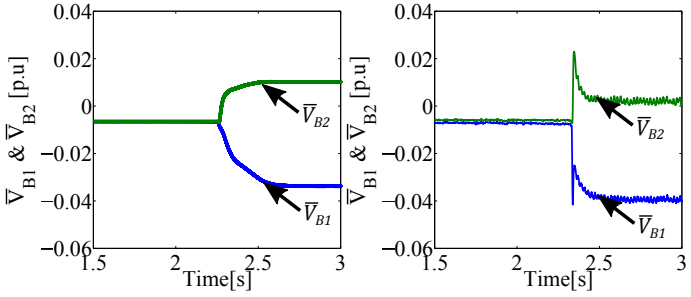


(b) Inserted mean dc voltages

Figure 6.8: Response of the CFC located at the positive pole for a ramp change in power: Simulation (left) and experimental (right) results.



(a) Capacitor voltage



(b) Inserted mean dc voltages

Figure 6.9: Response of the CFC located at the negative pole for a ramp change in power: Simulation (left) and experimental (right) results.

6.3.1.2 Pole balancing - bi-pole

In this test case CFCs are used to provide an auxiliary pole balancing support during an imbalance condition that occurs due to different cable degradation rate. Fig. 6.10 shows the test network configuration. The CFCs are placed at the positive and negative poles of lines L_{12} and L_{13}. The imbalance is induced by introducing a resistor R_{imb} = 0.6 Ω in series with line $L_{12,-}$. The dc grid responses under pole balancing support is shown in Fig. 6.12. Initially, both positive and negative pole CFCs are by-passed through switches Q_1 and Q_2 and an imbalance of 25% (i_m) is observed between the poles. In simulation, an imbalance of 30% (i_m) is observed between the poles as result of fixed diode voltage drops. Fig. 6.11 depicts the block diagram of current reference set-point calculator for bi-pole operation. The controller provide balancing support if the imbalance i_m exceeds the threshold value t_h. For this test case, threshold value of 5% is adopted. Although a proportional term is used to estimate the current reference during imbalance, the imbalance can be completely eliminated as poles currents are maintained at the same value through independent PI controllers.

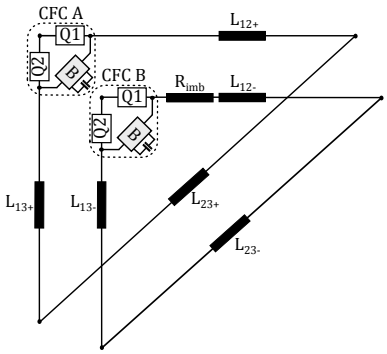


Figure 6.10: DC grid and CFC modules arrangement during pole imbalance.

At time t = 2 s, both poles CFCs are enabled and are requested to maintain line currents $i_{12,+}$ and $i_{12,-}$ at $i_{12,+,ref}$ and $i_{12,-,ref}$, respectively. In CC mode, the imbalances between currents $i_{12,+}$ and $i_{12,-}$ are reduced to ≈ 0 (0.01%). A small deviation is observed between the experimental

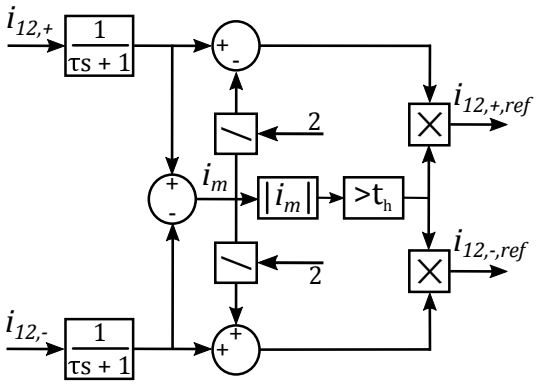


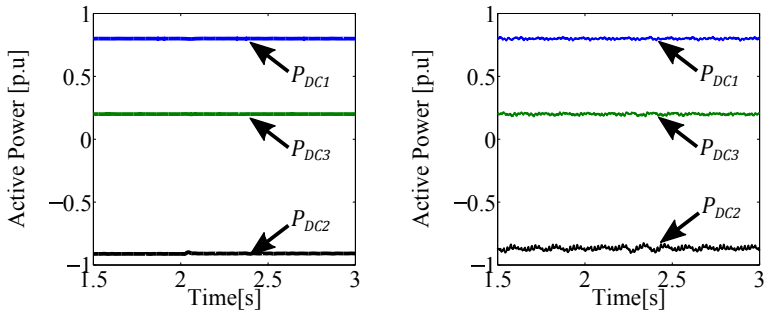
Figure 6.11: Pole imbalance controller

and simulation values which is within an acceptable margin.

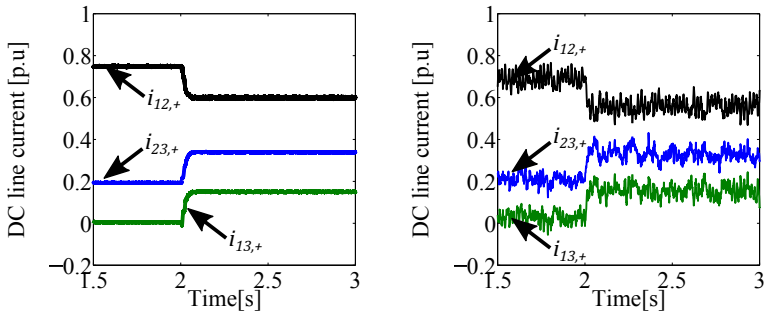
$$\begin{aligned} \text{Experiment}: i_{12,+,ref} &= i_{12,+} - \frac{\Delta_i}{100} = 0.7 - 0.125 = 0.575 p.u. \\ \text{Simulation}: i_{12,+,ref} &= i_{12,+} - \frac{\Delta_i}{100} = 0.75 - 0.15 = 0.6 p.u. \end{aligned} \tag{6.5}$$

$$\begin{aligned} \text{Experiment}: i_{12,-,ref} &= i_{12,-} + \frac{\Delta_i}{100} = 0.45 + 0.125 = 0.575 p.u. \\ \text{Simulation}: i_{12,-,ref} &= i_{12,-} + \frac{\Delta_i}{100} = 0.45 + 0.5 = 0.6 p.u. \end{aligned}$$

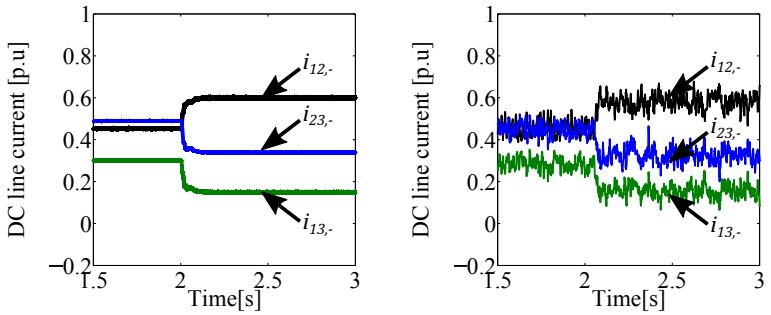
Fig. 6.13 and Fig. 6.14 shows the voltage profiles of positive and negative pole CFCs, respectively. As shown in Fig. 6.13(a) and Fig. 6.14(a), in experiment, the capacitor voltages of positive and negative pole CFCs are regulated at 0.006 p.u. whereas, in simulation, positive and negative pole CFCs capacitor voltages are regulated at 0.004 p.u. and 0.006 p.u., respectively. The observed mismatch between the simulation and experimental capacitor voltages are due to semiconductor on state voltage drop which results in different line current redistributions. Mean dc voltages as shown in Fig. 6.13(b) and Fig. 6.14(b) are inserted in series with the positive and negative pole lines, respectively. It must be emphasized that since the required line current reduction/increment is very small, voltage drops on CFC diodes are large enough to achieve the desired line current. Thus, inserted dc voltages of both CFCs are larger than their capacitor voltages.



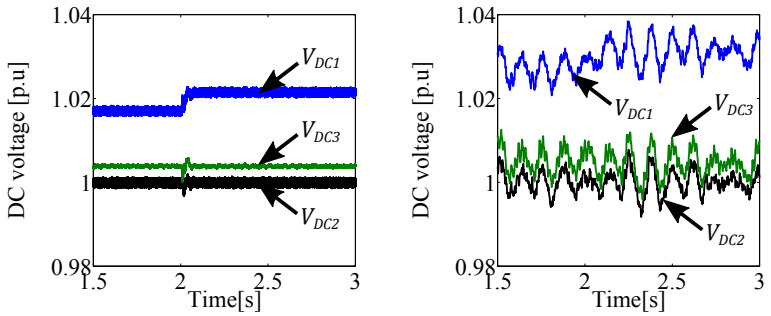
(a) VSC active power



(b) dc line current (positive pole)

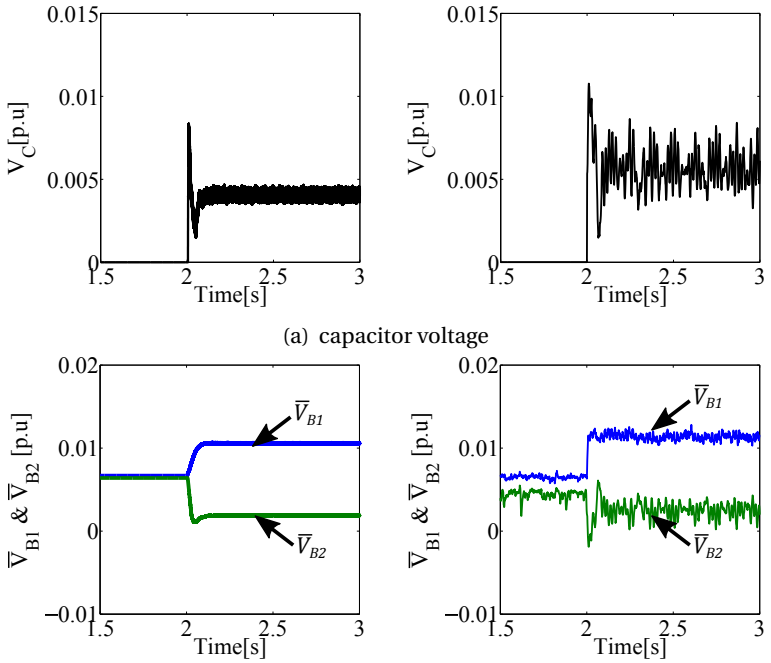


(c) dc line current (negative pole)



(d) dc terminal voltage

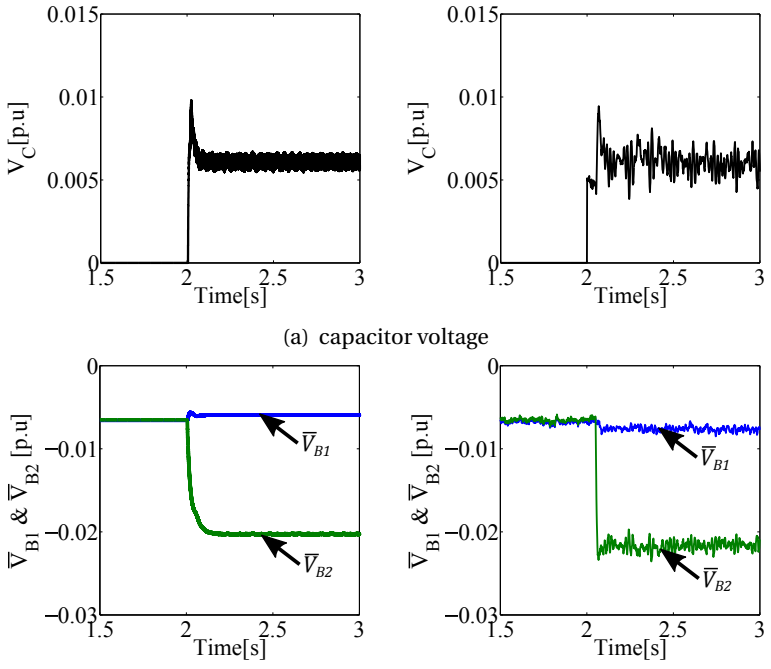
Figure 6.12: DC grid response during bi-pole balancing: Simulation (left) and experimental (right) results.



(a) capacitor voltage

(b) inserted mean dc voltages

Figure 6.13: Response of the CFC located at the positive pole during bi-pole balancing: Simulation (left) and experimental (right) results.



(a) capacitor voltage

(b) inserted mean dc voltages

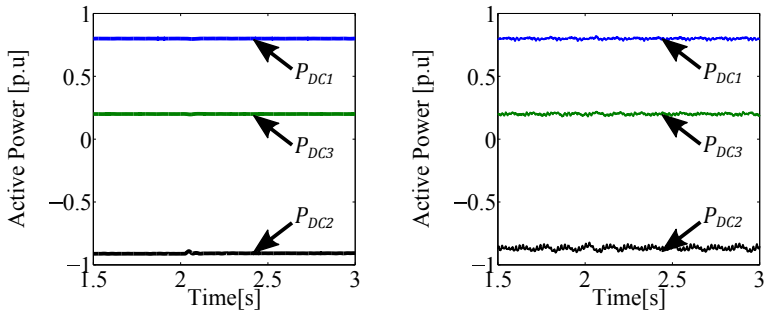
Figure 6.14: Response of the CFC located at the positive pole during bi-pole balancing: Simulation (left) and experimental (right) results.

6.3.1.3 Pole balancing under an asymmetrical tapping

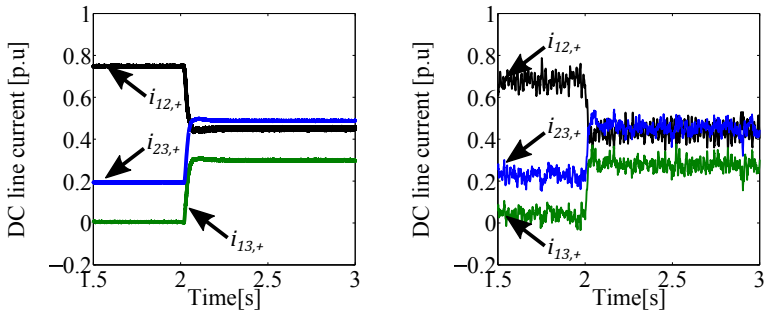
As discussed before, an asymmetrical tapping of a dc line could cause imbalance between the dc poles. In such condition, a dc voltage can be inserted in series with the tapped dc line to adjust the line current to be same as the other pole. In this test case, a CFC is used to eliminate the imbalances between poles under uni-pole operation. The experimental set-up as described in subsection 6.3.1.2 is adopted to validate the concept where CFC B is operated under bypass mode. Fig. 6.15 shows the dc grid response. Initially, both positive and negative pole CFCs are by-passed through switches Q_1 and Q_2 and an imbalance of 25% is observed between the pole. At time $t = 2$ s, the positive pole CFC is enabled and is requested to maintain the positive pole current $i_{12,+}$ at the same level as the negative pole current $i_{12,-}$. From Fig. 6.15(b) and Fig. 6.15(c), it can be seen that both poles currents are balanced and imbalance is eliminated. In experiment, the positive pole CFC capacitor voltage (Fig. 6.16(a)) is maintained at 0.011 p.u. whereas, in simulation, the required capacitor voltage is 0.001 p.u. higher than the experimental value. As shown in Fig. 6.16(b), during the CC mode, mean dc voltages $\overline{V}_{B1}$ and $\overline{V}_{B2}$ are inserted in series with lines L_{12+} and L_{13+}, respectively.

6.3.1.4 Coordinated control of CFCs under communication failure

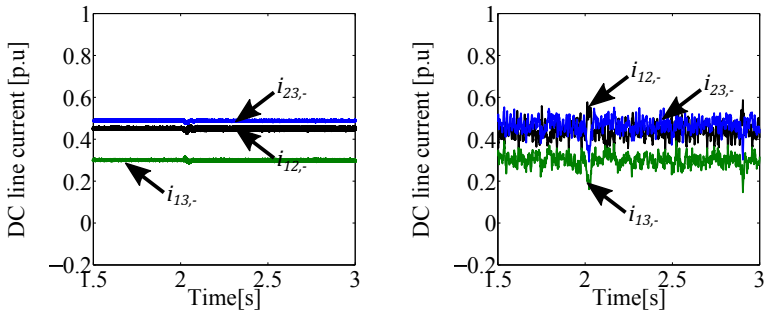
In this experiment, the coordination between two 2B-CFCs is examined when no communication between the LCs and the RCC exists. Fig. 6.17 depicts the system configuration for this test. CFC A is installed between the positive poles of lines L_{12} and L_{13}, whereas CFC B is installed between the positive poles of L_{13} and L_{23}. The voltage sharing method described in Section 6.2 is adopted to provide the required current control. CFC A is set to operate under a CC mode while CFC B operates under a VC mode. In CFC B, switches S_{11} and S_{22} are modulated during the VC mode as the current flows from T_{2B} to T_{1B} and T_{3B} and T_{1B}. As discussed in Chapter 4, the duty cycle of switch S_{22} is set to 1 and switch S_{11} is controlled to build up the capacitor voltage. Both CFCs are initially operated in a by-pass mode. At $t = 2$ s, the power reference of VSC 1 is ramped up from 0.8 to 1.4 p.u. Since there is no communication between the CFCs and the RCC, the LCs determine the reference set-points and dictate the CFC control following the detection of an overload condition. The LCs determine the voltage and current reference set-points using look-up tables as shown in Fig. 6.3, where instantaneous dc line currents measurements are



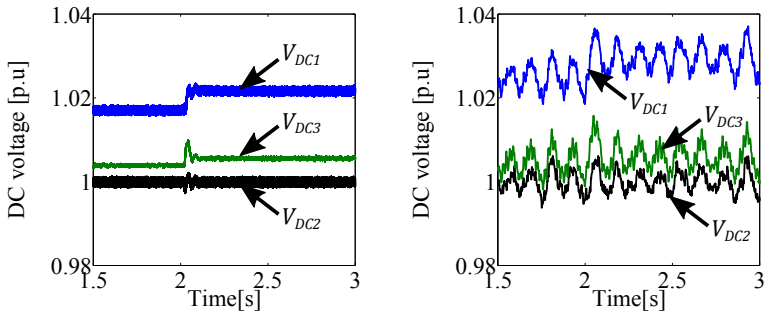
(a) VSC active power



(b) dc line current (positive pole)

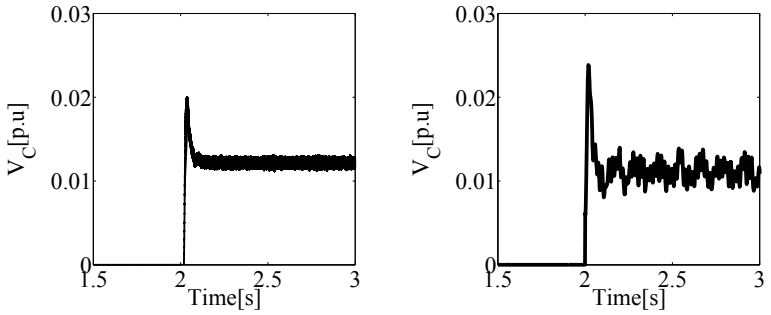


(c) dc line current (negative pole)

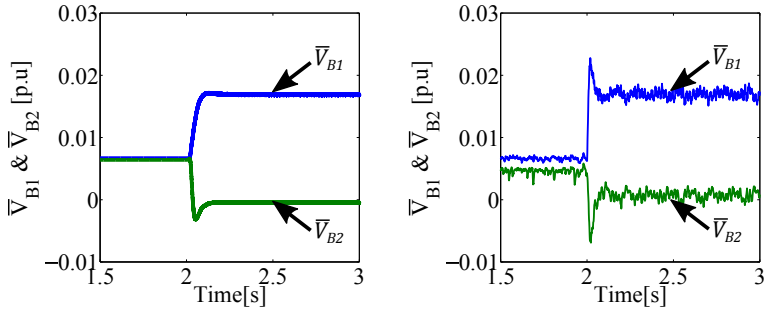


(d) dc terminal voltage

Figure 6.15: DC grid response during uni-pole balancing: Simulation (left) and experimental (right) results.



(a) capacitor voltage



(b) inserted mean dc voltages

Figure 6.16: Response of the CFC located at the positive pole during uni-pole balancing: Simulation (left) and experimental (right) results.

used as inputs.

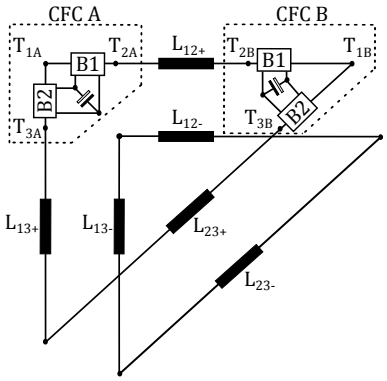
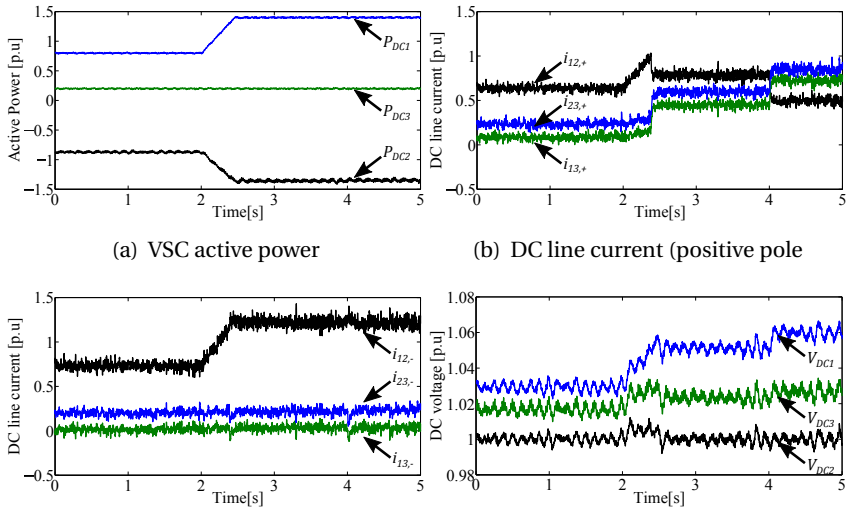


Figure 6.17: DC grid with two CFCs.

Fig. 6.18 shows the dc grid response. Following the change in set-point power (see Fig. 6.18(a)), L_{12+} and L_{12-} become overloaded. This is illustrated in Figs. 6.18(b) and 6.18(c). Once this condition is detected, CFC B is enabled to provide half of the required voltage injection (0.016 p.u.). CFC A is enabled at $t = 4$ s to decrease i_{12+} to 0.5 p.u. so that a better current distribution is achieved. It should be emphasized that since no CFC is placed on the negative pole, L_{12-}

remains overloaded. The voltage profiles of the CFCs are shown in Figs. 6.19 and 6.20. It should be recalled that two diodes are inserted in series with the capacitor during a charging mode (see Fig. 4.4(b)). In this case, a voltage drop of 0.0065 p.u. (0.8 V) is observed across each diode. As a result, the inserted mean bridge voltages $\overline{V}_{B1}$ of CFCs A (Fig. 6.19(b)) and B (Fig. 6.20(b)) are higher than their capacitor voltages. Based on eq. 6.1 and eq.6.2, the total amount of required capacitor voltage for current control is shared between CFCs in a ratio of n:m. In this test case, the voltage across each capacitor is nearly the same as the CFCs share the required voltage in a 1:1 (n:m) ratio (see Figs. 6.19(a) and 6.20(a)). The voltage sharing between CFCs is mainly determined by their control mode and location. Since its a simple three terminal network, the required dc voltage is equally (approximately) shared between the CFCs.

It must be highlighted that in this test case, CFCs are only installed at the positive pole as the main objective is to validate the operation of CFCs under VSM. However, in a real system, CFCs will be installed at both negative and positive poles. The experimental results presented in this section demonstrate the need to install a CFC in the positive and negative poles.



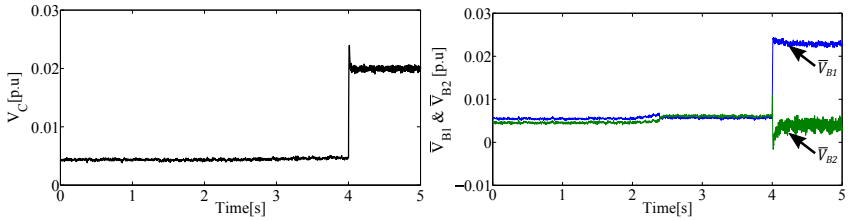
(a) VSC active power

(b) DC line current (positive pole

(c) DC line current (negative pole)

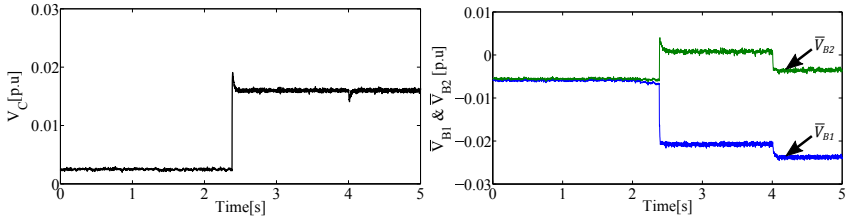
(d) DC terminal voltage

Figure 6.18: DC grid response.



(a) Capacitor voltage (b) Inserted mean dc voltages

Figure 6.19: CFC A response.



(a) Capacitor voltage (b) Inserted mean dc voltages

Figure 6.20: CFC B response.

6.4 CFC Protection and Failure Considerations

One of the most important aspects in the design and development of a CFC is its protection system. In essence, the protection of a CFC could be jeopardised by either module/control (system) failure or dc fault. In both cases, the CFC could experience overcurrent and overvoltage, which could lead to permanent failure. Since the CFCs are series connected devices, a failure could interrupt the dc lines current flows, leading to instability. Therefore, additional control measures must be implemented to avoid any interruption in grid operation during any failure or fault. Following this line, an assessment of the proposed CFCs under dc fault and system failure is fundamental.

6.4.1 CFC failures

The operation of a CFC could be affected by internal failures such as semiconductor module failure, failure of gate drivers and mechanical failures. According to a survey conducted on 200 products of 80 companies, failure of a power electronic module due to semiconductor and soldering failures has been contributed to 34% of system failures [95]. Therefore, in an event of aforementioned failures, the CFC must be bypassed to avoid any interruption to grid operation.

The CFC is immediately set to enter the self-protection mode when one or more of the following conditions are satisfied:

- Errors (S_{error}) due to component failures
- If line current, i_{dc}, magnitude is above 1.3 p.u
- If the voltage, V_C, across the CFC capacitor is 30% above the rated value
- If the local DCCBs in series with CFC are opened (S_{DCCB})

By incorporating the above conditions as inputs, a self protection logic controller as shown in Fig. 6.21 is proposed to bypass the CFC.

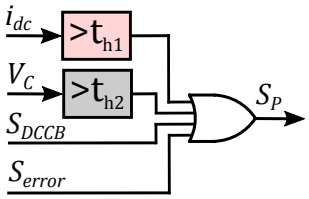


Figure 6.21: CFC self protection logic controller.

A simulation based study is carried out to demonstrate the impact of CFC failure on system performance. Fig. 6.22 shows the test network where CFC is installed between lines L_{12} and L_{13}. The internal fault is assumed to be failure of the controlled IGBT switches gate drivers. Fig. 6.23 shows the simulation results of voltage and current profiles of a 2B-CFC during the drive failure. The internal fault detection and discrimination time of 1 ms is adopted. Initially, CFC is operated under CC mode and capacitor voltage, V_C, and line current, i_{13}, are regulated at 0.04 p.u. and 0.5 p.u., respectively. At $t_0 = 2$ s, an internal fault is applied by blocking the control signals to IGBTs. Following the internal failure, as shown in Fig. 6.23(a), voltage across the capacitor increases as line currents i_{12} and i_{13} flow through bridges B_1 and B_2 charge it (Fig. 6.24(a)). Thus, line currents i_{12} and i_{13} start falling towards zero as voltages across bridges B_1 (V_{B1}) and B_2 (V_{B2}) start to increase. Since VSC 1 is in power control mode (injection), it increases the terminal voltage to maintain the power balance. Therefore, to maintain the system stability and to avoid any overvoltage, CFC must be by-passed. This is achieved by redirecting the line currents through by-pass switches Q_1 and Q_2 (Fig. 6.24(b)) by turning them on at $t_1 = 2.001$ s.

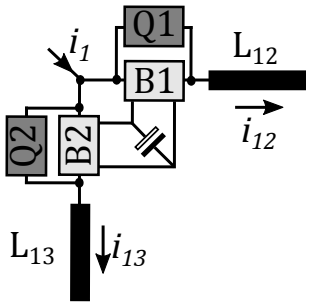
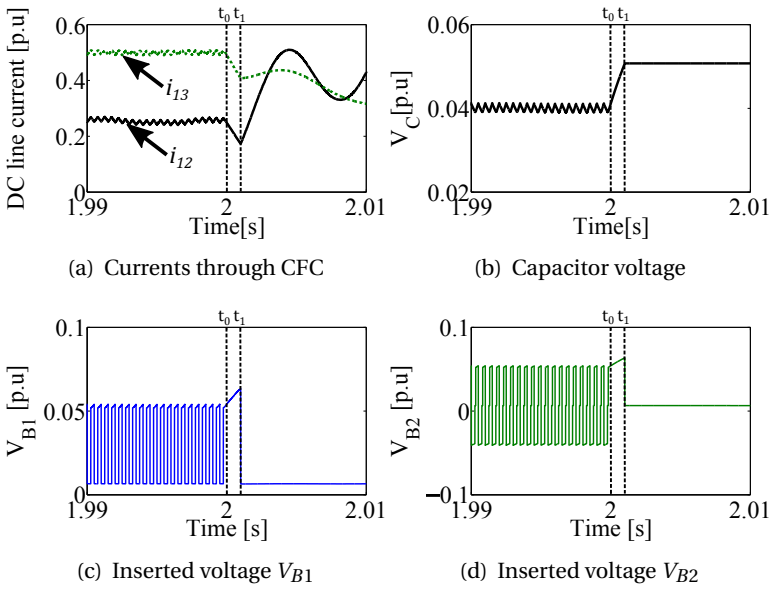


Figure 6.22: 2B-CFC internal failure test network.



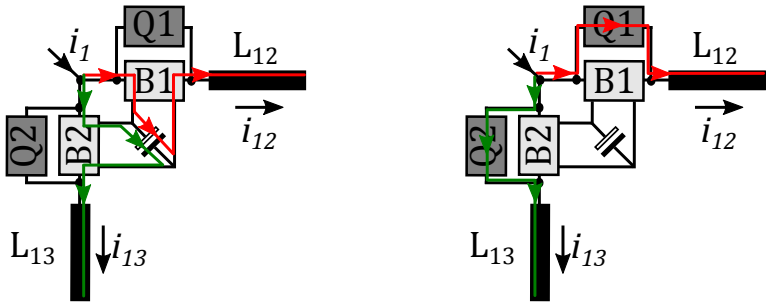
(a) Currents through CFC

(b) Capacitor voltage

(c) Inserted voltage V_{B1}

(d) Inserted voltage V_{B2}

Figure 6.23: CFC response during internal failure: Simulation results.



(a) CFC in blocking mode

(b) CFC in by-pass mode

Figure 6.24: 2B CFC operational states during an internal control failure.

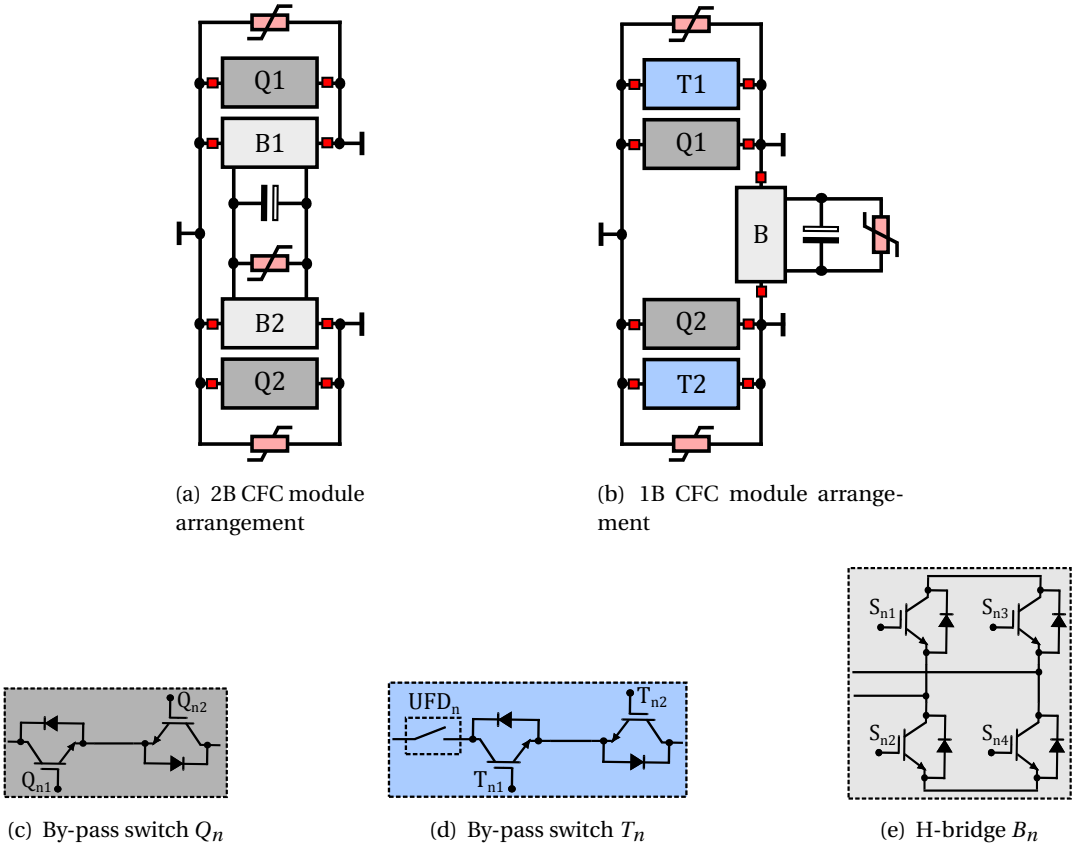
The results have shown that by-pass switches are vital part of a CFC to maintain the system stability and to protect the device against any potential overvoltage and overcurrent conditions.

Fig. 6.25 shows the by-pass and control modules arrangements of 2B and 1B-CFCs with embedded surge arresters. The surge arresters are connected across the by-pass switches and capacitor to limit the voltage across them during the fault. The possible switch arrangements of by-pass switches are shown in Fig. 6.25(c) to Fig. 6.25(e). The first switch arrangement (Q_n) is composed of two anti-series connected IGBTs. The second by-pass switch arrangement (T_n) comprises an ultra-fast disconnector (UFD) in series with anti-series connected IGBTs. The addition of an UFD reduces the number of required series IGBTs by taking most part of the open circuit voltage across itself. In Chapter 4, by-pass switch Q_n is exclusively used to by-pass the 2B-CFC. In Chapter 5, these switches are utilized to provide current control. Thus, the expected life cycle of these switches are far lesser than by-pass switches of 2B-CFC. In Fig. 6.25(b), failure of by-pass switches, Q_1 and Q_2, could lead to unstable system and trigger the dc grid protection. Therefore, additional by-pass switches (T_n) must be added in parallel to by-pass switches Q_1 and Q_2. Following this line, switches Q_1 and Q_2 in Fig. 6.25(a), can be replaced with switch T_n as they exhibit higher on state losses compared to Q_n. On the contrary, switch T_n has a slower response time than switch Q_n, which could increase the rating of the surge arrestors. The red squares on Fig. 6.25(b) and Fig. 6.25(a) represent the mechanical isolator switches. These provide electrical isolation during maintenance.

6.4.2 DC Fault

A major challenge in the development of an MTdc system is grid protection. Due to the low dc side impedance, a dc fault will generate large fault currents. Thus, care should be exercised since a poor protection system may lead to permanent damages. Following this line, an assessment of the proposed CFCs under dc and system faults is fundamental.

Since CFCs are series connected devices, their protection is mainly determined by the fault current magnitude and the response time of by-pass switches. In line with this, an experiment is carried out to evaluate the performance of 1B and 2B CFCs under a pole-to-pole fault. The pole-to-pole dc fault is applied through the fault generator as shown in Fig. 6.27. The generator consists of a series connected RL section and an IGBT. As shown in Fig. 6.26, the fault is applied between the positive and negative poles of line L_{12} by connecting the generator terminals $T_{f,+}$ and $T_{f,-}$ between the positive and negative poles, respectively. When switch S_f is turned on, as



(a) 2B CFC module arrangement

(b) 1B CFC module arrangement

(c) By-pass switch Q_n

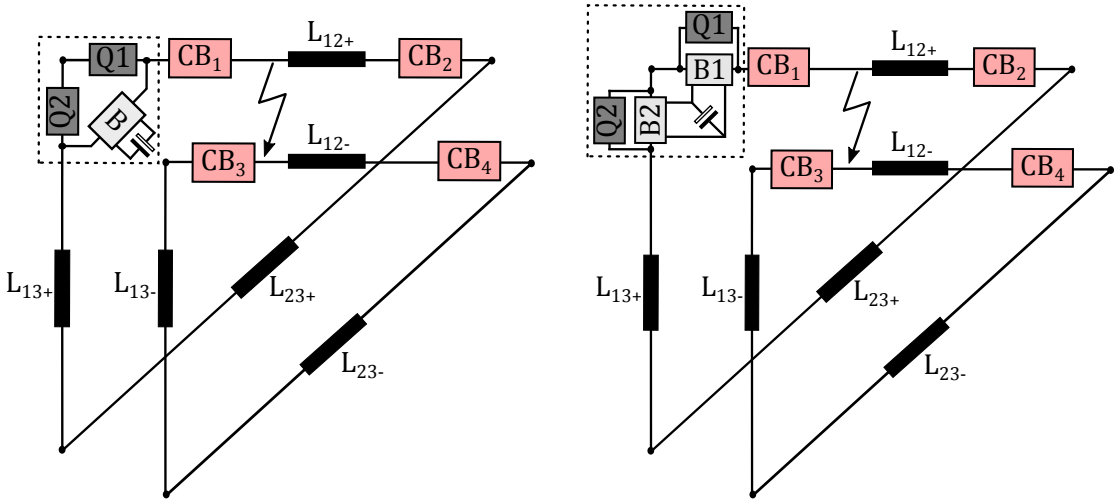
(d) By-pass switch T_n

(e) H-bridge B_n

Figure 6.25: Protection of 2B and 1B CFC

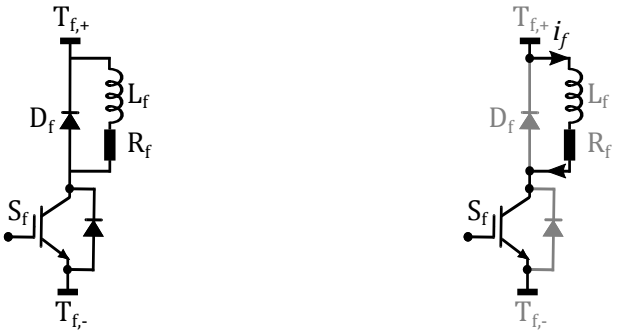
shown in Fig. 6.27(b), a dc fault is applied between the poles and fault current i_f flows through the generator. The fault current magnitude is limited via resistor R_f whereas the rate of change is limited by inductor L_f. A freewheeling diode D_f is added in parallel with the RL circuit to limit the voltage surges during current interruption. Small-scale solid-state based DCCBs (as shown in Fig. 6.28) are installed at each end to interrupt the fault current. The DCCBs are rated for 300 V and have the ability break fault currents up-to 20 A (2.5 p.u). The short circuit generator parameters are provided in Appendix B.

A communication-less single-ended protection strategy is used to detect the fault. The DCCBs and by-pass switches are set to open and close, respectively, if the rate of change in line current is > 800 p.u./s and the current magnitude is above 1.3 p.u. In addition, if the voltage across the CFC capacitor is 30% above the rated value, the CFC will be switched to a by-pass mode to protect it against overvoltage. MOVs are connected across the by-pass switches and the CFC



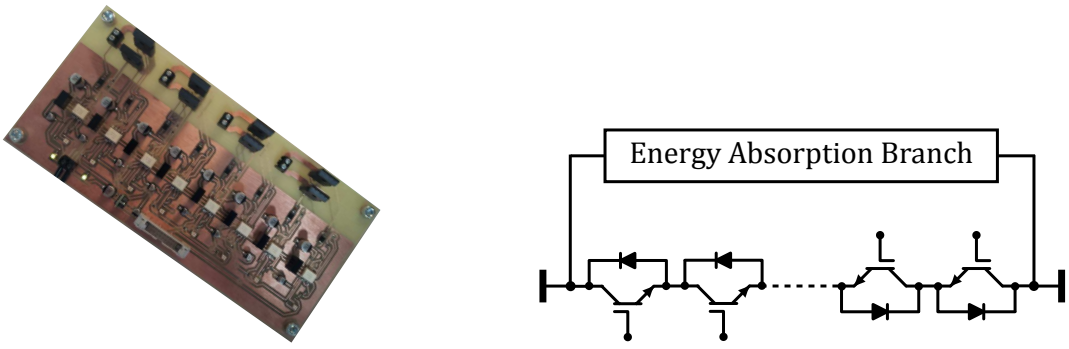
(a) 1B-CFC under dc fault (b) 2B-CFC under dc fault

Figure 6.26: Pole-to-pole fault location.



(a) Topology (b) Active

Figure 6.27: DC fault generator.



(a) (b)

Figure 6.28: Solid State DCCB; (a) small scale prototype, (b) DCCB topology

Table 6.1: System state during dc fault

Time	System state
t_0	Pole-to-pole fault applied
t_1	Fault detected by CFC, bypass switches activated and control signals disabled
t_2	Opening of DCCBs

capacitor to protect the device against overvoltages. The system states during the fault are provided in Table 6.1.

6.4.2.1 1B-CFC under pole-to-pole fault

This test evaluates the performance of a 1B-CFC under a pole-pole fault. Fig. 6.26(a) shows the location of the CFC where modules Q_1 and Q_2 are placed in series with dc lines $L_{12,+}$ and $L_{13,+}$, respectively. Initially, the CFC is in CC mode and line current i_{13} is regulated at 0.5 p.u. A single modulation controller as discussed in chapter 5 is adopted to regulate the line current. A pole-to pole fault is triggered at t_0. The fault currents through the CFC are shown in Fig. 6.29. Following the dc fault, line current $i_{12,+}$ has started to increase while i_{13} has decreased. Hence, CFC capacitor voltage and bridge voltages increase (Fig. 6.31(a)) as it tries to maintain the line current constant by increasing the required capacitor voltage. Following the fault detection at $t = t_1$, the control signals are disabled and the CFC is switched to by-pass mode; this way, the fault current is completely redirected to switches Q_1 and Q_2. The capacitor voltage remains constant as the H-bridge is bypassed. The DCCBs voltage profiles are shown in Fig. 6.31(b). The fault current is interrupted at $t = t_2$ by opening the DCCBs. As it can be observed, the voltage across each DCCB is equal to the pole voltage.

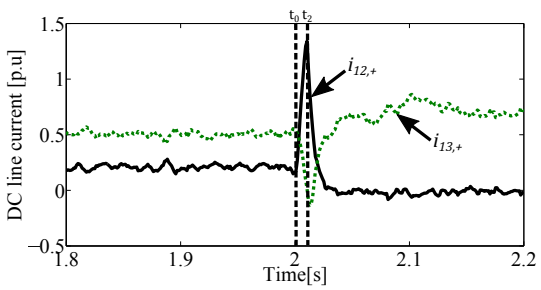


Figure 6.29: Fault current through CFC

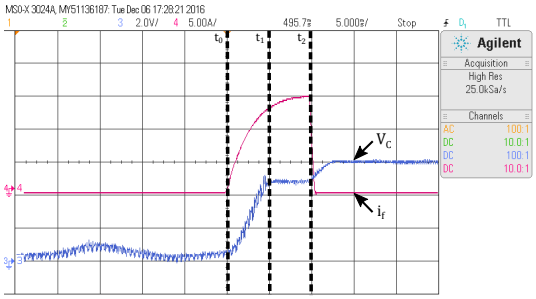
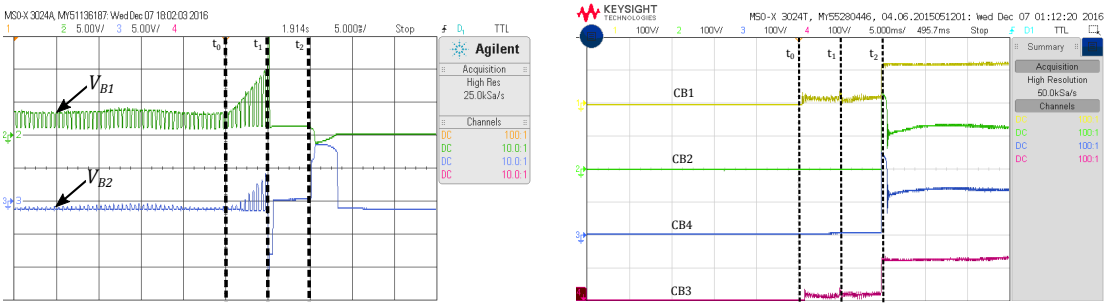


Figure 6.30: 1B-CFC capacitor voltage and fault generator current



(a) 1B-CFC voltage profile

(b) DCCBs voltage profile

Figure 6.31: Fault response with embedded 1B-CFC

6.4.2.2 2B-CFC under pole-to-pole fault

Fig. 6.32 shows the fault current through the CFC. During pre-fault conditions, the CFC is set to control line current i_{13} at 0.5 p.u. and capacitor voltage V_C at 0.04 p.u. (5 V). After the fault is applied at $t = t_0$, the magnitude of line current i_{12} rapidly increases and i_{13} decreases, while the CFC capacitor voltage and bridge voltages increase (Fig. 6.33(a)). This occurs as the CFC tries to maintain the line current at the reference value since the fault has not been detected yet. At $t = t_1$, the fault is detected by the local protection system and the CFC transitions from a CC to by-pass mode. The capacitor voltage remains constant as the H-bridges are bypassed. Fig. 6.33(b) shows the voltage profiles of the DCCBs. The fault current is interrupted at $t = t_2$ by opening the DCCBs.

A comparison between ac powered CFCs (IGBT and thyristor CFCs) and 2B-CFC in terms of dc fault performances and power losses are provided in Appendix 6.5.

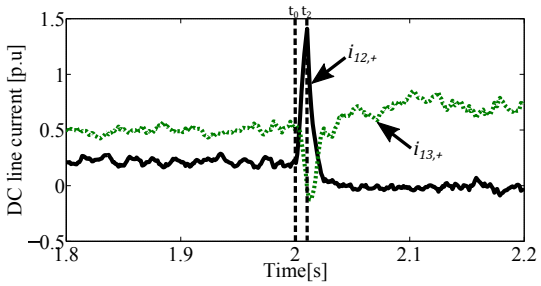
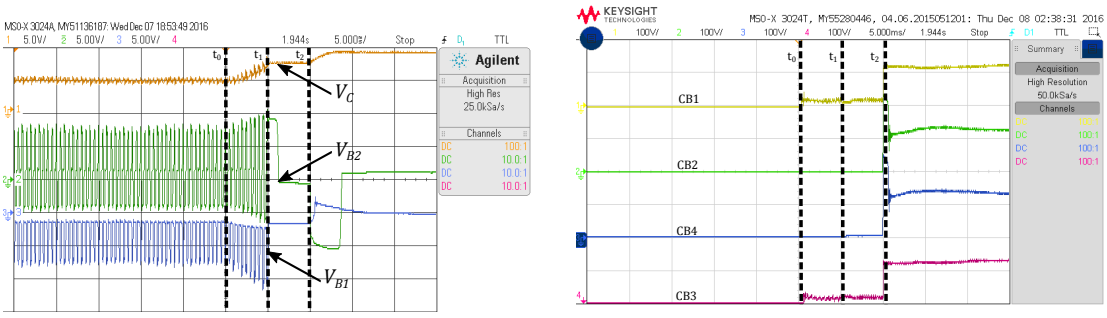


Figure 6.32: Fault current through CFC



(a) 2B-CFC voltage profile

(b) DCCBs voltage profile

Figure 6.33: Fault response with embedded 2B-CFC

6.5 Fault Study on Full Scale Model

In this section, performances of thyristors, IGBT and 2B-CFCs are compared in terms of power losses and dc fault on a four-terminal meshed MTdc grid (discussed in Chapter 2). The MTdc grid and the CFCs have been modeled in Simulink/ SimPowerSystems.

6.5.1 CFCs Dc fault Performances

CFC protection during dc faults is mainly determined by the fault current magnitude and the response time of bypass switches. To analyze the impact of a dc fault on the CFCs, a pole-to-pole fault is applied at $t_0 = 1.5$ s. The fault locations are shown in Fig. 6.34. The fault has been applied on the line where the CFCs are installed to maximize its effect. A communication-less single-ended protection strategy, as described in Section 6.4.2, is used to trigger the DCCBs. System states during the fault are provided in Table 6.2.

Fig. 6.35 shows the response of the thyristor-based CFC. A surge arrester is installed for overvolt-

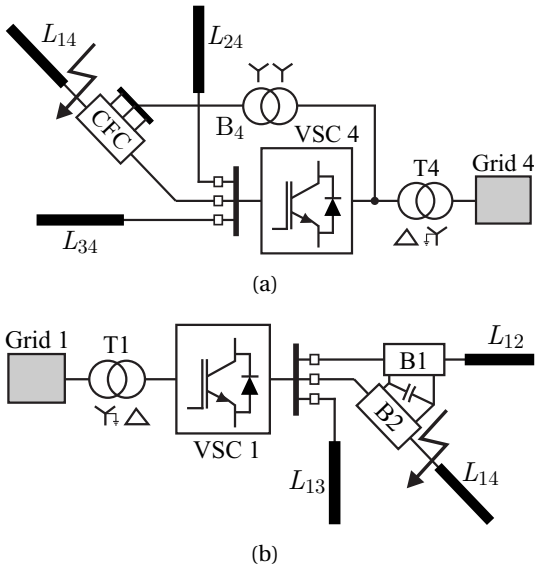


Figure 6.34: DC fault location

Table 6.2: System state during dc fault

Time	System state
t_0	Pole-to-pole fault applied
t_1	Fault detected by CFC, bypass switches activated and control signals disabled
t_2	Opening of DCCBs

age protection (see Fig. 2.6). At $t = t_1$, the fault current is transferred from the surge arrester to the bypass switch B_{SW}, with the current through the CFC, I_{DC}, becoming zero. The DCCBs are activated at $t = t_2$ ms to isolate the faulty line. The thyristor modules can hold a very large surge current for several milliseconds; however, they should be immediately bypassed to avoid any contribution from the ac side.

Fig. 6.36 illustrates the voltage and current profiles of the H-bridge CFC. Similar test conditions as for the thyristor-based CFC have been applied. The capacitor is rapidly charged by the fault current between t_0 and t_1, with its voltage being limited by a surge arrester. At $t = t_1$, the fault is detected by the CFC, the control signals are disabled and the IGBTs are blocked; this way, the fault current is redirected to bypass switch B_{SW}. The faulty line DCCBs are opened at $t = t_2$ to isolate the line. The magnitude of the capacitor voltage V_C remains high as no discharging paths are available. As mentioned before, the voltage level can be brought down a safer level by using

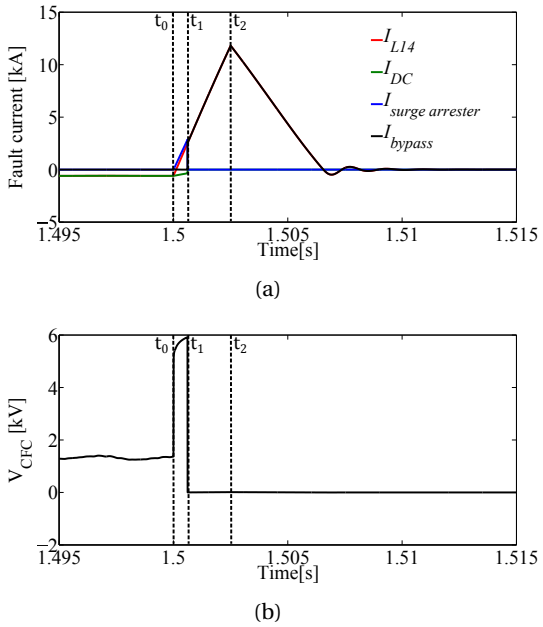


Figure 6.35: Fault response of thyristor-based CFC. (a) Fault current distribution. (b) Terminal voltage.

a controllable discharge circuit.

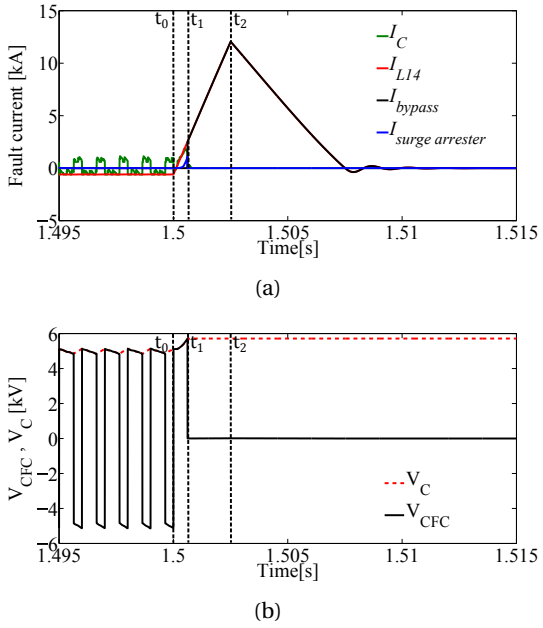
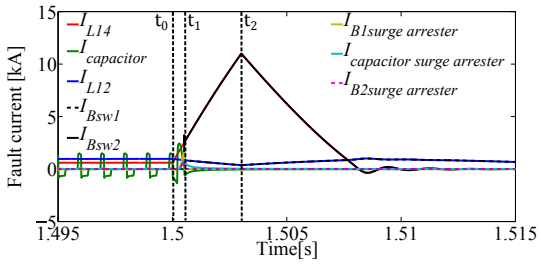


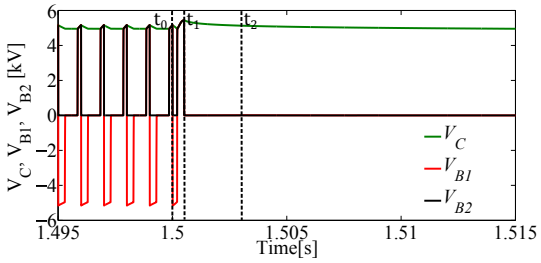
Figure 6.36: Fault response of H-bridge based CFC. (a) Fault current distribution. (b) Capacitor and H-bridge voltage.

The performance of the 2B-CFC is shown in Fig. 6.37. After the fault is applied at $t = t_0$, the

magnitudes of line currents I_{L12} and I_{L12} rapidly increase, with I_{L12} changing polarity. This occurs as the CFC tries to maintain the line current at the reference value as it has not detected the fault yet. In turn, this causes the capacitor and bridge voltages to build up to a maximum level (limited by commutating part of the fault current into the surge arresters). At $t = t_1$, the CFC detects the fault, the control signals are disabled, the IGBTs are blocked and the bypass switches B_{SW1} and B_{SW2} are activated. The lines are isolated at $t = t_2$ by opening the DCCBs. As with the H-bridge CFC, the capacitor voltage V_C remains high and should be drained to a safer level. As it can be observed, the dual H-bridge has shown a similar level of vulnerability as the other CFCs.



(a)

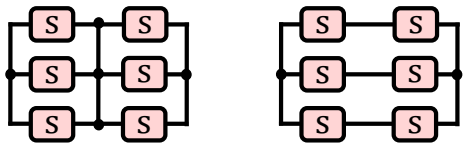


(b)

Figure 6.37: Fault response of 2B-CFC. (a) Fault current distribution. (b) Capacitor voltage and H-bridge voltage.

In terms of fault management, the proposed CFCs may be affected by dc faults; thus fast DCCBs and communication are required to ensure a good protection. However, thyristors can hold a large surge current when compared to IGBT devices –this makes the thyristor-based CFC less vulnerable to a dc fault. From the results presented in this section, it is clear that the bypass switch needs to hold a large current until the fault is cleared. Thus, arrays of IGBTs must be added in parallel to withstand the fault current. Fig. 6.38 shows the possible topologies of these bypass switches. The required number of IGBTs in each bypass module is mainly determined by

the response time of the DCCB. For example, the number of required IGBTs in bypass switches could be higher for a system with mechanical DCCBs compared to a system with hybrid DCCBs. IGCT-based bypass switches may provide a better solution in terms of high fault current handling capabilities and lower on-state losses compared to IGBT-based switches [96]. On the other hand, ac faults could affect the operation of thyristor-based and H-bridge CFCs.



(a) (b)

Figure 6.38: Topologies for the CFC bypass switch: (a) arrangement 1; (b) arrangement 2.

Although the simulations carried out in this section provide an initial indication of the fault responses for the different types of CFCs, further work is necessary for detailed fault studies where frequency dependent models are employed to represent dc lines.

6.5.2 Power losses and dc harmonics

To evaluate the switching losses of the proposed CFCs, IGBT model 5SNA 2000K451300 [97] and thyristor model 5STP 21H4200 [98] have been adopted. A single IGBT of a CFC represents two series connected IGBTs. Each IGBT is rated for 4500 V with a collector current rating of 2000 A. A similar strategy is adopted for the thyristor-based CFC, where two 4200 V rated thyristors with an on-state current of 3443 A are used to build each arm of both positive and negative converters. The number of IGBTs or thyristors in each arm may be increased to achieve a higher reliability level.

Table 6.3 shows the maximum power losses of each CFC. It should be emphasized that the calculated values include conduction and switching losses. Power losses on ac transformers for the H-bridge and thyristor-based CFCs have not been considered. Among all devices, the H-bridge CFC exhibits the highest losses (171 kW). This is understandable as it features the greatest number of switching elements (the IGBTs of the two-level converter switch at 1650 Hz and those of the H-bridge switch at 1000 Hz). The 2B-CFC under dual modulation has power losses of 45 kW. On the other hand, the thyristor-based CFC has considerably lower power losses,

19 kW, although if losses on the smoothing reactors are considered the total increases to 122 kW. It should be noted that the total losses could be decreased by using different types of IGBT and thyristors which are optimized to have lower turn-on and turn-off energy and reverse recovery charge.

Table 6.3: Total power losses of the CFCs

Device	Total power losses [kW]
Thyristor	122
H-bridge	171
Dual H-bridge	45

6.6 Conclusions

In this chapter a centralised hierarchical control scheme has been presented to coordinate the operation between multiple CFCs in the MTdc grid. It has been shown that when multiple CFCs are employed, the workload of a CFC that has reached its maximum operating point can be reduced by sharing the dc voltage insertion among the other CFCs. Potential control conflicts between active CFCs can be eliminated by restricting the operation of a single CFC in CC mode and the remaining CFCs in VC mode.

The protection of CFCs is determined by the response time of the DCCBs and bypass switches. The performance of 1B and 2B-CFCs has been studied under the presence of a pole-to-pole dc fault. It has been observed that a fast protection system is required to protect the CFCs against overvoltages and overcurrents.

In addition, the performances of thyristor, H-bridge and 2B based CFCs have been assessed under a dc fault on a full scale model. The CFCs have showed a similar level of vulnerability under the dc fault. Furthermore, a preliminary analysis shows that the 2B-CFC features the lowest power losses compared to thyristor and H-bridge CFCs.

7 Conclusion

This chapter presents the summary of the main ideas and contributions along with possible avenues for further research and recommendations based on the key findings.

7.1 Thesis Summary

7.1.1 Flexible Power Flow Between DC Nodes Using DC CFCs

Meshed dc grids will require a greater degree of line current control as the current carrying capability of dc lines is limited by their thermal and electric stress limits. Thus, the line current must be maintained within the permissible operational region to protect the lines from damages. A small dc voltage injection (1-2 % of the rated system voltage) in series with the congested lines can virtually increase or decrease their impedances and consequently alter their current flow. The most straightforward way to achieve current control is through the inclusion of a variable resistor. It has been demonstrated that the variable resistor based CFCs, R and RC-CFCs, are capable of providing required current control at the cost of high power losses which may not be acceptable in practice.

In this thesis three types of inter-line CFCs (C, 1B and 2B-CFCs) have been introduced to minimise the power losses by exchanging the power between dc nodes. Each variant share the same fundamental characteristic but offers unique advantages for deployment. Among the proposed devices, the C-CFC provides the better solution in terms of footprint and cost as it

utilises the by-pass elements for current control. Conversely, 1B and 2B-CFCs provide better controllability (four quadrant) compare to C-CFC where the operation of C-CFC is limited to two quadrants as its voltage source element cannot be discharged when line currents flow in opposite directions. The lack of controllability of the C-CFC may be relieved by the installation of multiple devices, which may be afforded due to its low cost. A multi-port CFC could increase the control flexibility and eliminate contingencies arising from the failure of a single or multiple ports.

The operation and control of proposed inter-line CFCs have been experimentally validated in a meshed MTdc grid test-rig against simulation results. It has been shown that regardless of the configurations, the controllability and reliability of the MTdc grid may be increased by a CFC that regulates and redistributes line currents. The experimental study demonstrates that a n-port CFC can be used to facilitate current control on $n-1$ lines.

During the transition from by-pass mode to current control mode, use of a single loop current controller could leads to overvoltage across the CFC capacitor. This could introduce additional stress on CFC and dc line. To this end, two control approaches have been taken. In the first approach, a single modulation controller has been proposed to maintain the capacitor voltage within a safe limit by adding an inner voltage loop. In the second approach, a dual modulation scheme has been proposed to independently control the line current and capacitor voltage. The dual modulation scheme provides faster current control compared to single modulation scheme due to decoupled voltage and current regulation. In contrast, the single modulation controller is more suitable to establish a communication-free control scheme as the required capacitor voltage is determined by the outer controller.

Besides current control, a CFC can be used provide auxiliary pole balancing service in presence of pole imbalance that occurs due to cable degradation or asymmetrical cable tapping. The imbalance can be eliminated by providing dc voltage injections in series with dc lines. This improves the system performance by balancing the voltages of negative and positive poles. This could eliminate the need of a star-point transformer which is expensive and requires a larger installation platform.

The CFC generates pulsed dc voltages in series with the dc lines. This increases the ripple on

line current and introduces additional stress on dc lines. It has been observed that introduction of a CFC has increased the harmonics content on the dc side by 20% at a switching frequency of 500 Hz. Thus, extra power losses are generated on dc lines and other passive elements. Generally, in power system, the amount harmonics generated by a power electronic device must be maintained within an adequate amount to minimize its impact on the operations of other components. Following this line, contribution of CFC operation to dc side harmonics must be minimised. It has been shown that the harmonic content can be reduced by increasing the switching frequency of the CFC. Conversely, a passive filter can be employed to eliminate the harmonics content.

7.1.2 Control and Protection of CFCs on Meshed DC Grids

With enlarging dc grids, deployment of a single CFC is not adequate enough to achieve flexible power flow control. Since inter-line CFCs are inexpensive, a dc grid could be employed with multiple CFCs at different locations. This increases the grid control flexibility and reduces the stress on a single CFC. For a given point of grid operation, multiple CFCs could be available to provide the required current control. The amount of required series dc voltage injection for current control is a variable reflecting the configuration of the dc grid at a point in time. Therefore, the operation between CFCs must be coordinated to avoid conflicts between them. This has been achieved by proposing a centralised hierarchical control scheme. The proposed scheme reduces the system losses ans stress by optimizing the required dc voltage among the active CFCs.

In chapter 3, the R-CFC has reached its operational limit (i.e. maximum dc voltage injection) before achieving required current reduction. Based on this finding, a new control scheme called voltage sharing mode has been proposed to share the required dc voltage between multiple CFCs. It has been shown that when multiple CFCs are employed, the workload of a CFC that has reached its maximum operating point can be reduced by sharing the dc voltage compensation among the other CFCs. This increases the control flexibility and reduces the stress level on CFCs. Potential control conflicts between active CFCs can be eliminated by restricting the operation of a single CFC in current control mode and the remaining CFCs in voltage control mode. The concept has been adopted to coordinate the operation between multiple CFCs in an event of

communication failure.

Since the CFCs are series connected devices, a failure could interrupt the dc lines current flows, leading to instability. Thus, CFC could experience overcurrent and overvoltage, which could lead to permanent failure. The system response during the internal failure has demonstrated need of surge arrestor and additional by-pass switches. The experimental based dc fault analysis on 1B and 2B-CFCs have revealed that the protection of CFCs is mainly determined by the response times of CFC bypass switches and DCCBs. The by-pass switches must be to handle the fault current without deterioration as fault current is diverted to these switches following the fault detection.

7.2 Publications

7.2.1 Journal Papers

(a) S. Balasubramaniam, C. E. Ugalde-Loo, J. Liang, T. Joseph, R. King and A. Adamczyk " Experimental Validation of Dual H-Bridge Current Flow Controllers for Meshed HVdc Grids" in *IEEE Transactions on Power Delivery* (Accepted, special issue on "Frontiers of DC technology", 2017).

(b) S. Balasubramaniam, J. Liang, C. E. Ugalde-Loo, R. King and A. Adamczyk " Series Current Flow Controllers for DC Grids" in *IEEE Transactions on Power Delivery* (Submitted, 2017).

(c) S. Balasubramaniam, J. Liang, C. E. Ugalde-Loo, and T. Joseph " Power Flow Management in Meshed DC Grids using Capacitive based Current Flow Controllers" in *IEEE Transactions on Power Delivery* (Submitted, 2017).

(d) S. Wang, J. Guo, C. Li, S. Balasubramaniam, R. Zheng and J. Liang, "Coordination of DC power flow controllers and AC/DC converters on optimising the delivery of wind power," in IET Renewable Power Generation, vol. 10, no. 6, pp. 815-823,7 2016.

7.2.2 Conference Papers

(a) S. Balasubramaniam, J. Liang and C. E. Ugalde-Loo, "Control, Dynamics and Operation of a Dual H-Bridge Current Flow Controller," in *IEEE ECCE*, Montreal, Canada, 2015.

(b) S. Balasubramaniam, J. Liang and C. E. Ugalde-Loo, "An IGBT Based Series Power Flow Controller for Multi-Terminal HVDC Transmission," in *IEEE 49th UPEC*, Cluj-Napoca, Romania, pp. 1-6, 2014.

7.3 Future Research

The present research work has opened a number of avenues for further research. By addressing them it will be possible to define the most feasible engineering solution towards full deployment of CFCs in dc grids. The potential research lines are listed below:

- **Hardware implementation of DCCB based hybrid CFC:** In Chapter 3, a hybrid CFC topology has been proposed through utilising the load commutation switches of DCCBs to provide current control. A hybrid CFC could significantly reduce the investment cost and footprint of a CFC. This research work could explore the possibility and challenges associated with the realisation of a hybrid CFC through experimentally studying its control and operation on a meshed dc grid under normal operation and dc faults.
- **Operation of multi-port CFC in an event of a port failure or line outage due to dc fault:** In chapter 5, a multi-port CFC has been used to achieve current control on multiple lines simultaneously. One of the main advantages of a multi-port CFC is that it can remain functional even after failure of n-2 ports. This research work is aimed to implement a new control scheme which should coordinate the operation between active ports though assigning them with new control objectives.
- **Impact of CFC switching on dc cable lifespan and passive filter design:** The pulsed dc voltage injections in series with dc cables could increase the stress level on cables. This could reduce the cable life span and lead to deterioration. Therefore, impact of CFC swicthing on dc cable operation must be studied to define the filtering requirement prior to CFC deployment.

- **Hardware-in-the-loop (HIL) based experimental validation of ac/dc based CFCs:** In literature, operation and control of ac/dc based CFCs have been analysed only using simulation. The experimental validations of these devices have not yet been discussed. This research work bridges this gap by analysing the characteristics, range of operation, control, and dynamic operation of ac/dc CFC configurations through experiments on a meshed HVdc test-rig.

Appendices

A Four-Terminal MTdc Grid System Parameters

Table A.1 includes the parameters of the VSC terminals. The dc line parameters used in the simulation of Chapter 2 are given in Table A.2. The dc lines have been modeled as PI sections [68, 69], where the electrical parameters have been taken from a cable manufacturer [70] and line lengths adapted from [13].The line lengths used in our work have been scaled by a factor of 1/4 from the ones reported in [35] (i.e. the actual North Sea grid distances). Table A.3 provides the initial dc voltage and power reference set-points. The negative signs indicate that power is added to the AC system from the DC grid. In this case, the terminals are operated under inversion mode. Conversely, terminals with a positive power injection are adding power to the DC grid from AC system, implying a rectification mode.

Table A.1: VSC terminals: System parameters

Parameter	Value
AC transformer	430 kV/320 kV
Nominal power	1 GW
Phase inductance and resistance	49.89 mH/153.9 mΩ
DC capacitance**	200 μF
Converter f_{sw}	1650 Hz
AC frequency	50 Hz
DC voltage	640 kV

** Dc link capacitance can be estimated using the following equation [31]:

$$C_{dc} = \frac{S}{V_{dc} \cdot \Delta V_{dc} \cdot 2\omega_e} \tag{A.1}$$

Where S, V_{dc}, ΔV_{dc} and ω_e denotes the apparent power, nominal dc voltage, allowed ripple value and electrical frequency, respectively.

Table A.2: DC line parameters [13, 70]

DC Line	L_{12}	L_{13}	L_{14}	L_{24}	L_{34}
Length [km]	125	80	125	160	160
Resistance [Ω]	2.4	1.53	3.84	3.07	3.07
Inductance [mH]	30	19.2	48	38.4	38.4
Capacitance [μF]	19	12.16	19	24.32	24.32

Table A.3: Initial dc voltage and power reference values

Terminal	T_1	T_2	T_3	T_4
$P_{\text{DC,ref}}$ [MW]	800	-	700	−500
$V_{\text{DC,ref}}$ [kV]	-	640	-	-

Table A.4: CFCs system parameters

Parameter	Type of CFC	
	Thyristor	H-bridge
AC transformer [kV]	320/4	320/2.5
Nominal power [MW]	8	8
Phase inductance [mH]	0.49	0.49
Phase resistance	-	-
DC capacitance [F]	-	5.2 m
Limit. induct. L_p, L_n [mH]	10	-
Smoothing induct. L_f [mH]	70	-
Converter f_{sw} [Hz]	-	1650
H-Bridge f_{sw} [Hz]	-	1000
AC frequency [Hz]	50	50
Capacitor voltage V_C [kV]	-	5
V_{CFC} [kV]	±5	±5

The CFC parameters corresponding to the topologies in Figs. 2.6, and 2.10 of Chapter 2 are given in Table A.4. It should be highlighted that dc capacitance for the CFCs can be selected as a trade-off among the maximum voltage ripple, module voltage rating, power losses and switching frequency. The values shown in Table A.4 were obtained by defining the following constraints: a maximum voltage ripple of 10% to minimize the stress level on the capacitor, and maximum power losses of 0.001% of the system power rating.

B HVdc Test-Rig Parameters

The test-rig parameters are listed Table B.1. The test rig consists of three 2kW voltage source VSCs, emulated DC lines, four current flow controller (CFC) modules and a dSPACE controller. The VSCs have been arranged in symmetrical monopole configuration and rated at +/- 125V. Three autotransformers connected to the 415V AC power supply in the lab were used to represent three AC grids. The DC cables are represented by emulated RL circuits.

Table B.1: Specifications and parameters of the three terminal test-rig

Devices	Specifications	Operating Rating
VSCs	Rated power	2 kW
	Rated ac voltage	140 V
	Rated dc voltage	250 V
	Topology	Two-level symmetrical monopole
AC inductors	L_{g1}, L_{g2}, L_{g3}	2.2 mH
DC lines	L_{12}	2.4 mH
	L_{13}	5.8 mH
	L_{23}	11.8 mH
	Equivalent R_{12}	0.045 Ω
	Equivalent R_{13}	0.68 Ω
	Equivalent R_{23}	0.18 Ω
DC capacitors	C_{g1}, C_{g2}, C_{g3}	1020 μF
Control system	dSPACE DS1005 / ControlDesk 3.2(Simulink interface)	

The fault generator, reported in Chapter 6, consists of a high-power-rated series connected resistor and an inductor. The fault generator parameters are summarized in Table B.2. It

provides a controlled DC fault analysis in the DC grid. The fault current is limited by the size of the resistance and the inductance. The generator can be used to study pole-to-ground faults and pole-to-pole faults.

Table B.2: Specifications of the dc fault generator

Parameters	Operating Rating
Voltage rating	900 V
Current rating	30 A
R_f	14 Ω
L_f	45 mH

The VSCs and CFC controller parameters are provided in Table B.3. The VSC inner-loop and outer-loop controllers are realised with PI controllers. In Table B.3, the PI controllers are represented in the form: $K(s) = K_p + \frac{K_i}{s}$.

Table B.3: Controller Parameters

Device	Controller	Parameters
VSC	inner-current(dq)	$K_p = 45$ V/A, $K_i = 45000$ V·s/A
	dc voltage	$K_p = 0.2$ A/V, $K_i = 20$ A·s/V
	active power	$K_p = 0.2$ A/W, $K_i = 20$ A·s/W
	reactive power	$K_p = 0.3$ A/VAr, $K_i = 10$ A·s/VAr
R and RC-CFCs	current controller	$K_p = 112\times10^{-3}$ V/A, $K_i = 1.2$V ·s/A
C-CFC	current controller	$K_p = 5\times10^{-3}$ V/A, $K_i = 0.5$ V·s/A
	capacitor voltage	$K_p = 100\times10^{-3}$ V, $K_i = 1.8$ V ·s
2B-CFC	current controller	$K_p = 112\times10^{-3}$ V/A , $K_i = 1.2$ V·s/A
	capacitor voltage	$G_k(s) = 14\left(\frac{5\times10^{-3}s+1}{2.1\times10^{-4}s+1}\right)\left(\frac{13\times10^{-3}s+1}{s}\right)$
1B-CFC	current controller	$K_p = 5\times10^{-3}$ V/A, $K_i = 0.5$ V·s/A
	capacitor voltage	$G_k(s) = 14\left(\frac{5\times10^{-3}s+1}{2.1\times10^{-4}s+1}\right)\left(\frac{13\times10^{-3}s+1}{s}\right)$
CFC gain	K_c	5000
Feedback loop gain	K_f	0.09

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