# The 2018 GaN power electronics roadmap

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## Abstract

GaN is a compound semiconductor that has a tremendous potential to facilitate economic growth in a semiconductor industry that is silicon-based and currently faced with diminishing returns of performance versus cost of investment. At a material level, its high electric field strength and electron mobility have already shown tremendous potential for high frequency communications and photonic applications. Advances in growth on commercially viable large area substrates are now at the point where power conversion applications of GaN are at the cusp of commercialisation. The future for building on the work described here in ways driven by specific challenges emerging from entirely new markets and applications is very exciting. This collection of GaN technology developments is therefore not itself a road map but a valuable collection of global state-of-the-art GaN research that will inform the next phase of the technology as market driven requirements evolve. First generation production devices are igniting large new markets and applications that can only be achieved using the advantages of higher speed, low specific resistivity and low saturation switching transistors. Major investments are being made by industrial companies in a wide variety of markets exploring the use of the technology in new circuit topologies, packaging solutions and system architectures that are required to achieve and optimise the system advantages offered by GaN transistors. It is this momentum that will drive priorities for the next stages of device research gathered here.

## Introduction

Silicon-based Insulated Gate Bipolar Transistors (IGBTs) and Superjunction MOSFETs are fundamental components of present day power electronic systems for the conversion, control and conditioning of electrical energy, from generation to the point of load. If silicon devices were to be replaced by a more efficient semiconductor such as GaN, compact converters with ultra-high density can be designed only because the breakdown strength and electron mobility in GaN are respectively 10x and 2-5x higher. These basic material properties translate into smaller devices leading to higher frequency of operation, lower switching losses, and reduction in the component count and size of passives. This was demonstrated by over 100 hours testing by NREL of 2kW GaN inverters designed by the Red Electrical Devils, winners of the Google Little Box Challenge in 2015. Compact modules translate directly into lower weight, volume and cost. Coupled with increasing concern and government commitment to global warming, there are now strong commercial and legal pressures to accelerate adoption of these advantages into production systems.

Applications are now emerging that have no other practical solution than GaN. Take for example the automotive industry: GaN is the semiconductor of choice for power converters throughout vehicle electronics apart from the final drive inverter. Even here, there is now a very strong push to create production devices capable of switching as much as 100 Amps at 900 Volts. The advent of mass adoption of electric vehicles will in turn accelerate two other major markets that depend on highly efficient high-density power converters. Charging electric cars will require intelligent switching in the local power distribution grid to manage local generation and storage of electrical power in order to balance the load presented to the distribution grid. Simultaneously, IT infrastructure to support autonomous driving will create another massive parallel requirement for efficient compact power conversion.

GaN has evolved to the point where the cost of the transistor itself is no longer considered as the key driver in system cost. The novel solutions that the technology facilitates, provide savings in both manufacturing and running costs. Focus will come to bear on manufacturing parts in volume that will finally demonstrate the predicted price learning curves and focus attention on those research avenues that provide the fastest route to manufacturing maturity.

First generation production devices are now available from a broad range of suppliers including Transphorm, EPC, Panasonic, Infineon, GaN Systems, Dialog and Navitas. Each currently represents a different combination of process and design technology but their existence, proven performance advantages over silicon devices; reliability and manufacturability are seeing them designed into emerging applications in potentially massive new market applications. Investment in the GaN supply industry by major global companies such as Google, BMW and Delta Electronics underline the importance of GaN devices to the Automotive, Information Technology and Power Supply industries. It is the focus of research and development in the manufacturing value chain beyond the transistor in these new systems that will have a very strong effect in directing the next phase of the roadmap for GaN semiconductor device technology

This work brings together a palette of advanced research into GaN process developments presented by global leaders in GaN process and device technology that will inform solutions to challenges driven by the specific needs of converter and system development. Emerging demands that will feed from this work are the need to achieve 900V breakdown in applications for local 3 phase grid

interface and high-speed charging for vehicles, bi-directional switching, low inductance high thermal efficiency packaging and the potential to include on-chip sensing and control.

We hope you enjoy this peek into an enticing perhaps all-GaN future!

# 1 - Manufacturing Challenges of GaN-on-Si HEMTs in a 200 mm CMOS fab

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**Status**

GaN is anticipated to be the next generation power semiconductor. With a higher breakdown strength, faster switching speed, higher thermal conductivity and lower on-resistance ($R_{on}$), power devices based on this wide-bandgap semiconductor material can significantly outperform the traditional Si-based power chips. As such, GaN-based power devices will play a key role in the power conversion market within battery chargers, smartphones, computers, servers, automotive, lighting systems and photovoltaics.

In absence of viable low-cost GaN bulk substrates, GaN is grown on a variety of substrates, the most popular being sapphire, silicon carbide (SiC) and silicon (Si). Si substrates have become attractive for GaN growth because of their larger wafer diameter (200 mm and higher) though the large mismatch in lattice constant and coefficient of thermal expansion (CTE) imposes epitaxy challenges, especially for larger Si substrate sizes. Moreover, GaN devices are naturally normally-on or depletion mode (d-mode) devices whereas, to replace commercially available Si power devices, the GaN devices should be normally-off or enhancement-mode (e-mode) devices. Furthermore, GaN devices should be fabricated by a low-cost, reproducible and reliable production process. While e-mode operation can be readily achieved by adding a p-doped GaN layer under the gate, hereby lifting the conduction band at equilibrium and resulting in electron depletion, the ability to manufacture GaN-on-Si power devices in existing 200 mm Si production facilities offers further cost competitiveness to the Si power technology.

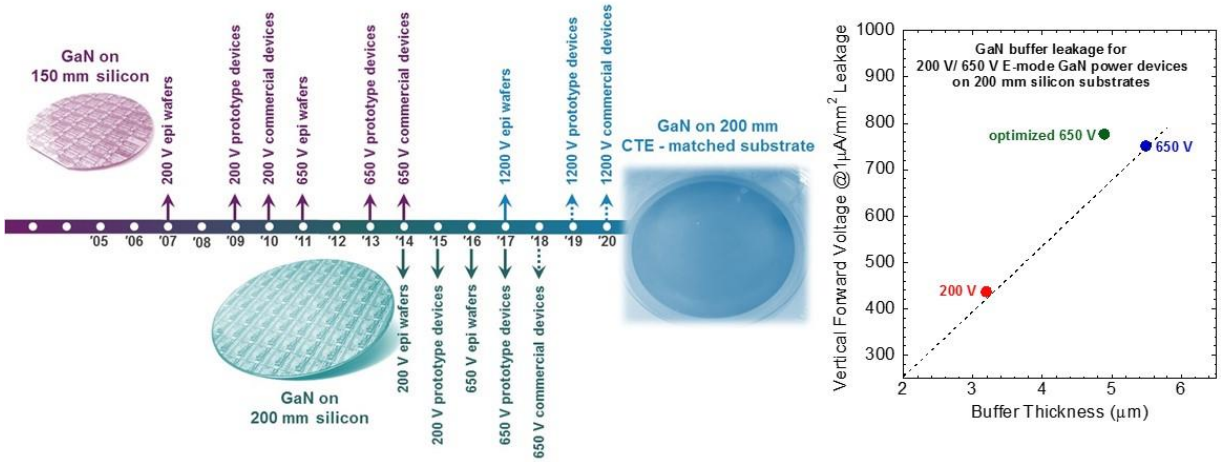


**Figure 1.** Left: timeline for 200 V, 650 V and 1200 V GaN-on-Si epi wafers, prototype and commercial enhancement-mode power devices. Right: buffer leakage at 25˚C of imec's 200 V (red) and 650 V (blue and green) GaN-on-Si epi wafers after full processing in the 200 mm CMOS fab.

Initially, the development of GaN-based technology focused on high voltage (200 V and 650 V) power-switching applications. First commercial 200 V e-mode GaN devices, fabricated on 150 mm Si substrates, were released in 2010 and first 650 V commercial devices followed in 2014 (Figure 1, left). After first developing the technology on 100 mm [1, 2], and later 150 mm wafer sizes using Au-free metallization schemes [3], imec has been pioneering 200 mm GaN-on-Si technology with first GaN 200

V epitaxy [4] and devices in 2014 [5-9]. The imec 200 mm GaN-on-Si e-mode transistor and diode platform was recently extended and qualified for 650 V applications. Today, the focus is on the technology development for higher level of integration and for 1200 V applications using 200 mm CTE-matched polycrystalline AlN substrates.

**Current and Future Challenges**

Because of the much higher CTE of GaN compared to Si, the GaN in-film stress during epitaxial growth needs to be tuned compressive to compensate for the tensile stress during cool down. The use of 1.15 mm-thick 200 mm Si substrates is beneficial to reduce wafer warp during growth and hence avoiding wafer cracking. Without significant hardware changes and lowering the robot speed of some handling systems, the thicker and heavier GaN-on-Si wafers can be processed in the standard imec CMOS fab. The warp specification of 50 μm is sufficiently low to avoid chucking issues on electrostatic chucks. Prior to the fab introduction, the 200 mm GaN-on-Si wafers are tested for mechanical robustness, hereby reducing the wafer breakage during processing to less than 1%. After epitaxy, Ga and Al contamination on the wafer backside is unavoidable. Since Ga is a p-type dopant for Si, one of the major concerns of processing GaN wafers in a CMOS fab is Ga cross-contamination. The Ga and Al backside contamination after epitaxy is effectively removed by an in-house developed $HF/H_2O_2$-based cleaning procedure, hereby reducing the contamination level of the wafer backside and bevel to below $10^{11}$ at/cm$^2$. Moreover, imec's e-mode pGaN process flow contains (Al)GaN dry etch steps. A first one to dry etch the pGaN layer selectively to the AlGaN barrier layer, and a second to recess the AlGaN barrier in the ohmic contact areas. Since conventional F-containing cleaning recipes of the dry etch tools can form non-volatile $GaF_x$ species (i.e. $GaF_x$ is not volatile below 800°C), a $Cl_2$-based clean that forms volatile $GaCl_3$ at ~200°C is used. This cleaning procedure effectively and reproducibly maintains the Ga contamination level in the dry etch tools well below the maximum allowed level.

Finally, since Au is a rapidly diffusing contaminant in Si that deteriorates the minority carrier lifetime, the GaN metallization schemes need to be Au-free. Because of the high bandgap and the absence of explicit doping of the epilayers, especially the development of Au-free ohmic contacts is challenging. By using a Si/Ti/Al/Ti/TiN ohmic metal scheme and decreasing the alloy temperature to 565˚C, the ohmic contact resistance could be lowered to 0.3 Ω·mm with excellent reproducibility and uniformity.

**Advances in Science and Technology to Meet Challenges**

Because the breakdown field of the Si substrate is ten times lower compared to GaN, the breakdown voltage of the power devices is dictated by the GaN buffer thickness. In Figure 1 (right) the vertical buffer breakdown voltage (at 1 μA/mm$^2$ leakage) is plotted versus the buffer thickness. Straightforward extension of the 3.2 μm-thick 200 V buffer (red) to 5.5 μm for 650 V applications (blue) was resulting in low wafer yield: the yield related to wafer breakage in the mechanical screening test was reduced from 90% for 200 V to 77% for 650 V. This issue was tackled by implementing Si substrates with high boron doping (0.01 Ω·cm resistivity) hereby increasing the mechanical wafer strength, and by developing a new buffer concept with reduced thickness (4.9 μm, green) that resulted in an equally high buffer breakdown voltage while maintaining the low buffer dispersion, and increasing the wafer yield for 200 V applications to 99% and to 97% for 650 V applications.

By optimization of the cleaning and dielectric deposition conditions, together with the field plate design, state-of-the-art 650 V 36 mm gatewidth power devices with 2.1 V threshold voltage (at maximum transconductance), 13 Ω·mm $R_{on}$ and 8 A output current (Figure 2a and b) were obtained

on 200 mm wafer size and processed in a standard CMOS wafer fab. Moreover, the devices exhibit dynamic $R_{on}$ dispersion below 20% (10 μs on, 90 μs off) up to 650 V over the full temperature range from 25°C to 150°C (Figure 2c).

For 1200 V power applications, imec is working on using polycrystalline AlN (poly-AlN) substrates that have a better CTE-match to GaN. In this approach, a thin crystalline Si layer is transferred to a 200 mm poly-AlN substrate. This new technology is promising to go beyond the current technology limitations, because it is possible to grow thicker, higher quality GaN buffers on 200 mm substrates with a standard thickness of 725 μm. Imec has already demonstrated the CMOS-compatibility of these substrates in terms of contamination and wafer handling [10]. Furthermore, first high quality transistors have been processed illustrating the high promise of this new approach.

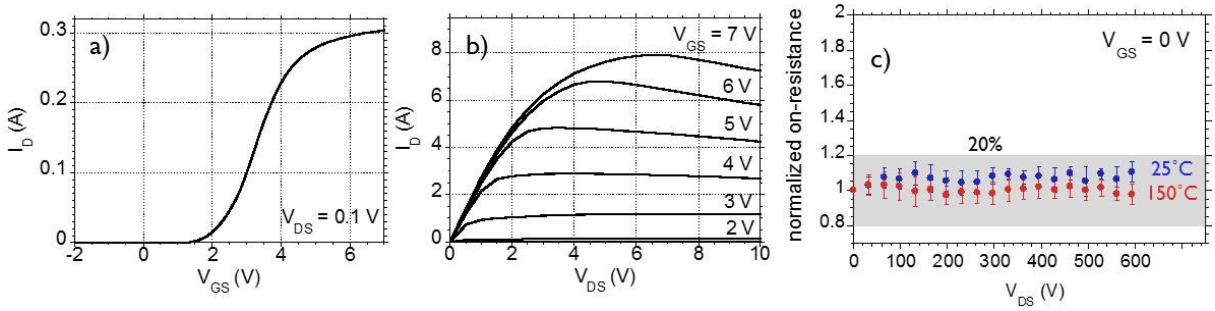


**Figure 2.** (a) Transfer and (b) output characteristics of a typical 36 mm gate width 650 V e-mode power device, and (c) the dynamic $R_{on}$ device dispersion. The devices were fabricated in imec's 200 mm CMOS fab.

## Concluding Remarks

GaN technology offers faster switching power devices with higher breakdown voltage and lower on-resistance than Si, making it an ideal material for advanced power electronic components. For cost competitiveness, GaN power devices are preferably fabricated on large diameter Si substrates in existing Si CMOS fabs. Due to the large mismatch in lattice constant and thermal expansion coefficient, the epitaxy of GaN on large diameter Si substrates is very challenging. Imec has demonstrated for the first time that is possible to manufacture 200 V and 650 V GaN-on-Si e-mode devices in a 200 mm CMOS fab. For 1200 V applications, it is proposed to transfer the technology to 200 mm Si-on-poly-AlN substrates, which is CTE-matched with GaN. This substrate technology allows for thicker GaN buffers, which is needed to reach 1200 V and beyond, and was also assessed to be CMOS-compatible in terms of contamination and tool handling.

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# 2 – Epitaxial Lift-Off of GaN and Related Materials for Power Device Applications

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**Status**

GaN and other III-N compound semiconductors have had an enormous impact on optoelectronics—with the widespread adoption of LEDs, lasers, and solar-blind photodetectors—as well as RF electronics for both consumer wireless infrastructure and military communications and sensing. The continuing advance of III-N electronics promises to bring this revolution also into the power electronics space. With power device concepts based both on extensions of conventional lateral FET designs, as well as concepts based on vertical transistor designs, GaN and related materials promise to dramatically enhance the performance, efficiency, and ubiquity of sophisticated power management and control functions. Advances in growth and substrate technologies for achieving high-quality material, along with improved device designs, promise to enable continued increases in device performance. In addition, novel processing techniques are also promising to provide significant performance, cost, and integration improvements. Among these processing-related advances, techniques that enable epitaxial lift-off and substrate transfer are especially attractive. Epitaxial lift-off has been demonstrated for optoelectronic applications (see e.g. [1], [2]), and offers the potential for improved light extraction, smaller device form factor, and ultimately more flexible displays as well as sensors for emerging applications such as wearables. In the power application space, epitaxial lift-off can enable substantial increases in thermal performance (through improved heat removal), electrical performance (through lower resistive losses and higher breakdown voltages), economics (through more efficient materials utilization, die size reduction, and substrate reclaim and reuse), and enhanced integrability with other electronics technologies. A range of epitaxial lift-off technologies for GaN and related materials have been demonstrated, including selective wet etching of ZnO layers [2], dry etching of epitaxial $Nb_2N$ layers by $XeF_2$ [3], mechanical exfoliation and separation using graphene or BN layers [4, 5], and band gap selective photoelectrochemical etching based on wet-chemical etching of lower-band gap materials such as InGaN [1, 6, 7, 8]. In addition to the mechanism by which the lift-off occurs, epitaxial lift-off processes may be distinguished by whether they lift off a single device (Fig. 1(b)) or small circuit (e.g., [1], [3]), or seek to lift off a larger film (Fig. 1(a)) either for subsequent processing into devices (e.g., [2], [4], [5]) or after fabrication of the devices is largely complete (e.g. [7, 8]).

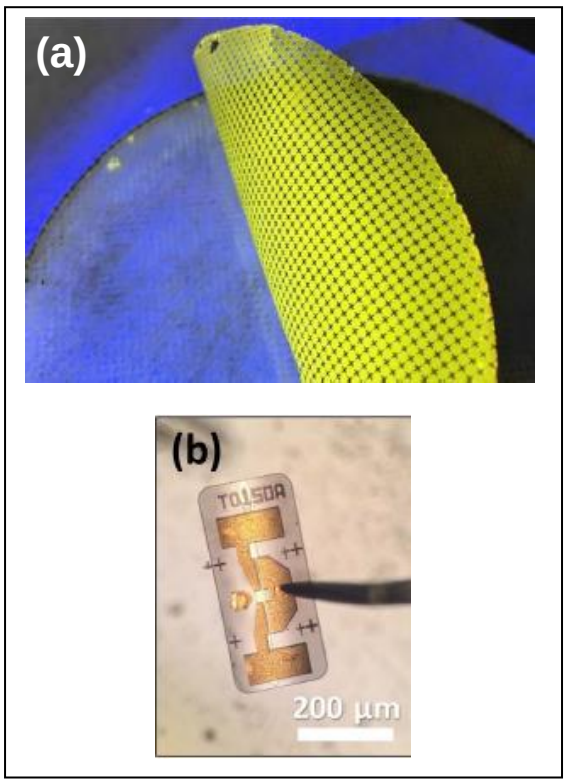


**Figure 1.** (a) Large-area (100 mm wafer) epitaxial lift-off of GaN-based epitaxial device layers achieved using band-gap selective photoelectrochemical wet etching of an InGaN [7]; (b) single-die release of a GaN-based device using dry etching of $Nb_2N$ with $XeF_2$ [3].

**Current and Future Challenges**

Advances in power electronics are poised to radically alter the design and implementation of electronic products and systems; ultimately, sophisticated power electronics and circuit topologies for enhanced efficiency and power-control capability could become ubiquitous if the key technological and economic challenges can be solved. Realization of this vision is currently constrained by cost, device performance, and integration challenges—all of which can be addressed by epitaxial lift-off. Due to the wide diversity of potential applications there is unlikely to be a single optimal solution; instead, we can expect different approaches to benefit different application segments. For example, for modest voltage and current requirements for which lateral devices (e.g. MISHEMTs) provide sufficient performance and economic benefit, use of conventional lattice-mismatched substrates such as SiC, sapphire, or Si is appropriate; epitaxial lift-off can then be used to accomplish substrate transfer for improved thermal or breakdown performance (see e.g. [9]), as well as the potential for reusing high-cost substrates (e.g. SiC) [3]. For applications where high currents and material-limited breakdown voltages are required, as well as applications where economics dictates a high areal current density, vertical device structures offer inherent advantages. However, these devices also place additional demands on material quality; while high dislocation densities are often tolerable in optoelectronic and lateral electronic nitride devices, these defects significantly compromise the performance of vertical devices. This can be addressed by homoepitaxial devices on bulk GaN substrates, but this in turn places more stringent demands on the epitaxial lift-off approach to avoid the generation of dislocations. The economic benefits of epitaxial lift-off from bulk GaN substrates are substantial, given their high cost and small diameter. In addition to substrate reuse, thermo-electric modelling indicates that direct bonding of lifted-off vertical FETs to a heatsink could enable die size reduction by more than 50% compared to devices on bulk GaN substrates [8]. Of the current techniques, only band gap selective photoelectrochemical etching with pseudomorphic InGaN release

layers has been demonstrated to maintain fully coherent single-crystal material from the bulk substrate through the device epitaxial layers, and so may provide a unique solution to achieving epitaxial lift-off of vertical devices on bulk GaN substrates. Reuse of bulk GaN substrates after lift-off has recently been demonstrated with lift-off of GaN pn junctions (Fig. 2) demonstrating a pathway to improved economics; future efforts will be needed to fully realize the thermal and integration benefits.

**Advances in Science and Technology to Meet Challenges**

To address the challenges and fully realize the benefits of epitaxial lift-off as an enabling technology for high-performance, low-cost, ubiquitous power electronics, significant technological challenges must be overcome. For material-quality sensitive applications such as vertical devices, additional development of lattice-matched or pseudomorphic release layers is an important future direction. Current demonstrations have been based on the use of InGaN release layers [1, 6, 7, 8]; while this approach has been successfully demonstrated for both single-die release and lift-off of large areas (> 100 mm wafer), the lateral etch rate is modest and the surface morphology of the N-face GaN is not yet easily controlled due to limited etch rate selectivity. Additionally, the use of pseudomorphic release layers such as InGaN have been reported to influence the mechanical behaviour of released structures [10]. Development of strain-control strategies or deposition of alternative release layer materials with basal plane lattices commensurate with the GaN devices are areas for future development and exploration. Another area that is largely unexplored to date is that of novel packaging and bonding strategies to leverage the unique features of devices fabricated using epitaxial lift-off. The thermal performance of ultra-thin devices has been projected [8], but experimental validation and–in particular—optimization for the unique characteristics of ultra-thin devices is an area for additional development. Heterogeneous integration of lifted-off devices with conventional electronics, and packaging of lifted-off devices for emerging applications such as flexible or ultra-thin form factors is another area where substantial additional innovation is needed. Finally, the reliability of lifted-off devices is an important topic, but one that has not yet been addressed due to the nascence of the technology.

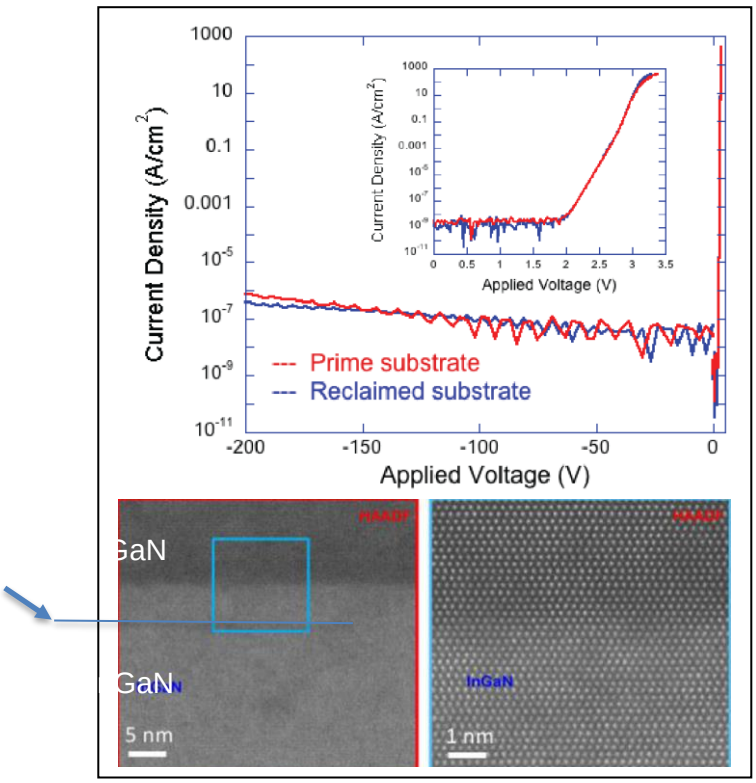


Figure 2. (a) Measured current-voltage characteristics of typical GaN vertical PN junction diodes on prime bulk GaN substrate and on a reclaimed substrate (i.e., after growth, lift-off, repolish, and a second device growth and fabrication sequence, validating that device performance on epi-ready prime and reclaimed/reused substrates is nearly indistinguishable. (b) TEM image showing pseudomorphic InGaN release layer growth [7].

## Concluding Remarks

Epitaxial lift-off is an emerging technology that is poised to be of significant benefit to the developing field of III-N based devices, and in particular to high-performance, cost-effective power electronics. The improvements in electrical and thermal performance, economic benefits derived from reduced die size and bulk GaN or SiC substrate reuse, and potential for enhanced heterogeneous integration with other electronics and packaging technologies makes epitaxial lift-off appear promising for advancing power electronics across a broad range of applications.

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# 3 – GaN-on-Si 200 mm for power devices

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**Status**

The main objective in the LETI power electronic roadmap is the miniaturization of power converters to increase the energy efficiency of the systems while reducing the cost. It is also important to improve reliability and ensure operation at higher temperatures (300 °C), with the markets of automotive (EV and HEV) and motor drives for industrial tools being targeted. To achieve these objectives for power convertors from a few Watts to several hundred kW, it is essential to increase their operating frequency [1]. GaN-on-Si power devices are capable of responding to these requirements because GaN allows high frequency switching (several MHz) and a higher power density than silicon (10 times greater), although these solutions must be implemented at the system level in order to fully benefit from the materials properties. Furthermore GaN on 200 mm Si enables CMOS compatible technology leading to lower cost and improved robustness of the processes.

LETI has chosen to develop MOS-HEMT GaN architecture, fabricating "Normally-Off" devices which give functionality similar to a classic silicon based MOS. To take full advantage of these devices, a route towards monolithic solutions for low and mid power applications and a route towards system in package is promoted at LETI, fig. 1, with 5 main axes of work: epitaxy, devices, passives, co-integration, and system architectures. Here we will focus on the device roadmap.

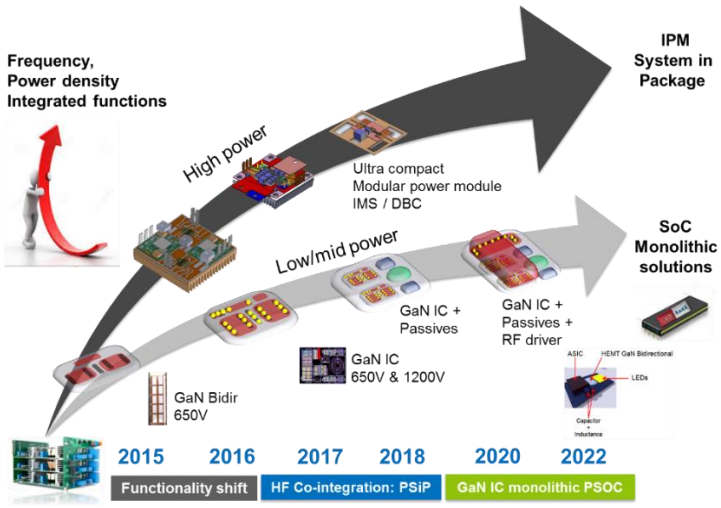


**Figure 1.** Power systems roadmap at LETI. An SOC (system on chip) route towards monolithic solutions is important for miniaturization for low and mid power solutions. For higher voltages, an ultra-compact power module is preferred [2]

**Current and Future Challenges**

Adoption of GaN in the industry requires high performance, high reliability devices produced at low cost. For automotive applications, GaN transistors of 1200 V - 50 A and 650 V - 200 A are targeted. Current requirements are a $R_{onS}$ below 1 mohm/cm², Fig. 2, with an $R_{dyn}$ of no more than 10 % of the $R_{onS}$, meaning low losses [4]. The epitaxy is expected to improve in several ways: Firstly, a constant

improvement in the buffer layers and active layers to decrease the dislocation density, even though this has not been proven to be essential for high quality HEMT performance, and a reduction in point defects which cause trapping; Secondly, a vertical leakage current lower than 1µA/mm$^2$ at 150°C and thirdly improvements and optimisations in the design of the epi stack, such as integration of back barriers to improve confinement of the free carriers in the potential well. Of course, all this has to be implemented while maintaining a wafer bow < 50 µm for a silicon wafer thickness of 1 mm maximum to enable the process in standard 200 mm tools [3].

The most developed structure to make normally-off GaN HEMTs is pGaN gate architecture. P-type GaN may have potential work function of up to 7.5 eV which makes pGaN an outstanding gate metal in addition to the depolarization effect for depleting the channel beneath the gate. However this design suffers from a compromise between the threshold voltage and the sheet resistance in the channel and so high positive threshold voltages are difficult to achieve. This is why at LETI we are developing an alternative strategy, the MOS-HEMT. This architecture is a hybrid monolithic device which essentially puts a MOS channel and a HEMT drift layer in series. At the heart of this technology is the MOS gate, which needs to be reliable and robust; a challenge that Si and SiC have already faced in the past.

**Advances in Science and Technology to Meet these Challenges**

These advances required to meet the challenges listed above can be described in five bullet points:

Simulation: to design complex architectures, capture process influence and describe device behaviour, simulations such as TCAD are of major importance. Currently, significant efforts are needed to ensure simulators properly recreate the physics of III-N materials and devices.

Device Characterisation**:** the JEDEC standards are not sufficient to fully qualify GaN-based power devices due to restrictive criteria. Dynamic properties and aging effects, which show common patterns with dielectric aging, are key topics to be understood in order to bring GaN-on-Si products to industrial maturity in mass markets.

Device technology: as discussed above, constant improvements are required in the epitaxy, with in particular improved defect characterization and analysis of their impact on device performance. The understanding of the gate oxide trap passivation will also be a significant scientific and technological challenge. The whole technology has to be CMOS compatible, which brings an additional constraint to GaN power device design, and the potential of GaN on 300 mm Si has to be investigated.

Thermal dissipation: The reduction in size of power devices when using GaN raises the challenge of thermal dissipation. In order to benefit from the full potential of GaN technology, the power density will need to be increased, and so process and packaging will need to be optimised to improve thermal dissipation.

Switching frequency**:** To allow high frequency switching, co-integration is key. Transistors, flyback diodes, rectifiers or drivers are examples of active devices that can be monolithically integrated to reduce parasitic elements and reach high performance converters.

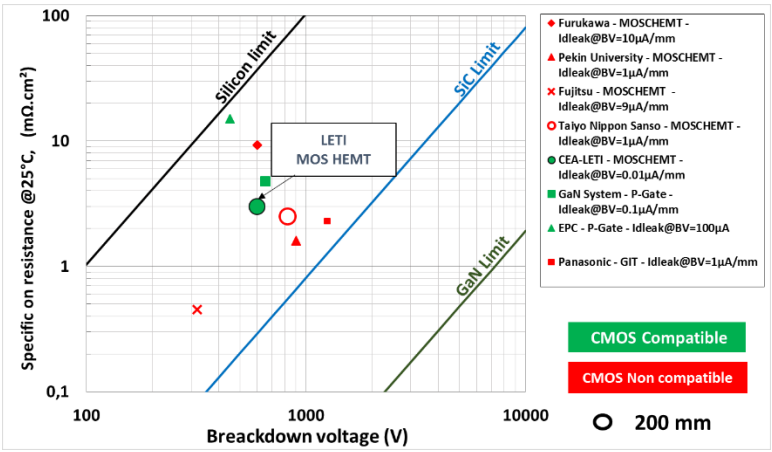


Figure 2. Specific on resistance versus breakdown voltage. Benchmark of different laboratory results versus CMOS or non CMOS compatible technology.

## Concluding Remarks

The use of GaN-on-Si as a substrate for high power transistors is becoming an increasingly common choice, as an affordable large area alternative to expensive bulk substrates. Although there are still significant challenges to be overcome in order to produce high quality devices on these substrates, GaN devices will take full advantage of both the remarkable properties of GaN, and of production in CMOS compatible fabrication plants to achieve high performance and low cost devices.

Furthermore, the development of high power integrated circuits on GaN on silicon wafers will further reduce costs and encourage the use of this technology. With all of these advances, it will surely not be long before GaN-on-Si devices become a huge market as the demand for highly energy efficient convertors becomes ever greater.

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# 4 - Buffer design in GaN-on-Silicon Power devices

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**Status**

Uptake of GaN devices for power applications requires that they can be manufactured in volume at comparable cost to Si components, and with validated device reliability. The key innovation that has made this possible is the ability to grow epitaxial device quality layers of GaN and AlGaN on 6" or 8" (111) Si wafers. Together with the development of Si CMOS compatible device process flows, this has allowed GaN power devices to be fabricated using existing Si fabrication lines with Si and GaN processing occurring in parallel. This section addresses the electrical and material design of the GaN-on-Si epitaxial platform that is now being used to realise HEMT devices for power applications.

GaN HEMTs were first successfully grown on Si in the 1990s, however the epitaxy did not have sufficient breakdown voltage for power applications. GaN-on-SiC RF devices used Fe doping to suppress short-channel drain leakage and increase drain breakdown, representing the first realization that the nominally insulating GaN layer underneath the 2DEG channel is actually electrically active and needs just as much design and optimisation as the upper barrier and channel region. However, Fe doping was found to deliver insufficient breakdown voltage when applied to high voltage power devices. Eventually it was found that a combination of a complex strain relief buffer together with carbon doping to control breakdown could achieve sufficient voltage handling[1]. Unfortunately there continued to be bulk trapping related issues collectively known as dynamic $R_{ON}$ dispersion or current collapse, and their solution has only recently been demonstrated commercially. The reasons for the wide variation in dynamic $R_{ON}$ performance achieved for apparently identical carbon doped epitaxies is only now becoming understood.

**Current and Future Challenges**

Key issues in epitaxial growth of GaN-on-Si are the lattice and thermal expansion coefficient mismatches which make strain management critical. As a result large numbers of defects (>$10^{10}$cm$^{-2}$) are generated, and cracking of the GaN layers can occur on cooling from the growth temperatures (≈1000°C) [2]. The epitaxial layer structure which has been adopted to solve these issues is shown in Figure 1. A nucleation layer of AlN is universally used to initiate growth and avoid the Ga/Si eutectic that causes "melt-back". This is followed by a strain relief stack, where two successful approaches have been found based on either a step-graded AlGaN layer[3], or a superlattice of AlN/GaN[4]. The detailed stack design is normally proprietary. These buffers are used to induce compressive strain during growth which counteracts the tensile strain introduced on cooling, preventing cracking and yielding a flat wafer. To aid growth uniformity, thick Si substrates (1mm) tend to be adopted, which also helps to reduce the wafer breakage during processing which has been observed for standard thickness wafers (675µm). Total epi-layer thickness as large as 8µm can be achieved, but the challenges of wafer bow and stress become more difficult to overcome. Typical dislocation densities at the surface of the stack, i.e. at the 2DEG, are ≈$10^{9}$cm$^{-2}$.

Due to the incorporation of impurities and point defects, as-grown GaN is typically n-type and it has been found that it is essential to add deep level dopants to suppress leakage. The dopant of

choice is carbon[1] with a density well above $10^{18}cm^{-3}$ delivering excellent isolation and breakdown voltage. Carbon primarily incorporates substitutionally on the nitrogen site[5]. This pins the Fermi level about 0.9eV above the valence band making the GaN:C p-type, with electrical transport being via low mobility holes rather than electrons. It is found that the carbon doping must be spaced away from the active 2DEG to reduce trapping effects[6]. A key issue with carbon doping is current collapse (dynamic $R_{ON}$)[7]. Charge trapping occurs in the epitaxial bulk during off-state operation when there is high drain bias. When the device is switched on, trapped negative charge reduces the electron density in the active channel and increases the on-resistance. Some current commercial devices show as much as a factor of two increase following off-state bias.

**Advances in Science and Technology to Meet Challenges**

Suppression of current collapse is key for technology uptake. The p-type nature of GaN:C means that there is a p-n junction between the 2DEG channel and the bulk of the epitaxy, meaning that the bulk can be electrically floating. Suppression requires that this floating buffer is grounded to the active 2DEG channel preventing it from providing a back bias, and hence, counter-intuitively, a vertical leakage path is essential. Figure 2 shows an electrical network representation of the buffer, and simulations to show the impact of different leakage paths[8]. It is found that there is a trade-off between vertical leakage and current-collapse, with careful process control of leakage paths being absolutely required. Current state-of-the-art power devices are able to achieve less than 10% change in $R_{ON}$ in the 25-150°C temperature range by careful leakage control[9]. Recently it has been shown that changing the stoichiometry of the $Si_3N_4$ surface passivation can change the bulk vertical leakage and control the dynamic $R_{ON}$[10]. Further work is still required to achieve a guaranteed simultaneous optimisation of leakage and current collapse.

Many power switching topologies require the series connection of devices. Current technologies would require a hybrid packaging approach to prevent undesirable Si substrate bias being applied to the upper transistor in a half-bridge configuration. New approaches to allow transistor electrical isolation are therefore required before full integration is feasible. One approach being investigated is the use of buried oxide layers with 200V isolation being achieved by imec.

Operating at voltages much above 650V will require the growth of thicker epitaxy, and that requires a solution to reducing stress. Although single crystal GaN or AlN would be the ideal substrates, cost and wafer size make this unlikely to have any impact. One possible approach is the use of thermal expansion matched substrates as an alternative to Si wafers. For example polycrystalline AlN wafers have been successfully used as a growth substrate, achieving 18µm thick epitaxial layers.

**Concluding Remarks**

GaN-on-Si based power transistors are already achieving impressive performance and reliability based on the remarkable ability to grow strain-engineered, electrically-optimised, high-quality epitaxy on low cost 6” or 8” Si wafers. Buffer-related trapping leading to dynamic $R_{ON}$ has been a serious issue, requiring a delicate balance between leakage and performance for its suppression. This is only now being achieved by commercial suppliers. Going significantly beyond the current 650V market segment to much higher voltages will require major changes and innovation in the substrates and epitaxy to allow thicker epitaxial layers to be grown yet still retaining control of wafer bow.

**Acknowledgements**

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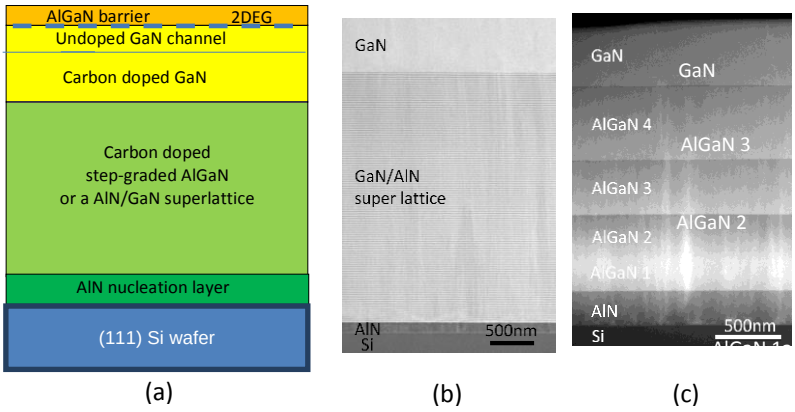


**Figure 1.** (a) Schematic cross-section of the typical epitaxial layer structure used for the manufacture of GaN-on-Si HEMTs. (b) TEM image of a GaN/AlN superlattice buffer layer and (c) a step graded AlGaN buffer layer, both on Si substrates.

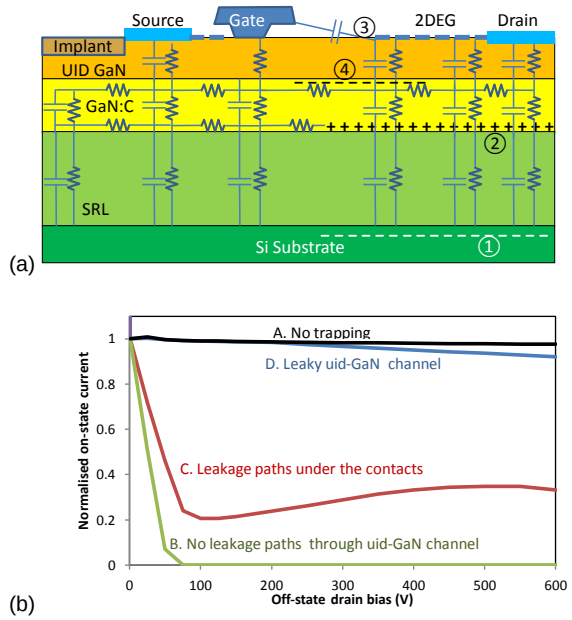


Figure 2. (a) Schematic showing leakage and capacitive paths within the buffer. ① to ④ indicate some of the key locations where charge accumulates. (b) Simulated dynamic $R_{ON}$ for different leakage paths within the buffer. All these different behaviours are observed in practice[8].

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# 5 - Challenges in growth for GaN power Electronics

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**Status**

Gallium nitride (GaN) based devices are promising for many power applications such as switching functions and inverters that can save a significant amount of energy. The performance and efficiency of these GaN power devices greatly rely on the epitaxial growth of GaN and related alloys. High quality GaN epitaxial growth can be achieved by using native free-standing GaN substrates. However, the downside of epitaxial GaN-on-GaN is it is expensive and only small-diameter GaN substrates. This in turn impede the mass production of GaN power devices at an affordable cost for commercial applications. To overcome this, the heteroepitaxial growth of GaN is carried out on foreign substrates such as silicon carbide (SiC), sapphire and silicon (Si). From commercial aspects, the heteroepitaxial growth of GaN-on-Si is attractive because of the large-size scalability of inexpensive Si substrates. Nevertheless, the areas of concern are the large differences in the physical properties between wide bandgap GaN and Si substrate that often results in poor crystal quality leading to high dislocation density, pits and cracks for GaN-on-Si. Therefore, appropriate epitaxial growth of GaN-on-Si and subsequent fabrication processes are absolutely necessary for power device applications. For example, several switching applications require lateral GaN-on-Si high-electron-mobility transistors (HEMTs) with high breakdown voltage (BV) [1]. To realize these GaN-on-Si lateral devices, we have used the metalorganic chemical vapor deposition (MOCVD) grown thick-AlN initial layer and GaN/AlN strained layer superlattice (SLS) structures. The AlGaN/GaN HEMTs grown on 8-inch silicon by using similar epitaxial growth technique delivered a high BV of 1.6 kV. For expanding the applications to electric and hybrid vehicles, high performance GaN power devices are required to drive high-power motors, power modules such as DC-DC converter and inverters. Typically, in these applications high-voltage GaN-on-Si vertical devices with reduced chip area are preferred. To facilitate the fabrication process of such devices, we have successfully grown thick GaN-on-Si vertical structures by using conductive buffer layers comprising of thin-AlN initial layer and SLS. The recent advances in the hetero epitaxial GaN-on-Si are encouraging for the growth of GaN power electronics on larger diameter Si substrates.

**Current and Future Challenges**

Despite its merits, the GaN-on-Si power devices have also associated technical challenges which need attention. Of these, the most important issue is the growth of a high-quality and thick GaN-on-Si. The large differences in lattice constants and thermal expansion coefficient between GaN and Si are responsible for the difficulties in the growth of high-quality and thick GaN-on-Si. The inset of Fig. 1 shows the cross-sectional structure of AlGaN/GaN HEMT on Si using metalorganic chemical vapour deposition (MOCVD). High temperature growth of GaN-on-Si could likely result in melt-back etching of Si substrate caused by Ga atoms [2]. As a result, deep pits, dislocations and cracks could arise, which in turn would deteriorate the device performance like an increase in buffer leakage, and reduced breakdown [3]. Therefore, the growth of high-temperature-grown AlN nucleation layer (NL) is indispensable to avoid both the melt-back etching and deep pits. Recent studies have revealed the influence of AlN NL on the vertical breakdown characteristics for GaN-on-Si and the AlN NL with better surface morphology and lower O impurity were preferred to grow highly resistive buffers [4]. Figure 1 illustrates the typical relationship between wafer bowing and total epitaxial thickness for the AlGaN/GaN HEMT on 4-inch Si. From this correlation, it could be understood that the use of GaN/AlN SLS is effective in controlling the bowing [5]. Subsequently, the growth of SLS is essential to control the wafer bowing for GaN-on-Si. Additionally, thick epi layers grown by using SLS multipairs supressed the vertical leakage and showed a vertical breakdown field of 2.3 MV/cm [6]. A high lateral $BV_{Off}$ of 1.4 kV was also demonstrated for AlGaN/GaN HEMT on Si grown with the above recommendations [7]. The recent systematic investigations and the promising results as discussed earlier would provide substantial understanding for the growth dynamics of epitaxial GaN typically on 8-inch Si substrates. Indeed, our AlGaN/GaN HEMT on 8-inch Si has shown a three-terminal off-state breakdown voltage 1650 V for the gate-drain distance of 50 µm. The availability of modern MOCVD reactors with multi-wafer capability and evaluation tools suggest promising features for GaN-on-Si lateral power devices.

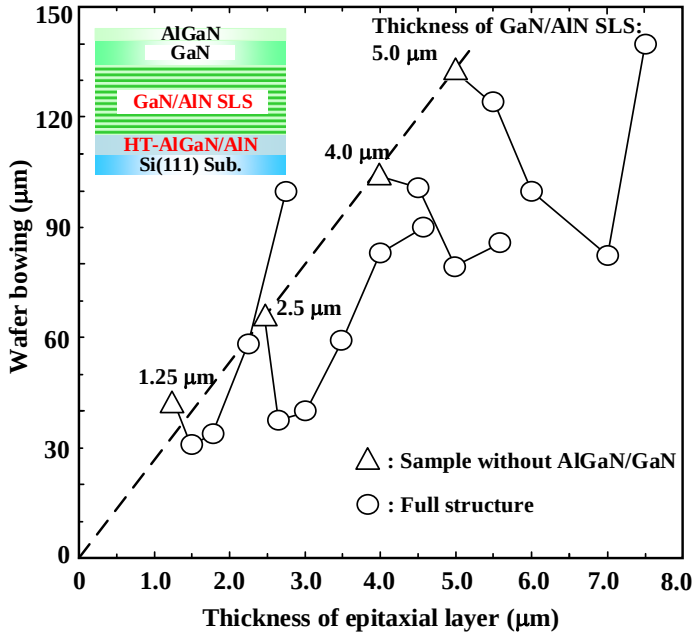


**Figure 1.** Wafer bowing as a function of total epitaxial layer thickness of AlGaN/GaN HEMT on Si. Copyright 2012 IEEE, reprinted with permission from Ref. 5.

**Advances in Science and Technology to Meet Challenges**

The GaN-on-GaN vertical devices are expected to play a vital role in future high-power conversion applications as it can reduce the overall chip area. However, the GaN substrate has disadvantages such as its limited wafer size and are expensive. Therefore, the realization of GaN-on-Si vertical devices is the upcoming challenge owing to growth and fabrication difficulties. Unlike the lateral AlGaN/GaN devices, deeper understanding on the growth and fabrication of GaN-on-Si vertical devices are required for potential power device applications. Some researchers have demonstrated the GaN-on-Si vertical p-n diodes fabricated by wafer bonding and substrate removal technology [8]. This technique could complicate the fabrication process and eventually lead to increase in cost. Others showed GaN p-n diodes by using a quasi-vertical structure [9]. Irrespective of these methods, a detailed study is required for the growth of GaN-on-Si vertical structures that should complement the fabrication as well. To realize such GaN-on-Si vertical device, (i) the doping density ($N_d$-$N_a$) in the drift region must be controlled and (ii) the buffer layer should be conductive. Figure 2 represents the net $N_d$-$N_a$ in the drift region as a function of $SiH_4$ flow rate for a GaN-on-Si grown with two SLS thicknesses. As shown, the $N_d$-$N_a$ could be controlled for GaN-on-Si by increasing the SLS multipairs, which is due to the reduction of dislocation density. The conductive buffer layers including the AlGaN/AlN layers and SLS are indispensable for realizing GaN-on-Si vertical devices. Therefore, a Si-doped AlN NL as thin as 3 nm was initially deposited followed by the deposition of Si-doped AlGaN and SLS. This novel fully vertical GaN-on-Si p-n diode comprises of doped buffer layers and not involve substrate removal technology. This GaN-on-Si p-n diode has ohmic contacts on the p-GaN layer and backside of n+-Si substrate, that showed a turn-on voltage of 3.4 V and a breakdown voltage of 288 V for the 1.5-µm-thick $n^-$-GaN drift layer [10]. The BV can be further improved by increasing the buffer thickness and/or by using field plate structures. These improvements in the MOCVD growth of GaN-on-Si vertical structures suggest their potential role in power electronics in near future.

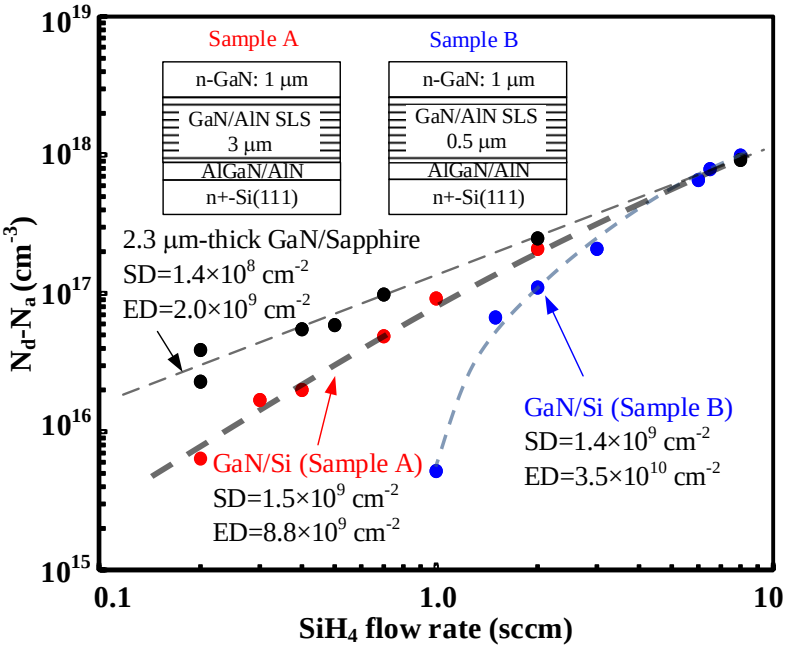

**Figure 2.** Net doping concentration as a function of $SiH_4$ flow rate for GaN-on-Si with different SLS thickness. For comparison, the data of GaN/sapphire are also shown. Copyright (2016) The Japan Society of Applied Physics, reprinted with permission from Ref. 10.

## Concluding Remarks

The GaN-on-Si power devices are emerging to play a dominant role in the next-generation power electronics. Significant improvements in the hetero epitaxial growth and device fabrication are indispensable for the commercialization of these power devices. For the epitaxial growth of GaN-on-Si lateral devices, we have utilized the high temperature AlN NL to prevent the melt back etching of Ga into Si. It was also found that the growth of SLS is essential to control the wafer bowing for GaN-on-Si. In addition, the growth of SLS multipairs effectively enhanced the breakdown voltage of GaN-on-Si HEMTs. On the other hand, fully-vertical GaN-on-Si p-n diodes were demonstrated by using conductive buffer layers. We have used AlN NL as thin as 3 nm and SLS multipairs, both highly doped in order to realize fully-vertical GaN-on-Si p-n diodes. These advancements in the MOCVD growth of GaN-on-Si and device fabrication processes will lead to the high-performance power electronics.

## Acknowledgement

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# 6 – Vertical GaN Power Devices

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**Status**

Central to improving the efficiency of power electronics is the availability of low-cost, efficient and reliable power switching devices. GaN-based devices are exciting candidates for next-generation power electronics. Currently, both lateral and vertical structures are considered for GaN power devices. Vertical GaN power devices have attracted significant attention recently, due to the capability of achieving high breakdown voltage (*BV*) and current levels without enlarging the chip size, the superior reliability gained by moving the peak electric field away from the surface into bulk devices, and the easier thermal management than lateral devices [1].

Since 2010, the field of vertical GaN power devices has grown exponentially and seen numerous demonstrations of vertical diodes and transistors (figure 1). A 3.7 kV vertical GaN pn diode [2] and a 1.1 kV vertical GaN Schottky barrier diode (SBD) [3] have recently showed near-theoretical power figure of merit. Trench metal-insulator-semiconductor barrier Schottky diodes [4] (figure 2(a)) and junction barrier Schottky diodes [5] (figure 2(b)) have also been proposed to combine the good forward characteristics of SBDs (e.g. low turn-on voltage) and reverse characteristics of pn diodes (e.g. low leakage current and high *BV*).

Several structures have been proposed for vertical GaN transistors, with the highest *BV* close to 2 kV. Current aperture vertical electron transistor (CAVET) combines the high conductivity of a two-dimensional electron gas (2DEG) channel at the AlGaN/GaN heterojunction and the improved field distribution of a vertical structure [6] (figure 2(c)). The CAVET is intrinsically normally-on, but a trench semi-polar gate could allow for normally-off operation [7] (figure 2(d)). Vertical GaN trench MOSFETs have no 2DEG channels, but do not need the regrowth of AlGaN/GaN structures and are intrinsically normally-off [8] (figure 2 (e)). Recently, vertical fin MOSFETs have been demonstrated to achieve normally-off operation without the need for p-type GaN materials or epitaxial regrowth [9] (figure 2(f)).

While most vertical devices utilize expensive GaN substrates, it is also feasible to make vertical GaN devices on low-cost Si substrates. Quasi- and fully-vertical GaN-on-Si vertical diodes have been demonstrated with a *BV* over 500 V and excellent high-temperature performance [10]. These devices can enable 100-fold lower substrate and epitaxial cost than GaN-on-GaN vertical devices.

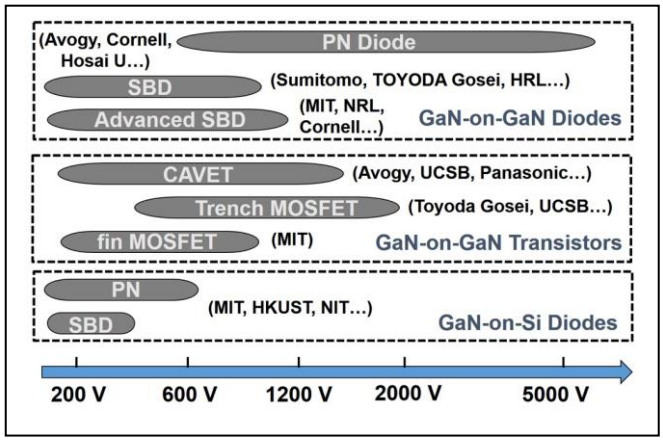


**Figure 1.** Overview of the main device types and voltage classes for the vertical GaN power devices reported in recent years.

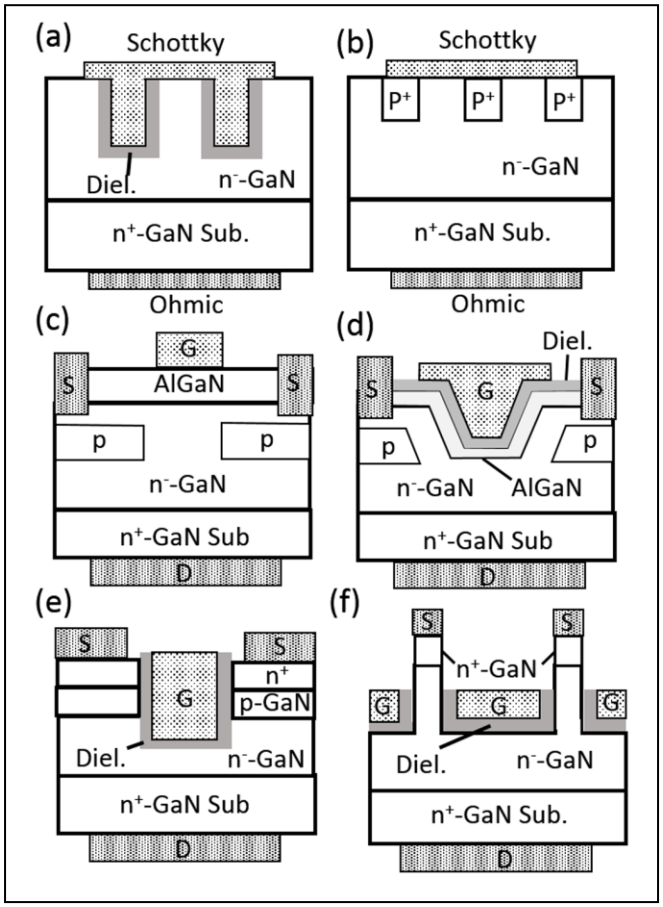


Figure 2. Schematic of representative vertical GaN advanced Schottky barrier diodes and vertical GaN transistors: (a) trench MIS barrier Schottky diode, (b) junction barrier Schottky diode, (c) CAVET, (d) trench CAVET, (e) trench MOSFET and (f) vertical fin MOSFET. In this Figure, "Diel." stands for dielectrics, and "Sub." for substrates.

**Current and Future Challenges**

In spite of the great progress, the full potential of vertical GaN SBDs and transistors has not been exploited yet. The *BV* demonstrated in these devices, with no avalanche capability reported, is still much lower than the avalanche *BV* in vertical GaN pn diodes. The lack of avalanche capability would greatly compromise the device robustness when operating in inductive switching environments. Although the nature of avalanche breakdown is still not fully understood in GaN devices, a key factor is believed to be good edge termination technologies and a way to remove holes from the structure. In SiC power devices, successful edge termination technologies, such as junction termination extension and field rings, was enabled by selective p-type doping. However, in GaN devices, the current selective area doping or selective area epitaxial regrowth technologies cannot yield material of sufficiently high quality to enable defect-free patterned lateral pn diodes. In particular, p-type implantation and activation in GaN is far from mature. With complicated activation annealing schemes, the activation ratio for acceptors is typically below 5%, resulting in very low concentration and mobility for the activated free holes [5].

There remain open questions on the selection of carrier channels in vertical GaN transistors to improve the device forward characteristics. The ideal channel for these devices would have normally-off configuration with high carrier mobility and without the need for epitaxial re-growth. Further work is needed for all the three channels reported so far, 2DEG channel [6], MOS inversion layer [8] and bulk fin channel [9].

The commercialization of vertical GaN power devices has been hindered by the high cost of bulk GaN substrates. The mainstream GaN substrates are 2-inch, while 4- and 6-inch GaN substrates are available very recently in small volumes. The wafer cost (per area) for 2-inch GaN-on-GaN is \$60~\$100/cm$^2$, still much higher than the cost for 4-inch SiC (~\$8/cm$^2$) and 8-inch GaN-on-Si (~\$1/cm$^2$). The fundamental challenge is how to achieve the material quality associated with free-standing GaN substrates, while allowing the devices to be transferred to alternate substrates and have the GaN substrates re-used to reduce cost.

**Advances in Science and Technology to Meet Challenges**

Different technological solutions can be envisioned to address the challenges in making patterned lateral pn junctions for edge termination structures. For example, compared to p-type ion implantation, n-type ion implantation (e.g. Si, N, etc.) and activation is much easier. Lightly-doped p-GaN edge terminations has been then demonstrated by implanting donors to compensate highly-doped p-GaN layers in vertical GaN pn diodes [2]. Patterned pn junctions have also been reported by n-type ion implantation into epitaxially grown p-GaN regions [5]. Besides selective ion implantation, the patterned pn junctions can be also made by selective p-GaN regrowth to fill n-GaN trenches. The initial feasibility of this approach has been demonstrated in CAVET [6], although much more work is needed to study the regrown interface quality and passivate parasitic leakage currents.

In parallel, different electrical, mechanical and chemical techniques are under development to enable devices to be lifted off from native GaN substrates and transferred to low-cost substrates. Successful layer transfer technology, combined with patterned interconnections on the supporting substrate and re-use of GaN substrates, should greatly reduce the cost and pave the way to commercialize high-performance vertical GaN power devices.

Another approach that can fundamentally circumvent the cost issue of vertical GaN devices is to fabricate them on Si substrates, which could allow for almost 100-fold lower wafer and epitaxial cost as well as 8-inch fabrication. Recently, GaN-on-Si vertical pn diodes with blocking capability of 500-600 V have been demonstrated [10]. Fully-vertical GaN-on-Si power devices have also been demonstrated by different technologies, such as layer transfer, conductive buffer layer, and selective removal of the substrate and buffer layer. To improve the performance of these devices, advances in epitaxial growth technology are needed to enable thicker GaN layers with very low background carrier concentration (< $10^{16}$ cm$^{-3}$) on Si substrate.

**Concluding Remarks**

Vertical GaN devices are key to achieve the high currents (> 100 A) and voltages (> 600 V) required by many power applications, such as electric vehicles and renewable energy processing. Record performance near the theoretical Baliga figure of merit has been demonstrated in vertical GaN pn diodes, although more work is needed in vertical Schottky barrier diodes and transistors. Exciting research opportunities exist in the field, especially in making patterned pn junctions, recycling GaN substrates and developing vertical GaN devices on Si substrates.

**Acknowledgements**

The authors gratefully acknowledge the funding support by the ARPA-E SWITCHES program monitored by Dr. T. Heidel and Dr. I. Kizilyalli, and tby the ONR PECASE program monitored by Dr. Paul Maki.

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# 7 – GaN Insulated Gate Field-Effect Transistors

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**Status**

GaN-based insulated gate field-effect transistors with an insulating gate dielectric provide many desirable properties such as suppressed gate leakage and large gate voltage swing [1]. These devices are typically in the form of metal-insulator-semiconductor HEMT (MIS-HEMT) or MIS-FET with the insulating dielectric on a heterojunction (e.g. AlGaN/GaN) channel or a GaN channel, respectively, as illustrated in Fig. 1(a) and (b). The MIS-HEMT was first studied for RF/microwave power amplifier applications [2], and then intensively investigated as a promising power switching device. The MIS-gate transistors are especially attractive to high-frequency power switching applications because they can better tolerate gate voltage over-shoot that often occurs in circuits with high slew rate.

As is the case of Si- and SiC-based MOSFETs, the gate dielectric in GaN insulated gate FETs is required to deliver a dielectric/III-nitride interface with low trap density, high reliability and long lifetime under various stresses (e.g. electrical, thermal, humidity, etc.). GaN MIS-HEMTs typically exhibit depletion-mode (D-mode) operation with a large negative threshold voltage ($V_{th}$) because of the presence of high-density positive polarization charges in the barrier layer (e.g. AlGaN). The D-mode MIS-HEMT, with its gate (input) terminal seldom forward biased during circuit operation, typically exhibit less adverse effects from the gate dielectric. This is mainly due to the presence of the barrier layer that decouples the 2DEG channel from the interface/border traps in the dielectric as long as the "spill-over" of electrons toward the dielectric does not occur, leading to small $V_{th}$ hysteresis. Very good gate reliability [3] has been obtained in D-mode MIS-HEMTs featuring a thin gate dielectric layer ($SiO_2$, $Si_3N_4$ or high-κ dielectrics) under relatively small forward gate bias.

Enhancement-mode (E-mode) MIS-HEMTs and MIS-FETs with a positive $V_{th}$ are highly desirable from the circuit application point of view for their simpler gate control circuitry and fail-safe operation. To fully turn on the channel current, however, large positive forward gate needs to be applied. This is when the gate dielectric is under the most demanding operational conditions (e.g. high electric field, charge injection to the dielectric and carriers leaking through the dielectric). $V_{th}$-instability (both static and dynamic) at different temperature and bias stress conditions, and its impact on dynamic on-resistance ($R_{ON}$) need to be systematically studied and clearly understood [4, 5]. The time-dependent dielectric breakdown (TDDB) is the ultimate hurdle to overcome before commercialization of E-mode GaN-based MIS-HEMTs and MIS-FETs.

**Current and Future Challenges**

Trap states at the dielectric/III-nitride interface and inside the dielectric present the biggest challenges to GaN MIS-HEMTs and MIS-FETs [6]. With a wide bandgap in GaN, a large energy window is available to accommodate interface and bulk trap states at shallow and deep energy levels with short and long emission time constant $\tau_{it}$. The dynamic charging/discharging processes of these traps could lead to $V_{TH}$ instability during a switching operation, and consequently affect circuit and system stability.

Unlike Si on which highly uniform and highly reliable thermal oxide can be prepared using high-temperature (800 °C ~ 1200 °C) furnaces, GaN surface becomes unstable when the ambient temperature exceeds 800 °C. In addition, the Ga-O bonds at an oxide/III-nitride interface fundamentally induce high-density gap states, except in a few very specific crystalline oxide

configurations, according to a first-principles calculation study [7]. Thus, removing the detrimental Ga-O bonds at the GaN surface is a critical step for obtaining low interface trap density ($D_{it}$). If oxide-based gate dielectric is to be used for their high dielectric constant and large bandgap, a non-oxide (e.g. nitride-based) interfacial layer would be highly desirable.

Although there are many reports on E-mode GaN MIS-HEMTs and MIS-FETs in research literature, the commercialization of these devices has been hindered by concerns over the gate dielectric reliability. The commonly used gate dielectric (SiN, $SiO_2$ and $Al_2O_3$) is deposited by PECVD or ALD (atomic layer deposition) at relatively low temperature (at 300~400 $^oC$). While the low temperature helps maintain GaN surface morphology, it is also the main reason for high-density defects in the dielectric, making it difficult for these devices to pass reliability tests and qualifications. High-temperature annealing only shows moderate effect on enhancing the dielectric reliability. Thus, it is of critical importance to develop high-temperature gate dielectric films (e.g.~ 800 $^oC$ or above) with lower defect density and longer TDDB lifetime. The biggest challenge to high-temperature dielectric on GaN is the degradation (via decomposition or chemical reaction) of GaN surface at high temperatures. A possible solution could feature a low-temperature interface protection layer and high-temperature gate dielectric.

**Advances in Science and Technology to Meet Challenges**

The first D-mode GaN MIS-HEMT was demonstrated using PECVD-$SiO_2$ as the gate dielectric [2]. With MOCVD-grown in-situ $SiN_x$ as the gate dielectric, low $D_{it}$ and excellent gate reliability are obtained [3]. At 10 years, for a 100ppm failure rate, a $V_{gs\_max}$ of ~3.1V is extracted, which is well above the operating $V_{gs}$ for a D-mode MIS-HEMT ($V_{gs\_max}$=0V).

The first E-mode GaN MIS-HEMT was demonstrated using PECVD-$SiN_x$ deposited on fluorine-implanted AlGaN/GaN heterojunction [8]. Low-damage and well-controlled dry and digital etching techniques are being developed to obtain positive threshold voltage. E-mode partially recessed MIS-HEMTs and fully MIS-FETs have both been developed with low on-resistance, high saturation current, small $V_{th}$ hysteresis and low dynamic on-resistance. In particular, *in-situ* removal of native oxide and consequent nitridation by low-power plasma (as illustrated in Fig. 1 (c)) prior to dielectric deposition [9] are important techniques for producing high-quality dielectric/GaN interface by passivating the dangling bonds while introducing minimum gap states.

To achieve high gate dielectric reliability under large positive gate bias required for E-mode insulated gate FETs, $SiN_x$ deposited by LPCVD (low-pressure chemical vapor deposition) has emerged as a compelling candidate as it possesses several important benefits including large conduction band offset with GaN ($\Delta E_c$ ~ 2.3 eV), relatively high dielectric constant ($\kappa$ ~ 7) and especially the long TDDB lifetime as a result of the low defect density achieved at high deposition temperature (e.g. 780 $^oC$). Implementing the LPCVD-$SiN_x$ gate dielectric in recessed-gate E-mode MIS-HEMTs and MIS-FETs has been more challenging since an etched GaN surface suffers more severe degradation than an as-grown GaN surface at high temperatures. An effective approach to suppressing such a degradation while maintaining low $D_{it}$ ($10^{11}$~$10^{12}$ $cm^{-2}$ $eV^{-1}$) has been developed using a low-temperature PECVD-$SiN_x$ thin film as an interfacial protection layer [10], as depicted in Fig. 2. For a 10-year lifetime, the maximum gate bias is determined to be 11 V at a failure rate of 63.2 % and 9.1 V at a failure rate of 0.01%.

**Concluding Remarks**

There is strong demand for GaN insulated gate field-effect transistors with both depletion- and enhancement-mode operations, as the insulated gate provides strong immunity to control voltage spikes and could be driven with circuits very similar to those used for the mainstream Si and SiC power MOSFETs. The most critical need of a GaN insulated gate FET technology is a gate dielectric technique that simultaneously delivers low interface/bulk trap density and robust reliability under stringent

electrical and thermal stresses. The E-mode GaN MIS-HEMTs and MIS-FETs are especially challenging as they operate under large positive gate bias and the recessed-etched GaN demands better protections during high temperature process associated with high-quality dielectric deposition. Combining low-temperature interfacial layer with high-temperature gate dielectric could be a promising pathway toward reliable and stable GaN insulated gate FETs.

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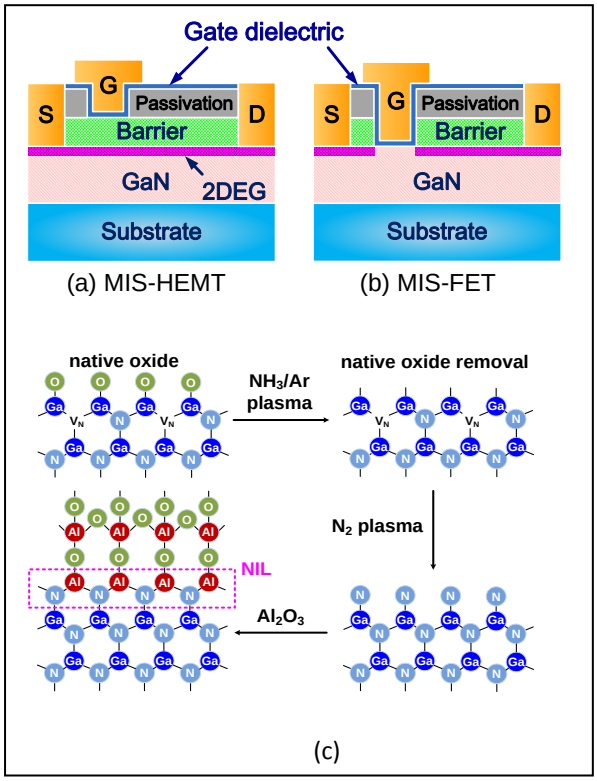


**Figure 1.** Schematic cross sections of GaN-based (a) MIS-HEMT and (b) MIS-FET. (c) Schematic process for *in-situ* native oxide removal and surface nitridation of GaN.

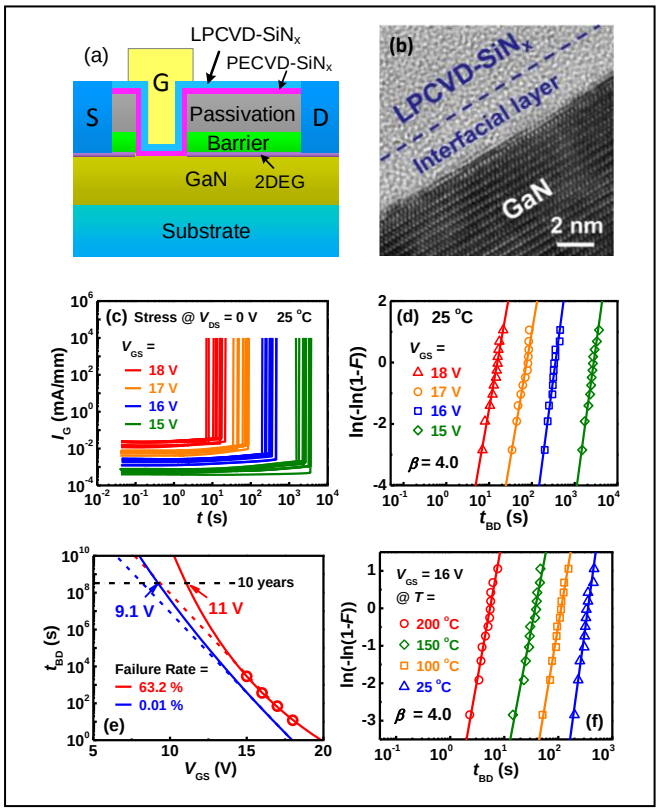


**Figure 2.** (a) Schmematic cross section of an E-mode fully recessed GaN MIS-FET with interfacial protection layer. (b) High-resolution TEM of an LPCVD-$SiN_x$/PECVD-$SiN_x$/GaN interface. (c) Time to breakdown ($t_{BD}$) of the LPCVD-$SiN_x$ MIS-FETs with interfacial protection layer at forward gate stress of 18, 17, 16 and 15 V at 25 °C. (d) Weibull plot of the electric field-dependent $t_{BD}$ distribution. (e) Lifetime prediction with a failure rate of 63.2 % and 0.01 %, respectively. (f) Weibull plot of the temperature-dependent $t_{BD}$ distribution.

# 8 - Reliability of GaN Power Devices: Normally-on and Normally-off

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**Status**

Reliability is essential for the application of GaN power devices to critical electronic systems, for high-voltage energy conversion, control of electrical engines, automotive electronics [1]. GaN is a robust material, capable of withstanding extremely high electric field and temperature; in order to fully exploit its potential, deep levels effects and failure mechanisms induced by high voltage and high temperature stress must be known in detail.

Several technological options are available for the fabrication of GaN power high electron mobility transistors (HEMTs): Schottky-gate normally-off transistors, which have the simplest structure, are prone to higher leakage current with respect to their insulated-gate counterpart; nevertheless they can reach breakdown voltages higher than 1100 V and can achieve normally-off operation in conjunction with a Si MOS driver in cascode configuration [2]. Normally-off devices can be achieved using p-type AlGaN or GaN with high acceptor doping on top of the AlGaN [3]. Recessed-gate metal-insulator-semiconductor devices (MISHEMT) enable operation at positive gate bias without measurable gate current $I_G$ [4]. Normally-off operation can be achieved by decreasing the thickness of the AlGaN layer under the gate in a recessed structure.

The different structures can be affected by specific failure mechanisms. When biased in off-state at high reverse bias, Schottky-gate, normally-on HEMT were subject to a significant and progressive increase of gate leakage current (several orders of magnitude), correlated with the onset of leakage current paths which can be detected by electroluminescence (EL) [5]. Further analysis revealed that this catastrophic increase of $I_G$ was time dependent, that time to failure depended on the electric field, followed a Weibull distribution, and decreased slightly with temperature (activation energy = 0.12 eV). $I_G$ increase was attribute to the formation of a conductive percolation path across defects [5]. This concept of GaN as a “lossy dielectric” was a major breakthrough for GaN reliability: it allowed the extrapolation of device lifetime using standard time-dependent dielectric breakdown (TDDB) tests, and promoted the study of other GaN time-dependent failure mechanisms, described in the following.

**Current and Future Challenges**

Time dependent breakdown effects in Schottky gate devices were due to different physical mechanisms either related to device design or materials quality: (i) in normally-on power Schottky HEMTs with double field-plate, TDDB was found to be due to the failure of the insulating SiN layer between the two-dimensional electron gas (2DEG) and the first field-plate edge. Increased robustness was achieved by changing the substrate conductivity in order to move the 2DEG edge towards the drain [2]; (ii) in AlGaN/GaN power Schottky diodes, breakdown involved first the dielectric at the diode edge and then the AlGaN; as a consequence, lifetime improves by adopting either a thicker plasma-enhanced atomic layer deposition (PEALD) SiN edge-termination dielectric (from 15 nm to 25 nm) or

a more robust one (25 nm in-situ SiN) [6]; (iii) drain-source off-state catastrophic breakdown of n-on Schottky gate HEMTs, may occur as a consequence of hole trapping and accumulation at the source edge of the gate: trapped positive charge shifts threshold voltage towards negative values and turns on the device while a high drain voltage is applied, thus resulting in device burn-out [7].

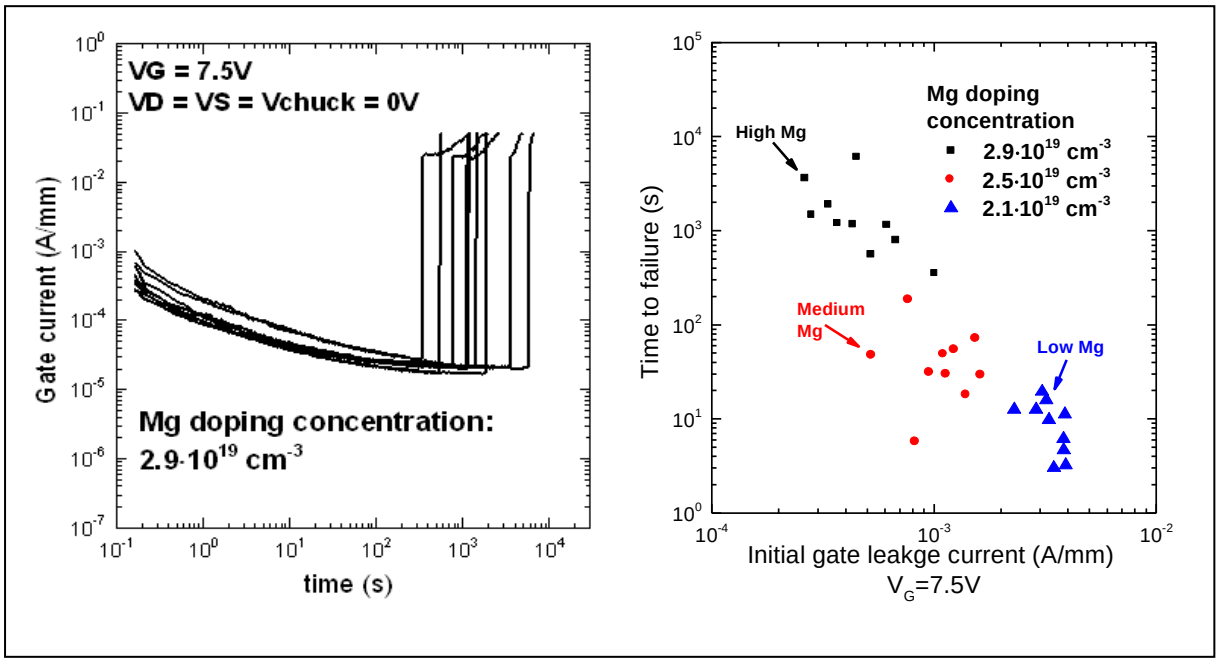


**Figure 1.** Left: Time-dependent breakdown experiment on the p-gate of a normally-off GaN HEMT; Right: dependence of time to failure on initial gate leakage current at $V_G$ = 7.5 V (and consequently on p-type doping concentration in the p-GaN layer [8]. Reprinted from Microelectronics Reliability, Vol 76-77, I. Rossetto, M. Meneghini, E. Canato, M. Barbato, S. Stoffels, N.Posthuma, S. Decoutere, A.N. Tallarico, G. Meneghesso, E. Zanoni, "Field- and current-driven degradation of GaN-based power HEMTs with p-GaN gate: Dependence on Mg-doping level", Pages No. 298-303, Copyright 2017, with permission from Elsevier.

P-gate devices (either with an ohmic or a Schottky metal contact on top of the p-layer) are currently the most popular choice for n-off devices. A critical mechanism for p-gate HEMTs is the TDDB consequent to the application of a positive gate bias. In the case of a rectifying contact on p, positive bias leads to increased electric field, potentially leading to breakdown. Time to failure decreases at increasing gate leakage current and consequently at higher temperature ($E_a$ = 0.5 eV); times to failure are Weibull-distributed. Higher Mg doping in the p-layer reduces leakage current and therefore improves lifetime. A possible explanation consists in the accumulation of positive charge at the interface with the AlGaN, proportional to leakage current which, at its turn, enhances gate current and promotes further degradation. A second hypothesis implies the formation of a percolation path, consequent to defects formation due to hot carriers (collected by the gate). In this case also, times to failure are Weibull-distributed; a 20-years lifetime at $V_{GS}$ = +7.2 V was demonstrated for a 200 V n-off technology [3].

The vertical drain-substrate stack is also sustaining a high electric field and is prone to time-dependent breakdown: a 200 V n-off technology was submitted to tests at $V_{D\text{-substrate}}$ in excess of 700 V and failed due to vertical burnout in approximately 2 X $10^4$ s. Higher leakage current and temperature correspond to shorter lifetime, with a decrease which is thermally activated with a 0.25 eV activation energy. The maximum applicable voltage for a lifetime of 20 years with 1% failure rate is about 560 V at RT, considerably higher than the operating voltage [9].

The GaN MISHEMT represents an ideal structure for normally-off power GaN electron devices since the dielectric layer reduces significantly the gate leakage; unfortunately the MIS structure introduces new reliability problems, related with the stability of device threshold voltage. Large positive $V_{th}$ shifts (positive bias temperature instabilities) have been observed under forward gate bias conditions and attributed to accumulation of electrons at the dielectric/III-N interface where a second electron channel forms in the so-called "spill-over" conditions [10]. According to [10], the density of interface states of any dielectric is currently high enough to completely deplete the 2DEG channel with a typical electron density in the order of $10^{13}$ $cm^{-2}$. Improvements therefore require either a reduction of interface states or an increase of the voltage required to induce the "spill-over".

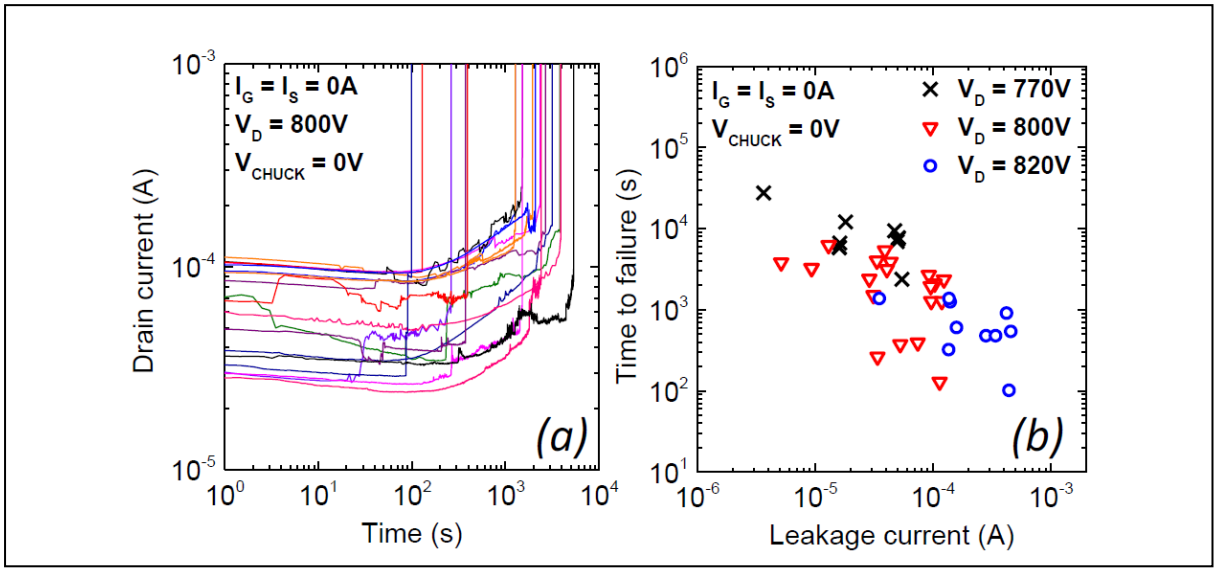


Figure 2. (a): time-dependent breakdown test on drain current at $V_{DS}$ = 800 V. Data refer to normally-off p-GaN gate devices at RT. (b): time to failure dependence on the initial leakage for three drain bias levels applied during the constant voltage stress [9]. Reprinted with permission from: Matteo Borga, Matteo Meneghini, Isabella Rossetto, Steve Stoffels, Niels Posthuma, Marleen Van Hove, Denis Marcon, Stefaan Decoutere, Gaudenzio Meneghesso, and Enrico Zanoni, "Evidence of Time-Dependent Vertical Breakdown in GaN-on-Si HEMTs", Transaction on Electron Devices, vol. 64 no. 9, pp. 3616-3621, September 2017. © IEEE 2017

Negative voltage shift (NBTI), observed when negative voltage is applied to the gate is usually less severe, and becomes relevant only at high temperature (activation energy 0.37 eV, see [4] and reference therein). According to [4], NBTI is due to detrapping of states at the SiN/AlGaN interface; authors in [11] have formulated a unified model for positive bias temperature instability (PBTI) and NBTI, which implies electron trapping/detrapping in pre-existing oxide traps that form a defect band very close to the GaN/insulator interface. NBTI can reduce the threshold voltage of n-off devices, thus thinning the safety margin in off-state. Conversely, NBTI does not represent a critical problem for n-on devices: under cascode operation, the on/off state is controlled by the Si MOSFET; moreover, due to the leakage current of the Si MOSFET, the HEMT is always in slight semi-on state, and this limits the electric field across the SiN/AlGaN stack.

**Advances in Science and Technology to Meet Challenges**

Schottky-gate and MISHEMT n-on devices for cascode configuration and p-gate n-off devices are gaining maturity; time-dependent breakdown effects can be evaluated using standard, well-established testing methods; methods for long-term thermal stability assessment still have to be developed and consolidated into standards. Some issues remain, concerning gate leakage, hot

electron degradation, instantaneous breakdown. Since the electric field plays a key role in the reported degradations and failures, it is important to develop solutions in order to reduce its impact on the reliability issues. The regions/interfaces where the electric field reaches its maximum value often represent the weakest point of the device due to several effects: (i) the inverse piezoelectric effect could bring to a catastrophic failure due to the lattice damage; (ii) hot electrons gain energy thanks to the high electric field in the pinch-off region; (iii) it has been shown that the p-gate failures are related to the electric field peak along the gate edge. Both preventing the building up of high electric field and growing high quality materials that can withstand the electrical stress are ways to improve the reliability of the devices. The quality of the passivation layer has been shown to be crucial to improve both the lifetime and the robustness, and the optimization of the materials quality is needed.

Also, the process is important and could be improved, since the etching treatment could damage the passivation layer at the gate edge, exactly where the electric field peaks in a forward gate bias condition.

Concerning n-off MISHEMTs, stabilization of threshold voltage remains an open issue, which requires in-depth physical characterization of surface and interface properties and of dielectric materials.

Since one of the targets is to increase the operating voltage over 1000V, it is important to focus on the drain-to-substrate stack. In order to reduce the vertical leakage, the transition layers must be optimized and engineered, avoiding the defects to behave like conductive paths between the silicon substrate and the drain. It is worth noticing that these paths are the starting point which leads to the formation of the conductive percolation path leading to a TDDB behavior. Nevertheless, electric field peaks within the structure can also lead to reliability issues; smoothing the electric field at the hetero-interfaces will results in a higher breakdown voltage of the vertical stack. In particular, it has been shown that this type of failure occurs within the silicon (substrate), which is the material with the lower breakdown field. A possible solution that increases considerably the breakdown voltage of the vertical stack consists in the removal of the silicon substrate removal, which, however, involves some processing complications.

## Concluding Remarks

This chapter has reviewed reliability of n-on and n-off GaN power HEMTs, with particular emphasis on time-dependent breakdown mechanisms and NBTI/PBTI effects. Results described here have been obtained by means of on-wafer short-term (<100 h) tests. Knowledge on the long-term reliability of these devices is being developed only recently, thanks also to cooperative projects such as POWERBASE and InRel-Npower, which promise to achieve full maturity for GaN power technologies in the 650 – 1200 V range.

## Acknowledgements

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# 9 – Plasma Processing for GaN Power Electronic Devices

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**Status**

To significantly impact the marketplace of energy efficient power switching, GaN-based transistors must be produced in high volumes at low cost. Adopting silicon-based substrates and silicon-like manufacturing approaches enables production using legacy 150 mm and 200 mm wafer facilities driving cost efficiencies. Standard silicon manufacturing approaches rely heavily on plasma processing for etching semiconductors and deposition of dielectrics and metals. These procedures need to be migrated to GaN-based materials and optimised to minimise process induced damage of the semiconductor layers. These can present as reductions in channel carrier concentration and mobility and therefore increased on-resistance; and hysteretic effects due to the formation of charge trapping states which can influence dynamic response.

As shown in Figure 1(a), there are three areas where plasma processing as part of device manufacture can have a significant effect.

1 – in the source-drain regions, controlled etching into the semiconductor to the same relative position compared to the device channel offers a generic solution as described in [1] irrespective of the thickness of the AlGaN barrier layer of the device.

2 – in the gate-drain region, effective passivation of the semiconductor surface is vital to minimise leakage current and current collapse. A variety of dielectrics are being actively used and demonstrated encouraging performance [2], [3] with further work required to fully understand the interaction between the dielectric and the semiconductor.

3 – in the gate stack, a dielectric introduced between the gate metal and the semiconductor (Figure 1(b)) can suppress gate leakage current. Subjecting the semiconductor to a fluorine plasma (Figure 1(c)) has been shown to be effective in shifting positive the device threshold voltage [4], important for normally-off device operation. There can be issues with long term reliability of this approach however. An alternate is to perform a gate recess etch prior to gate dielectric and metal deposition (Figure 1(d)) – controlling the etch depth to control threshold voltage requires the use of low damage plasma based atomic layer etching approaches, such as those described in [5]. Wafer scale and wafer to wafer uniformity of these etching approaches still need to be confirmed.

**Current and Future Challenges**

*Plasma Processing in the Source-Drain Region*

As reported in [1] and [6], plasma etching of the semiconductor layers in the source-drain region before contact metal deposition results in reduced contact resistance (0.18 Ohm mm was obtained in [6] using "patterned" $Cl_2$-based plasma etching), and reduced thermal budget (contact resistance of 0.5 Ohm mm was achieved in [1] at a contact anneal temperature of 550 $^oC$ using a $SiCl_4$-based chemistry). Driving down the thermal budget to below 500$^oC$ opens new opportunities for "gate first" approaches to device realisation which may be important in improving the stability of the gate/semiconductor interface.

*Plasma Processing in the Gate-Drain Region*

As described in [2], passivation of the gate-drain region using low pressure chemical vapour deposition (LPCVD) of $SiN_x$ with optimal conditions had a strong effect on both current collapse and

leakage currents. This is a high temperature (850 $^{o}$C) process. A key property of the LPCVD-SiNx films in this study was the stress. Recently, the use of stress control in room temperature deposited inductively coupled plasma-CVD (ICP-CVD) $SiN_x$ films for surface passivation was also shown to reduce significantly leakage currents [3], therefore a key challenge at this time is to understand the underlying physical mechanisms that govern the leakage current and current collapse phenomena.

*Plasma Processing in the Gate Stack*

As mentioned above, the incorporation of a gate dielectric is important to reducing the gate leakage current in GaN transistors and allows for a larger gate voltage swing, which is particularly important for normally-off devices. As reported in [7], controlling the properties of the GaN surface, in this case by removing a SiN capping layer deposited as the final stage of the wafer growth using an $SF_6$ plasma etch immediately prior to atomic layer deposition of an $Al_2O_3$, resulted in a 4x reduction in hysteresis to 60 mV for GaN MOS-capacitors. This work also reported the impact of the introduction of TiN into the gate stack, which resulted in a 35% increase in accumulation capacitance. Understanding of the origin of these effects will be vital to further device optimisation.

**Advances in Science and Technology to Meet Challenges**

Understanding the role and impact of plasma-based processing will be vital to further optimising and improving the efficiency of GaN power device operation in terms of static and dynamic on-resistance, current collapse, leakage currents and threshold voltage control. Control of the semiconductor surface, both mechanically and chemically is a key. This can best be addressed by understanding and correlating the properties of the semiconductor surface and its interface with dielectrics and/or metals with transistor performance. Combining plasma processing equipment so that an etched wafer can be transferred directly into a dielectric or metal deposition tool is an important technological advance. This “clustered” approach to wafer processing is relatively standard in the mainstream silicon industry – research needs to be undertaken to validate such approaches for GaN-based materials and devices for power electronics applications. A cluster tool such as that shown in Figure 2 is already proving highly insightful in this regard. In addition to combined process chambers, the cluster tool shown in Figure 2 also has in-situ scanning Auger capability. Clustered plasma process and metrology engines are going to be the key to unlocking the full potential of plasma processing for GaN power electronics.

**Concluding Remarks**

Plasma processing is a vital element in the manufacture of GaN power electronics as, based on its use in the mainstream silicon industry, only plasma processing offers reproducible wafer scale and wafer to wafer etching and dielectric and metal deposition. Arguably, the GaN surface is one of the most process sensitive in the electronics industry, so its control at a chemical level is key to fully optimising device performance. Having a profound and fundamental understanding of the impact of plasma processing on the GaN surface is therefore an imperative to ultimate GaN power device realisation.

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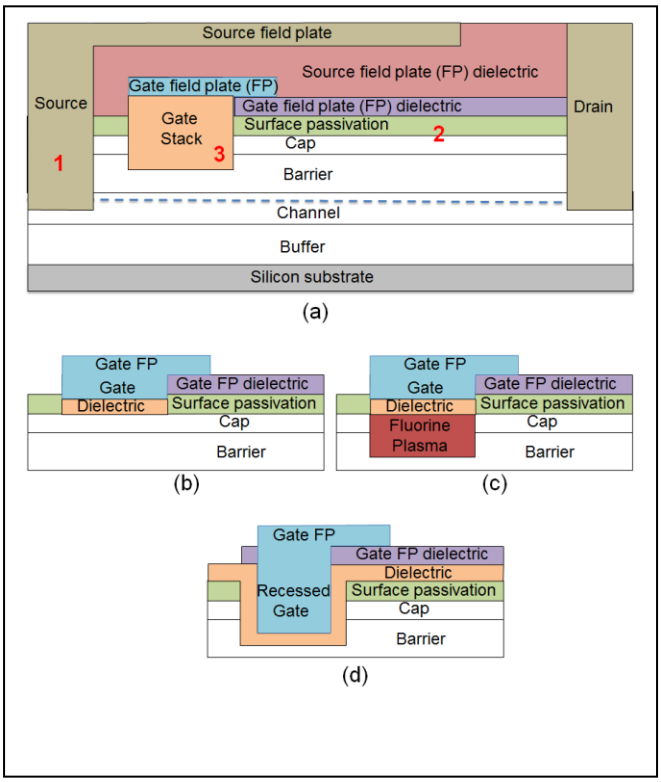


**Figure 1.** (a) Schematic of a generic GaN-on-silicon power transistor. Key areas for device optimisation using plasma processing are **1** – recessed ohmic contacts for low resistance, high field compatible source-drain contacts ; **2** – the gate-drain region to mitigate leakage current and dynamic on-resistance issues; **3** – the gate stack to control threshold voltage and minimise gate leakage current with minimal hysteretic effects. (b), (c) and (d) are specific gate stack solutions. (b) has a gate dielectric deposited on the GaN surface; (c) has a gate dielectric above a fluorine plasma treated region to tune threshold voltage; (d) has a recessed gate prior to dielectric deposition

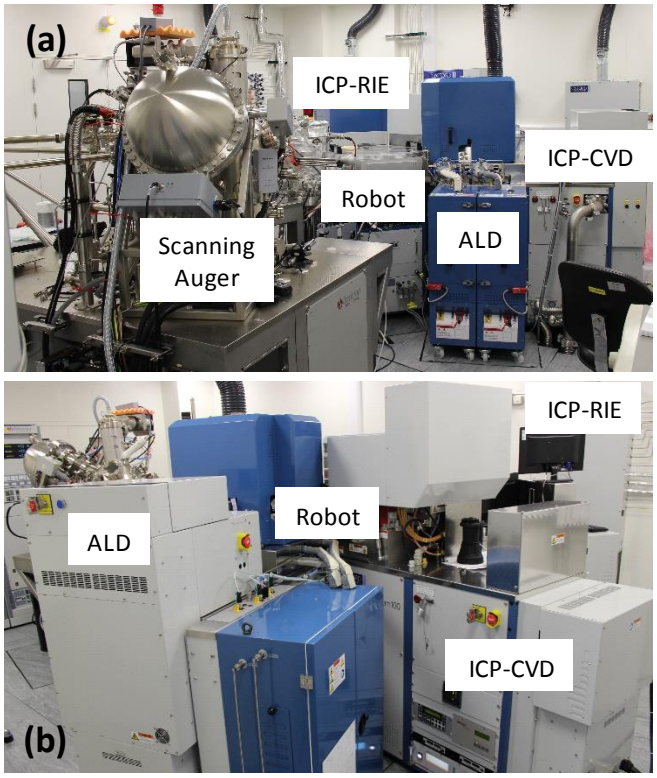


Figure 2. Views of clustered plasma process chambers. A central robot handler allows movements of wafers between reactive ion etch, atomic layer deposition and chemical vapour deposition chambers without atmospheric exposure. Also clustered is a scanning Auger microscope to enable in-situ mid-process surface analysis.

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# 10 - Challenges to dielectric processing for E-mode GaN

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**Status**

The growth of ultrathin dielectric layers into GaN-based devices incorporating metal-insulator-semiconductor (MIS) structures has been extensively investigated as a method of minimising gate leakage currents, which are lost through the gate by electron tunnelling, leading to poorer power efficiency and electrical noise. For normally-off, enhancement mode devices, low off- currents are necessary to reduce the static power consumption and ensure fail-safe operation. The incorporation of various oxide or nitride dielectric materials into GaN-based heterostructures has been explored previously using a range of conversion (e.g. oxidation or wet chemical methods) and chemical (e.g. CVD or ALD) or physical vapour (e.g. sputtering or evaporation) growth processes. Regardless of the dielectric or fabrication process used, the discontinuity (see figure 1) at the resulting insulator-semiconductor interface gives rise to electrically active interface trap states. These can influence device performance, by acting as remote impurity scattering centres that can either lower the carrier mobility ($\mu$) [1] or influence the threshold voltage ($V_{th}$) [2]. The insulator itself may also contain deleterious intrinsic charge traps. Furthermore, the insulator will have valence band and conduction band offsets with respect to the III-nitride (e.g. GaN, AlGaN, InAlN etc) which will influence the carrier confinement properties in the semiconductor [3]. Despite these issues, both depletion-mode and enhancement-mode insulated-gate GaN-based transistors have been realised through the development of surface pre-treatments; dielectric film deposition processes; and post-deposition heat treatments [4].

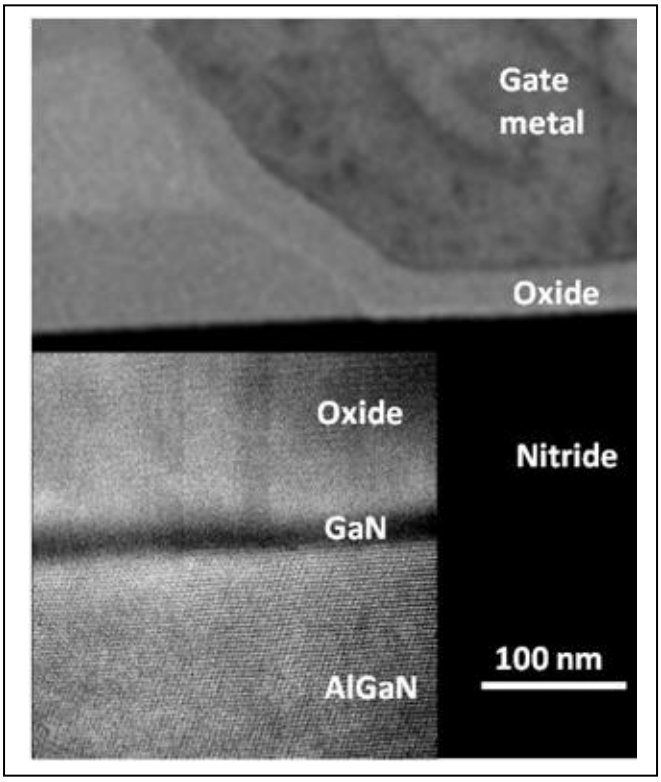
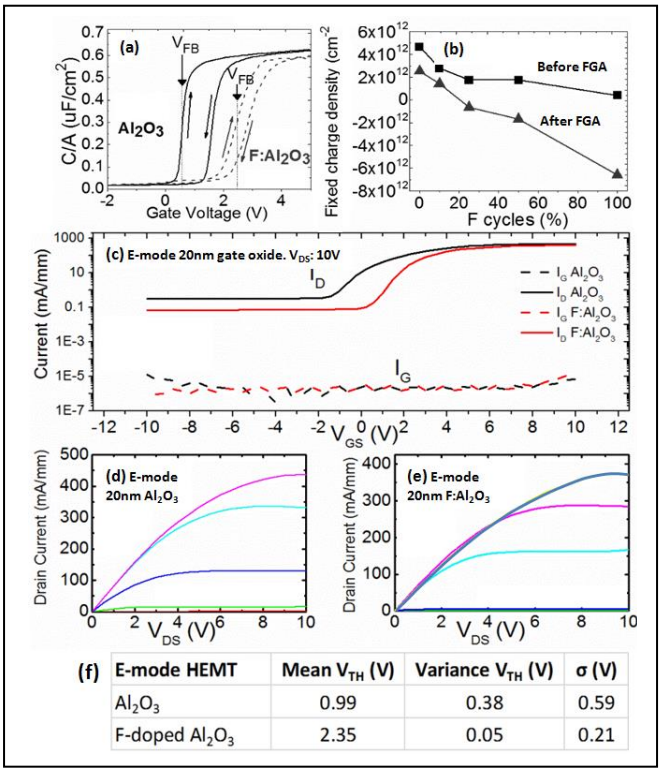



**Figure 1.** Cross section TEM of the gate MIS structure in a GaN-based MISHEMT. The inset shows a high resolution dark field image indicating the disruption of atomic lattice structure in the GaN cap adjacent to the $Al_2O_3$ dielectric layer.

**Current and Future Challenges**

The integration of insulted gate dielectric with III–N semiconductors continues to represent a significant hurdle to be overcome before E-mode MIS transistors can reach maturity. The dynamic charging of deep traps at the dielectric-semiconductor interface is associated with $V_{th}$ instability and long term reliability of the material system under electrical stress is uncertain. To begin to address some of these issues, gate dielectrics have been explored in the fabrication of E-mode MIS GaN-based devices. Two of the approaches explored to date include: (1) fluorine-doping which is used to passivate or neutralise positive charges at the semiconductor surface or in the dielectric itself; or (2) by recessing the gate by selectively etching the barrier layer in the region under the gate electrode. One example of F-doping via, $CF_4$-plasma treatment in the gate region of an AlGaN/GaN high-electron-mobility transistor (HEMT) [5]. Exposure to the plasma implants $F^-$ ions into the AlGaN barrier and underlying GaN-channel. After application of an ALD $Al_2O_3$ gate - dielectric, the F-doped semiconductor acts as a source of fluorine that diffuses into an $Al_2O_3$ dielectric compensating its intrinsic positive charge. It was reported that the $V_{th}$ increases with gate dielectric thickness, exceeding 3.5V for gate dielectrics 25 nm thick. Using in-situ fluorine-doping during ALD $Al_2O_3$ deposition, we reported the control of $V_{th}$ in enhancement-mode AlGaN/GaN MIS-HFETS [6]. When compared to the undoped dielectric, the F-doping caused positive threshold voltage shift (see figure 2) and a reduction of positive fixed charge in the gate oxide.




(f)

| E-mode HEMT | Mean $V_{TH}$ (V) | Variance $V_{TH}$ (V) | σ (V) |
|---|---|---|---|
| $Al_2O_3$ | 0.99 | 0.38 | 0.59 |
| F-doped $Al_2O_3$ | 2.35 | 0.05 | 0.21 |

Figure 2. Effect of F-doping in $Al_2O_3$ in E-mode MOS capacitors (a) Reduction in CV hysteresis.(b) Influence of forming gas annealing on fixed charge density. Effect of F-doping in $Al_2O_3$ in E-mode MISHFETs (c) $I_D$ and $I_G$ versus $V_{GS}$ for 20 nm $Al_2O_3$ and F:$Al_2O_3$. (d) $I_D$ versus $V_{DS}$ for 20nm $Al_2O_3$ gate oxide with $V_{GS}$ from -4V to +6 V in 2 V steps. (e) ID against $V_{DS}$ for 20 nm F:$Al_2O_3$ gate oxide with $V_{GS}$. (f) Mean, variance, and standard deviation (σ) of $V_{TH}$ for 15 of each type of MISHFET.

A dielectric is exploited in recessed gate MIS-HEMT, to suppress gate leakage current and increase the on-state gate swing. However, in the case of E-mode MIS-HEMTs, $V_{th}$ hysteresis can be caused by

large positive gate voltages due to 2DEG entering the deep trap states at the oxide/III-nitride interface. A demonstration of how this effect can be mitigated is through the application of an $Al_2O_3$/AlN gate stack insulator [7]. The insertion of a 2-nm thin plasma enhanced ALD AlN interfacial passivation layer yielded a device with a $V_{th}$ of +1.5 V, a current density of 420mA/mm and an OFF-state breakdown of 600V with low drain leakage of 1.7μA/mm.

The preceding discussion has focused on n-type (2DEG) channel MIS E-mode devices, however the realisation of p-type (2DHG) devices has received less attention to date. A significant advance in this respect, has been the demonstration of complementary metal–oxide–semiconductor (CMOS) GaN field-effect-transistor technology [8]. This landmark achievement is considered in more detail elsewhere in this roadmap. In the context of the dielectric employed, an MOCVD AlN/SiN dielectric stack was exploited as the gate oxide for both NMOS ($\mu_e$ - 300 $cm^2$/V-s) and PMOS ($\mu_h$ - 20 $cm^2$/V-s) transistors. The devices were used to demonstrate a functional inverter integrated circuit.

Significant advances have been made in the integration of gate dielectrics into III-N transistors, with the main purpose of minimising leakage currents in normally-off devices. A variety of dielectric materials have been assessed, using different deposition processes, but the main focused has been on $SiO_2$, $SiN_x$ and $Al_2O_3$. The continuing challenges for E-mode MIS devices are: (1) the minimisation of charge trap densities at the insulator/semiconductor interface across the range of barrier and channel III-nitride materials; (2) minimisation of the effect charging – discharging of trap states which gives rise to $V_{th}$ instability; (3) minimisation of the influence of bulk and border traps within the insulator dielectric itself which may impair the long term gate reliability and performance; (4) the development of processes and materials matched to the thermal budget of the device manufacture and the longer term in-field operating environment; (5) lastly addressing issues (1)-(4) in the context of PMOS E-mode devices [9, 10].

**Advances in Science and Technology to Meet Challenges**

The challenges of processing dielectrics for E-mode GaN MIS-based device technology are comparable to those encountered over the last two decades in the field of silicon CMOS. Fundamentally, the processing of dielectrics requires atomic-scale control over the preparation of the semiconductor surface, followed by assembly of the insulator with sub-nanometre precision over non-planar substrates comprising of a mixture of materials. The strategies for preparing III-nitride semiconductor (e.g. GaN, AlGaN, AlInN etc) surfaces for subsequent dielectric deposition will continue further development for both NMOS and PMOS technologies. Where these are combined on the same wafer for nitride-based circuits will add process complexity. The solution to this problem will have to involve removal or conversion of any unwanted native contamination at the semiconductor surface. Ideally the semiconductor surface would be atomically planar after preparation. Various wet and dry (e.g. thermal and plasma) processes have been explored to passivate and protect the semiconductor. It seems likely that future strategies may rely more on capping the semiconductor wafer in-situ at the end the III-nitride growth process to mitigate the problems associated with post-growth environmental exposure. Obvious candidates for this would be AlN- or SiN-based materials, but could include others. Alternatively, advanced strategies for the dielectric deposition process (e.g. ALD MOCVD PECVD, LPCVD or some physical vapour deposition method), would involve an in-situ preparation step. As an example, one prospect might be the

introduction of an atomic layer etching (ALE) step to remove unwanted native oxide / contamination. ALE could be applied to remove disordered gallium oxide / aluminium oxide residue, prior to the ALD of a "dielectric – quality" ALD layer. To realise this, further research would be required to develop ALE chemistries for the group-III oxides and nitrides.

In addition to surface pre-treatments, there is clearly scope for the development of improved dielectrics. Alternatives to the existing candidates, future developments might target multilayer dielectric stacks to target the overall gate capacitance, whilst enhancing resistance to gate-leakage. Multilayer gate stack might also be exploited to engineer band alignments to both the underlying semiconductor and the gate contact material. Current research has identified the use of fluorine- or hydrogen- "doping" in $Al_2O_3$ or $SiN_x$, as a method of "defect engineering" to neutralise or passivate traps in dielectric materials. There is clear scope for basic materials research to take this defect engineering further to enhance the electrical properties of gate dielectrics.

**Concluding Remarks**

The incorporation of MIS structures within E-mode GaN transistors offers a range of device design freedoms to realise monolithic GaN power IC, with reduced parasitic inductance and more efficient power switching at high frequencies. It is foreseeable that the development of gate dielectrics will be tuned to meet three overarching challenges. Firstly at the materials level, the dielectric stack will mitigate the effects of detrimental traps or defects within the dielectric and at the nitride semiconductor-dielectric interface, with negligible gate-leakage and maximum resistance to high-voltage electrical breakdown. Secondly, at the manufacturing stage, processing technologies will be required incorporate the dielectric into increasingly complex device architectures within the bounds of thermal budget. Thirdly, the development of dielectrics will be driven by the operational issues of life-time and reliability in the extreme environments experienced by GaN-based device technology.

**Acknowledgements**

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# 11 - Future Applications, Roadmap for GaN ICs

Dan Kinzer and Stephen Oliver, Navitas Semiconductor

**Status**

**The Power GaN Progression**

With Gallium Nitride (GaN) already established as a leading material for LED / opto applications and for RF amplifiers, this wide band-gap material emerged as an interesting academic option for discrete power devices around the turn of the century. Today, discrete GaN power devices have been qualified to JEDEC standards from 80 to 650V, using technology that has advanced from complex, costly and slow 'cascoded d-mode' implementations in highly-inductive through-hole packaging, to true single-die, e-mode devices in SMT formats [1]. However, significant system factors still exist which restrict practical switching speeds, negate the performance advantages of GaN and, as a result, have slowed market adoption.

The answer to this problem is derived from the lateral structure of GaN itself. A two-dimensional electron gas (2-DEG) with AlGaN/GaN heterojunction gives very high mobility in the channel and drain drift region, so resistance is much reduced compared to both Si and SiC. Circa 2009, early GaN power IC technology was published from university research [2]. The ability to integrate multiple power switches on a single chip is a big advantage for GaN power ICs. Isolating substrates began with sapphire and silicon carbide, though it was clear that an ability to grow GaN onto Si substrates enabled a cost structure and an ability to use existing large-diameter wafer fabs that would be a big cost and capacity advantage. Since Si is conductive, this introduces an additional challenge, of handling the substrate potential, and the way that it interacts with the power device.

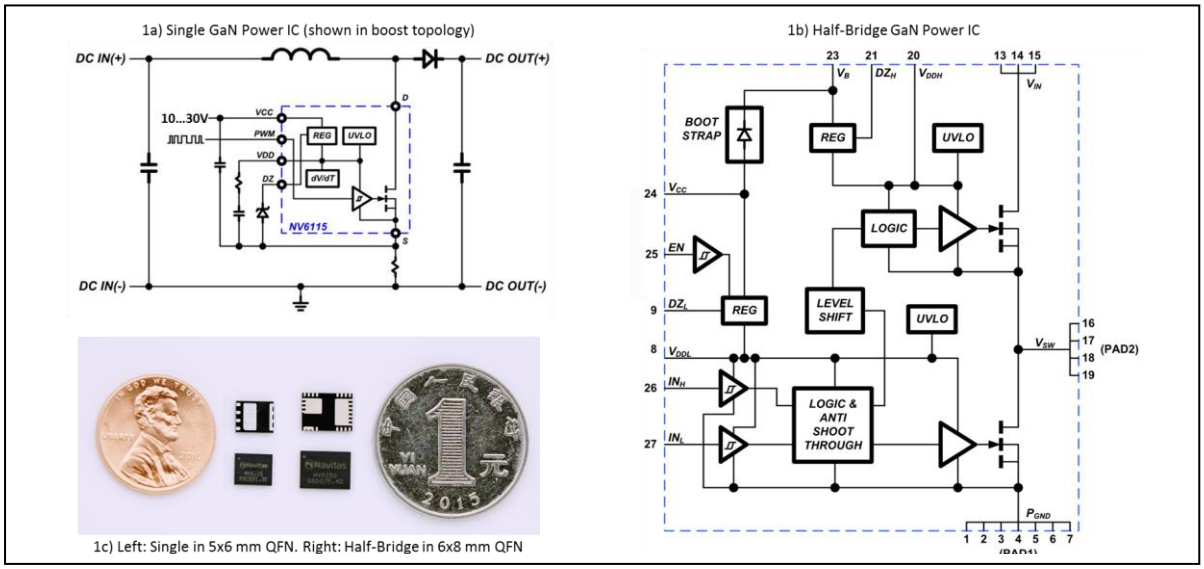


**Figure 1.** 650 V GaN Power ICs: 1a) single, 1b) half-bridge, 1c) package types, dimensions (Navitas Semiconductor)

**Current and Future Challenges - The GaN Power IC**

AllGaN™ is the industry's first GaN Power IC Process Design Kit (PDK), and allows the monolithic integration of 650V GaN IC circuits (drive, logic) with GaN FETs [3]. This proprietary PDK is remarkable given the restricted device-level tool-set, e.g. no p-channel devices are available. This monolithic integration is impractical using vertical GaN, d-mode GaN or SiC technologies.

For high-frequency operation, the most critical achievement has been the monolithic integration of GaN driver and GaN FET. In discrete implementations, the exposed GaN gate is vulnerable to noise and potentially damaging voltage spikes. Even when the GaN FET is included in a co-packaged, multi-chip module, the impedance between Si driver output and GaN FET gate leads to losses and potentially unstable operation. Only a monolithic solution delivers the required speed, efficiency and robustness [4]. From the driver integration, we can then consider 'higher-order' functions of the power IC such as inclusion of logic, start-up protection, dV/dt control, dV/dt robustness, and ESD to create full-function GaN Power ICs. Another major step is the combination of two FETs plus all associated drive, level-shift, bootstrap charging, and protection features (e.g. shoot-through prevention, UVLO, etc.) into a complete half-bridge power IC. Now, PWM ICs need simply to generate two, low current, ground-referenced digital signals and the half-bridge GaN power IC completes this ubiquitous building block.
Since the 1990s, when Si-based junction-isolation (JI) level-shifting techniques were introduced, power designers have searched for higher-efficiency and higher-frequency methods. Hybrid level-shifter techniques, e.g. capacitive- or inductive-coupling, have been introduced but the disparate semiconductor technologies used, plus complex assembly techniques meant large and expensive modules. The 650 V GaN Power IC enables the true, next-generation, monolithic-integration approach and results in a level-shifter which has 10x lower loss than Si and 3x lower than the best-in-class hybrids.

**Advances in Science and Technology to Meet Challenges**

**Real-World Applications**

GaN is a low-loss, fast-switching material and enables a range of new high-frequency topologies to move from academic to commercial applications. Commercial devices now have blocking voltage ranging from 40 V to 1,200 V. Generational improvements are driving $R_{DS(ON)}$ and device capacitances lower, but still far from a theoretical limit. For high voltage devices, $R_{DS(ON)}$ scales approximately as $(L_{GD})^2$. Drain-drift length is still 5X larger than the limit for 650 V devices, which means a 10X improvement in transistor area for a specific resistance value is possible and can be expected over the next 10 years.
The easy-to-use GaN power IC building block now becomes the core enabler for high frequency, soft-switching topologies such as active clamp flyback (ACF), critical conduction mode (CrCM) and totem-pole power factor correction (PFC) and LLC DC-DC circuits to enter mainstream markets [5], [6], [7]. Expect more system-enhancing and application specific features to be added to the power ICs, which will improve timing control, fault detection and feedback, and light-load loss reduction.
In parallel, new magnetic materials are being developed and released to production with high-efficiency operation up to 5 MHz. Multi-MHz DSP controllers are available for higher power applications and new high-frequency, cost-effective ASICs are being introduced to enable adoption in price-sensitive markets such as smartphone and laptop chargers. Soft-switching circuits in the 5-10 MHz range frequency with simultaneous increase in efficiency deliver cost-effective, increased power density [8].
Practical examples of soft-switching topologies today are shown below in Figure 2. Note that the mechanical construction/assembly techniques used are industry-standard, and readily-available at low cost. The 65 W solution operates at ~400 kHz, while the 150W circuit operates at 1 MHz.

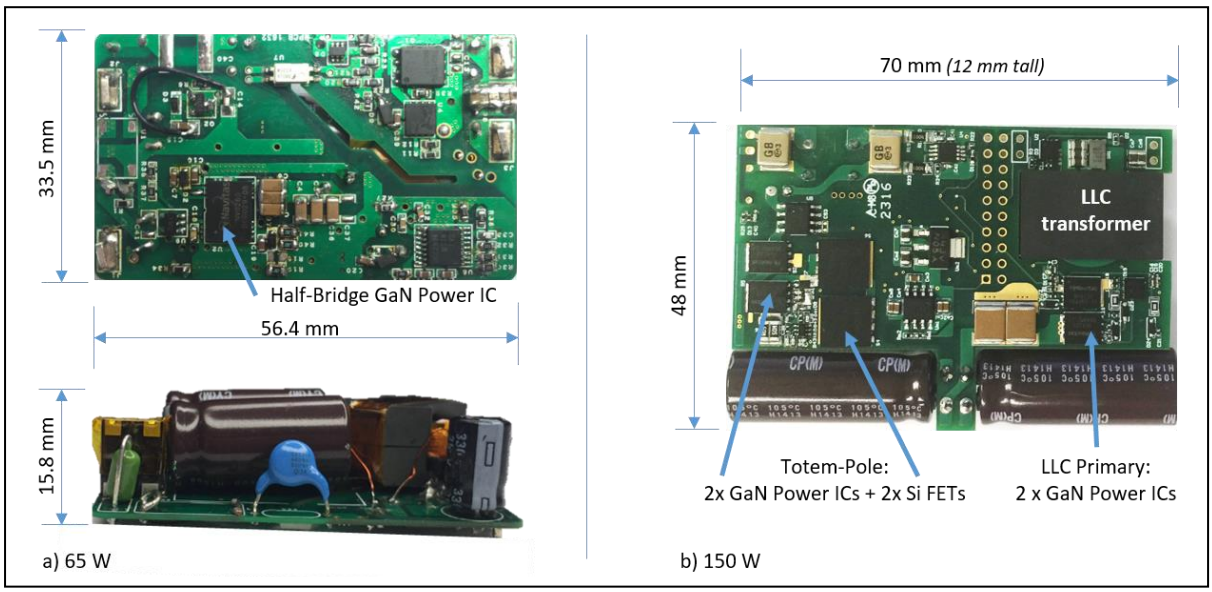


Figure 2. Examples of AC-DC converters using GaN Power ICs;
a) 65 W Active Clamp Flyback at 300 kHz using commercial control ASIC and Half-Bridge GaN Power IC, 94.5% peak efficiency at full load, 1.5 W/cc (24.6 W/in$^3$) uncased power density (Navitas Semiconductor), and
b) 150 W Totem-Pole PFC plus LLC at 1 MHz using single GaN Power ICs, >95% peak efficiency at full load, 3.7 W/cc (60 W/in$^3$) uncased power density. DSP controller not shown (courtesy of CPES, Virginia Polytechnic).

The same GaN Power ICs may be applied in high-power, multi-kW applications, with one example being a 3.2 kW, 1 MHz, AC-48 V converter prototype with 65 W/in$^3$ power density [9]. Here, the single devices are paralleled to achieve lower $R_{DS(ON)}$ and interleaving techniques are used for the Totem-Pole PFC and LLC sections.

## Concluding Remarks

### Major Accomplishments, Major Opportunities

The last 20 years have seen GaN's progression from RF to power discrete and now to the first generation of AllGaN power ICs. This has enabled advanced, soft-switching topologies to enter the commercial marketplace. Next-generation monolithic integration (e.g. advanced I/O features, over-current and over-temperature protection) will enable even higher levels of efficiency, power density and reduced system cost. Today, we see the simultaneous 'perfect storm' of new devices, new topologies, new magnetics and integration lead to major steps in efficiency, density and system cost-reductions. The power revolution of the late 1970's [10] will finally repeat today, 40 years later.

## Acknowledgements

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# 12 - Potential of Polarisation Super Junction Technology in Gallium Nitride

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**Status**

Amongst many semiconductors, Silicon Carbide (SiC), Gallium Nitride (GaN) and Diamond can offer significant system level benefits and have the potential to meet the anticipated power densities by 2025 [1]. GaN offers similar performance benefits to SiC, but with a greater potential for cost-reduction as well as higher frequency. Price advantage over SiC is also possible because GaN power devices can be grown on substrates that are larger and less expensive than SiC. Since the first report of high density 2-Dimensional Electron Gas in 1991 [2] and High Electron Mobility Transistors in 1993 [3], GaN has gained traction and now discrete GaN transistors are emerging as commercial products. Their performance is however limited to about 1/5$^{th}$ of their potential capability by slower external silicon gate driver circuits required to control them. Si circuits have a limited operating temperature range and inherently efficient GaN devices are forced to slow down, leading to failure and severe derating of efficiency. The dual (Si & GaN) technology approach impacts cost deleteriously. By monolithically integrating control circuits with power devices on a single GaN technology platform the efficiency can be greatly increased, and cost reduced. Moreover, because of the difficulty in obtaining p-channel devices, integrated circuits (ICs) thus far demonstrated are made of n-channel devices.

**Current and Future Challenges**

In GaN-on-Si technology, the breakdown voltage is primarily determined by the GaN buffer and therefore thick buffer and transition layers are necessary to sustain high voltage, which make the wafers more susceptible to bowing and crack generation. The inherent tensile stress due to mismatch in lattice constants and coefficients of thermal expansion in such structures can also compromise the reliability of devices. Lack of avalanche capability or non-destructive breakdown behaviour, necessitates over-rating the device breakdown voltage for a given application. Moreover, there is a significant level of defects in layers and understanding of these defects and their relationship with device reliability is necessary. The conventional GaN technology uses metal field plates. However, the distribution of the electric field is not uniform, which impacts breakdown voltage along with rendering such devices to be sensitive to current collapse during high voltage switching. The field distribution is also highly sensitive to changes in charges accumulated in the insulators sandwiched between the semiconductor surface and the field plates. Realizing such high voltage devices also requires sophisticated processing capability for formation of precise field modulating plates. An alternative solution for manufacturing low-cost high-voltage GaN power switching devices, which can overcome some of the above-mentioned challenges is the Polarisation Super Junction (PSJ) technology, which is described in the next section. This technology is also a highly promising candidate for the fully GaN based power ICs.

**Advances in Science and Technology to Meet Challenges**

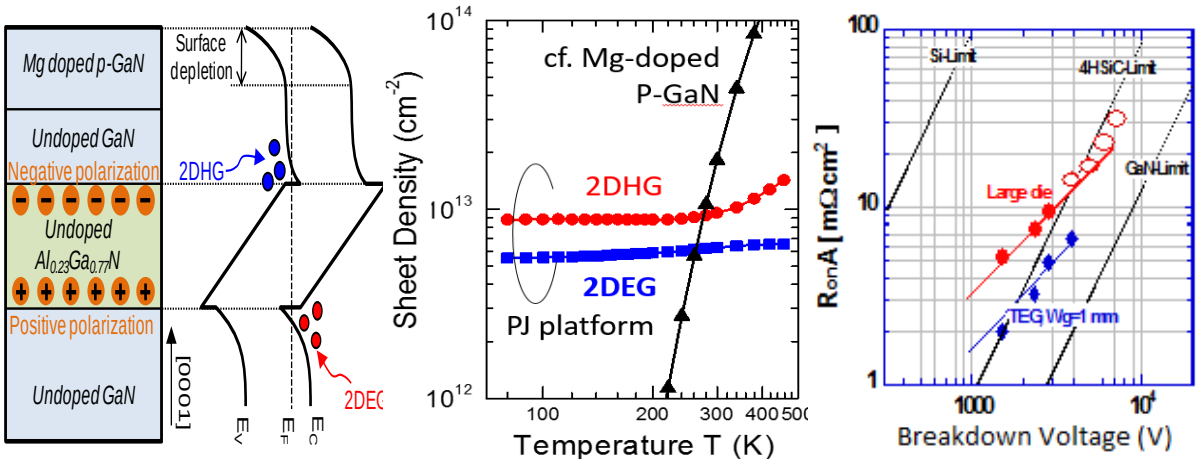


**Figure 1 (left): Double heterostructure in GaN [5]; Figure 1(middle) Measured 2DEG and 2DHG through Hall Effect measurements; Figure 1(right) Variation of measured specific on-state resistance with breakdown voltage of PSJ-HFETs against calculated unipolar 1-D material limits of Silicon, SiC and GaN [8].**

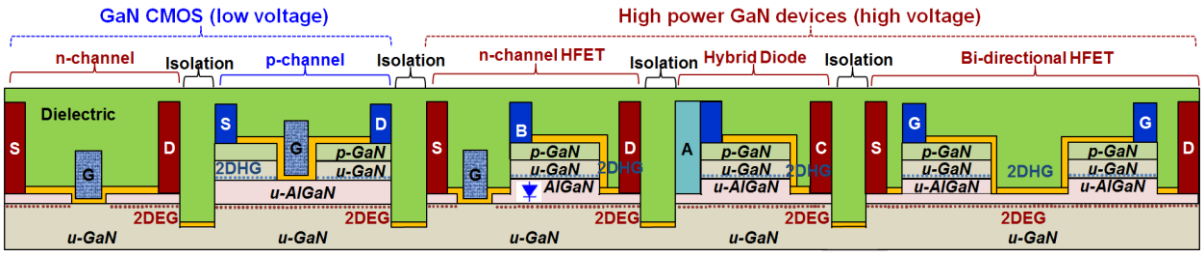


**Figure 2: Proposed PSJ Platform for Monolithic Power Integrated Circuits. Please note that the substrate is not specified. However, thin sapphire is the most cost-effective option because of the use of uniform thickness of 1 µm u-GaN buffer layers to serve for both low as well as high voltage devices and provide full electrical isolation (critical requirement for monolithic integration).**

In 2006, a polarisation junction (PJ) concept was proposed based on the charge compensation of positive and negative polarisation charges at heterointerfaces of a GaN/AlGaN/GaN structure [4]. This was followed by the successful demonstration of GaN double heterostructures, grown along the (0001) crystal axis, where high density positive and negative polarisation charges coexist at the AlGaN(000$\bar{1}$)/GaN(0001) interface with accumulated two-dimensional electron gas (2DEG) and two-dimensional hole gas (2DHG) accumulated at the GaN(000$\bar{1}$)/AlGaN(0001) interface respectively, as shown in Fig 1 (left) and Fig 1(middle) which has since enabled a Polarisation Super Junction (PSJ) technology [5]. Like the Superjunction in Si, PSJ enables linear scaling of breakdown voltage with increase in thickness or length of the drift region and with performances beyond that of 1-D 4-H Silicon Carbide limit, as shown in Fig 1(right). Over the past few years, high performance diodes, transistors as well bidirectional switches have been demonstrated [6,7]. Enhancement-mode PSJ-HEMTs have also been reported with most recent results of large (4 X 6 mm$^2$) and small devices made on Sapphire substrates showing with breakdown voltages beyond 3 kV [8]. Moreover, due to the effective lateral charge balance and field distribution, these devices fabricated on Sapphire substrate show no current collapse. One of the key attributes of the PSJ technology is that it is viable to make both NMOS as well as PMOS circuits, and CMOS inverter operation of a monolithic P- and N-channel MOSFETs has been demonstrated on this platform [9]. This technology also paves way for bidirectional switches with integrated diodes. This device is well suited for a variety of applications and for solid state circuit breaker because, PSJ offers the possibility of realising much lower saturation currents than conventional HFETs [5], while maintaining ultra-low on-state resistance. Thus, Polarisation Super Junction technology can pave the way for high power density monolithic integration of various devices for a variety of applications, as shown in Fig. 2.

Most recently, the PSJ concept has been extended to Vertical GaN technologies and is termed as Vertical Polarisation Super Junction (VIPSJ) with predicted benefits of 2 orders of magnitude reduction in specific on-state resistance in comparison to SiC at 1 kV rating [10].

**Concluding Remarks**

There are several scientific, technological and manufacturing challenges that need to be addressed before GaN power semiconductor devices can be considered mainstream. It is also becoming apparent that a transition from the general scheme of manufacturing power conversion circuits using discrete devices to that of a fully integrated power system-on-chip is anticipated to be a prerequisite to fully harness the high-frequency power switching benefits of GaN. To conclude, GaN PSJ technology will be instrumental in shaping a viable and a new era of an integrated power electronics for ultra-high-power density converters.

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# 13 - Technological Challenges in Next-Generation GaN-based Power Integrated Circuits

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**Status**

Si-based lateral power devices have been widely utilized in high-frequency and low-power converters for ratings of up to several hundred watts [1]. On the other hand, GaN-based heterojunction field-effect transistors (HFETs) utilizing polarization-induced 2D electron gas (2DEG) are emerging components for such high-frequency converters. GaN-based discrete devices up to 650-V rating are commercially available now. The development of GaN growth technology on conductive Si substrates has largely contributed to the improvement in the device performance and decrease in cost [2]. As a next step, towards achieving high intrinsic switching capability of GaN devices, monolithic integration of GaN-based converter circuits will be necessary. Area-specific on-resistances of GaN-HFETs are already two orders of magnitude smaller than those of Si-based lateral power devices. Owing to this significant footprint reduction, high output powers of up to several kilowatts can be expected in GaN-based monolithic converters. In this article, two technological challenges are addressed: the "crosstalk effect" and "heat dissipation" in next-generation ultra-high-frequency monolithic power integrated circuits (ICs). These issues are quantitatively discussed using simple analytical models.

**Current and Future Challenges**

As an example of GaN power ICs, if an integrated half-bridge circuit on a conductive Si substrate as shown in Fig. 1 is assumed with the following parameters: voltage rating of the GaN devices are 600 V, input voltage $V_{IN}$ is 400 V, 2DEG density $N_s$ has a conventional value of $10^{13}$ cm$^{-2}$, and dielectric constant $\varepsilon$ of the GaN-based epilayer is $9.0\varepsilon_0$.

Firstly, the "crosstalk effect" is discussed. In discrete GaN devices, the substrate potential is shorted with the source electrode. The conductive Si substrate acts as a back-side field plate contributing to the suppression of current collapse. However, in an IC, it induces a significant increase in the on-resistance of the high-side transistor [3]. This is because the 2DEG of the high-side transistor interacts with the substrate potential through the GaN epilayer capacitance $C_{epi}$. During the on-state of the high-side transistor, the input voltage $V_{IN}$ is directly applied to $C_{epi}$, inducing a 2DEG density reduction $\Delta N_s$:

$$q\Delta N_s = C_{epi}V_{IN} / A = \varepsilon V_{IN} / t_{epi}, \qquad (1)$$

where $q$ is the electron charge, $A$ is the GaN device area, and $t_{epi}$ is the GaN-based epilayer thickness grown over silicon substrate. If we consider a 2DEG density reduction of 10% (i.e., 10% on-resistance increase), the calculated $t_{epi}$ is 20 μm. In comparison with a GaN-based epilayer in conventional discrete devices (3-5 μm), power IC applications require an epilayer which is thicker by five times.

Next, the issue of "heat dissipation" challenges are discussed under hard switching condition. When the gate drive speed is sufficiently high, power loss of the hard-switching circuit (Fig. 1) reaches the minimum value. Under the minimum loss condition, the heat density $HD$ of the GaN chip can be expressed as

$$HD = Q_{oss}V_{IN} f / A = qN_s V_{IN} f, \qquad (2)$$

where $Q_{oss}$ is the output charge of each GaN transistor and $f$ is the the output pulse-width modulation frequency. Eq. (2) implies that a charge $Q_{oss}$ is supplied from the voltage source $V_{IN}$ during every switching period, and the energy is consumed as joule heat in the GaN chip. Fig. 2 shows the heat density calculated using Eq. (2). Although high-frequency operation is expected in hard-switched GaN

monolithic converters, the estimated heat density is unacceptably high. For example, it is 6.4 kW/cm$^2$ at 10 MHz.

**Advances in Science and Technology to Meet Challenges**

The substrate material for the growth of GaN-based layers is a key element of power ICs. Because conductive Si substrates induce the crosstalk effect, novel platform substrates are required for next-generation ICs, especially for high-voltage and high-frequency applications. GaN-on-silicon-on-insulator (SOI) technologies are a promising solution which can enable CMOS compatibility in the GaN device fabrication process [4, 5]. The contribution of the back-side field plate effect is also obtained through substrate contact from the front side [5]. However, a several-μm-thick $SiO_2$ buried layer will be required to sustain 600 V or more. The thermal conductivity of $SiO_2$ is two orders of magnitude smaller than that of Si. Therefore, heat dissipation from integrated GaN devices on an SOI substrate will be big challenge. Furthermore, GaN power device technologies on insulator sapphire substrates are equally promising candidates [6, 7] because they yield high-quality GaN crystals. However, on such insulator substrates, current collapse must be eliminated without the support of the back-side field plate effect. Effective lateral electric field management strategies will be necessary, such as polarization superjunction technology [6].

In addition, other emerging candidates must be considered. Because the thermal conductivity of SiC is three times higher than that of Si, GaN technologies on highly resistive SiC substrates have been widely used in RF applications and are also emerging candidates in power converter applications. Finally, GaN-on-diamond technology might be the ultimate solution to the heat dissipation issue because diamond has the highest thermal conductivity [8-10].

**Concluding Remarks**

In next-generation GaN-based power ICs, device isolation technologies are a key challenge, especially in high-voltage applications. GaN-on-SOI and GaN-on-sapphire technologies are promising candidates from this perspective. In addition, thermal management is a key issue. Area-specific on-resistance has been a major benchmark parameter of GaN-HFETs. In addition, the minimization of area-specific "thermal-resistance" will be a key strategy in GaN-based IC development. Therefore, GaN device technologies utilizing high-thermal-conductivity substrates such as SiC and diamond are also emerging as platform substrates for GaN power ICs. However, on any platform, potential advantages in performance and cost should be considered from the system level viewpoint.

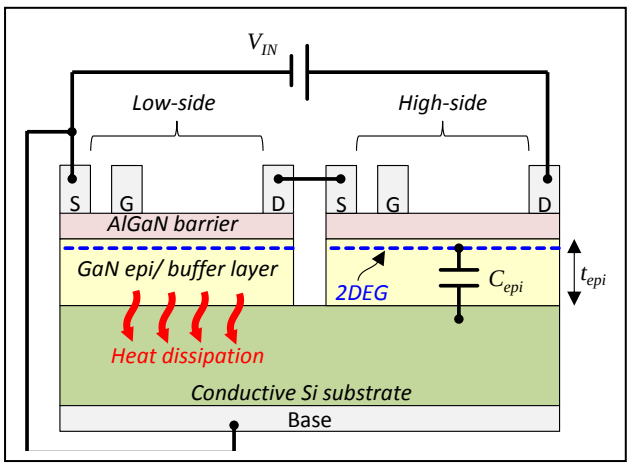


**Figure 1.** Schematic cross section of monolithic half-bridge circuit on conductive Si substrate.

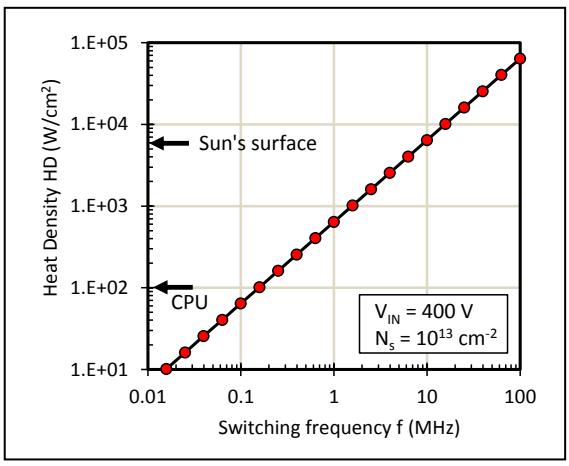


**Figure 2.** Calculated heat densities of GaN chip depending on output frequency under hard switching condition.

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# 14 - GaN CMOS: fact or fiction?

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**Status**

GaN power transistors have demonstrated unprecedented switching speed [1]. At high switching speed, parasitic inductance in the power loop as well as in the drive loop causes large voltage overshoot [2]. In current practice, the GaN switch is often intentionally slowed down to avoid catastrophic failure and additional power consumption induced by the voltage overshoot [3]. To take full advantage of the high-speed GaN switch, one need to eliminate the parasitic inductance by monolithically integrating power switches and their gate drivers. The gate driver typically uses a Totem-Pole topology with a pair of complementary N-type and P-type transistors. The complementary transistors eliminate static power consumption. GaN CMOS technology is needed to realize monolithic GaN power IC integrating high-voltage GaN transistors with low-voltage N- and P-type GaN transistors on the same chip.

The monolithic GaN power IC, as shown in Figure 1, minimizes interconnect parasitic between power switches and gate drives. Reduction of interconnect parasitic enables efficient power switching at high frequencies. At high frequencies, the size of passive components can be drastically reduced. Reduction of interconnect parasitic also enables active control of switching trajectory with minimal time delay. Active control of switching trajectory mitigates device stress and improves the reliability. The monolithic GaN power IC enables modular architecture where a number of power switching unit cells, e.g. half bridge, can be stacked in parallel and in series to scale the current and voltage handling capability. The monolithic GaN power IC enables cost reduction by cutting the assembly and packaging cost, as well as by using the modular architecture consisting of standardized switching unit cells.

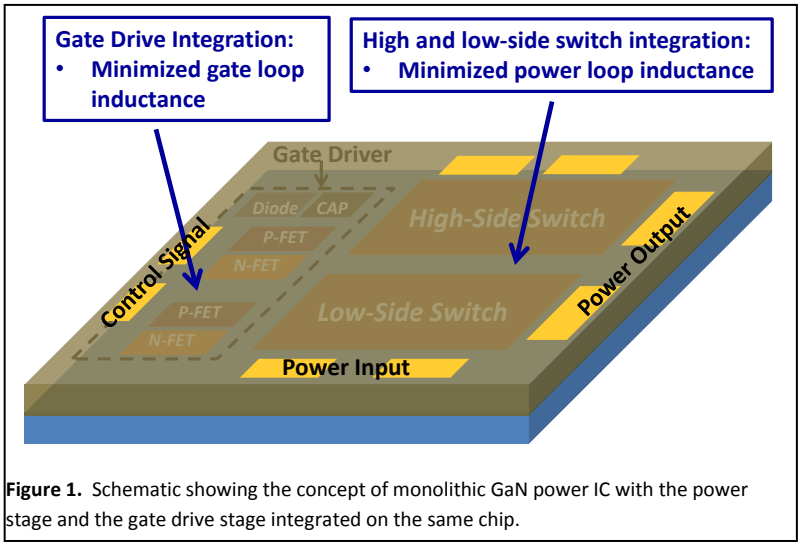


**Figure 1.** Schematic showing the concept of monolithic GaN power IC with the power stage and the gate drive stage integrated on the same chip.

**Current and Future Challenges**

N-type GaN high- and low-voltage transistors are readily available. Difficulty in making P-type GaN transistor and integrating it with the N-type transistor has been the major obstacle for realizing the GaN CMOS technology. There have been a few early studies on P-type GaN transistors [4]–[7], an attempt to integrate P- and N-type Schottky gate GaN transistors [8], and lately a demonstration of a working GaN CMOS IC inverter [9]. The GaN CMOS demonstration was achieved through selective area regrowth of P-type GaN transistor structure on a wafer with N-type GaN transistor epitaxy structure. Significant improvement of the GaN CMOS technology is needed to meet the performance requirement of the monolithic power IC. Specifically, there are two major challenges to be addressed. One challenge is the low output current, or high on-resistance, of the P-type transistor. The other challenge is the off-state leakage current of the P-type transistor when integrated with the N-type transistor. The low output current results from poor hole mobility, low mobile hole concentration, and

poor ohmic contacts. The off-state leakage is attributed to impurity contamination at the regrowth interface.

**Advances in Science and Technology to Meet Challenges**

Figure 2 shows device structure, IV curves, and on-resistance component breakdown of a P-type GaN transistor reported in Ref. 9. Inefficient P-type doping is the primary challenge responsible for the low current and the high on-resistance. Mg, with an activation energy as high as 0.2 eV in GaN, is used as the acceptor. High dopant activation energy leads to low concentration of mobile holes even at high doping level, therefore high contact resistance and high access resistance. Advance in P-type doping technique, e.g. polarization-assisted doping [10], has the potential of overcoming the doping challenge. Low hole mobility is another important factor responsible for the high on-resistance. Low hole mobility is caused by severe impurity scattering, interface scattering under the gate insulator, and large hole effective mass. In addition to enhancing doping efficiency, improvement of insulator-semiconductor interface is important for achieving better hole mobility and lower channel resistance. Strain engineering may increase the population of light holes, thereby improving the hole mobility. In addition to improving hole density and mobility, reducing or eliminating the spacings between gate and source/drain electrodes can effectively improve the on-resistance.

Improvement of epitaxy regrowth process is needed to eliminate the off-state leakage current shown in Figure 2. P-type transistors fabricated on P-type only wafers didn't show this off-state leakage. The off-state leakage is attributed to Si contamination commonly observed at the regrowth interface. The source of the Si contamination can be volatile organic silicon compound in the air ambient. A regrowth process avoiding such contamination is needed to integrate high-performance P- and N-type transistors.

Comprehensive study of gate dielectric in P-type transistors is also needed to ensure stable threshold voltage, and facilitate scaling to smaller gate lengths.

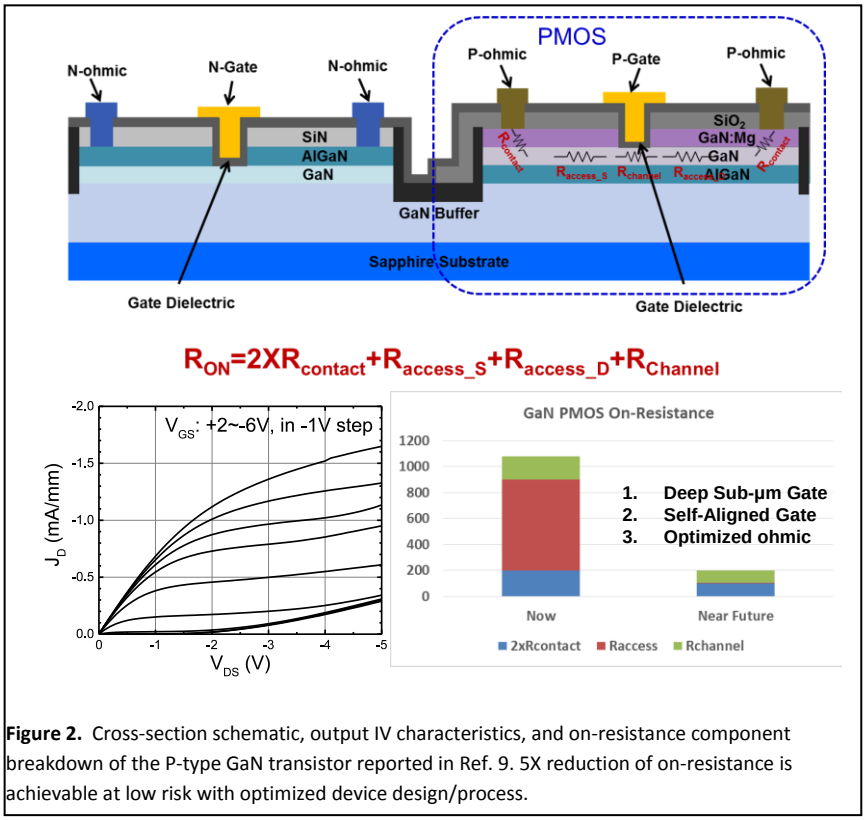


**Figure 2.** Cross-section schematic, output IV characteristics, and on-resistance component breakdown of the P-type GaN transistor reported in Ref. 9. 5X reduction of on-resistance is achievable at low risk with optimized device design/process.

**Concluding Remarks**

Monolithic power IC based on the GaN CMOS technology is essential for realizing and maximizing the performance/cost potential of GaN power electronics. Early work on GaN N/P-type transistors and GaN CMOS technology has proved that the GaN CMOS is a fact, not a fiction. Improvement of P-type doping and selective area regrowth is important for realizing high-performance GaN CMOS technology for monolithic power IC applications.

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# 16 - 600V E-mode GaN Power Transistor Technology: Achievements & Challenges

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**Status**

Since the first confirmation of a 2DEG at the AlGaN/GaN interface in 1992 and the first availability of GaN-on-SiC radio frequency power transistors in 1998, nitride semiconductor hetero structure electron devices now constitute a hundred million dollar market for RF power. As regards power conversion applications, GaN-on-Si high voltage power transistors have been in development stage for the past decade with initial focus on depletion mode devices due to the inherent nature of the 2DEG. However most power electronic applications demand for enhancement mode devices. The first high voltage solution released to market in 2015 by TransPhorm [1] is based on a cascode configuration of a low voltage Si-MOSFET in series connection with a high voltage GaN MIS-HEMT to solve that issue. Following the progress of enhancement mode devices based on a p doped GaN gate module for low voltage GaN power transistors from EPC [2] we now see the first fully industrial qualified 600V true enhancement mode (E-mode) GaN power transistors on the market from Panasonic and Infineon [3-5]. These E-mode GaN power transistors are based on a fully recessed gate module with subsequent regrowth of a second AlGaN barrier with pGaN (see Fig. 1) on top for an excellent control of the threshold voltage independent of the drift layer carrier density [6]. pGaN is also used at the drain region as drain extension which improves the dynamic on state resistance to well below 10% even at high temperatures of 150°C and full rated drain voltage of 600V down with delay times as short as few hundreds of ns from blocking mode to settled on state resistance measurement. At the same time this drain sided pGaN region (see Fig. 1) also improves the robustness of the device to the required levels for hard switching applications [3]. The devices are offered in surface mount device packages allowing for designs with low loop inductances including top side cooled variants for enabling 3kW converters without need for paralleled devices (see Fig. 1). Recently it has been demonstrated that the gate module even allows for a >10µs short circuit robustness at full bus voltage of 400V when driven properly [7]. The technology has been implemented in a volume silicon power fab with a very high degree of equipment sharing with standard silicon processes to achieve economy of scale.

When comparing Infineon's CoolGaN™ technology to the state-of-the-art silicon super junction devices (Si SJ) as well as other wide band gap technologies on the market (see Table I) we see that all WBG technologies offer roughly the same order of magnitude improvement in output charge $Q_{OSS}$ per $R_{DSON}$ and two orders of magnitude improvement in reverse recovery charge per $R_{DSON}$. However, only E-mode GaN offers at the same time one order of magnitude of gate charge $Q_G$ improvement which makes it the perfect device for high frequency resonant switching. Resonant converters with 3kW power level operating at 350kHz without sacrificing peak efficiency of 98.4% demonstrate high density of 170W/in³ [8]. For hard switching applications the relevant figure-of-merit is the energy stored in the output capacitance ($E_{oss}$) and here recent developments in Si SJ devices have raised the bar significantly so that as of today only E-mode GaN can outperform Si. In combination with the lack of reverse recovery charge that enables the use of GaN devices in half bridge configurations new and simpler topologies like full bridge totem pole are possible.

| Device | Rating [V] | $R_{DSON}$ [mOhm] | $R_{DSON}*Q_{OSS}$ [mΩμC] | $R_{DSON}*Q_{RR}$ [mΩμC] | $R_{DSON}*E_{OSS}$ [mOhm*uJ] | $R_{DSON}*Q_G$ [mΩnC] |
|---|---|---|---|---|---|---|
| Si Super Junction [a] | 600 | 56 | 23.5 | 336 | 450 | 3800 |
| **GaN eMode** [b] | 600 | 55 | **2.2** | **0** | **350** | **320** |
| GaN Cascode [c] | 600 | 52 | 3.8 | 7.1 | 730 | 1460 |
| GaN Direct Drive [d] | 600 | 70 | 4.1 | **0** | 530 | n.a. |
| SiC DMOS [e] | 900 | 65 | 4.5 | 8.5 | 570 | 1950 |
| SiC TMOS [f] | 650 | 60 | 3.8 | 3.3 | 540 | 3480 |

**Table 1.** Benchmark of State-of-the-Art High Voltage Power Transistors: a) Infineon CoolMOS™ IPL60R065C7 Datasheet, b) Infineon CoolGaN™ Preliminary Datasheet ($Q_{RR}$ is exclusive of $Q_{OSS}$), c) TransPhorm Cascode TPH3205WS Datasheet, d) TI Direct Drive LMG3410 Datasheet, e) Wolfspeed C3M0065090J Datasheet, f) Rohm SCT3060AL Datasheet (all values given typical at 25°C incl. package).

*Current and Future Challenges.* One of the biggest challenges to release power GaN devices to the market has for sure been their reliability. The hetero epitaxial growth of the GaN buffer on silicon wafers unavoidably leads to lattice misfit dislocations and other growth defects. At the same time present lateral GaN devices differ from the established silicon power devices in many aspects as they are based on hetero junctions, differences in spontaneous polarizations and bulk/surface donors to generate the 2DEG instead of p and n dopings. The qualification of those devices therefore cannot solely rely on established silicon procedures (e.g. according to JEDEC Solid State Technology Association, former Joint Electron Device Engineering Council) but must take into consideration the new possible failure modes and physics together with the corresponding lifetime models and application profiles to determine appropriate qualification tests and durations. It is also essential to derive appropriate screening tests based on intrinsic and extrinsic lifetime models to achieve the needed low field failure rates of 1 fit or less. Passing all those qualification procedures still does not guarantee stable long term behaviour in the application. Long term testing of the devices under real application conditions with no fails is a first necessary step, but only application testing with accelerated conditions (e.g. higher temperatures, bus voltages, peak currents) and testing to failure allows extraction of life time models and hence failure rates in real life [9]. As a joint effort by the major semiconductor companies involved in GaN, a working group for the standardization of GaN qualification under the framework of JEDEC has been recently established to address many of the before mentioned aspects [10].

**Advances in Science and Technology to Meet Challenges**

For further advancing the reliability of GaN devices it is important to further deepen the understanding of defects and their relation to device behaviour and device reliability. This comprises e.g. the understanding of point defects including their electronic structure mainly in the various parts of the AlN/AlGaN/GaN buffer, channel and barrier layers and how those defects are influenced by the growth conditions of the material and the selection of possible advanced substrates. In order to possibly achieve future enhancement mode devices based on MIS gate structures with low leakage currents and a wide range of threshold voltages and gate drive voltages a big step in understanding on how to reduce the interface defect density of gate dielectrics on top of GaN and how to improve channel mobility is needed.

An important mid to long term challenge for GaN technology to enable broader market penetration is approaching cost parity per same $R_{DSON}$ compared to silicon devices like CoolMOS™.

This will be driven on the one hand side by reducing the cost per die area through increasing economy of scale and increased yield with rising volume and the introduction of 200mm wafer diameter for GaN-on-Si during the next few years as well as the step to 300mm within the next decade. On the other hand we will see further die shrinks through better exploration of the material limits e.g. by increased material quality allowing for shorter drift regions through higher electric fields as well as advanced drift region engineering (improved field plates, graded 2DEG density, etc.) allowing for higher carrier densities without compromising reliability.

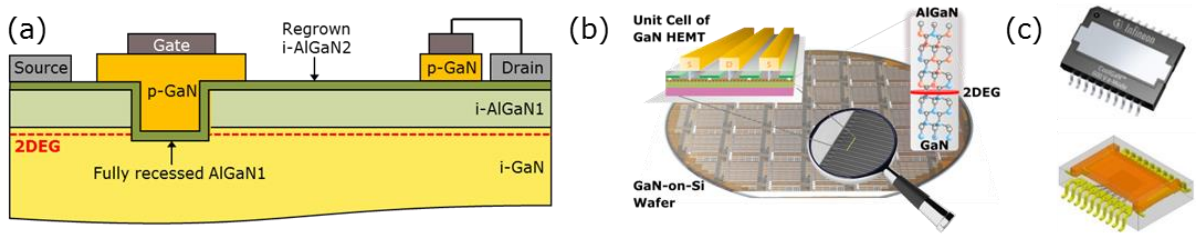


Figure 1. a) 600V E-mode GaN cell concept with through recessed first AlGaN barrier and regrown thin second AlGaN barrier with pGaN enhancement mode gate, b) GaN-on-Si wafer with enlarged unit cell and schematic of AlGaN/GaN hetero junction forming the 2DEG, c) top side cooled SMD package: top view and schematic with wire bonds

**Concluding Remarks**.

After GaN-on-SiC RF power devices have reached a multi hundred million dollar market volume, and after a decade of intense research and development of GaN-on-Si power technology, fully industrial qualified 600V true enhancement mode GaN power devices are finally entering the market. Qualification procedures and screening methods have been established according to the needs of the new material system and taking into consideration typical industrial application profiles targeting field failure rates below 1 fit. The new devices offer customers the degree of freedom to either boost the power conversion efficiency to unprecedented levels of 99% and beyond or to significantly increase the power density of their converters without compromising the efficiency.

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# 17 - Potential of GaN Integrated Cascode Transistors

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**Status**

AlGaN/GaN high electron mobility transistors (HEMTs) are poised to replace Si MOSFETs for high frequency power switching applications up to 600 V. Enhancement mode (E-mode) operation with a positive threshold voltage ($V_{TH}$) $\geq$ 3 V is desirable for circuitry protection and safety purposes but GaN HEMTs are naturally depletion mode (D-mode) devices. Cascode devices with low voltage E-mode Si MOSFETs and high voltage D-mode GaN HEMTs offer an excellent solution to the E-mode operation issue using existing gate drivers. In addition, the cascode structure can lead to improved switching speed and reduced switching losses compared to an equivalent discrete transistor [1]. Here, we discuss the challenges faced by cascode devices as well as the potential of integrated cascode structures to achieve high switching frequency.

**Current and Future Challenges**

Despite the promising performance of commercial 600 V hybrid GaN plus Si cascode transistors [2], several issues hinder their switching performance. Firstly, additional package connections in the hybrid cascode lead to increased parasitic inductances which can cause excessive ringing and limit the operating frequency [3]. This presents major challenges to packaging design. In addition, the intrinsic capacitance mismatch between the Si and GaN transistors and the body diode in the Si MOSFET can result in additional switching losses when the Si device is driven into avalanche mode during turn-off [4].

Monolithically integration of E-mode and D-mode GaN devices in the cascode configuration, on the other hand, will mitigate the parasitic inductances and the 'slower' Si device issues in the hybrid GaN plus Si cascode devices. However, $V_{TH}$ of the reported E-mode GaN devices using various techniques such as fluorine (F) treatment on the barrier under the gate [5], GaN MOSFETs [6] and p-AlGaN gate [7] remains low, typically less than 2 V. This presents an issue for gate driving as un-intended turn-on may occur with a voltage ringing effect as a result of CdV/dt coupling from the drain to the gate.

**Advances in Science and Technology to Meet Challenges**

The switching losses in a field effect transistor are partly determined by the current through the resistive loss-generating channel during the charging/discharging processes [8] and hence depend on the speed of charging and discharging the Miller capacitance (Miller effect) at high voltages. The latter depends on the load current-to-gate drive current ratio. On the other hand, the discharging of the charge stored in the output capacitance of the cascode device is not limited by the gate drive current during turn-on as shown in Figure 1(a). During turn-off, the cascode connection utilises the load current to charge the output capacitance and a faster turn-off time can be achieved for the same gate drive capability. The GaN-based integrated cascode transistor is an excellent candidate to exploit these switching advantages without the additional parasitic inductance. In our recent work using F treatment technology to achieve E-mode in the integrated cascode GaN transistor ($V_{TH}$ = +2 V) (Figure 2), we demonstrated a reduction in turn-on and turn-off energy losses of 21 % and 35 %,

respectively in comparison to a discrete GaN E-mode transistor under 200 V hard switching conditions [9]. The immediate challenge is to achieve a reliable E-mode technology with $V_{TH}$ greater than +2 V.

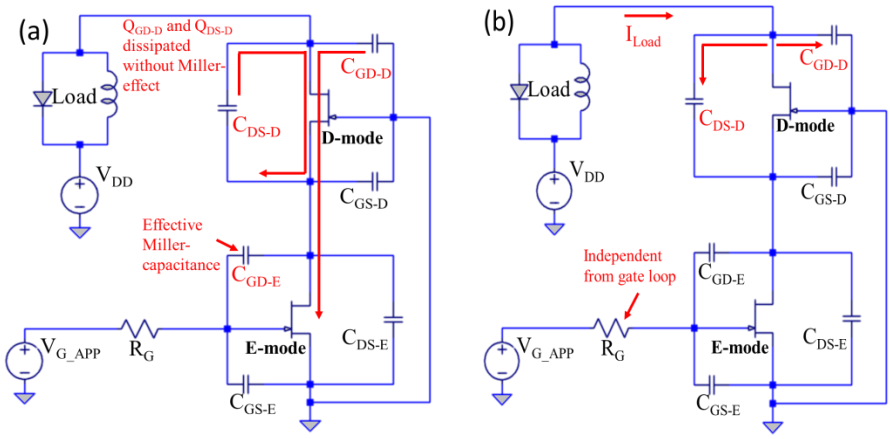


Figure 1. Charging and discharging paths of the output capacitance in the cascode device during (a) turn-on and (b) turn-off processes.

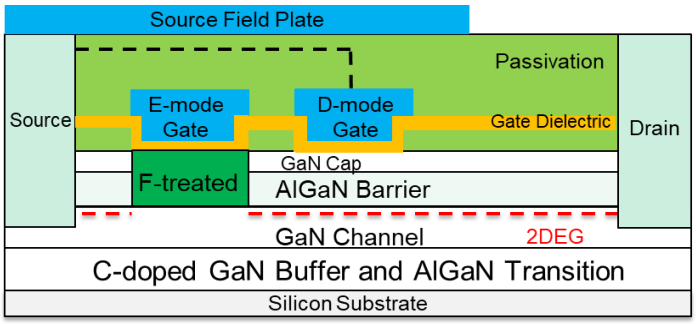


Figure 2: Device structure of GaN integrated cascode transistors.

Matching of intrinsic capacitances between E-mode and D-mode devices in the cascode connection is critical to control the off-state operating voltage of the E-mode device. For hybrid cascodes, adding an external capacitor in parallel with drain-source of E-mode Si MOSFETs has been proposed to provide this matching and prevent the Si device running into avalanche [4], but at the expense of additional package inductances. For GaN integrated cascode transistors, different field plate structures in E-mode and D-mode devices can be employed to achieve capacitance matching. In addition, with the lack of a body diode in the low voltage GaN E-mode device, the integrated cascode devices have the option to trade the off-state operating voltage of the E-mode part for a faster switching speed, without the avalanche loss.

## Concluding Remarks

Monolithically integrated GaN cascode HEMTs open up new opportunities to achieve high efficiency power devices in the MHz range. It is however necessary to overcome both problems with the magnitude of $V_{TH}$ of the E-mode and the mismatch of D-mode and E-mode devices to realise the full potential of integrated GaN cascode HEMTs.

## Acknowledgements

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# 18 - Converter Topologies in GaN

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**Status**

The commercialization of 600V GaN power devices, including the cascode-based FETs and the enhancement mode FETs, has enabled large scale R&D effort in academia and industry [1] to evaluate the impact on converter design and performance. Compared with the best 600V Si super-junction (SJ) MOSFET, the input figure of merit ($R_{on}$·$C_{iss}$) of 600V GaN FET has been improved by about 20 times, the output figure of merit ($R_{on}$·$C_{oss}$) has been improved by about 5 times while the reverse recovery figure of merit ($R_{on}$·$Q_{rr}$) has been improved by more than 40 times [1]. These revolutionary improvements make GaN devices ideal for high efficiency and high density power supply design, especially for applications where the DC link voltage is around 400V. Many converter topologies exist that can take advantages of the improved device performance by directly replacing Si SJ MOSFETs with GaN FETs, operating at the same switching frequency or at an increased frequency. Example topologies include the active-clamped flyback converter (Fig. 1 (a)) for universal AC/DC adapter which can use GaN devices in the primary side [2]; the soft-switched isolated DC/DC converters, such as LLC resonant converter, Phase-Shift-Full-Bridge (PSFB), Dual-Active-Bridge (DAB), etc., which use the GaN devices in the primary side or both sides [3]. Many designs explore the ability to push the switching frequency to much higher value than the Si-based ones, achieving ultra-high efficiency and density. Some topologies are rarely used in the past, limited by the severe reverse recovery issue such as large $Q_{rr}$ and high recovery di/dt in the Si SJ MOSFET. However, by using the GaN devices where the reverse recovery $Q_{rr}$ is pretty much zero due to the absence of any minority carrier injection, some of these topologies become feasible and have demonstrated extraordinary performance. Examples include the 99% efficient totem-pole PFC (Fig. 1 (b)), full-bridge (FB) photovoltaic (PV) inverter (Fig. 1 (c)) and the 98.8% efficient hard-switching isolated full-bridge converter [4-7]. In addition to the circuits, improved modulations also make the same topologies perform even better. The continuous conduction mode (CCM) totem-pole power factor corrector(PFC) and FB PV inverter work with hard switching and constant frequency, typically only in the range of 50~100kHz. However, the triangular current mode (TCM) totem-pole PFC and FB PV inverter can work with soft switching and variable frequency in the range of 100 kHz~3MHz [4, 5, 7]. With these GaN-based topologies, the efficiency and the power density are significantly improved compared with the Si-based solutions.

**Current and Future Challenges**

The main challenges for the GaN based converter topologies are:

1. The optimization of the switching frequency: The switching frequency determines the frequency related loss and the size of the passive components. The optimization of the switching frequency is an important research topic.

2. Selection between hard switching and soft switching: Constant frequency hard switching modulation has low control complexity and high reliability, while the size of the passive components is large. Variable frequency soft switching techniques can reduce the size of the passive components due to the high frequency. However, the control complexity is significantly increased due to the variable frequency operation. The selection between hard switching and soft switching is a challenge.

3. The reduction of the differential mode (DM) filter size for soft-switched topologies: Soft-switched topologies, such as the TCM totem-pole PFC and the TCM inverter, have large input current ripples. It is still challenging to dramatically reduce the DM filter size even the frequency is high.
4. New converter topologies in GaN: To take full advantage of the GaN device, developing new topologies and new power delivery architecture is a needed new challenge

**Advances in Science and Technology to Meet Challenges**

The progresses in addressing and investigating the previously mentioned challenges are:
1. The optimization of the switching frequency: The optimization of the switching frequency depends on the requirements of the application. For applications focusing on the high efficiency, lower frequency is preferred. For the applications requiring high density, such as the Google Little Box challenge, higher frequency is preferred.
2. Selection between hard switching and soft switching: Due to the elimination of the turn on loss, the zero-voltage-switching (ZVS) converters can realize high switching frequency. Thus, the size of all the passive components, especially the EMI filters, can be reduced. In addition, the slower dv/dt of the ZVS converters also reduce the EMI noises. The soft-switched converters have demonstrated ultra-high density, over 145W/inch$^3$, on the totem-pole PFC and FB PV inverter [4, 5, 7].
3. The reduction of the DM filter size for soft-switched topologies: Multiphase interleaved soft-switched topologies (Fig. 1 (d)) can solve this challenge [8]. The interleaving technologies significantly reduce the current ripples. The DM filter size is optimized, too.
4. New converter topologies in GaN: The upcoming GaN-based AC switch could enable a number of new high-performance topologies. The resonant converter with GaN AC switch (Fig. 1 (e)) not only realizes high efficiency, but also achieves the wide input and wide output voltage conversion [9]. A new single stage solution, the isolated AC/DC DAB converter with GaN AC switches (Fig. 1 (f)) on the primary side, can be used for on-board charger and battery system with significantly improving the system efficiency [10].

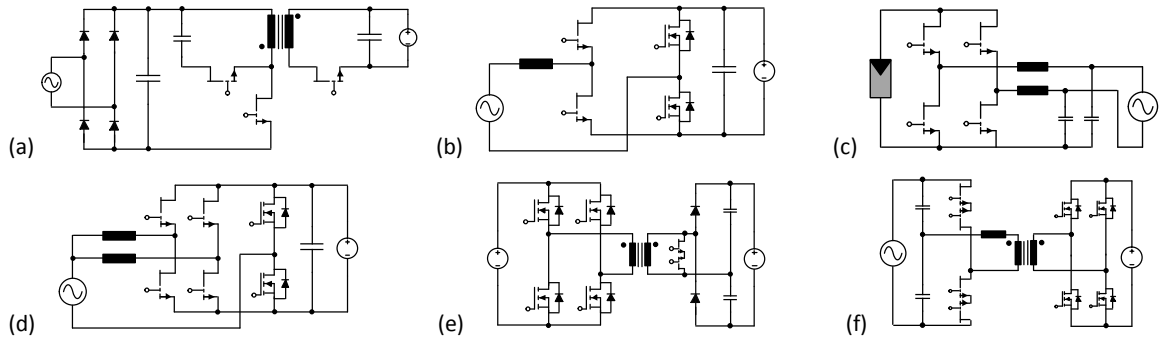


**Fig. 1.** Topologies discussed previously with GaN FETs: (a) active clamped flyback; (b) totem-pole PFC; (c) FB PV inverter; (d) two-phase interleaved totem-pole PFC; (e) resonant converter with GaN-AC switch at the secondary side; (f) AC/DC DAB with GaN AC switches

| | Frequency | Efficiency | Power density |
|---|---|---|---|
| 65W active-clamp Flyback Charger [2] | 1MHz | 93.0% (full load) | 25W/inch$^3$ |
| 2.4kW FB isolated DC/DC [6] | 50kHz | 98.6% (full load) | 116W/inch$^3$ |
| 1kW TCM two-phase totem-pole PFC [4] | 4MHz (max) | 98.7% (full load) | 220W/inch$^3$ (no bulky capacitors) |
| 2kW multiphase TCM FB PV inverter [7] | 35~240kHz | 95.4% (CEC) | 150W/inch$^3$ |

Table 1. Benchmark of the state of the art GaN-based converters

**Concluding Remarks**

The GaN-based converters have demonstrated extraordinary performance. As shown in Table 1, the power density and the efficiency have been improved significantly based on these benchmark GaN

converters. With the innovation and the optimization of the converter topologies in GaN, the density and efficiency will be further improved. Even though the cost of the devices is increased, the high density and efficiency will reduce the system cost in the future.

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# 19 – Fast switching with GaN and dynamic on-resistance from application view-point

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**Status**

GaN semiconductors have gained popularity in GHz applications, while power electronic applications are still in the early stages of development. The focus of this section is the application of GaN devices for power electronics with device breakdown voltages from 400V up to 900V. Applications of GaN transistors include uni- and bidirectional DC/DC and AC/DC converters, inverters for high-speed motor drives as well as inductive heating and wireless power transmission (Fig. 1). High system efficiencies and power densities are the main requirements for these applications. This is enabled by low conduction and low switching losses from a semiconductor point of view. GaN transistors allow both aspects. Low conduction losses are achieved by GaN transistors with low area-related on-resistance compared to Silicon (Si) and Silicon Carbide (SiC) counterparts. Low switching losses are achieved by fast switching between the on- and off state. GaN transistors show a purely capacitive behaviour due to their unipolar device characteristic, while Si- and SiC-MOSFETs lack from reverse recovery charge due to intrinsic bipolar body diodes [1]. Regarding the switching speed of the drain-source-voltage, 5-20 V/ns is considered as "fast" for Si devices. Slew rates are typically limited to the range of 1-16 V/ns in motor drive applications [2]. In contrast, optimized SiC and GaN circuits allow up to 200 V/ns and 500 V/ns, respectively [3,4]. The possibility of ultra-fast switching exceeds the boundary conditions of most applications. However, operating two 600V transistors in half-bridge configuration for e.g. hard-switching bidirectional DC/DC converters, Si-MOSFETs are not suitable due to their bipolar body diode. SiC-MOSFETs with orders of magnitude lower reverse recovery charge are suitable, but higher system efficiency can be achieved with unipolar GaN-transistors.

**Current and Future Challenges**

The main challenges for GaN transistors in power electronic applications are:

1. Normally-off characteristic: System developers require normally-off devices because of safety reasons, while the realization of normally-off device characteristics is still a main research topic (section 8).
2. Dynamic on-resistance: Some GaN transistors show dynamic on-resistance. After turn-on, their on-resistance $r_{ds,on}$ is higher than the static value $R_{ds,on,typ}$ and decays over time until it reaches the static value $R_{ds,on,typ}$. The main reason is a physical phenomenon called "trapping" due to high electric-field strengths in the off-state, when the blocking voltage is applied (drain-source-voltage is e.g. 400V) [5,6]. Fig. 2 shows a comparison of three devices from different manufacturers. GaN #1 shows the highest dynamic on-resistance with a ratio of $r_{ds,on}$ ($t_1$)/ $R_{ds,on,typ}$ = 4.3 while it decreases to 2.5 after 300 µs. For example, the turn on time of a DC/DC converter operating at a moderate switching frequency of 100 kHz and a duty cycle of 50 % is only 5 µs. This results in an effective on-resistance of 4.2·$R_{ds,on,typ}$ for the system design and therefore in higher losses and lower efficiency. The influence of this issue becomes even worse when the switching frequency is increased.

3. Reverse conduction capability: In half-bridge configuration, reverse conduction capability is required for negative drain currents. Though there is no intrinsic body-diode in GaN transistors, current can flow from source to drain. However, the source-drain-voltage drop $v_{sd}$ increases with decreasing gate-source-voltage $v_{gs}$. This is valid for all commercially GaN transistors known to the authors. For example, for some GaN transistors, the forward voltage drop $v_{sd}$ is 8 V or higher, when the gate is kept in the off state with $v_{gs}$ = -5 V.
4. Parasitics, packaging, controllability and EMI: In general, the influence of parasitic inductances and capacitances is the same as with Si and SiC circuits. This situation worsens for GaN transistors due to tighter gate voltage margins compared to Si and SiC devices which can lead to device destruction and phase leg short circuits. In general, fast switching semiconductors enable higher power densities, but require additional filters for electromagnetic interference (EMI), also.
5. Reliability issues and countermeasures are discussed in section 8.

**Advances in Science and Technology to Meet Challenges**

The progresses in addressing and investigating the challenges from the preceding subsection are:

1. Normally-off characteristic: This challenge must be solved at the level of the device technology. Alternatively, a cascode circuit with normally-off behaviour can be realized by using a normally-on high-voltage GaN transistor and a normally-off low-voltage Si transistor. However, recent studies have shown that the switching speed of cascodes is barely adjustable without additional components inside the cascode [7]. The necessity of an additional Si transistor for the cascode is another disadvantage of the cascode compared to normally-off GaN transistors. All commercial GaN transistors at the time of this study show normally-off behaviour by intrinsic normally-off characteristic or cascode configuration.
2. Dynamic on-resistance: As can be seen in Fig. 2, the GaN transistor #3 shows no dynamic on-resistance for the full time scale. The manufacturer applies an additional p-GaN-layer to provide the injection of holes from the drain and dynamic on-resistance can be prevented successfully [8]. However, other manufacturers still face the challenge of the dynamic on-resistance which is also indicated by significantly increased scientific activities regarding this topic.
3. Reverse conduction capability: The high forward voltage drop in reverse conduction mode of GaN transistors can be avoided by using synchronous rectification. This means to turn the GaN transistor on shortly after the current has commutated to the transistor in reverse direction. In contrast to a diode, the transistor has to be turned off before the complementary transistor of the half-bridge turns on. Otherwise, phase leg short circuits may occur which lead to immediate destruction of both switches. In this case, special protection circuits are necessary. Additionally, the adaption of the dead-time between the half-bridge switching actions helps to increase the efficiency even more.
4. Parasitics, packaging, controllability and EMI: Integration of GaN transistors and gate drivers within one package will minimize the effects of parasitic circuit elements. The next step is to integrate GaN transistors and drivers within one chip which has already been demonstrated. To gain the most advantage for power electronic systems, the integration of GaN transistor, gate drivers, auxiliary circuits and DC link filters within one device will allow minimum parasitic

circuit inductance and high switching speeds. The EMI can also be improved by the enclosure on low footprint as well as novel active filters.

**Concluding Remarks**

GaN transistors have evolved dramatically in the last ten years and enable power electronic systems with highest efficiencies due to their unipolar device characteristic and low area-specific on-resistance (Fig. 2). The issues discussed in this section will diminish with further research similar to the advances with Si and SiC devices in the last 70 and 20 years, respectively.

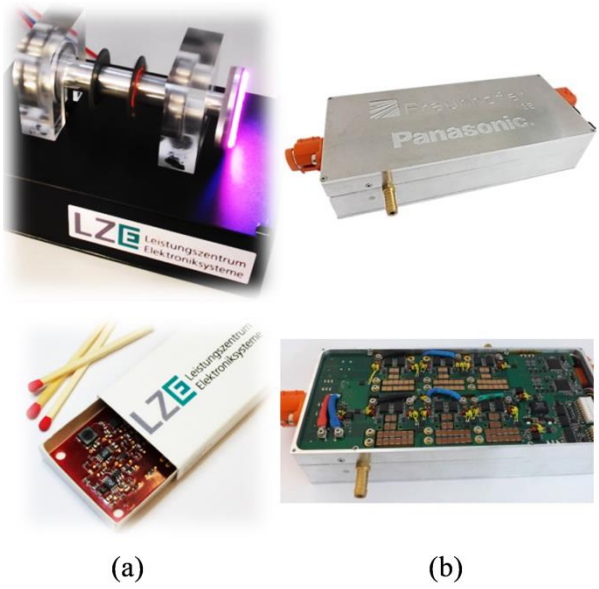


**Figure 1**. (a) Demonstrator of 20 W inductive power transmission for high-speed rotating applications (top) and corresponding matchbox-sized GaN power electronics (bottom) [9]. (b) Demonstrator of 6 kW on-board charger for electric vehicles with 3 kW/l power density (top) and power electronics setup (bottom) [10].

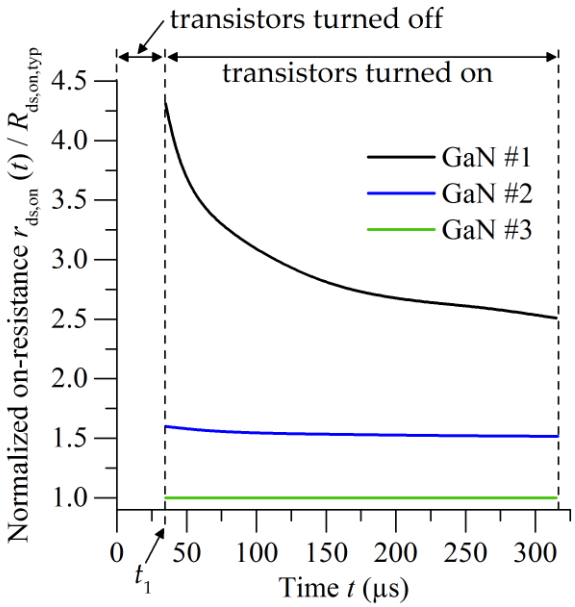


**Figure 2.** Measurement of the on-resistance of three GaN transistors from different manufacturers. The drain-source voltage in the off-state is kept at 50 % of the drain-source breakdown voltage for 20 seconds.

**Acknowledgements**

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# The 2018 GaN power electronics roadmap

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## Abstract

GaN is a compound semiconductor that has a tremendous potential to facilitate economic growth in a semiconductor industry that is silicon-based and currently faced with diminishing returns of performance versus cost of investment. At a material level, its high electric field strength and electron mobility have already shown tremendous potential for high frequency communications and photonic applications. Advances in growth on commercially viable large area substrates are now at the point where power conversion applications of GaN are at the cusp of commercialisation. Nevertheless, there are still many more opportunities for enhancement to be explored. This roadmap comes at a crucial time to consolidate recent developments and predict future requirements of materials, growth, device architectures and reliability that underpin the manufacturing challenges in real-life applications of GaN in power circuit applications.

## Introduction

Silicon-based Insulated Gate Bipolar Transistors (IGBTs) and Superjunction MOSFETs are fundamental components of present day power electronic systems for the conversion, control and conditioning of electrical energy, from generation to the point of load. If silicon devices were to be replaced by a more efficient semiconductor such as GaN, compact converters with ultra-high density can be designed only because the breakdown strength and electron mobility in GaN are respectively 10x and 2-5x higher. These basic material properties translate into smaller devices leading to higher frequency of operation, lower switching losses, and reduction in the component count and size of passives. This was demonstrated by over 100 hours testing by NREL of 2kW GaN inverters designed by the Red Electrical Devils, winners of the Google Little Box Challenge in 2015. Compact modules translate directly into lower weight, volume and cost. Coupled with increasing concern and government commitment to global warming, there are now strong commercial and legal pressures to accelerate adoption of these advantages into production systems.

Applications are now emerging that have no other practical solution than GaN. Take for example the automotive industry: GaN is the semiconductor of choice for power converters throughout vehicle electronics apart from the final drive inverter. Even here, there is now a very strong push to create production devices capable of switching as much as 100 Amps at 900 Volts. The advent of mass adoption of electric vehicles will in turn accelerate two other major markets that depend on highly efficient high-density power converters. Charging electric cars will require intelligent switching in the local power distribution grid. Simultaneously, IT infrastructure to support autonomous driving will create another massive parallel requirement for efficient power conversion.

GaN has evolved to the point where the cost of the transistor itself is no longer considered as the key driver in system cost. The novelsolutions that the technology facilitates, provides savings in both manufacturing and running costs. Focus will come to bear on manufacturing parts in volume that will finally demonstrate the predicted price learning curves and focus attention on those research avenues that provide the fastest route to manufacturing maturity.

There has been considerable diversification of approaches over the last decade into addressing some of the problems with GaN. The roadmap presents a snapshot, highlighting consolidation of this research into substrates, gate architectures, device and circuit topologies and their reliability. We expect growth and reliability to be greatly accelerated by the first phase of volume production, but this is just the start. A parallel critical path in the technology roadmap highlights that the full material benefits of GaN cannot be achieved via existing product design approaches using slower silicon gate drivers. Novel circuit approaches, better companion passive devices and packaging will be the new frontier for research to addresses the thermal, electrical and electromagnetic design of a converter system. Particularly exciting is the potential and challenge of integration, on a chip where transistors are capable of even out-switching the delays of signal paths.

We hope you enjoy this peek into an enticing perhaps all-GaN future!

# 1 - Manufacturing Challenges of GaN-on-Si HEMTs in a 200 mm CMOS fab

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**Status**

GaN is anticipated to be the next generation power semiconductor. With a higher breakdown strength, faster switching speed, higher thermal conductivity and lower on-resistance ($R_{on}$), power devices based on this wide-bandgap semiconductor material can significantly outperform the traditional Si-based power chips. As such, GaN-based power devices will play a key role in the power conversion market within battery chargers, smartphones, computers, servers, automotive, lighting systems and photovoltaics.

In absence of viable low-cost GaN bulk substrates, GaN is grown on a variety of substrates, the most popular being sapphire, silicon carbide (SiC) and silicon (Si). Si substrates have become attractive for GaN growth because of their larger wafer diameter (200 mm and higher) though the large mismatch in lattice constant and coefficient of thermal expansion (CTE) imposes epitaxy challenges, especially for larger Si substrate sizes. Moreover, GaN devices are naturally normally-on or depletion mode (d-mode) devices whereas, to replace commercially available Si power devices, the GaN devices should be normally-off or enhancement-mode (e-mode) devices. Furthermore, GaN devices should be fabricated by a low-cost, reproducible and reliable production process. While e-mode operation can be readily achieved by adding a p-doped GaN layer under the gate, hereby lifting the conduction band at equilibrium and resulting in electron depletion, the ability to manufacture GaN-on-Si power devices in existing 200 mm Si production facilities offers further cost competitiveness to the Si power technology.

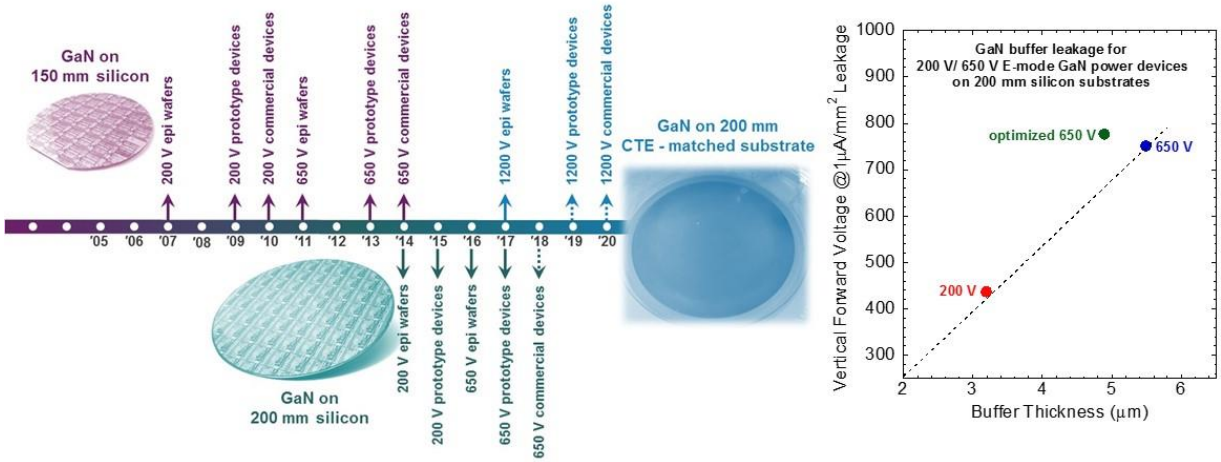


**Figure 1.** Left: timeline for 200 V, 650 V and 1200 V GaN-on-Si epi wafers, prototype and commercial enhancement-mode power devices. Right: buffer leakage at 25˚C of imec's 200 V (red) and 650 V (blue and green) GaN-on-Si epi wafers after full processing in the 200 mm CMOS fab.

Initially, the development of GaN-based technology focused on high voltage (200 V and 650 V) power-switching applications. First commercial 200 V e-mode GaN devices, fabricated on 150 mm Si substrates, were released in 2010 and first 650 V commercial devices followed in 2014 (Figure 1, left). After first developing the technology on 100 mm [1, 2], and later 150 mm wafer sizes using Au-free metallization schemes [3], imec has been pioneering 200 mm GaN-on-Si technology with first GaN 200

V epitaxy [4] and devices in 2014 [5-9]. The imec 200 mm GaN-on-Si e-mode transistor and diode platform was recently extended and qualified for 650 V applications. Today, the focus is on the technology development for higher level of integration and for 1200 V applications using 200 mm CTE-matched polycrystalline AlN substrates.

**Current and Future Challenges**

Because of the much higher CTE of GaN compared to Si, the GaN in-film stress during epitaxial growth needs to be tuned compressive to compensate for the tensile stress during cool down. The use of 1.15 mm-thick 200 mm Si substrates is beneficial to reduce wafer warp during growth and hence avoiding wafer cracking. Without significant hardware changes and lowering the robot speed of some handling systems, the thicker and heavier GaN-on-Si wafers can be processed in the standard imec CMOS fab. The warp specification of 50 μm is sufficiently low to avoid chucking issues on electrostatic chucks. Prior to the fab introduction, the 200 mm GaN-on-Si wafers are tested for mechanical robustness, hereby reducing the wafer breakage during processing to less than 1%. After epitaxy, Ga and Al contamination on the wafer backside is unavoidable. Since Ga is a p-type dopant for Si, one of the major concerns of processing GaN wafers in a CMOS fab is Ga cross-contamination. The Ga and Al backside contamination after epitaxy is effectively removed by an in-house developed $HF/H_2O_2$-based cleaning procedure, hereby reducing the contamination level of the wafer backside and bevel to below $10^{11}$ at/cm$^2$. Moreover, imec's e-mode pGaN process flow contains (Al)GaN dry etch steps. A first one to dry etch the pGaN layer selectively to the AlGaN barrier layer, and a second to recess the AlGaN barrier in the ohmic contact areas. Since conventional F-containing cleaning recipes of the dry etch tools can form non-volatile $GaF_x$ species (i.e. $GaF_x$ is not volatile below 800°C), a $Cl_2$-based clean that forms volatile $GaCl_3$ at ~200°C is used. This cleaning procedure effectively and reproducibly maintains the Ga contamination level in the dry etch tools well below the maximum allowed level.

Finally, since Au is a rapidly diffusing contaminant in Si that deteriorates the minority carrier lifetime, the GaN metallization schemes need to be Au-free. Because of the high bandgap and the absence of explicit doping of the epilayers, especially the development of Au-free ohmic contacts is challenging. By using a Si/Ti/Al/Ti/TiN ohmic metal scheme and decreasing the alloy temperature to 565˚C, the ohmic contact resistance could be lowered to 0.3 Ω·mm with excellent reproducibility and uniformity.

**Advances in Science and Technology to Meet Challenges**

Because the breakdown field of the Si substrate is ten times lower compared to GaN, the breakdown voltage of the power devices is dictated by the GaN buffer thickness. In Figure 1 (right) the vertical buffer breakdown voltage (at 1 μA/mm$^2$ leakage) is plotted versus the buffer thickness. Straightforward extension of the 3.2 μm-thick 200 V buffer (red) to 5.5 μm for 650 V applications (blue) was resulting in low wafer yield: the yield related to wafer breakage in the mechanical screening test was reduced from 90% for 200 V to 77% for 650 V. This issue was tackled by implementing Si substrates with high boron doping (0.01 Ω·cm resistivity) hereby increasing the mechanical wafer strength, and by developing a new buffer concept with reduced thickness (4.9 μm, green) that resulted in an equally high buffer breakdown voltage while maintaining the low buffer dispersion, and increasing the wafer yield for 200 V applications to 99% and to 97% for 650 V applications.

By optimization of the cleaning and dielectric deposition conditions, together with the field plate design, state-of-the-art 650 V 36 mm gatewidth power devices with 2.1 V threshold voltage (at maximum transconductance), 13 Ω·mm $R_{on}$ and 8 A output current (Figure 2a and b) were obtained

on 200 mm wafer size and processed in a standard CMOS wafer fab. Moreover, the devices exhibit dynamic $R_{on}$ dispersion below 20% (10 μs on, 90 μs off) up to 650 V over the full temperature range from 25°C to 150°C (Figure 2c).

For 1200 V power applications, imec is working on using polycrystalline AlN (poly-AlN) substrates that have a better CTE-match to GaN. In this approach, a thin crystalline Si layer is transferred to a 200 mm poly-AlN substrate. This new technology is promising to go beyond the current technology limitations, because it is possible to grow thicker, higher quality GaN buffers on 200 mm substrates with a standard thickness of 725 μm. Imec has already demonstrated the CMOS-compatibility of these substrates in terms of contamination and wafer handling [10]. Furthermore, first high quality transistors have been processed illustrating the high promise of this new approach.

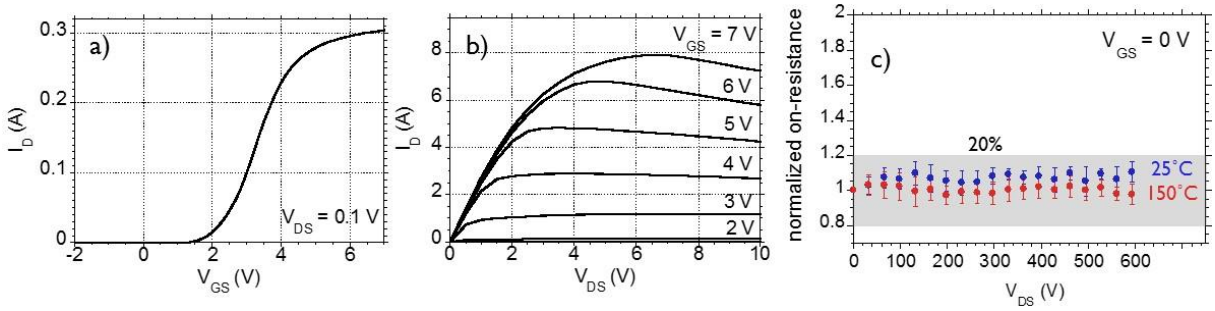


**Figure 2.** (a) Transfer and (b) output characteristics of a typical 36 mm gate width 650 V e-mode power device, and (c) the dynamic $R_{on}$ device dispersion. The devices were fabricated in imec's 200 mm CMOS fab.

## Concluding Remarks

GaN technology offers faster switching power devices with higher breakdown voltage and lower on-resistance than Si, making it an ideal material for advanced power electronic components. For cost competitiveness, GaN power devices are preferably fabricated on large diameter Si substrates in existing Si CMOS fabs. Due to the large mismatch in lattice constant and thermal expansion coefficient, the epitaxy of GaN on large diameter Si substrates is very challenging. Imec has demonstrated for the first time that is possible to manufacture 200 V and 650 V GaN-on-Si e-mode devices in a 200 mm CMOS fab. For 1200 V applications, it is proposed to transfer the technology to 200 mm Si-on-poly-AlN substrates, which is CTE-matched with GaN. This substrate technology allows for thicker GaN buffers, which is needed to reach 1200 V and beyond, and was also assessed to be CMOS-compatible in terms of contamination and tool handling.

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# 2 – Epitaxial Lift-Off of GaN and Related Materials for Power Device Applications

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**Status**

GaN and other III-N compound semiconductors have had an enormous impact on optoelectronics—with the widespread adoption of LEDs, lasers, and solar-blind photodetectors—as well as RF electronics for both consumer wireless infrastructure and military communications and sensing. The continuing advance of III-N electronics promises to bring this revolution also into the power electronics space. With power device concepts based both on extensions of conventional lateral FET designs, as well as concepts based on vertical transistor designs, GaN and related materials promise to dramatically enhance the performance, efficiency, and ubiquity of sophisticated power management and control functions. Advances in growth and substrate technologies for achieving high-quality material, along with improved device designs, promise to enable continued increases in device performance. In addition, novel processing techniques are also promising to provide significant performance, cost, and integration improvements. Among these processing-related advances, techniques that enable epitaxial lift-off and substrate transfer are especially attractive. Epitaxial lift-off has been demonstrated for optoelectronic applications (see e.g. [1], [2]), and offers the potential for improved light extraction, smaller device form factor, and ultimately more flexible displays as well as sensors for emerging applications such as wearables. In the power application space, epitaxial lift-off can enable substantial increases in thermal performance (through improved heat removal), electrical performance (through lower resistive losses and higher breakdown voltages), economics (through more efficient materials utilization, die size reduction, and substrate reclaim and reuse), and enhanced integrability with other electronics technologies. A range of epitaxial lift-off technologies for GaN and related materials have been demonstrated, including selective wet etching of ZnO layers [2], dry etching of epitaxial $Nb_2N$ layers by $XeF_2$ [3], mechanical exfoliation and separation using graphene or BN layers [4, 5], and band gap selective photoelectrochemical etching based on wet-chemical etching of lower-band gap materials such as InGaN [1, 6, 7, 8]. In addition to the mechanism by which the lift-off occurs, epitaxial lift-off processes may be distinguished by whether they lift off a single device (Fig. 1(b)) or small circuit (e.g., [1], [3]), or seek to lift off a larger film (Fig. 1(a)) either for subsequent processing into devices (e.g., [2], [4], [5]) or after fabrication of the devices is largely complete (e.g. [7, 8]).

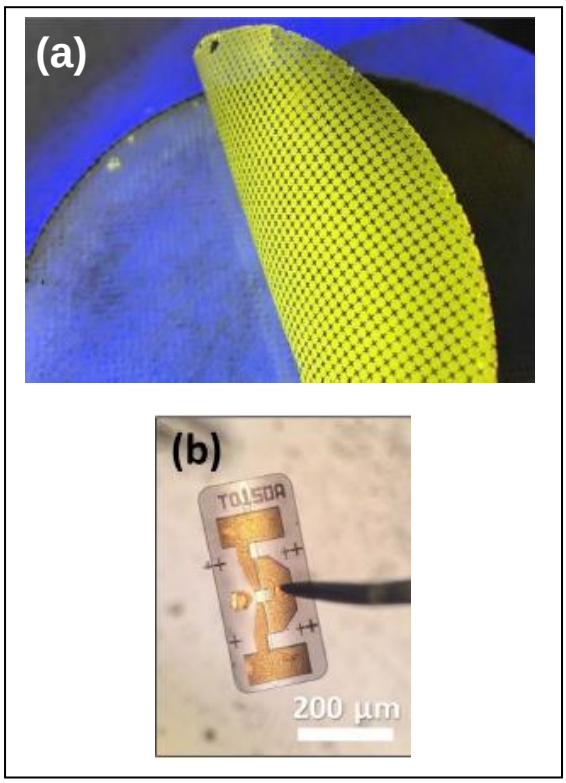


**Figure 1.** (a) Large-area (100 mm wafer) epitaxial lift-off of GaN-based epitaxial device layers achieved using band-gap selective photoelectrochemical wet etching of an InGaN [7]; (b) single-die release of a GaN-based device using dry etching of $Nb_2N$ with $XeF_2$ [3].

**Current and Future Challenges**

Advances in power electronics are poised to radically alter the design and implementation of electronic products and systems; ultimately, sophisticated power electronics and circuit topologies for enhanced efficiency and power-control capability could become ubiquitous if the key technological and economic challenges can be solved. Realization of this vision is currently constrained by cost, device performance, and integration challenges—all of which can be addressed by epitaxial lift-off. Due to the wide diversity of potential applications there is unlikely to be a single optimal solution; instead, we can expect different approaches to benefit different application segments. For example, for modest voltage and current requirements for which lateral devices (e.g. MISHEMTs) provide sufficient performance and economic benefit, use of conventional lattice-mismatched substrates such as SiC, sapphire, or Si is appropriate; epitaxial lift-off can then be used to accomplish substrate transfer for improved thermal or breakdown performance (see e.g. [9]), as well as the potential for reusing high-cost substrates (e.g. SiC) [3]. For applications where high currents and material-limited breakdown voltages are required, as well as applications where economics dictates a high areal current density, vertical device structures offer inherent advantages. However, these devices also place additional demands on material quality; while high dislocation densities are often tolerable in optoelectronic and lateral electronic nitride devices, these defects significantly compromise the performance of vertical devices. This can be addressed by homoepitaxial devices on bulk GaN substrates, but this in turn places more stringent demands on the epitaxial lift-off approach to avoid the generation of dislocations. The economic benefits of epitaxial lift-off from bulk GaN substrates are substantial, given their high cost and small diameter. In addition to substrate reuse, thermo-electric modelling indicates that direct bonding of lifted-off vertical FETs to a heatsink could enable die size reduction by more than 50% compared to devices on bulk GaN substrates [8]. Of the current techniques, only band gap selective photoelectrochemical etching with pseudomorphic InGaN release

layers has been demonstrated to maintain fully coherent single-crystal material from the bulk substrate through the device epitaxial layers, and so may provide a unique solution to achieving epitaxial lift-off of vertical devices on bulk GaN substrates. Reuse of bulk GaN substrates after lift-off has recently been demonstrated with lift-off of GaN pn junctions (Fig. 2) demonstrating a pathway to improved economics; future efforts will be needed to fully realize the thermal and integration benefits.

**Advances in Science and Technology to Meet Challenges**

To address the challenges and fully realize the benefits of epitaxial lift-off as an enabling technology for high-performance, low-cost, ubiquitous power electronics, significant technological challenges must be overcome. For material-quality sensitive applications such as vertical devices, additional development of lattice-matched or pseudomorphic release layers is an important future direction. Current demonstrations have been based on the use of InGaN release layers [1, 6, 7, 8]; while this approach has been successfully demonstrated for both single-die release and lift-off of large areas (> 100 mm wafer), the lateral etch rate is modest and the surface morphology of the N-face GaN is not yet easily controlled due to limited etch rate selectivity. Additionally, the use of pseudomorphic release layers such as InGaN have been reported to influence the mechanical behaviour of released structures [10]. Development of strain-control strategies or deposition of alternative release layer materials with basal plane lattices commensurate with the GaN devices are areas for future development and exploration. Another area that is largely unexplored to date is that of novel packaging and bonding strategies to leverage the unique features of devices fabricated using epitaxial lift-off. The thermal performance of ultra-thin devices has been projected [8], but experimental validation and–in particular—optimization for the unique characteristics of ultra-thin devices is an area for additional development. Heterogeneous integration of lifted-off devices with conventional electronics, and packaging of lifted-off devices for emerging applications such as flexible or ultra-thin form factors is another area where substantial additional innovation is needed. Finally, the reliability of lifted-off devices is an important topic, but one that has not yet been addressed due to the nascence of the technology.

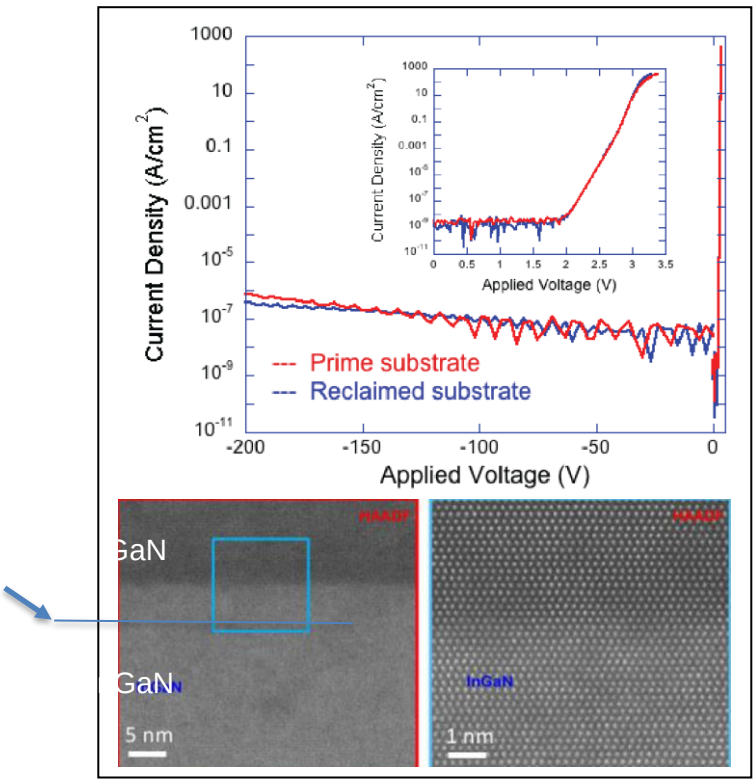


Figure 2. (a) Measured current-voltage characteristics of typical GaN vertical PN junction diodes on prime bulk GaN substrate and on a reclaimed substrate (i.e., after growth, lift-off, repolish, and a second device growth and fabrication sequence, validating that device performance on epi-ready prime and reclaimed/reused substrates is nearly indistinguishable. (b) TEM image showing pseudomorphic InGaN release layer growth [7].

## Concluding Remarks

Epitaxial lift-off is an emerging technology that is poised to be of significant benefit to the developing field of III-N based devices, and in particular to high-performance, cost-effective power electronics. The improvements in electrical and thermal performance, economic benefits derived from reduced die size and bulk GaN or SiC substrate reuse, and potential for enhanced heterogeneous integration with other electronics and packaging technologies makes epitaxial lift-off appear promising for advancing power electronics across a broad range of applications.

## Acknowledgements

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# 3 – GaN-on-Si 200 mm for power devices

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**Status**

The main objective in the LETI power electronic roadmap is the miniaturization of power converters to increase the energy efficiency of the systems while reducing the cost. It is also important to improve reliability and ensure operation at higher temperatures (300 °C), with the markets of automotive (EV and HEV) and motor drives for industrial tools being targeted. To achieve these objectives for power convertors from a few Watts to several hundred kW, it is essential to increase their operating frequency [1]. GaN-on-Si power devices are capable of responding to these requirements because GaN allows high frequency switching (several MHz) and a higher power density than silicon (10 times greater), although these solutions must be implemented at the system level in order to fully benefit from the materials properties. Furthermore GaN on 200 mm Si enables CMOS compatible technology leading to lower cost and improved robustness of the processes.

LETI has chosen to develop MOS-HEMT GaN architecture, fabricating "Normally-Off" devices which give functionality similar to a classic silicon based MOS. To take full advantage of these devices, a route towards monolithic solutions for low and mid power applications and a route towards system in package is promoted at LETI, fig. 1, with 5 main axes of work: epitaxy, devices, passives, co-integration, and system architectures. Here we will focus on the device roadmap.

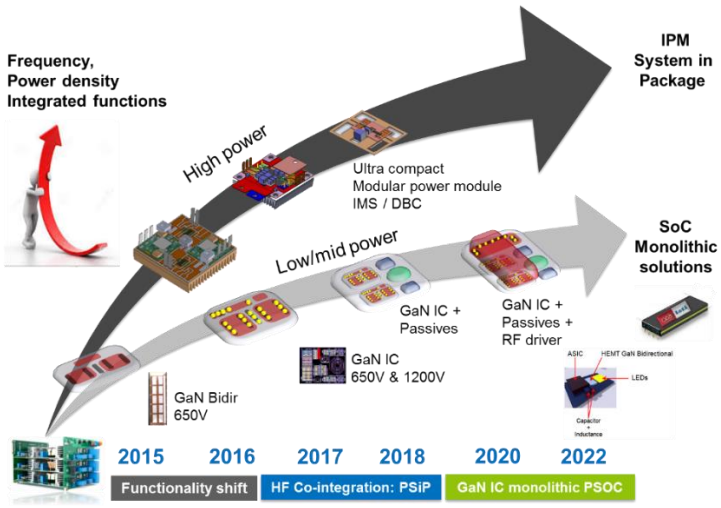


**Figure 1.** Power systems roadmap at LETI. An SOC (system on chip) route towards monolithic solutions is important for miniaturization for low and mid power solutions. For higher voltages, an ultra-compact power module is preferred [2]

**Current and Future Challenges**

Adoption of GaN in the industry requires high performance, high reliability devices produced at low cost. For automotive applications, GaN transistors of 1200 V - 50 A and 650 V - 200 A are targeted. Current requirements are a $R_{onS}$ below 1 mohm/cm², Fig. 2, with an $R_{dyn}$ of no more than 10 % of the $R_{onS}$, meaning low losses [4]. The epitaxy is expected to improve in several ways: Firstly, a constant

improvement in the buffer layers and active layers to decrease the dislocation density, even though this has not been proven to be essential for high quality HEMT performance, and a reduction in point defects which cause trapping; Secondly, a vertical leakage current lower than 1µA/mm$^2$ at 150°C and thirdly improvements and optimisations in the design of the epi stack, such as integration of back barriers to improve confinement of the free carriers in the potential well. Of course, all this has to be implemented while maintaining a wafer bow < 50 µm for a silicon wafer thickness of 1 mm maximum to enable the process in standard 200 mm tools [3].

The most developed structure to make normally-off GaN HEMTs is pGaN gate architecture. P-type GaN may have potential work function of up to 7.5 eV which makes pGaN an outstanding gate metal in addition to the depolarization effect for depleting the channel beneath the gate. However this design suffers from a compromise between the threshold voltage and the sheet resistance in the channel and so high positive threshold voltages are difficult to achieve. This is why at LETI we are developing an alternative strategy, the MOS-HEMT. This architecture is a hybrid monolithic device which essentially puts a MOS channel and a HEMT drift layer in series. At the heart of this technology is the MOS gate, which needs to be reliable and robust; a challenge that Si and SiC have already faced in the past.

**Advances in Science and Technology to Meet these Challenges**

These advances required to meet the challenges listed above can be described in five bullet points:

Simulation: to design complex architectures, capture process influence and describe device behaviour, simulations such as TCAD are of major importance. Currently, significant efforts are needed to ensure simulators properly recreate the physics of III-N materials and devices.

Device Characterisation**:** the JEDEC standards are not sufficient to fully qualify GaN-based power devices due to restrictive criteria. Dynamic properties and aging effects, which show common patterns with dielectric aging, are key topics to be understood in order to bring GaN-on-Si products to industrial maturity in mass markets.

Device technology: as discussed above, constant improvements are required in the epitaxy, with in particular improved defect characterization and analysis of their impact on device performance. The understanding of the gate oxide trap passivation will also be a significant scientific and technological challenge. The whole technology has to be CMOS compatible, which brings an additional constraint to GaN power device design, and the potential of GaN on 300 mm Si has to be investigated.

Thermal dissipation: The reduction in size of power devices when using GaN raises the challenge of thermal dissipation. In order to benefit from the full potential of GaN technology, the power density will need to be increased, and so process and packaging will need to be optimised to improve thermal dissipation.

Switching frequency**:** To allow high frequency switching, co-integration is key. Transistors, flyback diodes, rectifiers or drivers are examples of active devices that can be monolithically integrated to reduce parasitic elements and reach high performance converters.

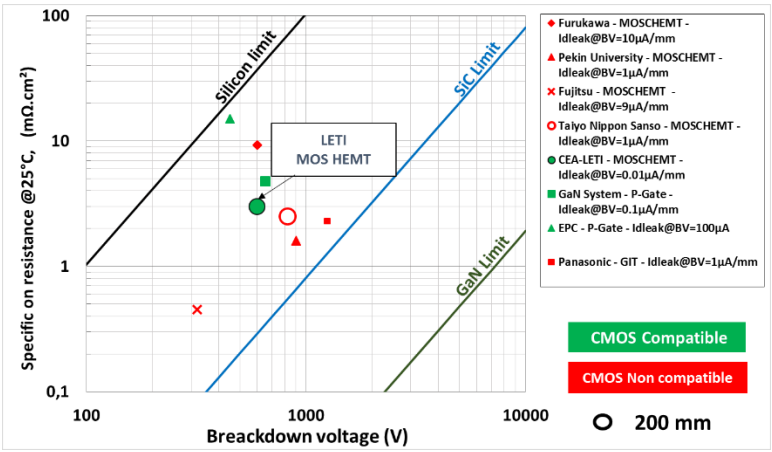


Figure 2. Specific on resistance versus breakdown voltage. Benchmark of different laboratory results versus CMOS or non CMOS compatible technology.

## Concluding Remarks

The use of GaN-on-Si as a substrate for high power transistors is becoming an increasingly common choice, as an affordable large area alternative to expensive bulk substrates. Although there are still significant challenges to be overcome in order to produce high quality devices on these substrates, GaN devices will take full advantage of both the remarkable properties of GaN, and of production in CMOS compatible fabrication plants to achieve high performance and low cost devices.

Furthermore, the development of high power integrated circuits on GaN on silicon wafers will further reduce costs and encourage the use of this technology. With all of these advances, it will surely not be long before GaN-on-Si devices become a huge market as the demand for highly energy efficient convertors becomes ever greater.

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# 4 - Buffer design in GaN-on-Silicon Power devices

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**Status**

Uptake of GaN devices for power applications requires that they can be manufactured in volume at comparable cost to Si components, and with validated device reliability. The key innovation that has made this possible is the ability to grow epitaxial device quality layers of GaN and AlGaN on 6" or 8" (111) Si wafers. Together with the development of Si CMOS compatible device process flows, this has allowed GaN power devices to be fabricated using existing Si fabrication lines with Si and GaN processing occurring in parallel. This section addresses the electrical and material design of the GaN-on-Si epitaxial platform that is now being used to realise HEMT devices for power applications.

GaN HEMTs were first successfully grown on Si in the 1990s, however the epitaxy did not have sufficient breakdown voltage for power applications. GaN-on-SiC RF devices used Fe doping to suppress short-channel drain leakage and increase drain breakdown, representing the first realization that the nominally insulating GaN layer underneath the 2DEG channel is actually electrically active and needs just as much design and optimisation as the upper barrier and channel region. However, Fe doping was found to deliver insufficient breakdown voltage when applied to high voltage power devices. Eventually it was found that a combination of a complex strain relief buffer together with carbon doping to control breakdown could achieve sufficient voltage handling[1]. Unfortunately there continued to be bulk trapping related issues collectively known as dynamic $R_{ON}$ dispersion or current collapse, and their solution has only recently been demonstrated commercially. The reasons for the wide variation in dynamic $R_{ON}$ performance achieved for apparently identical carbon doped epitaxies is only now becoming understood.

**Current and Future Challenges**

Key issues in epitaxial growth of GaN-on-Si are the lattice and thermal expansion coefficient mismatches which make strain management critical. As a result large numbers of defects (>$10^{10}$cm$^{-2}$) are generated, and cracking of the GaN layers can occur on cooling from the growth temperatures (≈1000°C) [2]. The epitaxial layer structure which has been adopted to solve these issues is shown in Figure 1. A nucleation layer of AlN is universally used to initiate growth and avoid the Ga/Si eutectic that causes "melt-back". This is followed by a strain relief stack, where two successful approaches have been found based on either a step-graded AlGaN layer[3], or a superlattice of AlN/GaN[4]. The detailed stack design is normally proprietary. These buffers are used to induce compressive strain during growth which counteracts the tensile strain introduced on cooling, preventing cracking and yielding a flat wafer. To aid growth uniformity, thick Si substrates (1mm) tend to be adopted, which also helps to reduce the wafer breakage during processing which has been observed for standard thickness wafers (675µm). Total epi-layer thickness as large as 8µm can be achieved, but the challenges of wafer bow and stress become more difficult to overcome. Typical dislocation densities at the surface of the stack, i.e. at the 2DEG, are ≈$10^{9}$cm$^{-2}$.

Due to the incorporation of impurities and point defects, as-grown GaN is typically n-type and it has been found that it is essential to add deep level dopants to suppress leakage. The dopant of

choice is carbon[1] with a density well above $10^{18}cm^{-3}$ delivering excellent isolation and breakdown voltage. Carbon primarily incorporates substitutionally on the nitrogen site[5]. This pins the Fermi level about 0.9eV above the valence band making the GaN:C p-type, with electrical transport being via low mobility holes rather than electrons. It is found that the carbon doping must be spaced away from the active 2DEG to reduce trapping effects[6]. A key issue with carbon doping is current collapse (dynamic $R_{ON}$)[7]. Charge trapping occurs in the epitaxial bulk during off-state operation when there is high drain bias. When the device is switched on, trapped negative charge reduces the electron density in the active channel and increases the on-resistance. Some current commercial devices show as much as a factor of two increase following off-state bias.

**Advances in Science and Technology to Meet Challenges**

Suppression of current collapse is key for technology uptake. The p-type nature of GaN:C means that there is a p-n junction between the 2DEG channel and the bulk of the epitaxy, meaning that the bulk can be electrically floating. Suppression requires that this floating buffer is grounded to the active 2DEG channel preventing it from providing a back bias, and hence, counter-intuitively, a vertical leakage path is essential. Figure 2 shows an electrical network representation of the buffer, and simulations to show the impact of different leakage paths[8]. It is found that there is a trade-off between vertical leakage and current-collapse, with careful process control of leakage paths being absolutely required. Current state-of-the-art power devices are able to achieve less than 10% change in $R_{ON}$ in the 25-150°C temperature range by careful leakage control[9]. Recently it has been shown that changing the stoichiometry of the $Si_3N_4$ surface passivation can change the bulk vertical leakage and control the dynamic $R_{ON}$[10]. Further work is still required to achieve a guaranteed simultaneous optimisation of leakage and current collapse.

Many power switching topologies require the series connection of devices. Current technologies would require a hybrid packaging approach to prevent undesirable Si substrate bias being applied to the upper transistor in a half-bridge configuration. New approaches to allow transistor electrical isolation are therefore required before full integration is feasible. One approach being investigated is the use of buried oxide layers with 200V isolation being achieved by imec.

Operating at voltages much above 650V will require the growth of thicker epitaxy, and that requires a solution to reducing stress. Although single crystal GaN or AlN would be the ideal substrates, cost and wafer size make this unlikely to have any impact. One possible approach is the use of thermal expansion matched substrates as an alternative to Si wafers. For example polycrystalline AlN wafers have been successfully used as a growth substrate, achieving 18µm thick epitaxial layers.

**Concluding Remarks**

GaN-on-Si based power transistors are already achieving impressive performance and reliability based on the remarkable ability to grow strain-engineered, electrically-optimised, high-quality epitaxy on low cost 6” or 8” Si wafers. Buffer-related trapping leading to dynamic $R_{ON}$ has been a serious issue, requiring a delicate balance between leakage and performance for its suppression. This is only now being achieved by commercial suppliers. Going significantly beyond the current 650V market segment to much higher voltages will require major changes and innovation in the substrates and epitaxy to allow thicker epitaxial layers to be grown yet still retaining control of wafer bow.

**Acknowledgements**

*This work was funded by the UK EPSRC PowerGaN project K0114471/1.*

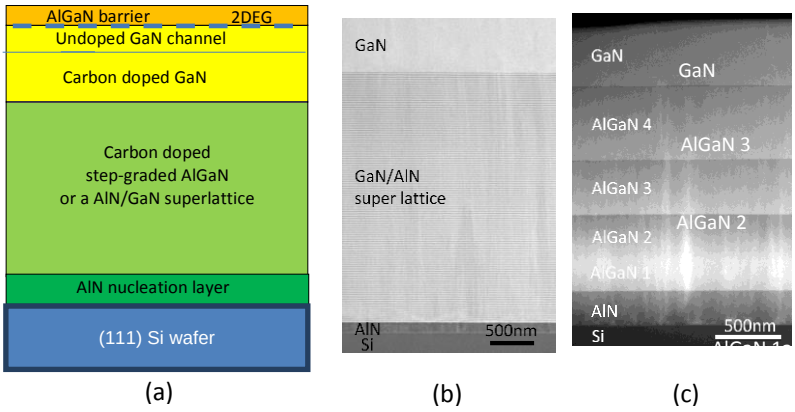


**Figure 1.** (a) Schematic cross-section of the typical epitaxial layer structure used for the manufacture of GaN-on-Si HEMTs. (b) TEM image of a GaN/AlN superlattice buffer layer and (c) a step graded AlGaN buffer layer, both on Si substrates.

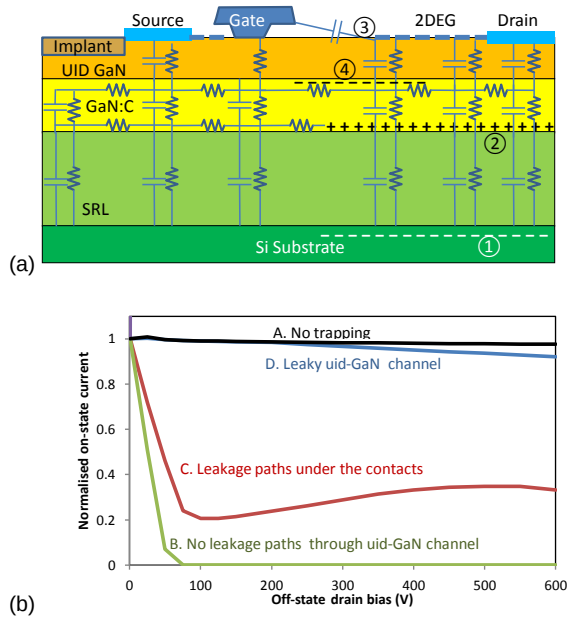


Figure 2. (a) Schematic showing leakage and capacitive paths within the buffer. ① to ④ indicate some of the key locations where charge accumulates. (b) Simulated dynamic $R_{ON}$ for different leakage paths within the buffer. All these different behaviours are observed in practice[8].

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# 5 - Challenges in growth for GaN power Electronics

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**Status**

Gallium nitride (GaN) based devices are promising for many power applications such as switching functions and inverters that can save a significant amount of energy. The performance and efficiency of these GaN power devices greatly rely on the epitaxial growth of GaN and related alloys. High quality GaN epitaxial growth can be achieved by using native free-standing GaN substrates. However, the downside of epitaxial GaN-on-GaN is it is expensive and only small-diameter GaN substrates. This in turn impede the mass production of GaN power devices at an affordable cost for commercial applications. To overcome this, the heteroepitaxial growth of GaN is carried out on foreign substrates such as silicon carbide (SiC), sapphire and silicon (Si). From commercial aspects, the heteroepitaxial growth of GaN-on-Si is attractive because of the large-size scalability of inexpensive Si substrates. Nevertheless, the areas of concern are the large differences in the physical properties between wide bandgap GaN and Si substrate that often results in poor crystal quality leading to high dislocation density, pits and cracks for GaN-on-Si. Therefore, appropriate epitaxial growth of GaN-on-Si and subsequent fabrication processes are absolutely necessary for power device applications. For example, several switching applications require lateral GaN-on-Si high-electron-mobility transistors (HEMTs) with high breakdown voltage (BV) [1]. To realize these GaN-on-Si lateral devices, we have used the metalorganic chemical vapor deposition (MOCVD) grown thick-AlN initial layer and GaN/AlN strained layer superlattice (SLS) structures. The AlGaN/GaN HEMTs grown on 8-inch silicon by using similar epitaxial growth technique delivered a high BV of 1.6 kV. For expanding the applications to electric and hybrid vehicles, high performance GaN power devices are required to drive high-power motors, power modules such as DC-DC converter and inverters. Typically, in these applications high-voltage GaN-on-Si vertical devices with reduced chip area are preferred. To facilitate the fabrication process of such devices, we have successfully grown thick GaN-on-Si vertical structures by using conductive buffer layers comprising of thin-AlN initial layer and SLS. The recent advances in the hetero epitaxial GaN-on-Si are encouraging for the growth of GaN power electronics on larger diameter Si substrates.

**Current and Future Challenges**

Despite its merits, the GaN-on-Si power devices have also associated technical challenges which need attention. Of these, the most important issue is the growth of a high-quality and thick GaN-on-Si. The large differences in lattice constants and thermal expansion coefficient between GaN and Si are responsible for the difficulties in the growth of high-quality and thick GaN-on-Si. The inset of Fig. 1 shows the cross-sectional structure of AlGaN/GaN HEMT on Si using metalorganic chemical vapour deposition (MOCVD). High temperature growth of GaN-on-Si could likely result in melt-back etching of Si substrate caused by Ga atoms [2]. As a result, deep pits, dislocations and cracks could arise, which in turn would deteriorate the device performance like an increase in buffer leakage, and reduced breakdown [3]. Therefore, the growth of high-temperature-grown AlN nucleation layer (NL) is indispensable to avoid both the melt-back etching and deep pits. Recent studies have revealed the influence of AlN NL on the vertical breakdown characteristics for GaN-on-Si and the AlN NL with better surface morphology and lower O impurity were preferred to grow highly resistive buffers [4]. Figure 1 illustrates the typical relationship between wafer bowing and total epitaxial thickness for the AlGaN/GaN HEMT on 4-inch Si. From this correlation, it could be understood that the use of GaN/AlN SLS is effective in controlling the bowing [5]. Subsequently, the growth of SLS is essential to control the wafer bowing for GaN-on-Si. Additionally, thick epi layers grown by using SLS multipairs supressed the vertical leakage and showed a vertical breakdown field of 2.3 MV/cm [6]. A high lateral $BV_{Off}$ of 1.4 kV was also demonstrated for AlGaN/GaN HEMT on Si grown with the above recommendations [7]. The recent systematic investigations and the promising results as discussed earlier would provide substantial understanding for the growth dynamics of epitaxial GaN typically on 8-inch Si substrates. Indeed, our AlGaN/GaN HEMT on 8-inch Si has shown a three-terminal off-state breakdown voltage 1650 V for the gate-drain distance of 50 µm. The availability of modern MOCVD reactors with multi-wafer capability and evaluation tools suggest promising features for GaN-on-Si lateral power devices.

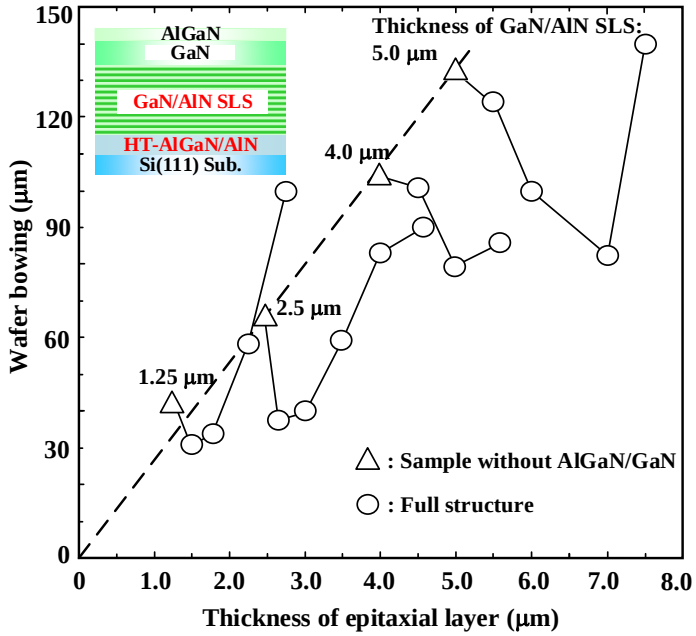


**Figure 1.** Wafer bowing as a function of total epitaxial layer thickness of AlGaN/GaN HEMT on Si. Copyright 2012 IEEE, reprinted with permission from Ref. 5.

**Advances in Science and Technology to Meet Challenges**

The GaN-on-GaN vertical devices are expected to play a vital role in future high-power conversion applications as it can reduce the overall chip area. However, the GaN substrate has disadvantages such as its limited wafer size and are expensive. Therefore, the realization of GaN-on-Si vertical devices is the upcoming challenge owing to growth and fabrication difficulties. Unlike the lateral AlGaN/GaN devices, deeper understanding on the growth and fabrication of GaN-on-Si vertical devices are required for potential power device applications. Some researchers have demonstrated the GaN-on-Si vertical p-n diodes fabricated by wafer bonding and substrate removal technology [8]. This technique could complicate the fabrication process and eventually lead to increase in cost. Others showed GaN p-n diodes by using a quasi-vertical structure [9]. Irrespective of these methods, a detailed study is required for the growth of GaN-on-Si vertical structures that should complement the fabrication as well. To realize such GaN-on-Si vertical device, (i) the doping density ($N_d$-$N_a$) in the drift region must be controlled and (ii) the buffer layer should be conductive. Figure 2 represents the net $N_d$-$N_a$ in the drift region as a function of $SiH_4$ flow rate for a GaN-on-Si grown with two SLS thicknesses. As shown, the $N_d$-$N_a$ could be controlled for GaN-on-Si by increasing the SLS multipairs, which is due to the reduction of dislocation density. The conductive buffer layers including the AlGaN/AlN layers and SLS are indispensable for realizing GaN-on-Si vertical devices. Therefore, a Si-doped AlN NL as thin as 3 nm was initially deposited followed by the deposition of Si-doped AlGaN and SLS. This novel fully vertical GaN-on-Si p-n diode comprises of doped buffer layers and not involve substrate removal technology. This GaN-on-Si p-n diode has ohmic contacts on the p-GaN layer and backside of n+-Si substrate, that showed a turn-on voltage of 3.4 V and a breakdown voltage of 288 V for the 1.5-µm-thick $n^-$-GaN drift layer [10]. The BV can be further improved by increasing the buffer thickness and/or by using field plate structures. These improvements in the MOCVD growth of GaN-on-Si vertical structures suggest their potential role in power electronics in near future.

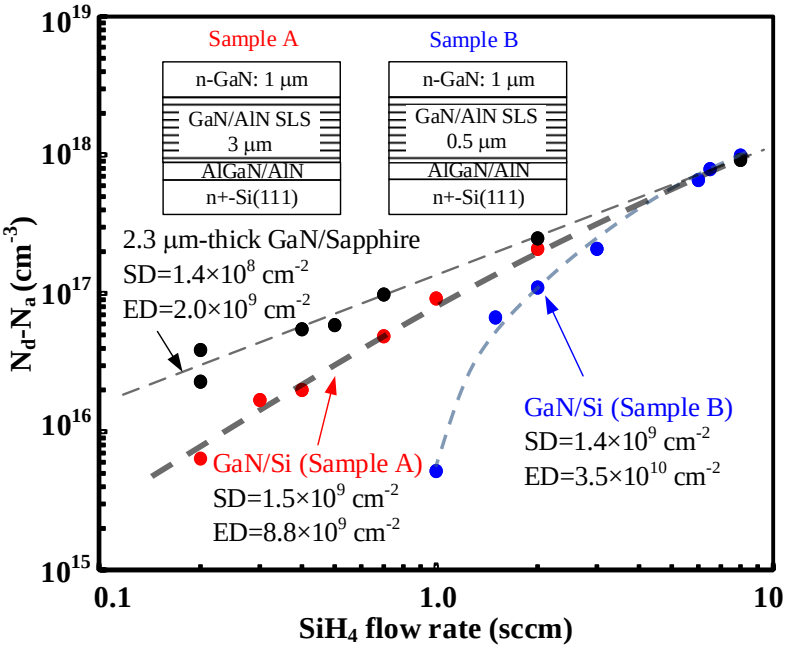

**Figure 2.** Net doping concentration as a function of $SiH_4$ flow rate for GaN-on-Si with different SLS thickness. For comparison, the data of GaN/sapphire are also shown. Copyright (2016) The Japan Society of Applied Physics, reprinted with permission from Ref. 10.

## Concluding Remarks

The GaN-on-Si power devices are emerging to play a dominant role in the next-generation power electronics. Significant improvements in the hetero epitaxial growth and device fabrication are indispensable for the commercialization of these power devices. For the epitaxial growth of GaN-on-Si lateral devices, we have utilized the high temperature AlN NL to prevent the melt back etching of Ga into Si. It was also found that the growth of SLS is essential to control the wafer bowing for GaN-on-Si. In addition, the growth of SLS multipairs effectively enhanced the breakdown voltage of GaN-on-Si HEMTs. On the other hand, fully-vertical GaN-on-Si p-n diodes were demonstrated by using conductive buffer layers. We have used AlN NL as thin as 3 nm and SLS multipairs, both highly doped in order to realize fully-vertical GaN-on-Si p-n diodes. These advancements in the MOCVD growth of GaN-on-Si and device fabrication processes will lead to the high-performance power electronics.

## Acknowledgement

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# 6 – Vertical GaN Power Devices

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**Status**

Central to improving the efficiency of power electronics is the availability of low-cost, efficient and reliable power switching devices. GaN-based devices are exciting candidates for next-generation power electronics. Currently, both lateral and vertical structures are considered for GaN power devices. Vertical GaN power devices have attracted significant attention recently, due to the capability of achieving high breakdown voltage (*BV*) and current levels without enlarging the chip size, the superior reliability gained by moving the peak electric field away from the surface into bulk devices, and the easier thermal management than lateral devices [1].

Since 2010, the field of vertical GaN power devices has grown exponentially and seen numerous demonstrations of vertical diodes and transistors (figure 1). A 3.7 kV vertical GaN pn diode [2] and a 1.1 kV vertical GaN Schottky barrier diode (SBD) [3] have recently showed near-theoretical power figure of merit. Trench metal-insulator-semiconductor barrier Schottky diodes [4] (figure 2(a)) and junction barrier Schottky diodes [5] (figure 2(b)) have also been proposed to combine the good forward characteristics of SBDs (e.g. low turn-on voltage) and reverse characteristics of pn diodes (e.g. low leakage current and high *BV*).

Several structures have been proposed for vertical GaN transistors, with the highest *BV* close to 2 kV. Current aperture vertical electron transistor (CAVET) combines the high conductivity of a two-dimensional electron gas (2DEG) channel at the AlGaN/GaN heterojunction and the improved field distribution of a vertical structure [6] (figure 2(c)). The CAVET is intrinsically normally-on, but a trench semi-polar gate could allow for normally-off operation [7] (figure 2(d)). Vertical GaN trench MOSFETs have no 2DEG channels, but do not need the regrowth of AlGaN/GaN structures and are intrinsically normally-off [8] (figure 2 (e)). Recently, vertical fin MOSFETs have been demonstrated to achieve normally-off operation without the need for p-type GaN materials or epitaxial regrowth [9] (figure 2(f)).

While most vertical devices utilize expensive GaN substrates, it is also feasible to make vertical GaN devices on low-cost Si substrates. Quasi- and fully-vertical GaN-on-Si vertical diodes have been demonstrated with a *BV* over 500 V and excellent high-temperature performance [10]. These devices can enable 100-fold lower substrate and epitaxial cost than GaN-on-GaN vertical devices.

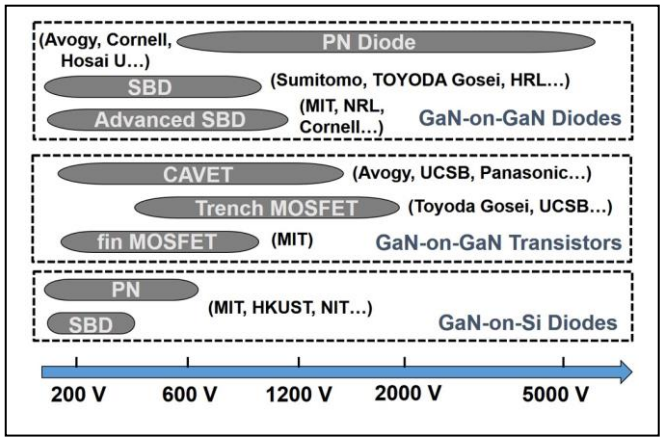


**Figure 1.** Overview of the main device types and voltage classes for the vertical GaN power devices reported in recent years.

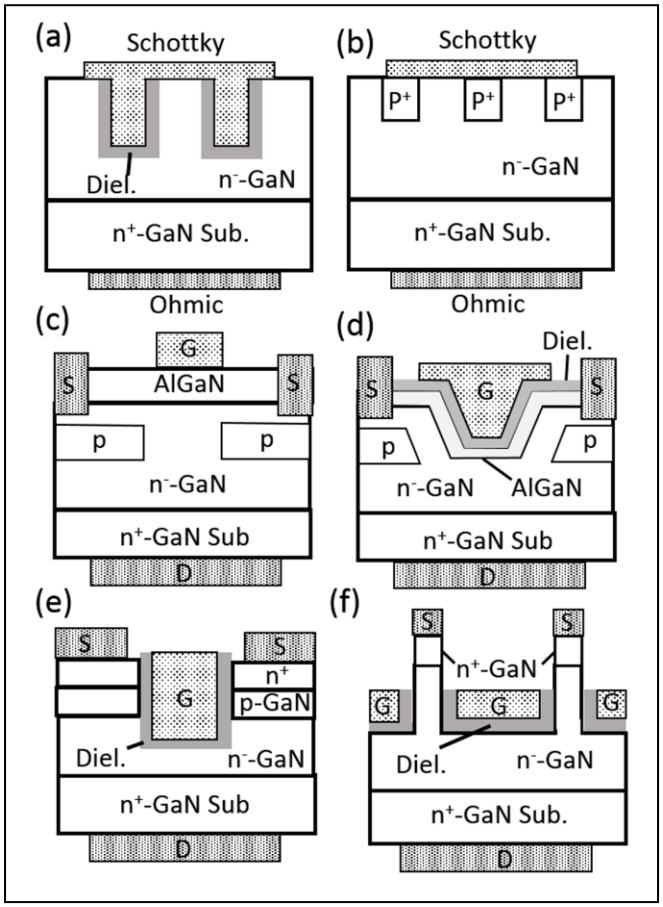


Figure 2. Schematic of representative vertical GaN advanced Schottky barrier diodes and vertical GaN transistors: (a) trench MIS barrier Schottky diode, (b) junction barrier Schottky diode, (c) CAVET, (d) trench CAVET, (e) trench MOSFET and (f) vertical fin MOSFET. In this Figure, "Diel." stands for dielectrics, and "Sub." for substrates.

**Current and Future Challenges**

In spite of the great progress, the full potential of vertical GaN SBDs and transistors has not been exploited yet. The *BV* demonstrated in these devices, with no avalanche capability reported, is still much lower than the avalanche *BV* in vertical GaN pn diodes. The lack of avalanche capability would greatly compromise the device robustness when operating in inductive switching environments. Although the nature of avalanche breakdown is still not fully understood in GaN devices, a key factor is believed to be good edge termination technologies and a way to remove holes from the structure. In SiC power devices, successful edge termination technologies, such as junction termination extension and field rings, was enabled by selective p-type doping. However, in GaN devices, the current selective area doping or selective area epitaxial regrowth technologies cannot yield material of sufficiently high quality to enable defect-free patterned lateral pn diodes. In particular, p-type implantation and activation in GaN is far from mature. With complicated activation annealing schemes, the activation ratio for acceptors is typically below 5%, resulting in very low concentration and mobility for the activated free holes [5].

There remain open questions on the selection of carrier channels in vertical GaN transistors to improve the device forward characteristics. The ideal channel for these devices would have normally-off configuration with high carrier mobility and without the need for epitaxial re-growth. Further work is needed for all the three channels reported so far, 2DEG channel [6], MOS inversion layer [8] and bulk fin channel [9].

The commercialization of vertical GaN power devices has been hindered by the high cost of bulk GaN substrates. The mainstream GaN substrates are 2-inch, while 4- and 6-inch GaN substrates are available very recently in small volumes. The wafer cost (per area) for 2-inch GaN-on-GaN is \$60~\$100/cm$^2$, still much higher than the cost for 4-inch SiC (~\$8/cm$^2$) and 8-inch GaN-on-Si (~\$1/cm$^2$). The fundamental challenge is how to achieve the material quality associated with free-standing GaN substrates, while allowing the devices to be transferred to alternate substrates and have the GaN substrates re-used to reduce cost.

**Advances in Science and Technology to Meet Challenges**

Different technological solutions can be envisioned to address the challenges in making patterned lateral pn junctions for edge termination structures. For example, compared to p-type ion implantation, n-type ion implantation (e.g. Si, N, etc.) and activation is much easier. Lightly-doped p-GaN edge terminations has been then demonstrated by implanting donors to compensate highly-doped p-GaN layers in vertical GaN pn diodes [2]. Patterned pn junctions have also been reported by n-type ion implantation into epitaxially grown p-GaN regions [5]. Besides selective ion implantation, the patterned pn junctions can be also made by selective p-GaN regrowth to fill n-GaN trenches. The initial feasibility of this approach has been demonstrated in CAVET [6], although much more work is needed to study the regrown interface quality and passivate parasitic leakage currents.

In parallel, different electrical, mechanical and chemical techniques are under development to enable devices to be lifted off from native GaN substrates and transferred to low-cost substrates. Successful layer transfer technology, combined with patterned interconnections on the supporting substrate and re-use of GaN substrates, should greatly reduce the cost and pave the way to commercialize high-performance vertical GaN power devices.

Another approach that can fundamentally circumvent the cost issue of vertical GaN devices is to fabricate them on Si substrates, which could allow for almost 100-fold lower wafer and epitaxial cost as well as 8-inch fabrication. Recently, GaN-on-Si vertical pn diodes with blocking capability of 500-600 V have been demonstrated [10]. Fully-vertical GaN-on-Si power devices have also been demonstrated by different technologies, such as layer transfer, conductive buffer layer, and selective removal of the substrate and buffer layer. To improve the performance of these devices, advances in epitaxial growth technology are needed to enable thicker GaN layers with very low background carrier concentration (< $10^{16}$ cm$^{-3}$) on Si substrate.

**Concluding Remarks**

Vertical GaN devices are key to achieve the high currents (> 100 A) and voltages (> 600 V) required by many power applications, such as electric vehicles and renewable energy processing. Record performance near the theoretical Baliga figure of merit has been demonstrated in vertical GaN pn diodes, although more work is needed in vertical Schottky barrier diodes and transistors. Exciting research opportunities exist in the field, especially in making patterned pn junctions, recycling GaN substrates and developing vertical GaN devices on Si substrates.

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# 7 – GaN Insulated Gate Field-Effect Transistors

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**Status**

GaN-based insulated gate field-effect transistors with an insulating gate dielectric provide many desirable properties such as suppressed gate leakage and large gate voltage swing [1]. These devices are typically in the form of metal-insulator-semiconductor HEMT (MIS-HEMT) or MIS-FET with the insulating dielectric on a heterojunction (e.g. AlGaN/GaN) channel or a GaN channel, respectively, as illustrated in Fig. 1(a) and (b). The MIS-HEMT was first studied for RF/microwave power amplifier applications [2], and then intensively investigated as a promising power switching device. The MIS-gate transistors are especially attractive to high-frequency power switching applications because they can better tolerate gate voltage over-shoot that often occurs in circuits with high slew rate.

As is the case of Si- and SiC-based MOSFETs, the gate dielectric in GaN insulated gate FETs is required to deliver a dielectric/III-nitride interface with low trap density, high reliability and long lifetime under various stresses (e.g. electrical, thermal, humidity, etc.). GaN MIS-HEMTs typically exhibit depletion-mode (D-mode) operation with a large negative threshold voltage ($V_{th}$) because of the presence of high-density positive polarization charges in the barrier layer (e.g. AlGaN). The D-mode MIS-HEMT, with its gate (input) terminal seldom forward biased during circuit operation, typically exhibit less adverse effects from the gate dielectric. This is mainly due to the presence of the barrier layer that decouples the 2DEG channel from the interface/border traps in the dielectric as long as the "spill-over" of electrons toward the dielectric does not occur, leading to small $V_{th}$ hysteresis. Very good gate reliability [3] has been obtained in D-mode MIS-HEMTs featuring a thin gate dielectric layer ($SiO_2$, $Si_3N_4$ or high-κ dielectrics) under relatively small forward gate bias.

Enhancement-mode (E-mode) MIS-HEMTs and MIS-FETs with a positive $V_{th}$ are highly desirable from the circuit application point of view for their simpler gate control circuitry and fail-safe operation. To fully turn on the channel current, however, large positive forward gate needs to be applied. This is when the gate dielectric is under the most demanding operational conditions (e.g. high electric field, charge injection to the dielectric and carriers leaking through the dielectric). $V_{th}$-instability (both static and dynamic) at different temperature and bias stress conditions, and its impact on dynamic on-resistance ($R_{ON}$) need to be systematically studied and clearly understood [4, 5]. The time-dependent dielectric breakdown (TDDB) is the ultimate hurdle to overcome before commercialization of E-mode GaN-based MIS-HEMTs and MIS-FETs.

**Current and Future Challenges**

Trap states at the dielectric/III-nitride interface and inside the dielectric present the biggest challenges to GaN MIS-HEMTs and MIS-FETs [6]. With a wide bandgap in GaN, a large energy window is available to accommodate interface and bulk trap states at shallow and deep energy levels with short and long emission time constant $\tau_{it}$. The dynamic charging/discharging processes of these traps could lead to $V_{TH}$ instability during a switching operation, and consequently affect circuit and system stability.

Unlike Si on which highly uniform and highly reliable thermal oxide can be prepared using high-temperature (800 °C ~ 1200 °C) furnaces, GaN surface becomes unstable when the ambient temperature exceeds 800 °C. In addition, the Ga-O bonds at an oxide/III-nitride interface fundamentally induce high-density gap states, except in a few very specific crystalline oxide

configurations, according to a first-principles calculation study [7]. Thus, removing the detrimental Ga-O bonds at the GaN surface is a critical step for obtaining low interface trap density ($D_{it}$). If oxide-based gate dielectric is to be used for their high dielectric constant and large bandgap, a non-oxide (e.g. nitride-based) interfacial layer would be highly desirable.

Although there are many reports on E-mode GaN MIS-HEMTs and MIS-FETs in research literature, the commercialization of these devices has been hindered by concerns over the gate dielectric reliability. The commonly used gate dielectric (SiN, $SiO_2$ and $Al_2O_3$) is deposited by PECVD or ALD (atomic layer deposition) at relatively low temperature (at 300~400 $^oC$). While the low temperature helps maintain GaN surface morphology, it is also the main reason for high-density defects in the dielectric, making it difficult for these devices to pass reliability tests and qualifications. High-temperature annealing only shows moderate effect on enhancing the dielectric reliability. Thus, it is of critical importance to develop high-temperature gate dielectric films (e.g.~ 800 $^oC$ or above) with lower defect density and longer TDDB lifetime. The biggest challenge to high-temperature dielectric on GaN is the degradation (via decomposition or chemical reaction) of GaN surface at high temperatures. A possible solution could feature a low-temperature interface protection layer and high-temperature gate dielectric.

**Advances in Science and Technology to Meet Challenges**

The first D-mode GaN MIS-HEMT was demonstrated using PECVD-$SiO_2$ as the gate dielectric [2]. With MOCVD-grown in-situ $SiN_x$ as the gate dielectric, low $D_{it}$ and excellent gate reliability are obtained [3]. At 10 years, for a 100ppm failure rate, a $V_{gs\_max}$ of ~3.1V is extracted, which is well above the operating $V_{gs}$ for a D-mode MIS-HEMT ($V_{gs\_max}$=0V).

The first E-mode GaN MIS-HEMT was demonstrated using PECVD-$SiN_x$ deposited on fluorine-implanted AlGaN/GaN heterojunction [8]. Low-damage and well-controlled dry and digital etching techniques are being developed to obtain positive threshold voltage. E-mode partially recessed MIS-HEMTs and fully MIS-FETs have both been developed with low on-resistance, high saturation current, small $V_{th}$ hysteresis and low dynamic on-resistance. In particular, *in-situ* removal of native oxide and consequent nitridation by low-power plasma (as illustrated in Fig. 1 (c)) prior to dielectric deposition [9] are important techniques for producing high-quality dielectric/GaN interface by passivating the dangling bonds while introducing minimum gap states.

To achieve high gate dielectric reliability under large positive gate bias required for E-mode insulated gate FETs, $SiN_x$ deposited by LPCVD (low-pressure chemical vapor deposition) has emerged as a compelling candidate as it possesses several important benefits including large conduction band offset with GaN ($\Delta E_c$ ~ 2.3 eV), relatively high dielectric constant ($\kappa$ ~ 7) and especially the long TDDB lifetime as a result of the low defect density achieved at high deposition temperature (e.g. 780 $^oC$). Implementing the LPCVD-$SiN_x$ gate dielectric in recessed-gate E-mode MIS-HEMTs and MIS-FETs has been more challenging since an etched GaN surface suffers more severe degradation than an as-grown GaN surface at high temperatures. An effective approach to suppressing such a degradation while maintaining low $D_{it}$ ($10^{11}$~$10^{12}$ $cm^{-2}$ $eV^{-1}$) has been developed using a low-temperature PECVD-$SiN_x$ thin film as an interfacial protection layer [10], as depicted in Fig. 2. For a 10-year lifetime, the maximum gate bias is determined to be 11 V at a failure rate of 63.2 % and 9.1 V at a failure rate of 0.01%.

**Concluding Remarks**

There is strong demand for GaN insulated gate field-effect transistors with both depletion- and enhancement-mode operations, as the insulated gate provides strong immunity to control voltage spikes and could be driven with circuits very similar to those used for the mainstream Si and SiC power MOSFETs. The most critical need of a GaN insulated gate FET technology is a gate dielectric technique that simultaneously delivers low interface/bulk trap density and robust reliability under stringent

electrical and thermal stresses. The E-mode GaN MIS-HEMTs and MIS-FETs are especially challenging as they operate under large positive gate bias and the recessed-etched GaN demands better protections during high temperature process associated with high-quality dielectric deposition. Combining low-temperature interfacial layer with high-temperature gate dielectric could be a promising pathway toward reliable and stable GaN insulated gate FETs.

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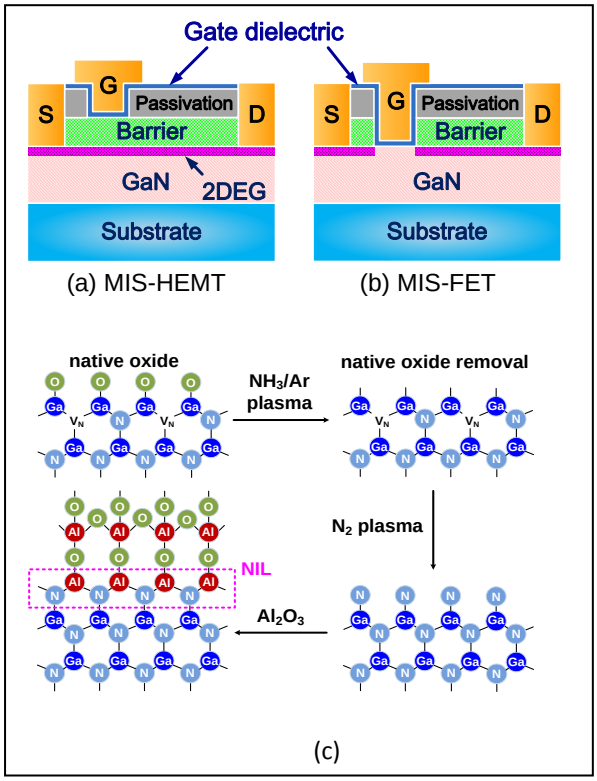


**Figure 1.** Schematic cross sections of GaN-based (a) MIS-HEMT and (b) MIS-FET. (c) Schematic process for *in-situ* native oxide removal and surface nitridation of GaN.

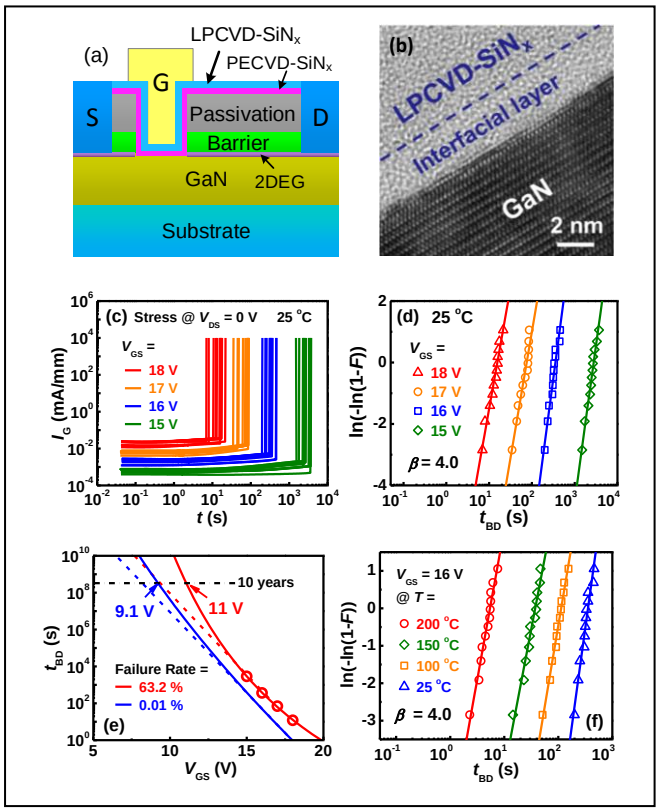


**Figure 2.** (a) Schmematic cross section of an E-mode fully recessed GaN MIS-FET with interfacial protection layer. (b) High-resolution TEM of an LPCVD-$SiN_x$/PECVD-$SiN_x$/GaN interface. (c) Time to breakdown ($t_{BD}$) of the LPCVD-$SiN_x$ MIS-FETs with interfacial protection layer at forward gate stress of 18, 17, 16 and 15 V at 25 °C. (d) Weibull plot of the electric field-dependent $t_{BD}$ distribution. (e) Lifetime prediction with a failure rate of 63.2 % and 0.01 %, respectively. (f) Weibull plot of the temperature-dependent $t_{BD}$ distribution.

# 8 - Reliability of GaN Power Devices: Normally-on and Normally-off

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**Status**

Reliability is essential for the application of GaN power devices to critical electronic systems, for high-voltage energy conversion, control of electrical engines, automotive electronics [1]. GaN is a robust material, capable of withstanding extremely high electric field and temperature; in order to fully exploit its potential, deep levels effects and failure mechanisms induced by high voltage and high temperature stress must be known in detail.

Several technological options are available for the fabrication of GaN power high electron mobility transistors (HEMTs): Schottky-gate normally-off transistors, which have the simplest structure, are prone to higher leakage current with respect to their insulated-gate counterpart; nevertheless they can reach breakdown voltages higher than 1100 V and can achieve normally-off operation in conjunction with a Si MOS driver in cascode configuration [2]. Normally-off devices can be achieved using p-type AlGaN or GaN with high acceptor doping on top of the AlGaN [3]. Recessed-gate metal-insulator-semiconductor devices (MISHEMT) enable operation at positive gate bias without measurable gate current $I_G$ [4]. Normally-off operation can be achieved by decreasing the thickness of the AlGaN layer under the gate in a recessed structure.

The different structures can be affected by specific failure mechanisms. When biased in off-state at high reverse bias, Schottky-gate, normally-on HEMT were subject to a significant and progressive increase of gate leakage current (several orders of magnitude), correlated with the onset of leakage current paths which can be detected by electroluminescence (EL) [5]. Further analysis revealed that this catastrophic increase of $I_G$ was time dependent, that time to failure depended on the electric field, followed a Weibull distribution, and decreased slightly with temperature (activation energy = 0.12 eV). $I_G$ increase was attribute to the formation of a conductive percolation path across defects [5]. This concept of GaN as a “lossy dielectric” was a major breakthrough for GaN reliability: it allowed the extrapolation of device lifetime using standard time-dependent dielectric breakdown (TDDB) tests, and promoted the study of other GaN time-dependent failure mechanisms, described in the following.

**Current and Future Challenges**

Time dependent breakdown effects in Schottky gate devices were due to different physical mechanisms either related to device design or materials quality: (i) in normally-on power Schottky HEMTs with double field-plate, TDDB was found to be due to the failure of the insulating SiN layer between the two-dimensional electron gas (2DEG) and the first field-plate edge. Increased robustness was achieved by changing the substrate conductivity in order to move the 2DEG edge towards the drain [2]; (ii) in AlGaN/GaN power Schottky diodes, breakdown involved first the dielectric at the diode edge and then the AlGaN; as a consequence, lifetime improves by adopting either a thicker plasma-enhanced atomic layer deposition (PEALD) SiN edge-termination dielectric (from 15 nm to 25 nm) or

a more robust one (25 nm in-situ SiN) [6]; (iii) drain-source off-state catastrophic breakdown of n-on Schottky gate HEMTs, may occur as a consequence of hole trapping and accumulation at the source edge of the gate: trapped positive charge shifts threshold voltage towards negative values and turns on the device while a high drain voltage is applied, thus resulting in device burn-out [7].

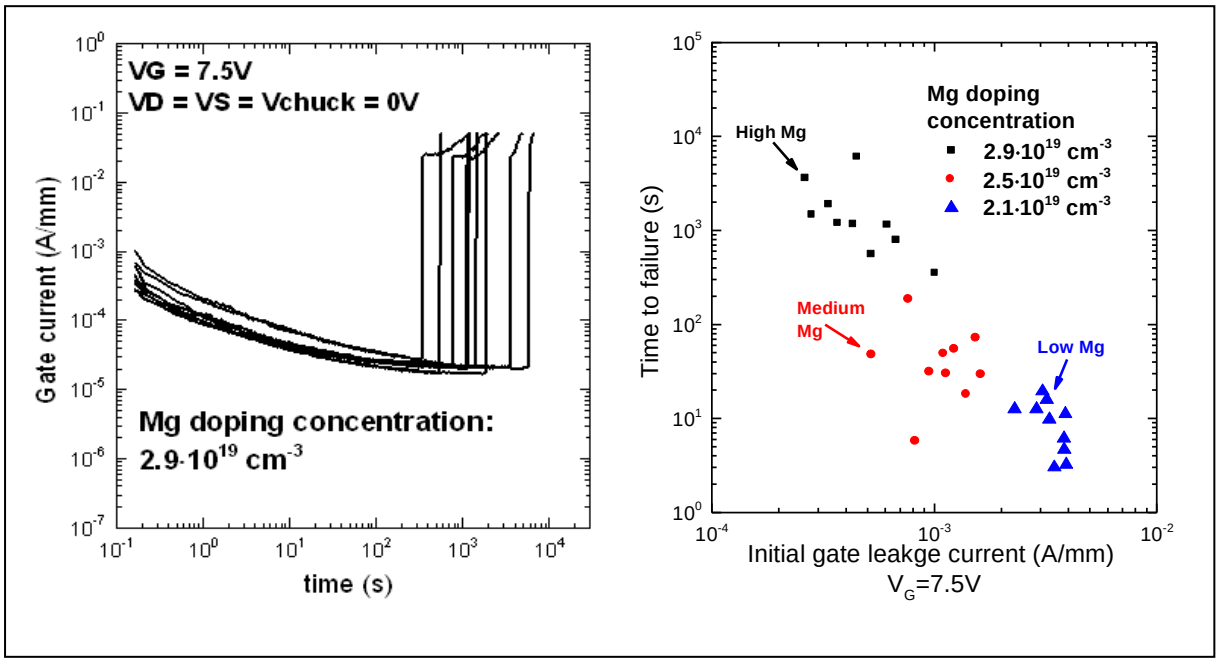


**Figure 1.** Left: Time-dependent breakdown experiment on the p-gate of a normally-off GaN HEMT; Right: dependence of time to failure on initial gate leakage current at $V_G$ = 7.5 V (and consequently on p-type doping concentration in the p-GaN layer [8]. Reprinted from Microelectronics Reliability, Vol 76-77, I. Rossetto, M. Meneghini, E. Canato, M. Barbato, S. Stoffels, N.Posthuma, S. Decoutere, A.N. Tallarico, G. Meneghesso, E. Zanoni, "Field- and current-driven degradation of GaN-based power HEMTs with p-GaN gate: Dependence on Mg-doping level", Pages No. 298-303, Copyright 2017, with permission from Elsevier.

P-gate devices (either with an ohmic or a Schottky metal contact on top of the p-layer) are currently the most popular choice for n-off devices. A critical mechanism for p-gate HEMTs is the TDDB consequent to the application of a positive gate bias. In the case of a rectifying contact on p, positive bias leads to increased electric field, potentially leading to breakdown. Time to failure decreases at increasing gate leakage current and consequently at higher temperature ($E_a$ = 0.5 eV); times to failure are Weibull-distributed. Higher Mg doping in the p-layer reduces leakage current and therefore improves lifetime. A possible explanation consists in the accumulation of positive charge at the interface with the AlGaN, proportional to leakage current which, at its turn, enhances gate current and promotes further degradation. A second hypothesis implies the formation of a percolation path, consequent to defects formation due to hot carriers (collected by the gate). In this case also, times to failure are Weibull-distributed; a 20-years lifetime at $V_{GS}$ = +7.2 V was demonstrated for a 200 V n-off technology [3].

The vertical drain-substrate stack is also sustaining a high electric field and is prone to time-dependent breakdown: a 200 V n-off technology was submitted to tests at $V_{D\text{-substrate}}$ in excess of 700 V and failed due to vertical burnout in approximately 2 X $10^4$ s. Higher leakage current and temperature correspond to shorter lifetime, with a decrease which is thermally activated with a 0.25 eV activation energy. The maximum applicable voltage for a lifetime of 20 years with 1% failure rate is about 560 V at RT, considerably higher than the operating voltage [9].

The GaN MISHEMT represents an ideal structure for normally-off power GaN electron devices since the dielectric layer reduces significantly the gate leakage; unfortunately the MIS structure introduces new reliability problems, related with the stability of device threshold voltage. Large positive $V_{th}$ shifts (positive bias temperature instabilities) have been observed under forward gate bias conditions and attributed to accumulation of electrons at the dielectric/III-N interface where a second electron channel forms in the so-called "spill-over" conditions [10]. According to [10], the density of interface states of any dielectric is currently high enough to completely deplete the 2DEG channel with a typical electron density in the order of $10^{13}$ $cm^{-2}$. Improvements therefore require either a reduction of interface states or an increase of the voltage required to induce the "spill-over".

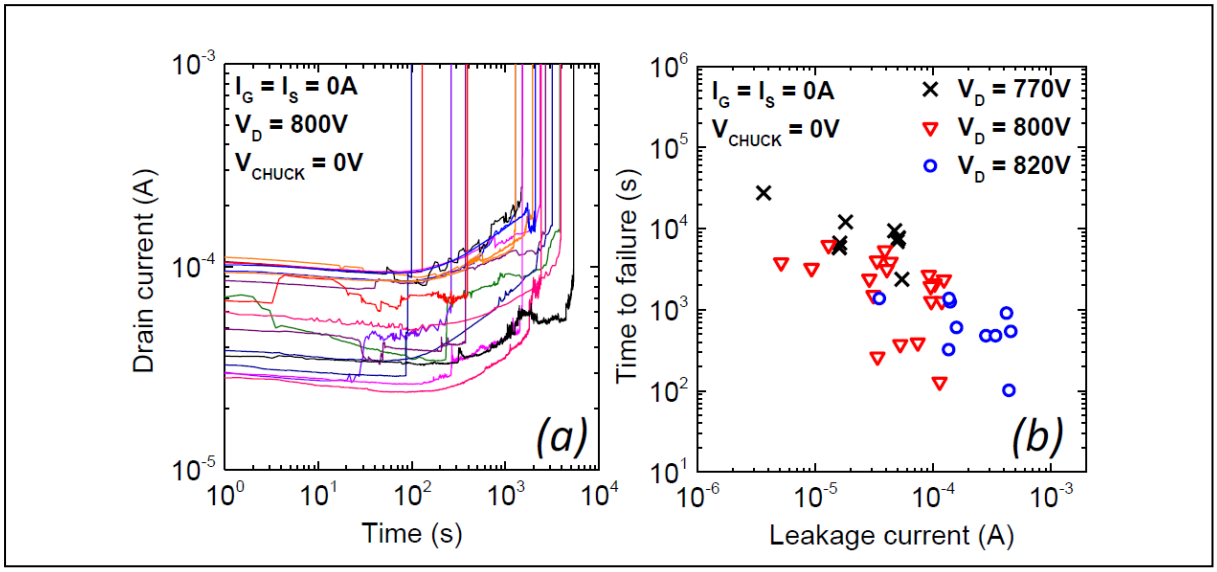


Figure 2. (a): time-dependent breakdown test on drain current at $V_{DS}$ = 800 V. Data refer to normally-off p-GaN gate devices at RT. (b): time to failure dependence on the initial leakage for three drain bias levels applied during the constant voltage stress [9]. Reprinted with permission from: Matteo Borga, Matteo Meneghini, Isabella Rossetto, Steve Stoffels, Niels Posthuma, Marleen Van Hove, Denis Marcon, Stefaan Decoutere, Gaudenzio Meneghesso, and Enrico Zanoni, "Evidence of Time-Dependent Vertical Breakdown in GaN-on-Si HEMTs", Transaction on Electron Devices, vol. 64 no. 9, pp. 3616-3621, September 2017. © IEEE 2017

Negative voltage shift (NBTI), observed when negative voltage is applied to the gate is usually less severe, and becomes relevant only at high temperature (activation energy 0.37 eV, see [4] and reference therein). According to [4], NBTI is due to detrapping of states at the SiN/AlGaN interface; authors in [11] have formulated a unified model for positive bias temperature instability (PBTI) and NBTI, which implies electron trapping/detrapping in pre-existing oxide traps that form a defect band very close to the GaN/insulator interface. NBTI can reduce the threshold voltage of n-off devices, thus thinning the safety margin in off-state. Conversely, NBTI does not represent a critical problem for n-on devices: under cascode operation, the on/off state is controlled by the Si MOSFET; moreover, due to the leakage current of the Si MOSFET, the HEMT is always in slight semi-on state, and this limits the electric field across the SiN/AlGaN stack.

**Advances in Science and Technology to Meet Challenges**

Schottky-gate and MISHEMT n-on devices for cascode configuration and p-gate n-off devices are gaining maturity; time-dependent breakdown effects can be evaluated using standard, well-established testing methods; methods for long-term thermal stability assessment still have to be developed and consolidated into standards. Some issues remain, concerning gate leakage, hot

electron degradation, instantaneous breakdown. Concerning n-off MISHEMTs, stabilization of threshold voltage remains an open issue, which requires in-depth physical characterization of surface and interface properties and of dielectric materials

**Concluding Remarks**

This chapter has reviewed reliability of n-on and n-off GaN power HEMTs, with particular emphasis on time-dependent breakdown mechanisms and NBTI/PBTI effects. Results described here have been obtained by means of on-wafer short-term (<100 h) tests. Knowledge on the long-term reliability of these devices is being developed only recently, thanks also to cooperative projects such as POWERBASE and InRel-Npower, which promise to achieve full maturity for GaN power technologies in the 650 – 1200 V range.

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# 9 – Plasma Processing for GaN Power Electronic Devices

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**Status**

To significantly impact the marketplace of energy efficient power switching, GaN-based transistors must be produced in high volumes at low cost. Adopting silicon-based substrates and silicon-like manufacturing approaches enables production using legacy 150 mm and 200 mm wafer facilities driving cost efficiencies. Standard silicon manufacturing approaches rely heavily on plasma processing for etching semiconductors and deposition of dielectrics and metals. These procedures need to be migrated to GaN-based materials and optimised to minimise process induced damage of the semiconductor layers. These can present as reductions in channel carrier concentration and mobility and therefore increased on-resistance; and hysteretic effects due to the formation of charge trapping states which can influence dynamic response.

As shown in Figure 1(a), there are three areas where plasma processing as part of device manufacture can have a significant effect.

1 – in the source-drain regions, controlled etching into the semiconductor to the same relative position compared to the device channel offers a generic solution as described in [1] irrespective of the thickness of the AlGaN barrier layer of the device.

2 – in the gate-drain region, effective passivation of the semiconductor surface is vital to minimise leakage current and current collapse. A variety of dielectrics are being actively used and demonstrated encouraging performance [2], [3] with further work required to fully understand the interaction between the dielectric and the semiconductor.

3 – in the gate stack, a dielectric introduced between the gate metal and the semiconductor (Figure 1(b)) can suppress gate leakage current. Subjecting the semiconductor to a fluorine plasma (Figure 1(c)) has been shown to be effective in shifting positive the device threshold voltage [4], important for normally-off device operation. There can be issues with long term reliability of this approach however. An alternate is to perform a gate recess etch prior to gate dielectric and metal deposition (Figure 1(d)) – controlling the etch depth to control threshold voltage requires the use of low damage plasma based atomic layer etching approaches, such as those described in [5]. Wafer scale and wafer to wafer uniformity of these etching approaches still need to be confirmed.

**Current and Future Challenges**

*Plasma Processing in the Source-Drain Region*

As reported in [1] and [6], plasma etching of the semiconductor layers in the source-drain region before contact metal deposition results in reduced contact resistance (0.18 Ohm mm was obtained in [6] using "patterned" $Cl_2$-based plasma etching), and reduced thermal budget (contact resistance of 0.5 Ohm mm was achieved in [1] at a contact anneal temperature of 550 $^oC$ using a $SiCl_4$-based chemistry). Driving down the thermal budget to below 500$^oC$ opens new opportunities for "gate first" approaches to device realisation which may be important in improving the stability of the gate/semiconductor interface.

*Plasma Processing in the Gate-Drain Region*

As described in [2], passivation of the gate-drain region using low pressure chemical vapour deposition (LPCVD) of $SiN_x$ with optimal conditions had a strong effect on both current collapse and

leakage currents. This is a high temperature (850 $^{o}$C) process. A key property of the LPCVD-SiNx films in this study was the stress. Recently, the use of stress control in room temperature deposited inductively coupled plasma-CVD (ICP-CVD) $SiN_x$ films for surface passivation was also shown to reduce significantly leakage currents [3], therefore a key challenge at this time is to understand the underlying physical mechanisms that govern the leakage current and current collapse phenomena.

*Plasma Processing in the Gate Stack*

As mentioned above, the incorporation of a gate dielectric is important to reducing the gate leakage current in GaN transistors and allows for a larger gate voltage swing, which is particularly important for normally-off devices. As reported in [7], controlling the properties of the GaN surface, in this case by removing a SiN capping layer deposited as the final stage of the wafer growth using an $SF_6$ plasma etch immediately prior to atomic layer deposition of an $Al_2O_3$, resulted in a 4x reduction in hysteresis to 60 mV for GaN MOS-capacitors. This work also reported the impact of the introduction of TiN into the gate stack, which resulted in a 35% increase in accumulation capacitance. Understanding of the origin of these effects will be vital to further device optimisation.

**Advances in Science and Technology to Meet Challenges**

Understanding the role and impact of plasma-based processing will be vital to further optimising and improving the efficiency of GaN power device operation in terms of static and dynamic on-resistance, current collapse, leakage currents and threshold voltage control. Control of the semiconductor surface, both mechanically and chemically is a key. This can best be addressed by understanding and correlating the properties of the semiconductor surface and its interface with dielectrics and/or metals with transistor performance. Combining plasma processing equipment so that an etched wafer can be transferred directly into a dielectric or metal deposition tool is an important technological advance. This “clustered” approach to wafer processing is relatively standard in the mainstream silicon industry – research needs to be undertaken to validate such approaches for GaN-based materials and devices for power electronics applications. A cluster tool such as that shown in Figure 2 is already proving highly insightful in this regard. In addition to combined process chambers, the cluster tool shown in Figure 2 also has in-situ scanning Auger capability. Clustered plasma process and metrology engines are going to be the key to unlocking the full potential of plasma processing for GaN power electronics.

**Concluding Remarks**

Plasma processing is a vital element in the manufacture of GaN power electronics as, based on its use in the mainstream silicon industry, only plasma processing offers reproducible wafer scale and wafer to wafer etching and dielectric and metal deposition. Arguably, the GaN surface is one of the most process sensitive in the electronics industry, so its control at a chemical level is key to fully optimising device performance. Having a profound and fundamental understanding of the impact of plasma processing on the GaN surface is therefore an imperative to ultimate GaN power device realisation.

**Acknowledgements**

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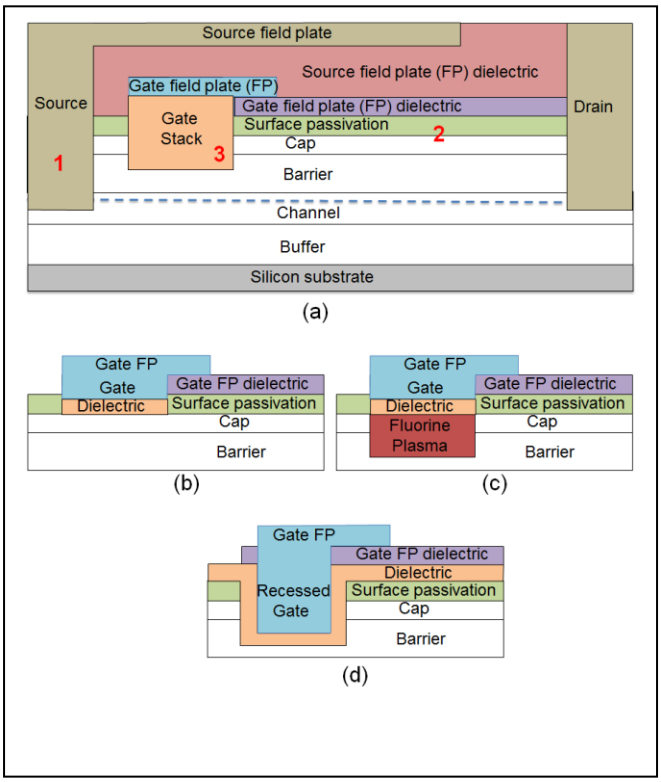


**Figure 1.** (a) Schematic of a generic GaN-on-silicon power transistor. Key areas for device optimisation using plasma processing are **1** – recessed ohmic contacts for low resistance, high field compatible source-drain contacts ; **2** – the gate-drain region to mitigate leakage current and dynamic on-resistance issues; **3** – the gate stack to control threshold voltage and minimise gate leakage current with minimal hysteretic effects. (b), (c) and (d) are specific gate stack solutions. (b) has a gate dielectric deposited on the GaN surface; (c) has a gate dielectric above a fluorine plasma treated region to tune threshold voltage; (d) has a recessed gate prior to dielectric deposition

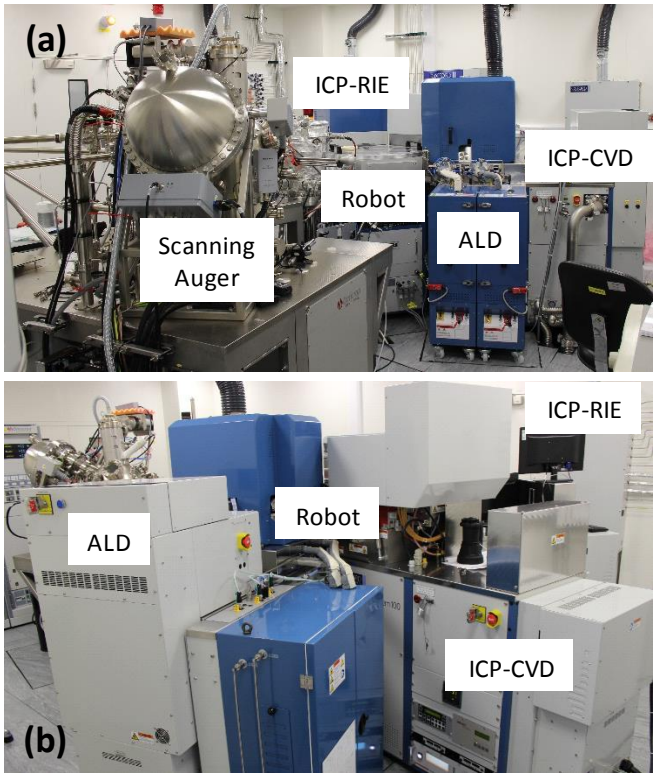


Figure 2. Views of clustered plasma process chambers. A central robot handler allows movements of wafers between reactive ion etch, atomic layer deposition and chemical vapour deposition chambers without atmospheric exposure. Also clustered is a scanning Auger microscope to enable in-situ mid-process surface analysis.

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# 10 - Challenges to dielectric processing for E-mode GaN

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**Status**

The growth of ultrathin dielectric layers into GaN-based devices incorporating metal-insulator-semiconductor (MIS) structures has been extensively investigated as a method of minimising gate leakage currents, which are lost through the gate by electron tunnelling, leading to poorer power efficiency and electrical noise. For normally-off, enhancement mode devices, low off- currents are necessary to reduce the static power consumption and ensure fail-safe operation. The incorporation of various oxide or nitride dielectric materials into GaN-based heterostructures has been explored previously using a range of conversion (e.g. oxidation or wet chemical methods) and chemical (e.g. CVD or ALD) or physical vapour (e.g. sputtering or evaporation) growth processes. Regardless of the dielectric or fabrication process used, the discontinuity (see figure 1) at the resulting insulator-semiconductor interface gives rise to electrically active interface trap states. These can influence device performance, by acting as remote impurity scattering centres that can either lower the carrier mobility ($\mu$) [1] or influence the threshold voltage ($V_{th}$) [2]. The insulator itself may also contain deleterious intrinsic charge traps. Furthermore, the insulator will have valence band and conduction band offsets with respect to the III-nitride (e.g. GaN, AlGaN, InAlN etc) which will influence the carrier confinement properties in the semiconductor [3]. Despite these issues, both depletion-mode and enhancement-mode insulated-gate GaN-based transistors have been realised through the development of surface pre-treatments; dielectric film deposition processes; and post-deposition heat treatments [4].

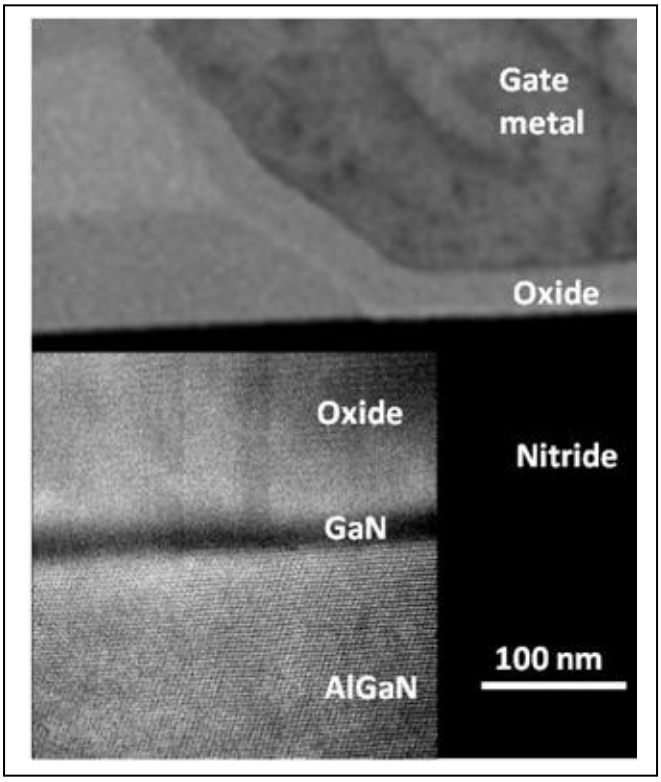
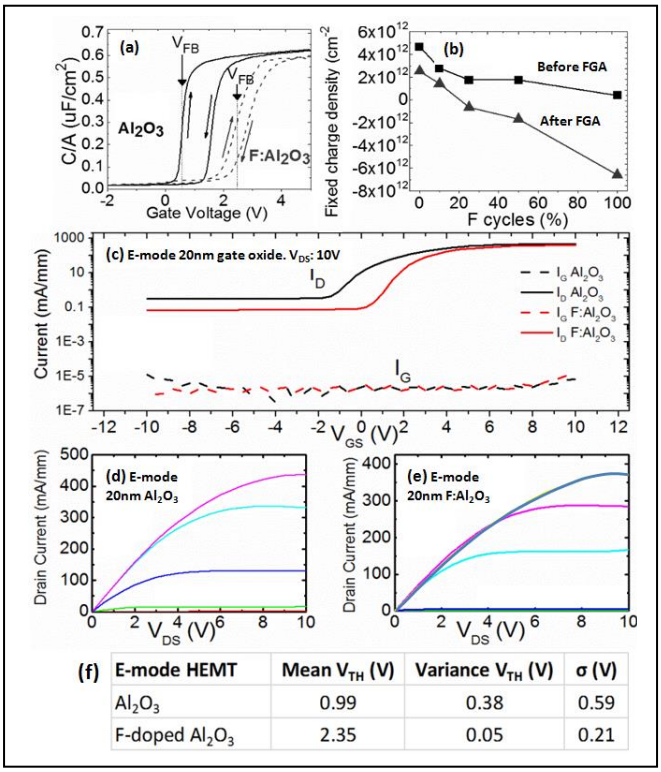



**Figure 1.** Cross section TEM of the gate MIS structure in a GaN-based MISHEMT. The inset shows a high resolution dark field image indicating the disruption of atomic lattice structure in the GaN cap adjacent to the $Al_2O_3$ dielectric layer.

**Current and Future Challenges**

The integration of insulted gate dielectric with III–N semiconductors continues to represent a significant hurdle to be overcome before E-mode MIS transistors can reach maturity. The dynamic charging of deep traps at the dielectric-semiconductor interface is associated with $V_{th}$ instability and long term reliability of the material system under electrical stress is uncertain. To begin to address some of these issues, gate dielectrics have been explored in the fabrication of E-mode MIS GaN-based devices. Two of the approaches explored to date include: (1) fluorine-doping which is used to passivate or neutralise positive charges at the semiconductor surface or in the dielectric itself; or (2) by recessing the gate by selectively etching the barrier layer in the region under the gate electrode. One example of F-doping via, $CF_4$-plasma treatment in the gate region of an AlGaN/GaN high-electron-mobility transistor (HEMT) [5]. Exposure to the plasma implants $F^-$ ions into the AlGaN barrier and underlying GaN-channel. After application of an ALD $Al_2O_3$ gate - dielectric, the F-doped semiconductor acts as a source of fluorine that diffuses into an $Al_2O_3$ dielectric compensating its intrinsic positive charge. It was reported that the $V_{th}$ increases with gate dielectric thickness, exceeding 3.5V for gate dielectrics 25 nm thick. Using in-situ fluorine-doping during ALD $Al_2O_3$ deposition, we reported the control of $V_{th}$ in enhancement-mode AlGaN/GaN MIS-HFETS [6]. When compared to the undoped dielectric, the F-doping caused positive threshold voltage shift (see figure 2) and a reduction of positive fixed charge in the gate oxide.




(f)

| E-mode HEMT | Mean $V_{TH}$ (V) | Variance $V_{TH}$ (V) | σ (V) |
|---|---|---|---|
| $Al_2O_3$ | 0.99 | 0.38 | 0.59 |
| F-doped $Al_2O_3$ | 2.35 | 0.05 | 0.21 |

Figure 2. Effect of F-doping in $Al_2O_3$ in E-mode MOS capacitors (a) Reduction in CV hysteresis.(b) Influence of forming gas annealing on fixed charge density. Effect of F-doping in $Al_2O_3$ in E-mode MISHFETs (c) $I_D$ and $I_G$ versus $V_{GS}$ for 20 nm $Al_2O_3$ and F:$Al_2O_3$. (d) $I_D$ versus $V_{DS}$ for 20nm $Al_2O_3$ gate oxide with $V_{GS}$ from -4V to +6 V in 2 V steps. (e) ID against $V_{DS}$ for 20 nm F:$Al_2O_3$ gate oxide with $V_{GS}$. (f) Mean, variance, and standard deviation (σ) of $V_{TH}$ for 15 of each type of MISHFET.

A dielectric is exploited in recessed gate MIS-HEMT, to suppress gate leakage current and increase the on-state gate swing. However, in the case of E-mode MIS-HEMTs, $V_{th}$ hysteresis can be caused by

large positive gate voltages due to 2DEG entering the deep trap states at the oxide/III-nitride interface. A demonstration of how this effect can be mitigated is through the application of an $Al_2O_3$/AlN gate stack insulator [7]. The insertion of a 2-nm thin plasma enhanced ALD AlN interfacial passivation layer yielded a device with a $V_{th}$ of +1.5 V, a current density of 420mA/mm and an OFF-state breakdown of 600V with low drain leakage of 1.7μA/mm.

The preceding discussion has focused on n-type (2DEG) channel MIS E-mode devices, however the realisation of p-type (2DHG) devices has received less attention to date. A significant advance in this respect, has been the demonstration of complementary metal–oxide–semiconductor (CMOS) GaN field-effect-transistor technology [8]. This landmark achievement is considered in more detail elsewhere in this roadmap. In the context of the dielectric employed, an MOCVD AlN/SiN dielectric stack was exploited as the gate oxide for both NMOS ($\mu_e$ - 300 $cm^2$/V-s) and PMOS ($\mu_h$ - 20 $cm^2$/V-s) transistors. The devices were used to demonstrate a functional inverter integrated circuit.

Significant advances have been made in the integration of gate dielectrics into III-N transistors, with the main purpose of minimising leakage currents in normally-off devices. A variety of dielectric materials have been assessed, using different deposition processes, but the main focused has been on $SiO_2$, $SiN_x$ and $Al_2O_3$. The continuing challenges for E-mode MIS devices are: (1) the minimisation of charge trap densities at the insulator/semiconductor interface across the range of barrier and channel III-nitride materials; (2) minimisation of the effect charging – discharging of trap states which gives rise to $V_{th}$ instability; (3) minimisation of the influence of bulk and border traps within the insulator dielectric itself which may impair the long term gate reliability and performance; (4) the development of processes and materials matched to the thermal budget of the device manufacture and the longer term in-field operating environment; (5) lastly addressing issues (1)-(4) in the context of PMOS E-mode devices [9, 10].

**Advances in Science and Technology to Meet Challenges**

The challenges of processing dielectrics for E-mode GaN MIS-based device technology are comparable to those encountered over the last two decades in the field of silicon CMOS. Fundamentally, the processing of dielectrics requires atomic-scale control over the preparation of the semiconductor surface, followed by assembly of the insulator with sub-nanometre precision over non-planar substrates comprising of a mixture of materials. The strategies for preparing III-nitride semiconductor (e.g. GaN, AlGaN, AlInN etc) surfaces for subsequent dielectric deposition will continue further development for both NMOS and PMOS technologies. Where these are combined on the same wafer for nitride-based circuits will add process complexity. The solution to this problem will have to involve removal or conversion of any unwanted native contamination at the semiconductor surface. Ideally the semiconductor surface would be atomically planar after preparation. Various wet and dry (e.g. thermal and plasma) processes have been explored to passivate and protect the semiconductor. It seems likely that future strategies may rely more on capping the semiconductor wafer in-situ at the end the III-nitride growth process to mitigate the problems associated with post-growth environmental exposure. Obvious candidates for this would be AlN- or SiN-based materials, but could include others. Alternatively, advanced strategies for the dielectric deposition process (e.g. ALD MOCVD PECVD, LPCVD or some physical vapour deposition method), would involve an in-situ preparation step. As an example, one prospect might be the

introduction of an atomic layer etching (ALE) step to remove unwanted native oxide / contamination. ALE could be applied to remove disordered gallium oxide / aluminium oxide residue, prior to the ALD of a "dielectric – quality" ALD layer. To realise this, further research would be required to develop ALE chemistries for the group-III oxides and nitrides.

In addition to surface pre-treatments, there is clearly scope for the development of improved dielectrics. Alternatives to the existing candidates, future developments might target multilayer dielectric stacks to target the overall gate capacitance, whilst enhancing resistance to gate-leakage. Multilayer gate stack might also be exploited to engineer band alignments to both the underlying semiconductor and the gate contact material. Current research has identified the use of fluorine- or hydrogen- "doping" in $Al_2O_3$ or $SiN_x$, as a method of "defect engineering" to neutralise or passivate traps in dielectric materials. There is clear scope for basic materials research to take this defect engineering further to enhance the electrical properties of gate dielectrics.

**Concluding Remarks**

The incorporation of MIS structures within E-mode GaN transistors offers a range of device design freedoms to realise monolithic GaN power IC, with reduced parasitic inductance and more efficient power switching at high frequencies. It is foreseeable that the development of gate dielectrics will be tuned to meet three overarching challenges. Firstly at the materials level, the dielectric stack will mitigate the effects of detrimental traps or defects within the dielectric and at the nitride semiconductor-dielectric interface, with negligible gate-leakage and maximum resistance to high-voltage electrical breakdown. Secondly, at the manufacturing stage, processing technologies will be required incorporate the dielectric into increasingly complex device architectures within the bounds of thermal budget. Thirdly, the development of dielectrics will be driven by the operational issues of life-time and reliability in the extreme environments experienced by GaN-based device technology.

**Acknowledgements**

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# 11 - Future Applications, Roadmap for GaN ICs

Dan Kinzer and Stephen Oliver, Navitas Semiconductor

**Status - The Power GaN Progression**

With Gallium Nitride (GaN) already established as a leading material for LED / opto applications and for RF amplifiers, this wide band-gap material emerged as an interesting academic option for discrete power devices around the turn of the century. Today, discrete GaN power devices have been qualified to JEDEC standards from 80 to 650V, using technology that has advanced from complex, costly and slow 'cascoded d-mode' implementations in highly-inductive through-hole packaging, to true single-die, e-mode devices in SMT formats [1]. However, significant system factors still exist which restrict practical switching speeds, negate the performance advantages of GaN and, as a result, have slowed market adoption.

The answer to this problem is derived from the lateral structure of GaN itself. A two-dimensional electron gas (2-DEG) with AlGaN/GaN heterojunction gives very high mobility in the channel and drain drift region, so resistance is much reduced compared to both Si and SiC. Circa 2009, early GaN power IC technology was published from university research [2]. The ability to integrate multiple power switches on a single chip is a big advantage for GaN power ICs. Isolating substrates began with sapphire and silicon carbide, though it was clear that an ability to grow GaN onto Si substrates enabled a cost structure and an ability to use existing large-diameter wafer fabs that would be a big cost and capacity advantage. Since Si is conductive, this introduces an additional challenge, of handling the substrate potential, and the way that it interacts with the power device.

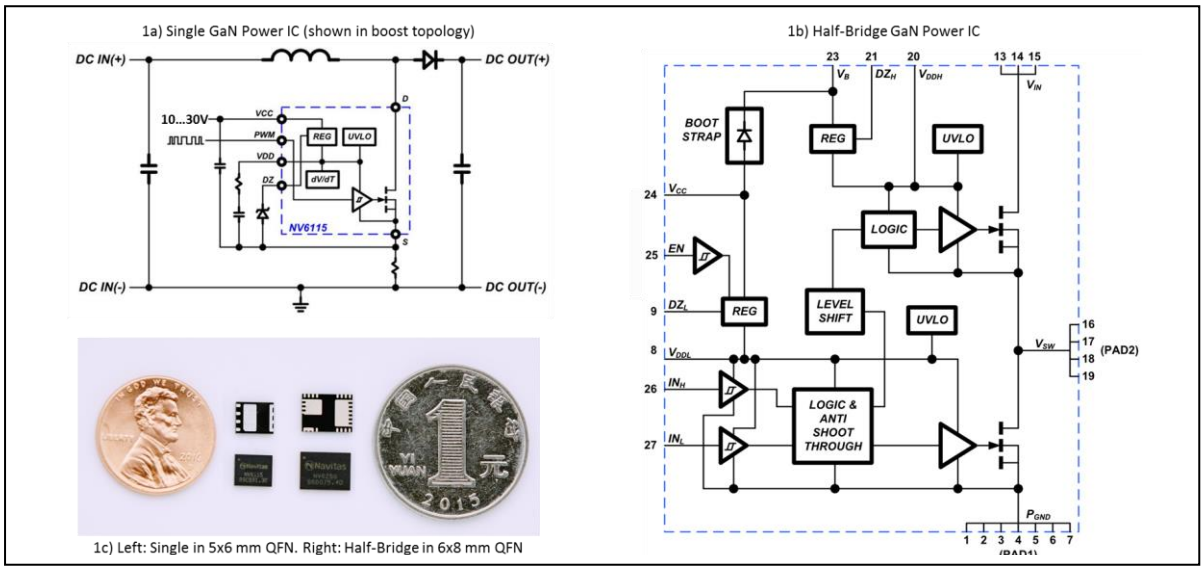


**Figure 1.** 650 V GaN Power ICs: 1a) single, 1b) half-bridge, 1c) package types, dimensions (Navitas Semiconductor)

**Current and Future Challenges - The GaN Power IC**

AllGaN™ is the industry's first GaN Power IC Process Design Kit (PDK), and allows the monolithic integration of 650V GaN IC circuits (drive, logic) with GaN FETs [3]. This proprietary PDK is remarkable given the restricted device-level tool-set, e.g. no p-channel devices are available. This monolithic integration is impractical using vertical GaN, d-mode GaN or SiC technologies.

For high-frequency operation, the most critical achievement has been the monolithic integration of GaN driver and GaN FET. In discrete implementations, the exposed GaN gate is vulnerable to noise

and potentially damaging voltage spikes. Even when the GaN FET is included in a co-packaged, multi-chip module, the impedance between Si driver output and GaN FET gate leads to losses and potentially unstable operation. Only a monolithic solution delivers the required speed, efficiency and robustness [4]. From the driver integration, we can then consider 'higher-order' functions of the power IC such as inclusion of logic, start-up protection, dV/dt control, dV/dt robustness, and ESD to create full-function GaN Power ICs. Another major step is the combination of two FETs plus all associated drive, level-shift, bootstrap charging, and protection features (e.g. shoot-through prevention, UVLO, etc.) into a complete half-bridge power IC. Now, PWM ICs need simply to generate two, low current, ground-referenced digital signals and the half-bridge GaN power IC completes this ubiquitous building block.

Since the 1990s, when Si-based junction-isolation (JI) level-shifting techniques were introduced, power designers have searched for higher-efficiency and higher-frequency methods. Hybrid level-shifter techniques, e.g. capacitive- or inductive-coupling, have been introduced but the disparate semiconductor technologies used, plus complex assembly techniques meant large and expensive modules. The 650 V GaN Power IC enables the true, next-generation, monolithic-integration approach and results in a level-shifter which has 10x lower loss than Si and 3x lower than the best-in-class hybrids.

**Advances in Science and Technology to Meet Challenges – Real-World Applications**

GaN is a low-loss, fast-switching material and enables a range of new high-frequency topologies to move from academic to commercial applications. The easy-to-use GaN power IC building block now becomes the core enabler for high frequency, soft-switching topologies such as active clamp flyback (ACF), critical conduction mode (CrCM) and totem-pole power factor correction (PFC) and LLC DC-DC circuits to enter mainstream markets [5], [6], [7]. In parallel, new magnetic materials have been released to production with high-efficiency operation up to 5 MHz. Multi-MHz DSP controllers are available for higher power applications and new high-frequency, cost-effective ASICs are being introduced to enable adoption in price-sensitive markets such as smartphone and laptop chargers. High MHz-range frequency with the simultaneous increase in efficiency delivers cost-effective, increased power density [8].

Practical examples of soft-switching topologies are shown below in Figure 2. Note that the mechanical construction/assembly techniques used are industry-standard, and readily-available at low cost.

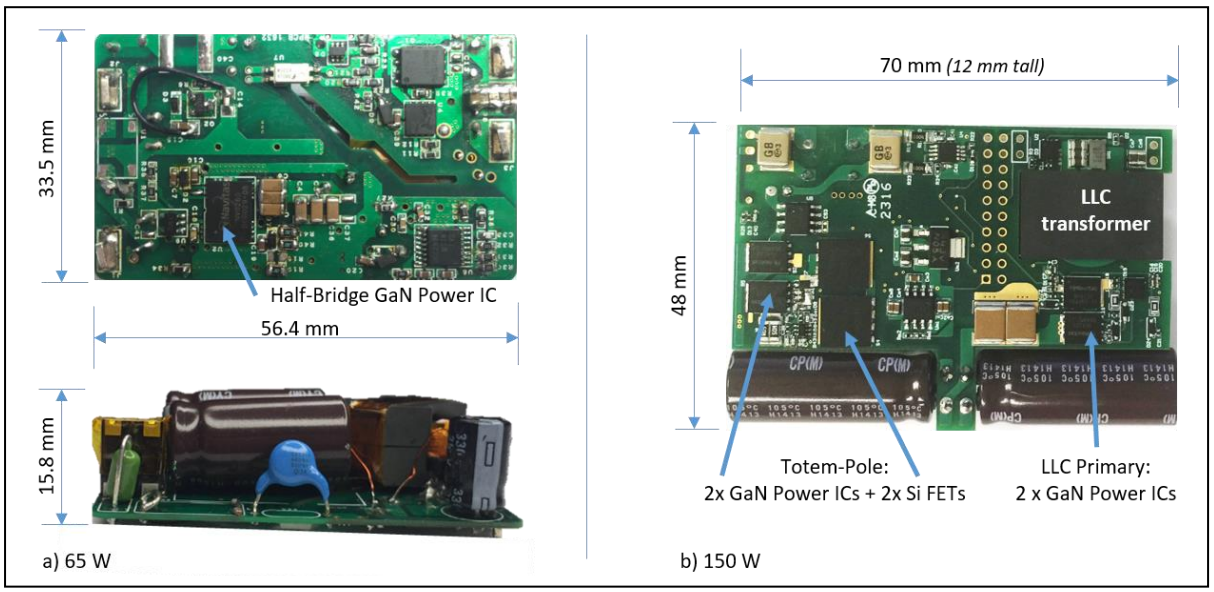


Figure 2. Examples of AC-DC converters using GaN Power ICs;
a) 65 W Active Clamp Flyback at 300 kHz using commercial control ASIC and Half-Bridge GaN Power IC, 94.5% peak efficiency at full load, 1.5 W/cc (24.6 W/in$^3$) uncased power density (Navitas Semiconductor), and
b) 150 W Totem-Pole PFC plus LLC at 1 MHz using single GaN Power ICs, >95% peak efficiency at full load, 3.7 W/cc (60 W/in$^3$) uncased power density. DSP controller not shown (courtesy of CPES, Virginia Polytechnic).

The same GaN Power ICs may be applied in high-power, multi-kW applications, with one example being a 3.2 kW, 1 MHz, AC-48 V converter prototype with 65 W/in$^3$ power density [9]. Here, the single devices are paralleled to achieve lower $R_{DS(ON)}$ and interleaving techniques are used for the Totem-Pole PFC and LLC sections.

## Concluding Remarks - Major Accomplishments, Major Opportunities

The last 20 years have seen GaN's progression from RF to power discrete and now to the first generation of AllGaN power ICs. This has enabled advanced, soft-switching topologies to enter the commercial marketplace. Next-generation monolithic integration (e.g. advanced I/O features, over-current and over-temperature protection) will enable even higher levels of efficiency, power density and reduced system cost.

## Acknowledgements

The authors wish to thank Dr. F.C. Lee (CPES, Virginia Polytechnic) and Dr. A.Q. Huang (FREEDM Systems Center, North Carolina State University) for their pioneering MHz application work with GaN Power ICs.

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# 12 - Potential of Polarisation Super Junction Technology in Gallium Nitride

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**Status**

Amongst many semiconductors, Silicon Carbide (SiC), Gallium Nitride (GaN) and Diamond can offer significant system level benefits and have the potential to meet the anticipated power densities by 2025 [1]. GaN offers similar performance benefits to SiC, but with a greater potential for cost-reduction as well as higher frequency. Price advantage over SiC is also possible because GaN power devices can be grown on substrates that are larger and less expensive than SiC. Since the first report of high density 2-Dimensional Electron Gas in 1991 [2] and High Electron Mobility Transistors in 1993 [3], GaN has gained traction and now discrete GaN transistors are emerging as commercial products. Their performance is however limited to about 1/5$^{th}$ of their potential capability by slower external silicon gate driver circuits required to control them. Si circuits have a limited operating temperature range and inherently efficient GaN devices are forced to slow down, leading to failure and severe derating of efficiency. The dual (Si & GaN) technology approach impacts cost deleteriously. By monolithically integrating control circuits with power devices on a single GaN technology platform the efficiency can be greatly increased, and cost reduced. Moreover, because of the difficulty in obtaining p-channel devices, integrated circuits (ICs) thus far demonstrated are made of n-channel devices.

**Current and Future Challenges**

In GaN-on-Si technology, the breakdown voltage is primarily determined by the GaN buffer and therefore thick buffer and transition layers are necessary to sustain high voltage, which make the wafers more susceptible to bowing and crack generation. The inherent tensile stress due to mismatch in lattice constants and coefficients of thermal expansion in such structures can also compromise the reliability of devices. Lack of avalanche capability or non-destructive breakdown behaviour, necessitates over-rating the device breakdown voltage for a given application. Moreover, there is a significant level of defects in layers and understanding of these defects and their relationship with device reliability is necessary. The conventional GaN technology uses metal field plates. However, the distribution of the electric field is not uniform, which impacts breakdown voltage along with rendering such devices to be sensitive to current collapse during high voltage switching. The field distribution is also highly sensitive to changes in charges accumulated in the insulators sandwiched between the semiconductor surface and the field plates. Realizing such high voltage devices also requires sophisticated processing capability for formation of precise field modulating plates. An alternative solution for manufacturing low-cost high-voltage GaN power switching devices, which can overcome some of the above-mentioned challenges is the Polarisation Super Junction (PSJ) technology, which is described in the next section. This technology is also a highly promising candidate for the fully GaN based power ICs.

**Advances in Science and Technology to Meet Challenges**

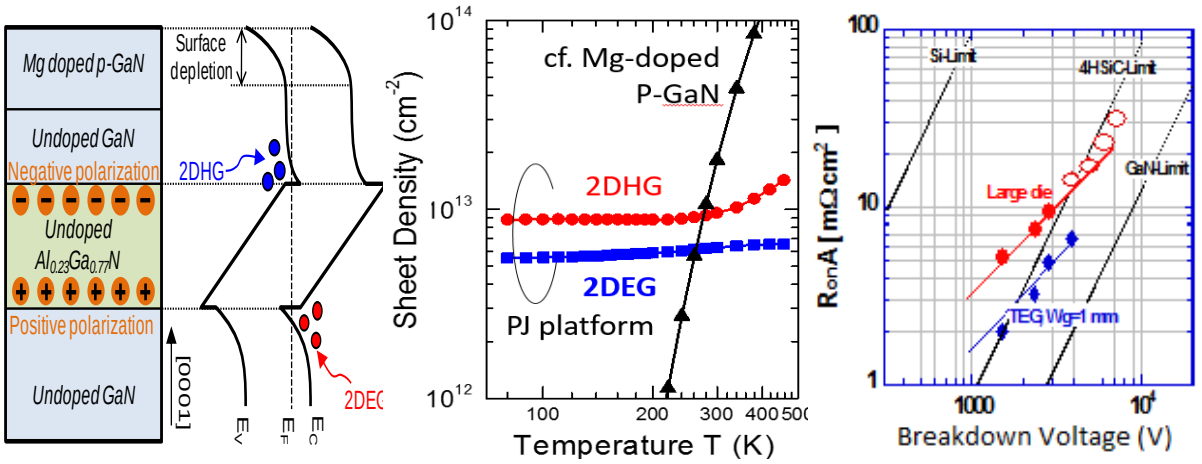


**Figure 1 (left): Double heterostructure in GaN [5]; Figure 1(middle) Measured 2DEG and 2DHG through Hall Effect measurements; Figure 1(right) Variation of measured specific on-state resistance with breakdown voltage of PSJ-HFETs against calculated unipolar 1-D material limits of Silicon, SiC and GaN [8].**

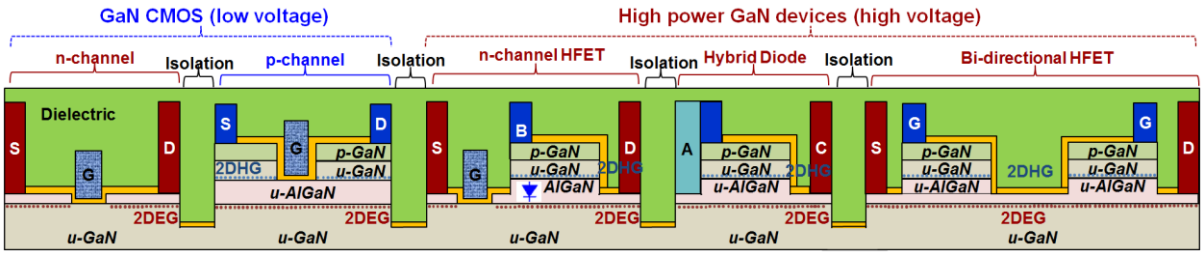


**Figure 2: Proposed PSJ Platform for Monolithic Power Integrated Circuits. Please note that the substrate is not specified. However, thin sapphire is the most cost-effective option because of the use of uniform thickness of 1 µm u-GaN buffer layers to serve for both low as well as high voltage devices and provide full electrical isolation (critical requirement for monolithic integration).**

In 2006, a polarisation junction (PJ) concept was proposed based on the charge compensation of positive and negative polarisation charges at heterointerfaces of a GaN/AlGaN/GaN structure [4]. This was followed by the successful demonstration of GaN double heterostructures, grown along the (0001) crystal axis, where high density positive and negative polarisation charges coexist at the AlGaN(000$\bar{1}$)/GaN(0001) interface with accumulated two-dimensional electron gas (2DEG) and two-dimensional hole gas (2DHG) accumulated at the GaN(000$\bar{1}$)/AlGaN(0001) interface respectively, as shown in Fig 1 (left) and Fig 1(middle) which has since enabled a Polarisation Super Junction (PSJ) technology [5]. Like the Superjunction in Si, PSJ enables linear scaling of breakdown voltage with increase in thickness or length of the drift region and with performances beyond that of 1-D 4-H Silicon Carbide limit, as shown in Fig 1(right). Over the past few years, high performance diodes, transistors as well bidirectional switches have been demonstrated [6,7]. Enhancement-mode PSJ-HEMTs have also been reported with most recent results of large (4 X 6 mm$^2$) and small devices made on Sapphire substrates showing with breakdown voltages beyond 3 kV [8]. Moreover, due to the effective lateral charge balance and field distribution, these devices fabricated on Sapphire substrate show no current collapse. One of the key attributes of the PSJ technology is that it is viable to make both NMOS as well as PMOS circuits, and CMOS inverter operation of a monolithic P- and N-channel MOSFETs has been demonstrated on this platform [9]. This technology also paves way for bidirectional switches with integrated diodes. This device is well suited for a variety of applications and for solid state circuit breaker because, PSJ offers the possibility of realising much lower saturation currents than conventional HFETs [5], while maintaining ultra-low on-state resistance. Thus, Polarisation Super Junction technology can pave the way for high power density monolithic integration of various devices for a variety of applications, as shown in Fig. 2.

Most recently, the PSJ concept has been extended to Vertical GaN technologies and is termed as Vertical Polarisation Super Junction (VIPSJ) with predicted benefits of 2 orders of magnitude reduction in specific on-state resistance in comparison to SiC at 1 kV rating [10].

**Concluding Remarks**

There are several scientific, technological and manufacturing challenges that need to be addressed before GaN power semiconductor devices can be considered mainstream. It is also becoming apparent that a transition from the general scheme of manufacturing power conversion circuits using discrete devices to that of a fully integrated power system-on-chip is anticipated to be a prerequisite to fully harness the high-frequency power switching benefits of GaN. To conclude, GaN PSJ technology will be instrumental in shaping a viable and a new era of an integrated power electronics for ultra-high-power density converters.

**Acknowledgements**

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# 13 - Technological Challenges in Next-Generation GaN-based Power Integrated Circuits

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**Status**

Si-based lateral power devices have been widely utilized in high-frequency and low-power converters for ratings of up to several hundred watts [1]. On the other hand, GaN-based heterojunction field-effect transistors (HFETs) utilizing polarization-induced 2D electron gas (2DEG) are emerging components for such high-frequency converters. GaN-based discrete devices up to 650-V rating are commercially available now. The development of GaN growth technology on conductive Si substrates has largely contributed to the improvement in the device performance and decrease in cost [2]. As a next step, towards achieving high intrinsic switching capability of GaN devices, monolithic integration of GaN-based converter circuits will be necessary. Area-specific on-resistances of GaN-HFETs are already two orders of magnitude smaller than those of Si-based lateral power devices. Owing to this significant footprint reduction, high output powers of up to several kilowatts can be expected in GaN-based monolithic converters. In this article, two technological challenges are addressed: the "crosstalk effect" and "heat dissipation" in next-generation ultra-high-frequency monolithic power integrated circuits (ICs). These issues are quantitatively discussed using simple analytical models.

**Current and Future Challenges**

As an example of GaN power ICs, if an integrated half-bridge circuit on a conductive Si substrate as shown in Fig. 1 is assumed with the following parameters: voltage rating of the GaN devices are 600 V, input voltage $V_{IN}$ is 400 V, 2DEG density $N_s$ has a conventional value of $10^{13}$ cm$^{-2}$, and dielectric constant $\varepsilon$ of the GaN-based epilayer is $9.0\varepsilon_0$.

Firstly, the "crosstalk effect" is discussed. In discrete GaN devices, the substrate potential is shorted with the source electrode. The conductive Si substrate acts as a back-side field plate contributing to the suppression of current collapse. However, in an IC, it induces a significant increase in the on-resistance of the high-side transistor [3]. This is because the 2DEG of the high-side transistor interacts with the substrate potential through the GaN epilayer capacitance $C_{epi}$. During the on-state of the high-side transistor, the input voltage $V_{IN}$ is directly applied to $C_{epi}$, inducing a 2DEG density reduction $\Delta N_s$:

$$q\Delta N_s = C_{epi}V_{IN} / A = \varepsilon V_{IN} / t_{epi}, \qquad (1)$$

where $q$ is the electron charge, $A$ is the GaN device area, and $t_{epi}$ is the GaN-based epilayer thickness grown over silicon substrate. If we consider a 2DEG density reduction of 10% (i.e., 10% on-resistance increase), the calculated $t_{epi}$ is 20 μm. In comparison with a GaN-based epilayer in conventional discrete devices (3-5 μm), power IC applications require an epilayer which is thicker by five times.

Next, the issue of "heat dissipation" challenges are discussed under hard switching condition. When the gate drive speed is sufficiently high, power loss of the hard-switching circuit (Fig. 1) reaches the minimum value. Under the minimum loss condition, the heat density $HD$ of the GaN chip can be expressed as

$$HD = Q_{oss}V_{IN} f / A = qN_s V_{IN} f, \qquad (2)$$

where $Q_{oss}$ is the output charge of each GaN transistor and $f$ is the the output pulse-width modulation frequency. Eq. (2) implies that a charge $Q_{oss}$ is supplied from the voltage source $V_{IN}$ during every switching period, and the energy is consumed as joule heat in the GaN chip. Fig. 2 shows the heat density calculated using Eq. (2). Although high-frequency operation is expected in hard-switched GaN

monolithic converters, the estimated heat density is unacceptably high. For example, it is 6.4 kW/cm$^2$ at 10 MHz.

**Advances in Science and Technology to Meet Challenges**

The substrate material for the growth of GaN-based layers is a key element of power ICs. Because conductive Si substrates induce the crosstalk effect, novel platform substrates are required for next-generation ICs, especially for high-voltage and high-frequency applications. GaN-on-silicon-on-insulator (SOI) technologies are a promising solution which can enable CMOS compatibility in the GaN device fabrication process [4, 5]. The contribution of the back-side field plate effect is also obtained through substrate contact from the front side [5]. However, a several-μm-thick $SiO_2$ buried layer will be required to sustain 600 V or more. The thermal conductivity of $SiO_2$ is two orders of magnitude smaller than that of Si. Therefore, heat dissipation from integrated GaN devices on an SOI substrate will be big challenge. Furthermore, GaN power device technologies on insulator sapphire substrates are equally promising candidates [6, 7] because they yield high-quality GaN crystals. However, on such insulator substrates, current collapse must be eliminated without the support of the back-side field plate effect. Effective lateral electric field management strategies will be necessary, such as polarization superjunction technology [6].

In addition, other emerging candidates must be considered. Because the thermal conductivity of SiC is three times higher than that of Si, GaN technologies on highly resistive SiC substrates have been widely used in RF applications and are also emerging candidates in power converter applications. Finally, GaN-on-diamond technology might be the ultimate solution to the heat dissipation issue because diamond has the highest thermal conductivity [8-10].

**Concluding Remarks**

In next-generation GaN-based power ICs, device isolation technologies are a key challenge, especially in high-voltage applications. GaN-on-SOI and GaN-on-sapphire technologies are promising candidates from this perspective. In addition, thermal management is a key issue. Area-specific on-resistance has been a major benchmark parameter of GaN-HFETs. In addition, the minimization of area-specific "thermal-resistance" will be a key strategy in GaN-based IC development. Therefore, GaN device technologies utilizing high-thermal-conductivity substrates such as SiC and diamond are also emerging as platform substrates for GaN power ICs. However, on any platform, potential advantages in performance and cost should be considered from the system level viewpoint.

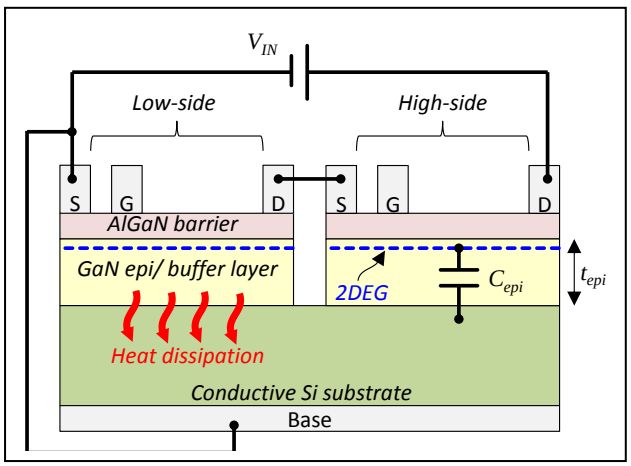


**Figure 1.** Schematic cross section of monolithic half-bridge circuit on conductive Si substrate.

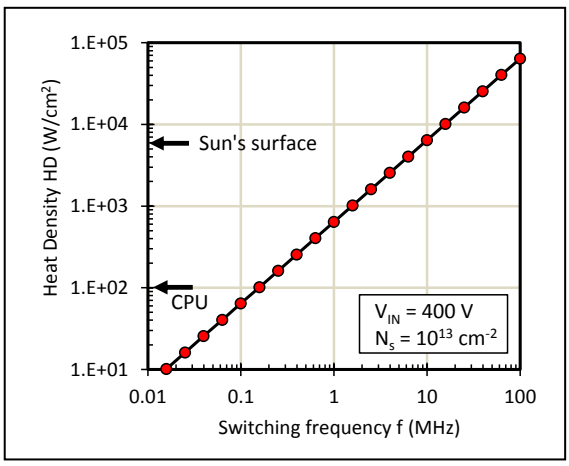


**Figure 2.** Calculated heat densities of GaN chip depending on output frequency under hard switching condition.

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# 14 - GaN CMOS: fact or fiction?

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**Status**

GaN power transistors have demonstrated unprecedented switching speed [1]. At high switching speed, parasitic inductance in the power loop as well as in the drive loop causes large voltage overshoot [2]. In current practice, the GaN switch is often intentionally slowed down to avoid catastrophic failure and additional power consumption induced by the voltage overshoot [3]. To take full advantage of the high-speed GaN switch, one need to eliminate the parasitic inductance by monolithically integrating power switches and their gate drivers. The gate driver typically uses a Totem-Pole topology with a pair of complementary N-type and P-type transistors. The complementary transistors eliminate static power consumption. GaN CMOS technology is needed to realize monolithic GaN power IC integrating high-voltage GaN transistors with low-voltage N- and P-type GaN transistors on the same chip.

The monolithic GaN power IC, as shown in Figure 1, minimizes interconnect parasitic between power switches and gate drives. Reduction of interconnect parasitic enables efficient power switching at high frequencies. At high frequencies, the size of passive components can be drastically reduced. Reduction of interconnect parasitic also enables active control of switching trajectory with minimal time delay. Active control of switching trajectory mitigates device stress and improves the reliability. The monolithic GaN power IC enables modular architecture where a number of power switching unit cells, e.g. half bridge, can be stacked in parallel and in series to scale the current and voltage handling capability. The monolithic GaN power IC enables cost reduction by cutting the assembly and packaging cost, as well as by using the modular architecture consisting of standardized switching unit cells.

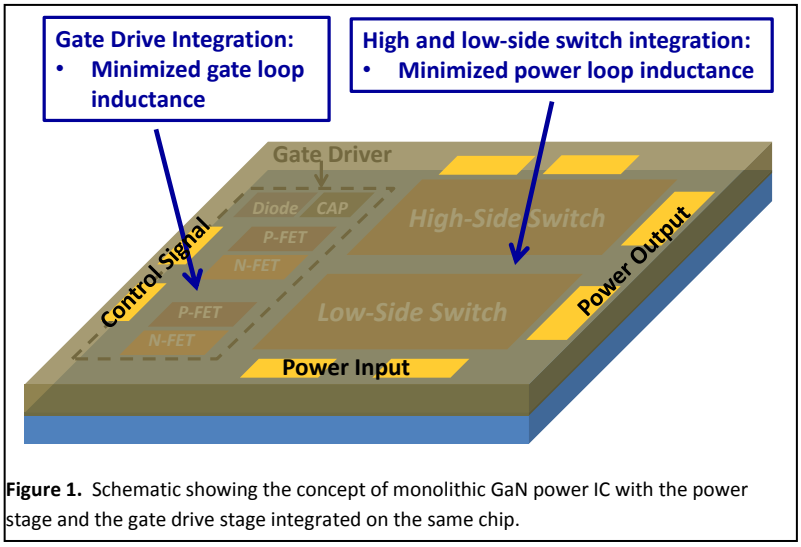


**Figure 1.** Schematic showing the concept of monolithic GaN power IC with the power stage and the gate drive stage integrated on the same chip.

**Current and Future Challenges**

N-type GaN high- and low-voltage transistors are readily available. Difficulty in making P-type GaN transistor and integrating it with the N-type transistor has been the major obstacle for realizing the GaN CMOS technology. There have been a few early studies on P-type GaN transistors [4]–[7], an attempt to integrate P- and N-type Schottky gate GaN transistors [8], and lately a demonstration of a working GaN CMOS IC inverter [9]. The GaN CMOS demonstration was achieved through selective area regrowth of P-type GaN transistor structure on a wafer with N-type GaN transistor epitaxy structure. Significant improvement of the GaN CMOS technology is needed to meet the performance requirement of the monolithic power IC. Specifically, there are two major challenges to be addressed. One challenge is the low output current, or high on-resistance, of the P-type transistor. The other challenge is the off-state leakage current of the P-type transistor when integrated with the N-type transistor. The low output current results from poor hole mobility, low mobile hole concentration, and

poor ohmic contacts. The off-state leakage is attributed to impurity contamination at the regrowth interface.

**Advances in Science and Technology to Meet Challenges**

Figure 2 shows device structure, IV curves, and on-resistance component breakdown of a P-type GaN transistor reported in Ref. 9. Inefficient P-type doping is the primary challenge responsible for the low current and the high on-resistance. Mg, with an activation energy as high as 0.2 eV in GaN, is used as the acceptor. High dopant activation energy leads to low concentration of mobile holes even at high doping level, therefore high contact resistance and high access resistance. Advance in P-type doping technique, e.g. polarization-assisted doping [10], has the potential of overcoming the doping challenge. Low hole mobility is another important factor responsible for the high on-resistance. Low hole mobility is caused by severe impurity scattering, interface scattering under the gate insulator, and large hole effective mass. In addition to enhancing doping efficiency, improvement of insulator-semiconductor interface is important for achieving better hole mobility and lower channel resistance. Strain engineering may increase the population of light holes, thereby improving the hole mobility. In addition to improving hole density and mobility, reducing or eliminating the spacings between gate and source/drain electrodes can effectively improve the on-resistance.

Improvement of epitaxy regrowth process is needed to eliminate the off-state leakage current shown in Figure 2. P-type transistors fabricated on P-type only wafers didn't show this off-state leakage. The off-state leakage is attributed to Si contamination commonly observed at the regrowth interface. The source of the Si contamination can be volatile organic silicon compound in the air ambient. A regrowth process avoiding such contamination is needed to integrate high-performance P- and N-type transistors.

Comprehensive study of gate dielectric in P-type transistors is also needed to ensure stable threshold voltage, and facilitate scaling to smaller gate lengths.

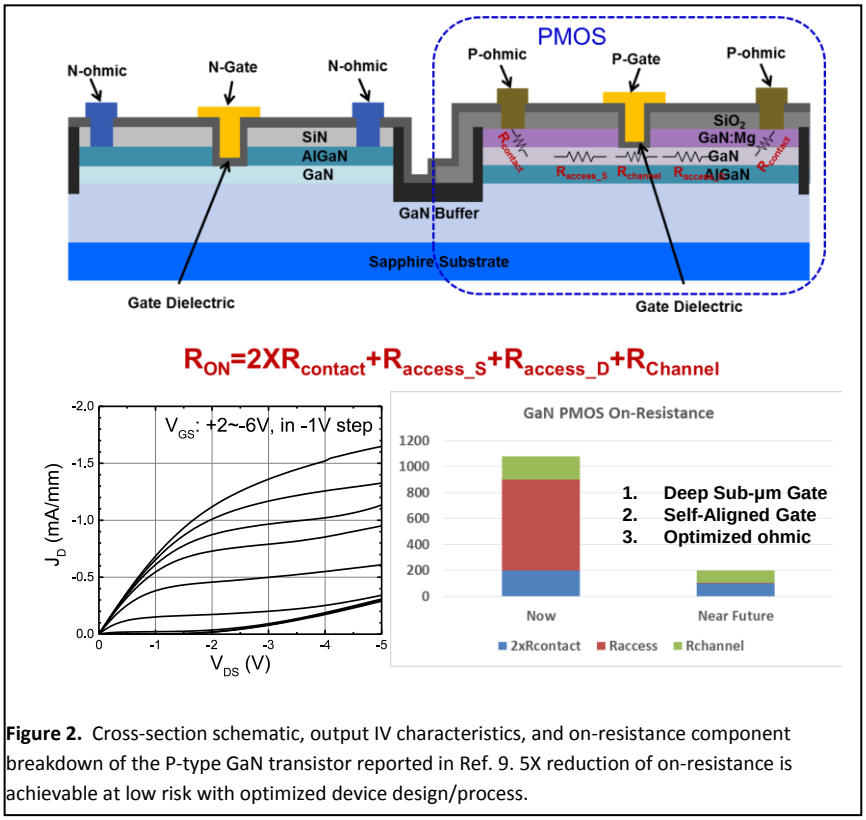


**Figure 2.** Cross-section schematic, output IV characteristics, and on-resistance component breakdown of the P-type GaN transistor reported in Ref. 9. 5X reduction of on-resistance is achievable at low risk with optimized device design/process.

**Concluding Remarks**

Monolithic power IC based on the GaN CMOS technology is essential for realizing and maximizing the performance/cost potential of GaN power electronics. Early work on GaN N/P-type transistors and GaN CMOS technology has proved that the GaN CMOS is a fact, not a fiction. Improvement of P-type doping and selective area regrowth is important for realizing high-performance GaN CMOS technology for monolithic power IC applications.

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# 15 - Assessing the limits of performance of p-type devices in GaN

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**Status**

P-type devices are required for integration of CMOS gate drivers and power devices to enable high frequency, high efficiency convertor systems on a chip in GaN. A D-mode p-channel HFET in GaN, utilising a low density (1x $10^{11}$ $cm^2$) polarization induced two dimensional hole gas (2DHG) as carrier was first demonstrated by T. Zimmermann *et. al* in 2004 [1]. It is more difficult to realise a normally-off (E-mode) operation, with negative threshold voltage $V_{th}$, since the 2DHG under the gate has to be depleted at zero gate bias. A recessed gate [2], and/or reduction of polarization charge via adjustment of the mole fractions [3] have been amongst techniques explored for E-mode operation, following logically from similar progression in n-type devices in GaN. However, these techniques are not easily transferrable, primarily because unlike a 2DEG in GaN, achieving a high density 2DHG is a challenge, and reported mobility of holes in a 2DHG, ranges no more than 6-43 $cm^2/Vs$ at room temperature [1,3].

**Current and Future Challenges**

The main challenge for a p-type MOSHFET in GaN is achieving a high threshold voltage $|V_{th}|$ to prevent false turn-on in PMIC applications, while maintaining a high $|I_{ON}|$ and $|I_{ON}/I_{OFF}|$ ratio. Achieving a $|V_{th}|$ of $|-2.0|$ $V$ is not feasible by etching alone, as it requires the thicknesses of the oxide and GaN channel layer to be reduced to undesirably small values ($\sim 5$ $nm$) [4]. On the other hand, achieving an E-mode operation by reducing the polarization charge via a reduction in the Al mole fraction leads to reduction in the density of both 2DHG and 2DEG, not only reducing the $|I_{ON}|$ in p-type devices but also deteriorating the performance of n-type devices on the same platform. Figures 1 (a) & (b) depict the on-current $|I_{ON}|$ and on-off current ratio $|I_{ON}/I_{OFF}|$ with threshold voltage $V_{th}$ of experimental p-channel HFETs reported in [2,3,5–7], highlighting the degradation of $|I_{ON}|$ as the device turns from D-mode to E-mode while $|I_{ON}/I_{OFF}|$ ratios improve with increasingly negative $|V_{th}|$. Except for the work of R. Chu [5] and G. Li *et. al* [7], which do not include an underlying 2DEG beneath the 2DHG, the activities can be summarised into two main barrier-layer platforms, ternary AlGaN and quaternary InAlGaN, both of which possess an inherent polarisation superjunction [8] that is eminently useful for management of the peak electric field distribution and reliability of GaN power devices. The best performing E-mode p-type device by gate recess so far, reported by Hahn *et. al* [3], resulted in an on-current $|I_{ON}|$ of $\sim 9$ $mA/mm$ at a $V_{th}$ of $-1.3$ $V$ and an on/off current ratio of $\sim 10^7$. In quaternary barriers, increasing the Al mole fraction leads to an increase in negative polarization charge, higher bandgap, and a smaller lattice constant, while increasing the In mole fraction has the opposite effect. Hence, by adjusting both Al and In mole

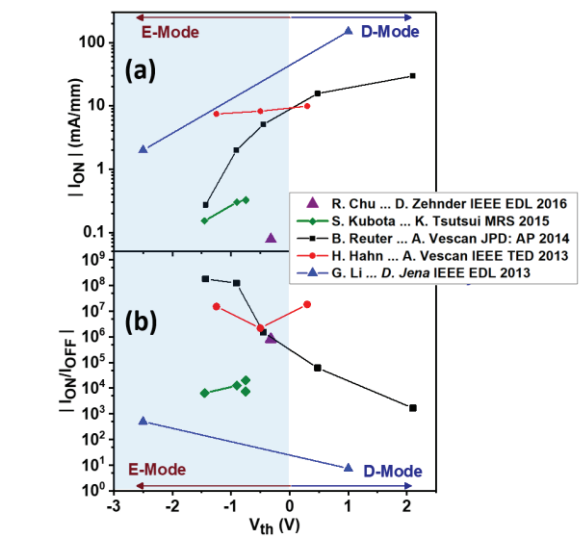


Figure 1. (a) on-current vs. threshold voltage, and (b) on-off current ratio vs. threshold voltage characteristics of the state-of-the-art p-channel HFETs reported to date.

fractions simultaneously, it is possible to tune the polarization and the bandgap of the barrier layer, independently, to some extent.

**Advances in Science and Technology to Meet Challenges**

A higher $|I_{ON}|$ requires a high density of 2DHG, nevertheless, for an overall lower parasitic resistance, as well as high on/off current ratio, requires a localised depletion of the 2DHG under the gate, so as to not affect the access regions. This can be achieved via an AlGaN cap between the oxide and GaN channel layers [9], where the barrier separating the 2DHG from the 2DEG can be either AlGaN or InAlGaN. As shown previously, for the device in Figure 2 (a), the additional polarisation charge introduced by the AlGaN cap not only depletes the 2DHG under the gate, but also minimises the trade-off between $|I_{ON}|$ and $|V_{th}|$ [4]. However, this approach demands a selective epitaxial regrowth of the AlGaN cap layer. Figure 2 (b) shows an alternate heterostructure, where in addition to the recessed gate, the 2DEG is biased via an additional base contact [6], thus acting as a secondary gate for the 2DHG. By applying a positive bias to the base contact $V_B$, the density of 2DHG can be reduced locally, without affecting other devices on the platform. In both the device structures (Figures 2 (a) & (b)), a 2DEG lying parallel beneath the 2DHG separated by an AlGaN/InAlGaN barrier contributes an additional parasitic capacitance which can be offset by increasing the barrier thickness.

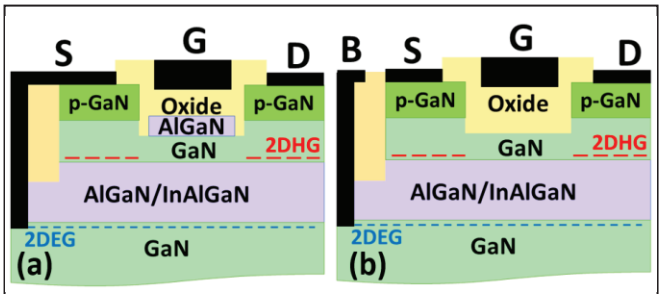


Figure 2. Schematic of p-type MOSHFETs with (a) an AlGaN cap and (b) a bias applied to the 2DEG.

Advancements in the growth of gate oxide are necessary to control and lower the impact of trap states at the oxide/AlGaN cap and oxide/GaN interfaces while at the same time lower the gate leakage current, for a reliable and replicable operation of these devices. The MOCVD growth of Mg doped p-GaN layer currently suffers from, large activation energy $(120 - 200\, meV)$ of Mg dopants and memory effect [10], which leads to poor hole density in p-GaN and a broader doping profile. Moreover, during the epitaxial growth at high temperature, Mg ions can diffuse into the GaN layer underneath, thus contributing to the leakage current and affecting the minimum channel thickness that can be achieved in manufacture. Therefore, novel doping techniques are required to obtain p-GaN layers with high hole density and sharper doping profile.

Other possibilities to boost the performance of p-type devices in GaN include, improving the hole mobility by tailoring the valence band structure in GaN, for example by the application of stress to lower the effective mass of holes or introduction of positive ions directly in the gate oxide to deplete the hole gas underneath.

**Concluding Remarks**

P-type devices in GaN are necessary in the long run to harness the full potential that GaN technology has to offer in achieving high efficiency power conversion. Despite the poor mobility of holes and challenges associated with Mg dopant, techniques to circumvent or limit their impact exist, although still in their infancy. More work is required for demonstrating their reliable operation and manufacturability at low cost.

**Acknowledgements**

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# 16 - 600V E-mode GaN Power Transistor Technology: Achievements & Challenges

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**Status**

Since the first confirmation of a 2DEG at the AlGaN/GaN interface in 1992 and the first availability of GaN-on-SiC radio frequency power transistors in 1998, nitride semiconductor hetero structure electron devices now constitute a hundred million dollar market for RF power. As regards power conversion applications, GaN-on-Si high voltage power transistors have been in development stage for the past decade with initial focus on depletion mode devices due to the inherent nature of the 2DEG. However most power electronic applications demand for enhancement mode devices. The first high voltage solution released to market in 2015 by TransPhorm [1] is based on a cascode configuration of a low voltage Si-MOSFET in series connection with a high voltage GaN MIS-HEMT to solve that issue. Following the progress of enhancement mode devices based on a p doped GaN gate module for low voltage GaN power transistors from EPC [2] we now see the first fully industrial qualified 600V true enhancement mode (E-mode) GaN power transistors on the market from Panasonic and Infineon [3-5]. These E-mode GaN power transistors are based on a fully recessed gate module with subsequent regrowth of a second AlGaN barrier with pGaN (see Fig. 1) on top for an excellent control of the threshold voltage independent of the drift layer carrier density [6]. pGaN is also used at the drain region as drain extension which improves the dynamic on state resistance to well below 10% even at high temperatures of 150°C and full rated drain voltage of 600V down with delay times as short as few hundreds of ns from blocking mode to settled on state resistance measurement. At the same time this drain sided pGaN region (see Fig. 1) also improves the robustness of the device to the required levels for hard switching applications [3]. The devices are offered in surface mount device packages allowing for designs with low loop inductances including top side cooled variants for enabling 3kW converters without need for paralleled devices (see Fig. 1). Recently it has been demonstrated that the gate module even allows for a >10µs short circuit robustness at full bus voltage of 400V when driven properly [7]. The technology has been implemented in a volume silicon power fab with a very high degree of equipment sharing with standard silicon processes to achieve economy of scale.

When comparing Infineon's CoolGaN™ technology to the state-of-the-art silicon super junction devices (Si SJ) as well as other wide band gap technologies on the market (see Table I) we see that all WBG technologies offer roughly the same order of magnitude improvement in output charge $Q_{OSS}$ per $R_{DSON}$ and two orders of magnitude improvement in reverse recovery charge per $R_{DSON}$. However, only E-mode GaN offers at the same time one order of magnitude of gate charge $Q_G$ improvement which makes it the perfect device for high frequency resonant switching. Resonant converters with 3kW power level operating at 350kHz without sacrificing peak efficiency of 98.4% demonstrate high density of 170W/in³ [8]. For hard switching applications the relevant figure-of-merit is the energy stored in the output capacitance ($E_{oss}$) and here recent developments in Si SJ devices have raised the bar significantly so that as of today only E-mode GaN can outperform Si. In combination with the lack of reverse recovery charge that enables the use of GaN devices in half bridge configurations new and simpler topologies like full bridge totem pole are possible.

| Device | Rating [V] | $R_{DSON}$ [mOhm] | $R_{DSON}*Q_{OSS}$ [mΩμC] | $R_{DSON}*Q_{RR}$ [mΩμC] | $R_{DSON}*E_{OSS}$ [mOhm*uJ] | $R_{DSON}*Q_G$ [mΩnC] |
|---|---|---|---|---|---|---|
| Si Super Junction [a] | 600 | 56 | 23.5 | 336 | 450 | 3800 |
| **GaN eMode** [b] | 600 | 55 | **2.2** | **0** | **350** | **320** |
| GaN Cascode [c] | 600 | 52 | 3.8 | 7.1 | 730 | 1460 |
| GaN Direct Drive [d] | 600 | 70 | 4.1 | **0** | 530 | n.a. |
| SiC DMOS [e] | 900 | 65 | 4.5 | 8.5 | 570 | 1950 |
| SiC TMOS [f] | 650 | 60 | 3.8 | 3.3 | 540 | 3480 |

**Table 1.** Benchmark of State-of-the-Art High Voltage Power Transistors: a) Infineon CoolMOS™ IPL60R065C7 Datasheet, b) Infineon CoolGaN™ Preliminary Datasheet ($Q_{RR}$ is exclusive of $Q_{OSS}$), c) TransPhorm Cascode TPH3205WS Datasheet, d) TI Direct Drive LMG3410 Datasheet, e) Wolfspeed C3M0065090J Datasheet, f) Rohm SCT3060AL Datasheet (all values given typical at 25°C incl. package).

*Current and Future Challenges.* One of the biggest challenges to release power GaN devices to the market has for sure been their reliability. The hetero epitaxial growth of the GaN buffer on silicon wafers unavoidably leads to lattice misfit dislocations and other growth defects. At the same time present lateral GaN devices differ from the established silicon power devices in many aspects as they are based on hetero junctions, differences in spontaneous polarizations and bulk/surface donors to generate the 2DEG instead of p and n dopings. The qualification of those devices therefore cannot solely rely on established silicon procedures (e.g. according to JEDEC Solid State Technology Association, former Joint Electron Device Engineering Council) but must take into consideration the new possible failure modes and physics together with the corresponding lifetime models and application profiles to determine appropriate qualification tests and durations. It is also essential to derive appropriate screening tests based on intrinsic and extrinsic lifetime models to achieve the needed low field failure rates of 1 fit or less. Passing all those qualification procedures still does not guarantee stable long term behaviour in the application. Long term testing of the devices under real application conditions with no fails is a first necessary step, but only application testing with accelerated conditions (e.g. higher temperatures, bus voltages, peak currents) and testing to failure allows extraction of life time models and hence failure rates in real life [9]. As a joint effort by the major semiconductor companies involved in GaN, a working group for the standardization of GaN qualification under the framework of JEDEC has been recently established to address many of the before mentioned aspects [10].

**Advances in Science and Technology to Meet Challenges**

For further advancing the reliability of GaN devices it is important to further deepen the understanding of defects and their relation to device behaviour and device reliability. This comprises e.g. the understanding of point defects including their electronic structure mainly in the various parts of the AlN/AlGaN/GaN buffer, channel and barrier layers and how those defects are influenced by the growth conditions of the material and the selection of possible advanced substrates. In order to possibly achieve future enhancement mode devices based on MIS gate structures with low leakage currents and a wide range of threshold voltages and gate drive voltages a big step in understanding on how to reduce the interface defect density of gate dielectrics on top of GaN and how to improve channel mobility is needed.

An important mid to long term challenge for GaN technology to enable broader market penetration is approaching cost parity per same $R_{DSON}$ compared to silicon devices like CoolMOS™.

This will be driven on the one hand side by reducing the cost per die area through increasing economy of scale and increased yield with rising volume and the introduction of 200mm wafer diameter for GaN-on-Si during the next few years as well as the step to 300mm within the next decade. On the other hand we will see further die shrinks through better exploration of the material limits e.g. by increased material quality allowing for shorter drift regions through higher electric fields as well as advanced drift region engineering (improved field plates, graded 2DEG density, etc.) allowing for higher carrier densities without compromising reliability.

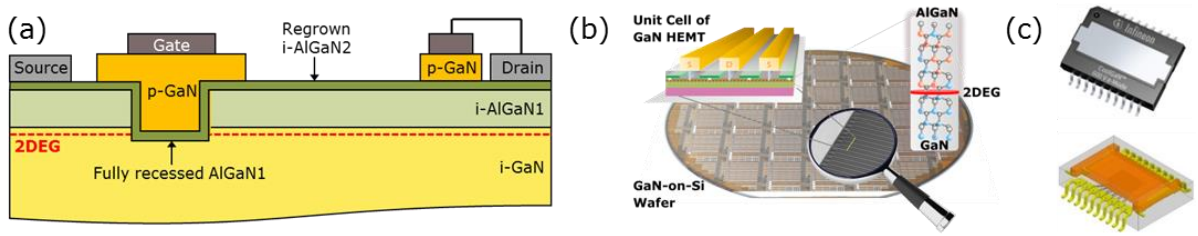


Figure 1. a) 600V E-mode GaN cell concept with through recessed first AlGaN barrier and regrown thin second AlGaN barrier with pGaN enhancement mode gate, b) GaN-on-Si wafer with enlarged unit cell and schematic of AlGaN/GaN hetero junction forming the 2DEG, c) top side cooled SMD package: top view and schematic with wire bonds

**Concluding Remarks**.

After GaN-on-SiC RF power devices have reached a multi hundred million dollar market volume, and after a decade of intense research and development of GaN-on-Si power technology, fully industrial qualified 600V true enhancement mode GaN power devices are finally entering the market. Qualification procedures and screening methods have been established according to the needs of the new material system and taking into consideration typical industrial application profiles targeting field failure rates below 1 fit. The new devices offer customers the degree of freedom to either boost the power conversion efficiency to unprecedented levels of 99% and beyond or to significantly increase the power density of their converters without compromising the efficiency.

**Acknowledgements**.

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# 17 - Potential of GaN Integrated Cascode Transistors

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**Status**

AlGaN/GaN high electron mobility transistors (HEMTs) are poised to replace Si MOSFETs for high frequency power switching applications up to 600 V. Enhancement mode (E-mode) operation with a positive threshold voltage ($V_{TH}$) $\geq$ 3 V is desirable for circuitry protection and safety purposes but GaN HEMTs are naturally depletion mode (D-mode) devices. Cascode devices with low voltage E-mode Si MOSFETs and high voltage D-mode GaN HEMTs offer an excellent solution to the E-mode operation issue using existing gate drivers. In addition, the cascode structure can lead to improved switching speed and reduced switching losses compared to an equivalent discrete transistor [1]. Here, we discuss the challenges faced by cascode devices as well as the potential of integrated cascode structures to achieve high switching frequency.

**Current and Future Challenges**

Despite the promising performance of commercial 600 V hybrid GaN plus Si cascode transistors [2], several issues hinder their switching performance. Firstly, additional package connections in the hybrid cascode lead to increased parasitic inductances which can cause excessive ringing and limit the operating frequency [3]. This presents major challenges to packaging design. In addition, the intrinsic capacitance mismatch between the Si and GaN transistors and the body diode in the Si MOSFET can result in additional switching losses when the Si device is driven into avalanche mode during turn-off [4].

Monolithically integration of E-mode and D-mode GaN devices in the cascode configuration, on the other hand, will mitigate the parasitic inductances and the 'slower' Si device issues in the hybrid GaN plus Si cascode devices. However, $V_{TH}$ of the reported E-mode GaN devices using various techniques such as fluorine (F) treatment on the barrier under the gate [5], GaN MOSFETs [6] and p-AlGaN gate [7] remains low, typically less than 2 V. This presents an issue for gate driving as un-intended turn-on may occur with a voltage ringing effect as a result of CdV/dt coupling from the drain to the gate.

**Advances in Science and Technology to Meet Challenges**

The switching losses in a field effect transistor are partly determined by the current through the resistive loss-generating channel during the charging/discharging processes [8] and hence depend on the speed of charging and discharging the Miller capacitance (Miller effect) at high voltages. The latter depends on the load current-to-gate drive current ratio. On the other hand, the discharging of the charge stored in the output capacitance of the cascode device is not limited by the gate drive current during turn-on as shown in Figure 1(a). During turn-off, the cascode connection utilises the load current to charge the output capacitance and a faster turn-off time can be achieved for the same gate drive capability. The GaN-based integrated cascode transistor is an excellent candidate to exploit these switching advantages without the additional parasitic inductance. In our recent work using F treatment technology to achieve E-mode in the integrated cascode GaN transistor ($V_{TH}$ = +2 V) (Figure 2), we demonstrated a reduction in turn-on and turn-off energy losses of 21 % and 35 %,

respectively in comparison to a discrete GaN E-mode transistor under 200 V hard switching conditions [9]. The immediate challenge is to achieve a reliable E-mode technology with $V_{TH}$ greater than +2 V.

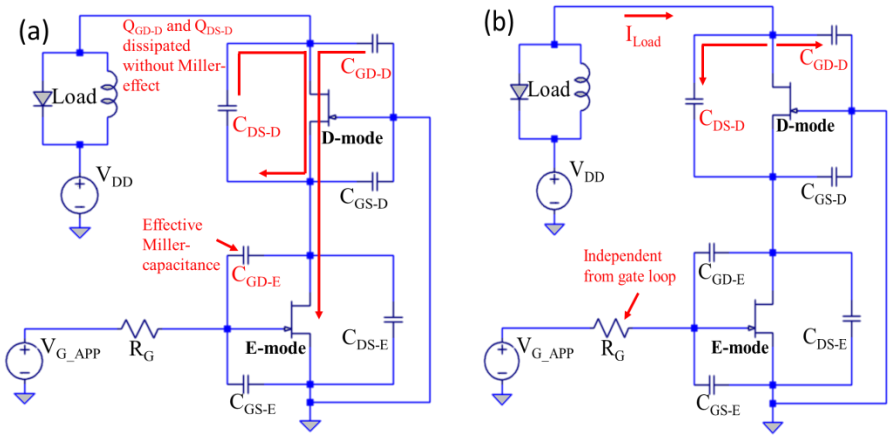


Figure 1. Charging and discharging paths of the output capacitance in the cascode device during (a) turn-on and (b) turn-off processes.

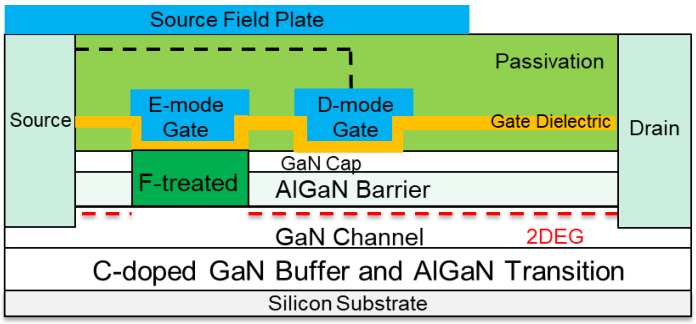


Figure 2: Device structure of GaN integrated cascode transistors.

Matching of intrinsic capacitances between E-mode and D-mode devices in the cascode connection is critical to control the off-state operating voltage of the E-mode device. For hybrid cascodes, adding an external capacitor in parallel with drain-source of E-mode Si MOSFETs has been proposed to provide this matching and prevent the Si device running into avalanche [4], but at the expense of additional package inductances. For GaN integrated cascode transistors, different field plate structures in E-mode and D-mode devices can be employed to achieve capacitance matching. In addition, with the lack of a body diode in the low voltage GaN E-mode device, the integrated cascode devices have the option to trade the off-state operating voltage of the E-mode part for a faster switching speed, without the avalanche loss.

## Concluding Remarks

Monolithically integrated GaN cascode HEMTs open up new opportunities to achieve high efficiency power devices in the MHz range. It is however necessary to overcome both problems with the magnitude of $V_{TH}$ of the E-mode and the mismatch of D-mode and E-mode devices to realise the full potential of integrated GaN cascode HEMTs.

## Acknowledgements

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# 18 - Converter Topologies in GaN

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**Status**

The commercialization of 600V GaN power devices, including the cascode-based FETs and the enhancement mode FETs, has enabled large scale R&D effort in academia and industry [1] to evaluate the impact on converter design and performance. Compared with the best 600V Si super-junction (SJ) MOSFET, the input figure of merit ($R_{on}$·$C_{iss}$) of 600V GaN FET has been improved by about 20 times, the output figure of merit ($R_{on}$·$C_{oss}$) has been improved by about 5 times while the reverse recovery figure of merit ($R_{on}$·$Q_{rr}$) has been improved by more than 40 times [1]. These revolutionary improvements make GaN devices ideal for high efficiency and high density power supply design, especially for applications where the DC link voltage is around 400V. Many converter topologies exist that can take advantages of the improved device performance by directly replacing Si SJ MOSFETs with GaN FETs, operating at the same switching frequency or at an increased frequency. Example topologies include the active-clamped flyback converter (Fig. 1 (a)) for universal AC/DC adapter which can use GaN devices in the primary side [2]; the soft-switched isolated DC/DC converters, such as LLC resonant converter, Phase-Shift-Full-Bridge (PSFB), Dual-Active-Bridge (DAB), etc., which use the GaN devices in the primary side or both sides [3]. Many designs explore the ability to push the switching frequency to much higher value than the Si-based ones, achieving ultra-high efficiency and density. Some topologies are rarely used in the past, limited by the severe reverse recovery issue such as large $Q_{rr}$ and high recovery di/dt in the Si SJ MOSFET. However, by using the GaN devices where the reverse recovery $Q_{rr}$ is pretty much zero due to the absence of any minority carrier injection, some of these topologies become feasible and have demonstrated extraordinary performance. Examples include the 99% efficient totem-pole PFC (Fig. 1 (b)), full-bridge (FB) photovoltaic (PV) inverter (Fig. 1 (c)) and the 98.8% efficient hard-switching isolated full-bridge converter [4-7]. In addition to the circuits, improved modulations also make the same topologies perform even better. The continuous conduction mode (CCM) totem-pole power factor corrector(PFC) and FB PV inverter work with hard switching and constant frequency, typically only in the range of 50~100kHz. However, the triangular current mode (TCM) totem-pole PFC and FB PV inverter can work with soft switching and variable frequency in the range of 100 kHz~3MHz [4, 5, 7]. With these GaN-based topologies, the efficiency and the power density are significantly improved compared with the Si-based solutions.

**Current and Future Challenges**

The main challenges for the GaN based converter topologies are:

1. The optimization of the switching frequency: The switching frequency determines the frequency related loss and the size of the passive components. The optimization of the switching frequency is an important research topic.

2. Selection between hard switching and soft switching: Constant frequency hard switching modulation has low control complexity and high reliability, while the size of the passive components is large. Variable frequency soft switching techniques can reduce the size of the passive components due to the high frequency. However, the control complexity is significantly increased due to the variable frequency operation. The selection between hard switching and soft switching is a challenge.

3. The reduction of the differential mode (DM) filter size for soft-switched topologies: Soft-switched topologies, such as the TCM totem-pole PFC and the TCM inverter, have large input current ripples. It is still challenging to dramatically reduce the DM filter size even the frequency is high.
4. New converter topologies in GaN: To take full advantage of the GaN device, developing new topologies and new power delivery architecture is a needed new challenge

**Advances in Science and Technology to Meet Challenges**

The progresses in addressing and investigating the previously mentioned challenges are:
1. The optimization of the switching frequency: The optimization of the switching frequency depends on the requirements of the application. For applications focusing on the high efficiency, lower frequency is preferred. For the applications requiring high density, such as the Google Little Box challenge, higher frequency is preferred.
2. Selection between hard switching and soft switching: Due to the elimination of the turn on loss, the zero-voltage-switching (ZVS) converters can realize high switching frequency. Thus, the size of all the passive components, especially the EMI filters, can be reduced. In addition, the slower dv/dt of the ZVS converters also reduce the EMI noises. The soft-switched converters have demonstrated ultra-high density, over 145W/inch$^3$, on the totem-pole PFC and FB PV inverter [4, 5, 7].
3. The reduction of the DM filter size for soft-switched topologies: Multiphase interleaved soft-switched topologies (Fig. 1 (d)) can solve this challenge [8]. The interleaving technologies significantly reduce the current ripples. The DM filter size is optimized, too.
4. New converter topologies in GaN: The upcoming GaN-based AC switch could enable a number of new high-performance topologies. The resonant converter with GaN AC switch (Fig. 1 (e)) not only realizes high efficiency, but also achieves the wide input and wide output voltage conversion [9]. A new single stage solution, the isolated AC/DC DAB converter with GaN AC switches (Fig. 1 (f)) on the primary side, can be used for on-board charger and battery system with significantly improving the system efficiency [10].

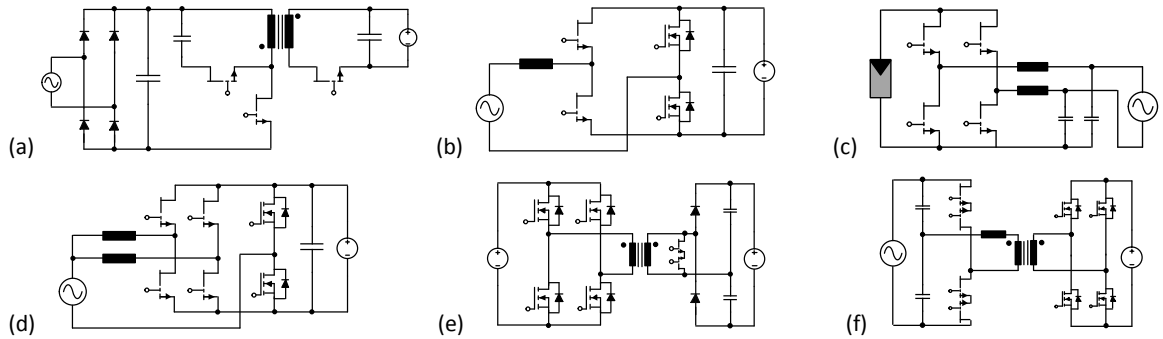


**Fig. 1.** Topologies discussed previously with GaN FETs: (a) active clamped flyback; (b) totem-pole PFC; (c) FB PV inverter; (d) two-phase interleaved totem-pole PFC; (e) resonant converter with GaN-AC switch at the secondary side; (f) AC/DC DAB with GaN AC switches

| | Frequency | Efficiency | Power density |
|---|---|---|---|
| 65W active-clamp Flyback Charger [2] | 1MHz | 93.0% (full load) | 25W/inch$^3$ |
| 2.4kW FB isolated DC/DC [6] | 50kHz | 98.6% (full load) | 116W/inch$^3$ |
| 1kW TCM two-phase totem-pole PFC [4] | 4MHz (max) | 98.7% (full load) | 220W/inch$^3$ (no bulky capacitors) |
| 2kW multiphase TCM FB PV inverter [7] | 35~240kHz | 95.4% (CEC) | 150W/inch$^3$ |

Table 1. Benchmark of the state of the art GaN-based converters

**Concluding Remarks**

The GaN-based converters have demonstrated extraordinary performance. As shown in Table 1, the power density and the efficiency have been improved significantly based on these benchmark GaN

converters. With the innovation and the optimization of the converter topologies in GaN, the density and efficiency will be further improved. Even though the cost of the devices is increased, the high density and efficiency will reduce the system cost in the future.

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# 19 – Fast switching with GaN and dynamic on-resistance from application view-point

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**Status**

GaN semiconductors have gained popularity in GHz applications, while power electronic applications are still in the early stages of development. The focus of this section is the application of GaN devices for power electronics with device breakdown voltages from 400V up to 900V. Applications of GaN transistors include uni- and bidirectional DC/DC and AC/DC converters, inverters for high-speed motor drives as well as inductive heating and wireless power transmission (Fig. 1). High system efficiencies and power densities are the main requirements for these applications. This is enabled by low conduction and low switching losses from a semiconductor point of view. GaN transistors allow both aspects. Low conduction losses are achieved by GaN transistors with low area-related on-resistance compared to Silicon (Si) and Silicon Carbide (SiC) counterparts. Low switching losses are achieved by fast switching between the on- and off state. GaN transistors show a purely capacitive behaviour due to their unipolar device characteristic, while Si- and SiC-MOSFETs lack from reverse recovery charge due to intrinsic bipolar body diodes [1]. Regarding the switching speed of the drain-source-voltage, 5-20 V/ns is considered as "fast" for Si devices. Slew rates are typically limited to the range of 1-16 V/ns in motor drive applications [2]. In contrast, optimized SiC and GaN circuits allow up to 200 V/ns and 500 V/ns, respectively [3,4]. The possibility of ultra-fast switching exceeds the boundary conditions of most applications. However, operating two 600V transistors in half-bridge configuration for e.g. hard-switching bidirectional DC/DC converters, Si-MOSFETs are not suitable due to their bipolar body diode. SiC-MOSFETs with orders of magnitude lower reverse recovery charge are suitable, but higher system efficiency can be achieved with unipolar GaN-transistors.

**Current and Future Challenges**

The main challenges for GaN transistors in power electronic applications are:

1. Normally-off characteristic: System developers require normally-off devices because of safety reasons, while the realization of normally-off device characteristics is still a main research topic (section 8).
2. Dynamic on-resistance: Some GaN transistors show dynamic on-resistance. After turn-on, their on-resistance $r_{ds,on}$ is higher than the static value $R_{ds,on,typ}$ and decays over time until it reaches the static value $R_{ds,on,typ}$. The main reason is a physical phenomenon called "trapping" due to high electric-field strengths in the off-state, when the blocking voltage is applied (drain-source-voltage is e.g. 400V) [5,6]. Fig. 2 shows a comparison of three devices from different manufacturers. GaN #1 shows the highest dynamic on-resistance with a ratio of $r_{ds,on}$ ($t_1$)/ $R_{ds,on,typ}$ = 4.3 while it decreases to 2.5 after 300 µs. For example, the turn on time of a DC/DC converter operating at a moderate switching frequency of 100 kHz and a duty cycle of 50 % is only 5 µs. This results in an effective on-resistance of 4.2·$R_{ds,on,typ}$ for the system design and therefore in higher losses and lower efficiency. The influence of this issue becomes even worse when the switching frequency is increased.

3. Reverse conduction capability: In half-bridge configuration, reverse conduction capability is required for negative drain currents. Though there is no intrinsic body-diode in GaN transistors, current can flow from source to drain. However, the source-drain-voltage drop $v_{sd}$ increases with decreasing gate-source-voltage $v_{gs}$. This is valid for all commercially GaN transistors known to the authors. For example, for some GaN transistors, the forward voltage drop $v_{sd}$ is 8 V or higher, when the gate is kept in the off state with $v_{gs}$ = -5 V.
4. Parasitics, packaging, controllability and EMI: In general, the influence of parasitic inductances and capacitances is the same as with Si and SiC circuits. This situation worsens for GaN transistors due to tighter gate voltage margins compared to Si and SiC devices which can lead to device destruction and phase leg short circuits. In general, fast switching semiconductors enable higher power densities, but require additional filters for electromagnetic interference (EMI), also.
5. Reliability issues and countermeasures are discussed in section 8.

**Advances in Science and Technology to Meet Challenges**

The progresses in addressing and investigating the challenges from the preceding subsection are:

1. Normally-off characteristic: This challenge must be solved at the level of the device technology. Alternatively, a cascode circuit with normally-off behaviour can be realized by using a normally-on high-voltage GaN transistor and a normally-off low-voltage Si transistor. However, recent studies have shown that the switching speed of cascodes is barely adjustable without additional components inside the cascode [7]. The necessity of an additional Si transistor for the cascode is another disadvantage of the cascode compared to normally-off GaN transistors. All commercial GaN transistors at the time of this study show normally-off behaviour by intrinsic normally-off characteristic or cascode configuration.
2. Dynamic on-resistance: As can be seen in Fig. 2, the GaN transistor #3 shows no dynamic on-resistance for the full time scale. The manufacturer applies an additional p-GaN-layer to provide the injection of holes from the drain and dynamic on-resistance can be prevented successfully [8]. However, other manufacturers still face the challenge of the dynamic on-resistance which is also indicated by significantly increased scientific activities regarding this topic.
3. Reverse conduction capability: The high forward voltage drop in reverse conduction mode of GaN transistors can be avoided by using synchronous rectification. This means to turn the GaN transistor on shortly after the current has commutated to the transistor in reverse direction. In contrast to a diode, the transistor has to be turned off before the complementary transistor of the half-bridge turns on. Otherwise, phase leg short circuits may occur which lead to immediate destruction of both switches. In this case, special protection circuits are necessary. Additionally, the adaption of the dead-time between the half-bridge switching actions helps to increase the efficiency even more.
4. Parasitics, packaging, controllability and EMI: Integration of GaN transistors and gate drivers within one package will minimize the effects of parasitic circuit elements. The next step is to integrate GaN transistors and drivers within one chip which has already been demonstrated. To gain the most advantage for power electronic systems, the integration of GaN transistor, gate drivers, auxiliary circuits and DC link filters within one device will allow minimum parasitic

circuit inductance and high switching speeds. The EMI can also be improved by the enclosure on low footprint as well as novel active filters.

**Concluding Remarks**

GaN transistors have evolved dramatically in the last ten years and enable power electronic systems with highest efficiencies due to their unipolar device characteristic and low area-specific on-resistance (Fig. 2). The issues discussed in this section will diminish with further research similar to the advances with Si and SiC devices in the last 70 and 20 years, respectively.

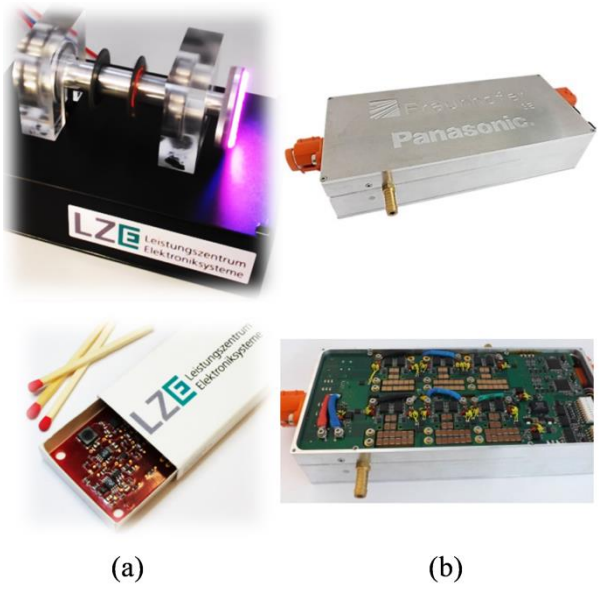


**Figure 1**. (a) Demonstrator of 20 W inductive power transmission for high-speed rotating applications (top) and corresponding matchbox-sized GaN power electronics (bottom) [9]. (b) Demonstrator of 6 kW on-board charger for electric vehicles with 3 kW/l power density (top) and power electronics setup (bottom) [10].

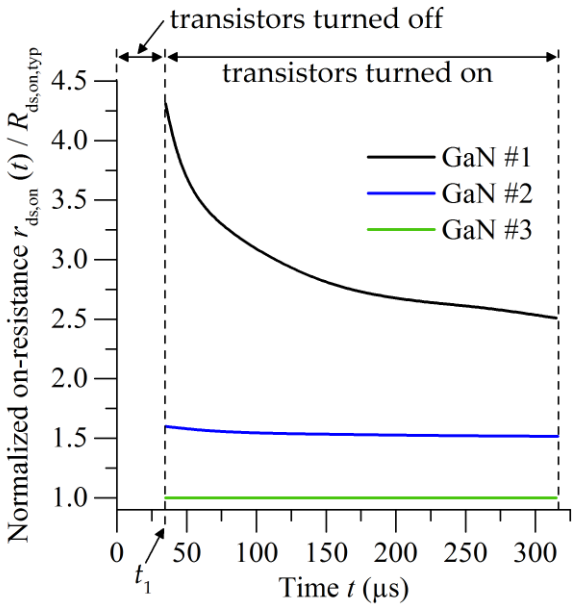


**Figure 2.** Measurement of the on-resistance of three GaN transistors from different manufacturers. The drain-source voltage in the off-state is kept at 50 % of the drain-source breakdown voltage for 20 seconds.

**Acknowledgements**

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# The 2018 GaN power electronics roadmap

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## Abstract

GaN is a compound semiconductor that has a tremendous potential to facilitate economic growth in a semiconductor industry that is silicon-based and currently faced with diminishing returns of performance versus cost of investment. At a material level, its high electric field strength and electron mobility have already shown tremendous potential for high frequency communications and photonic applications. Advances in growth on commercially viable large area substrates are now at the point where power conversion applications of GaN are at the cusp of commercialisation. Nevertheless, there are still many more opportunities for enhancement to be explored. This roadmap comes at a crucial time to consolidate recent developments and predict future requirements of materials, growth, device architectures and reliability that underpin the manufacturing challenges in real-life applications of GaN in power circuit applications.

## Introduction

Silicon-based Insulated Gate Bipolar Transistors (IGBTs) and Superjunction MOSFETs are fundamental components of present day power electronic systems for the conversion, control and conditioning of electrical energy, from generation to the point of load. If silicon devices were to be replaced by a more efficient semiconductor such as GaN, compact converters with ultra-high density can be designed only because the breakdown strength and electron mobility in GaN are respectively 10x and 2-5x higher. These basic material properties translate into smaller devices leading to higher frequency of operation, lower switching losses, and reduction in the component count and size of passives. This was demonstrated by over 100 hours testing by NREL of 2kW GaN inverters designed by the Red Electrical Devils, winners of the Google Little Box Challenge in 2015. Compact modules translate directly into lower weight, volume and cost. Coupled with increasing concern and government commitment to global warming, there are now strong commercial and legal pressures to accelerate adoption of these advantages into production systems.

Applications are now emerging that have no other practical solution than GaN. Take for example the automotive industry: GaN is the semiconductor of choice for power converters throughout vehicle electronics apart from the final drive inverter. Even here, there is now a very strong push to create production devices capable of switching as much as 100 Amps at 900 Volts. The advent of mass adoption of electric vehicles will in turn accelerate two other major markets that depend on highly efficient high-density power converters. Charging electric cars will require intelligent switching in the local power distribution grid. Simultaneously, IT infrastructure to support autonomous driving will create another massive parallel requirement for efficient power conversion.

GaN has evolved to the point where the cost of the transistor itself is no longer considered as the key driver in system cost. The novelsolutions that the technology facilitates, provides savings in both manufacturing and running costs. Focus will come to bear on manufacturing parts in volume that will finally demonstrate the predicted price learning curves and focus attention on those research avenues that provide the fastest route to manufacturing maturity.

There has been considerable diversification of approaches over the last decade into addressing some of the problems with GaN. The roadmap presents a snapshot, highlighting consolidation of this research into substrates, gate architectures, device and circuit topologies and their reliability. We expect growth and reliability to be greatly accelerated by the first phase of volume production, but this is just the start. A parallel critical path in the technology roadmap highlights that the full material benefits of GaN cannot be achieved via existing product design approaches using slower silicon gate drivers. Novel circuit approaches, better companion passive devices and packaging will be the new frontier for research to addresses the thermal, electrical and electromagnetic design of a converter system. Particularly exciting is the potential and challenge of integration, on a chip where transistors are capable of even out-switching the delays of signal paths.

We hope you enjoy this peek into an enticing perhaps all-GaN future!

# 1 - Manufacturing Challenges of GaN-on-Si HEMTs in a 200 mm CMOS fab

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**Status**

GaN is anticipated to be the next generation power semiconductor. With a higher breakdown strength, faster switching speed, higher thermal conductivity and lower on-resistance ($R_{on}$), power devices based on this wide-bandgap semiconductor material can significantly outperform the traditional Si-based power chips. As such, GaN-based power devices will play a key role in the power conversion market within battery chargers, smartphones, computers, servers, automotive, lighting systems and photovoltaics.

In absence of viable low-cost GaN bulk substrates, GaN is grown on a variety of substrates, the most popular being sapphire, silicon carbide (SiC) and silicon (Si). Si substrates have become attractive for GaN growth because of their larger wafer diameter (200 mm and higher) though the large mismatch in lattice constant and coefficient of thermal expansion (CTE) imposes epitaxy challenges, especially for larger Si substrate sizes. Moreover, GaN devices are naturally normally-on or depletion mode (d-mode) devices whereas, to replace commercially available Si power devices, the GaN devices should be normally-off or enhancement-mode (e-mode) devices. Furthermore, GaN devices should be fabricated by a low-cost, reproducible and reliable production process. While e-mode operation can be readily achieved by adding a p-doped GaN layer under the gate, hereby lifting the conduction band at equilibrium and resulting in electron depletion, the ability to manufacture GaN-on-Si power devices in existing 200 mm Si production facilities offers further cost competitiveness to the Si power technology.

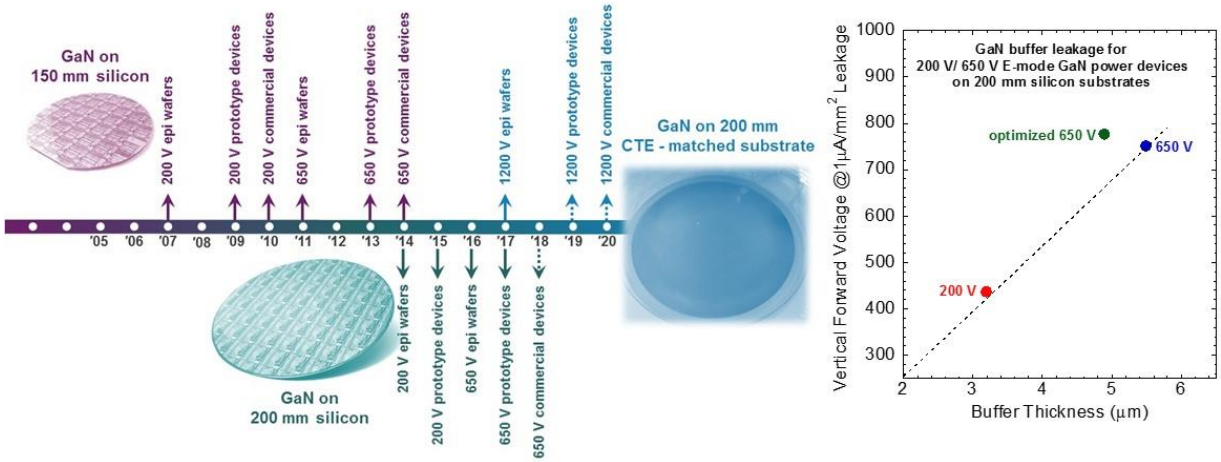


**Figure 1.** Left: timeline for 200 V, 650 V and 1200 V GaN-on-Si epi wafers, prototype and commercial enhancement-mode power devices. Right: buffer leakage at 25˚C of imec's 200 V (red) and 650 V (blue and green) GaN-on-Si epi wafers after full processing in the 200 mm CMOS fab.

Initially, the development of GaN-based technology focused on high voltage (200 V and 650 V) power-switching applications. First commercial 200 V e-mode GaN devices, fabricated on 150 mm Si substrates, were released in 2010 and first 650 V commercial devices followed in 2014 (Figure 1, left). After first developing the technology on 100 mm [1, 2], and later 150 mm wafer sizes using Au-free metallization schemes [3], imec has been pioneering 200 mm GaN-on-Si technology with first GaN 200

V epitaxy [4] and devices in 2014 [5-9]. The imec 200 mm GaN-on-Si e-mode transistor and diode platform was recently extended and qualified for 650 V applications. Today, the focus is on the technology development for higher level of integration and for 1200 V applications using 200 mm CTE-matched polycrystalline AlN substrates.

**Current and Future Challenges**

Because of the much higher CTE of GaN compared to Si, the GaN in-film stress during epitaxial growth needs to be tuned compressive to compensate for the tensile stress during cool down. The use of 1.15 mm-thick 200 mm Si substrates is beneficial to reduce wafer warp during growth and hence avoiding wafer cracking. Without significant hardware changes and lowering the robot speed of some handling systems, the thicker and heavier GaN-on-Si wafers can be processed in the standard imec CMOS fab. The warp specification of 50 μm is sufficiently low to avoid chucking issues on electrostatic chucks. Prior to the fab introduction, the 200 mm GaN-on-Si wafers are tested for mechanical robustness, hereby reducing the wafer breakage during processing to less than 1%. After epitaxy, Ga and Al contamination on the wafer backside is unavoidable. Since Ga is a p-type dopant for Si, one of the major concerns of processing GaN wafers in a CMOS fab is Ga cross-contamination. The Ga and Al backside contamination after epitaxy is effectively removed by an in-house developed $HF/H_2O_2$-based cleaning procedure, hereby reducing the contamination level of the wafer backside and bevel to below $10^{11}$ at/cm$^2$. Moreover, imec's e-mode pGaN process flow contains (Al)GaN dry etch steps. A first one to dry etch the pGaN layer selectively to the AlGaN barrier layer, and a second to recess the AlGaN barrier in the ohmic contact areas. Since conventional F-containing cleaning recipes of the dry etch tools can form non-volatile $GaF_x$ species (i.e. $GaF_x$ is not volatile below 800°C), a $Cl_2$-based clean that forms volatile $GaCl_3$ at ~200°C is used. This cleaning procedure effectively and reproducibly maintains the Ga contamination level in the dry etch tools well below the maximum allowed level.

Finally, since Au is a rapidly diffusing contaminant in Si that deteriorates the minority carrier lifetime, the GaN metallization schemes need to be Au-free. Because of the high bandgap and the absence of explicit doping of the epilayers, especially the development of Au-free ohmic contacts is challenging. By using a Si/Ti/Al/Ti/TiN ohmic metal scheme and decreasing the alloy temperature to 565˚C, the ohmic contact resistance could be lowered to 0.3 Ω·mm with excellent reproducibility and uniformity.

**Advances in Science and Technology to Meet Challenges**

Because the breakdown field of the Si substrate is ten times lower compared to GaN, the breakdown voltage of the power devices is dictated by the GaN buffer thickness. In Figure 1 (right) the vertical buffer breakdown voltage (at 1 μA/mm$^2$ leakage) is plotted versus the buffer thickness. Straightforward extension of the 3.2 μm-thick 200 V buffer (red) to 5.5 μm for 650 V applications (blue) was resulting in low wafer yield: the yield related to wafer breakage in the mechanical screening test was reduced from 90% for 200 V to 77% for 650 V. This issue was tackled by implementing Si substrates with high boron doping (0.01 Ω·cm resistivity) hereby increasing the mechanical wafer strength, and by developing a new buffer concept with reduced thickness (4.9 μm, green) that resulted in an equally high buffer breakdown voltage while maintaining the low buffer dispersion, and increasing the wafer yield for 200 V applications to 99% and to 97% for 650 V applications.

By optimization of the cleaning and dielectric deposition conditions, together with the field plate design, state-of-the-art 650 V 36 mm gatewidth power devices with 2.1 V threshold voltage (at maximum transconductance), 13 Ω·mm $R_{on}$ and 8 A output current (Figure 2a and b) were obtained

on 200 mm wafer size and processed in a standard CMOS wafer fab. Moreover, the devices exhibit dynamic $R_{on}$ dispersion below 20% (10 μs on, 90 μs off) up to 650 V over the full temperature range from 25°C to 150°C (Figure 2c).

For 1200 V power applications, imec is working on using polycrystalline AlN (poly-AlN) substrates that have a better CTE-match to GaN. In this approach, a thin crystalline Si layer is transferred to a 200 mm poly-AlN substrate. This new technology is promising to go beyond the current technology limitations, because it is possible to grow thicker, higher quality GaN buffers on 200 mm substrates with a standard thickness of 725 μm. Imec has already demonstrated the CMOS-compatibility of these substrates in terms of contamination and wafer handling [10]. Furthermore, first high quality transistors have been processed illustrating the high promise of this new approach.

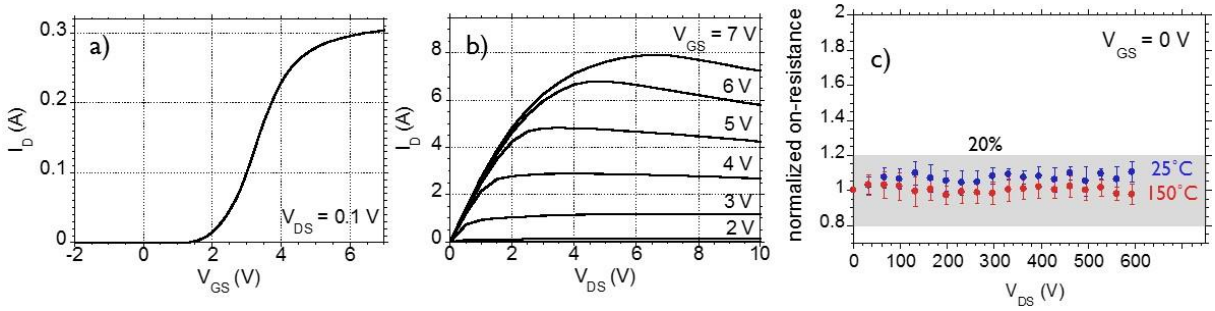


**Figure 2.** (a) Transfer and (b) output characteristics of a typical 36 mm gate width 650 V e-mode power device, and (c) the dynamic $R_{on}$ device dispersion. The devices were fabricated in imec's 200 mm CMOS fab.

## Concluding Remarks

GaN technology offers faster switching power devices with higher breakdown voltage and lower on-resistance than Si, making it an ideal material for advanced power electronic components. For cost competitiveness, GaN power devices are preferably fabricated on large diameter Si substrates in existing Si CMOS fabs. Due to the large mismatch in lattice constant and thermal expansion coefficient, the epitaxy of GaN on large diameter Si substrates is very challenging. Imec has demonstrated for the first time that is possible to manufacture 200 V and 650 V GaN-on-Si e-mode devices in a 200 mm CMOS fab. For 1200 V applications, it is proposed to transfer the technology to 200 mm Si-on-poly-AlN substrates, which is CTE-matched with GaN. This substrate technology allows for thicker GaN buffers, which is needed to reach 1200 V and beyond, and was also assessed to be CMOS-compatible in terms of contamination and tool handling.

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# 2 – Epitaxial Lift-Off of GaN and Related Materials for Power Device Applications

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**Status**

GaN and other III-N compound semiconductors have had an enormous impact on optoelectronics—with the widespread adoption of LEDs, lasers, and solar-blind photodetectors—as well as RF electronics for both consumer wireless infrastructure and military communications and sensing. The continuing advance of III-N electronics promises to bring this revolution also into the power electronics space. With power device concepts based both on extensions of conventional lateral FET designs, as well as concepts based on vertical transistor designs, GaN and related materials promise to dramatically enhance the performance, efficiency, and ubiquity of sophisticated power management and control functions. Advances in growth and substrate technologies for achieving high-quality material, along with improved device designs, promise to enable continued increases in device performance. In addition, novel processing techniques are also promising to provide significant performance, cost, and integration improvements. Among these processing-related advances, techniques that enable epitaxial lift-off and substrate transfer are especially attractive. Epitaxial lift-off has been demonstrated for optoelectronic applications (see e.g. [1], [2]), and offers the potential for improved light extraction, smaller device form factor, and ultimately more flexible displays as well as sensors for emerging applications such as wearables. In the power application space, epitaxial lift-off can enable substantial increases in thermal performance (through improved heat removal), electrical performance (through lower resistive losses and higher breakdown voltages), economics (through more efficient materials utilization, die size reduction, and substrate reclaim and reuse), and enhanced integrability with other electronics technologies. A range of epitaxial lift-off technologies for GaN and related materials have been demonstrated, including selective wet etching of ZnO layers [2], dry etching of epitaxial $Nb_2N$ layers by $XeF_2$ [3], mechanical exfoliation and separation using graphene or BN layers [4, 5], and band gap selective photoelectrochemical etching based on wet-chemical etching of lower-band gap materials such as InGaN [1, 6, 7, 8]. In addition to the mechanism by which the lift-off occurs, epitaxial lift-off processes may be distinguished by whether they lift off a single device (Fig. 1(b)) or small circuit (e.g., [1], [3]), or seek to lift off a larger film (Fig. 1(a)) either for subsequent processing into devices (e.g., [2], [4], [5]) or after fabrication of the devices is largely complete (e.g. [7, 8]).

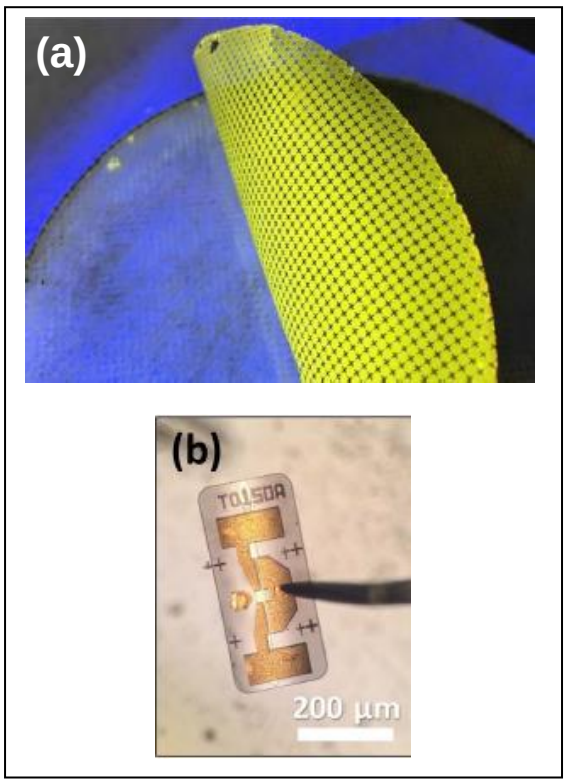


**Figure 1.** (a) Large-area (100 mm wafer) epitaxial lift-off of GaN-based epitaxial device layers achieved using band-gap selective photoelectrochemical wet etching of an InGaN [7]; (b) single-die release of a GaN-based device using dry etching of $Nb_2N$ with $XeF_2$ [3].

**Current and Future Challenges**

Advances in power electronics are poised to radically alter the design and implementation of electronic products and systems; ultimately, sophisticated power electronics and circuit topologies for enhanced efficiency and power-control capability could become ubiquitous if the key technological and economic challenges can be solved. Realization of this vision is currently constrained by cost, device performance, and integration challenges—all of which can be addressed by epitaxial lift-off. Due to the wide diversity of potential applications there is unlikely to be a single optimal solution; instead, we can expect different approaches to benefit different application segments. For example, for modest voltage and current requirements for which lateral devices (e.g. MISHEMTs) provide sufficient performance and economic benefit, use of conventional lattice-mismatched substrates such as SiC, sapphire, or Si is appropriate; epitaxial lift-off can then be used to accomplish substrate transfer for improved thermal or breakdown performance (see e.g. [9]), as well as the potential for reusing high-cost substrates (e.g. SiC) [3]. For applications where high currents and material-limited breakdown voltages are required, as well as applications where economics dictates a high areal current density, vertical device structures offer inherent advantages. However, these devices also place additional demands on material quality; while high dislocation densities are often tolerable in optoelectronic and lateral electronic nitride devices, these defects significantly compromise the performance of vertical devices. This can be addressed by homoepitaxial devices on bulk GaN substrates, but this in turn places more stringent demands on the epitaxial lift-off approach to avoid the generation of dislocations. The economic benefits of epitaxial lift-off from bulk GaN substrates are substantial, given their high cost and small diameter. In addition to substrate reuse, thermo-electric modelling indicates that direct bonding of lifted-off vertical FETs to a heatsink could enable die size reduction by more than 50% compared to devices on bulk GaN substrates [8]. Of the current techniques, only band gap selective photoelectrochemical etching with pseudomorphic InGaN release

layers has been demonstrated to maintain fully coherent single-crystal material from the bulk substrate through the device epitaxial layers, and so may provide a unique solution to achieving epitaxial lift-off of vertical devices on bulk GaN substrates. Reuse of bulk GaN substrates after lift-off has recently been demonstrated with lift-off of GaN pn junctions (Fig. 2) demonstrating a pathway to improved economics; future efforts will be needed to fully realize the thermal and integration benefits.

**Advances in Science and Technology to Meet Challenges**

To address the challenges and fully realize the benefits of epitaxial lift-off as an enabling technology for high-performance, low-cost, ubiquitous power electronics, significant technological challenges must be overcome. For material-quality sensitive applications such as vertical devices, additional development of lattice-matched or pseudomorphic release layers is an important future direction. Current demonstrations have been based on the use of InGaN release layers [1, 6, 7, 8]; while this approach has been successfully demonstrated for both single-die release and lift-off of large areas (> 100 mm wafer), the lateral etch rate is modest and the surface morphology of the N-face GaN is not yet easily controlled due to limited etch rate selectivity. Additionally, the use of pseudomorphic release layers such as InGaN have been reported to influence the mechanical behaviour of released structures [10]. Development of strain-control strategies or deposition of alternative release layer materials with basal plane lattices commensurate with the GaN devices are areas for future development and exploration. Another area that is largely unexplored to date is that of novel packaging and bonding strategies to leverage the unique features of devices fabricated using epitaxial lift-off. The thermal performance of ultra-thin devices has been projected [8], but experimental validation and–in particular—optimization for the unique characteristics of ultra-thin devices is an area for additional development. Heterogeneous integration of lifted-off devices with conventional electronics, and packaging of lifted-off devices for emerging applications such as flexible or ultra-thin form factors is another area where substantial additional innovation is needed. Finally, the reliability of lifted-off devices is an important topic, but one that has not yet been addressed due to the nascence of the technology.

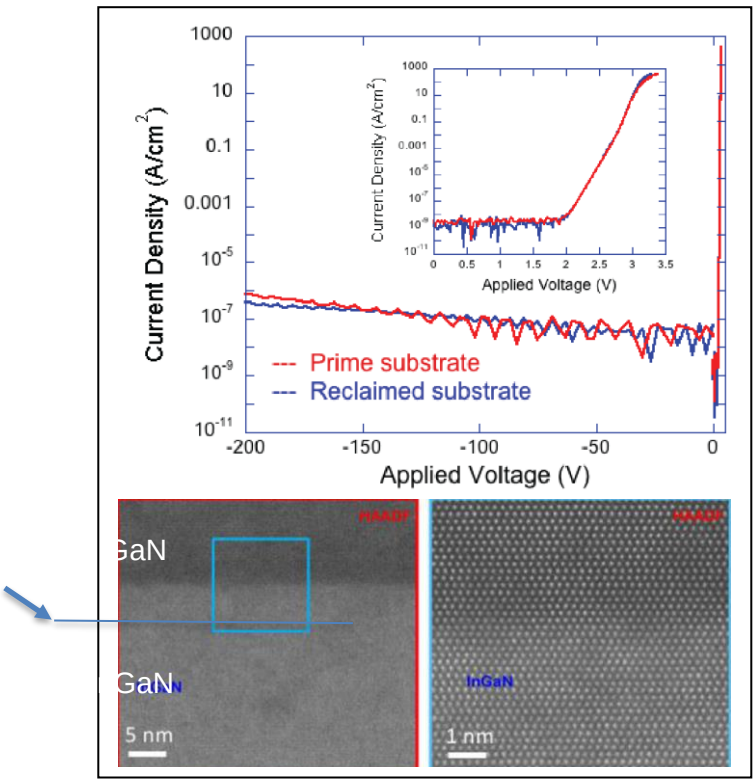


Figure 2. (a) Measured current-voltage characteristics of typical GaN vertical PN junction diodes on prime bulk GaN substrate and on a reclaimed substrate (i.e., after growth, lift-off, repolish, and a second device growth and fabrication sequence, validating that device performance on epi-ready prime and reclaimed/reused substrates is nearly indistinguishable. (b) TEM image showing pseudomorphic InGaN release layer growth [7].

## Concluding Remarks

Epitaxial lift-off is an emerging technology that is poised to be of significant benefit to the developing field of III-N based devices, and in particular to high-performance, cost-effective power electronics. The improvements in electrical and thermal performance, economic benefits derived from reduced die size and bulk GaN or SiC substrate reuse, and potential for enhanced heterogeneous integration with other electronics and packaging technologies makes epitaxial lift-off appear promising for advancing power electronics across a broad range of applications.

## Acknowledgements

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# 3 – GaN-on-Si 200 mm for power devices

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**Status**

The main objective in the LETI power electronic roadmap is the miniaturization of power converters to increase the energy efficiency of the systems while reducing the cost. It is also important to improve reliability and ensure operation at higher temperatures (300 °C), with the markets of automotive (EV and HEV) and motor drives for industrial tools being targeted. To achieve these objectives for power convertors from a few Watts to several hundred kW, it is essential to increase their operating frequency [1]. GaN-on-Si power devices are capable of responding to these requirements because GaN allows high frequency switching (several MHz) and a higher power density than silicon (10 times greater), although these solutions must be implemented at the system level in order to fully benefit from the materials properties. Furthermore GaN on 200 mm Si enables CMOS compatible technology leading to lower cost and improved robustness of the processes.

LETI has chosen to develop MOS-HEMT GaN architecture, fabricating "Normally-Off" devices which give functionality similar to a classic silicon based MOS. To take full advantage of these devices, a route towards monolithic solutions for low and mid power applications and a route towards system in package is promoted at LETI, fig. 1, with 5 main axes of work: epitaxy, devices, passives, co-integration, and system architectures. Here we will focus on the device roadmap.

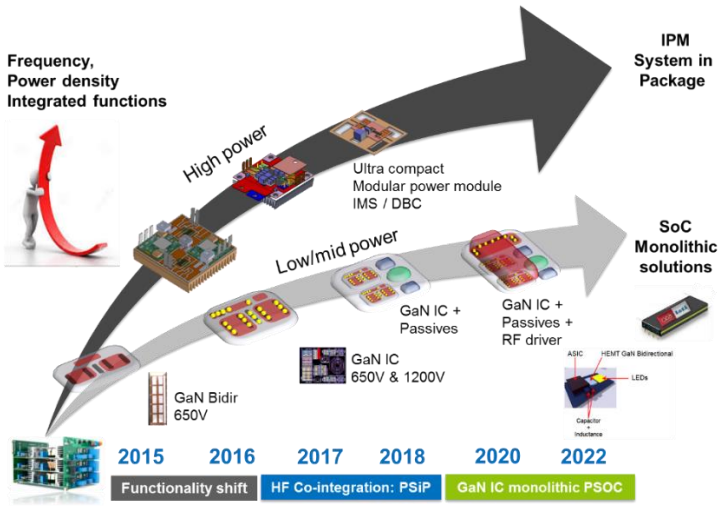


**Figure 1.** Power systems roadmap at LETI. An SOC (system on chip) route towards monolithic solutions is important for miniaturization for low and mid power solutions. For higher voltages, an ultra-compact power module is preferred [2]

**Current and Future Challenges**

Adoption of GaN in the industry requires high performance, high reliability devices produced at low cost. For automotive applications, GaN transistors of 1200 V - 50 A and 650 V - 200 A are targeted. Current requirements are a $R_{onS}$ below 1 mohm/cm², Fig. 2, with an $R_{dyn}$ of no more than 10 % of the $R_{onS}$, meaning low losses [4]. The epitaxy is expected to improve in several ways: Firstly, a constant

improvement in the buffer layers and active layers to decrease the dislocation density, even though this has not been proven to be essential for high quality HEMT performance, and a reduction in point defects which cause trapping; Secondly, a vertical leakage current lower than 1µA/mm$^2$ at 150°C and thirdly improvements and optimisations in the design of the epi stack, such as integration of back barriers to improve confinement of the free carriers in the potential well. Of course, all this has to be implemented while maintaining a wafer bow < 50 µm for a silicon wafer thickness of 1 mm maximum to enable the process in standard 200 mm tools [3].

The most developed structure to make normally-off GaN HEMTs is pGaN gate architecture. P-type GaN may have potential work function of up to 7.5 eV which makes pGaN an outstanding gate metal in addition to the depolarization effect for depleting the channel beneath the gate. However this design suffers from a compromise between the threshold voltage and the sheet resistance in the channel and so high positive threshold voltages are difficult to achieve. This is why at LETI we are developing an alternative strategy, the MOS-HEMT. This architecture is a hybrid monolithic device which essentially puts a MOS channel and a HEMT drift layer in series. At the heart of this technology is the MOS gate, which needs to be reliable and robust; a challenge that Si and SiC have already faced in the past.

**Advances in Science and Technology to Meet these Challenges**

These advances required to meet the challenges listed above can be described in five bullet points:

Simulation: to design complex architectures, capture process influence and describe device behaviour, simulations such as TCAD are of major importance. Currently, significant efforts are needed to ensure simulators properly recreate the physics of III-N materials and devices.

Device Characterisation**:** the JEDEC standards are not sufficient to fully qualify GaN-based power devices due to restrictive criteria. Dynamic properties and aging effects, which show common patterns with dielectric aging, are key topics to be understood in order to bring GaN-on-Si products to industrial maturity in mass markets.

Device technology: as discussed above, constant improvements are required in the epitaxy, with in particular improved defect characterization and analysis of their impact on device performance. The understanding of the gate oxide trap passivation will also be a significant scientific and technological challenge. The whole technology has to be CMOS compatible, which brings an additional constraint to GaN power device design, and the potential of GaN on 300 mm Si has to be investigated.

Thermal dissipation: The reduction in size of power devices when using GaN raises the challenge of thermal dissipation. In order to benefit from the full potential of GaN technology, the power density will need to be increased, and so process and packaging will need to be optimised to improve thermal dissipation.

Switching frequency**:** To allow high frequency switching, co-integration is key. Transistors, flyback diodes, rectifiers or drivers are examples of active devices that can be monolithically integrated to reduce parasitic elements and reach high performance converters.

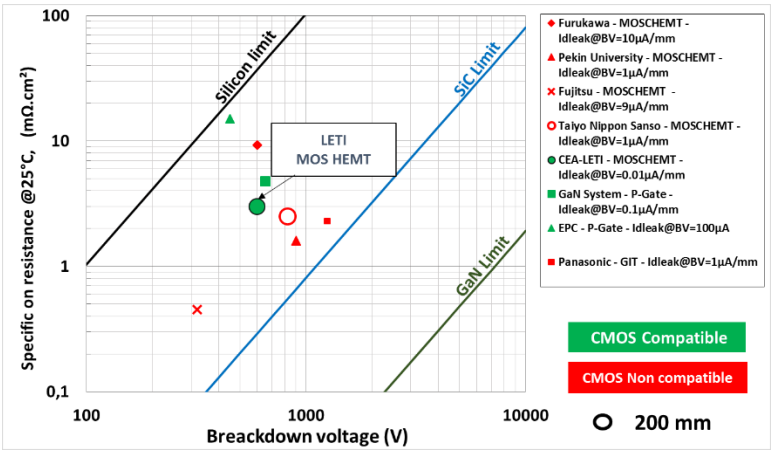


Figure 2. Specific on resistance versus breakdown voltage. Benchmark of different laboratory results versus CMOS or non CMOS compatible technology.

## Concluding Remarks

The use of GaN-on-Si as a substrate for high power transistors is becoming an increasingly common choice, as an affordable large area alternative to expensive bulk substrates. Although there are still significant challenges to be overcome in order to produce high quality devices on these substrates, GaN devices will take full advantage of both the remarkable properties of GaN, and of production in CMOS compatible fabrication plants to achieve high performance and low cost devices.

Furthermore, the development of high power integrated circuits on GaN on silicon wafers will further reduce costs and encourage the use of this technology. With all of these advances, it will surely not be long before GaN-on-Si devices become a huge market as the demand for highly energy efficient convertors becomes ever greater.

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# 4 - Buffer design in GaN-on-Silicon Power devices

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**Status**

Uptake of GaN devices for power applications requires that they can be manufactured in volume at comparable cost to Si components, and with validated device reliability. The key innovation that has made this possible is the ability to grow epitaxial device quality layers of GaN and AlGaN on 6" or 8" (111) Si wafers. Together with the development of Si CMOS compatible device process flows, this has allowed GaN power devices to be fabricated using existing Si fabrication lines with Si and GaN processing occurring in parallel. This section addresses the electrical and material design of the GaN-on-Si epitaxial platform that is now being used to realise HEMT devices for power applications.

GaN HEMTs were first successfully grown on Si in the 1990s, however the epitaxy did not have sufficient breakdown voltage for power applications. GaN-on-SiC RF devices used Fe doping to suppress short-channel drain leakage and increase drain breakdown, representing the first realization that the nominally insulating GaN layer underneath the 2DEG channel is actually electrically active and needs just as much design and optimisation as the upper barrier and channel region. However, Fe doping was found to deliver insufficient breakdown voltage when applied to high voltage power devices. Eventually it was found that a combination of a complex strain relief buffer together with carbon doping to control breakdown could achieve sufficient voltage handling[1]. Unfortunately there continued to be bulk trapping related issues collectively known as dynamic $R_{ON}$ dispersion or current collapse, and their solution has only recently been demonstrated commercially. The reasons for the wide variation in dynamic $R_{ON}$ performance achieved for apparently identical carbon doped epitaxies is only now becoming understood.

**Current and Future Challenges**

Key issues in epitaxial growth of GaN-on-Si are the lattice and thermal expansion coefficient mismatches which make strain management critical. As a result large numbers of defects (>$10^{10}$cm$^{-2}$) are generated, and cracking of the GaN layers can occur on cooling from the growth temperatures (≈1000°C) [2]. The epitaxial layer structure which has been adopted to solve these issues is shown in Figure 1. A nucleation layer of AlN is universally used to initiate growth and avoid the Ga/Si eutectic that causes "melt-back". This is followed by a strain relief stack, where two successful approaches have been found based on either a step-graded AlGaN layer[3], or a superlattice of AlN/GaN[4]. The detailed stack design is normally proprietary. These buffers are used to induce compressive strain during growth which counteracts the tensile strain introduced on cooling, preventing cracking and yielding a flat wafer. To aid growth uniformity, thick Si substrates (1mm) tend to be adopted, which also helps to reduce the wafer breakage during processing which has been observed for standard thickness wafers (675µm). Total epi-layer thickness as large as 8µm can be achieved, but the challenges of wafer bow and stress become more difficult to overcome. Typical dislocation densities at the surface of the stack, i.e. at the 2DEG, are ≈$10^{9}$cm$^{-2}$.

Due to the incorporation of impurities and point defects, as-grown GaN is typically n-type and it has been found that it is essential to add deep level dopants to suppress leakage. The dopant of

choice is carbon[1] with a density well above $10^{18}cm^{-3}$ delivering excellent isolation and breakdown voltage. Carbon primarily incorporates substitutionally on the nitrogen site[5]. This pins the Fermi level about 0.9eV above the valence band making the GaN:C p-type, with electrical transport being via low mobility holes rather than electrons. It is found that the carbon doping must be spaced away from the active 2DEG to reduce trapping effects[6]. A key issue with carbon doping is current collapse (dynamic $R_{ON}$)[7]. Charge trapping occurs in the epitaxial bulk during off-state operation when there is high drain bias. When the device is switched on, trapped negative charge reduces the electron density in the active channel and increases the on-resistance. Some current commercial devices show as much as a factor of two increase following off-state bias.

**Advances in Science and Technology to Meet Challenges**

Suppression of current collapse is key for technology uptake. The p-type nature of GaN:C means that there is a p-n junction between the 2DEG channel and the bulk of the epitaxy, meaning that the bulk can be electrically floating. Suppression requires that this floating buffer is grounded to the active 2DEG channel preventing it from providing a back bias, and hence, counter-intuitively, a vertical leakage path is essential. Figure 2 shows an electrical network representation of the buffer, and simulations to show the impact of different leakage paths[8]. It is found that there is a trade-off between vertical leakage and current-collapse, with careful process control of leakage paths being absolutely required. Current state-of-the-art power devices are able to achieve less than 10% change in $R_{ON}$ in the 25-150°C temperature range by careful leakage control[9]. Recently it has been shown that changing the stoichiometry of the $Si_3N_4$ surface passivation can change the bulk vertical leakage and control the dynamic $R_{ON}$[10]. Further work is still required to achieve a guaranteed simultaneous optimisation of leakage and current collapse.

Many power switching topologies require the series connection of devices. Current technologies would require a hybrid packaging approach to prevent undesirable Si substrate bias being applied to the upper transistor in a half-bridge configuration. New approaches to allow transistor electrical isolation are therefore required before full integration is feasible. One approach being investigated is the use of buried oxide layers with 200V isolation being achieved by imec.

Operating at voltages much above 650V will require the growth of thicker epitaxy, and that requires a solution to reducing stress. Although single crystal GaN or AlN would be the ideal substrates, cost and wafer size make this unlikely to have any impact. One possible approach is the use of thermal expansion matched substrates as an alternative to Si wafers. For example polycrystalline AlN wafers have been successfully used as a growth substrate, achieving 18µm thick epitaxial layers.

**Concluding Remarks**

GaN-on-Si based power transistors are already achieving impressive performance and reliability based on the remarkable ability to grow strain-engineered, electrically-optimised, high-quality epitaxy on low cost 6” or 8” Si wafers. Buffer-related trapping leading to dynamic $R_{ON}$ has been a serious issue, requiring a delicate balance between leakage and performance for its suppression. This is only now being achieved by commercial suppliers. Going significantly beyond the current 650V market segment to much higher voltages will require major changes and innovation in the substrates and epitaxy to allow thicker epitaxial layers to be grown yet still retaining control of wafer bow.

**Acknowledgements**

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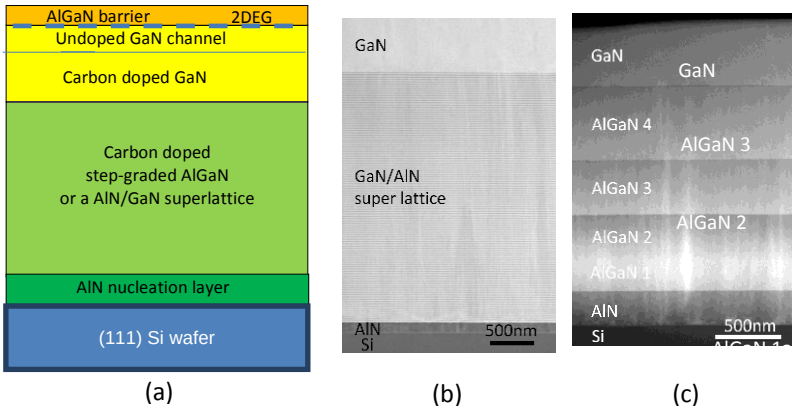


**Figure 1.** (a) Schematic cross-section of the typical epitaxial layer structure used for the manufacture of GaN-on-Si HEMTs. (b) TEM image of a GaN/AlN superlattice buffer layer and (c) a step graded AlGaN buffer layer, both on Si substrates.

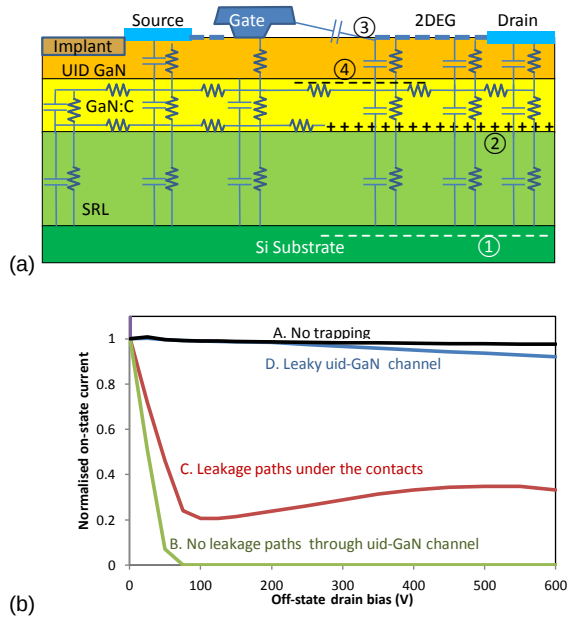


Figure 2. (a) Schematic showing leakage and capacitive paths within the buffer. ① to ④ indicate some of the key locations where charge accumulates. (b) Simulated dynamic $R_{ON}$ for different leakage paths within the buffer. All these different behaviours are observed in practice[8].

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# 5 - Challenges in growth for GaN power Electronics

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**Status**

Gallium nitride (GaN) based devices are promising for many power applications such as switching functions and inverters that can save a significant amount of energy. The performance and efficiency of these GaN power devices greatly rely on the epitaxial growth of GaN and related alloys. High quality GaN epitaxial growth can be achieved by using native free-standing GaN substrates. However, the downside of epitaxial GaN-on-GaN is it is expensive and only small-diameter GaN substrates. This in turn impede the mass production of GaN power devices at an affordable cost for commercial applications. To overcome this, the heteroepitaxial growth of GaN is carried out on foreign substrates such as silicon carbide (SiC), sapphire and silicon (Si). From commercial aspects, the heteroepitaxial growth of GaN-on-Si is attractive because of the large-size scalability of inexpensive Si substrates. Nevertheless, the areas of concern are the large differences in the physical properties between wide bandgap GaN and Si substrate that often results in poor crystal quality leading to high dislocation density, pits and cracks for GaN-on-Si. Therefore, appropriate epitaxial growth of GaN-on-Si and subsequent fabrication processes are absolutely necessary for power device applications. For example, several switching applications require lateral GaN-on-Si high-electron-mobility transistors (HEMTs) with high breakdown voltage (BV) [1]. To realize these GaN-on-Si lateral devices, we have used the metalorganic chemical vapor deposition (MOCVD) grown thick-AlN initial layer and GaN/AlN strained layer superlattice (SLS) structures. The AlGaN/GaN HEMTs grown on 8-inch silicon by using similar epitaxial growth technique delivered a high BV of 1.6 kV. For expanding the applications to electric and hybrid vehicles, high performance GaN power devices are required to drive high-power motors, power modules such as DC-DC converter and inverters. Typically, in these applications high-voltage GaN-on-Si vertical devices with reduced chip area are preferred. To facilitate the fabrication process of such devices, we have successfully grown thick GaN-on-Si vertical structures by using conductive buffer layers comprising of thin-AlN initial layer and SLS. The recent advances in the hetero epitaxial GaN-on-Si are encouraging for the growth of GaN power electronics on larger diameter Si substrates.

**Current and Future Challenges**

Despite its merits, the GaN-on-Si power devices have also associated technical challenges which need attention. Of these, the most important issue is the growth of a high-quality and thick GaN-on-Si. The large differences in lattice constants and thermal expansion coefficient between GaN and Si are responsible for the difficulties in the growth of high-quality and thick GaN-on-Si. The inset of Fig. 1 shows the cross-sectional structure of AlGaN/GaN HEMT on Si using metalorganic chemical vapour deposition (MOCVD). High temperature growth of GaN-on-Si could likely result in melt-back etching of Si substrate caused by Ga atoms [2]. As a result, deep pits, dislocations and cracks could arise, which in turn would deteriorate the device performance like an increase in buffer leakage, and reduced breakdown [3]. Therefore, the growth of high-temperature-grown AlN nucleation layer (NL) is indispensable to avoid both the melt-back etching and deep pits. Recent studies have revealed the influence of AlN NL on the vertical breakdown characteristics for GaN-on-Si and the AlN NL with better surface morphology and lower O impurity were preferred to grow highly resistive buffers [4]. Figure 1 illustrates the typical relationship between wafer bowing and total epitaxial thickness for the AlGaN/GaN HEMT on 4-inch Si. From this correlation, it could be understood that the use of GaN/AlN SLS is effective in controlling the bowing [5]. Subsequently, the growth of SLS is essential to control the wafer bowing for GaN-on-Si. Additionally, thick epi layers grown by using SLS multipairs supressed the vertical leakage and showed a vertical breakdown field of 2.3 MV/cm [6]. A high lateral $BV_{Off}$ of 1.4 kV was also demonstrated for AlGaN/GaN HEMT on Si grown with the above recommendations [7]. The recent systematic investigations and the promising results as discussed earlier would provide substantial understanding for the growth dynamics of epitaxial GaN typically on 8-inch Si substrates. Indeed, our AlGaN/GaN HEMT on 8-inch Si has shown a three-terminal off-state breakdown voltage 1650 V for the gate-drain distance of 50 µm. The availability of modern MOCVD reactors with multi-wafer capability and evaluation tools suggest promising features for GaN-on-Si lateral power devices.

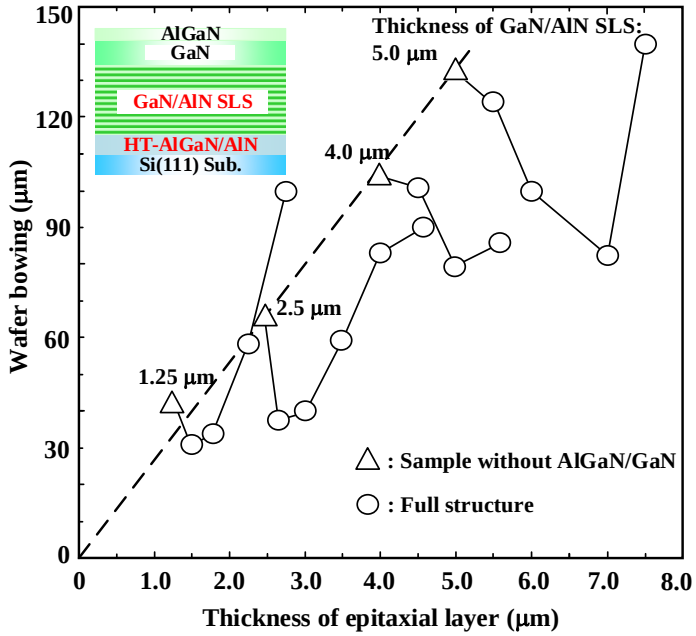


**Figure 1.** Wafer bowing as a function of total epitaxial layer thickness of AlGaN/GaN HEMT on Si. Copyright 2012 IEEE, reprinted with permission from Ref. 5.

**Advances in Science and Technology to Meet Challenges**

The GaN-on-GaN vertical devices are expected to play a vital role in future high-power conversion applications as it can reduce the overall chip area. However, the GaN substrate has disadvantages such as its limited wafer size and are expensive. Therefore, the realization of GaN-on-Si vertical devices is the upcoming challenge owing to growth and fabrication difficulties. Unlike the lateral AlGaN/GaN devices, deeper understanding on the growth and fabrication of GaN-on-Si vertical devices are required for potential power device applications. Some researchers have demonstrated the GaN-on-Si vertical p-n diodes fabricated by wafer bonding and substrate removal technology [8]. This technique could complicate the fabrication process and eventually lead to increase in cost. Others showed GaN p-n diodes by using a quasi-vertical structure [9]. Irrespective of these methods, a detailed study is required for the growth of GaN-on-Si vertical structures that should complement the fabrication as well. To realize such GaN-on-Si vertical device, (i) the doping density ($N_d$-$N_a$) in the drift region must be controlled and (ii) the buffer layer should be conductive. Figure 2 represents the net $N_d$-$N_a$ in the drift region as a function of $SiH_4$ flow rate for a GaN-on-Si grown with two SLS thicknesses. As shown, the $N_d$-$N_a$ could be controlled for GaN-on-Si by increasing the SLS multipairs, which is due to the reduction of dislocation density. The conductive buffer layers including the AlGaN/AlN layers and SLS are indispensable for realizing GaN-on-Si vertical devices. Therefore, a Si-doped AlN NL as thin as 3 nm was initially deposited followed by the deposition of Si-doped AlGaN and SLS. This novel fully vertical GaN-on-Si p-n diode comprises of doped buffer layers and not involve substrate removal technology. This GaN-on-Si p-n diode has ohmic contacts on the p-GaN layer and backside of n+-Si substrate, that showed a turn-on voltage of 3.4 V and a breakdown voltage of 288 V for the 1.5-µm-thick $n^-$-GaN drift layer [10]. The BV can be further improved by increasing the buffer thickness and/or by using field plate structures. These improvements in the MOCVD growth of GaN-on-Si vertical structures suggest their potential role in power electronics in near future.

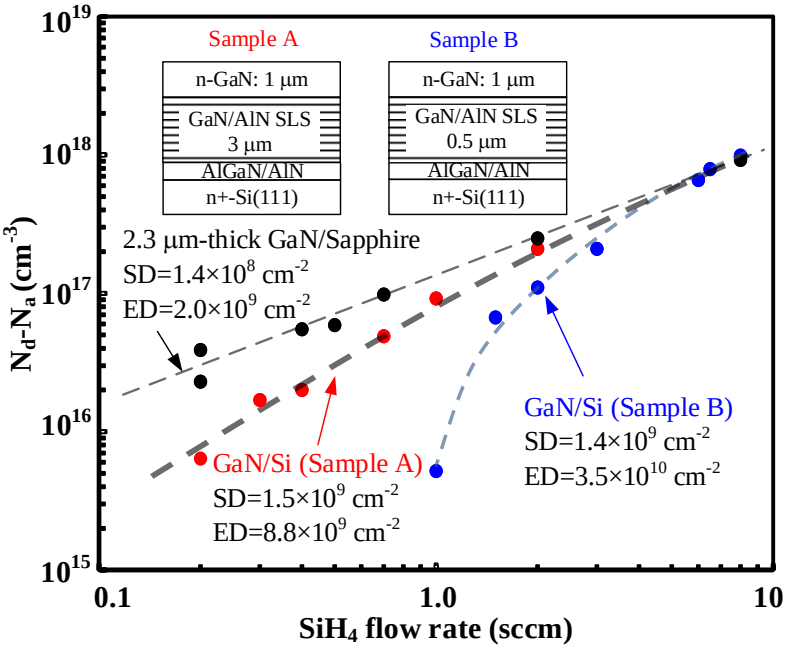

**Figure 2.** Net doping concentration as a function of $SiH_4$ flow rate for GaN-on-Si with different SLS thickness. For comparison, the data of GaN/sapphire are also shown. Copyright (2016) The Japan Society of Applied Physics, reprinted with permission from Ref. 10.

## Concluding Remarks

The GaN-on-Si power devices are emerging to play a dominant role in the next-generation power electronics. Significant improvements in the hetero epitaxial growth and device fabrication are indispensable for the commercialization of these power devices. For the epitaxial growth of GaN-on-Si lateral devices, we have utilized the high temperature AlN NL to prevent the melt back etching of Ga into Si. It was also found that the growth of SLS is essential to control the wafer bowing for GaN-on-Si. In addition, the growth of SLS multipairs effectively enhanced the breakdown voltage of GaN-on-Si HEMTs. On the other hand, fully-vertical GaN-on-Si p-n diodes were demonstrated by using conductive buffer layers. We have used AlN NL as thin as 3 nm and SLS multipairs, both highly doped in order to realize fully-vertical GaN-on-Si p-n diodes. These advancements in the MOCVD growth of GaN-on-Si and device fabrication processes will lead to the high-performance power electronics.

## Acknowledgement

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# 6 – Vertical GaN Power Devices

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**Status**

Central to improving the efficiency of power electronics is the availability of low-cost, efficient and reliable power switching devices. GaN-based devices are exciting candidates for next-generation power electronics. Currently, both lateral and vertical structures are considered for GaN power devices. Vertical GaN power devices have attracted significant attention recently, due to the capability of achieving high breakdown voltage (*BV*) and current levels without enlarging the chip size, the superior reliability gained by moving the peak electric field away from the surface into bulk devices, and the easier thermal management than lateral devices [1].

Since 2010, the field of vertical GaN power devices has grown exponentially and seen numerous demonstrations of vertical diodes and transistors (figure 1). A 3.7 kV vertical GaN pn diode [2] and a 1.1 kV vertical GaN Schottky barrier diode (SBD) [3] have recently showed near-theoretical power figure of merit. Trench metal-insulator-semiconductor barrier Schottky diodes [4] (figure 2(a)) and junction barrier Schottky diodes [5] (figure 2(b)) have also been proposed to combine the good forward characteristics of SBDs (e.g. low turn-on voltage) and reverse characteristics of pn diodes (e.g. low leakage current and high *BV*).

Several structures have been proposed for vertical GaN transistors, with the highest *BV* close to 2 kV. Current aperture vertical electron transistor (CAVET) combines the high conductivity of a two-dimensional electron gas (2DEG) channel at the AlGaN/GaN heterojunction and the improved field distribution of a vertical structure [6] (figure 2(c)). The CAVET is intrinsically normally-on, but a trench semi-polar gate could allow for normally-off operation [7] (figure 2(d)). Vertical GaN trench MOSFETs have no 2DEG channels, but do not need the regrowth of AlGaN/GaN structures and are intrinsically normally-off [8] (figure 2 (e)). Recently, vertical fin MOSFETs have been demonstrated to achieve normally-off operation without the need for p-type GaN materials or epitaxial regrowth [9] (figure 2(f)).

While most vertical devices utilize expensive GaN substrates, it is also feasible to make vertical GaN devices on low-cost Si substrates. Quasi- and fully-vertical GaN-on-Si vertical diodes have been demonstrated with a *BV* over 500 V and excellent high-temperature performance [10]. These devices can enable 100-fold lower substrate and epitaxial cost than GaN-on-GaN vertical devices.

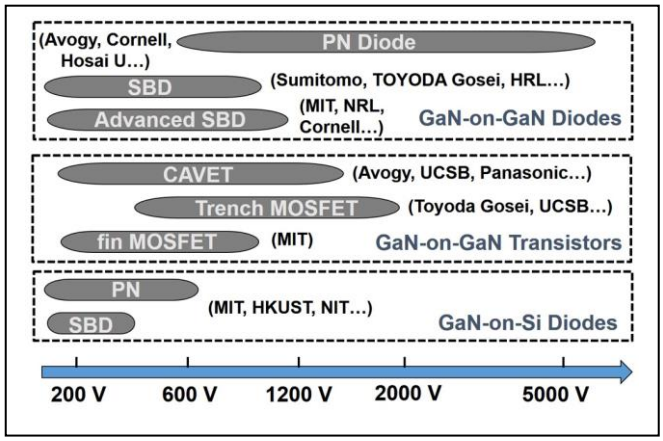


**Figure 1.** Overview of the main device types and voltage classes for the vertical GaN power devices reported in recent years.

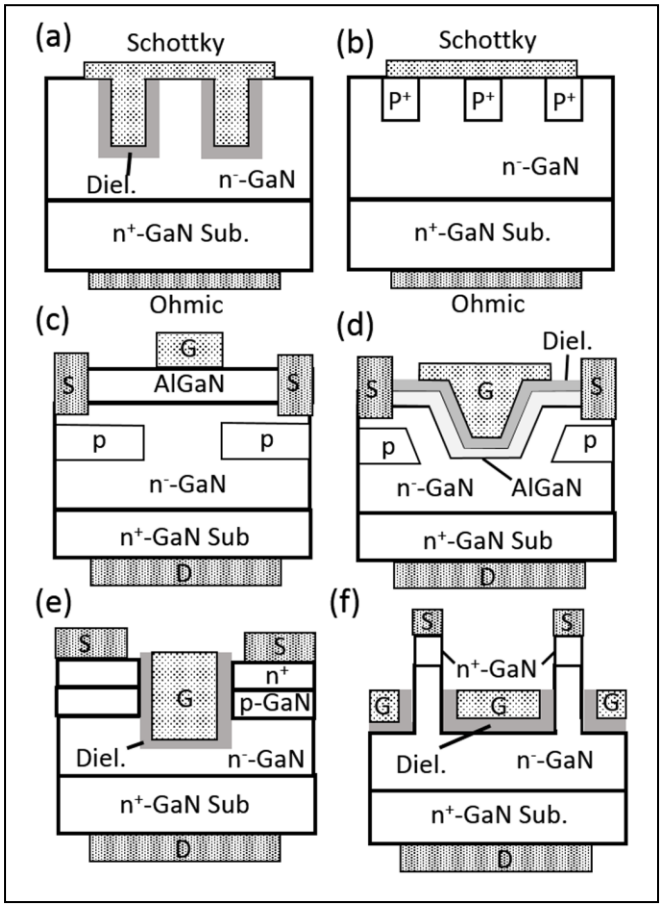


Figure 2. Schematic of representative vertical GaN advanced Schottky barrier diodes and vertical GaN transistors: (a) trench MIS barrier Schottky diode, (b) junction barrier Schottky diode, (c) CAVET, (d) trench CAVET, (e) trench MOSFET and (f) vertical fin MOSFET. In this Figure, "Diel." stands for dielectrics, and "Sub." for substrates.

**Current and Future Challenges**

In spite of the great progress, the full potential of vertical GaN SBDs and transistors has not been exploited yet. The *BV* demonstrated in these devices, with no avalanche capability reported, is still much lower than the avalanche *BV* in vertical GaN pn diodes. The lack of avalanche capability would greatly compromise the device robustness when operating in inductive switching environments. Although the nature of avalanche breakdown is still not fully understood in GaN devices, a key factor is believed to be good edge termination technologies and a way to remove holes from the structure. In SiC power devices, successful edge termination technologies, such as junction termination extension and field rings, was enabled by selective p-type doping. However, in GaN devices, the current selective area doping or selective area epitaxial regrowth technologies cannot yield material of sufficiently high quality to enable defect-free patterned lateral pn diodes. In particular, p-type implantation and activation in GaN is far from mature. With complicated activation annealing schemes, the activation ratio for acceptors is typically below 5%, resulting in very low concentration and mobility for the activated free holes [5].

There remain open questions on the selection of carrier channels in vertical GaN transistors to improve the device forward characteristics. The ideal channel for these devices would have normally-off configuration with high carrier mobility and without the need for epitaxial re-growth. Further work is needed for all the three channels reported so far, 2DEG channel [6], MOS inversion layer [8] and bulk fin channel [9].

The commercialization of vertical GaN power devices has been hindered by the high cost of bulk GaN substrates. The mainstream GaN substrates are 2-inch, while 4- and 6-inch GaN substrates are available very recently in small volumes. The wafer cost (per area) for 2-inch GaN-on-GaN is \$60~\$100/cm$^2$, still much higher than the cost for 4-inch SiC (~\$8/cm$^2$) and 8-inch GaN-on-Si (~\$1/cm$^2$). The fundamental challenge is how to achieve the material quality associated with free-standing GaN substrates, while allowing the devices to be transferred to alternate substrates and have the GaN substrates re-used to reduce cost.

**Advances in Science and Technology to Meet Challenges**

Different technological solutions can be envisioned to address the challenges in making patterned lateral pn junctions for edge termination structures. For example, compared to p-type ion implantation, n-type ion implantation (e.g. Si, N, etc.) and activation is much easier. Lightly-doped p-GaN edge terminations has been then demonstrated by implanting donors to compensate highly-doped p-GaN layers in vertical GaN pn diodes [2]. Patterned pn junctions have also been reported by n-type ion implantation into epitaxially grown p-GaN regions [5]. Besides selective ion implantation, the patterned pn junctions can be also made by selective p-GaN regrowth to fill n-GaN trenches. The initial feasibility of this approach has been demonstrated in CAVET [6], although much more work is needed to study the regrown interface quality and passivate parasitic leakage currents.

In parallel, different electrical, mechanical and chemical techniques are under development to enable devices to be lifted off from native GaN substrates and transferred to low-cost substrates. Successful layer transfer technology, combined with patterned interconnections on the supporting substrate and re-use of GaN substrates, should greatly reduce the cost and pave the way to commercialize high-performance vertical GaN power devices.

Another approach that can fundamentally circumvent the cost issue of vertical GaN devices is to fabricate them on Si substrates, which could allow for almost 100-fold lower wafer and epitaxial cost as well as 8-inch fabrication. Recently, GaN-on-Si vertical pn diodes with blocking capability of 500-600 V have been demonstrated [10]. Fully-vertical GaN-on-Si power devices have also been demonstrated by different technologies, such as layer transfer, conductive buffer layer, and selective removal of the substrate and buffer layer. To improve the performance of these devices, advances in epitaxial growth technology are needed to enable thicker GaN layers with very low background carrier concentration (< $10^{16}$ cm$^{-3}$) on Si substrate.

**Concluding Remarks**

Vertical GaN devices are key to achieve the high currents (> 100 A) and voltages (> 600 V) required by many power applications, such as electric vehicles and renewable energy processing. Record performance near the theoretical Baliga figure of merit has been demonstrated in vertical GaN pn diodes, although more work is needed in vertical Schottky barrier diodes and transistors. Exciting research opportunities exist in the field, especially in making patterned pn junctions, recycling GaN substrates and developing vertical GaN devices on Si substrates.

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# 7 – GaN Insulated Gate Field-Effect Transistors

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**Status**

GaN-based insulated gate field-effect transistors with an insulating gate dielectric provide many desirable properties such as suppressed gate leakage and large gate voltage swing [1]. These devices are typically in the form of metal-insulator-semiconductor HEMT (MIS-HEMT) or MIS-FET with the insulating dielectric on a heterojunction (e.g. AlGaN/GaN) channel or a GaN channel, respectively, as illustrated in Fig. 1(a) and (b). The MIS-HEMT was first studied for RF/microwave power amplifier applications [2], and then intensively investigated as a promising power switching device. The MIS-gate transistors are especially attractive to high-frequency power switching applications because they can better tolerate gate voltage over-shoot that often occurs in circuits with high slew rate.

As is the case of Si- and SiC-based MOSFETs, the gate dielectric in GaN insulated gate FETs is required to deliver a dielectric/III-nitride interface with low trap density, high reliability and long lifetime under various stresses (e.g. electrical, thermal, humidity, etc.). GaN MIS-HEMTs typically exhibit depletion-mode (D-mode) operation with a large negative threshold voltage ($V_{th}$) because of the presence of high-density positive polarization charges in the barrier layer (e.g. AlGaN). The D-mode MIS-HEMT, with its gate (input) terminal seldom forward biased during circuit operation, typically exhibit less adverse effects from the gate dielectric. This is mainly due to the presence of the barrier layer that decouples the 2DEG channel from the interface/border traps in the dielectric as long as the "spill-over" of electrons toward the dielectric does not occur, leading to small $V_{th}$ hysteresis. Very good gate reliability [3] has been obtained in D-mode MIS-HEMTs featuring a thin gate dielectric layer ($SiO_2$, $Si_3N_4$ or high-κ dielectrics) under relatively small forward gate bias.

Enhancement-mode (E-mode) MIS-HEMTs and MIS-FETs with a positive $V_{th}$ are highly desirable from the circuit application point of view for their simpler gate control circuitry and fail-safe operation. To fully turn on the channel current, however, large positive forward gate needs to be applied. This is when the gate dielectric is under the most demanding operational conditions (e.g. high electric field, charge injection to the dielectric and carriers leaking through the dielectric). $V_{th}$-instability (both static and dynamic) at different temperature and bias stress conditions, and its impact on dynamic on-resistance ($R_{ON}$) need to be systematically studied and clearly understood [4, 5]. The time-dependent dielectric breakdown (TDDB) is the ultimate hurdle to overcome before commercialization of E-mode GaN-based MIS-HEMTs and MIS-FETs.

**Current and Future Challenges**

Trap states at the dielectric/III-nitride interface and inside the dielectric present the biggest challenges to GaN MIS-HEMTs and MIS-FETs [6]. With a wide bandgap in GaN, a large energy window is available to accommodate interface and bulk trap states at shallow and deep energy levels with short and long emission time constant $\tau_{it}$. The dynamic charging/discharging processes of these traps could lead to $V_{TH}$ instability during a switching operation, and consequently affect circuit and system stability.

Unlike Si on which highly uniform and highly reliable thermal oxide can be prepared using high-temperature (800 °C ~ 1200 °C) furnaces, GaN surface becomes unstable when the ambient temperature exceeds 800 °C. In addition, the Ga-O bonds at an oxide/III-nitride interface fundamentally induce high-density gap states, except in a few very specific crystalline oxide

configurations, according to a first-principles calculation study [7]. Thus, removing the detrimental Ga-O bonds at the GaN surface is a critical step for obtaining low interface trap density ($D_{it}$). If oxide-based gate dielectric is to be used for their high dielectric constant and large bandgap, a non-oxide (e.g. nitride-based) interfacial layer would be highly desirable.

Although there are many reports on E-mode GaN MIS-HEMTs and MIS-FETs in research literature, the commercialization of these devices has been hindered by concerns over the gate dielectric reliability. The commonly used gate dielectric (SiN, $SiO_2$ and $Al_2O_3$) is deposited by PECVD or ALD (atomic layer deposition) at relatively low temperature (at 300~400 $^oC$). While the low temperature helps maintain GaN surface morphology, it is also the main reason for high-density defects in the dielectric, making it difficult for these devices to pass reliability tests and qualifications. High-temperature annealing only shows moderate effect on enhancing the dielectric reliability. Thus, it is of critical importance to develop high-temperature gate dielectric films (e.g.~ 800 $^oC$ or above) with lower defect density and longer TDDB lifetime. The biggest challenge to high-temperature dielectric on GaN is the degradation (via decomposition or chemical reaction) of GaN surface at high temperatures. A possible solution could feature a low-temperature interface protection layer and high-temperature gate dielectric.

**Advances in Science and Technology to Meet Challenges**

The first D-mode GaN MIS-HEMT was demonstrated using PECVD-$SiO_2$ as the gate dielectric [2]. With MOCVD-grown in-situ $SiN_x$ as the gate dielectric, low $D_{it}$ and excellent gate reliability are obtained [3]. At 10 years, for a 100ppm failure rate, a $V_{gs\_max}$ of ~3.1V is extracted, which is well above the operating $V_{gs}$ for a D-mode MIS-HEMT ($V_{gs\_max}$=0V).

The first E-mode GaN MIS-HEMT was demonstrated using PECVD-$SiN_x$ deposited on fluorine-implanted AlGaN/GaN heterojunction [8]. Low-damage and well-controlled dry and digital etching techniques are being developed to obtain positive threshold voltage. E-mode partially recessed MIS-HEMTs and fully MIS-FETs have both been developed with low on-resistance, high saturation current, small $V_{th}$ hysteresis and low dynamic on-resistance. In particular, *in-situ* removal of native oxide and consequent nitridation by low-power plasma (as illustrated in Fig. 1 (c)) prior to dielectric deposition [9] are important techniques for producing high-quality dielectric/GaN interface by passivating the dangling bonds while introducing minimum gap states.

To achieve high gate dielectric reliability under large positive gate bias required for E-mode insulated gate FETs, $SiN_x$ deposited by LPCVD (low-pressure chemical vapor deposition) has emerged as a compelling candidate as it possesses several important benefits including large conduction band offset with GaN ($\Delta E_c$ ~ 2.3 eV), relatively high dielectric constant ($\kappa$ ~ 7) and especially the long TDDB lifetime as a result of the low defect density achieved at high deposition temperature (e.g. 780 $^oC$). Implementing the LPCVD-$SiN_x$ gate dielectric in recessed-gate E-mode MIS-HEMTs and MIS-FETs has been more challenging since an etched GaN surface suffers more severe degradation than an as-grown GaN surface at high temperatures. An effective approach to suppressing such a degradation while maintaining low $D_{it}$ ($10^{11}$~$10^{12}$ $cm^{-2}$ $eV^{-1}$) has been developed using a low-temperature PECVD-$SiN_x$ thin film as an interfacial protection layer [10], as depicted in Fig. 2. For a 10-year lifetime, the maximum gate bias is determined to be 11 V at a failure rate of 63.2 % and 9.1 V at a failure rate of 0.01%.

**Concluding Remarks**

There is strong demand for GaN insulated gate field-effect transistors with both depletion- and enhancement-mode operations, as the insulated gate provides strong immunity to control voltage spikes and could be driven with circuits very similar to those used for the mainstream Si and SiC power MOSFETs. The most critical need of a GaN insulated gate FET technology is a gate dielectric technique that simultaneously delivers low interface/bulk trap density and robust reliability under stringent

electrical and thermal stresses. The E-mode GaN MIS-HEMTs and MIS-FETs are especially challenging as they operate under large positive gate bias and the recessed-etched GaN demands better protections during high temperature process associated with high-quality dielectric deposition. Combining low-temperature interfacial layer with high-temperature gate dielectric could be a promising pathway toward reliable and stable GaN insulated gate FETs.

**Acknowledgements**

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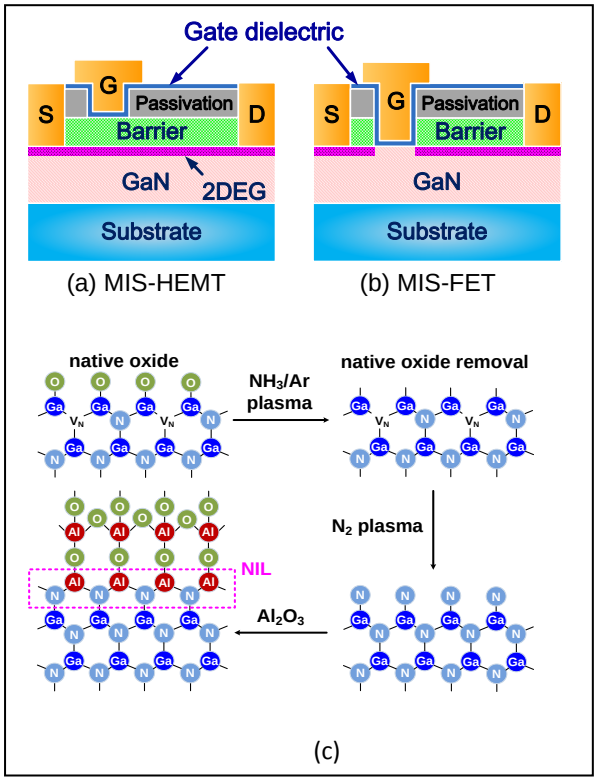


**Figure 1.** Schematic cross sections of GaN-based (a) MIS-HEMT and (b) MIS-FET. (c) Schematic process for *in-situ* native oxide removal and surface nitridation of GaN.

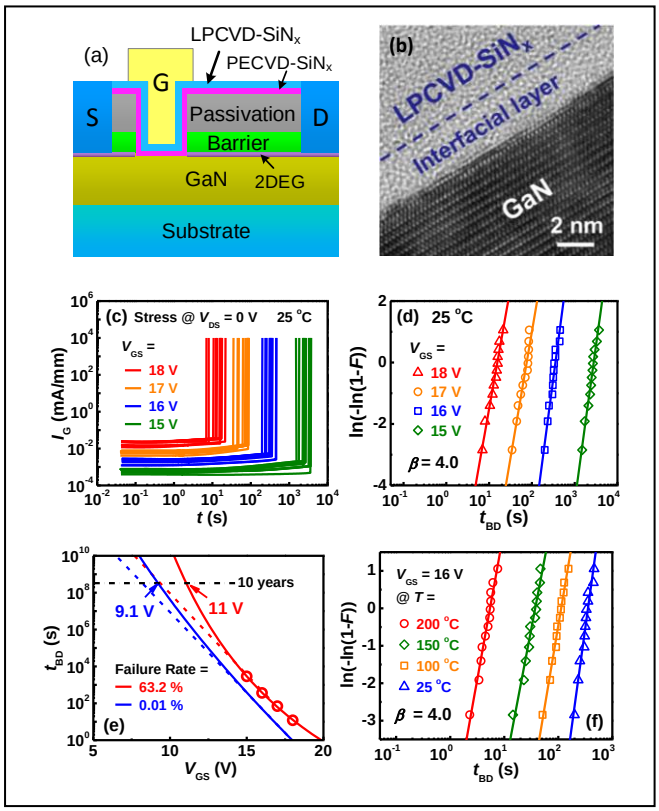


**Figure 2.** (a) Schmematic cross section of an E-mode fully recessed GaN MIS-FET with interfacial protection layer. (b) High-resolution TEM of an LPCVD-$SiN_x$/PECVD-$SiN_x$/GaN interface. (c) Time to breakdown ($t_{BD}$) of the LPCVD-$SiN_x$ MIS-FETs with interfacial protection layer at forward gate stress of 18, 17, 16 and 15 V at 25 °C. (d) Weibull plot of the electric field-dependent $t_{BD}$ distribution. (e) Lifetime prediction with a failure rate of 63.2 % and 0.01 %, respectively. (f) Weibull plot of the temperature-dependent $t_{BD}$ distribution.

# 8 - Reliability of GaN Power Devices: Normally-on and Normally-off

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**Status**

Reliability is essential for the application of GaN power devices to critical electronic systems, for high-voltage energy conversion, control of electrical engines, automotive electronics [1]. GaN is a robust material, capable of withstanding extremely high electric field and temperature; in order to fully exploit its potential, deep levels effects and failure mechanisms induced by high voltage and high temperature stress must be known in detail.

Several technological options are available for the fabrication of GaN power HEMTs: Schottky-gate normally-off transistors, which have the simplest structure, are prone to higher leakage current with respect to their insulated-gate counterpart; nevertheless they can reach breakdown voltages higher than 1100 V and can achieve normally-off operation in conjuction with a Si MOS driver in cascode configuration [2]. Normally-off devices can be achieved using p-type AlGaN or GaN with high acceptor doping on top of the AlGaN [3]. Recessed-gate metal-insulator-semiconductor devices (MISHEMT) enable operation at positive gate bias without measurable gate current $I_G$ [4]. Normally-off operation can be achieved by decreasing the thickness of the AlGaN layer under the gate in a recessed structure.

The different structures can be affected by specific failure mechanisms. When biased in off-state at high reverse bias, Schottky-gate, normally-on HEMT were subject to a significant and progressive increase of gate leakage current (several orders of magnitude), correlated with the onset of leakage current paths which can be detected by electroluminescence (EL) [5]. Further analysis revealed that this catastrophic increase of $I_G$ was time dependent, that time to failure depended on the electric field, followed a Weibull distribution, and decreased slightly with temperature (activation energy = 0.12 eV). $I_G$ increase was attribute to the formation of a conductive percolation path across defects [5]. This concept of GaN as a “lossy dielectric” was a major breakthrough for GaN reliability: it allowed the extrapolation of device lifetime using standard time-dependent dielectric breakdown (TDDB) tests, and promoted the study of other GaN time-dependent failure mechanisms, described in the following Sections.

**Current and Future Challenges**

Time dependent breakdown effects in Schottky gate devices were due to different physical mechanisms either related to device design or materials quality : (i) in normally-on power Schottky HEMTs with double field-plate, TDDB was found to be due to the failure of the insulating SIN layer between the 2DEG and the first field-plate edge. Increased robustness was achieved by changing the substrate conductivity in order to move the 2DEG edge towards the drain [2]; (ii) in AlGaN/GaN power Schottky diodes, breakdown involved first the dielectric at the diode edge and then the AlGaN; as a consequence, lifetime improves by adopting either a thicker PEALD-SiN edge-

termination dielectric (from 15 nm to 25 nm) or a more robust one (25 nm in-situ SiN) [6]; (iii) drain-source off-state catastrophic breakdown of n-on Schottky gate HEMTs, may occur as a consequence of hole trapping and acccumulation at the source edge of the gate: trapped positive charge shifts threshold voltage towards negative values and turns on the device while a high drain voltage is applied, thus resulting in device burn-out [7].

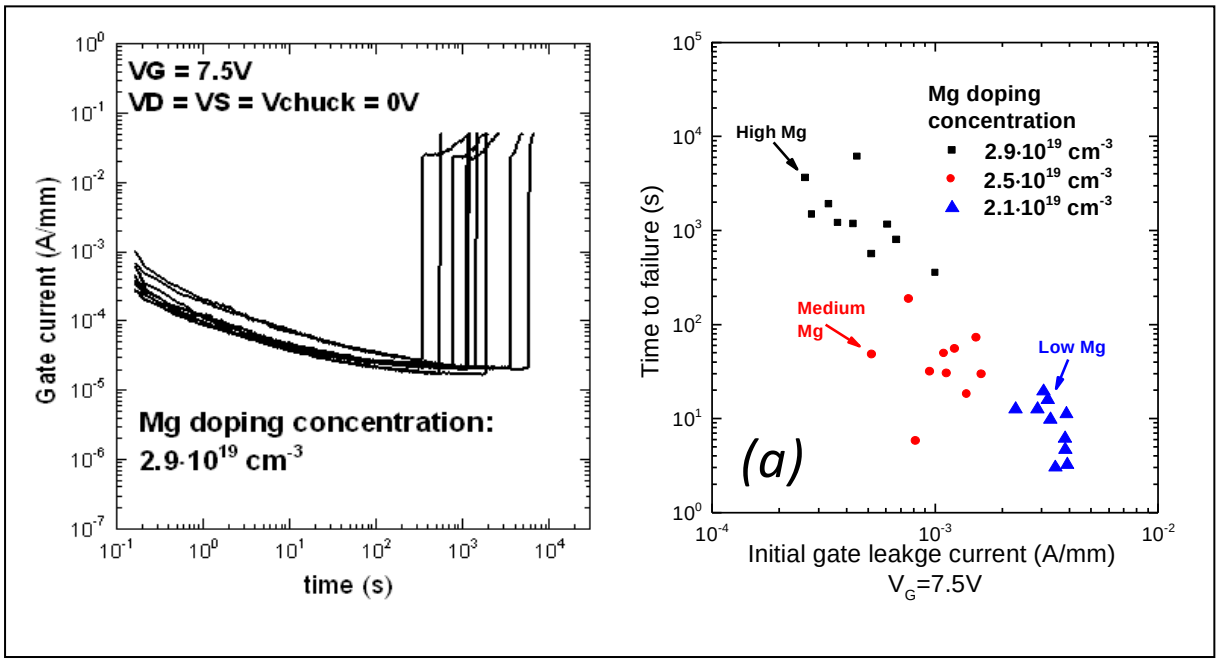


**Figure 1.** Left: Time-dependent breakdown experiment on the p-gate of a normally-off GaN HEMT; Right: dependence of time to failure on initial gate leakage current at $V_G$ = 7.5 V (and consequently on p-type doping concentration in the p-GaN layer. Reprinted with permission from ...

P-gate devices (either with an ohmic or a Schottky metal contact on top of the p-layer) are currently the most popular choice for n-off devices. A critical mechanism for p-gate HEMTs is the TDDB consequent to the application of a positive gate bias. In the case of a rectifying contact on p, positive bias leads to increased electric field, potentially leading to breakdown. Time to failure decreases at increasing gate leakage current and consequently at higher temperature ($E_a$ = 0.5 eV); times to failure are Weibull-distributed. Higher Mg doping in the p-layer reduces leakage current and therefore improves lifetime. A possible explanation consists in the accumulation of positive charge at the interface with the AlGaN, proportional to leakage current which, at its turn, enhances gate current and promotes further degradation. A second hypothesis implies the formation of a percolation path, consequent to defects formation due to hot carriers (collected by the gate). In this case also, times to failure are Weibull-distributed; a 20-years lifetime at $V_{GS}$ = +7.2 V was demonstrated for a 200 V n-off technology [3].

The vertical drain-substrate stack is also sustaining a high electric field and is prone to time-dependent breakdown: a 200 V n-off technology was submitted to tests at $V_{D\text{-substrate}}$ in excess of 700 V and failed due to vertical burnout in approximately 2 X $10^4$ s. Higher leakage current and temperature correspond to shorter lifetime, with a decrease which is thermally activated with a 0.25 eV activation energy. The maximum applicable voltage for a lifetime of 20 years with 1% failure rate is about 560 V at RT, considerably higher than the operating voltage [8].

The GaN MISHEMT represents an ideal structure for normally-off power GaN electron devices since the dielectric layer reduces significantly the gate leakage; unfortunately the MIS structure introduces new reliability problems, related with the stability of device threshold voltage.

Large positive $V_{th}$ shifts (positive bias temperature instabilities) have been observed under forward gate bias conditions and attributed to accumulation of electrons at the dielectric/III-N interface where a second electron channel forms in the so-called "spill-over" conditions [9]. According to [9], the density of interface states of any dielectric is currently high enough to completely deplete the 2DEG channel with a typical electron density in the order of $10^{13}$ $cm^{-2}$. Improvements therefore require either a reduction of interface states or an increase of the voltage required to induce the "spill-over".

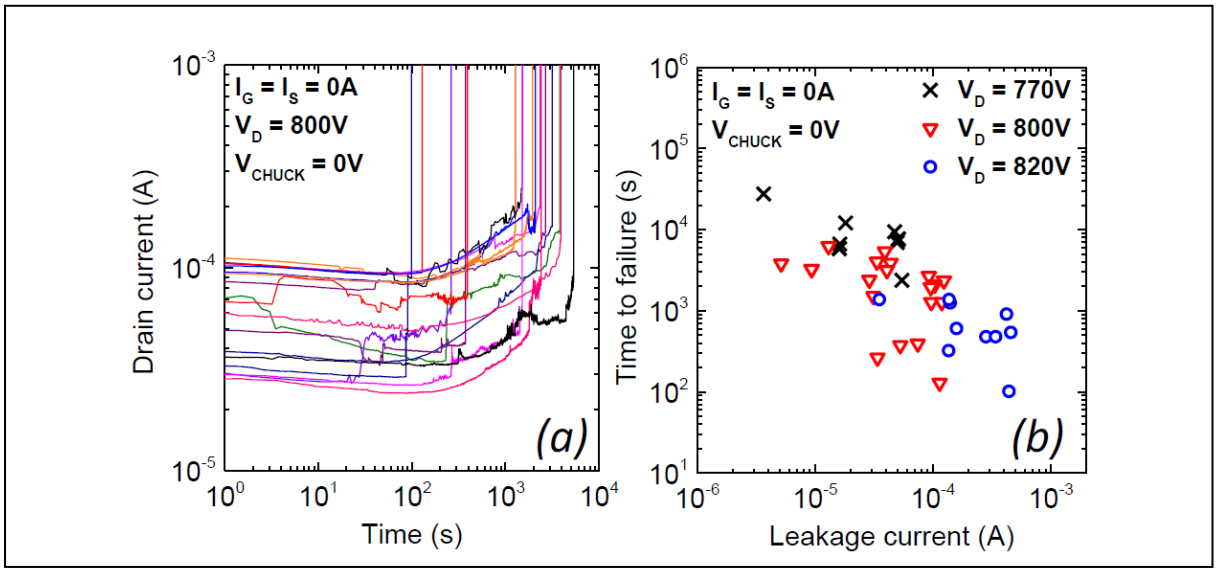


Figure 2. Left: time-dependent breakdown test on drain current at $V_{DS}$ = 800 V. Data refer to normally-off p-GaN gate devices at RT. Right: time to failure dependence on the initial leakage for three drain bias levels applied during the constant voltage stress. Reprinted with permission from ...

Negative voltage shift (NBTI), observed when negative voltage is applied to the gate is usually less severe, and becomes relevant only at high temperature (activation energy 0.37 eV, see [4] and reference therein). According to [4], NBTI is due to detrapping of states at the SiN/AlGaN interface; authors in [10] have formulated a unified model for PBTI and NBTI, which implies electron trapping/detrapping in pre-existing oxide traps that form a defect band very close to the GaN/insulator interface. NBTI can reduce the threshold voltage of n-off devices, thus thinning the safety margin in off-state. Conversely, NBTI does not represent a critical problem for n-on devices: under cascode operation, the on/off state is controlled by the Si MOSFET; moreover, due to the leakage current of the Si MOSFET, the HEMT is always in slight semi-on state, and this limits the electric field across the SiN/AlGaN stack.

**Advances in Science and Technology to Meet Challenges**

Schotty-gate and MISHEMT n-on devices for cascode configuration and p-gate n-off devices are gaining maturity; time-dependent breakdown effects can be evaluated using standard, well-established testing methods; methods for long-term thermal stability assessment still have to be developed and consolidated into standards. Some issues remain, concerning gate leakage, hot electron degradation, istantaneous breakdown. Concerning n-off MISHEMTs, stabilization of threshold voltage remains an open issue, which requires in-depth physical characterization of surface and interface properties and of dielectric materials

**Concluding Remarks**

This chapter has reviewed reliability of n-on and n-off GaN power HEMTs, with particular emphasis on time-dependent breakdown mechanisms and NBTI/PBTI effects. Results described here have been obtained by means of on-wafer short-term (<100 h) tests. Knowledge on the long-term reliability of these devices is being developed only recently, thanks also to cooperative projects such as POWERBASE and InRel-Npower, which promise to achieve full maturity for GaN power technologies in the 650 – 1200 V range.

**Acknowledgements**

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# 9 – Plasma Processing for GaN Power Electronic Devices

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**Status**

To significantly impact the marketplace of energy efficient power switching, GaN-based transistors must be produced in high volumes at low cost. Adopting silicon-based substrates and silicon-like manufacturing approaches enables production using legacy 150 mm and 200 mm wafer facilities driving cost efficiencies. Standard silicon manufacturing approaches rely heavily on plasma processing for etching semiconductors and deposition of dielectrics and metals. These procedures need to be migrated to GaN-based materials and optimised to minimise process induced damage of the semiconductor layers. These can present as reductions in channel carrier concentration and mobility and therefore increased on-resistance; and hysteretic effects due to the formation of charge trapping states which can influence dynamic response.

As shown in Figure 1(a), there are three areas where plasma processing as part of device manufacture can have a significant effect.

1 – in the source-drain regions, controlled etching into the semiconductor to the same relative position compared to the device channel offers a generic solution as described in [1] irrespective of the thickness of the AlGaN barrier layer of the device.

2 – in the gate-drain region, effective passivation of the semiconductor surface is vital to minimise leakage current and current collapse. A variety of dielectrics are being actively used and demonstrated encouraging performance [2], [3] with further work required to fully understand the interaction between the dielectric and the semiconductor.

3 – in the gate stack, a dielectric introduced between the gate metal and the semiconductor (Figure 1(b)) can suppress gate leakage current. Subjecting the semiconductor to a fluorine plasma (Figure 1(c)) has been shown to be effective in shifting positive the device threshold voltage [4], important for normally-off device operation. There can be issues with long term reliability of this approach however. An alternate is to perform a gate recess etch prior to gate dielectric and metal deposition (Figure 1(d)) – controlling the etch depth to control threshold voltage requires the use of low damage plasma based atomic layer etching approaches, such as those described in [5]. Wafer scale and wafer to wafer uniformity of these etching approaches still need to be confirmed.

**Current and Future Challenges**

*Plasma Processing in the Source-Drain Region*

As reported in [1] and [6], plasma etching of the semiconductor layers in the source-drain region before contact metal deposition results in reduced contact resistance (0.18 Ohm mm was obtained in [6] using "patterned" $Cl_2$-based plasma etching), and reduced thermal budget (contact resistance of 0.5 Ohm mm was achieved in [1] at a contact anneal temperature of 550 $^oC$ using a $SiCl_4$-based chemistry). Driving down the thermal budget to below 500$^oC$ opens new opportunities for "gate first" approaches to device realisation which may be important in improving the stability of the gate/semiconductor interface.

*Plasma Processing in the Gate-Drain Region*

As described in [2], passivation of the gate-drain region using low pressure chemical vapour deposition (LPCVD) of $SiN_x$ with optimal conditions had a strong effect on both current collapse and

leakage currents. This is a high temperature (850 $^{o}$C) process. A key property of the LPCVD-SiNx films in this study was the stress. Recently, the use of stress control in room temperature deposited inductively coupled plasma-CVD (ICP-CVD) $SiN_x$ films for surface passivation was also shown to reduce significantly leakage currents [3], therefore a key challenge at this time is to understand the underlying physical mechanisms that govern the leakage current and current collapse phenomena.

*Plasma Processing in the Gate Stack*

As mentioned above, the incorporation of a gate dielectric is important to reducing the gate leakage current in GaN transistors and allows for a larger gate voltage swing, which is particularly important for normally-off devices. As reported in [7], controlling the properties of the GaN surface, in this case by removing a SiN capping layer deposited as the final stage of the wafer growth using an $SF_6$ plasma etch immediately prior to atomic layer deposition of an $Al_2O_3$, resulted in a 4x reduction in hysteresis to 60 mV for GaN MOS-capacitors. This work also reported the impact of the introduction of TiN into the gate stack, which resulted in a 35% increase in accumulation capacitance. Understanding of the origin of these effects will be vital to further device optimisation.

**Advances in Science and Technology to Meet Challenges**

Understanding the role and impact of plasma-based processing will be vital to further optimising and improving the efficiency of GaN power device operation in terms of static and dynamic on-resistance, current collapse, leakage currents and threshold voltage control. Control of the semiconductor surface, both mechanically and chemically is a key. This can best be addressed by understanding and correlating the properties of the semiconductor surface and its interface with dielectrics and/or metals with transistor performance. Combining plasma processing equipment so that an etched wafer can be transferred directly into a dielectric or metal deposition tool is an important technological advance. This “clustered” approach to wafer processing is relatively standard in the mainstream silicon industry – research needs to be undertaken to validate such approaches for GaN-based materials and devices for power electronics applications. A cluster tool such as that shown in Figure 2 is already proving highly insightful in this regard. In addition to combined process chambers, the cluster tool shown in Figure 2 also has in-situ scanning Auger capability. Clustered plasma process and metrology engines are going to be the key to unlocking the full potential of plasma processing for GaN power electronics.

**Concluding Remarks**

Plasma processing is a vital element in the manufacture of GaN power electronics as, based on its use in the mainstream silicon industry, only plasma processing offers reproducible wafer scale and wafer to wafer etching and dielectric and metal deposition. Arguably, the GaN surface is one of the most process sensitive in the electronics industry, so its control at a chemical level is key to fully optimising device performance. Having a profound and fundamental understanding of the impact of plasma processing on the GaN surface is therefore an imperative to ultimate GaN power device realisation.

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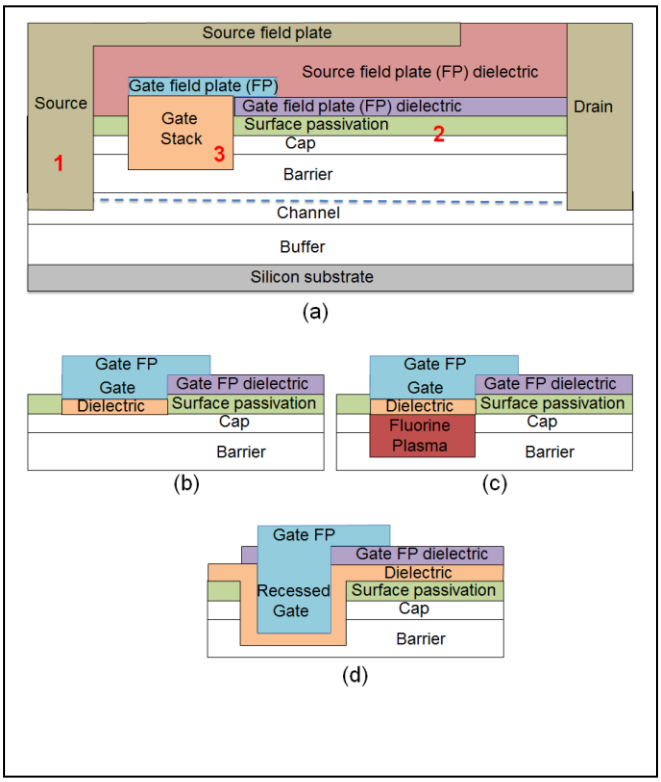


**Figure 1.** (a) Schematic of a generic GaN-on-silicon power transistor. Key areas for device optimisation using plasma processing are **1** – recessed ohmic contacts for low resistance, high field compatible source-drain contacts ; **2** – the gate-drain region to mitigate leakage current and dynamic on-resistance issues; **3** – the gate stack to control threshold voltage and minimise gate leakage current with minimal hysteretic effects. (b), (c) and (d) are specific gate stack solutions. (b) has a gate dielectric deposited on the GaN surface; (c) has a gate dielectric above a fluorine plasma treated region to tune threshold voltage; (d) has a recessed gate prior to dielectric deposition

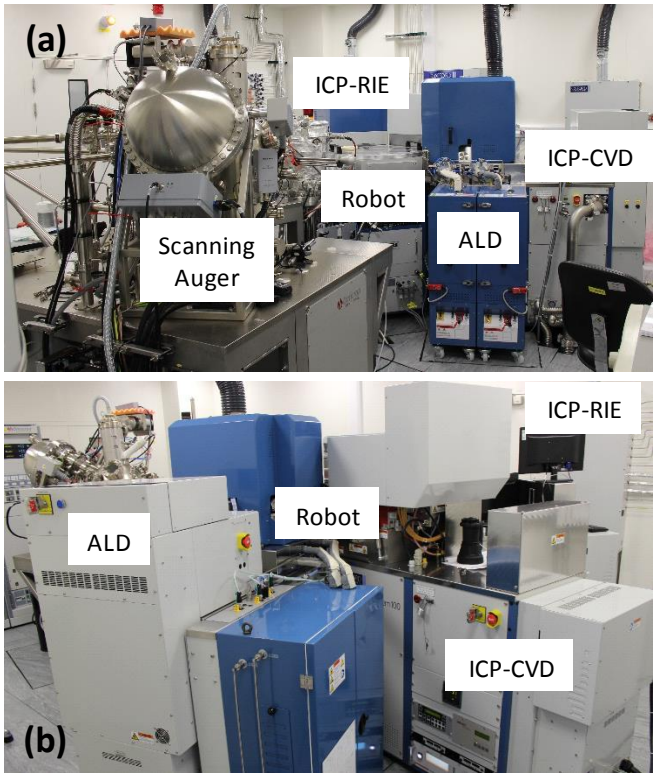


Figure 2. Views of clustered plasma process chambers. A central robot handler allows movements of wafers between reactive ion etch, atomic layer deposition and chemical vapour deposition chambers without atmospheric exposure. Also clustered is a scanning Auger microscope to enable in-situ mid-process surface analysis.

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# 10 - Challenges to dielectric processing for E-mode GaN

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**Status**

The growth of ultrathin dielectric layers into GaN-based devices incorporating metal-insulator-semiconductor (MIS) structures has been extensively investigated as a method of minimising gate leakage currents, which are lost through the gate by electron tunnelling, leading to poorer power efficiency and electrical noise. For normally-off, enhancement mode devices, low off- currents are necessary to reduce the static power consumption and ensure fail-safe operation. The incorporation of various oxide or nitride dielectric materials into GaN-based heterostructures has been explored previously using a range of conversion (e.g. oxidation or wet chemical methods) and chemical (e.g. CVD or ALD) or physical vapour (e.g. sputtering or evaporation) growth processes. Regardless of the dielectric or fabrication process used, the discontinuity (see figure 1) at the resulting insulator-semiconductor interface gives rise to electrically active interface trap states. These can influence device performance, by acting as remote impurity scattering centres that can either lower the carrier mobility ($\mu$) [1] or influence the threshold voltage ($V_{th}$) [2]. The insulator itself may also contain deleterious intrinsic charge traps. Furthermore, the insulator will have valence band and conduction band offsets with respect to the III-nitride (e.g. GaN, AlGaN, InAlN etc) which will influence the carrier confinement properties in the semiconductor [3]. Despite these issues, both depletion-mode and enhancement-mode insulated-gate GaN-based transistors have been realised through the development of surface pre-treatments; dielectric film deposition processes; and post-deposition heat treatments [4].

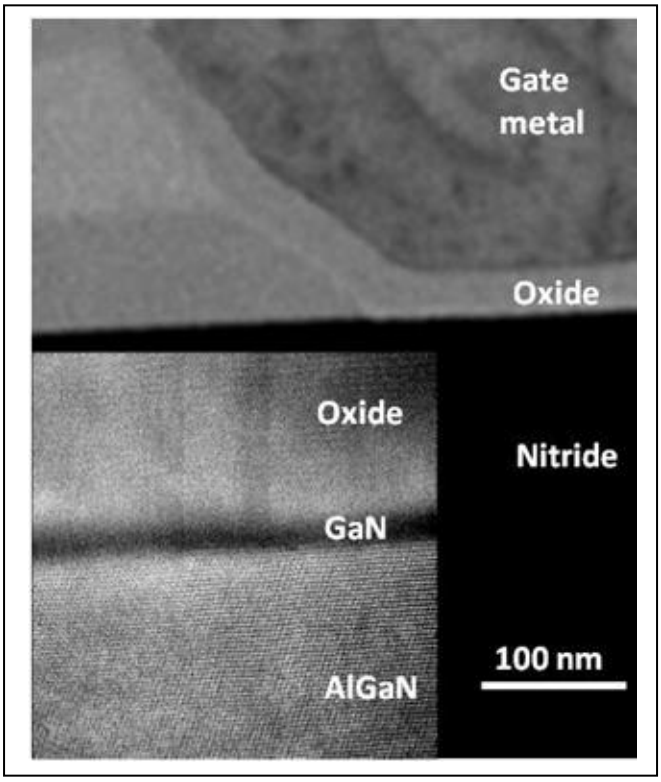
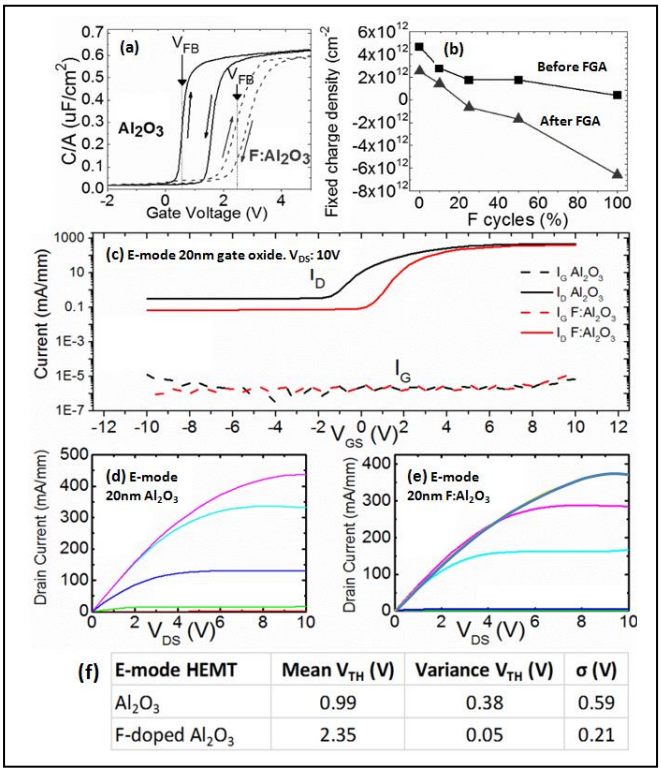



**Figure 1.** Cross section TEM of the gate MIS structure in a GaN-based MISHEMT. The inset shows a high resolution dark field image indicating the disruption of atomic lattice structure in the GaN cap adjacent to the $Al_2O_3$ dielectric layer.

**Current and Future Challenges**

The integration of insulted gate dielectric with III–N semiconductors continues to represent a significant hurdle to be overcome before E-mode MIS transistors can reach maturity. The dynamic charging of deep traps at the dielectric-semiconductor interface is associated with $V_{th}$ instability and long term reliability of the material system under electrical stress is uncertain. To begin to address some of these issues, gate dielectrics have been explored in the fabrication of E-mode MIS GaN-based devices. Two of the approaches explored to date include: (1) fluorine-doping which is used to passivate or neutralise positive charges at the semiconductor surface or in the dielectric itself; or (2) by recessing the gate by selectively etching the barrier layer in the region under the gate electrode. One example of F-doping via, $CF_4$-plasma treatment in the gate region of an AlGaN/GaN high-electron-mobility transistor (HEMT) [5]. Exposure to the plasma implants $F^-$ ions into the AlGaN barrier and underlying GaN-channel. After application of an ALD $Al_2O_3$ gate - dielectric, the F-doped semiconductor acts as a source of fluorine that diffuses into an $Al_2O_3$ dielectric compensating its intrinsic positive charge. It was reported that the $V_{th}$ increases with gate dielectric thickness, exceeding 3.5V for gate dielectrics 25 nm thick. Using in-situ fluorine-doping during ALD $Al_2O_3$ deposition, we reported the control of $V_{th}$ in enhancement-mode AlGaN/GaN MIS-HFETS [6]. When compared to the undoped dielectric, the F-doping caused positive threshold voltage shift (see figure 2) and a reduction of positive fixed charge in the gate oxide.




(f)

| E-mode HEMT | Mean $V_{TH}$ (V) | Variance $V_{TH}$ (V) | σ (V) |
|---|---|---|---|
| $Al_2O_3$ | 0.99 | 0.38 | 0.59 |
| F-doped $Al_2O_3$ | 2.35 | 0.05 | 0.21 |

Figure 2. Effect of F-doping in $Al_2O_3$ in E-mode MOS capacitors (a) Reduction in CV hysteresis.(b) Influence of forming gas annealing on fixed charge density. Effect of F-doping in $Al_2O_3$ in E-mode MISHFETs (c) $I_D$ and $I_G$ versus $V_{GS}$ for 20 nm $Al_2O_3$ and F:$Al_2O_3$. (d) $I_D$ versus $V_{DS}$ for 20nm $Al_2O_3$ gate oxide with $V_{GS}$ from -4V to +6 V in 2 V steps. (e) ID against $V_{DS}$ for 20 nm F:$Al_2O_3$ gate oxide with $V_{GS}$. (f) Mean, variance, and standard deviation (σ) of $V_{TH}$ for 15 of each type of MISHFET.

A dielectric is exploited in recessed gate MIS-HEMT, to suppress gate leakage current and increase the on-state gate swing. However, in the case of E-mode MIS-HEMTs, $V_{th}$ hysteresis can be caused by

large positive gate voltages due to 2DEG entering the deep trap states at the oxide/III-nitride interface. A demonstration of how this effect can be mitigated is through the application of an $Al_2O_3$/AlN gate stack insulator [7]. The insertion of a 2-nm thin plasma enhanced ALD AlN interfacial passivation layer yielded a device with a $V_{th}$ of +1.5 V, a current density of 420mA/mm and an OFF-state breakdown of 600V with low drain leakage of 1.7μA/mm.

The preceding discussion has focused on n-type (2DEG) channel MIS E-mode devices, however the realisation of p-type (2DHG) devices has received less attention to date. A significant advance in this respect, has been the demonstration of complementary metal–oxide–semiconductor (CMOS) GaN field-effect-transistor technology [8]. This landmark achievement is considered in more detail elsewhere in this roadmap. In the context of the dielectric employed, an MOCVD AlN/SiN dielectric stack was exploited as the gate oxide for both NMOS ($\mu_e$ - 300 $cm^2$/V-s) and PMOS ($\mu_h$ - 20 $cm^2$/V-s) transistors. The devices were used to demonstrate a functional inverter integrated circuit.

Significant advances have been made in the integration of gate dielectrics into III-N transistors, with the main purpose of minimising leakage currents in normally-off devices. A variety of dielectric materials have been assessed, using different deposition processes, but the main focused has been on $SiO_2$, $SiN_x$ and $Al_2O_3$. The continuing challenges for E-mode MIS devices are: (1) the minimisation of charge trap densities at the insulator/semiconductor interface across the range of barrier and channel III-nitride materials; (2) minimisation of the effect charging – discharging of trap states which gives rise to $V_{th}$ instability; (3) minimisation of the influence of bulk and border traps within the insulator dielectric itself which may impair the long term gate reliability and performance; (4) the development of processes and materials matched to the thermal budget of the device manufacture and the longer term in-field operating environment; (5) lastly addressing issues (1)-(4) in the context of PMOS E-mode devices [9, 10].

**Advances in Science and Technology to Meet Challenges**

The challenges of processing dielectrics for E-mode GaN MIS-based device technology are comparable to those encountered over the last two decades in the field of silicon CMOS. Fundamentally, the processing of dielectrics requires atomic-scale control over the preparation of the semiconductor surface, followed by assembly of the insulator with sub-nanometre precision over non-planar substrates comprising of a mixture of materials. The strategies for preparing III-nitride semiconductor (e.g. GaN, AlGaN, AlInN etc) surfaces for subsequent dielectric deposition will continue further development for both NMOS and PMOS technologies. Where these are combined on the same wafer for nitride-based circuits will add process complexity. The solution to this problem will have to involve removal or conversion of any unwanted native contamination at the semiconductor surface. Ideally the semiconductor surface would be atomically planar after preparation. Various wet and dry (e.g. thermal and plasma) processes have been explored to passivate and protect the semiconductor. It seems likely that future strategies may rely more on capping the semiconductor wafer in-situ at the end the III-nitride growth process to mitigate the problems associated with post-growth environmental exposure. Obvious candidates for this would be AlN- or SiN-based materials, but could include others. Alternatively, advanced strategies for the dielectric deposition process (e.g. ALD MOCVD PECVD, LPCVD or some physical vapour deposition method), would involve an in-situ preparation step. As an example, one prospect might be the

introduction of an atomic layer etching (ALE) step to remove unwanted native oxide / contamination. ALE could be applied to remove disordered gallium oxide / aluminium oxide residue, prior to the ALD of a "dielectric – quality" ALD layer. To realise this, further research would be required to develop ALE chemistries for the group-III oxides and nitrides.

In addition to surface pre-treatments, there is clearly scope for the development of improved dielectrics. Alternatives to the existing candidates, future developments might target multilayer dielectric stacks to target the overall gate capacitance, whilst enhancing resistance to gate-leakage. Multilayer gate stack might also be exploited to engineer band alignments to both the underlying semiconductor and the gate contact material. Current research has identified the use of fluorine- or hydrogen- "doping" in $Al_2O_3$ or $SiN_x$, as a method of "defect engineering" to neutralise or passivate traps in dielectric materials. There is clear scope for basic materials research to take this defect engineering further to enhance the electrical properties of gate dielectrics.

**Concluding Remarks**

The incorporation of MIS structures within E-mode GaN transistors offers a range of device design freedoms to realise monolithic GaN power IC, with reduced parasitic inductance and more efficient power switching at high frequencies. It is foreseeable that the development of gate dielectrics will be tuned to meet three overarching challenges. Firstly at the materials level, the dielectric stack will mitigate the effects of detrimental traps or defects within the dielectric and at the nitride semiconductor-dielectric interface, with negligible gate-leakage and maximum resistance to high-voltage electrical breakdown. Secondly, at the manufacturing stage, processing technologies will be required incorporate the dielectric into increasingly complex device architectures within the bounds of thermal budget. Thirdly, the development of dielectrics will be driven by the operational issues of life-time and reliability in the extreme environments experienced by GaN-based device technology.

**Acknowledgements**

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# 11 - Future Applications, Roadmap for GaN ICs

Dan Kinzer and Stephen Oliver, Navitas Semiconductor

**Status - The Power GaN Progression**

With Gallium Nitride (GaN) already established as a leading material for LED / opto applications and for RF amplifiers, this wide band-gap material emerged as an interesting academic option for discrete power devices around the turn of the century. Today, discrete GaN power devices have been qualified to JEDEC standards from 80 to 650V, using technology that has advanced from complex, costly and slow 'cascoded d-mode' implementations in highly-inductive through-hole packaging, to true single-die, e-mode devices in SMT formats [1]. However, significant system factors still exist which restrict practical switching speeds, negate the performance advantages of GaN and, as a result, have slowed market adoption.

The answer to this problem is derived from the lateral structure of GaN itself. A two-dimensional electron gas (2-DEG) with AlGaN/GaN heterojunction gives very high mobility in the channel and drain drift region, so resistance is much reduced compared to both Si and SiC. Circa 2009, early GaN power IC technology was published from university research [2]. The ability to integrate multiple power switches on a single chip is a big advantage for GaN power ICs. Isolating substrates began with sapphire and silicon carbide, though it was clear that an ability to grow GaN onto Si substrates enabled a cost structure and an ability to use existing large-diameter wafer fabs that would be a big cost and capacity advantage. Since Si is conductive, this introduces an additional challenge, of handling the substrate potential, and the way that it interacts with the power device.

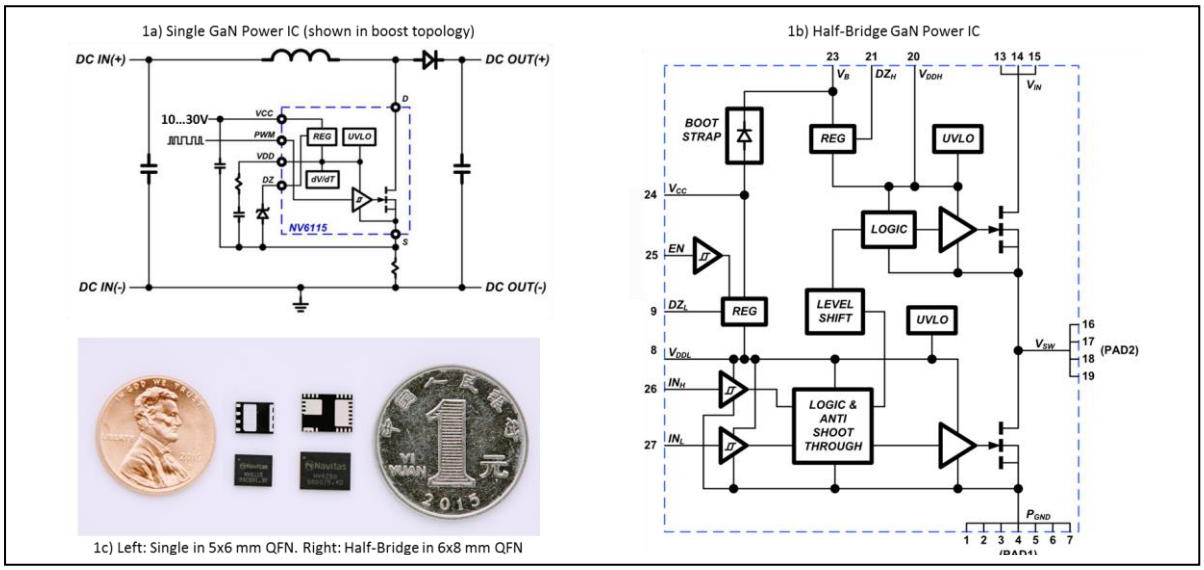


**Figure 1.** 650 V GaN Power ICs: 1a) single, 1b) half-bridge, 1c) package types, dimensions (Navitas Semiconductor)

**Current and Future Challenges - The GaN Power IC**

AllGaN™ is the industry's first GaN Power IC Process Design Kit (PDK), and allows the monolithic integration of 650V GaN IC circuits (drive, logic) with GaN FETs [3]. This proprietary PDK is remarkable given the restricted device-level tool-set, e.g. no p-channel devices are available. This monolithic integration is impractical using vertical GaN, d-mode GaN or SiC technologies.

For high-frequency operation, the most critical achievement has been the monolithic integration of GaN driver and GaN FET. In discrete implementations, the exposed GaN gate is vulnerable to noise

and potentially damaging voltage spikes. Even when the GaN FET is included in a co-packaged, multi-chip module, the impedance between Si driver output and GaN FET gate leads to losses and potentially unstable operation. Only a monolithic solution delivers the required speed, efficiency and robustness [4]. From the driver integration, we can then consider 'higher-order' functions of the power IC such as inclusion of logic, start-up protection, dV/dt control, dV/dt robustness, and ESD to create full-function GaN Power ICs. Another major step is the combination of two FETs plus all associated drive, level-shift, bootstrap charging, and protection features (e.g. shoot-through prevention, UVLO, etc.) into a complete half-bridge power IC. Now, PWM ICs need simply to generate two, low current, ground-referenced digital signals and the half-bridge GaN power IC completes this ubiquitous building block.

Since the 1990s, when Si-based junction-isolation (JI) level-shifting techniques were introduced, power designers have searched for higher-efficiency and higher-frequency methods. Hybrid level-shifter techniques, e.g. capacitive- or inductive-coupling, have been introduced but the disparate semiconductor technologies used, plus complex assembly techniques meant large and expensive modules. The 650 V GaN Power IC enables the true, next-generation, monolithic-integration approach and results in a level-shifter which has 10x lower loss than Si and 3x lower than the best-in-class hybrids.

**Advances in Science and Technology to Meet Challenges – Real-World Applications**

GaN is a low-loss, fast-switching material and enables a range of new high-frequency topologies to move from academic to commercial applications. The easy-to-use GaN power IC building block now becomes the core enabler for high frequency, soft-switching topologies such as active clamp flyback (ACF), critical conduction mode (CrCM) and totem-pole power factor correction (PFC) and LLC DC-DC circuits to enter mainstream markets [5], [6], [7]. In parallel, new magnetic materials have been released to production with high-efficiency operation up to 5 MHz. Multi-MHz DSP controllers are available for higher power applications and new high-frequency, cost-effective ASICs are being introduced to enable adoption in price-sensitive markets such as smartphone and laptop chargers. High MHz-range frequency with the simultaneous increase in efficiency delivers cost-effective, increased power density [8].

Practical examples of soft-switching topologies are shown below in Figure 2. Note that the mechanical construction/assembly techniques used are industry-standard, and readily-available at low cost.

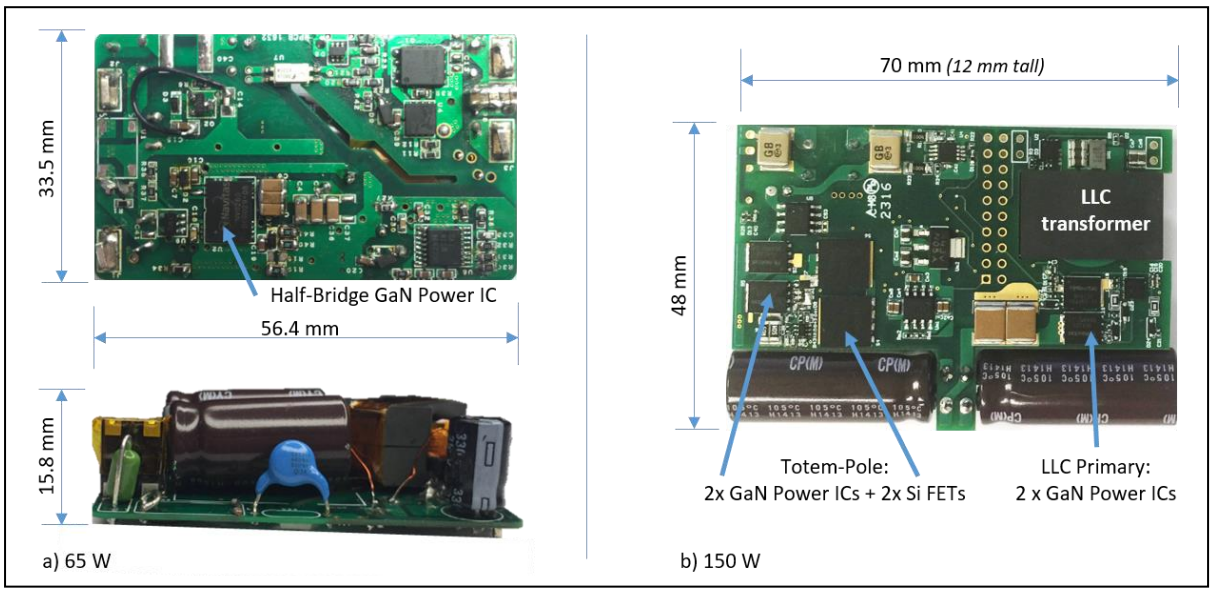


Figure 2. Examples of AC-DC converters using GaN Power ICs;
a) 65 W Active Clamp Flyback at 300 kHz using commercial control ASIC and Half-Bridge GaN Power IC, 94.5% peak efficiency at full load, 1.5 W/cc (24.6 W/in$^3$) uncased power density (Navitas Semiconductor), and
b) 150 W Totem-Pole PFC plus LLC at 1 MHz using single GaN Power ICs, >95% peak efficiency at full load, 3.7 W/cc (60 W/in$^3$) uncased power density. DSP controller not shown (courtesy of CPES, Virginia Polytechnic).

The same GaN Power ICs may be applied in high-power, multi-kW applications, with one example being a 3.2 kW, 1 MHz, AC-48 V converter prototype with 65 W/in$^3$ power density [9]. Here, the single devices are paralleled to achieve lower $R_{DS(ON)}$ and interleaving techniques are used for the Totem-Pole PFC and LLC sections.

## Concluding Remarks - Major Accomplishments, Major Opportunities

The last 20 years have seen GaN's progression from RF to power discrete and now to the first generation of AllGaN power ICs. This has enabled advanced, soft-switching topologies to enter the commercial marketplace. Next-generation monolithic integration (e.g. advanced I/O features, over-current and over-temperature protection) will enable even higher levels of efficiency, power density and reduced system cost.

## Acknowledgements

The authors wish to thank Dr. F.C. Lee (CPES, Virginia Polytechnic) and Dr. A.Q. Huang (FREEDM Systems Center, North Carolina State University) for their pioneering MHz application work with GaN Power ICs.

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# 12 - Potential of Polarisation Super Junction Technology in Gallium Nitride

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**Status**

Amongst many semiconductors, Silicon Carbide (SiC), Gallium Nitride (GaN) and Diamond can offer significant system level benefits and have the potential to meet the anticipated power densities by 2025 [1]. GaN offers similar performance benefits to SiC, but with a greater potential for cost-reduction as well as higher frequency. Price advantage over SiC is also possible because GaN power devices can be grown on substrates that are larger and less expensive than SiC. Since the first report of high density 2-Dimensional Electron Gas in 1991 [2] and High Electron Mobility Transistors in 1993 [3], GaN has gained traction and now discrete GaN transistors are emerging as commercial products. Their performance is however limited to about 1/5$^{th}$ of their potential capability by slower external silicon gate driver circuits required to control them. Si circuits have a limited operating temperature range and inherently efficient GaN devices are forced to slow down, leading to failure and severe derating of efficiency. The dual (Si & GaN) technology approach impacts cost deleteriously. By monolithically integrating control circuits with power devices on a single GaN technology platform the efficiency can be greatly increased, and cost reduced. Moreover, because of the difficulty in obtaining p-channel devices, integrated circuits (ICs) thus far demonstrated are made of n-channel devices.

**Current and Future Challenges**

In GaN-on-Si technology, the breakdown voltage is primarily determined by the GaN buffer and therefore thick buffer and transition layers are necessary to sustain high voltage, which make the wafers more susceptible to bowing and crack generation. The inherent tensile stress due to mismatch in lattice constants and coefficients of thermal expansion in such structures can also compromise the reliability of devices. Lack of avalanche capability or non-destructive breakdown behaviour, necessitates over-rating the device breakdown voltage for a given application. Moreover, there is a significant level of defects in layers and understanding of these defects and their relationship with device reliability is necessary. The conventional GaN technology uses metal field plates. However, the distribution of the electric field is not uniform, which impacts breakdown voltage along with rendering such devices to be sensitive to current collapse during high voltage switching. The field distribution is also highly sensitive to changes in charges accumulated in the insulators sandwiched between the semiconductor surface and the field plates. Realizing such high voltage devices also requires sophisticated processing capability for formation of precise field modulating plates. An alternative solution for manufacturing low-cost high-voltage GaN power switching devices, which can overcome some of the above-mentioned challenges is the Polarisation Super Junction (PSJ) technology, which is described in the next section. This technology is also a highly promising candidate for the fully GaN based power ICs.

**Advances in Science and Technology to Meet Challenges**

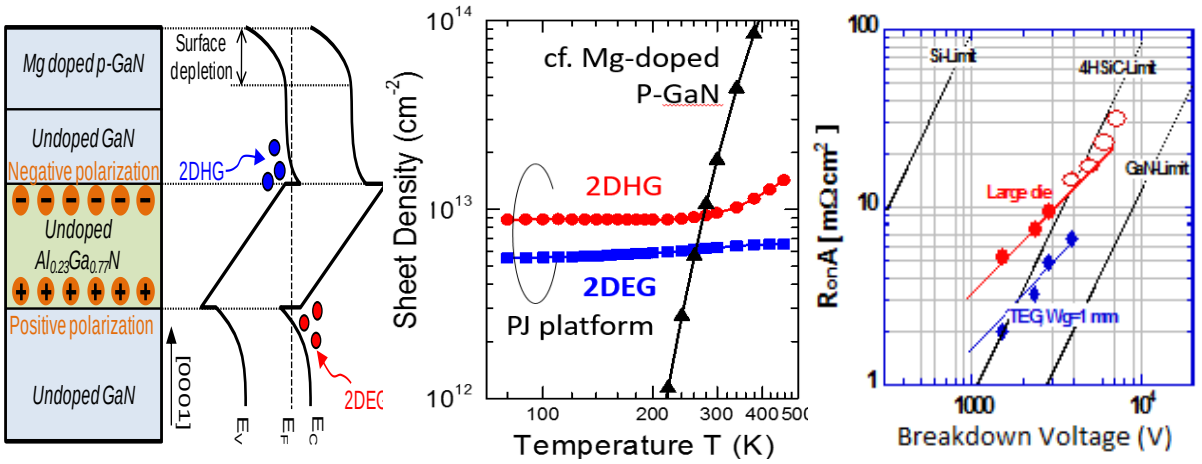


**Figure 1 (left): Double heterostructure in GaN [5]; Figure 1(middle) Measured 2DEG and 2DHG through Hall Effect measurements; Figure 1(right) Variation of measured specific on-state resistance with breakdown voltage of PSJ-HFETs against calculated unipolar 1-D material limits of Silicon, SiC and GaN [8].**

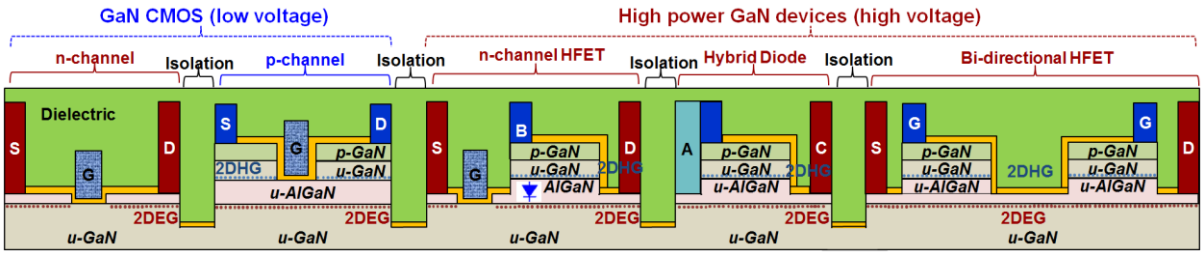


**Figure 2: Proposed PSJ Platform for Monolithic Power Integrated Circuits. Please note that the substrate is not specified. However, thin sapphire is the most cost-effective option because of the use of uniform thickness of 1 µm u-GaN buffer layers to serve for both low as well as high voltage devices and provide full electrical isolation (critical requirement for monolithic integration).**

In 2006, a polarisation junction (PJ) concept was proposed based on the charge compensation of positive and negative polarisation charges at heterointerfaces of a GaN/AlGaN/GaN structure [4]. This was followed by the successful demonstration of GaN double heterostructures, grown along the (0001) crystal axis, where high density positive and negative polarisation charges coexist at the AlGaN(000$\bar{1}$)/GaN(0001) interface with accumulated two-dimensional electron gas (2DEG) and two-dimensional hole gas (2DHG) accumulated at the GaN(000$\bar{1}$)/AlGaN(0001) interface respectively, as shown in Fig 1 (left) and Fig 1(middle) which has since enabled a Polarisation Super Junction (PSJ) technology [5]. Like the Superjunction in Si, PSJ enables linear scaling of breakdown voltage with increase in thickness or length of the drift region and with performances beyond that of 1-D 4-H Silicon Carbide limit, as shown in Fig 1(right). Over the past few years, high performance diodes, transistors as well bidirectional switches have been demonstrated [6,7]. Enhancement-mode PSJ-HEMTs have also been reported with most recent results of large (4 X 6 mm$^2$) and small devices made on Sapphire substrates showing with breakdown voltages beyond 3 kV [8]. Moreover, due to the effective lateral charge balance and field distribution, these devices fabricated on Sapphire substrate show no current collapse. One of the key attributes of the PSJ technology is that it is viable to make both NMOS as well as PMOS circuits, and CMOS inverter operation of a monolithic P- and N-channel MOSFETs has been demonstrated on this platform [9]. This technology also paves way for bidirectional switches with integrated diodes. This device is well suited for a variety of applications and for solid state circuit breaker because, PSJ offers the possibility of realising much lower saturation currents than conventional HFETs [5], while maintaining ultra-low on-state resistance. Thus, Polarisation Super Junction technology can pave the way for high power density monolithic integration of various devices for a variety of applications, as shown in Fig. 2.

Most recently, the PSJ concept has been extended to Vertical GaN technologies and is termed as Vertical Polarisation Super Junction (VIPSJ) with predicted benefits of 2 orders of magnitude reduction in specific on-state resistance in comparison to SiC at 1 kV rating [10].

**Concluding Remarks**

There are several scientific, technological and manufacturing challenges that need to be addressed before GaN power semiconductor devices can be considered mainstream. It is also becoming apparent that a transition from the general scheme of manufacturing power conversion circuits using discrete devices to that of a fully integrated power system-on-chip is anticipated to be a prerequisite to fully harness the high-frequency power switching benefits of GaN. To conclude, GaN PSJ technology will be instrumental in shaping a viable and a new era of an integrated power electronics for ultra-high-power density converters.

**Acknowledgements**

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# 13 - Technological Challenges in Next-Generation GaN-based Power Integrated Circuits

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**Status**

Si-based lateral power devices have been widely utilized in high-frequency and low-power converters for ratings of up to several hundred watts [1]. On the other hand, GaN-based heterojunction field-effect transistors (HFETs) utilizing polarization-induced 2D electron gas (2DEG) are emerging components for such high-frequency converters. GaN-based discrete devices up to 650-V rating are commercially available now. The development of GaN growth technology on conductive Si substrates has largely contributed to the improvement in the device performance and decrease in cost [2]. As a next step, towards achieving high intrinsic switching capability of GaN devices, monolithic integration of GaN-based converter circuits will be necessary. Area-specific on-resistances of GaN-HFETs are already two orders of magnitude smaller than those of Si-based lateral power devices. Owing to this significant footprint reduction, high output powers of up to several kilowatts can be expected in GaN-based monolithic converters. In this article, two technological challenges are addressed: the "crosstalk effect" and "heat dissipation" in next-generation ultra-high-frequency monolithic power integrated circuits (ICs). These issues are quantitatively discussed using simple analytical models.

**Current and Future Challenges**

As an example of GaN power ICs, if an integrated half-bridge circuit on a conductive Si substrate as shown in Fig. 1 is assumed with the following parameters: voltage rating of the GaN devices are 600 V, input voltage $V_{IN}$ is 400 V, 2DEG density $N_s$ has a conventional value of $10^{13}$ cm$^{-2}$, and dielectric constant $\varepsilon$ of the GaN-based epilayer is $9.0\varepsilon_0$.

Firstly, the "crosstalk effect" is discussed. In discrete GaN devices, the substrate potential is shorted with the source electrode. The conductive Si substrate acts as a back-side field plate contributing to the suppression of current collapse. However, in an IC, it induces a significant increase in the on-resistance of the high-side transistor [3]. This is because the 2DEG of the high-side transistor interacts with the substrate potential through the GaN epilayer capacitance $C_{epi}$. During the on-state of the high-side transistor, the input voltage $V_{IN}$ is directly applied to $C_{epi}$, inducing a 2DEG density reduction $\Delta N_s$:

$$q\Delta N_s = C_{epi}V_{IN} / A = \varepsilon V_{IN} / t_{epi}, \qquad (1)$$

where $q$ is the electron charge, $A$ is the GaN device area, and $t_{epi}$ is the GaN-based epilayer thickness grown over silicon substrate. If we consider a 2DEG density reduction of 10% (i.e., 10% on-resistance increase), the calculated $t_{epi}$ is 20 μm. In comparison with a GaN-based epilayer in conventional discrete devices (3-5 μm), power IC applications require an epilayer which is thicker by five times.

Next, the issue of "heat dissipation" challenges are discussed under hard switching condition. When the gate drive speed is sufficiently high, power loss of the hard-switching circuit (Fig. 1) reaches the minimum value. Under the minimum loss condition, the heat density $HD$ of the GaN chip can be expressed as

$$HD = Q_{oss}V_{IN} f / A = qN_s V_{IN} f, \qquad (2)$$

where $Q_{oss}$ is the output charge of each GaN transistor and $f$ is the the output pulse-width modulation frequency. Eq. (2) implies that a charge $Q_{oss}$ is supplied from the voltage source $V_{IN}$ during every switching period, and the energy is consumed as joule heat in the GaN chip. Fig. 2 shows the heat density calculated using Eq. (2). Although high-frequency operation is expected in hard-switched GaN

monolithic converters, the estimated heat density is unacceptably high. For example, it is 6.4 kW/cm$^2$ at 10 MHz.

**Advances in Science and Technology to Meet Challenges**

The substrate material for the growth of GaN-based layers is a key element of power ICs. Because conductive Si substrates induce the crosstalk effect, novel platform substrates are required for next-generation ICs, especially for high-voltage and high-frequency applications. GaN-on-silicon-on-insulator (SOI) technologies are a promising solution which can enable CMOS compatibility in the GaN device fabrication process [4, 5]. The contribution of the back-side field plate effect is also obtained through substrate contact from the front side [5]. However, a several-μm-thick $SiO_2$ buried layer will be required to sustain 600 V or more. The thermal conductivity of $SiO_2$ is two orders of magnitude smaller than that of Si. Therefore, heat dissipation from integrated GaN devices on an SOI substrate will be big challenge. Furthermore, GaN power device technologies on insulator sapphire substrates are equally promising candidates [6, 7] because they yield high-quality GaN crystals. However, on such insulator substrates, current collapse must be eliminated without the support of the back-side field plate effect. Effective lateral electric field management strategies will be necessary, such as polarization superjunction technology [6].

In addition, other emerging candidates must be considered. Because the thermal conductivity of SiC is three times higher than that of Si, GaN technologies on highly resistive SiC substrates have been widely used in RF applications and are also emerging candidates in power converter applications. Finally, GaN-on-diamond technology might be the ultimate solution to the heat dissipation issue because diamond has the highest thermal conductivity [8-10].

**Concluding Remarks**

In next-generation GaN-based power ICs, device isolation technologies are a key challenge, especially in high-voltage applications. GaN-on-SOI and GaN-on-sapphire technologies are promising candidates from this perspective. In addition, thermal management is a key issue. Area-specific on-resistance has been a major benchmark parameter of GaN-HFETs. In addition, the minimization of area-specific "thermal-resistance" will be a key strategy in GaN-based IC development. Therefore, GaN device technologies utilizing high-thermal-conductivity substrates such as SiC and diamond are also emerging as platform substrates for GaN power ICs. However, on any platform, potential advantages in performance and cost should be considered from the system level viewpoint.

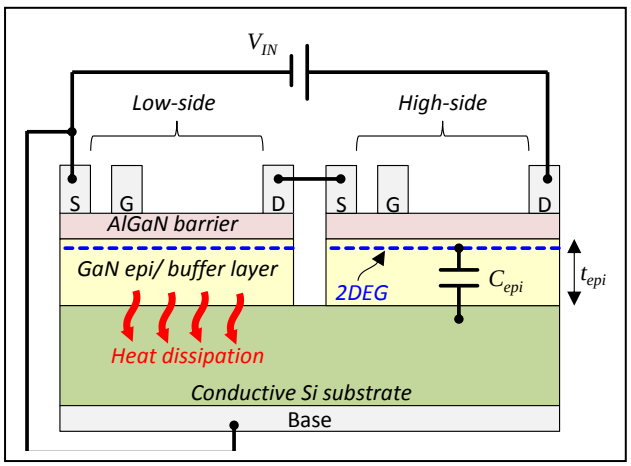


**Figure 1.** Schematic cross section of monolithic half-bridge circuit on conductive Si substrate.

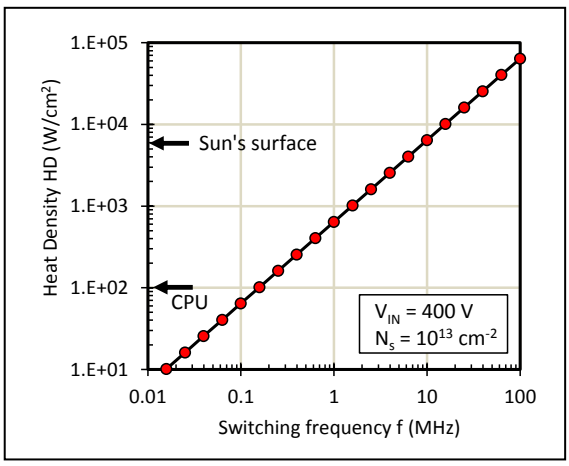


**Figure 2.** Calculated heat densities of GaN chip depending on output frequency under hard switching condition.

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# 14 - GaN CMOS: fact or fiction?

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**Status**

GaN power transistors have demonstrated unprecedented switching speed [1]. At high switching speed, parasitic inductance in the power loop as well as in the drive loop causes large voltage overshoot [2]. In current practice, the GaN switch is often intentionally slowed down to avoid catastrophic failure and additional power consumption induced by the voltage overshoot [3]. To take full advantage of the high-speed GaN switch, one need to eliminate the parasitic inductance by monolithically integrating power switches and their gate drivers. The gate driver typically uses a Totem-Pole topology with a pair of complementary N-type and P-type transistors. The complementary transistors eliminate static power consumption. GaN CMOS technology is needed to realize monolithic GaN power IC integrating high-voltage GaN transistors with low-voltage N- and P-type GaN transistors on the same chip.

The monolithic GaN power IC, as shown in Figure 1, minimizes interconnect parasitic between power switches and gate drives. Reduction of interconnect parasitic enables efficient power switching at high frequencies. At high frequencies, the size of passive components can be drastically reduced. Reduction of interconnect parasitic also enables active control of switching trajectory with minimal time delay. Active control of switching trajectory mitigates device stress and improves the reliability. The monolithic GaN power IC enables modular architecture where a number of power switching unit cells, e.g. half bridge, can be stacked in parallel and in series to scale the current and voltage handling capability. The monolithic GaN power IC enables cost reduction by cutting the assembly and packaging cost, as well as by using the modular architecture consisting of standardized switching unit cells.

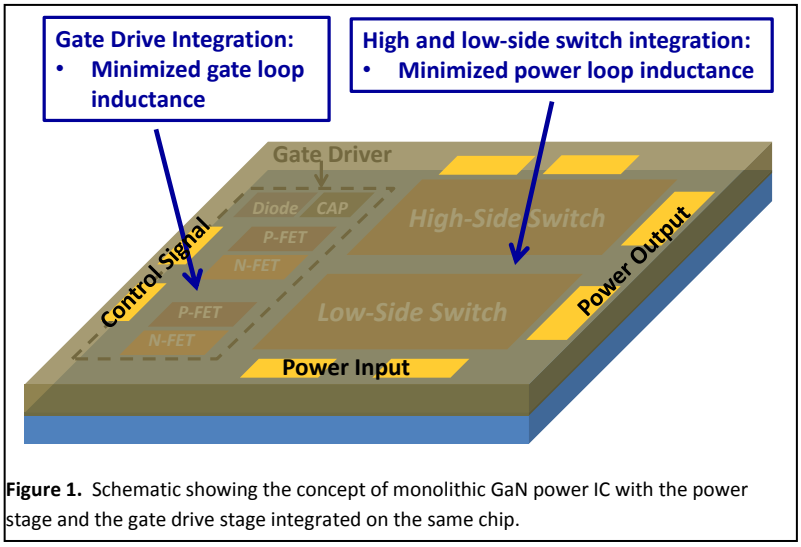


**Figure 1.** Schematic showing the concept of monolithic GaN power IC with the power stage and the gate drive stage integrated on the same chip.

**Current and Future Challenges**

N-type GaN high- and low-voltage transistors are readily available. Difficulty in making P-type GaN transistor and integrating it with the N-type transistor has been the major obstacle for realizing the GaN CMOS technology. There have been a few early studies on P-type GaN transistors [4]–[7], an attempt to integrate P- and N-type Schottky gate GaN transistors [8], and lately a demonstration of a working GaN CMOS IC inverter [9]. The GaN CMOS demonstration was achieved through selective area regrowth of P-type GaN transistor structure on a wafer with N-type GaN transistor epitaxy structure. Significant improvement of the GaN CMOS technology is needed to meet the performance requirement of the monolithic power IC. Specifically, there are two major challenges to be addressed. One challenge is the low output current, or high on-resistance, of the P-type transistor. The other challenge is the off-state leakage current of the P-type transistor when integrated with the N-type transistor. The low output current results from poor hole mobility, low mobile hole concentration, and

poor ohmic contacts. The off-state leakage is attributed to impurity contamination at the regrowth interface.

**Advances in Science and Technology to Meet Challenges**

Figure 2 shows device structure, IV curves, and on-resistance component breakdown of a P-type GaN transistor reported in Ref. 9. Inefficient P-type doping is the primary challenge responsible for the low current and the high on-resistance. Mg, with an activation energy as high as 0.2 eV in GaN, is used as the acceptor. High dopant activation energy leads to low concentration of mobile holes even at high doping level, therefore high contact resistance and high access resistance. Advance in P-type doping technique, e.g. polarization-assisted doping [10], has the potential of overcoming the doping challenge. Low hole mobility is another important factor responsible for the high on-resistance. Low hole mobility is caused by severe impurity scattering, interface scattering under the gate insulator, and large hole effective mass. In addition to enhancing doping efficiency, improvement of insulator-semiconductor interface is important for achieving better hole mobility and lower channel resistance. Strain engineering may increase the population of light holes, thereby improving the hole mobility. In addition to improving hole density and mobility, reducing or eliminating the spacings between gate and source/drain electrodes can effectively improve the on-resistance.

Improvement of epitaxy regrowth process is needed to eliminate the off-state leakage current shown in Figure 2. P-type transistors fabricated on P-type only wafers didn't show this off-state leakage. The off-state leakage is attributed to Si contamination commonly observed at the regrowth interface. The source of the Si contamination can be volatile organic silicon compound in the air ambient. A regrowth process avoiding such contamination is needed to integrate high-performance P- and N-type transistors.

Comprehensive study of gate dielectric in P-type transistors is also needed to ensure stable threshold voltage, and facilitate scaling to smaller gate lengths.

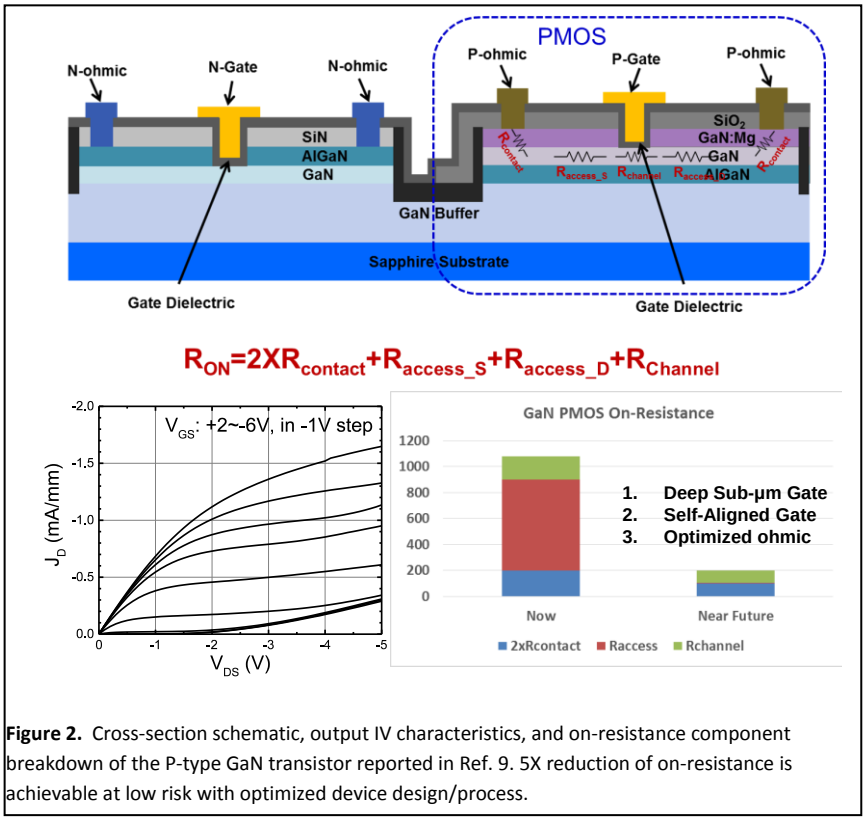


**Figure 2.** Cross-section schematic, output IV characteristics, and on-resistance component breakdown of the P-type GaN transistor reported in Ref. 9. 5X reduction of on-resistance is achievable at low risk with optimized device design/process.

**Concluding Remarks**

Monolithic power IC based on the GaN CMOS technology is essential for realizing and maximizing the performance/cost potential of GaN power electronics. Early work on GaN N/P-type transistors and GaN CMOS technology has proved that the GaN CMOS is a fact, not a fiction. Improvement of P-type doping and selective area regrowth is important for realizing high-performance GaN CMOS technology for monolithic power IC applications.

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# 15 - Assessing the limits of performance of p-type devices in GaN

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**Status**

P-type devices are required for integration of CMOS gate drivers and power devices to enable high frequency, high efficiency convertor systems on a chip in GaN. A D-mode p-channel HFET in GaN, utilising a low density (1x $10^{11}$ $cm^2$) polarization induced two dimensional hole gas (2DHG) as carrier was first demonstrated by T. Zimmermann *et. al* in 2004 [1]. It is more difficult to realise a normally-off (E-mode) operation, with negative threshold voltage $V_{th}$, since the 2DHG under the gate has to be depleted at zero gate bias. A recessed gate [2], and/or reduction of polarization charge via adjustment of the mole fractions [3] have been amongst techniques explored for E-mode operation, following logically from similar progression in n-type devices in GaN. However, these techniques are not easily transferrable, primarily because unlike a 2DEG in GaN, achieving a high density 2DHG is a challenge, and reported mobility of holes in a 2DHG, ranges no more than 6-43 $cm^2/Vs$ at room temperature [1,3].

**Current and Future Challenges**

The main challenge for a p-type MOSHFET in GaN is achieving a high threshold voltage $|V_{th}|$ to prevent false turn-on in PMIC applications, while maintaining a high $|I_{ON}|$ and $|I_{ON}/I_{OFF}|$ ratio. Achieving a $|V_{th}|$ of $|-2.0|$ $V$ is not feasible by etching alone, as it requires the thicknesses of the oxide and GaN channel layer to be reduced to undesirably small values ($\sim 5$ $nm$) [4]. On the other hand, achieving an E-mode operation by reducing the polarization charge via a reduction in the Al mole fraction leads to reduction in the density of both 2DHG and 2DEG, not only reducing the $|I_{ON}|$ in p-type devices but also deteriorating the performance of n-type devices on the same platform. Figures 1 (a) & (b) depict the on-current $|I_{ON}|$ and on-off current ratio $|I_{ON}/I_{OFF}|$ with threshold voltage $V_{th}$ of experimental p-channel HFETs reported in [2,3,5–7], highlighting the degradation of $|I_{ON}|$ as the device turns from D-mode to E-mode while $|I_{ON}/I_{OFF}|$ ratios improve with increasingly negative $|V_{th}|$. Except for the work of R. Chu [5] and G. Li *et. al* [7], which do not include an underlying 2DEG beneath the 2DHG, the activities can be summarised into two main barrier-layer platforms, ternary AlGaN and quaternary InAlGaN, both of which possess an inherent polarisation superjunction [8] that is eminently useful for management of the peak electric field distribution and reliability of GaN power devices. The best performing E-mode p-type device by gate recess so far, reported by Hahn *et. al* [3], resulted in an on-current $|I_{ON}|$ of $\sim 9$ $mA/mm$ at a $V_{th}$ of $-1.3$ $V$ and an on/off current ratio of $\sim 10^7$. In quaternary barriers, increasing the Al mole fraction leads to an increase in negative polarization charge, higher bandgap, and a smaller lattice constant, while increasing the In mole fraction has the opposite effect. Hence, by adjusting both Al and In mole

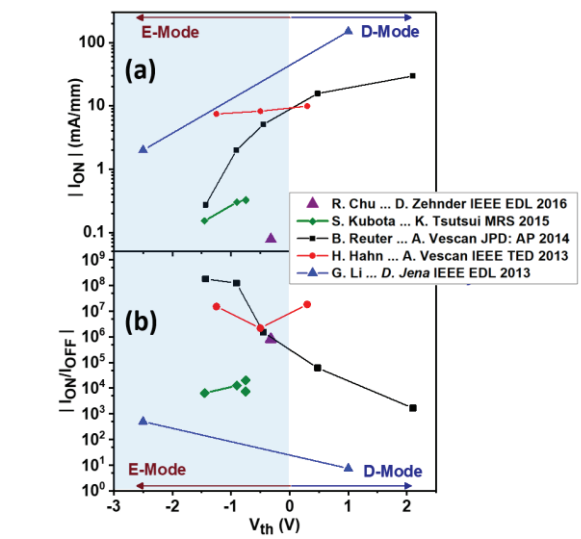


Figure 1. (a) on-current vs. threshold voltage, and (b) on-off current ratio vs. threshold voltage characteristics of the state-of-the-art p-channel HFETs reported to date.

fractions simultaneously, it is possible to tune the polarization and the bandgap of the barrier layer, independently, to some extent.

**Advances in Science and Technology to Meet Challenges**

A higher $|I_{ON}|$ requires a high density of 2DHG, nevertheless, for an overall lower parasitic resistance, as well as high on/off current ratio, requires a localised depletion of the 2DHG under the gate, so as to not affect the access regions. This can be achieved via an AlGaN cap between the oxide and GaN channel layers [9], where the barrier separating the 2DHG from the 2DEG can be either AlGaN or InAlGaN. As shown previously, for the device in Figure 2 (a), the additional polarisation charge introduced by the AlGaN cap not only depletes the 2DHG under the gate, but also minimises the trade-off between $|I_{ON}|$ and $|V_{th}|$ [4]. However, this approach demands a selective epitaxial regrowth of the AlGaN cap layer. Figure 2 (b) shows an alternate heterostructure, where in addition to the recessed gate, the 2DEG is biased via an additional base contact [6], thus acting as a secondary gate for the 2DHG. By applying a positive bias to the base contact $V_B$, the density of 2DHG can be reduced locally, without affecting other devices on the platform. In both the device structures (Figures 2 (a) & (b)), a 2DEG lying parallel beneath the 2DHG separated by an AlGaN/InAlGaN barrier contributes an additional parasitic capacitance which can be offset by increasing the barrier thickness.

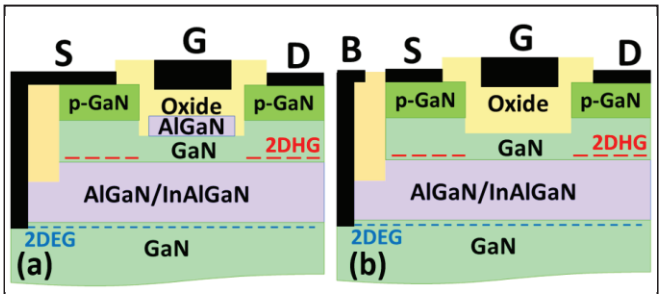


Figure 2. Schematic of p-type MOSHFETs with (a) an AlGaN cap and (b) a bias applied to the 2DEG.

Advancements in the growth of gate oxide are necessary to control and lower the impact of trap states at the oxide/AlGaN cap and oxide/GaN interfaces while at the same time lower the gate leakage current, for a reliable and replicable operation of these devices. The MOCVD growth of Mg doped p-GaN layer currently suffers from, large activation energy $(120 - 200\, meV)$ of Mg dopants and memory effect [10], which leads to poor hole density in p-GaN and a broader doping profile. Moreover, during the epitaxial growth at high temperature, Mg ions can diffuse into the GaN layer underneath, thus contributing to the leakage current and affecting the minimum channel thickness that can be achieved in manufacture. Therefore, novel doping techniques are required to obtain p-GaN layers with high hole density and sharper doping profile.

Other possibilities to boost the performance of p-type devices in GaN include, improving the hole mobility by tailoring the valence band structure in GaN, for example by the application of stress to lower the effective mass of holes or introduction of positive ions directly in the gate oxide to deplete the hole gas underneath.

**Concluding Remarks**

P-type devices in GaN are necessary in the long run to harness the full potential that GaN technology has to offer in achieving high efficiency power conversion. Despite the poor mobility of holes and challenges associated with Mg dopant, techniques to circumvent or limit their impact exist, although still in their infancy. More work is required for demonstrating their reliable operation and manufacturability at low cost.

**Acknowledgements**

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# 16 - 600V E-mode GaN Power Transistor Technology: Achievements & Challenges

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**Status**

Since the first confirmation of a 2DEG at the AlGaN/GaN interface in 1992 and the first availability of GaN-on-SiC radio frequency power transistors in 1998, nitride semiconductor hetero structure electron devices now constitute a hundred million dollar market for RF power. As regards power conversion applications, GaN-on-Si high voltage power transistors have been in development stage for the past decade with initial focus on depletion mode devices due to the inherent nature of the 2DEG. However most power electronic applications demand for enhancement mode devices. The first high voltage solution released to market in 2015 by TransPhorm [1] is based on a cascode configuration of a low voltage Si-MOSFET in series connection with a high voltage GaN MIS-HEMT to solve that issue. Following the progress of enhancement mode devices based on a p doped GaN gate module for low voltage GaN power transistors from EPC [2] we now see the first fully industrial qualified 600V true enhancement mode (E-mode) GaN power transistors on the market from Panasonic and Infineon [3-5]. These E-mode GaN power transistors are based on a fully recessed gate module with subsequent regrowth of a second AlGaN barrier with pGaN (see Fig. 1) on top for an excellent control of the threshold voltage independent of the drift layer carrier density [6]. pGaN is also used at the drain region as drain extension which improves the dynamic on state resistance to well below 10% even at high temperatures of 150°C and full rated drain voltage of 600V down with delay times as short as few hundreds of ns from blocking mode to settled on state resistance measurement. At the same time this drain sided pGaN region (see Fig. 1) also improves the robustness of the device to the required levels for hard switching applications [3]. The devices are offered in surface mount device packages allowing for designs with low loop inductances including top side cooled variants for enabling 3kW converters without need for paralleled devices (see Fig. 1). Recently it has been demonstrated that the gate module even allows for a >10µs short circuit robustness at full bus voltage of 400V when driven properly [7]. The technology has been implemented in a volume silicon power fab with a very high degree of equipment sharing with standard silicon processes to achieve economy of scale.

When comparing Infineon's CoolGaN™ technology to the state-of-the-art silicon super junction devices (Si SJ) as well as other wide band gap technologies on the market (see Table I) we see that all WBG technologies offer roughly the same order of magnitude improvement in output charge $Q_{OSS}$ per $R_{DSON}$ and two orders of magnitude improvement in reverse recovery charge per $R_{DSON}$. However, only E-mode GaN offers at the same time one order of magnitude of gate charge $Q_G$ improvement which makes it the perfect device for high frequency resonant switching. Resonant converters with 3kW power level operating at 350kHz without sacrificing peak efficiency of 98.4% demonstrate high density of 170W/in³ [8]. For hard switching applications the relevant figure-of-merit is the energy stored in the output capacitance ($E_{oss}$) and here recent developments in Si SJ devices have raised the bar significantly so that as of today only E-mode GaN can outperform Si. In combination with the lack of reverse recovery charge that enables the use of GaN devices in half bridge configurations new and simpler topologies like full bridge totem pole are possible.

| Device | Rating [V] | $R_{DSON}$ [mOhm] | $R_{DSON}*Q_{OSS}$ [mΩμC] | $R_{DSON}*Q_{RR}$ [mΩμC] | $R_{DSON}*E_{OSS}$ [mOhm*uJ] | $R_{DSON}*Q_G$ [mΩnC] |
|---|---|---|---|---|---|---|
| Si Super Junction [a] | 600 | 56 | 23.5 | 336 | 450 | 3800 |
| **GaN eMode** [b] | 600 | 55 | **2.2** | **0** | **350** | **320** |
| GaN Cascode [c] | 600 | 52 | 3.8 | 7.1 | 730 | 1460 |
| GaN Direct Drive [d] | 600 | 70 | 4.1 | **0** | 530 | n.a. |
| SiC DMOS [e] | 900 | 65 | 4.5 | 8.5 | 570 | 1950 |
| SiC TMOS [f] | 650 | 60 | 3.8 | 3.3 | 540 | 3480 |

**Table 1.** Benchmark of State-of-the-Art High Voltage Power Transistors: a) Infineon CoolMOS™ IPL60R065C7 Datasheet, b) Infineon CoolGaN™ Preliminary Datasheet ($Q_{RR}$ is exclusive of $Q_{OSS}$), c) TransPhorm Cascode TPH3205WS Datasheet, d) TI Direct Drive LMG3410 Datasheet, e) Wolfspeed C3M0065090J Datasheet, f) Rohm SCT3060AL Datasheet (all values given typical at 25°C incl. package).

*Current and Future Challenges.* One of the biggest challenges to release power GaN devices to the market has for sure been their reliability. The hetero epitaxial growth of the GaN buffer on silicon wafers unavoidably leads to lattice misfit dislocations and other growth defects. At the same time present lateral GaN devices differ from the established silicon power devices in many aspects as they are based on hetero junctions, differences in spontaneous polarizations and bulk/surface donors to generate the 2DEG instead of p and n dopings. The qualification of those devices therefore cannot solely rely on established silicon procedures (e.g. according to JEDEC Solid State Technology Association, former Joint Electron Device Engineering Council) but must take into consideration the new possible failure modes and physics together with the corresponding lifetime models and application profiles to determine appropriate qualification tests and durations. It is also essential to derive appropriate screening tests based on intrinsic and extrinsic lifetime models to achieve the needed low field failure rates of 1 fit or less. Passing all those qualification procedures still does not guarantee stable long term behaviour in the application. Long term testing of the devices under real application conditions with no fails is a first necessary step, but only application testing with accelerated conditions (e.g. higher temperatures, bus voltages, peak currents) and testing to failure allows extraction of life time models and hence failure rates in real life [9]. As a joint effort by the major semiconductor companies involved in GaN, a working group for the standardization of GaN qualification under the framework of JEDEC has been recently established to address many of the before mentioned aspects [10].

**Advances in Science and Technology to Meet Challenges**

For further advancing the reliability of GaN devices it is important to further deepen the understanding of defects and their relation to device behaviour and device reliability. This comprises e.g. the understanding of point defects including their electronic structure mainly in the various parts of the AlN/AlGaN/GaN buffer, channel and barrier layers and how those defects are influenced by the growth conditions of the material and the selection of possible advanced substrates. In order to possibly achieve future enhancement mode devices based on MIS gate structures with low leakage currents and a wide range of threshold voltages and gate drive voltages a big step in understanding on how to reduce the interface defect density of gate dielectrics on top of GaN and how to improve channel mobility is needed.

An important mid to long term challenge for GaN technology to enable broader market penetration is approaching cost parity per same $R_{DSON}$ compared to silicon devices like CoolMOS™.

This will be driven on the one hand side by reducing the cost per die area through increasing economy of scale and increased yield with rising volume and the introduction of 200mm wafer diameter for GaN-on-Si during the next few years as well as the step to 300mm within the next decade. On the other hand we will see further die shrinks through better exploration of the material limits e.g. by increased material quality allowing for shorter drift regions through higher electric fields as well as advanced drift region engineering (improved field plates, graded 2DEG density, etc.) allowing for higher carrier densities without compromising reliability.

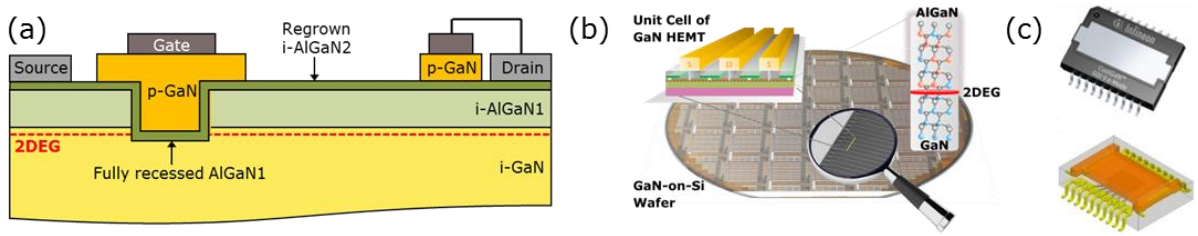


Figure 1. a) 600V E-mode GaN cell concept with through recessed first AlGaN barrier and regrown thin second AlGaN barrier with pGaN enhancement mode gate, b) GaN-on-Si wafer with enlarged unit cell and schematic of AlGaN/GaN hetero junction forming the 2DEG, c) top side cooled SMD package: top view and schematic with wire bonds

**Concluding Remarks**.

After GaN-on-SiC RF power devices have reached a multi hundred million dollar market volume, and after a decade of intense research and development of GaN-on-Si power technology, fully industrial qualified 600V true enhancement mode GaN power devices are finally entering the market. Qualification procedures and screening methods have been established according to the needs of the new material system and taking into consideration typical industrial application profiles targeting field failure rates below 1 fit. The new devices offer customers the degree of freedom to either boost the power conversion efficiency to unprecedented levels of 99% and beyond or to significantly increase the power density of their converters without compromising the efficiency.

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# 17 - Potential of GaN Integrated Cascode Transistors

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**Status**

AlGaN/GaN high electron mobility transistors (HEMTs) are poised to replace Si MOSFETs for high frequency power switching applications up to 600 V. Enhancement mode (E-mode) operation with a positive threshold voltage ($V_{TH}$) $\geq$ 3 V is desirable for circuitry protection and safety purposes but GaN HEMTs are naturally depletion mode (D-mode) devices. Cascode devices with low voltage E-mode Si MOSFETs and high voltage D-mode GaN HEMTs offer an excellent solution to the E-mode operation issue using existing gate drivers. In addition, the cascode structure can lead to improved switching speed and reduced switching losses compared to an equivalent discrete transistor [1]. Here, we discuss the challenges faced by cascode devices as well as the potential of integrated cascode structures to achieve high switching frequency.

**Current and Future Challenges**

Despite the promising performance of commercial 600 V hybrid GaN plus Si cascode transistors [2], several issues hinder their switching performance. Firstly, additional package connections in the hybrid cascode lead to increased parasitic inductances which can cause excessive ringing and limit the operating frequency [3]. This presents major challenges to packaging design. In addition, the intrinsic capacitance mismatch between the Si and GaN transistors and the body diode in the Si MOSFET can result in additional switching losses when the Si device is driven into avalanche mode during turn-off [4].

Monolithically integration of E-mode and D-mode GaN devices in the cascode configuration, on the other hand, will mitigate the parasitic inductances and the 'slower' Si device issues in the hybrid GaN plus Si cascode devices. However, $V_{TH}$ of the reported E-mode GaN devices using various techniques such as fluorine (F) treatment on the barrier under the gate [5], GaN MOSFETs [6] and p-AlGaN gate [7] remains low, typically less than 2 V. This presents an issue for gate driving as un-intended turn-on may occur with a voltage ringing effect as a result of CdV/dt coupling from the drain to the gate.

**Advances in Science and Technology to Meet Challenges**

The switching losses in a field effect transistor are partly determined by the current through the resistive loss-generating channel during the charging/discharging processes [8] and hence depend on the speed of charging and discharging the Miller capacitance (Miller effect) at high voltages. The latter depends on the load current-to-gate drive current ratio. On the other hand, the discharging of the charge stored in the output capacitance of the cascode device is not limited by the gate drive current during turn-on as shown in Figure 1(a). During turn-off, the cascode connection utilises the load current to charge the output capacitance and a faster turn-off time can be achieved for the same gate drive capability. The GaN-based integrated cascode transistor is an excellent candidate to exploit these switching advantages without the additional parasitic inductance. In our recent work using F treatment technology to achieve E-mode in the integrated cascode GaN transistor ($V_{TH}$ = +2 V) (Figure 2), we demonstrated a reduction in turn-on and turn-off energy losses of 21 % and 35 %,

respectively in comparison to a discrete GaN E-mode transistor under 200 V hard switching conditions [9]. The immediate challenge is to achieve a reliable E-mode technology with $V_{TH}$ greater than +2 V.

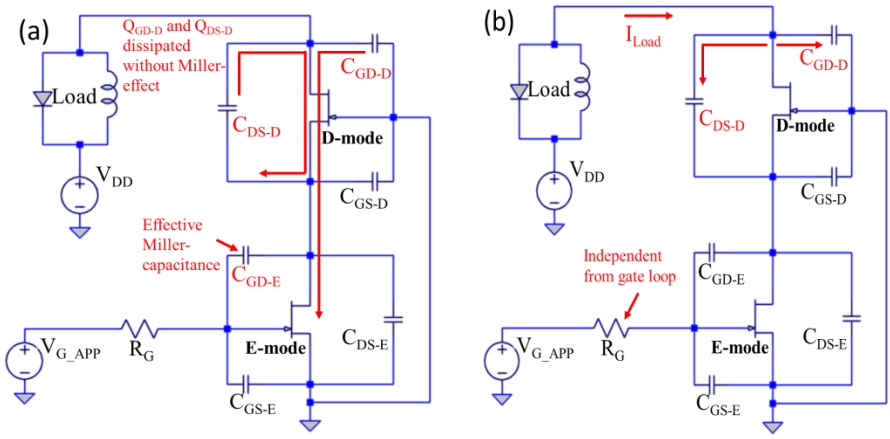


Figure 1. Charging and discharging paths of the output capacitance in the cascode device during (a) turn-on and (b) turn-off processes.

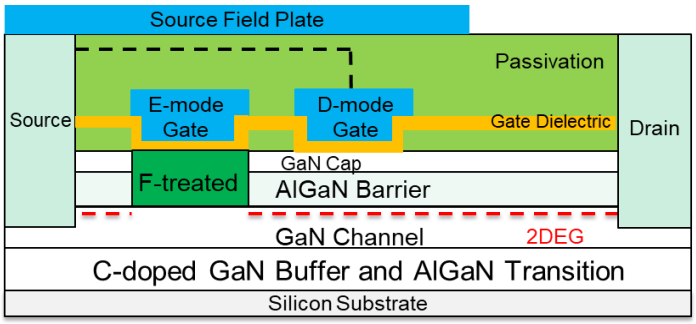


Figure 2: Device structure of GaN integrated cascode transistors.

Matching of intrinsic capacitances between E-mode and D-mode devices in the cascode connection is critical to control the off-state operating voltage of the E-mode device. For hybrid cascodes, adding an external capacitor in parallel with drain-source of E-mode Si MOSFETs has been proposed to provide this matching and prevent the Si device running into avalanche [4], but at the expense of additional package inductances. For GaN integrated cascode transistors, different field plate structures in E-mode and D-mode devices can be employed to achieve capacitance matching. In addition, with the lack of a body diode in the low voltage GaN E-mode device, the integrated cascode devices have the option to trade the off-state operating voltage of the E-mode part for a faster switching speed, without the avalanche loss.

## Concluding Remarks

Monolithically integrated GaN cascode HEMTs open up new opportunities to achieve high efficiency power devices in the MHz range. It is however necessary to overcome both problems with the magnitude of $V_{TH}$ of the E-mode and the mismatch of D-mode and E-mode devices to realise the full potential of integrated GaN cascode HEMTs.

## Acknowledgements

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# 18 - Converter Topologies in GaN

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**Status**

The commercialization of 600V GaN power devices, including the cascode-based FETs and the enhancement mode FETs, has enabled large scale R&D effort in academia and industry [1] to evaluate the impact on converter design and performance. Compared with the best 600V Si super-junction (SJ) MOSFET, the input figure of merit ($R_{on}$·$C_{iss}$) of 600V GaN FET has been improved by about 20 times, the output figure of merit ($R_{on}$·$C_{oss}$) has been improved by about 5 times while the reverse recovery figure of merit ($R_{on}$·$Q_{rr}$) has been improved by more than 40 times [1]. These revolutionary improvements make GaN devices ideal for high efficiency and high density power supply design, especially for applications where the DC link voltage is around 400V. Many converter topologies exist that can take advantages of the improved device performance by directly replacing Si SJ MOSFETs with GaN FETs, operating at the same switching frequency or at an increased frequency. Example topologies include the active-clamped flyback converter (Fig. 1 (a)) for universal AC/DC adapter which can use GaN devices in the primary side [2]; the soft-switched isolated DC/DC converters, such as LLC resonant converter, Phase-Shift-Full-Bridge (PSFB), Dual-Active-Bridge (DAB), etc., which use the GaN devices in the primary side or both sides [3]. Many designs explore the ability to push the switching frequency to much higher value than the Si-based ones, achieving ultra-high efficiency and density. Some topologies are rarely used in the past, limited by the severe reverse recovery issue such as large $Q_{rr}$ and high recovery di/dt in the Si SJ MOSFET. However, by using the GaN devices where the reverse recovery $Q_{rr}$ is pretty much zero due to the absence of any minority carrier injection, some of these topologies become feasible and have demonstrated extraordinary performance. Examples include the 99% efficient totem-pole PFC (Fig. 1 (b)), full-bridge (FB) photovoltaic (PV) inverter (Fig. 1 (c)) and the 98.8% efficient hard-switching isolated full-bridge converter [4-7]. In addition to the circuits, improved modulations also make the same topologies perform even better. The continuous conduction mode (CCM) totem-pole power factor corrector(PFC) and FB PV inverter work with hard switching and constant frequency, typically only in the range of 50~100kHz. However, the triangular current mode (TCM) totem-pole PFC and FB PV inverter can work with soft switching and variable frequency in the range of 100 kHz~3MHz [4, 5, 7]. With these GaN-based topologies, the efficiency and the power density are significantly improved compared with the Si-based solutions.

**Current and Future Challenges**

The main challenges for the GaN based converter topologies are:

1. The optimization of the switching frequency: The switching frequency determines the frequency related loss and the size of the passive components. The optimization of the switching frequency is an important research topic.

2. Selection between hard switching and soft switching: Constant frequency hard switching modulation has low control complexity and high reliability, while the size of the passive components is large. Variable frequency soft switching techniques can reduce the size of the passive components due to the high frequency. However, the control complexity is significantly increased due to the variable frequency operation. The selection between hard switching and soft switching is a challenge.

3. The reduction of the differential mode (DM) filter size for soft-switched topologies: Soft-switched topologies, such as the TCM totem-pole PFC and the TCM inverter, have large input current ripples. It is still challenging to dramatically reduce the DM filter size even the frequency is high.
4. New converter topologies in GaN: To take full advantage of the GaN device, developing new topologies and new power delivery architecture is a needed new challenge

**Advances in Science and Technology to Meet Challenges**

The progresses in addressing and investigating the previously mentioned challenges are:
1. The optimization of the switching frequency: The optimization of the switching frequency depends on the requirements of the application. For applications focusing on the high efficiency, lower frequency is preferred. For the applications requiring high density, such as the Google Little Box challenge, higher frequency is preferred.
2. Selection between hard switching and soft switching: Due to the elimination of the turn on loss, the zero-voltage-switching (ZVS) converters can realize high switching frequency. Thus, the size of all the passive components, especially the EMI filters, can be reduced. In addition, the slower dv/dt of the ZVS converters also reduce the EMI noises. The soft-switched converters have demonstrated ultra-high density, over 145W/inch$^3$, on the totem-pole PFC and FB PV inverter [4, 5, 7].
3. The reduction of the DM filter size for soft-switched topologies: Multiphase interleaved soft-switched topologies (Fig. 1 (d)) can solve this challenge [8]. The interleaving technologies significantly reduce the current ripples. The DM filter size is optimized, too.
4. New converter topologies in GaN: The upcoming GaN-based AC switch could enable a number of new high-performance topologies. The resonant converter with GaN AC switch (Fig. 1 (e)) not only realizes high efficiency, but also achieves the wide input and wide output voltage conversion [9]. A new single stage solution, the isolated AC/DC DAB converter with GaN AC switches (Fig. 1 (f)) on the primary side, can be used for on-board charger and battery system with significantly improving the system efficiency [10].

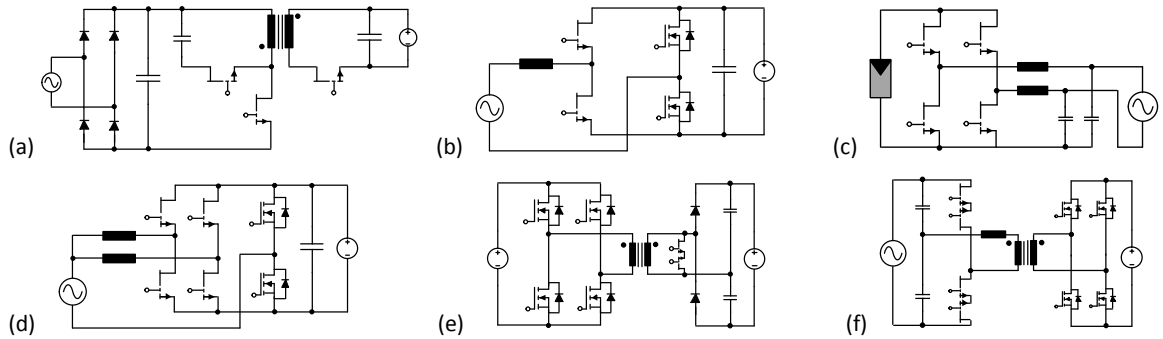


**Fig. 1.** Topologies discussed previously with GaN FETs: (a) active clamped flyback; (b) totem-pole PFC; (c) FB PV inverter; (d) two-phase interleaved totem-pole PFC; (e) resonant converter with GaN-AC switch at the secondary side; (f) AC/DC DAB with GaN AC switches

| | Frequency | Efficiency | Power density |
|---|---|---|---|
| 65W active-clamp Flyback Charger [2] | 1MHz | 93.0% (full load) | 25W/inch$^3$ |
| 2.4kW FB isolated DC/DC [6] | 50kHz | 98.6% (full load) | 116W/inch$^3$ |
| 1kW TCM two-phase totem-pole PFC [4] | 4MHz (max) | 98.7% (full load) | 220W/inch$^3$ (no bulky capacitors) |
| 2kW multiphase TCM FB PV inverter [7] | 35~240kHz | 95.4% (CEC) | 150W/inch$^3$ |

Table 1. Benchmark of the state of the art GaN-based converters

**Concluding Remarks**

The GaN-based converters have demonstrated extraordinary performance. As shown in Table 1, the power density and the efficiency have been improved significantly based on these benchmark GaN

converters. With the innovation and the optimization of the converter topologies in GaN, the density and efficiency will be further improved. Even though the cost of the devices is increased, the high density and efficiency will reduce the system cost in the future.

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# 19 – Fast switching with GaN and dynamic on-resistance from application view-point

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**Status**

GaN semiconductors have gained popularity in GHz applications, while power electronic applications are still in the early stages of development. The focus of this section is the application of GaN devices for power electronics with device breakdown voltages from 400V up to 900V. Applications of GaN transistors include uni- and bidirectional DC/DC and AC/DC converters, inverters for high-speed motor drives as well as inductive heating and wireless power transmission (Fig. 1). High system efficiencies and power densities are the main requirements for these applications. This is enabled by low conduction and low switching losses from a semiconductor point of view. GaN transistors allow both aspects. Low conduction losses are achieved by GaN transistors with low area-related on-resistance compared to Silicon (Si) and Silicon Carbide (SiC) counterparts. Low switching losses are achieved by fast switching between the on- and off state. GaN transistors show a purely capacitive behaviour due to their unipolar device characteristic, while Si- and SiC-MOSFETs lack from reverse recovery charge due to intrinsic bipolar body diodes [1]. Regarding the switching speed of the drain-source-voltage, 5-20 V/ns is considered as "fast" for Si devices. Slew rates are typically limited to the range of 1-16 V/ns in motor drive applications [2]. In contrast, optimized SiC and GaN circuits allow up to 200 V/ns and 500 V/ns, respectively [3,4]. The possibility of ultra-fast switching exceeds the boundary conditions of most applications. However, operating two 600V transistors in half-bridge configuration for e.g. hard-switching bidirectional DC/DC converters, Si-MOSFETs are not suitable due to their bipolar body diode. SiC-MOSFETs with orders of magnitude lower reverse recovery charge are suitable, but higher system efficiency can be achieved with unipolar GaN-transistors.

**Current and Future Challenges**

The main challenges for GaN transistors in power electronic applications are:

1. Normally-off characteristic: System developers require normally-off devices because of safety reasons, while the realization of normally-off device characteristics is still a main research topic (section 8).
2. Dynamic on-resistance: Some GaN transistors show dynamic on-resistance. After turn-on, their on-resistance $r_{ds,on}$ is higher than the static value $R_{ds,on,typ}$ and decays over time until it reaches the static value $R_{ds,on,typ}$. The main reason is a physical phenomenon called "trapping" due to high electric-field strengths in the off-state, when the blocking voltage is applied (drain-source-voltage is e.g. 400V) [5,6]. Fig. 2 shows a comparison of three devices from different manufacturers. GaN #1 shows the highest dynamic on-resistance with a ratio of $r_{ds,on}$ ($t_1$)/ $R_{ds,on,typ}$ = 4.3 while it decreases to 2.5 after 300 µs. For example, the turn on time of a DC/DC converter operating at a moderate switching frequency of 100 kHz and a duty cycle of 50 % is only 5 µs. This results in an effective on-resistance of 4.2·$R_{ds,on,typ}$ for the system design and therefore in higher losses and lower efficiency. The influence of this issue becomes even worse when the switching frequency is increased.

3. Reverse conduction capability: In half-bridge configuration, reverse conduction capability is required for negative drain currents. Though there is no intrinsic body-diode in GaN transistors, current can flow from source to drain. However, the source-drain-voltage drop $v_{sd}$ increases with decreasing gate-source-voltage $v_{gs}$. This is valid for all commercially GaN transistors known to the authors. For example, for some GaN transistors, the forward voltage drop $v_{sd}$ is 8 V or higher, when the gate is kept in the off state with $v_{gs}$ = -5 V.
4. Parasitics, packaging, controllability and EMI: In general, the influence of parasitic inductances and capacitances is the same as with Si and SiC circuits. This situation worsens for GaN transistors due to tighter gate voltage margins compared to Si and SiC devices which can lead to device destruction and phase leg short circuits. In general, fast switching semiconductors enable higher power densities, but require additional filters for electromagnetic interference (EMI), also.
5. Reliability issues and countermeasures are discussed in section 8.

**Advances in Science and Technology to Meet Challenges**

The progresses in addressing and investigating the challenges from the preceding subsection are:

1. Normally-off characteristic: This challenge must be solved at the level of the device technology. Alternatively, a cascode circuit with normally-off behaviour can be realized by using a normally-on high-voltage GaN transistor and a normally-off low-voltage Si transistor. However, recent studies have shown that the switching speed of cascodes is barely adjustable without additional components inside the cascode [7]. The necessity of an additional Si transistor for the cascode is another disadvantage of the cascode compared to normally-off GaN transistors. All commercial GaN transistors at the time of this study show normally-off behaviour by intrinsic normally-off characteristic or cascode configuration.
2. Dynamic on-resistance: As can be seen in Fig. 2, the GaN transistor #3 shows no dynamic on-resistance for the full time scale. The manufacturer applies an additional p-GaN-layer to provide the injection of holes from the drain and dynamic on-resistance can be prevented successfully [8]. However, other manufacturers still face the challenge of the dynamic on-resistance which is also indicated by significantly increased scientific activities regarding this topic.
3. Reverse conduction capability: The high forward voltage drop in reverse conduction mode of GaN transistors can be avoided by using synchronous rectification. This means to turn the GaN transistor on shortly after the current has commutated to the transistor in reverse direction. In contrast to a diode, the transistor has to be turned off before the complementary transistor of the half-bridge turns on. Otherwise, phase leg short circuits may occur which lead to immediate destruction of both switches. In this case, special protection circuits are necessary. Additionally, the adaption of the dead-time between the half-bridge switching actions helps to increase the efficiency even more.
4. Parasitics, packaging, controllability and EMI: Integration of GaN transistors and gate drivers within one package will minimize the effects of parasitic circuit elements. The next step is to integrate GaN transistors and drivers within one chip which has already been demonstrated. To gain the most advantage for power electronic systems, the integration of GaN transistor, gate drivers, auxiliary circuits and DC link filters within one device will allow minimum parasitic

circuit inductance and high switching speeds. The EMI can also be improved by the enclosure on low footprint as well as novel active filters.

**Concluding Remarks**

GaN transistors have evolved dramatically in the last ten years and enable power electronic systems with highest efficiencies due to their unipolar device characteristic and low area-specific on-resistance (Fig. 2). The issues discussed in this section will diminish with further research similar to the advances with Si and SiC devices in the last 70 and 20 years, respectively.

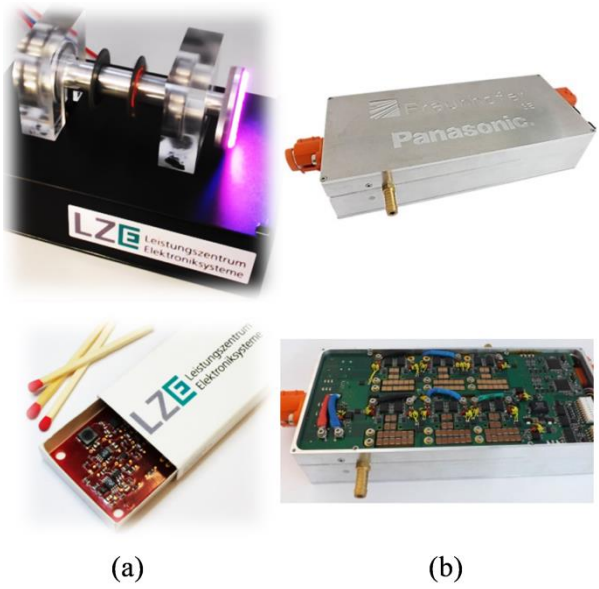


**Figure 1**. (a) Demonstrator of 20 W inductive power transmission for high-speed rotating applications (top) and corresponding matchbox-sized GaN power electronics (bottom) [9]. (b) Demonstrator of 6 kW on-board charger for electric vehicles with 3 kW/l power density (top) and power electronics setup (bottom) [10].

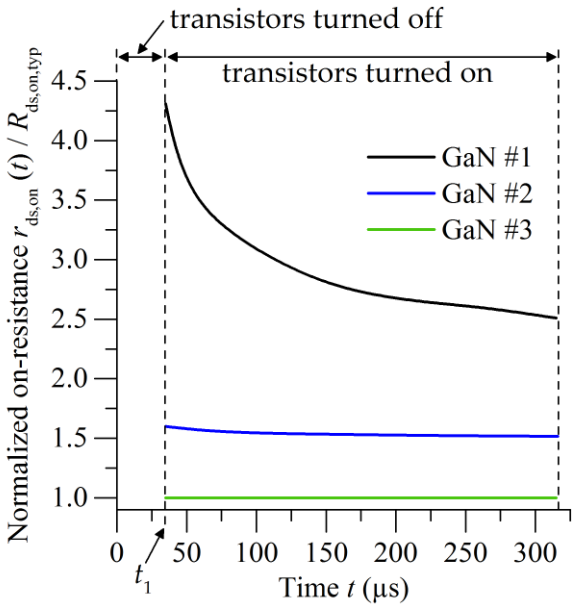


**Figure 2.** Measurement of the on-resistance of three GaN transistors from different manufacturers. The drain-source voltage in the off-state is kept at 50 % of the drain-source breakdown voltage for 20 seconds.

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