Growing antiphase-domain-free GaAs thin films out of highly ordered planar nanowire arrays on exact (001) silicon

Qiang Li, Kar Wei Ng, and Kei May Lau

Citation: Appl. Phys. Lett. **106**, 072105 (2015); doi: 10.1063/1.4913432
View online: https://doi.org/10.1063/1.4913432
View Table of Contents: http://aip.scitation.org/toc/apl/106/7
Published by the American Institute of Physics

Growing antiphase-domain-free GaAs thin films out of highly ordered planar nanowire arrays on exact (001) silicon

Qiang Li, Kar Wei Ng, and Kei May Lau[a)]
Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

(Received 11 December 2014; accepted 11 February 2015; published online 20 February 2015)

We report the use of highly ordered, dense, and regular arrays of in-plane GaAs nanowires as building blocks to produce antiphase-domain-free GaAs thin films on exact (001) silicon. High quality GaAs nanowires were grown on V-grooved Si (001) substrates using the selective aspect ratio trapping concept. The 4.1% lattice mismatch has been accommodated by the initial GaAs, a few nanometer-thick with high density stacking faults. The bulk of the GaAs wires exhibited smooth facets and a low defect density. An unusual defect trapping mechanism by a "tiara"-like structure formed by Si undercuts was discovered. As a result, we were able to grow large-area antiphase-domain-free GaAs thin films out of the nanowires without using SiO_2 sidewalls for defect termination. Analysis from XRD ω-rocking curves yielded full-width-at-half-maximum values of 238 and 154 arc sec from 900 to 2000 nm GaAs thin films, respectively, indicating high crystalline quality. The growth scheme in this work offers a promising path towards integrated III-V electronic, photonic, or photovoltaic devices on large scale silicon platform. © *2015 AIP Publishing LLC*.
[http://dx.doi.org/10.1063/1.4913432]

Epitaxial growth of III–V nanostructures and thin films on silicon is one of the most vibrant research fields today, due to its potential in bringing III–V functionalities to mainstream Si technology. To date, numerous efforts have been devoted to tackling the challenges associated with material incompatibility, including the large mismatch of lattice constants and thermal expansion coefficients and the polar-nonpolar nature of the III–V/IV semiconductor system. Among the various strategies available, selective patterned growth using the aspect ratio trapping (ART) method[1] stands out, for its capability in defect trapping, good controllability, and high compatibility with the Si complementary metal-oxide-semiconductor (CMOS) process. Recent studies also suggest that the use of V-grooved Si (111) surfaces[2,3] in the ART process is effective to restrict the generation of antiphase-domains, which has plagued the growth of III–V materials on industrial-standard (001) silicon for decades. Using the ART technique, selective area growth of high crystalline quality GaAs,[1,2] InP,[3] and InGaAs[4] in nanoscale trench-patterned silicon has been reported, aiming for eventual goal of extending Moore's Law with III–V transistors. Unfortunately, the volume of useable material within the growth cavity is too small and in too close proximity to the underlying defects,[5] limiting its application in photonic devices. Although there were a few attempts to combine the ART growth with the epitaxial lateral overgrowth (ELOG) to provide large area planar films,[6,7] V-groove patterned Si was not adopted in these former studies. In addition, the existence of dielectric patterns in the ELOG process causes hard-to-control asymmetries and irregularities of faceted growth regions, leading to higher coalescence defects and rough surface morphology in the resulting film.[6] Chemical mechanical polishing (CMP) is usually required to smoothen the surface for device fabrication.[7]

In the letter, we demonstrate the use of orderly array of planar GaAs nanowires (NWs) to produce antiphase-domain-free GaAs thin films on exact (001) silicon substrates. Closely pitched GaAs nanowires were selectively grown on SiO_2 patterned Si (001) substrates with V-grooved Si (111) surfaces through the ART process. Using these GaAs nanowire arrays as seed templates for the subsequent epitaxial lateral overgrowth, we were able to achieve GaAs thin films with a flat surface, a low defect density, and no antiphase domains. The method in the present work eliminates the necessity to use misorientated Si substrates and graded SiGe/Ge buffers.[7,8] Unlike traditional approach utilizing embedded dielectric patterns for defect termination, we have identified and exploited a "tiara"-like structure formed by the patterned Si to trap defects in the nanowires and the thin films. As a result, it erases the difficulties in achieving coalescence over dielectric patterns. A flat planar film can be obtained in a simpler way without additional CMP process. The growth scheme shows great potential to engineer high quality GaAs-on-Si compliant substrates and provides opportunities for integration of electronic, photonic, or photovoltaic devices on silicon wafers.

N-type on-axis Si (001) substrates were used in the experiment. A [110] direction orientated SiO_2 stripe pattern with line width of 90 nm and SiO_2 spacing of 40 nm was realized by dry etching. The patterned Si substrates were first cleaned in an RCA-1 (NH_4OH:H_2O_2:H_2O = 1:1:5) solution to remove surface contaminants, followed by a brief dip in 1% diluted HF to remove native oxide. Immediately after, the samples were immersed in a 45% KOH solution at a temperature of 70 °C for 15 s to form V-grooved (111) facets at the bottom of the trenches. Material growth was performed in a low-pressure (0.1 atm) metal-organic chemical vapor

[a)]Email: eekmlau@ust.hk. Tel.: (852)23587049. Fax: (852) 23581485.

deposition (MOCVD) system with a horizontal reactor (AIXTRON 200/4). The samples were thermally cleaned in the MOCVD chamber at 800 °C for 15 min in an H_2 ambient. The GaAs nanowires were grown using a two-step method that consisted of a low-temperature nucleation layer deposited at 385 °C and a high-temperature main layer deposited at 550 °C. Triethylgallium (TEGa) and Tertiarybutylarsine (TBA) were used as precursors and V/III ratios of 30 and 22 were chosen for the low-temperature and high-temperature growth, respectively. The growth rate for the GaAs NWs main layer was estimated to be 6 nm/min. After the NWs growth, the SiO_2 stripe patterns were removed by buffered oxide etch (BOE). Coalesced GaAs thin films were grown out of the nanowire arrays at a temperature of 600 °C. Arsine (AsH_3) was used as the group-V source during the lateral overgrowth to provide a high V/III ratio. The growth of the GaAs thin films was initiated with a low growth rate of 6 nm/min and a V/III ratio of 420. Afterwards, the growth rate was increased gradually to 24 nm/min, whereas the V/III ratio was decreased to 105 accordingly. Scanning electron microscope (SEM), atomic-force microscopy (AFM), high-resolution x-ray diffraction (HRXRD), transmission electron diffraction (TEM), and room temperature photoluminescence (PL) have been used to characterize the planar nanowires and the overgrown GaAs thin films.

Fig. 1(a) shows the tilted-view (70°) SEM image of the planar GaAs nanowires separated by SiO_2 sidewalls, showing good uniformity and smooth facets. XRD was used to evaluate the crystalline quality of the GaAs nanowires in the trenches. An Empyrean system working at 40 kV voltage and 40 mA current was used to perform the XRD measurements. A hybrid monochromator consisted of an x-ray mirror and a two-crystal Ge (220) two-bounce monochromator provides an intense and line-collimated x-ray beam with Cu Kα1 radiation. A channel-cut Ge analyzer crystal is placed in front of the detector to reduce angular acceptance. The defects in the imperfect epilayer manifest themselves in the broadening of the ω-rocking curves. To detect any asymmetric distribution of the defects characteristic of ART growth in line patterns, we did two-scans across the GaAs peak, with the x-ray beam perpendicular to the stripes and the other with the beam parallel to the stripes. Interestingly, we found the former alignment gives smaller rocking curve full-width-at-half-maximum (FWHM) than the latter, as indicated by Fig. 1(b). The orientation dependence of the x-ray linewidth stemmed from an unequal distribution of defects in the [1$\bar{1}$0] and [110] directions, which has been observed in former studies of InP growth on patterned Si.[9] Fig. 1(b) also presents the FWHM of the GaAs nanowire array decreasing monotonically with its thickness. For ~200 nm GaAs on V-grooved Si (111) surface, we measured an FWHM of 414 and 540 arc sec with x-ray beam perpendicular to and parallel to the stripes, respectively, which surpassed the FWHM (611 arc sec) measured from a 1 μm thick GaAs film on a nonpatterned Si substrate.

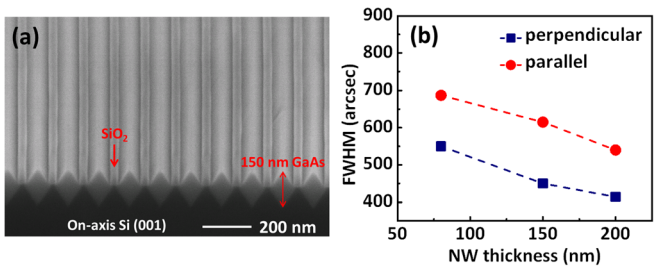

FIG. 1. (a) Tilted SEM image of 150 nm thick GaAs nanowires separated by SiO_2 sidewalls. (b) Dependence of (004) ω-rocking curve FWHM on nanowire thickness.

Cross-sectional TEM has been utilized for defect analysis in the GaAs nanowires. TEM specimens were prepared using conventional mechanical thinning, followed by ion beam milling. A JEOL2010F field-emission microscope operating at 200 keV was used for the TEM observation. Fig. 2(a) displays a bright-field TEM image of the planar GaAs nanowires taken along the [110] zone axis. Narrow (001) top facets and smooth {111} side facets were observed at the growth fronts. Fig. 2(b) presents the selective area diffraction pattern taken near the peak of a GaAs nanowire, revealing a single-crystalline zinc blend structure with excellent coherency. The zoomed-in image in Fig. 2(c) shows that the lattice mismatch between Si and GaAs was accommodated by the initial few-nanometer-thick GaAs layer containing high-density {111} plane stacking faults. The bulk of the GaAs, on the other hand, shows high crystalline quality, with few defects. Because the growth of GaAs in every trench started with nucleation on the two equivalent Si{111} planes simultaneously, a void tube was formed at the bottom of the V-groove when the two growth fronts merged together, which can been seen in the high-resolution TEM image in Fig. 2(d). One challenge of using such a patterned growth method is the lack of capability to trap (111)-orientated

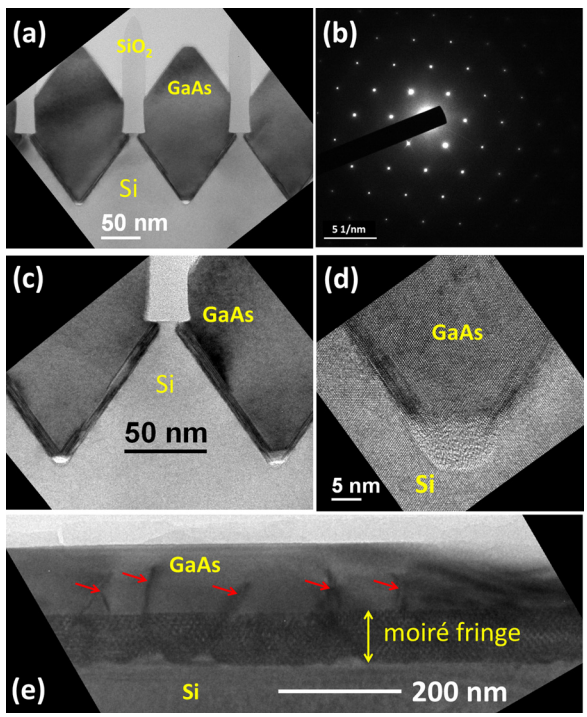

FIG. 2. (a) Cross-sectional TEM image of GaAs nanowires taken along the [110] zone axis; (b) selective area diffraction pattern taken near the peak of a GaAs nanowire; (c) cross-sectional TEM image of the initial few-nanometer-thick GaAs with high density stacking faults; (d) high resolution TEM image of the hetero-interface of GaAs/Si(111); and (e) cross-sectional TEM image of GaAs nanowires along the parallel direction of the trench.

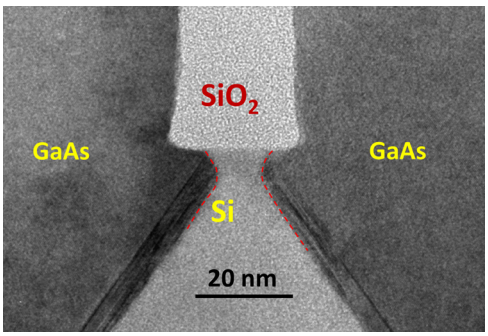

FIG. 3. Zoomed-in TEM image showing the stacking fault trapping by a "tiara"-like structure formed by the Si undercuts.

defects along the parallel direction of the trench. Fig. 2(e) shows a parallel-view TEM image taken along the [1$\bar{1}$0] zone axis. Due to the lattice overlap of Si and GaAs, a thick moiré fringe pattern appears at the V-grooves region. Compared to the perpendicular-view TEM, there are more defects threading upwards in the parallel direction, as indicated by the red arrows in Fig. 2(e).

Compared with former studies on ART growth, one distinct feature of these highly ordered nanowires is that the stacking faults at the hetero-interface of GaAs/Si(111) were stopped by a "tiara"-like structure formed by the Si undercutting beneath the SiO_2 sidewalls, as evidenced by the zoomed-in TEM image in Fig. 3. Thanks to this unique defect confinement mechanism, the SiO_2 sidewalls can be removed for the subsequent overgrowth process without compromising defect trapping capability. We performed ELOG of GaAs on nanowires of 150 nm thick. The nanowire coalescence region has been inspected by TEM. Fig. 4(a) shows a cross-sectional TEM image consisting of two complete Si V-grooves. Remarkably, the "tiara"-like structure has prevented most of the stacking faults from propagating into the upper GaAs film. Fig. 4(b) highlights the hetero-

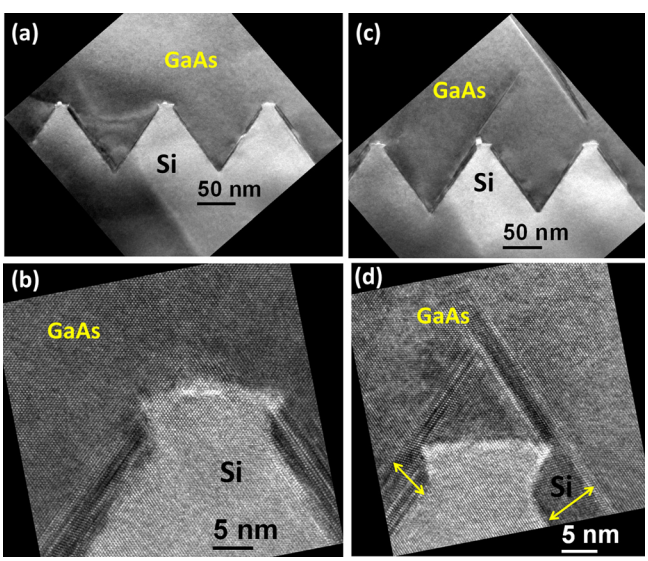

FIG. 4. (a) and (b) Cross-sectional TEM image showing the defect trapping in the coalesced GaAs thin film by a "tiara"-like structure formed by Si; (c) cross-sectional TEM showing a part of stacking faults propagating into the upper layer; and (d) high-resolution TEM image showing the crossing of two stacking faults over the Si ridge.

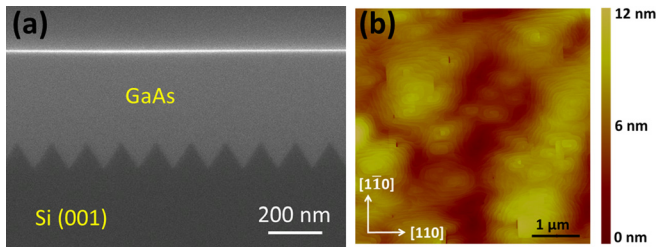

FIG. 5. (a) Cross-sectional SEM image and (b) AFM image of approximately 300 nm coalesced GaAs thin film grown on a nanowire array.

interface of GaAs/Si surrounding the peak of the "tiara." There are no threading defects from the top of the Si ridge. In some V-grooves, the stacking-disorder region can be too thick for a complete defect trapping, and a part of the stacking fault will climb out of the concave area, as shown in Fig. 4(c). The closely pitched V-groove structures enhanced the likelihood of interactions and annihilation of those escaped {111} plane stacking faults. Fig. 4(d) presents the crossing of two stacking faults over the Si ridge, ending up with the removal of one stacking fault from the upper layer.

Merging nanowires without SiO_2 in between is advantageous for improving the surface morphology of the resulting planar thin films. The cross-sectional SEM image in Fig. 5(a) indicates that a flat surface was reached after 300 nm of GaAs overgrowth. The morphology of the 300 nm thick coalesced GaAs was further examined by AFM, as illustrated in Fig. 5(b). A root-mean-square (rms) roughness of 1.9 nm across a scanned area of $5 \times 5\ \mu m^2$ has been achieved. We found spiral patterns and a few lines related to stacking faults, but no antiphase-domain boundaries. The absence of antiphase-domains is attributed to the III–V epitaxy on Si {111} planes with a homogeneous nucleation.[2] Eventually, thicker GaAs layers grown on top of the faceted nanowires are antiphase-domain free with better crystalline quality. For a 900 nm GaAs thin film, analysis from XRD ω-rocking curves yielded an FWHM of 238 arc sec in the [110] direction (i.e., x-ray beam parallel to the V-grooves) and of 310 arc sec in the [1$\bar{1}$0] direction (i.e., x-ray beam perpendicular to the V-grooves). For a 2 μm GaAs thin film, an FWHM of 154 arc sec in the [110] direction and of 196 arc sec in the [1$\bar{1}$0] direction was achieved. These results are among the low records of FWHM of GaAs epitaxy on Si with the same thickness.[10]

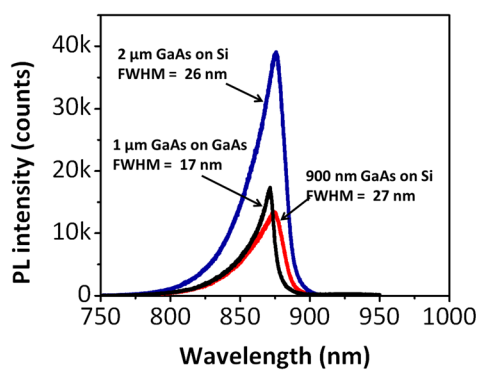

FIG. 6. Room-temperature PL spectra measured from the un-doped GaAs films grown out of nanowires on Si and a reference PL spectra collected from 1 μm un-doped GaAs grown on a semi-insulating GaAs substrate.

Room-temperature PL measurement was performed with 633 nm laser excitation to further study the epi-layer quality. Fig. 6 plots the PL spectra measured from the un-doped GaAs films grown out of nanowires on Si and a reference PL spectra collected from 1 μm un-doped GaAs grown on a semi-insulating GaAs substrate. Compared to the homo-epitaxial GaAs reference, the GaAs films on Si show approximately 50% larger FWHM and high intensity level, promising for device applications.

The high quality heteroepitaxial GaAs films in this study were constructed by the planar array of selectively grown GaAs nanowires on Si. The influence of the width, spacing, and height of the nanowires on the resultant thin films is yet to be systematically investigated. But, in general, we have found that the crystalline quality of the coalesced GaAs is not sensitive to the initial nanowire thickness. For a 900 nm GaAs thin film grown out of nanowires with a height of 80 nm, analysis from XRD ω-rocking curves yielded an FWHM of 223 arc sec in the [110] direction and of 317 arc sec in the $[1\bar{1}0]$ direction, comparable to the aforementioned x-ray linewidth measured from 900 nm GaAs grown out of the nanowires of 150 nm thicknesses. In terms of the nanowire spacing, we expect a larger impact on the quality of the coalesced films. On the one hand, the defect density can be further reduced in the ELOG process with wider nanowire spacing, provided that no new defects were generated at the GaAs/Si interfacial region during lateral overgrowth. On the other hand, merging nanowires that are too far apart from each other after a long distance lateral overgrowth may increase the coalescence dislocations and elevate surface roughness of the GaAs films.

In conclusion, we have demonstrated the growth of low defect density GaAs thin films out of highly ordered planar GaAs nanowires on industrial-standard on-axis Si (001) substrates. The use of V-grooved Si (111) surfaces in the aspect ratio trapping process prevents the formation of antiphase-domains. TEM analysis reveals an unusual defect trapping effect via a "tiara"-like structure formed by the patterned Si. X-ray diffraction shows high crystalline quality of the resulting coalesced GaAs thin films. The growth scheme in this work provides a strategy to integrate large-area GaAs and other III–V materials onto industrial-standard Si substrates for device applications.

This work was supported in part by Grant (Nos. 614312 and 614813) from the Research Grants Council of Hong Kong. The authors would like to thank SEMATECH for providing the patterned Si substrates and the MCPF of HKUST for technical support. Helpful discussions with C. Liu, B. Shi, X. Lu, and Y. Wan are also acknowledged.

[1]J. Z. Li, J. Bai, J.-S. Park, B. Adekore, K. Fox, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, Appl. Phys. Lett. **91**, 021114 (2007).
[2]W. Guo, L. Date, V. Pena, X. Bao, C. Merckling, N. Waldron, N. Collaert, M. Caymax, E. Sanchez, E. Vancoille, K. Barla, A. Thean, P. Eyben, and W. Vandervorst, Appl. Phys. Lett. **105**, 062101 (2014).
[3]C. Merckling, N. Waldron, S. Jiang, W. Guo, N. Collaert, M. Caymax, E. Vancoille, K. Barla, A. Thean, M. Heyns, and W. Vandervorst, J. Appl. Phys. **115**, 023710 (2014).
[4]R. Cipro, T. Baron, M. Martin, J. Moeyaert, S. David, V. Gorbenko, F. Bassani, Y. Bogumilowicz, J. P. Barnes, N. Rochat, V. Loup, C. Vizioz, N. Allouti, N. Chauvin, X. Y. Bao, Z. Ye, J. B. Pin, and E. Sanchez, Appl. Phys. Lett. **104**, 262103 (2014).
[5]N. H. Julian, P. A. Mages, C. Zhang, and J. E. Bowers, J. Cryst. Growth **402**, 234 (2014).
[6]J. Z. Li, J. Bai, C. Major, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, J. Appl. Phys. **103**, 106102 (2008).
[7]Y. Q. Wu, M. Xu, P. D. Ye, Z. Cheng, J. Li, J.-S. Park, J. Hydrick, J. Bai, M. Carroll, J. G. Fiorenza, and A. Lochtefeld, Appl. Phys. Lett. **93**, 242106 (2008).
[8]R. M. Sieg, S. A. Ringel, S. M. Ting, S. B. Samavedam, M. Currie, T. Landgo, and E. A. Fitzgerald, J. Vac. Sci. Technol., B **16**, 1471 (1998).
[9]Q. Li, K. W. Ng, C. W. Tang, K. M. Lau, R. Hill, and A. Vert, J. Cryst. Growth **405**, 81–86 (2014).
[10]Y. B. Bolkhovityanov and O. P. Pchelyakov, Phys. Usp. **51**, 437 (2008).