GaAs-InGaAs-GaAs Fin-Array Tunnel Diodes on (001) Si Substrates with Room-Temperature Peak-to-Valley Current Ratio of 5.4

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***Abstract*—In this letter, we report selective area growth of GaAs, $In_{0.2}Ga_{0.8}As$ and GaAs/$In_{0.2}Ga_{0.8}As$/GaAs quantum-well fins of 65 nm width on exactly orientated (001) Si substrates. By exploiting high aspect ratio trenches formed by patterned SiO_2 on Si and a V-grooved Si (111) surface in the aspect ratio trapping process, we are able to achieve good material quality and structural properties, as evidenced by x-ray diffraction, scanning electron microscopy, and transmission electron microscopy. The fabricated GaAs-$In_{0.2}Ga_{0.8}As$-GaAs fin-array tunnel diodes exhibit a maximum room-temperature peak-to-valley current ratio of 5.4, and negative differential resistance characteristics up to 200 ˚C.**

***Index Terms*—Aspect ratio trapping, peak-to-valley current ratio, quantum-well fins, tunnel diode.**

I. Introduction

TUNNEL DIODES with negative differential resistance (NDR) have been used to build high-frequency oscillators [1], multiple-valued logic [2,3], and low-power static random access memory cells [4]. Compared with silicon tunnel diodes, III-V materials can lead to much higher peak-to-valley current ratio (PVCR) because of their direct band-gap properties, low tunneling effective masses, and heterostructures. Attempts have been made in recent years to integrate III-V tunnel diodes on silicon substrates [5-9], aiming to advance CMOS technology with novel device concepts and circuit architectures.

Among various III-V/Si hybrid integration schemes, the aspect ratio trapping (ART) technique is attracting significant attention due to its unique defect trapping capability and good compatibility with the existing CMOS manufacturing platform [10-12]. Using the ART approach, III-V crystals are selectively grown in high aspect ratio cavities formed by a patterned dielectric on Si. Hetero-interfacial defects can presumably be blocked by the dielectric sidewalls, leading to high quality materials in the upper region of the cavities where devices are built. Recent advances in this field have led to the demonstration of InGaAs FinFETs [13] and Gate-All-Around nanowire transistors [14] on 300 mm Si substrates.

In this work, we report high density, orderly array of GaAs and $In_{0.2}Ga_{0.8}As$ fins with fin-width of 65 nm on exactly orientated (001) Si substrates. GaAs-$In_{0.2}Ga_{0.8}As$-GaAs fin-array tunnel diodes were fabricated to demonstrate the good material quality and atomically-sharp surface facets. Maximum room-temperature PVCR of 5.4 has been achieved, outperforming vertical nanowires based tunnel diodes on (111) Si substrates reported in the literature.

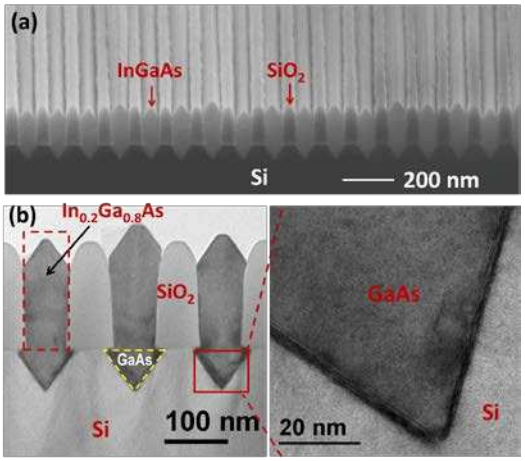

Fig. 1. Tilted-view SEM image (a) and cross-sectional TEM image (b) of the array of InGaAs fins separated by SiO_2 spacer on (001) Si substrates. The zoomed-in TEM image highlights the hetero-interface between the GaAs buffer and Si substrate.

II. Material Growth and Characterization

On-axis (001) Si substrates were patterned by SiO_2 stripes with a line width of 65 nm and a line pitch of 130 nm. Si V-grooves with (111) surface were formed by anisotropic KOH etching. The combined SiO_2 sidewall and recessed V-shaped Si pocket results in an aspect ratio of approximately 3.6 for effective defect trapping. The GaAs and InGaAs fins were grown using a two-step procedure [15, 16] in a low-pressure MOCVD system. Fig. 1(a) shows 70˚ tilted-view SEM image of the $In_{0.2}Ga_{0.8}As$ fins separated by SiO_2 spacers. Fig. 1(b) displays cross-sectional TEM images of $In_{0.2}Ga_{0.8}As$ fins with underlying GaAs buffer, approximately 60 nm thick just filling up the V-shaped pockets. Despite the few-nanometer-thick stacking faults formed at the GaAs/Si hetero-interface, as

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highlighted by the zoomed-in TEM image, the main InGaAs

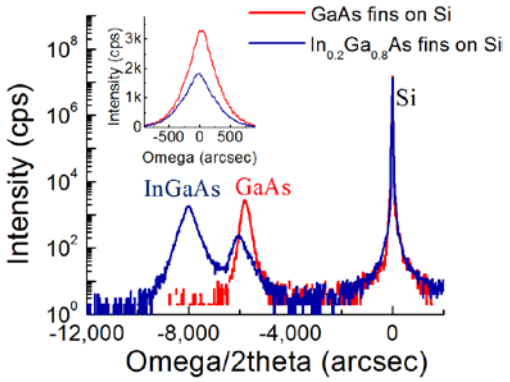

Fig. 2. High resolution XRD ω-2theta curves of InGaAs and GaAs fin-arrays near the (004) reflections; the inset shows ω-rocking curves.

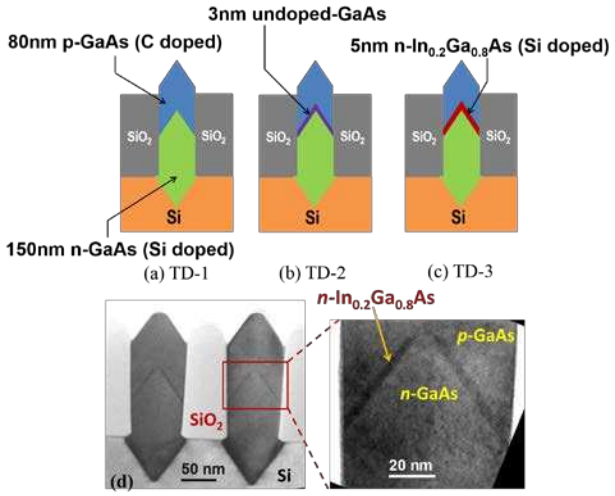

Fig. 3. (a)-(c) Schematics of three tunnel diodes in this study; (d) Cross-sectional TEM images of the GaAs-InGaAs-GaAs tunnel diode.

layer shows good crystalline quality.

High-resolution x-ray diffraction was used to further characterize the nano-fin arrays. The lattice parameters of the InGaAs fins in the growth plane $a_{//}$ and in the growth direction $a_{\perp}$ were determined to be 5.692 Å and 5.767 Å, respectively, based on x-ray reciprocal space maps of the (224) reflections. The free-standing lattice constant (a_0 = 5.731 Å) and hence an Indium fraction (19.3%) can be calculated from the elastic theory

$$a_{\perp} = (a_0 - a_{//})(1 + 2\frac{C_{12}}{C_{11}}) + a_{//} \quad (1)$$

where the elastic stiffness constants C_{12} and C_{11} of $In_{0.19}Ga_{0.81}As$ were determined to be 51.88 and 112.24 GPa, respectively, by linear extrapolation.

Fig. 2 shows the data of x-ray diffraction ω-2theta scan measurements. The peak reflected from the $In_{0.2}Ga_{0.8}As$ fins is left-shifted as expected. The inset of Fig. 2 compares (004) plane ω-rocking curves, the full-width-at-half-maximum (FWHM) of which is directly related to the concentration of defects that disrupt the perfect parallelism of atomic planes in a crystalline lattice [17]. The GaAs and InGaAs fins exhibited FWHM of 529 and 551 arcsec, respectively, indicating comparable crystalline quality. Plan-view (PV) TEM is a more reliable technique to estimate defect density. A recent study of GaAs fins of comparable thicknesses grown on V-grooved Si

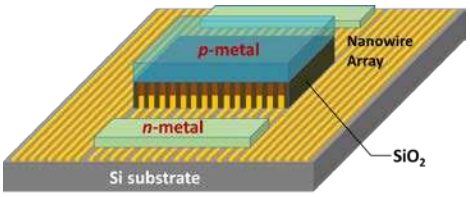

Fig. 4. Schematic of fabricated tunnel diodes (not drawn to scale).

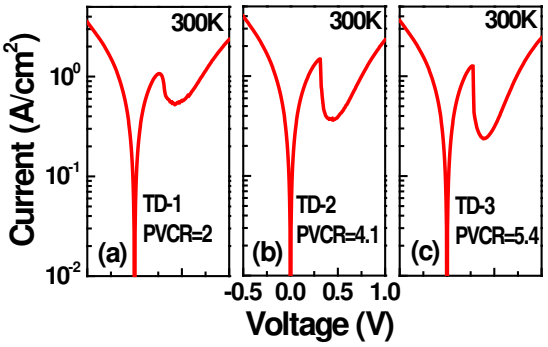

Fig. 5. Semi-logarithmic plots of the current-voltage characteristics.

correlated a XRD ω-scan FWHM of 647 arcsec to a twin plane density of 8×10^8 cm^{-2} in PV-TEM micrograph [17]. In this work, a slightly smaller twin plane density is expected.

III. Device Fabrication and Results

Three fin-array tunnel diode samples (TD-1, TD-2 and TD-3) were fabricated. Fig. 3(a)-(c) show the diode structures grown. Silicon was used for n-type doping and carbon was used for p-type doping. According to Hall measurement on planar calibration wafers, the electron and hole densities were $1\times10^{19}/cm^3$ and $3.2\times10^{19}/cm^3$, respectively. Fig. 3(d) shows cross-sectional TEM images of TD-3. The 5 nm n-InGaAs layer at the junction interface was clearly identified.

Device fabrication started with formation of the Ti/Pt/Au p-metal pad by e-beam evaporation and lift-off. Using the p-contacts as a self-aligned mask, the n-GaAs layer was exposed by wet etching (H_3PO_4:H_2O_2:H_2O=3:1:50) and the SiO_2 spacer was removed by buffered oxide etch subsequently. Finally, n-metal pad was formed by evaporating Ni/Ge/Au metal stack on the exposed n-GaAs wires and lift-off process. Fig. 4 presents a 3D schematic of a fabricated diode.

Fig. 5 shows semi-logarithmic plots of the current-voltage characteristics measured from tunnel diodes comprising of 192 fins in parallel. TD-1, TD-2, and TD-3 exhibit negative differential resistance at forward bias with PVCR of 2.0, 4.1, and 5.4, respectively. Voltage swing, which refers to the difference between peak voltage and projected forward voltage with the same current, was determined to be around 0.5V for all the diodes. It reflects noise handling ability in tunnel diode based logic circuits. The peak current densities J_p normalized by the total area of the (111) facets are 1.1, 1.5, and 1.3 A/cm^2 for TD-1, TD-2, and TD-3, respectively. These values are comparable to tunnel diodes used for SRAMs [4] but lower than those for TFETs [7]. According to the experimentally derived

characteristic trend line [18] for GaAs homojunction tunnel

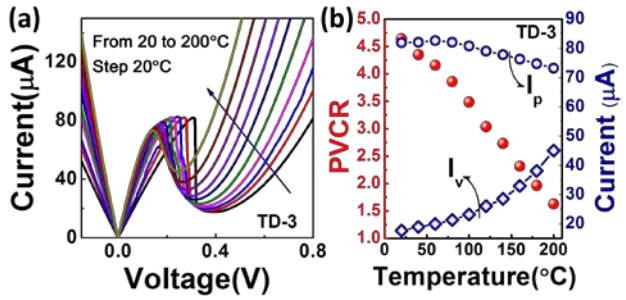

Fig. 6. I_p, I_v, and PVCR as a function of temperature for a diode of TD-3.

TABLE I
COMPARISON OF THIS WORK WITH PUBLISHED NANOWIRE TUNNEL DIODES INTEGRATED ON SILICON PLATFORM

Study	Substrate	Growth technique	Diode structure	PVCR
[7]	Si(111)	MOCVD	Esaki: *n*-InAs/*p*-Si	2.4
[8]	Si(111)	MBE	Esaki: *n*-In(Ga)As/*p*-Si	3
[20]	Si(111)	VLS	Esaki: *p*/*n*-Si	4.3
[21]	Si(111)	PAMBE	RTD: AlN/GaN	2.4
[22]	Si (111)	VLS	Esaki: *n*-Si/*p*-Ge	2.75
TD-1	Si(001)	MOCVD	Esaki: *p*/*n*- GaAs	2.0
TD-2	Si(001)	MOCVD	Esaki: *p*/*i*/*n*- GaAs	4.1
TD-3	Si(001)	MOCVD	Esaki: *p*-GaAs /*n*-$In_{0.2}Ga_{0.8}As$/*n*-GaAs	5.4

diodes, which describes an exponential relationship between J_P and reduced doping $N^*=N_AN_D/(N_A+N_D)$, the J_p reported here is in a reasonable range but clearly limited by the maximum doping concentration we can achieve presently. Since the density of states (DOS) for holes (9.0×10^{18} cm^{-3}) is much greater than DOS for electrons (4.7×10^{17} cm^{-3}) in GaAs, a higher doping level in p-GaAs is highly desirable to boost J_p and PVCR simultaneously [18].

Fig. 6(a) displays temperature-dependent current-voltage curves of a diode of TD-3. The peak current (I_p), valley current (I_v) and PVCR as a function of temperature were extracted and plotted in Fig. 6(b). The valley current increases monotonically with temperature, due to enhanced tunneling via defect states in the bang gap. The peak current initially shows a slight increase with temperature, and then begins decreasing with temperature beyond 60 ˚C. This behavior is attributed to the smearing of the Fermi function and increase in the density of states at high temperatures [5, 19]. At 100˚C, the operating temperature of most microprocessors [5], TD-3 still remains a PVCR of 3.5. And the negative differential resistance characteristic is maintained up to 200˚C.

Table I compares this work to published reports of Ge, Si, and III-V nanowire based tunnel diodes integrated on Si substrates. In sharp contrast to most of previous results using vertical nanowires on (111) Si substrates, our devices were fabricated using in-plane fin-arrays formed by catalyst-free growth on CMOS-compatible (001) Si and thereby offers a much better compatibility for heterogeneous integration by direct growth. The smooth and abrupt interfaces of InGaAs quantum wells also suggest the great potential of using these fin-arrays for high-mobility (111) channel multi-gate transistors [23].

IV. CONCLUSION

In conclusion, we have demonstrated highly ordered GaAs and $In_{0.2}Ga_{0.8}As$ fins as well as GaAs-$In_{0.2}Ga_{0.8}As$-GaAs tunnel diodes on exact (001) Si substrates. The results show great potential of integrating these nanostructured III-V fin-arrays on silicon platform for the application in ultra-fast and low power logic circuits.

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