Fin-array tunneling trigger with tunable hysteresis on (001) silicon substrate

Yu Han, Qiang Li, *member, IEEE*, and Kei May Lau, *Fellow, IEEE*

***Abstract*— We report the fabrication and characterization of a GaAs fin-array tunneling trigger monolithically integrated on an exact (001) silicon substrate. A Schmitt-trigger-like behavior was observed under double sweep condition by connecting the tunnel diode with an on-chip load resistor. The tunneling trigger circuit was studied using load line analysis. Critical parameters of the circuit were extracted. We found that the circuit hysteresis can be tuned by tailoring of the diode dimensions and load resistor values.**

***Index Terms*— Tunnel diodes, GaAs fin-array, Schmitt trigger, monolithic integration, digital circuits.**

I. Introduction

Aiming at enhancing circuit performance and functionalities, merging III-V electronic and photonic technologies with silicon complementary metal-oxide-semiconductor (CMOS) process is receiving a tremendous amount of attention [1]-[4]. Integrating III-V tunnel diodes on Si can form the building blocks for a new class of ultra-high speed circuits with reduced power consumption and circuit complexity [5]-[11], if challenges associated with the thermal and lattice mismatches and the polar/non-polar growth can be properly addressed [12]-[16]. In addition, direct integration on (001) silicon substrates is fully compatible with the well-established processing technologies of advanced CMOS foundries. Taking advantage of the defect necking effect in the aspect ratio trapping (ART) process, we have recently demonstrated GaAs/InGsAs fin-array tunnel diodes and inverters on exact (001) silicon substrates using a GaAs buffer with a thickness of only 160 nm [17], [18].

When a tunnel diode is connected with a load resistor or transistor, hysteresis of current-voltage (IV) characteristics can be observed if the value of the load resistance is larger than that of the negative differential resistance (NDR). This hysteresis has been utilized to build various digital circuits, including universal and reconfigurable logic gates [19], trigger circuits [20], and multi-valued memory cells [21]. In this work, we fabricated a tunneling trigger with two fin-array tunnel diodes connected back to back. By sweeping forward and backward at the input end, a Schmitt-trigger-like behavior is observed at the output end. We also show that the tunneling trigger circuit is highly predictable and controllable by varying the device size and series resistance.

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Y. Han, Q. Li, and K.M. Lau are with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong. (E-mail: eekmlau@ust.hk).

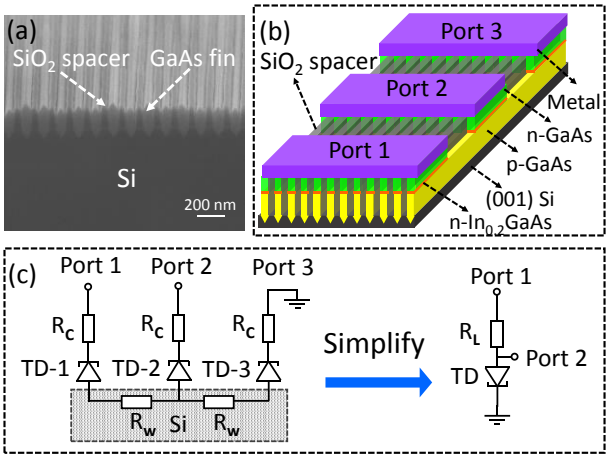

Fig. 1. (a) 70° tilted SEM image of the as-grown GaAs fin-array on (001) Si substrate. (b) Schematic of the GaAs fin-array tunneling trigger monolithically integrated on (001) Si substrates. (c) Equivalent circuit of the tunneling trigger. Simplified circuits is shown on the right.

II. Device Structure And Fabrication

Fig. 1(a) presents a 70° tilted-view SEM image of the highly ordered GaAs fin-array grown on (001) silicon. Detailed material growth and characterization of this structure has been reported [17]. Prior to device fabrication, the sample was thermally annealed at 550 °C for 30 sec to activate the hydrogen-passivated carbon in the p-GaAs. Metal stack (Ni/Ge/Au) was firstly patterned on the n-GaAs fins. Then, wet etching (H_3PO_4:H_2O_2:H_2O = 3:1:50) was performed to remove the top n-GaAs/InGaAs and partially etch the p-GaAs. Fig. 1(b) displays the schematic of the fabricated fin-array tunneling trigger. Three identical tunnel diodes are electrically connected by partially etched p-GaAs fins. Each fin consists of three epi-layers: 80 nm n-GaAs, 5 nm n-$In_{0.2}GaAs$ and 150 nm p-GaAs. Fig. 1(c) shows the equivalent circuit of the fabricated tunneling trigger, where R_C corresponds to the contact resistance between the metal stack and the n-GaAs fins, while R_W refers to the resistance of the partially etched p-GaAs fins. The input voltage was applied on Port 1 and the output voltage was measured from Port 2, with Port 3 grounded. During the measurement, TD-1 was reverse biased and served as a resistor. Therefore, the simplified circuit, consisting of series-connected tunnel diode and resistor, is displayed on right side of Fig. 1(c).

III. Results And Discussion

We measured the voltage and current characteristics of the fabricated fin-array tunneling trigger under a double sweep condition (0 to 3 V and then 3 V to 0). For clear comparison, the curves of tunnel diode voltage (V_{TD}), load resistor voltage (V_R) and total current (I) are plotted together in Fig. 2. The voltage drop across the tunnel diode exhibits a Schmitt-trigger-like behavior, with abrupt increase and decrease at different input voltages. When the input voltage was increased to 2.12 V (sweep forward), the output voltage increased suddenly from 0.41 V to 0.80 V. Similarly, the output voltage slumped from 0.54 V to 0.25 V, when the input voltage was decreased to 1.45 V (sweep backward). Bistable characteristic can be observed in all the measured parameters when the input voltage falls between 1.45 V and 2.12 V.

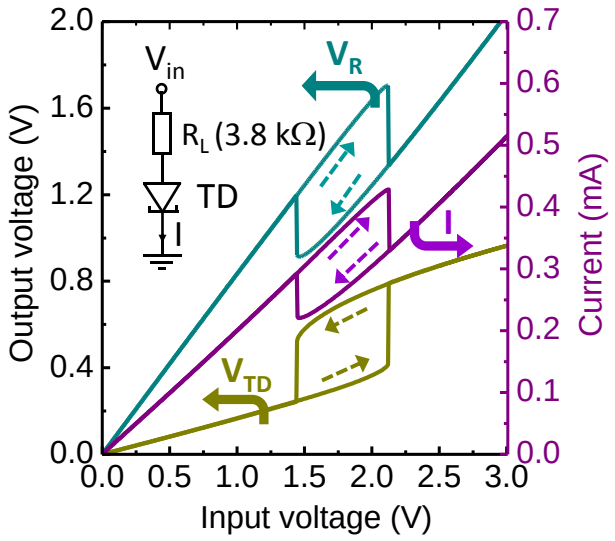

Fig. 2. Measured current and voltage across both series resistor and tunnel diode when sweep forward and backward. Hysteresis was observed in all parameters and Schmitt-trigger-like behavior was obtained from the voltage across the tunnel diode.

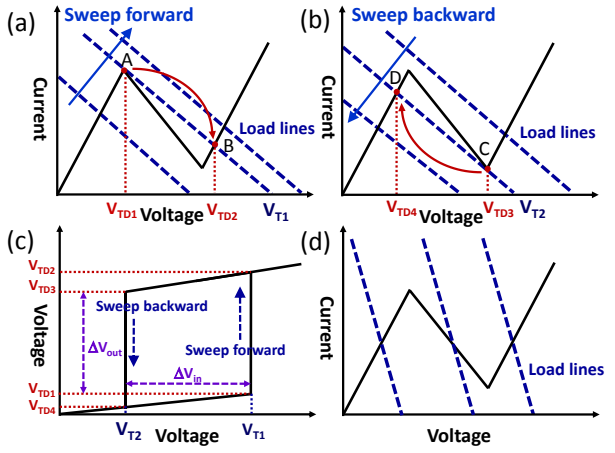

Fig. 3. Schematic showing the basic principle of the tunneling trigger. (a) Tunnel diode IV curve with load line when sweeping forward. Switch point resides around the peak point. (b) Tunnel diode IV curve with load line when sweeping backward. Switch point resides around the valley point. (c) Schematic showing the Schmitt-trigger characteristic (d) No switch point can be found when series resistance is smaller than the negative differential resistance.

Fig. 3 briefly summarizes the basic principle of the tunneling trigger. To simplify the analysis, we used an ideal tunnel diode IV curve with constant resistance at different regions before the valley voltage. While after the valley point, we treated the tunnel diode as a simple forward-biased PN junction. The current-voltage relationship of an ideal PN junction can be written as $J = J_0 \exp(\frac{qV}{kT} - 1)$, where J_0 is the saturation current density. The trigger behavior can only be observed when the series resistance exceeds the NDR of the tunnel diode. As shown by the load line analysis in Fig. 3(a), the intersections of the load line of the resistor and the IV curve of the tunnel diode indicate stable working points of the circuit. The intersection of the load line and the abscissa axis refers to the input voltage value, and the abscissa of the working point corresponds to the voltage drop across the tunnel diode (output voltage). When sweeping forward, the output voltage increases linearly until the input voltage reaches the value of V_{T1}, where two stable working points A and B co-exist. Further increase of the input voltage leads to the transition to a single working point and an abrupt increases of output voltage from V_{TD1} to V_{TD2}. However, when sweeping backward, we observe the turning point when the input voltage decreases to the value of V_{T2}, as indicated by the red arrow in Fig. 3(b). Fig. 3(c) presents the voltage drop across the tunnel diode under the double sweep condition with clearly identified Schmitt-trigger-like behavior. When the series resistance is smaller than the NDR, only one stable working point exists and no trigger behavior can be obtained, as evidenced by the load lines analysis in Fig. 3(d).

TABLE I
Calculated Parameter Values of Tunneling Trigger

Parameters	Theoretical values	Experimental values
V_{T1}	$V_{Pi} + J_P A(R_L + R_P)$	2.12 V
V_{T2}	$V_{Vi} + J_V A(R_L + R_P)$	1.44 V
V_{TD1}	$V_{pi} + J_P A R_P$	0.41 V
V_{TD2}	$V_{Vi} + J_V A R_P < V_{TD2} < \frac{kT}{q} \ln(\frac{J_P}{J_o} + 1)$	0.79 V
V_{TD3}	$V_{Vi} + J_V A R_P$	0.52 V
V_{TD4}	$0 < V_{TD4} < V_{pi} + J_P A R_P$	0.24 V
ΔV_{in}	$(V_{Pi} - V_{Vi}) + A(J_P - J_V)(R_L + R_P)$	0.68 V
ΔV_{out}	$(V_{Vi} - V_{Pi}) - A(J_P - J_V)R_P$	0.11 V
NDR	$(V_{Pi} - V_{Vi}) / A(J_P - J_V) - R_P$	1.25 kΩ (intrinsic)

Based on the ideal case in Fig. 3, we calculated the values of different parameters of the tunneling trigger circuit and summarized the results (both theoretical and experimental) in Table I. Both V_{T1} and V_{T2} are influenced by the intrinsic peak and valley voltage (V_{Pi} and V_{Vi}) of the tunnel junction, the peak and valley current density (J_P and J_V), and device size "A". V_{Pi} and V_{Vi} are determined solely by the properties of the tunnel junction. R_p is the parasitic resistance of the tunnel diode and R_L is the load resistance of the circuit. The definition of other critical parameters is illustrated in Fig. 3(c). As summarized in Table II, when R approaches infinity (load line parallel to abscissa axis), ΔV_{in} would also be infinity and the ratio $\Delta V_{out}/\Delta V_{in}$ (describing the curve shape) would be zero. When

R_L is equal to NDR, ΔV_{in} is zero and the curve ratio $\Delta V_{out}/\Delta V_{in}$ would approach infinity.

TABLE II
BOUNDARY CONDITIONS OF THE TUNNELING TRIGGER

	ΔV_{in}	$\Delta V_{out}/\Delta V_{in}$
$R_L \rightarrow \infty$	∞	0
$R_L \rightarrow$ NDR	0	∞

We demonstrated the hysteresis is tunable by varying the device dimensions. As shown in Fig. 4(a), we observe a monotonic decrease of the curve ratio $\Delta V_{out}/\Delta V_{in}$ as device size increases. As illustrated previously in Table I, both ΔV_{out} and ΔV_{in} are directly related to device size "A", area of the metal contacts. Changes in the device size would result in a direct scaling of the peak current. Although the contact resistance R_P and R_L would also scale with the device area, the effect is much smaller. Therefore, the observed change of ΔV_{out} and ΔV_{in} with device dimension scales agrees with the theoretical analysis shown in Fig. 3. The hysteresis can also be tuned by varying the values of the load resistor, as verified by the measurement in Fig. 4(b). An increase of the load resistor value results in the decrease of the curve ratio $\Delta V_{out}/\Delta V_{in}$. It should be noted that both V_{TD1} and V_{TD3} become smaller as R_L increases and V_{TD1} exhibits a much larger dependence on R_L than V_{TD3}. The shift of V_{TD1} with R_L might be due to the rounded peak point and the kinks in the NDR region, as has been reported in Ref. [12] and [22]. The mechanism of the weak dependence of V_{TD3} on R_L is still under investigation.

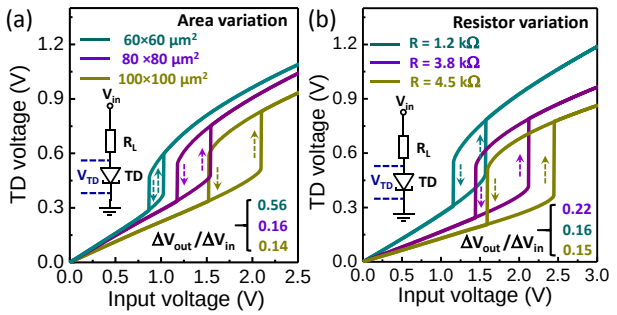

Fig. 4. (a) Tunneling trigger behavior measured from devices with different sizes. (b) Tunneling trigger behavior measured from devices with different load resistance.

IV. CONCLUSION

In conclusion, we have demonstrated tunneling trigger characteristics in fin-arrays with tunable hysteresis on exact (001) silicon substrates. The tunable hysteresis was theoretically proven by load line analysis and experimentally validated by varying device dimension and load resistance. These results show promises for III-V tunnel diode based digital circuits on exact (001) silicon substrates.

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