A Study of Current Transport in Schottky Diodes Based on AlInSb/InSb-QW Heterostructures

A thesis submitted in fulfilment of the requirement for the degree of Doctor of Philosophy

By

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ABSTRACT

The major objective of this thesis is the analysis of novel AlInSb/InSb QW Schottky diodes which may play an important role in future low-power high-speed electronic devices such as FETs, as well as showing promise for high frequency rectification. Although InSb has the highest electron mobility among the III-V semiconductors, due to lattice mismatch with common binary substrates, its 2DEG systems have far less mobility than anticipated values. The large lattice mismatch between AlInSb alloy and the substrate GaAs in AlInSb/InSb system results in a high density of structural defects which results in a high leakage current. Both large leakage current and low barrier height introduce difficulties in forming good Schottky diodes. Schottky diodes in this material system are largely unexplored. Two different planar structure designs (elementary, and surface channel) were used in this thesis to form AlInSb/InSb QW Schottky diodes. Various surface treatments were trialled to suppress diode leakage current. The fabricated AlInSb/InSb QW Schottky diodes were evaluated based on I-V measurements over a wide range of temperatures 3-290 K.

Various models are evaluated and successfully used to describe the I-V characteristics of these AlInSb/InSb QW Schottky diodes. Depending on the applied surface treatment, two barrier heights (Φ_B) are reported, ~0.36 eV and ~0.16 eV. The larger Φ_B was successfully explained with Fermi level (FL) pinning at one third of the band gap $\left(\frac{1}{3}\mathrm{E}_g\right)$, and the lower barrier was ascribed to FL depinning or weak pinning at mid-gap. The analysis also revealed a large series resistance that attenuate the diodes current and due to the low barrier, it is suggested to be one of the major causes of diodes nonidealities. From the temperature dependent measurements, the barrier height and ideality factor were found to be strong functions of temperature leading to a non-linear Richardson plot. The observed anomalies were attributed to trap assisted current via dislocations. The I-V-T analysis suggested a dominance of TFE and TAT mechanisms across AlInSb/InSb Schottky diodes. However, TAT current overtakes TFE current at higher temperatures.

Finally, preliminary RF measurements have been carried out at 4 GHz. The measurements reveal the potential of using the AlInSb/InSb QW Schottky diodes as detectors at microwave frequencies, but the devices exhibited power dissipation through devices parasitics. However, additional investigations must be done to reduce the power loss through the device parasitics as well as to push the devices towards higher frequencies.

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ABBREVIATIONS

AFM	Atomic Force Microscopy
BEEM	Ballistic Electron Mission Microscopy
CPW	Co-Planar Waveguide
DEG	Dimensional Electron Gas
DUT	Device Under Test
GSG	Ground Signal Ground
FE	Field Emission
FET	Field Effect Transistor
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
I-V	Current Voltage
I-V-T	Current Voltage Temperature
MBE	Molecular Beam Epitaxy
MIGS	Metal Induced Gap States
mmW	Millimetre Wave
MS	Metal Semiconductor
QW	Quantum Well
RF	Radio Frequency
SBD	Schottky Barrier Diode
SEM	Scanning Electron Microscopy
TE	Thermionic Emission
TFE	Thermionic Field Emission
VNA	Vector Network Analyser

Chapter 1

Introduction

1.1 The Motivation for InSb Semiconductors for Electronic Devices.

The narrow-gap III-V compound semiconductors along with their related alloys are characterised by extremely high electron mobility and have amongst the narrowest band-gap energies of any known semiconductor. These properties have attracted device researchers towards the development of III-V based electronics for high-speed, low-power consumption applications, such as high electron mobility transistors (HEMTs)[1, 2]. Table 1-1 shows the electrical properties of a range of III-V semiconductors along with silicon and germanium for comparison. Among III-V compound semiconductors, Indium antimonide (InSb) has exceptional material properties with a dielectric constant of 16.8, the largest lattice constant (6.479 Å), the narrowest energy gap ($E_g = 170\ meV$), the smallest electron effective mass ($m_e^* = 0.13$), and the highest electron mobility at room temperature 78000 cm^2 /V. Due to these exceptional properties, InSb based materials have gained interest for the next-generation of high speed devices such as field effect transistors (FETs), and heterojunction bipolar transistors (HBTs)[5-7]. Furthermore, InSb has the highest reported electron saturation velocity, greater than $5 \times 10^7 cm/s,$ compared to $1 \times 10^7 cm/s$ and $4 \times 10^7 cm/s$ for GaAs, and InAs

Table 1-1 Selected electrical properties of a range of IV and III-V semiconductors for comparison.

System	Material	m_e^*/m_o	$\mu_e\ (cm^2/VS)$	$\mu_p\ (cm^2/VS)$	Band gap *(eV)*
IV	Si	0.188	1450	500	1.16
	Ge	0.038	3900	1900	0.74
III-V	GaN	0.15	400	10	3.5
	InP	0.079	4600	150	1.42
	GaAs	0.067	8000	400	1.519
	GaSb	0.042	5000	880	0.725
	InAs	0.24	33000	460	0.42
	InSb	0.013	78000	1900	0.235

respectively[8]. Theoretically, InSb channel HEMTs can achieve higher speed than GaAs and InAs channel HEMTs. Figure 1-1 illustrates the trend towards the use of narrow-bandgap semiconductors with higher lattice constant in high-speed, low-power devices, particularly HEMTs and HBTs. Among the Sb-based devices, InSb has the highest potential for the next generation of high-speed electronics. InSb has the smallest energy gap and the highest electron mobility resulting in higher speed and lower-power consumption[3, 4]. Recently, confinement of a two-dimensional electron gas 2DEG in a single InSb/AlInSb quantum well (QW) using the modulation doping technique[9] has resulted in increasing interest in the field of high-speed electronics due to the extra high electron mobility they can provide for these applications at a low level of noise. There has been growing interest during the last decade in the development of InSb/AlInSb-QW. Lately, the ultra-high-speed and the low-power consumption of FETs based on InSb/AlInSb-QW have exceeded those transistors made of other semiconductors, resulting in the core motivation for the study of this material system for future high-speed and low-power logic applications[10, 11]. However, InSb QW FETs still have many difficult challenges which must be overcome before they can be considered convenient for logic applications or for high frequency analogue applications.

Because of the extremely high room temperature mobility, Schottky diodes based on InSb are predicted to act as very high-frequency rectifiers. Electron mobilities as high as 78,000 $cm^2V^{-1}s^{-1}$ have been measured in intrinsic bulk material[12], and in excess of 50,000 $cm^2V^{-1}s^{-1}$ in InSb/AlInSb-QW material[13] affording high conductivity. These properties make InSb based material particularly suited to certain electronic

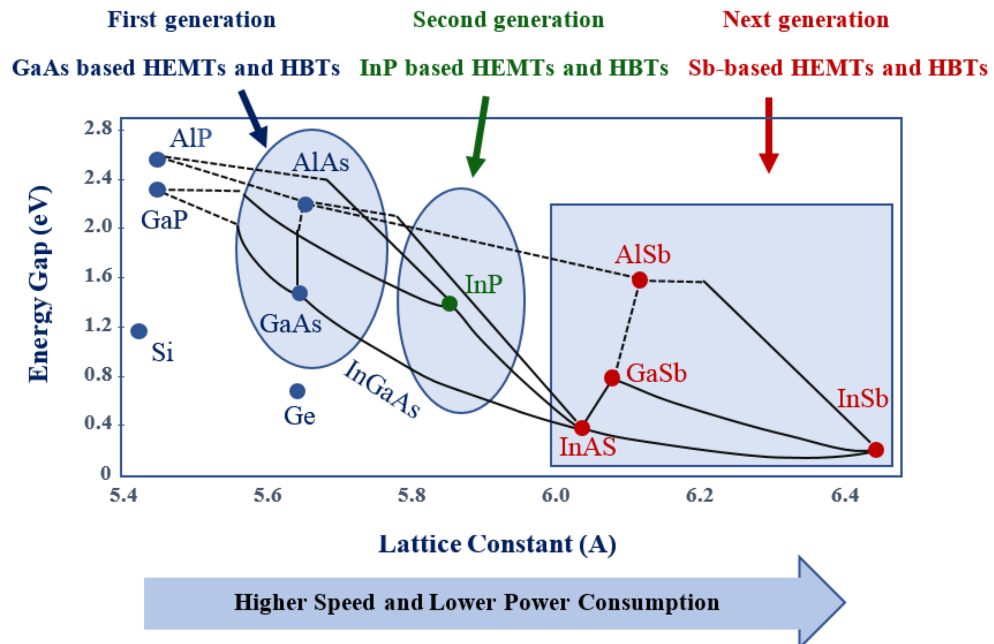

Figure 1-1 energy versus lattice constant diagram of selected semiconductors at room temperature, showing the trend of transistors toward larger lattice constants and narrower bandgaps for high speed application and low power consumption. Indium antimonide has the smallest energy gap and the largest lattice constant[3, 4]

applications and has allowed for the development of low voltage millimetre-wave (mmW) transistors[11].

Schottky diodes made from this material could have application in the recently emerged applications at millimetre-wave and sub-millimetre wave frequencies. There are numerous applications of mmW technology, such as poor-visibility sensing and medical and security imaging, in addition to communications applications operating at frequencies above 100 GHz. These new applications demand high-frequency low-noise devices; key areas in which InSb/AlInSb-QW Schottky diodes may excel, and could well rival the best reported backward diode devices for these applications[14]. Consequently, there is an increasing drive to investigate the ultimate performance obtainable from such devices that might enable technologies needed to address these rapidly expanding needs.

However, due to the challenging growth conditions, the progress in the understanding of InSb/AlInSb-QW materials is still at a quite immature stage compared to wider energy gap III-V semiconductors such as GaAs or GaN. So far, fabrication of

InSb/AlInSb-QW Schottky diodes remains challenging because of the high-density of dislocations within the $Al_xIn_{1-x}Sb$ buffer layer located between the QW and the substrate and the relatively low Schottky barrier heights obtainable. These difficulties can plague excessive leakage current and limit the breakdown properties. The electrical characterisation and investigation of state of the art InSb/AlInSb-QW Schottky diodes is the subject of this thesis.

1.2 Historical Perspective

Rectifying metal-semiconductor contacts are of substantial scientific and technical interest as they have lots of attractive properties and applicability to electronic, optoelectronic, and electrochemical devices. The first rectifying action in a metal-semiconductor contact was first reported in 1874 by the German physicist F. Braun[15, 16] while studying point contacts between thin metal wires and sulphide crystals such as lead sulphide, the so-called “cat’s whisker contact”. Subsequently, many substances such as Si and Ge were shown to exhibit the same rectification effect. Although the mechanism of conduction was unclear, practical experiments continued, but only to a limited extent, until 1887 when Hertz confirmed the existence of radio waves. Initially, these waves were detected using a device called a coherer, a loose contact that conducts when stimulated by RF currents, but due to the difficulty of use and poor sensitivity, there was a need for new detectors. In 1898 Braun[17] began his experiments on wireless communication and in 1901 was able to pick up wireless signals by using semiconductor rectifiers. By 1904 Sir J. Bose [18], another researcher in this field, was granted the first patent for a point metal semiconductor rectifier. The contact was made of a thin wire lightly touching a galena crystal for detecting radio signals. This invention made a jump in wireless engineering and opened the way for the transition from wired to wireless communication. After the invention of wireless communication, diodes have become more important, and significant experimental work continued to find and investigate new materials. The use of silicon in the world of communications appeared for the first time in 1906, where the American inventor G Pickard[19], who was interested in finding a new detector to receive the new wireless telegraphy messages, tried about 30,000 crystal combinations including silicon and galena and metallurgical grade silicon. Pickard was granted a patent for the first silicon rectifier in 1906. With

the emergence of silicon semiconductors, the scene was set for a substantial leap into the world of semiconductor technology. In 1915, the Swedish scientist C. Benedicks[17, 20], during his work on the properties of some rare materials, used germanium to manufacture point contact rectifiers using platinum and copper.

The first and most critical step towards understanding and clarifying the rectifying action of the MS contact was introduced by the German scientist W. Schottky et al. in 1931. The MS contact was later named the Schottky diode in his honour. The authors proved the formation of a potential barrier on the MS interface because of the voltage drop across the junction due to electrons flow from semiconductor to metal when contact is made. Afterward, in 1938, both Schottky[21] and Mott[22] presented independent explanations to the mechanism behind the potential barrier formation. They also proposed models to find the height and the shape of the barrier. These models were known as the Schottky barrier and Mott barrier; sometimes it is called the Schottky-Mott model. According to the Schottky-Mott model, the barrier height is equal to the difference between the metal work function and the semiconductor work function, and not considering the interfacial properties of the MS contact. Progress in our understanding of MS contacts was made by Bethe[23] in 1942, who introduced the theory of thermal emission as a mechanism for the transmission of electrons over the barrier. Unfortunately, experimental measurements showed a deviation from the Schottky-Mott rule, the barrier height for some semiconductors were found to be only a function of the semiconductor (i.e. independent of the metal work function). Many theories have been presented to clarify this observed deviation. Most of these theories involved the presence of interface states in the band-gap of the semiconductor that pins the Fermi level position at the MS interface. The first theory is known as “surface states theory” was presented by Bardeen[24] in 1947. According to this theory, the deviation in determining the barrier height was attributed to the existence of surface states resulting from the dangling bonds present at the semiconductor surface. After surface state theory, many varied and often ambiguous experimental studies emerged. The study of silicon contacts has shown an excellent matching to the Schottky model, in contrast for example to III-V semiconductors. The experimental results of Archer and Atalla[25] in 1963 on Au/Si contacts using cleaved silicon surfaces showed good agreement with the theory proposed by Schottky. Mead and Spitzer’s[26] study in 1964 on various metal-semiconductor systems using cleaved III-V semiconductor surfaces showed that

the Fermi level position at the surface is independent of the metal work function and it is nearly equal to one-third of the energy gap from the edge of the valence band. In the same year, Crowell, Sze, and Spitzer[27], with their study on Au/Si contacts, observed that the temperature dependence of the barrier height is the same as the temperature dependence of the silicon energy gap. They also demonstrated that the Fermi level at the metal-semiconductor junction is pinned relative to the valence band edge. These two findings were supported theoretically in 1965 by Cowley and Sze[28], with the conflict in the experimental results being attributed to the surface treatment applied to the semiconductor before metal deposition. Cowley and Sze derived a theoretical expression for the barrier height dependence of the metal work function, density of surface states, and the interfacial layer thickness. In the same year, the theory of 'metal-induced gap states' (MIGS), was introduced by Heine[29]. According to this theory, interfacial states are assumed to be formed due to the overlapping of the metal conduction band with the semiconductor energy gap. These gap states pin the Fermi level and control the properties of the MS junction, not the semiconductor surface states. This model was confirmed experimentally by Louie and Cohen[30] in 1976. Another important theory, 'unified defect model (UDM), was introduced by Spicer et al.[31] in 1979. He proposed the formation of native defects due to the metallization process, and the Fermi level to be pinned at discrete surface states of these defects. Instead of discrete defect levels, Hasegawa and Ohno[32] in 1986 presented the disorder induced gap states (DIGS) theory, assuming a continuum of surface states in the band-gap. It was proposed that these continuum states are induced due to a disturbance in the crystalline perfection of the semiconductor surface during the metallization.

Experimental and theoretical study of epitaxial MS contacts implemented by R.T Tung[33] in 1993 showed that any minor change in the interface structure leads to a variance in the barrier height by more than $\frac{1}{3}E_g$. This finding as suggested by Tung refers to the possibility of forming an inhomogeneous barrier on the non-epitaxial MS contacts as have been proven by several experimental studies. The presence of barrier inhomogeneity in polycrystalline contacts was first recognize in the 1980s in different studies[34, 35] and confirmed in 1999 by Fowell and co-workers[36], who spatially mapped Schottky barriers of Au/n-CdTe contacts on the nanoscale using ballistic electron emission microscopy (BEEM). In general, the local BEEM barrier heights of the polycrystalline interfaces were found to exhibit Gaussian distributions indicating

the formation of patches of increased and reduced barrier heights. In 2000, another theory emerged regarding Schottky barrier formation known as 'bond polarization theory' (R. Tung[37, 38]) which can account for the observation of barrier inhomogeneity at polycrystalline interfaces and the interface-structure dependency of Schottky barrier height at the single crystal interface. The polarization theory assuming an interfacial chemical interaction between the metal and the semiconductor results in charge re-distribution at the MS interface. Due to the polarization effect, the barrier formed is slightly dependent on the metal work function and the resulting polarized chemical bonds from this reaction are proved to be responsible for Fermi level pinning. For polycrystalline contacts, it is believed that an inhomogeneous interaction at the MS contacts results in an inhomogeneous barrier.

In fact, most of the early studies on Schottky barriers assume Fermi Level pinning at a unique position of the MS interface. Recent experimental and theoretical studies on epitaxial MS interfaces suggest that the Fermi level is not pinned and that the interface structure plays a vital role in shaping the Schottky barrier hight. Therefore, an examination of the degree of SBH variation at various MS interfaces may be a revealing test of SB models. Many of the observed anomalies in the SB experiments can be explained in terms of SBH inhomogeneity.

To conclude, the barrier height of Schottky diodes is a function of three components; semiconductor, metal, and the atomic interface structure. The manufacturing process has a vital impact on the contact properties, and surface defects can add more complexity to the atomic interface structure due to local disturbances occurring in the surface states. Adequate knowledge of the MS interface atomic properties can help a lot in understanding the Schottky barrier formation mechanism.

1.3 Thesis Outlines

The main goal of this thesis was to achieve a Schottky diode based on the AlInSb/InSb heterostructure. Hence, the work involves processing, characterization as well as current transport analysis. Devices characterization and analysis were based on current voltage (I-V) measurements taken over a wide range of temperatures. The motivation for this work along with the historical background have been presented in chapter one. The upcoming work in the thesis can be outlined as follows; *Chapter two* gives a brief

description of the basic physics of Schottky diodes, such as the theory of barrier formation, current transport mechanisms and ideality factor. The chapter also describes most of the common phenomena related to Schottky barrier formation such as surface states, Image force lowering, and interfacial layer formation. *Chapter three* describes the quantum well material used in this work as well as the diode fabrication process. The setups used for the I-V measurements and the temperature dependent current voltage (I-V-T) measurements are also described in this chapter. The room temperature analysis of the I-V measurements in the forward bias are investigated in *chapter four*. Several methods have been used in this chapter to analyse and extract the fundamental parameters of the fabricated Schottky diodes. All the methods used are based on modified versions of thermionic emission theory for a diode with high series resistance. The analysis of the I-V-T measurements, which is considered a useful tool in characterising the electron transport mechanisms in the MS contact are presented in *Chapter five*. Many models have been used to explain the abnormal behaviour in the Richardson plot as well as the high-temperature dependency of both ideality factor and barrier height. *Chapter six*, includes a preliminary assessment of using the InSb/AlInSb Schottky diodes as a rectifier at millimetre wave frequencies. The study includes designing, processing, modelling, as well as characterizing using DC and RF measurements. *Chapter seven* provides a summary and conclusions of the entire results obtained from the research. The thesis is completed with an appendix describing the photomasks that were designed and used in this study.

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Chapter 2

Metal-Semiconductor Contacts

2.1 Introduction

Metal-semiconductor (MS) contacts are of substantial scientific and technical interest due their attractive properties and their multiple applications in electronic, optoelectronic, and electrochemical devices. MS contacts can act either as a rectifying contact (a Schottky contact) or as a non-rectifying contact (an ohmic contact). The rectifying contact exhibits a nonlinear current-voltage characteristic when changing the polarity of the applied voltage (bias). It passes a current in the forward bias and blocks it in the reverse-bias which implies a high current resistance in the reverse-bias. The ohmic contact exhibits a linear I-V characteristic regardless of the applied voltage polarity. Such behaviour requires a low contact resistance that allows the current to pass easily and equally in both biasing directions[3]. Both contacts have an essential role in electronic devices performance[4]. This chapter considers the background physics of MS contacts, including the barrier formation mechanism, current transport mechanisms and some of the important phenomena that can alter the I-V characteristics of the contact such as interface states and image force lowering.

2.2 Ideal Metal Semiconductor Rectifying Contact

Based on the Schottky-Mott model, the energy band diagram for an MS contact on a n-type semiconductor with $\Phi_M > \Phi_S$ before contact is formed as is illustrated in Figure 2-1. Here, (Φ_M) and (Φ_S) are the metal and the semiconductor work functions (i.e. the amount of energy required to liberate an electron from the metal surface of the semiconductor to the vacuum level (E_o), an is equal to the difference between the Fermi and the vacuum levels measured in electron volts). The energy difference between the lower edge of the conduction band (E_C) and the vacuum level (E_o), is known as the semiconductor electron affinity (χ_s). The electron density distribution for the metal and the semiconductor are also shown in Figure 2-1. It can be clearly seen that the energies of the semiconductor electrons, due to the difference in Fermi levels, are higher than the energies of the metal electrons[5-7]. As the metal is connected to the semiconductor, the electrons begin to flow from the semiconductor to the metal until thermal equilibrium is reached and the Fermi levels of the metal and the semiconductor are aligned with each other. The electron flow creates a depleted region in the semiconductor as illustrated in Figure 2-2. The width of the negatively charged space charge region of the metal is negligibly small on this scale, due to the high density of

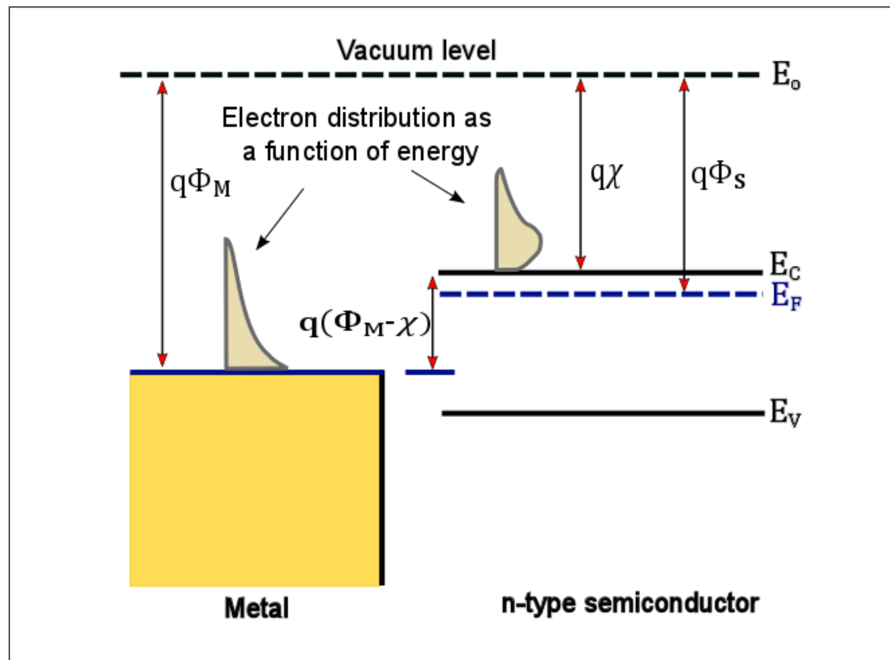

Figure 2-1 Schematic energy band diagram of metal-n type semiconductor contact before contact is made. Where $\Phi_M > \Phi_S$.

electrons in the metal compared to the semiconductor. At thermal equilibrium, the 'potential barrier' for electrons on the metal side can be determined from:

$$\Phi_B = \Phi_M - \chi \quad (2\text{-}1)$$

where (Φ_B) denotes the Schottky barrier height. However, electrons that move from the semiconductor to the metal face a similar barrier known as the "built-in potential" (V_{bi}). The built-in potential barrier is given by the difference between the metal and the semiconductor work functions as in the relation:

$$V_{bi} = \Phi_M - \Phi_S \quad (2\text{-}2)$$

The barrier formation process is illustrated in the energy-band schematic diagrams shown in Figure 2-2. The semiconductor work function (Φ_S) has the same expression as the metal work function but, it is a variable quantity due to the variation of the Fermi level with the doping density[7, 8]. It is worth mentioning that interface states and barrier lowering are not considered in ideal contacts. The shape of the formed barrier can be determined from the charge distribution in the space-charge region. Generally,

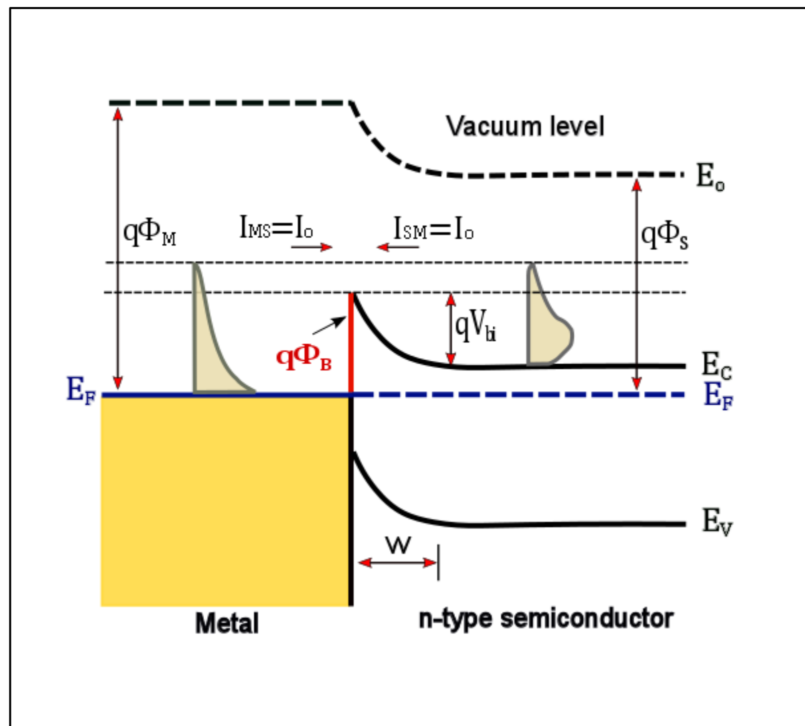

Figure 2-2 Schematic energy band diagram of metal n-type semiconductor after contact is formed. (Vbi) is the built-in voltage across the semiconductor depletion region at thermal equilibrium, $qV_{bi} = q(\Phi_M - \Phi_S)$. *W is the width of the depletion region.*

the barrier height is higher than the thermal voltage q/kT and the space-charge region of the semiconductor depleted from mobile carriers and turn out into a high resistivity area. The original analysis by Schottky assumed a uniformly doped semiconductor, hence the charge density at the depletion region will be uniformly distributed. The linear increase of the electrical field strength in this space-charge region with increasing distance, approaching the edge of the space-charge region, forms a parabolic barrier Schottky contact.

2.3 Forward and Reverse Bias

At thermal equilibrium, Figure 2-3 the current (I_{MS}) resulting from the transition of electrons from the metal to the semiconductor is equal to the current (I_{SM}) resulting from the transmission of electrons from the semiconductor to the metal. Hence, the net current passing through the contact is zero.

The MS contact becomes forward biased when a negative voltage ($-V$) is applied to the n-type semiconductor with respect to the metal as shown in Figure 2-3 (a). Under this bias condition, the width of the depletion region is decreased and the value of the built-in potential decreases from its value at thermal equilibrium (qV_{bi}) to a value of

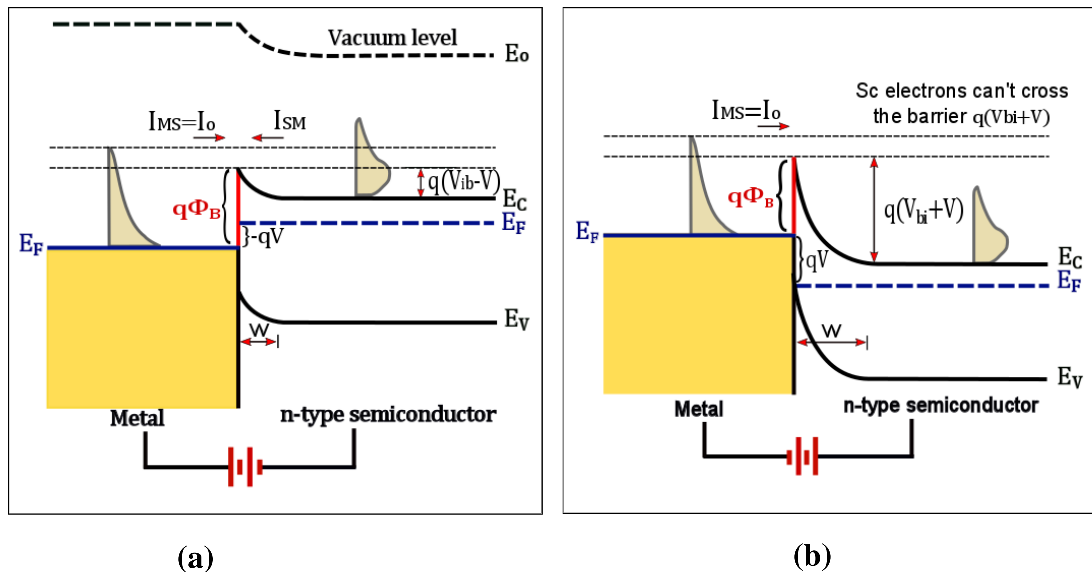

Figure 2-3 Schematic energy band diagrams of a rectifying metal n-type semiconductor contact under (a) forward bias and (b) reverse bias

$q(V_{bi} - V)$. Due to the barrier reduction, more electrons can easily flow from the semiconductor into the metal. The I_{SM} current increases exponentially above its value at thermal equilibrium (I_o) according to the relation $I_{SM} = I_o \exp(\frac{V}{V_T})$. The term ($V_T$) represents the thermal voltage (equal to kT/q), where the terms (k, T and q) represent the Boltzmann constant, temperature in Kelvin, and electron charge respectively. The Schottky barrier height Φ_B remains constant with bias, and the value of I_{MS} remains the same as its thermal equilibrium value I_o. Therefore, the net current flow (I) across the contact in the forward bias can be expressed by the relation:

$$I = I_{SM} - I_{MS} = I_o \exp\left(\frac{V}{V_T}\right) - I_o = I_o \left[\exp\left(\frac{V}{V_T}\right) - 1\right] \qquad (2\text{-}3)$$

In this case, the increase in the built-in potential prevents the flow of electrons from the semiconductor to the metal. The contact is under revers bias when a positive voltage (V) is applied to the n-type semiconductor with respect to the metal as shown in Figure 2-3 (b). Under the reverse bias condition, the width of the depletion region is increased and the value of the built-in potential increases from its thermal equilibrium value (qV_{bi}) into $q(V_{bi} + V)$. Therefore, the barrier height facing the electrons moving from the semiconductor to the metal increases. A bias of a few hundred millivolts would be adequate to stop electron transport from the semiconductor into the metal as the electron density distribution as shown in Figure 2-3 (b) is lower than the barrier, $q(V_{bi} + V)$. Therefore, the current I_{SM} resulting from the electrons flow from the semiconductor into the metal becomes zero. However, the current I_{MS} flow from the metal to the semiconductor remains unchanged from the I_o value as the Schottky barrier height Φ_B remains constant. Therfore, the MS contact with a positive barrier height has a noticeable rectifying behaviour, conducting a large current under forward bias, while almost blocking the current under reverse bias

2.4 Ideal Metal Semiconductor Ohmic Contacts

The energy band diagrams for MS contacts on n-type semiconductors with $\Phi_M < \Phi_S$ are shown in Figure 2-4 in four different cases. Figure 2-4 (a) illustrates the metal and the semiconductor band diagram before contact is made. After the MS contact is formed, the electrons begin to flow from the metal to the semiconductor until thermal equilibrium is reached and both of their Fermi levels are aligned. Transmission of the electrons will result in a positive charge on the metal surface and the accumulation of

electrons in a layer on the semiconductor side as shown in Figure 2-4 (b). Therefore, the current is only limited by the resistance of the bulk region of the semiconductor as there is no depletion layer. A small bending in the conduction band over a short distance would be sufficient to accommodate many electrons. Therefore, when the contact is forward biased the electrons can flow easily from the semiconductor to the metal while in the revers bias any small applied voltage will help the electrons to overcome the small barrier and flow from the metal to the semiconductor. The energy band diagram of the forward and the reverse bias conditions are shown in Figure 2-4 (c, d). Such an MS contact is called an ohmic contact as it is conducting in both directions with near linearity in response.

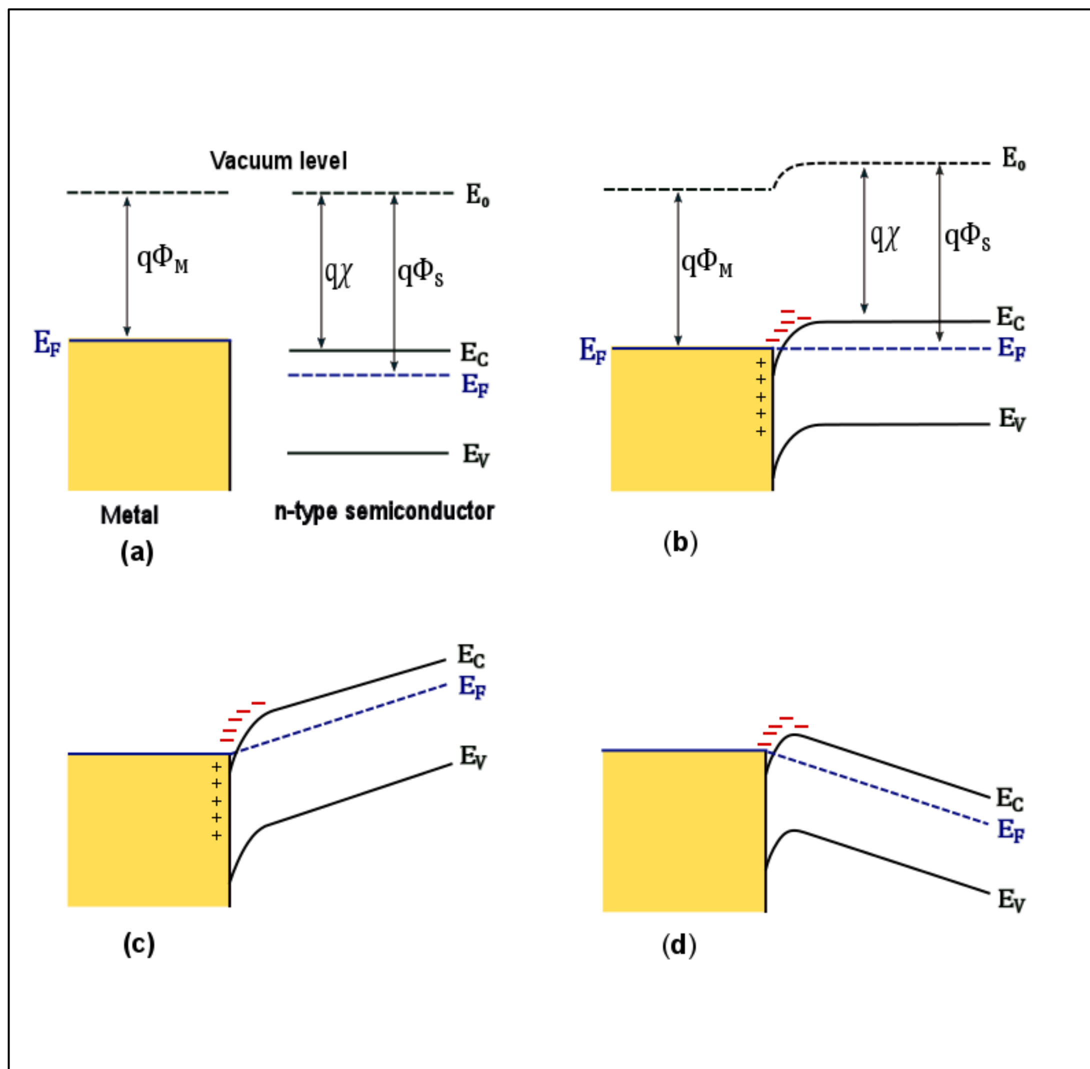

Figure 2-4 Energy band diagrams of an ohmic metal n-type semiconductor, $\Phi_M < \Phi_S$. (a) before contact, (b) after contact, (c) forward bias, and (b) reverse bias.

Ohmic contacts can also be formed even when $\Phi_M > \Phi_S$ by using a heavily doped semiconductor. Increasing the doping density for the semiconductor reduces the depletion region and thus enhances the tunnelling current through the barrier to form an ohmic like contact or what is called the transparent Schottky where the current across the barrier is dominated by tunnelling mechanism rather than thermionic emission[5-7].

2.5 Current Mechanisms in Schottky Contacts

The current flow across a Schottky barrier is due to carriers moving from the semiconductor to the metal and vice-versa. In forward bias, the current transport can occur in four basic mechanisms shown in Figure 2-5: (A) thermionic emission (TE) of electrons over the barrier; (B) quantum-mechanical tunnelling through the barrier; (C) carrier recombination in the depletion region; and (D) carrier recombination in the neutral part of the semiconductor. The ideal case of a Schottky diode assumes purely thermionic emission current. The contribution of the other current mechanisms leads to a departure from ideal behaviour [6, 7].

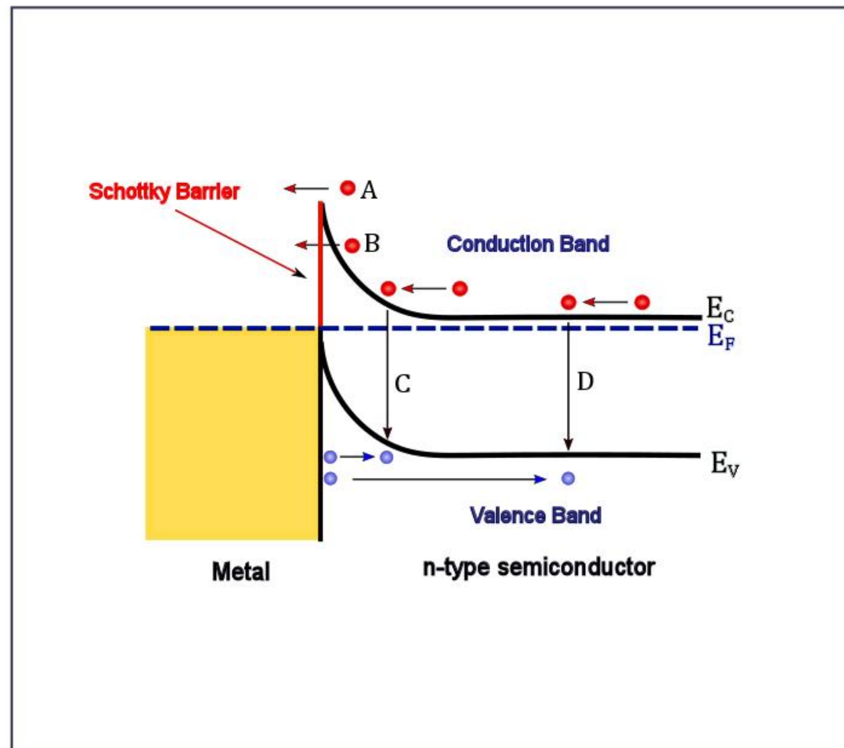

Figure 2-5 Current transport mechanisms across Schottky diodes in the forward bias; (A) thermionic emission, (B) tunnelling, (C) carrier recombination in the depletion region, (D) hole injection from the metal.

For moderately doped semiconductors, the thermionic emission is the dominant current mechanism at room temperature, while quantum mechanical tunnelling dominates at low temperatures as well as with heavily-doped semiconductors. In a given junction, a combination of all four mechanisms could exist, but typically only one current mechanism dominates.

2.5.1 Thermionic Emission Mechanism

For moderately doped semiconductors, thermionic emission TE is supposed to be the dominant current flow mechanism across Schottky contacts. According to TE theory, only charge carriers that have energies higher than the potential barrier can overcome the barrier and generate the diode current. The ideal I-V characteristics of a Schottky diode can be well described by equation (2-4)[6, 9]

$$I = I_o \left[exp^{\left(\frac{qV}{KT}\right)} - 1 \right] \tag{2-4}$$

where, (I_o) is the saturation current

$$I_o = AA^{**}T^2\, exp^{\left(\frac{-\Phi_B}{KT}\right)} \tag{2-5}$$

The symbol (A^{**}) is referred to as the Richardson constant and is given by:

$$A^{**} = \frac{4\pi q k^2}{h^3} \frac{m_n^*}{m_o} \tag{2-6}$$

By substituting for the value of each constant in equation (2-6) we get,

$$A^{**} = 120\, m^* \frac{A}{cm^2 k^2} \tag{2-7}$$

The Richardson constant is a function of the semiconductor material which depends on the ratio of the electron effective mass (m_n^*) to the actual rest electron mass in vacuum (m_o). The ideal current voltage curve according to TE model is shown in Figure 2-6. It is apparent that the diode current increasing exponentially in forward bias while in the reverse bias the current saturates at I_o when (V_R) is greater than the thermal energy by nearly four times, $V > 4\frac{q}{kT}$. For an ideal diode, a semi-log of the current-voltage plot should result in a straight line with a slope of unity as it is illustrated in the inset plot.

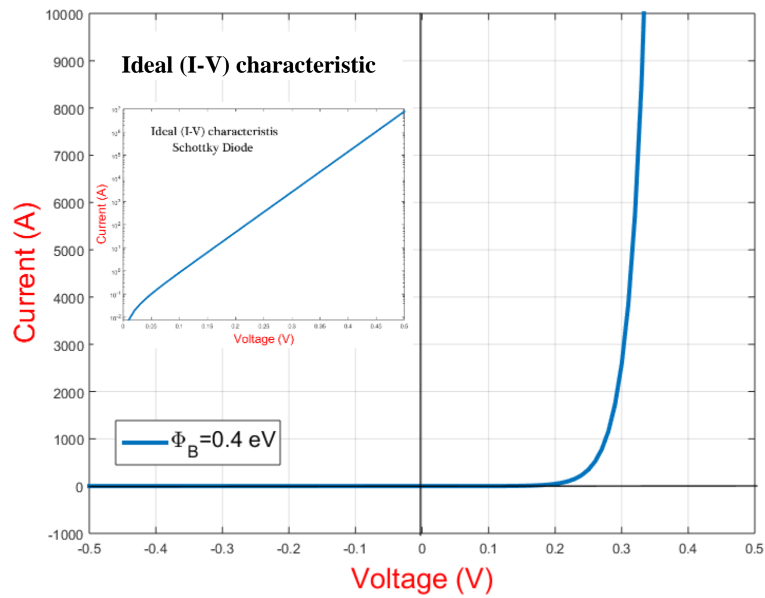

Figure 2-6 An ideal current-voltage characteristic which has been generated based on thermionic emission model. The inset plot represents the I-V curve on a semi-log scale.

2.5.2 Tunnelling Mechanism

Electrons with energies less than the barrier height can pass through the barrier by quantum mechanical tunnelling. Quantum tunnelling occurs in heavily doped semiconductors where the Fermi level lies above the bottom of the conduction, and the potential barrier is, as a result, extremely thin. The tunnelling can occur in both forward and reverse bias directions as illustrated in Figure 2-7. At low temperatures, the forward bias current is due to the tunnelling of electrons with energies at the Fermi level. Such a mechanism is known as field emission (FE). If the temperature is raised, a significant number of electrons can gain energies above the Fermi level, and the tunnelling probability increases as the electrons are presented with a thinner barrier. The tunnelling mechanism due to thermally excited electrons is called thermionic field emission (TFE). Due to the rapid decrease in the density of electrons above the Fermi level and the decrease in the barrier thickness, the tunnelling probability increases with increasing temperature until it reaches a maximum value at a certain energy level (E_m). Any further raise in temperature leads to decrease TFE gradually until it becomes negligible whereas the TE begins to dominate as a result of increasing the number of thermally

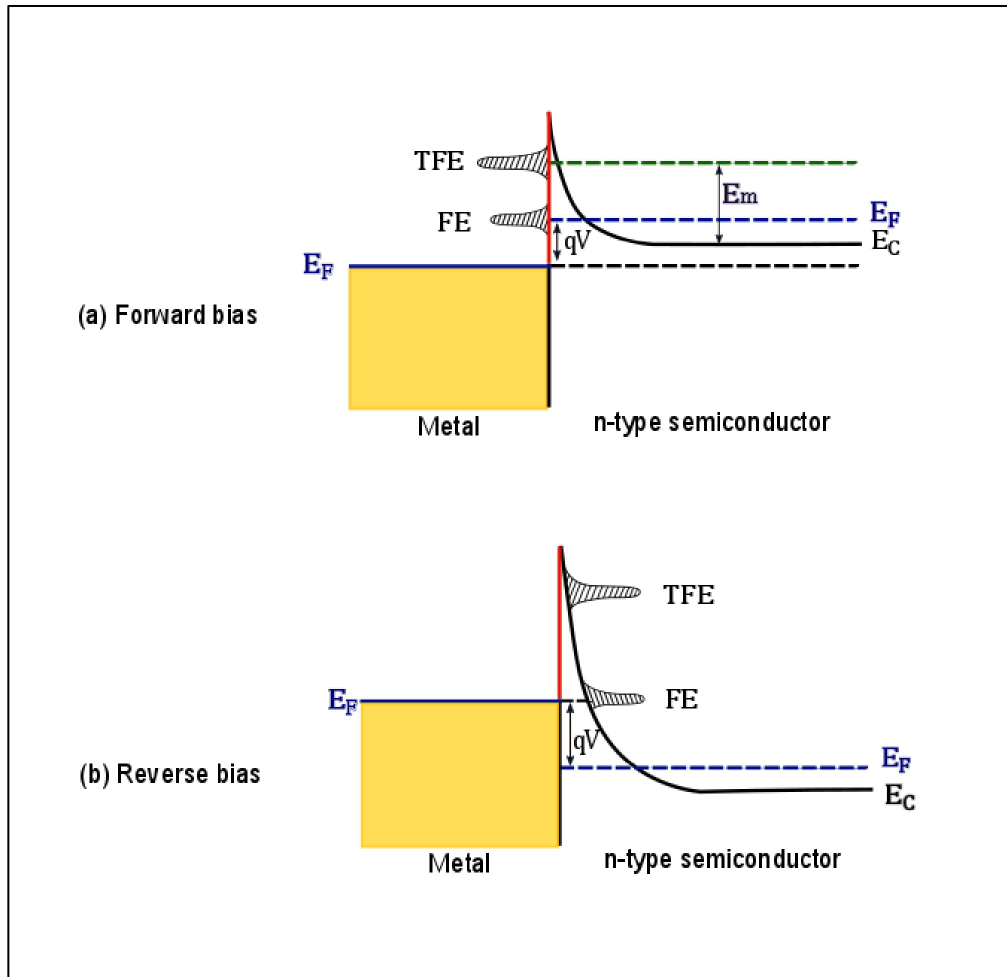

Figure 2-7 Field emission FE and thermionic emission TFE tunnelling through a Schottky barrier based on heavily doped n-type semiconductor. (a) forward bias and (b) reverse bias. (After Padovani and Stratton[1]).

exited electrons capable of crossing over the barrier[6, 7]. For moderately doped semiconductors, quantum-mechanical tunnelling is only expected in reverse-bias in the form of TFE mechanism at the top of the barrier where the barrier width gets thinner and thinner with the applied voltage.

The mathematical expression of the tunnelling current has been derived by Crowell and Rideout[10]. They extended the thermionic model for I-V characteristics given by equation (2-4 to include the tunnelling current as

$$I = I_o \exp\left(\frac{qV}{E_o}\right) \tag{2-8}$$

where the tunnelling probability (E_o) is given by

$$E_o = E_{oo} \coth\left(\frac{E_{oo}}{kT}\right) \tag{2-9}$$

The tunnelling parameter (E_{oo}), is an energy constant which is related to the material and can be calculated from the expression

$$E_{oo} = \frac{qh}{4\pi}\left(\frac{N_d}{m^* \epsilon_s}\right) \tag{2-10}$$

where (h) is Planck's constant, (ϵ_s) is the semiconductor permittivity, and (N_d) is the donor concentration express in m^{-3}. The value of the saturation current I_o depends on several factors, namely the barrier height, temperature and semiconductor properties, as well as being weakly dependent on the applied voltage. The energy constant E_{oo} can be used to determine the contribution of thermionic emission and tunnelling. At low temperature, the energy constant E_{oo} has a high value, therefore $kT/qE_{oo} \ll 1$, and $E_o \cong E_{oo}$, and so the slope of the semi-log plot of the current against the voltage is independent of temperature. This case refers to FE. At high temperature, E_{oo} has a low value, therefore $kT/qE_{oo} \gg 1$, and $E_o = kT$. Therefore, the slope of the semi-log plot of current-voltage curve is equal to q/kT. This case refers to TE. At intermediate temperatures, $E_{oo} \cong kT$, though $kT/qE_{oo} \cong 1$ and the slope of the semi-log plot can be written as

$$\eta = \frac{E_{oo}}{kT} \coth\left(\frac{E_{oo}}{kT}\right) \tag{2-11}$$

This case is where the TFE current dominates. This model provides a smooth transition from TFE into pure FE. The most important result of their study was that FE occurs only in heavily doped semiconductors and that the relationship can predict the I-V characteristics at low voltages.

2.5.3 Generation and Recombination Mechanisms

Generation and recombination of an electron-hole pair in the depletion region can contribute to the main current component of a Schottky diode. At thermal equilibrium, the rate of the generated electron-hole pairs is equal to the rate of their recombination. Thus the net current is zero where the number of generated electron-hole pair is equal to (n_i^2). The rate of generation departs from (n_i^2) when applying voltage to the barrier. A net generation current or a net recombination current will be formed depending on

the bias direction. If a reverse bias is applied to the Schottky barrier (on the assumption of n-type semiconductor), the rate of electron-hole pair generation increases in the depletion region. These pairs will be injected out of the depletion region under the effect of the electric field across the barrier producing the reverse current component. When the diode is forward biased, the electrons will flow out from the neutral bulk semiconductor to the depletion region and the holes will flow out from the metal. Electrons will recombine with holes because of their accumulation in the depletion region forming a forward recombination current component. Recombination also occurs by localised centres such as deep trap centres that have energies near the mid-gap which are most effective. The generation recombination current (I_{rg}) in the depletion region is given by the relation:

$$I_{rg} = I_{ro}\left[\exp\left(\frac{qV}{2kT}\right) - 1\right] \qquad (2\text{-}12)$$

where

$$I_{r0} = \frac{qn_iW}{2\tau_o}$$

and (W) is related to the thickness of the depletion region, and (τ_o) is the carrier lifetime in the depletion region. Therefore, the total current across the Schottky diode is giving by

$$I = I_{TE} + I_{rg} = I_o\left(\exp\left(\frac{qV}{kT}\right) - 1\right) + I_{ro}\left(\exp\left(\frac{qV}{2kT}\right) - 1\right) \qquad (2\text{-}13)$$

In some Schottky diodes, the recombination current is responsible for the non-ideality in the forward bias, where $\eta > 1$. The generation current is a common cause of the unsaturated current in reverse bias. The ratio between the two saturation currents (I_{ro}/I_o) is given by

$$\frac{I_{gr}}{I_o} = \frac{qn_i}{A^*T^2}\left(\frac{W}{2\tau_o}\right)\exp\left(\frac{\Phi_B}{kT}\right) \qquad (2\text{-}14)$$

According to this relation, the generation-recombination current is more critical in diodes with high barriers based on lightly doped semiconductors (i.e., large values of W) and it is more noticeable at low temperatures as it’s activation energy is less than the activation energy of TE.

2.6 Non-Ideal Characteristics of Schottky Diodes

Experimentally, most of the I-V characteristics of Schottky diodes deviate from the ideal case of the TE model in both forward and reverse-bias conditions. The thermionic I-V model must be modified to fit the experimental data. A factor (η) which is known as 'ideality factor' has been introduced to the exponential term of the ideal Schottky diode equation (2-4 as in the following expression[6, 7]

$$I = I_o \left[exp^{\left(\frac{qV}{\eta KT}\right)} - 1 \right] \tag{2-15}$$

For an ideal MS contact which assumes a pure thermionic current, the ideality factor takes a value of unity, $\eta = 1$. Many factors can increase the ideality factor beyond unity. Some of these factors are due to the contribution of other current mechanisms such as tunnelling and generation recombination to the diode total current. Other factors are attributed to the bias-dependence of the barrier height and image-force effect[6, 7]. According to the inhomogeneous barrier theory, Tung ascribed the high value of η to the presence of a wide distribution of low-SBH patches formed at a spatially inhomogeneous MS interface[11-13]. The variation of I-V characteristics with increasing ideality factor in the forward bias is illustrated in Figure 2-8. It is apparent that the current density reduces as the ideality factor increases.

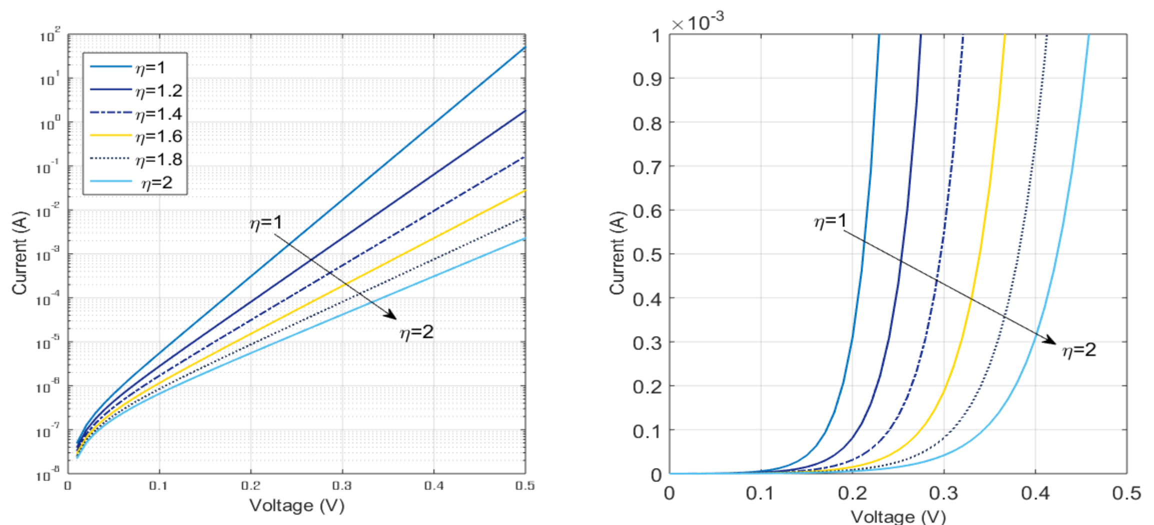

Figure 2-8 Simulated I-V characteristics in the forward bias at different values of ideality factor in (a) semi-log scale and (b) normal scale. Considering $\Phi_B = 0.3\ eV$, and $A^{**} = 1.68\ A\ cm^{-2}K^{-2}$.

Another Non-ideality can be in the reverse bias where the current in the reverse-bias keeps increasing and doesn't saturate at I_o. The Unsaturated current in the reverse bias is usually explained by two main effects. The first effect is the barrier lowering, whether resulting from the image force effect or the presence of a thin interfacial layer between the metal and semiconductor. Quantum mechanical tunnelling (FE and TFE) is the second reason for the excessive increase in leakage current with applied voltage. At moderate reverse bias, the potential barrier becomes sufficiently thin so that the electrons can tunnel into the semiconductor before reaching the top of the barrier. The contribution of barrier lowering and tunnelling current to the reverse bias current can be extremely high in some semiconductors as illustrated in Figure 2-9.

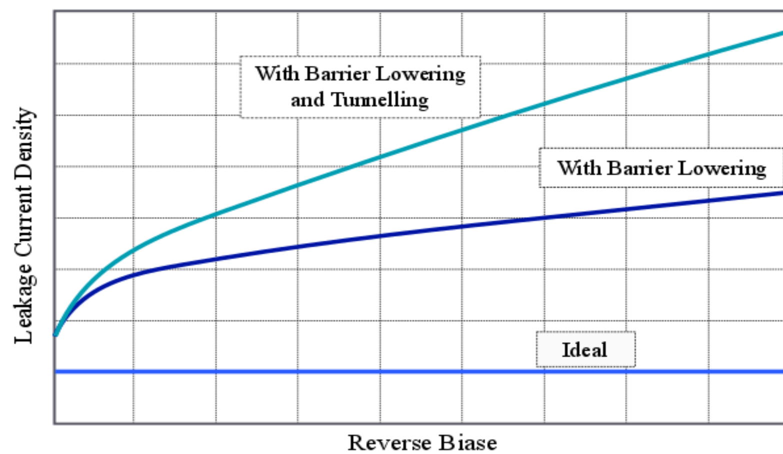

Figure 2-9 Effects of the barrier lowering and quantum mechanical tunnelling on the reverse I-V characteristics of the Schottky diode.

2.7 Modifications to the Barrier Potential

So far, it has been assumed that the height of the Schottky barrier remains constant over any applied voltage conditions. However, it has been found that the barrier height can be a bias dependent function in both forward and reverse bias conditions. In some practical diodes, the barrier height reduces due to the high electrical field (ξ) at the semiconductor surface[7]. The bias dependence of the barrier height is more important in the reverse bias direction than in the forward bias where the reverse current will not saturate and keeps increasing until breakdown.

The bias-dependent barrier height can be attributed to three main effects; image-force lowering; interfacial layer; and metal induced gap (MIG) states. All these effects predict

that Φ_B should be a decreasing function of the electrical field strength(ξ) at the junction. Since the electrical field strength is higher in the reverse bias and it is an increasing function of the reverse voltage, this causes Φ_B to decrease with increasing the reveres bias. Therefore, the backward current will keep increasing following the expression, $\exp\left(\frac{q\Delta\Phi_B}{kt}\right)$.

2.7.1 Image-Force Lowering

In a metal-semiconductor contact, the injection of an electron from the metal to the semiconductor induces an equal positive image charge inside the metal. The induced positive image charge tends to pull back the electron into the metal with a Coulomb attraction force $(q^2/(4\pi\varepsilon_s(2x)^2 = q^2/16\pi\varepsilon_s x^2)$, where (x) is the distance between the electron and the surface, and (ξ_{IF}) is the corresponding electrical field of the two particles due to the attraction force which can be expressed as in equation (2-16, where, (ε_s) is the semiconductor permittivity.

$$\xi_{IF}(x) = -\frac{F_{(x)}}{q} = -\frac{q}{16\pi\varepsilon_s x^2} \tag{2-16}$$

The equivalent potential energy of the electric field equals:

$$V_{IF}(x) = -\int_x^{\infty} \xi_{IF}(x)\, dx = -\frac{q}{16\pi\varepsilon_s x} \tag{2-17}$$

The resultant image potential energy must be combined with the potential energy of the Schottky barrier, the potential inside the depletion region, and is assumed to be constant near the surface with a maximum value (ξ_{max}):

$$\xi_{max} = \sqrt{\frac{2qN_d(\Phi_B - E_{CF} + V_a)}{\varepsilon_s}} \tag{2-18}$$

Therefore, in the presence of an external uniform electrical field (ξ_{max}), the total electrostatic potential $\Phi(x)$ at any distance (x) from the metal semicomductor interface is given by

$$\Phi(x) = -q\xi_{max} - \frac{q^2}{16\pi\varepsilon_s x} \tag{2-19}$$

The maximum barrier height occurs at distance (x_m) from the metal semiconductor interface, where the electrostatic field of the image charge force and depletion region cancel each other. This is illustrated in Figure 2-10 and is described by

$$\frac{q}{16\pi\varepsilon_s x_m^2} = \xi_{max} \tag{2-20}$$

Correspondingly, the maximum barrier potential reduction can be given by

$$\Delta\Phi_{\mathrm{B}} = x_m\xi_{max} + \frac{q}{16\pi\varepsilon_s x_m^2} = 2x_m\xi_{max} \tag{2-21}$$

Based on equations (2-18)and (2-21), it is clear that the barrier reduction depends on the applied voltage, semiconductor dielectric constant, doping concentration of the semiconductor (N_d), and the difference between the Fermi level and the edge of the conduction band of the semiconductor. Hence, the saturation current of the thermionic emission becomes bias dependent and the reverse bias current will not saturate[7, 14].

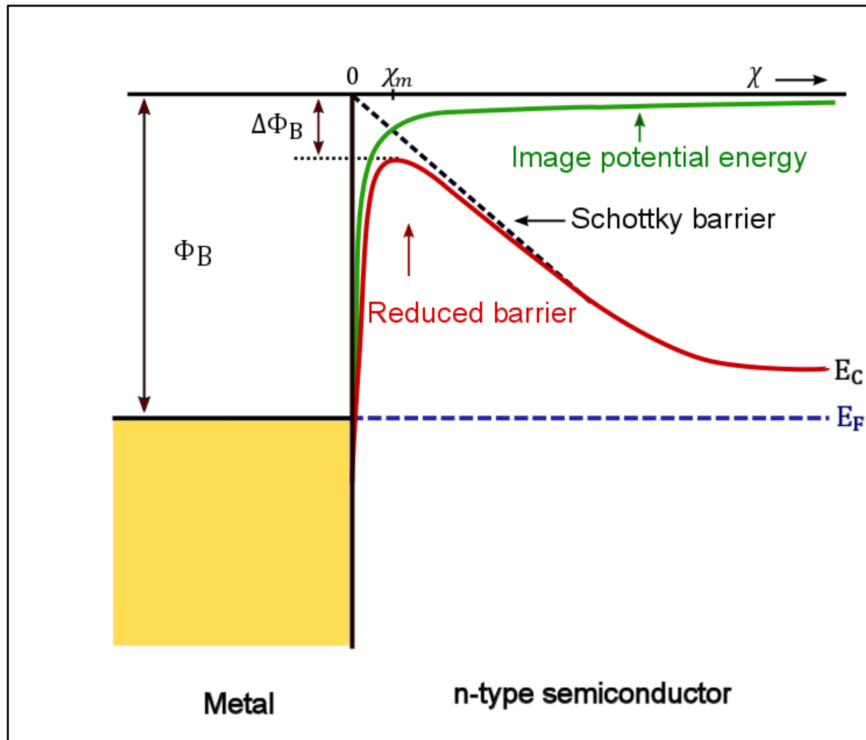

Figure 2-10 Energy band diagram illustrating the Schottky barrier lowering due to the image force effect.

2.7.2 Interfacial Layers

Most real-world compound semiconductor Schottky diodes have an interfacial oxide layer of 10-30 Å thickness, sandwiched between the metal and the semiconductor. Formation of oxide layers on the semiconductors surface is attributed to air exposure (and are very often humidity driven). The interfacial oxide layer in MS contact acts as an insulator layer which can alter the diode performance. The energy band diagram of MS contact in the presence an insulator layer is illustrated in Figure 2-11. It is apparent that the insulator layer has altered the energy band diagram and affects the Schottky diode performance. Both barrier height and ideality factor can be affected by this layer in different ways. In the presence of the insulator layer, an electrical field (ξ) in the semiconductor alters the potential (V_i) across the insulator layer and modifies the barrier height. Due to voltage drop across the insulator layer, the Schottky barrier height at zero bias is lower than it would be without the interfacial layer. Hence, the barrier height in the presence of an interfacial layer can be expressed as:

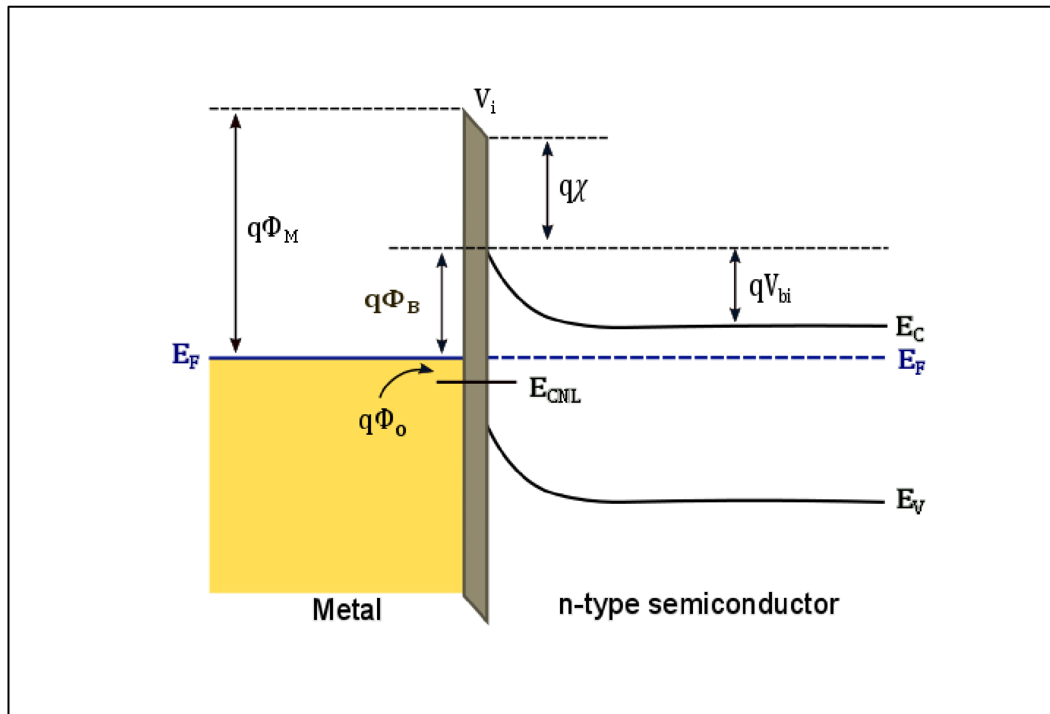

Figure 2-11 Energy band diagram of metal-semiconductor contact with a very thin insulating interfacial layer at forward bias.

$$\Phi_B = \Phi_M - x - V_i \tag{2-22}$$

The barrier reduction in term of the electric maximum electric field (ξ_{max}) in the semiconductor can be written as

$$\Phi_B = \Phi_B^0 - \alpha\xi_{max} \tag{2-23}$$

Where (Φ_B^0) is the barrier height at zero bias, and

$$\alpha = \frac{\delta\epsilon_s}{\epsilon_i + q\delta D_s}$$

The barrier height reduction depends on the maximum electric field (ξ_{max}) in the semiconductor and this expression is valid for any applied voltage if the density of the interface states (D_s) remains constant over the entire energy. It is also obvious that the barrier reduction is higher for interfacial layers with a low dielectric constant (ϵ_i).

The interfacial layer acts as a tunnel barrier and is assumed to be very thin such that it does not restrict the current flow at low forward voltages until a certain voltage where it will start to restrict the current flow. This behaviour leads to a higher ideality factor η for the Schottky diode. Experimental results show increasing values of η with increasing oxide thickness. Interfacial layers of 20 Å usually raise the value of η to a range of $1.3 - 1.5$. With applying a forward bias, the depletion zone begins to decrease and consequently both the electric field and the voltage drop decrease across the insulating layer causing a variation in the barrier height with the applied voltage ($\frac{\partial\Phi_B}{\partial V}$) . This variation is expressed in terms of the ideality factor given by

$$\eta^{-1} = \left(1 - \frac{\partial\Phi_B}{q\partial V}\right) \tag{2-24}$$

Thus, η is bias independent only if the oxides energy states at the semiconductor-oxide interface are uniformly distributed. In the reverse bias condition, the reduction in the barrier height in the presence of an insulator layer leads to prohibiting the saturation of the reverse current. Due to the barrier height reduction, the reverse current for diodes with a thicker insulating layer can be higher than that in diodes with an ultra-thin layer. In this case, the electrons must tunnel through the insulating barrier, but the effect of the barrier reduction is more prominent.

2.7.3 Surface States

Experimentally, the barrier height Φ_B has been found to be a less sensitive function of the metal work function Φ_M than equation (2-2) would suggest. This weak dependence on Φ_M was first explained by Bardeen who attributed this discrepancy to the existence of a high density of surface states at the semiconductor surface. For MS contacts possessing a high density of surface states, the Fermi level position is believed to be pinned at some level within the band gap of the semiconductor and became independent of Φ_M. Surface states arise from dangling bonds at the semiconductor surface due to the interruption of the crystal periodicity. These energy states can be occupied or empty depending on their position with respect to the Fermi level. The surface states are characterized by a neutral level ($q\Phi_o$) or what is called charge neutral level (CNL) (measured from the edge of the valence band) as shown in Figure 2-12. If the energy states are occupied to an energy level above $q\Phi_o$, the surface would be negatively charged, and the surface states act as acceptors. Also, when the energy states are occupied to an energy level below $q\Phi_o$, the surface would be positively charged and

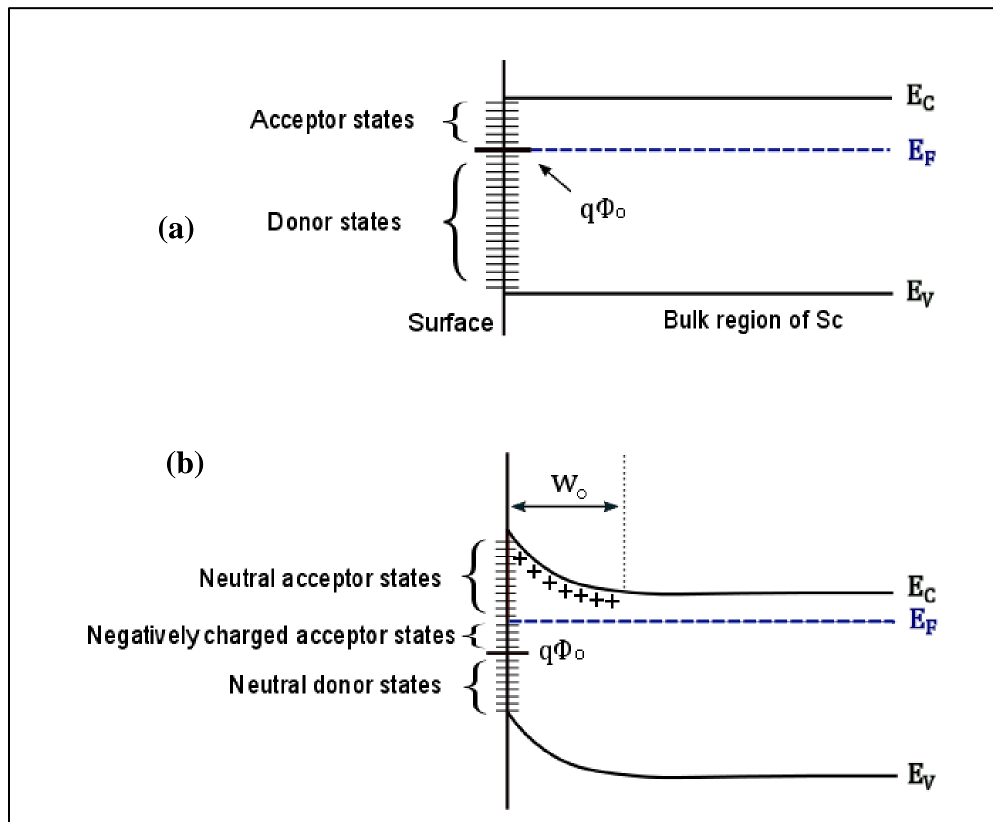

Figure 2-12 Energy band diagram showing the surface states distribution inside the band gap at the semiconductor surface (a) The neutral level coincides with Fermi level. (b) n-type semiconductor, the neutral level is below Fermi level.

the surface states act as donors[5, 7, 15]. The barrier height will be increased or reduced depending on the location of the charge-neutral level to the Fermi level. If the charge neutrality level $q\Phi_o$ is located above the Fermi level the surface states behave as acceptors and reduces the downward band bending. While, if the $q\Phi_o$ is located below the Fermi level, the surface states behave as donors and increases the downward band bending. Accordingly, the Fermi level is pinned at the surface by the surface states around the neutral level. Thus, the formed barrier height leaves the ideal Schottky-Mott model and can be reformed as in the expression:

$$q\Phi_B = E_g - q\Phi_o \qquad (2\text{-}25)$$

The location of the charge-neutral level to the valence band is a function of the semiconductor and its surface states. Generally, the charge-neutral level is found to be located at one-third of the energy gap ($1/3E_g$), pinning the barrier heights of the electrons around 0.75 eV and holes around 0.37 eV[16]. When the donor level is located far away from the conduction band, it is referred to as a deep donor level. Correspondingly, when the acceptor level is located far away from the edge of the valence band it is referred as a deep acceptor level. These are different from shallow donor and shallow acceptor levels when they are close to the edges of the conduction and the valance bands respectively[5]. For n-type semiconductors such as silicon and GaAs, the charge-neutral level ($q\Phi_o$) is around one third of the bandgap. Therefore, the value of Φ_B is independent of (Φ_M) and it is approximately equal to two thirds of the energy gap for n-type semiconductors as illustrated in Figure 2-13. Thus, the barrier

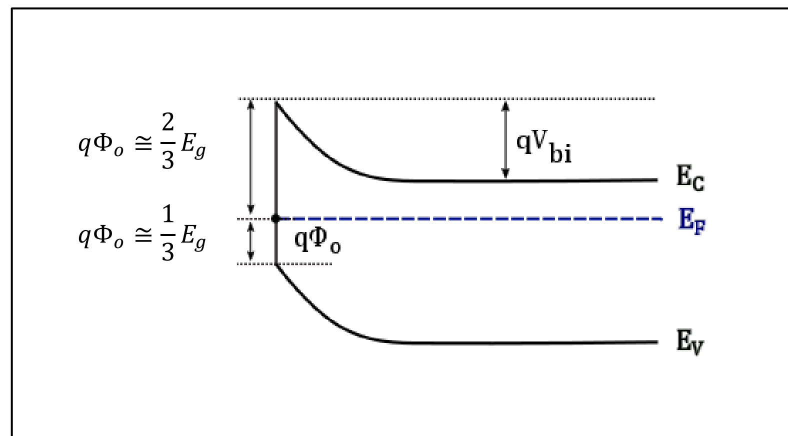

Figure 2-13 Energy band diagram of illustrating Fermi level pinning at MS contact on n-type semiconductor with high density of surface states.

height Φ_B is always high in n-type semiconductors. However, Φ_B is always low in p-type semiconductors. Experimental measurements of Schottky barrier heights on III-V semiconductors, which have a high density of surface states (i.e., $D_{ii} = 10^{13}\ states/cm^2eV$)[17], showed good agreement with this assumption. It is expected for MS contacts, based on n-type semiconductors, to form rectifying contacts regardless of the metal work function.

2.7.4 Metal-Induced Gap States (MIGS)

Surface states present at the MS interface with an interfacial layer of high defects density have been assumed to be the primary cause for Fermi level pinning. However, Fermi level pinning has also been observed at intimate MS interfaces. According to the surface states theory of Heine[18], the surface states at an MS contact does not relate to the semiconductor alone but should be the result of the interaction between the metal and the semiconductor surface. He proposed that the wavefunction of the metal electron, with energies equivalent to the forbidden gap of the semiconductor, would decay exponentially into the semiconductor. This induces a continuum of surface states in the forbidden gap known as metal-induced gap states MIGS which can lead to Fermi level pining. The exponential tails of the wave fun1ctions represent a transfer of negative charges from the metal into the semiconductor. MIGS close to the valence band act as donors, while MIGS close to the conduction band act as acceptors. MIGS can be donor-like charges or acceptor-like charges corresponding to their position to the charge neutral level (E_{CNL}), Figure 2-14. Due to the presence of intrinsic surface states, charges move across the interface and occupy MIGS states. Occupying acceptor-like states results in a net negative charge while leaving the donor-like states empty results in a net positive charge. Thus, filling MIGS creates a dipole that tends to force the band line up towards a neutral position that gives a zero-dipole charge. Figure 2-14. (b) illustrates the case when the Fermi level of the metal lays above the E_{CNL} so that the created dipole which is negatively charged on the semiconductor side forces the Fermi level E_F to move toward E_{CNL} and lines up with it. With the Fermi level pinning at the Φ_{CNL} by MIGS, the Schottky barrier height is modified as in the expression[19]:

$$\Phi_B = E_{CNL} - S(x_m - x_s) \qquad (2\text{-}26)$$

where, (Φ_{CNL}) is the CNL potential measured from the Fermi level and the term $(x_m - x_s)$ is the difference between the metal and the semiconductor

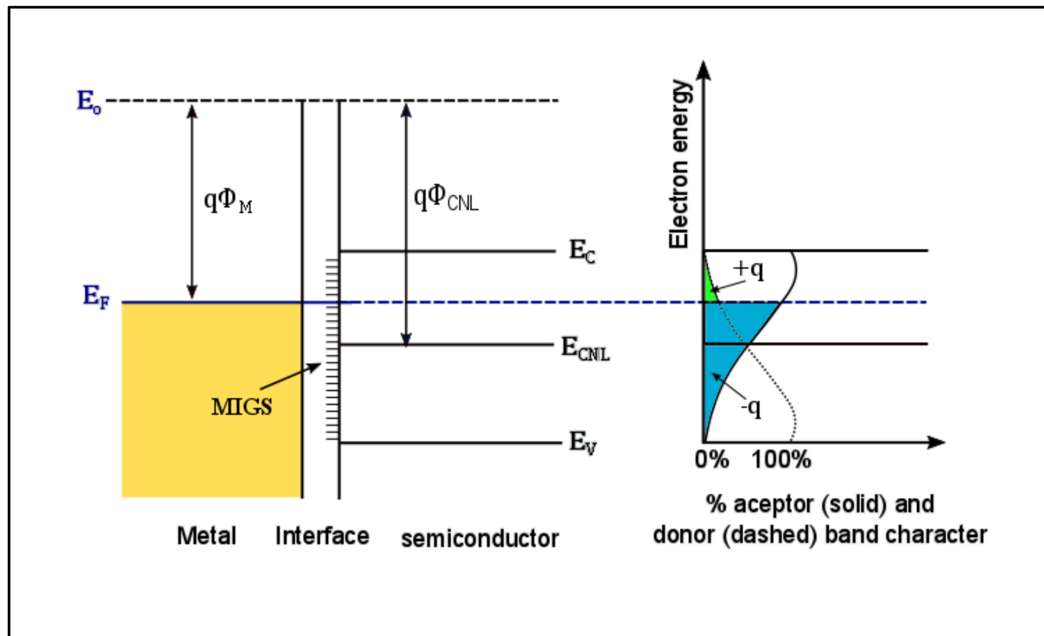

Figure 2-14 (a) Energy band diagram and (b) charging character of MIGS at a metal semiconductor contact showing the charge neutrality level ECNL. MIGS close to E_C are acceptor-like while, MIGS close to E_V are donor-like. Filling acceptor-like states results in a negative charge (green shaded area) whereas, leaving donor-like states empty results in a positive charge (blue shaded area)(redrawn from Ref. [2]).

electronegativities. Fermi level pinning at various semiconductors can be determined through a parameter known as the pinning factor S, expressed as

$$S = \frac{\partial \Phi_B}{\partial \Phi_M} \tag{2-27}$$

Typically, (S) can have values $0 \leq S \leq 1$, where material with smaller value of S have strong Femi level pinning and vice-versa. In the case of strong FL pinning interfaces, the diode approaches the Bardeen limit, $S = 0$, where the value of Φ_B is independent of Φ_M. Strong Fermi level pinning has been proven at surface state densities exceeding $10^{13} cm^{-2} eV^{-1}$[20]. For a weak FL pinning, the diode approaches the Schottky-Mott limit, $S = 1$, where Φ_B depends on Φ_M as in the ideal situation.

The MIGS theory accounts for the semiconductor contribution through E_{CNL} and for the metal and the semiconductor contributions through their electronegativity difference. The Schottky barrier height is mainly determined by the E_{CNL}, (a property of the semiconductor), and by the surface dipole due to the MS electronegativity difference.

2.7.5 The Ideality Factor

According to the simple I-V model of the thermionic emission for Schottky diode, the ideality factor η is unity. However, many factors can contribute to the departure of the diode from the ideal case and increases the ideality above unity. For instance, image force effect leads to a slight increase in the ideality factor, one obtains $\eta = 1.02$ for $N_D = 10^{17} cm^{-3}$ [6]. A presence of an interfacial layer between the metal and the semiconductor has a significant impact on the ideality factor. For example, a layer of 20 Å thickness will normally lead to a value for $\eta \cong 1.3 - 1.5$[1]. An ideality factor above (2) has been attributed to trap assisted tunnelling at room temperature[21]. A significant contribution of quantum mechanical tunnelling (FE and TFE) or carrier recombination in the Schottky diode current results in a temperature dependent ideality factor. Contrary to what is expected from purely thermionic emission current, η is independent of temperature. Barrier height inhomogeneity is another factor which can lead to an abnormal increase in the ideality factor with decreasing temperature[12, 22-24]. However, a temperature-dependent ideality factor has also been observed in the absence of these current mechanisms and in some diodes this temperature-dependence of (η) can follow the relation[25]

$$\eta = \left(1 + \frac{T_o}{T}\right) \tag{2-28}$$

where (T_o) is an access temperature parameter, typically 10-60 K[26]. This behaviour is known as the "T_o effect". Levine has attributed the T_o effect to the presence of an exponential distribution of interface states[27]. However, this analysis which depends on the presence of an interfacial layer has been rejected because the T_o effect has also been observed in intimate SB contacts[26].

It has been proposed that the I-V measurements at different temperatures can be used to identify the current transport mechanism of a given Schottky diode by observing the variation of η with temperature. From temperature dependent current voltage (I-V-T) measurement, the ideality factor can be evaluated at every individual temperature and then represented as a plot of ηT versus T as illustrated in Figure 2-15. If FE is dominant, the tunnelling constant, $\eta kT/q$, will be a straight line whereas for TFE it has a weak temperature dependency at low temperature, increasing as temperature is increased. In the case where TE is the dominated mechanism, $\eta kT/q$ shows a strong temperature

dependence for three different conditions: an ideal diode where $\eta = 1$; non-ideal diode where $\eta > 1$; and the T_o effect.

The increase in the ideality factor due to image force lowering, TFE, and generation/recombination current can be evaluated from the experimental measurements, and the maximum ideality factor which is related to these mechanisms can be estimated. However, the experimental values of the ideality factors often far exceed the estimated values, strengthening the assumption that interface states are the primary cause of raising ideality factors above unity. Two ideas have been proposed to clarify the abnormal behaviour of the ideality factor due to interface states. A diode with a thin insulator layer MIS model, and the intimate contact of MIGS model. Applying a forward bias to a diode in the presence of an interfacial layer leads to increase or reduce, depending on the semiconductor type, the negative charge at the insulator-semiconductor interface and thus increasing the barrier height with bias increasing the ideality factor. However, the outcome of this assumption does not agree with the temperature-dependence of Schottky barrier heights. Also, large ideality factors have also been observed in intimate as well as in annealed contacts where no interfacial states are expected. In intimate contacts, MIGS can also lead to high η. The band of the

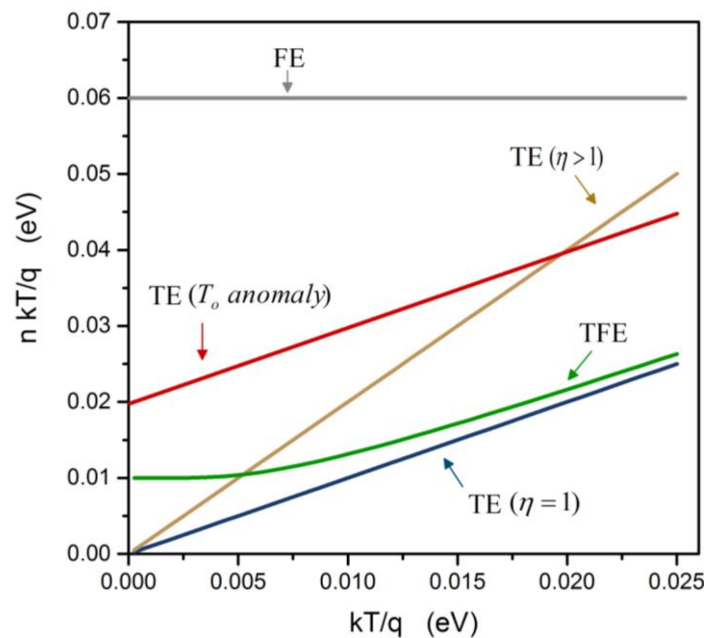

Figure 2-15 Theoretically generated plots of ηkT/q as a function of ηkT/q representing the five different categories of current transport mechanisms FE, TFE and TE at different conditions η=1, η>1 and, T_o effect.

semiconductor bends upwards near the MS interface because of the spatial extension of negative charges which alter the turning points of the potential/SB height based on the electric field. The variation of the ideality factor with the intimate MS contact can be explained in the same manner as the SBH variation. The band bending at the MS interface does not depend on the doping type, and hence, may be used to explain one type of semiconductor. For a specific MS system, MIGS can lead to high η only for n-type or p-type semiconductor, but not for both types. But, high η has been observed on both types of semiconductor in contradiction to the MIGS mechanism. There is some experimental observation that can't be explained in terms of interface states. For example, the ideality factor has been found to vary significantly with processing, or among similarly fabricated diodes, while the barrier heights are basically the same. These outcomes can't be explained according to interface states, as it's supposed to affect the values of both the ideality factor and the barrier height of the Schottky diode. In some diodes, the ideality factor seems to be associated with the value of the barrier height, as the higher ideality factor values for identical prepared diodes are always accompanied with lower barrier heights[26]. However, the mechanism for the observation is not clear yet.

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Chapter 3

Materials and Devices Fabrication

3.1 InSb/ AlxIn1-xSb QW Heterostructures

Quantum well (QW) structures can be realised through band-gap engineering by having a thin layer of a narrow-bandgap semiconductor sandwiched between two other layers of a wider-bandgap semiconductor with, ideally, almost identical lattice constants. This results in abrupt discontinuities at the interfaces of the energy bands, as illustrated schematically in Figure 3-1 (a). Use of the modulation-doping technique, pioneered by Stormer et al.[1], where a shallow donor doping of the wide-gap semiconductor shifts

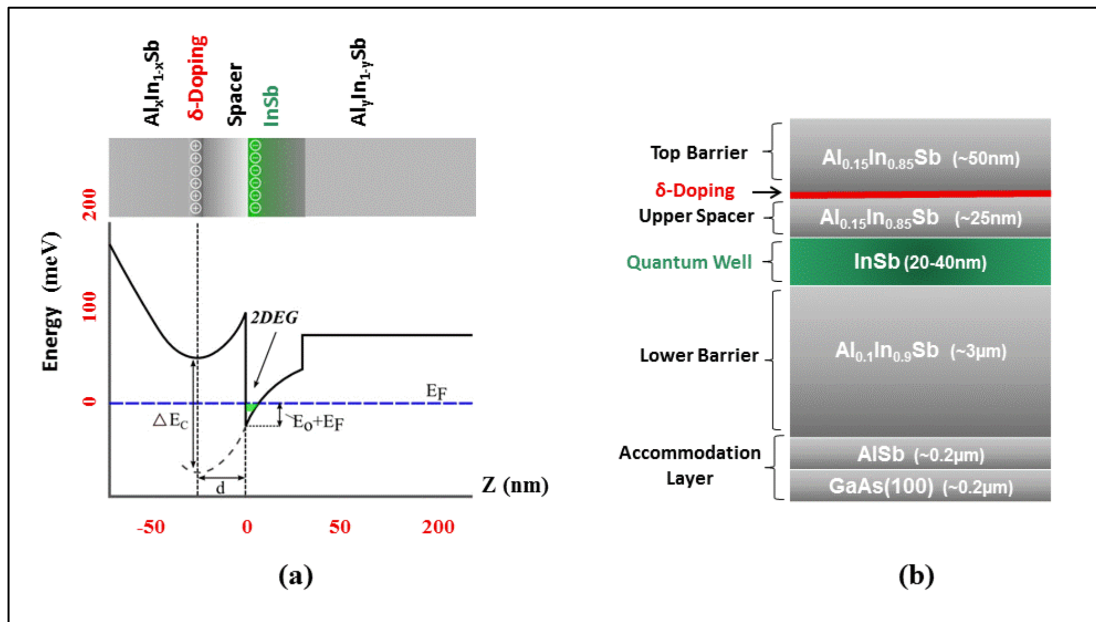

Figure 3-1 Schematics of a InSb/$Al_xIn_{1-x}Sb$ QW heterostructure showing (a) the energy band diagram and the 2DEG formed at the InSb/$Al_xIn_{1-x}Sb$ interface. (b) layer structure.

the Fermi level from the middle of the bandgap towards the conduction band edge. As a result, electrons will flow from the wide-gap semiconductor toward the narrow-gap semiconductor to keep a constant chemical potential across the two materials. This leads to ‘’band bending’’ at the interface as shown in Figure 3-1 (b). Due to band bending, the electron movement is confined to an approximately triangular potential well at the material interface. This forms what is known as a two-dimensional electron gas (2DEG), due to the reduced dimensionality of the electron movement. Electrons in 2DEGs can move with a high mobility because they are physically separated from the ionised impurities and therefore suffer less scattering. For high-quality materials, electrons at low temperatures can travel several microns without being scattered elastically off impurities (although they are still limited by inelastic scattering by other electrons or phonons). To restrict and thus quantise the electron motion in one direction, the width of the potential well has to be comparable to de Broglie wavelength of the electrons (or holes). The record electron mobility values in this system (for specialist GaAs/AlGaAs materials) can exceed 10^7 cm^2/Vs at low temperatures compared to only ~10^4 cm^2/Vs in early III-V heterojunctions[2].

The samples used in this thesis are based on the narrow gap semiconductor Indium Antimonide (InSb). The epitaxial layers of $InSb/Al_xIn_{1-x}Sb$ -QW heterostructures are grown by molecular beam epitaxy (MBE) on semi-insulating GaAs substrates. A single $InSb/Al_xIn_{1-x}Sb$ quantum well structure modified by modulation doping is illustrated in Figure 3-1, where a thin InSb layer 20-30 nm is sandwiched between two layers of $Al_xIn_{1-x}Sb$ of a wider gap that is varied between 200-650 mV depending on the aluminum content in the alloy. The electrons in the InSb layer are trapped by the potential barriers at each side by the discontinuity in the conduction band. These barriers quantise the states in the z (crystal growth) direction, but the motion in the x, y plane is still free. Although InSb QWs can be grown on Si, Ge or GaAs substrates, semi-insulating GaAs (001) substrates which have the same zinc-blend structure as InSb and AlInSb are preferable to avoid the problem of anti-phase boundaries forming.

The growth of this material on GaAs (001) substrates is normally done through an $Al_xIn_{1-x}Sb$ buffer layer which is necessary for suppressing dislocations which propagate from the extremely mismatched interface between the substrate and the alloy [2-5]. Choosing GaAs as a substrate is due to many reasons, including its mechanical strength, relatively high resistivity, and its reasonable cost. Moreover, GaAs has the same atomic

structure, zinc-blende, as InSb and AlInSb. However, using GaAs substrates has a major drawback, a high lattice mismatch of 14.6% between GaAs and InSb leads to the formation of a high density of structural defects such as threading dislocations (TDs) and micro-twins (MTs). These structural defects act as strong scattering centres and decrease the room temperature electron mobility in InSb QWs [3-7].

3.2 Atomic Force Microscopy (AFM) Analysis

Atomic force microscopy AFM is a powerful technique in imaging and assessing the surface roughness and the density of threading dislocations TDs. AFM has been used to analyse the surface morphology of the AlInSb epitaxial wafer surface. Figure 3-2 shows a series of AFM images of the InSb/AlInSb heterostructure surface, where atomic layer steps can be clearly observed on the surface combined with uniformly distributed

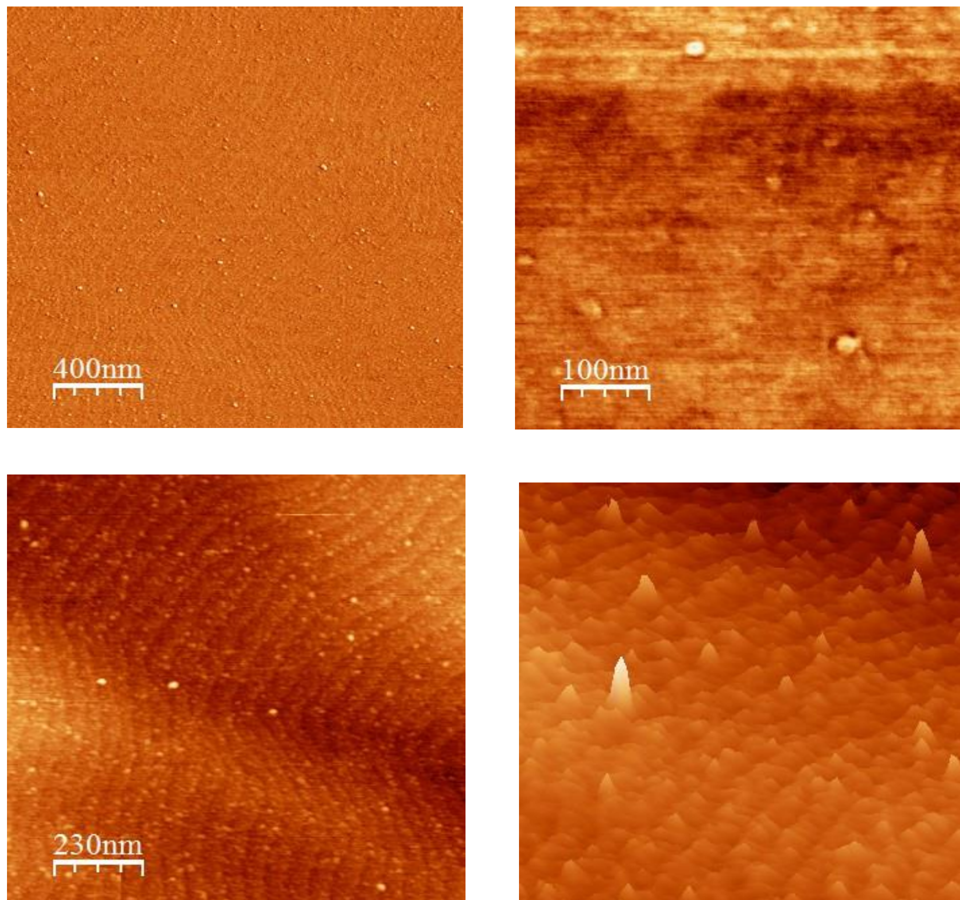

Figure 3-2 AFM images of InSb/AlInSb QW heterostructure surface exhibiting an array of atomic layer steps, Light dots are threading dislocations that have spread upward to the surface.

pits over the surface. The density of these pits was calculated by counting the number of pits within the scanned area. For the chosen layer, the pits density was found to be $2 \times 10^{11}\ cm^{-2}$ which is comparable to the density of TDs determined by TEM for a similar material, as shown in Figure 3-3. Hence, one can conclude that these pits take place on the TDs sites. They are forming around the threading dislocations which propagate upward in the growth direction. The dislocation regions are likely to have a high electrical potential due to the presence of charged traps or dopants accumulation. Therefore, the potential at the dislocation regions are speculated to be higher than the surrounding areas[8]. These areas are probably micro-masked with charged particles or an interaction might take place with other defects or impurities that may block the TDs.

From the AFM and TEM analysis, it is evident that these AlInSb/InSb heterostructures have a poor surface morphology. The buffer layer and subsequent AlInSb has a high density of threading dislocations, the dislocations are first generated at the GaAs/AlSb and AlSb/AlInSb interfaces due to the high lattice mismatch and propagate through the grown layers up to the surface. Therefore, the poor surface morphology of the AlInSb/InSb structure from AFM measurement is almost certainly due to the high level of threading defects, as observed by cross-sectional TEM micrograph, Figure 3-3.

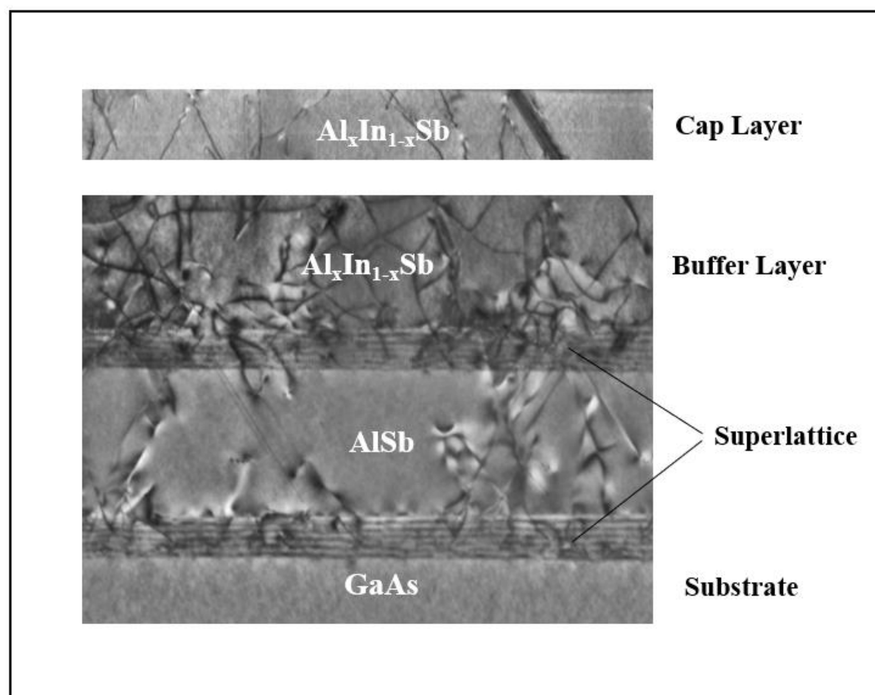

Figure 3-3 Cross sectional TEM micrograph of an AlInSb/InSb layer. A high density of threading dislocations is observed in the buffer layers which then propagate through the structure during the growth process.

3.3 Device Processing

AlInSb/InSb-QW Schottky diodes were fabricated from the as-grown wafers described in 3.1 using a combination of standard semiconductor processing techniques. The used materials, AlInSb/InSb heterostrctures, were grown by solid source molecular beam epitaxy (MBE) in the National Centre for III-V Technologies in Sheffield University. All the devices were fabricated and initially tested using a class 1000 and class 100 clean room environment within the School of Physics and Astronomy at Cardiff University. According to the British standard 5295 (1989), the number designation of the class is taken from the maximum permissible number of particles 0.35 micron or larger per cubic foot of air.

3.3.1 Photolithography

Optical lithography is the technique of transferring a desired pattern from a photomask onto a thin film of a photosensitive material (photoresist) covering the surface of a semiconductor sample, by exposure to ultraviolet (UV) light through the mask. The exposed regions of a positive photoresist or the unexposed region of a negative photoresist can be easily removed when immersed in a developer solution forming patterns in the remaining photoresist. The key photolithography steps implemented in this work are illustrated in Figure 3-4 (a-d). The photolithography is normally started by preparing the sample and cleaning it appropriately using Acetone and Isopropyl (IPA) respectively and then applying a thin film of a photoresist, Figure 3-4 (b), in a liquid form to the semiconductor substrate and dispensed it evenly using a mechanical spin coater. After this, the sample is soft baked on a hot plate to evaporate the solvents, and for obtaining a solid film that strongly adheres to the substrate. In this work two positive tone photoresists; PMGI SF11 and S1813 were used to form a bi-layer of photoresists using different exposure parameters. First, SF11 resist is spun onto the substrate at 5000 rpm for 20 seconds and soft baked on a hot plate at 95°C for 10 minutes. Then, S1813 is spun at 5000 rpm for 20 seconds onto the SF11 film and soft baked at 80°C for 5 min. This results in a bi-layer of approximately 0.5 µm thickness for the SF11 layer, and 1.5 µm for the S1813 layer. A bi-layer photoresist process is normally used for metal deposition (evaporation) to facilitate the lift-off process, and a single layer of S1813 photoresist is usually used for the chemical wet etch process. The devices patterns were transferred from the photomask to the photoresist by exposure to

ultraviolet (UV) radiation for 5 Sec using a Karl Suss MJB3 Mask Aligner, Figure 3-4 (c). As a final step, the resist is then developed in MF319 for 15 Sec to remove the exposed regions of the resist then rinsed with de-ionised water for more than 30 Sec which completes the pattern transfer from the mask to the substrate as illustrated

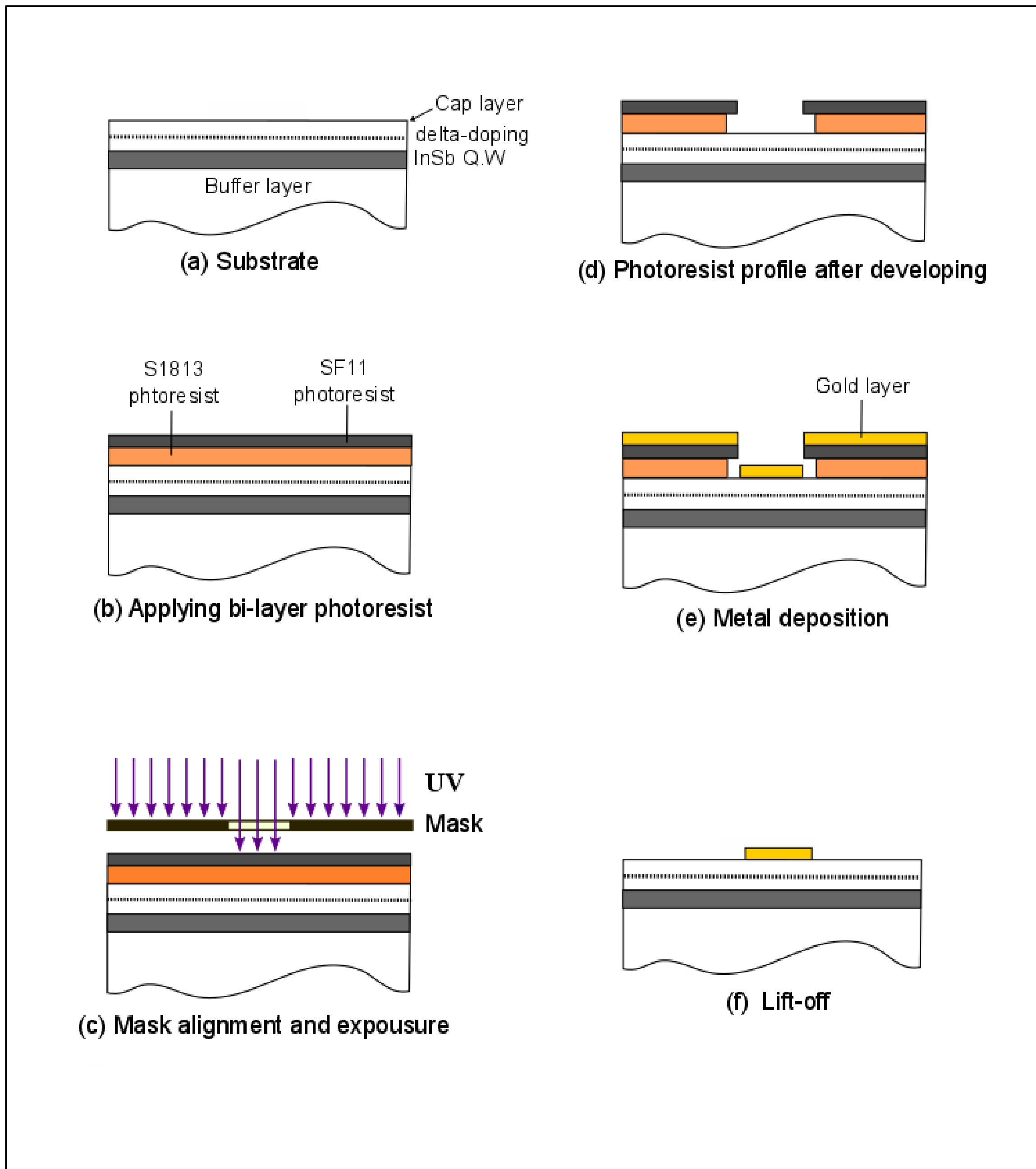

Figure 3-4 Schematics of the key photolithography steps (a-c) followed in processing the AlInSb/InSb QW heterostructure based Schottky diodes, along with the metallization (e) and lift-off (f) steps.

in Figure 3-4 (d). To ensure the accuracy of the developing, samples were inspected under an optical microscope continuously.

3.3.2 Metallization

The fabrication of Schottky diodes on AlInSb/InSb heterostructure material involves two metallization processes that can be made simultaneously on the same wafer. The first deposition is for the ohmic contact and the second deposition is for the Schottky contact. The metallization processes were done by the common thermal evaporation method. In thermal evaporation, the source metal to be evaporated is placed in a resistive heated crucible or filament. It's temperature is then raised by Ohmic heating, passing a high current through the filament, until the source metal melts and vaporises in all directions and condenses on the wafer surface (as well as the surface of the bell jar or deposition chamber[9]). For an ultra-clean and contamination-free deposition, the evaporation processes were done under a high vacuum (below 1×10^{-6} mbar). A quartz crystal was used to monitor the film thickness. In this work, the metallization processes were done in two different Edwards E306 thermal evaporation vacuum systems. One of these was arranged for evaporating gold (Au), nickel (Ni), and chrome (Cr) while the other system was arranged to evaporate Au and zinc (Zn) layers (at slightly more elevated temperature). The sample holder of the Zn/Au evaporator was supplied with a heater and a thermocouple to control the temperature of the sample wafer during the evaporation process. To avoid possible heat damage to Schottky contacts, ohmic contacts were evaporated first by depositing Zn/Au layers onto the substrate surface in 10 nm Zn:300 nm Au thicknesses. In the ohmic contact metallization process, the substrate was heated up to 100°C before and during the evaporation process; this helps in improving the adhesion of the metal film to the substrate to a certain extent. Schottky contacts were made by depositing Ni/Au (nickel, gold) layers onto the surface with thicknesses of 10 nm Ni:300 nm Au. Au is always used for the upper metal layer because of its very low oxidation characteristic and its high resistance to chemical attack, in addition to its easy bonding property as a result of its ductility and non-oxidation nature[9]. Annealing is usually applied at suitable stages for obtaining a good ohmic contact and improving the Schottky diode parameters. However, due to the low melting temperature of InSb about 525°C, and previous experience within material

degradation at elevated process temperatures, annealing was excluded because of the risk of altering or damaging the material structure.

Once the metal film was deposited onto the sample, the photoresist layer and the unwanted metal (on top of the photoresist) were removed by immersing the sample in acetone for more than 20 min, and then in NMP for another 10 min. This lifting-off step results in a patterned sample of Schottky/ohmic contacts as shown in Figure 3-4 (e-f).

3.4 Fabricated Devices

In this work, two types of planar structure, elementary and surface channel, were used to fabricated AlInSb/InSb Schottky diodes following the processing techniques described in section 3.3. The mask of the elementary structured diodes consisted of a variety of large size devices 50 µm to 200 µm. Processing of the elementary devices was implemented by depositing the ohmic and the Schottky contacts directly to a cleaned substrate in two different metallization steps without mesa isolation. Two optical microscope images of a set of fabricated devices and an individual diode are shown in Figure 3-5. Such a simple diode structure gives rise to a high leakage current in both forward and revers bias. Under reverse-bias conditions, the leakage current is due to the high electric field generated at the contact edges. In forward bias, the leakage current is generated as a result of the high conductivity of the substrate material (InSb/AlInSb heterostructure). The drawback of high leakage through the epitaxy cap

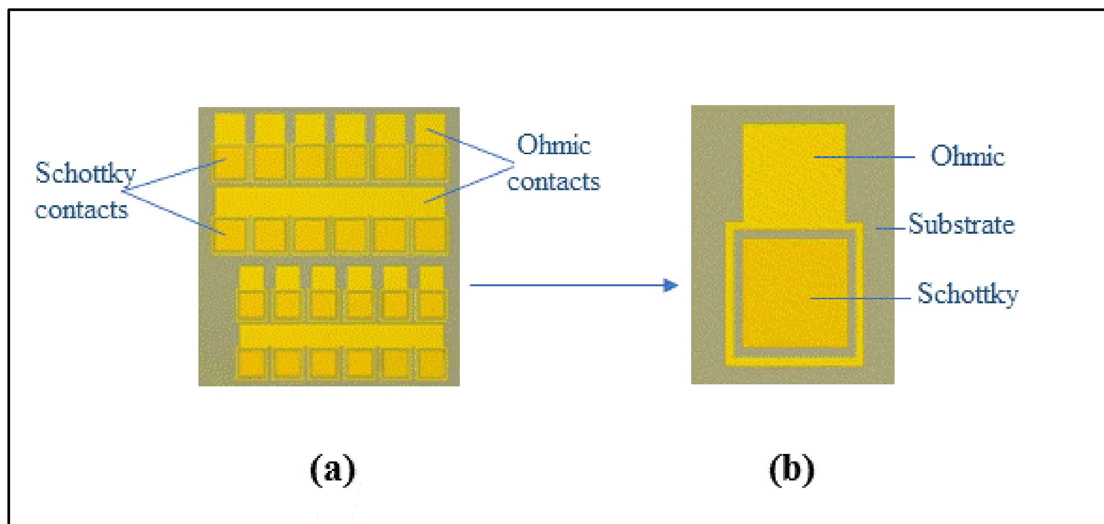

Figure 3-5 Two microscope images showing (a) a set of the large size fabricated Schottky diodes.

layer was overcome by designing a new mask of surface-channel planar diode construction. The configurations of two selected devices, 2-terminal, and 3-terminal are shown in Figure 3-6. The design has a small area Schottky contact formed at the finger-substrate contact at a close distance from the ohmic contact to reduce the spreading resistance. The Schottky Contact is connected to a large contact Schottky pad through a narrow finger. To confine the current to pass through the small-area Schottky contact to the large-area Ohmic pad, wet etching was used to isolate the Schottky and the ohmic pads and to form a narrow air-bridge around the finger. A closeup view on a 2 μm finger Schottky contact is shown Figure 3-6 (c), the image illustrates the formation of the surface channel. Detailed information about the mask are described in detail in appendix A.

A novel technique was introduced to processing recipe with this mask. The Schottky contact was deposited on a shallow etched substrate, and the deposition of the ohmic

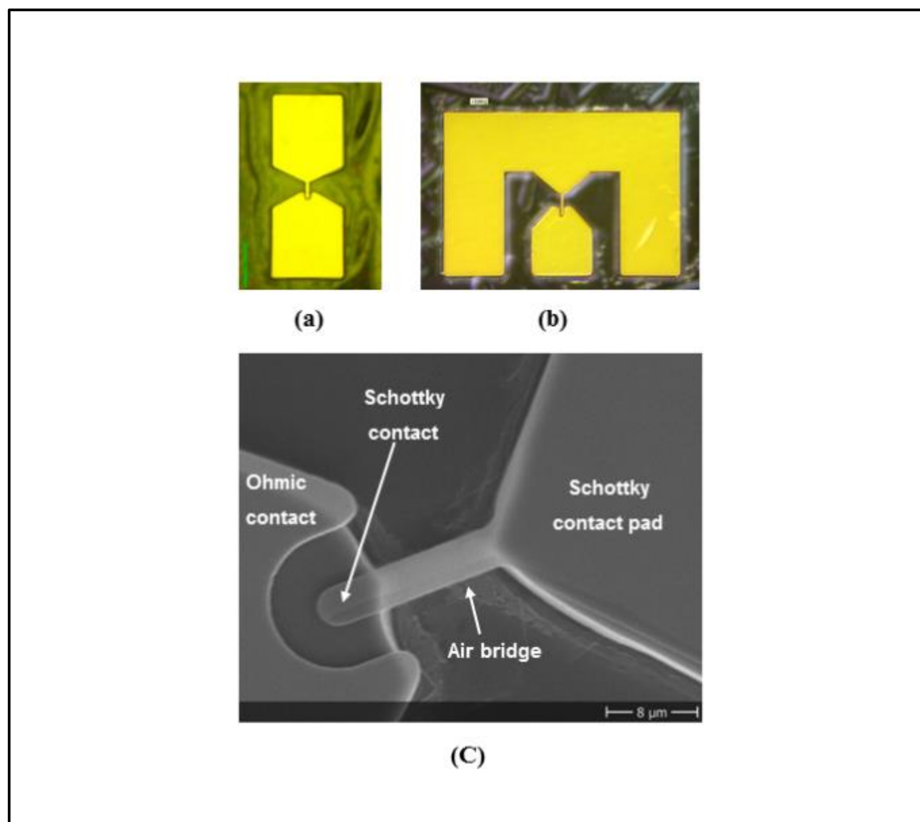

Figure 3-6 Two microscopic images of a (a) 2-terminal Schottky diode and (b) 3-terminal Schottky diode and (c) SEM image of a fabricated 2 μm Schottky contact that gives a closeup view of the contact area and the air bridge finger formed after the etching process.

contact was just above the dopant layer in the material. Wet etching was used to remove the substrate top layers and reach the required level before deposition.

3.5 Wet Chemical Etching

Material removal is done using two different techniques, "wet etching" which depends on chemical liquid etchants, or "dry etching" which depends on chemical vapours and/or plasma ion etchants[10]. Etching techniques are usually used in the fabrication process of semiconductor devices to remove undesirable layers of semiconductor material mainly for electrical isolation, cleaning, or surface oxides removal. In the wet etching technique, the undesirable materials are removed by immersing the wafer in an appropriate chemical etchant that interacts with the exposed regions to form soluble by-products. The process of wet etching can be described in three basic stages. First, the diffusion of liquid etchant to the parts to be removed that have been pre-defined for example by photolithography on the semiconductor substrate. Then a reduction-oxidation reaction between the etchant and the material to be etched away. Finally, diffusion of the reaction by-products away from the reacted surface. Wet etching is a comparatively easy technique to apply but, it is hard to control because the etch depends on lots of factors such as temperature, etchant PH, passivation, and the consistency of the method of application e.g. immersion, spin, agitation, etc.

The fabrication of the AlInSb/InSb-QW based Schottky diodes reported here comprised an elaborate procedure involving surface treatment, thermal evaporation, and mesa isolation to attempt to achieve consistency. Both surface treatment and mesa etching were performed by using wet etching in two different etchant solutions. Therefore, for these samples wet etching was used for two different purposes. The first one was aiming for cleaning and preparing the surface before the metallization process and the second purpose was for devices isolation which applies after the deposition processes of the ohmic and Schottky contacts.

Surface treatment utilising citric acid etchant prior to metal deposition was trialled for the Ohmic and the Schottky contact. The citric acid etchant solution was prepared by dissolving anhydrous citric acid crystals in deionised water DI H_2O at a ratio of 4 g C6H8O7:8 ml DI H_2O with a subsequent etch rate of ~2 nm/min. For complete dissolution, the mixture was mixed in an ultrasonic bath for a minute at room

temperature and allowed to stand. The substrate masking was accomplished by lithography using a bi-layer photoresist to define the contacts patterns. Two etch times were used depending on the contact type. For Schottky contacts, the substrate was immersed in the citric acid etchant for 2 min, in general to clean the surface and remove the surface oxide layer in an attempt to reduce the surface states and the insulating oxide layer which might degrade the Schottky diode performance. Ohmic contacts were immersed in the etchant for around 10 min (depending on layer design) to etch down to the doping layer as illustrated in Figure 3-7. The goal of this etching was to deposit the

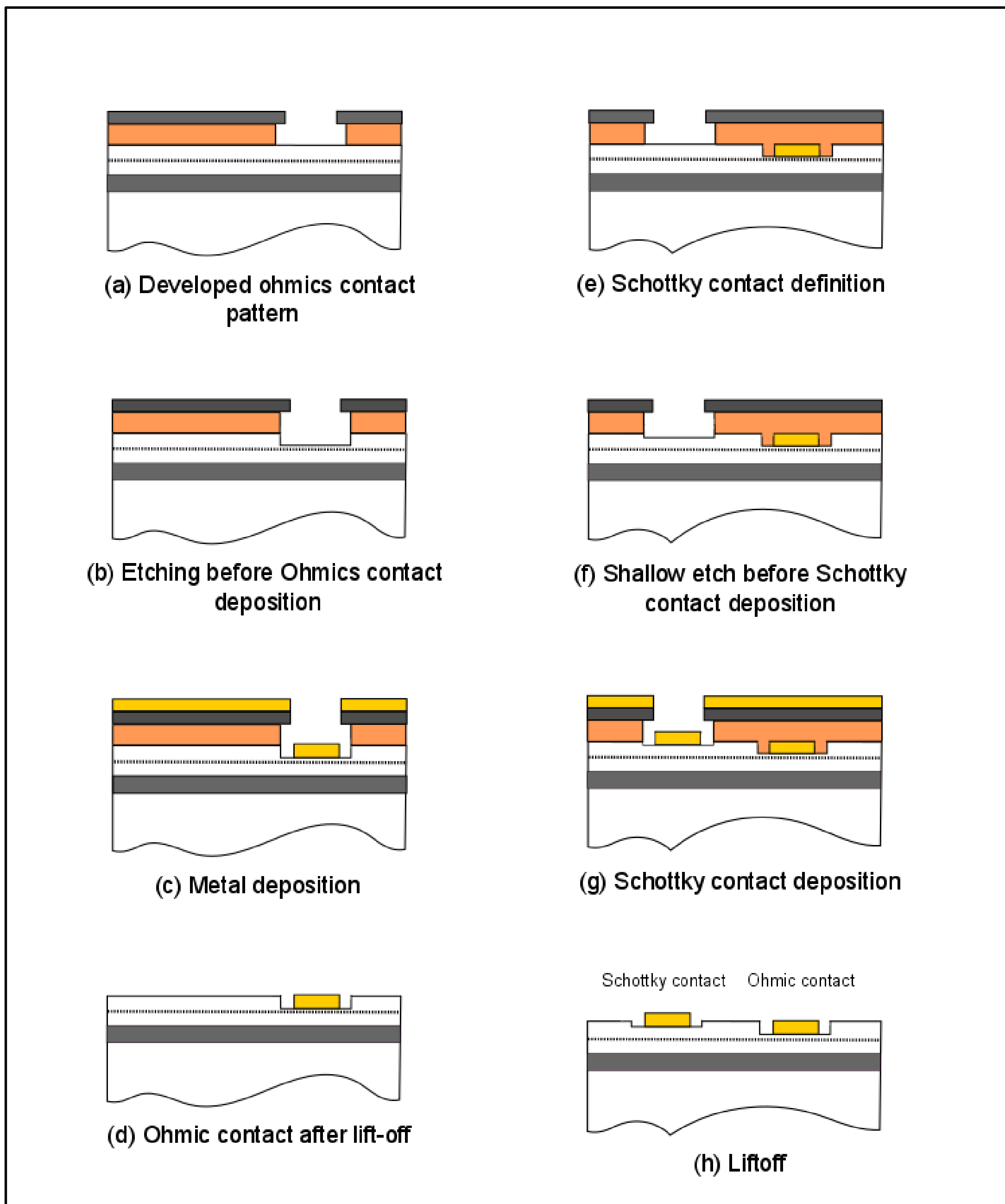

Figure 3-7 Schematic of Surface treatment applied to the semiconductor surface before depositing the metal contacts.

ohmic contact on the highest doped layer in the AlInSb/InSb structure to obtain a good ohmic contact with low series resistance. Etching was stopped by rinsing thoroughly in DI H_2O for more than one minute, and finally the sample was blown dry using dry nitrogen gas.

Devices Isolation is an important process to isolate the effective area of the device and prevent current flowing beyond the given boundaries of the device. The electrical isolation was realised by using the wet etching technique. After the completion of the metallization process, the sample was coated with S1813 and patterned in a manner to maximise coverage of the devices area, except the areas to be etched away as shown in Figure 3-7 schematically. Device isolation is achieved by immersing the substrate in a mixture of lactic and nitric acids in a ratio of 10 ml:80 ml, with a typical etch rate of ~20 nm/Sec. To insure a total electrical isolation to the active regions of each devices, a deep wet etching was carried out down to the GaAs substrate layer, of ~3 µm etch depth. An optical microscope and a Dektak Stylus Profiler were used to monitor the etch depth. Finally, a SEM was used as well to ensure that all the Schottky's fingers are air-bridged as illustrated Figure 3-8 (a-c). Measuring the etch depth doesn't guarantee the formation of the surface channel. The imaging was done with the resist in-situ to enable further etching if necessary. If the devices were not totally isolated as in Figure 3-8 (a), the etching process would be continued until isolation was achieved.

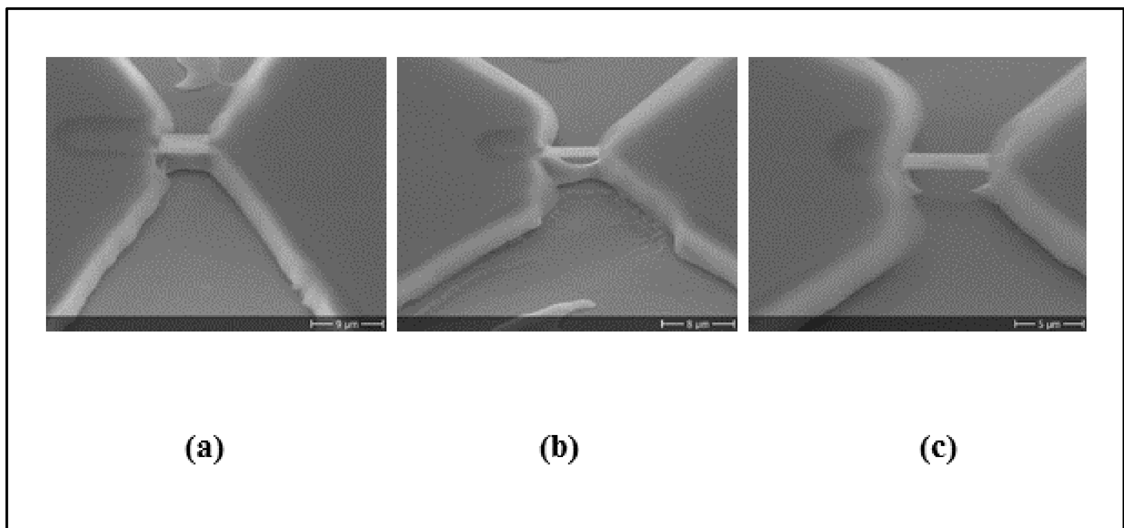

Figure 3-8 Wet etch for mesa formation inspected with an SEM to ensure total isolation of the devices with the photo resist patterns still on. Three different stages (a) after nearly 3 minutes in acid the etch depth is 3 µm. The device is not isolated (b) further etch for 30 additional 30 seconds, the device is totally isolated.

3.6 Room Temperature I-V Measurements

Once they were fabricated, the I-V characteristics (analysed in chapter four) of the AlInSb/InSb Schottky diodes were initially measured at room temperature. A specific setup was used for conducting the I-V measurements. The setup includes an on-wafer DC probe station, Figure 3-9, and low voltage source and current measurement meter. The probe station and the source meter were interfaced with a computer that allows automated I-V measurements via a software[1] written in the python programming language. The used source meter, 2401 from Keithley instruments, provides precision voltage sourcing of ±1 μV to ±20 V. The I-V measurements were taken under a two-terminal arrangement at voltage range -500 mV to +500 mV, the applied voltage sweep was kept low to avoid heating and possible melting of the gate metal.

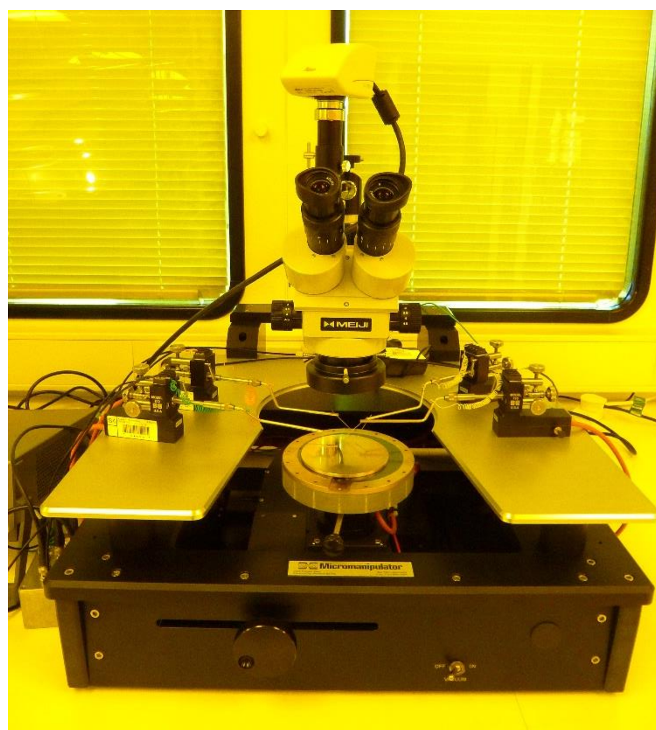

Figure 3-9 DC probe station used for on-wafer (I-V) measurements.

1 Software written by L Hanks.

3.7 Packaging

To perform the temperature dependent current voltage I-V-T, the fabricated samples were cleaved into 3.6 mm × 3.6 mm sections (die) and then mounted into 20-pin surface mount ceramic packages with a low temperature GE varnish. A manual West-Bond 7400A Wedge-Wedge Wire Bonder was used to bond the contact pads of the fabricated devices to the package pins (using a fine gold wire of 12.5 µm diameter). The bonding process wedge-wedge bonding is a thermocompression process which requires applying a combination of heat and pressure to provide a strong mechanical and electrical connection between the two-metal surface[9]. The 20-pin package allows the bonding of ten devices of two terminals or six devices of three terminals, which has the advantage of allowing measurements of multiple devices at one time. Figure 3-10 shows a ceramic package (a) before, and (b) after mounting the sample to the package. The bonding wires are also shown in figure (b) while figure(c) shows an individual bonded device. After the bonding process, the 20-pin ceramic package is uploaded into a

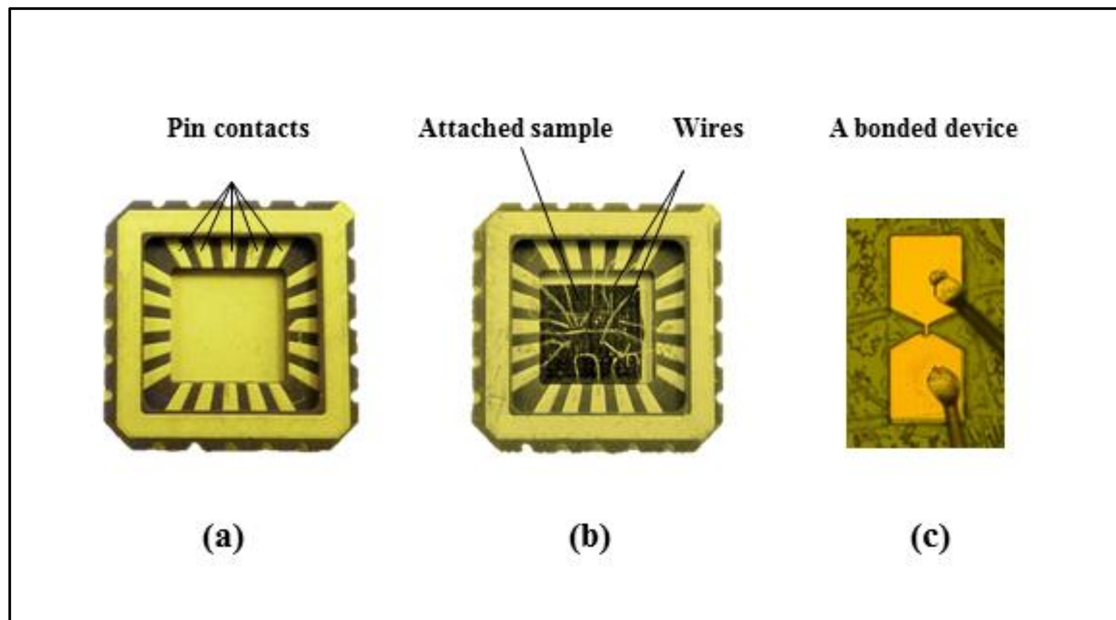

Figure 3-10 (a) A photo of an empty 20-pin ceramic package. (b) A photo of a wire bonded package where a sample is mounted into the package using low temperature GE varnish. Electrical bonds are made between the contacts of the devices on the mounted sample and the individual pin on the package using a gold wire. (c) A microscope image of bonding gold wire attached to a Schottky contact.

package holder located in the cooled finger of a cryostat for temperature dependent measurements.

3.8 Temperature Dependent I-V Measurements

The temperature dependent (I-V-T) measurements, analysed in chapter 5, of the AlInSb/InSb Schottky barrier devices were carried out in a cryostat system. The system is equipped with an Oxford Instruments Optistat AC-V12 instrument which can achieve temperatures as low as 2.8 K. The measurement temperature was maintained by using an Oxford Instruments MercuryiTC Cryogenic programmable temperature controller. For I-V measurements, an Agilent Technologies E5270B precision current voltage analyser and an Agilent Technologies E5281B Medium Power Source Monitor Unit (MPSMU) were used. Both the temperature controller and the I-V analyser were interfaced with a computer that allows fully automated I-V-T measurements via a computer software written in the python programming language. The software allows applying a fully automated temperature sweep over the entire temperature range. At each temperature, the software controls a voltage sweep at a certain range for the diode under test and measures the current within this range. For thermal stability at each

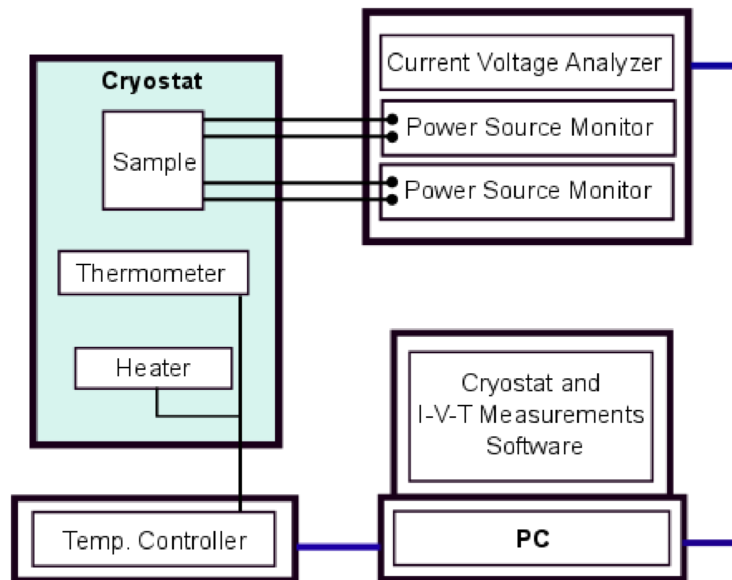

Figure 3-11 Schematic of the I-V-T measurement setup. Blue lines dedicated for digital signals and black lines are for analogue signals.

temperature measurement, a time delay of 10 min was generally introduced before taking the I-V measurements. The experimental setup of our cryostat system and other supporting components is illustrated in Figure 3-11 For precise I-V measurements, the cables resistances were eliminated by adopting a 4-terminal measurement technique, where the contacts used to apply the voltage through the sample are different from the contacts used to measure. With this method, resistance is measured only between the two voltage probes, contrary to a 2-terminal measurement method where the detected resistance includes the cable and contact resistances.

3.9 Bibliography

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Chapter 4

I-V Characterization of AlInSb/InSb QW Based Schottky Diodes

4.1 Introduction

The electrical performance of Schottky diodes can be described by their physical parameters: effective barrier height (Φ_B), ideality factor (η), series resistance (R_S), and saturation current (I_o). These physical parameters are of great importance because they give us a better understanding of the transport mechanisms over the MS barrier as well as helping achieve technology developments. Moreover, a precise knowledge of these parameters is required for any electronic circuits comprising Schottky diodes. Several methods that extract these parameters from the forward I-V characteristics are widely known [1-14]. In this chapter, four main methods are presented, the Rhoderick method [1], the Cheung method [4], the Norde method [5], and the Werner method [15] for determining the physical parameters of fabricated AlInSb/InSb-QW Schottky diodes from forward current-voltage measurements. Most of these methods are based on the thermionic emission model that assumes the current transport over the barrier is in according with equation (4-1).

$$J = J_o \left[\exp\left(\frac{qV}{\eta KT}\right) - 1\right] \tag{4-1}$$

The first one is known as the standard I-V method which was described by Rhoderick, who considered the case of an ideal diode with zero series resistance and an ideality factor of $1 < \eta < 1.2$. Whereas the other three techniques, known as Cheung, Norde, and Werner methods have considered the problem of the most practical diodes, represented by the diode series resistance (R_s). These methods have used a modified thermionic emission model, as in equation (4-2), to assess the diode series resistance and then deducing the voltage drop across the resistance from the applied voltage.

$$J = J_o\,[\exp\frac{q(V - IR_s)}{\eta KT} - 1] \tag{4-2}$$

In this equation, two important parameters η and R_s were added to the ideal model to extend it to the non-ideal diodes case. The ideality factor indicates the contribution of other current mechanisms to the TE, and series resistance reveals the current loss seen by the contact.

4.2 I-V Characteristics of AlInSb/InSb-QW Schottky Diodes

A typical I-V measurement of a AlInSb/InSb Schottky diode with surface channel structure are shown in Figure 4-1. The measurements are compared to theoretical curves simulated based on the TE model, equation (4-1). The blue line represents the ideal case where only pure TE is expected, and the other two curves belong to extreme cases where $\eta = 2$ and $\eta = 3$. From the plot, it is apparent that the experimental data deviates considerably not only from the ideal case but also deviates from other extreme cases. It is worth mentioning that several sets of Schottky diodes based on AlInSb/InSb-QW material have been fabricated using various process conditions and different structures. The current voltage measurements have been measured for most of the fabricated devices. The majority of the fabricated diodes have nearly the same behaviour especially in forward bias. The I-V characteristics of two different AlInSb/InSb Schottky diodes will be analysed in the next sections to discuss the challenges in determining the diode parameters. Firstly, the Rhoderick technique will be used to assess and extract the fundamental parameters of SBD followed by the modified methods of Norde, Werner, and Cheung.

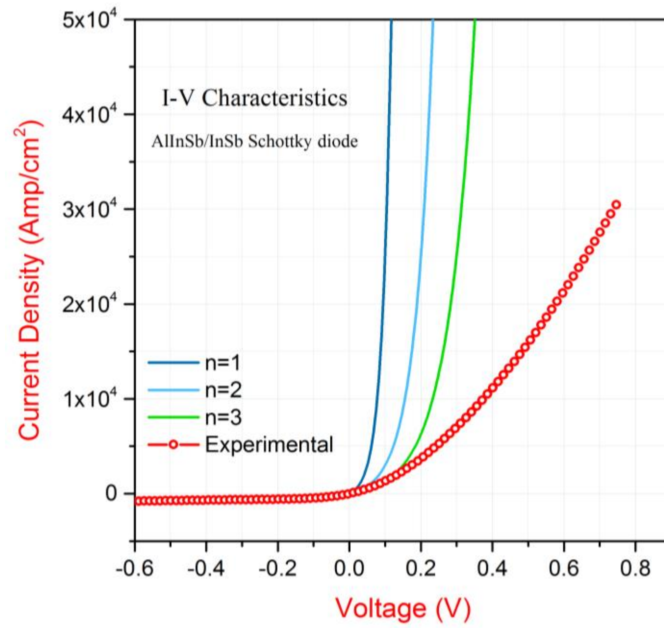

Figure 4-1 Current-Voltage characteristics of a fabricated AlInSb/InSb-QW based Schottky diode compared to simulated curves at three different ideality factors (1, 2, 3).

4.3 Rhoderick Method

The Rhoderick method is the most common and the easiest method used to determine the Schottky diode parameters. The Rhoderick approach is based on the TE theory to determine the barrier height and the ideality factor of the diode from experimental data. He assumed that the I-V characteristics for-highly doped semiconductors, at $V > 3KT/q$, can be represented in a simplified form of the TE model, equation (4-1)[1] as:

$$J = J_o \exp\left(\frac{qV}{\eta KT}\right) \tag{4-3}$$

where,

$$J_o = A^{**}\mathrm{T}^2 \exp\left(-\frac{q\Phi_{B0}}{KT}\right) \tag{4-4}$$

The Richardson constant (A^{**}) is an electrical constant which is supposed to be known in most cases. However, this constant can be found experimentally by using the activation energy method [3]. The barrier height and the idealty factor can be extracted by plotting the current density on a semi-log scale ln(*J*) versus *V*. The plot yields a straight line that intersects the y-axis at the value of $\ln(J_o)$ at zero-voltage. Once J_o is

known, the effective barrier height at zero bias (Φ_{B0}) can be evaluated directly from equation (4-4). The slope of the line can be used to calculate the diode ideality factor as:

$$\eta = \frac{q}{slope \times KT} \tag{4-5}$$

Figure 4-2 shows theoretical I-V curves on a semilog scale calculated over a range of ideality factors using the TE model. Most curves show linearity over the whole applied voltage apart from the one with high ideality factor $\eta = 3$ which shows a slight downward curvature at low voltage.

Rhoderick proposed an ideal SBD where $1.1 > \eta \geq 1$ and ignored the effect of the diode series resistance which exists in most practical diodes. The diode series resistance dominates the current at high voltages and affects the linearity of the I-V semilog plot. Therefore, the linear part will be limited to a reduced voltage range $3\mathrm{kT/q} < V \ll IR_s$ where the effect of the series resistance can be neglected. When the diode series resistance increases, the linear part decreases, causing difficulties in determining the slope and intercept accurately[1, 16]. This interval will be even smaller for diodes built

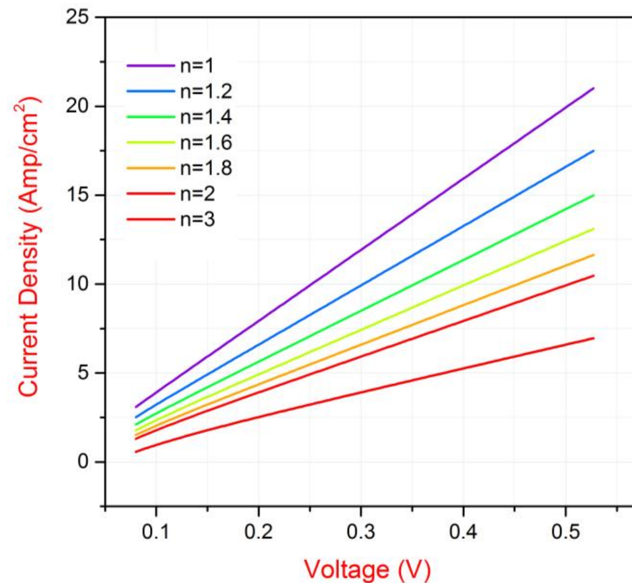

Figure 4-2 Simulated I-V curves of AlInSb/InSb Schottky diode in semilog scale at different ideality factors. it is apparent that as η increases the curves bend downward.

on narrow band gap semiconductors. The drop-off voltage of such diodes is too low, approximately less than 0.3 eV, because of the small energy band gap of these materials. The effect of the diode series resistance on a semilog plot of I-V characteristics for SBDs is illustrated in Figure 4-3. The I-V curves have been calculated for different barrier heights $0.2 - 0.7\ eV$ using the modified TE model, equation (4-2), considering a series resistance of 100Ω and an ideality factor of unity. From the figure, it is apparent that the series resistance affects the linearity of SBDs with low barrier height more than diodes with a higher barrier. The effect of series resistance values on the I-V characteristics for two diodes of $\Phi_B = 0.2\ eV$ and $\Phi_B = 0.4\ eV$ was also considered. The simulated I-V curves for the two diodes are shown in Figure 4-4. It is apparent that a series resistance as small as 5 Ω can alter the linearity of the I-V characteristic. Thus, the diode with lower barrier height is more affected by the series resistance than the higher one. Finally, another source of uncertainty in determining I_o could be attributed to recombination current which is expected to represent a high portion of the diode current at low voltages. A typical I-V measurement of a AlInSb/InSb-QW Schottky diodes is shown in Figure 4-5. Figure (a) shows the I-V data on a semilog scale in the

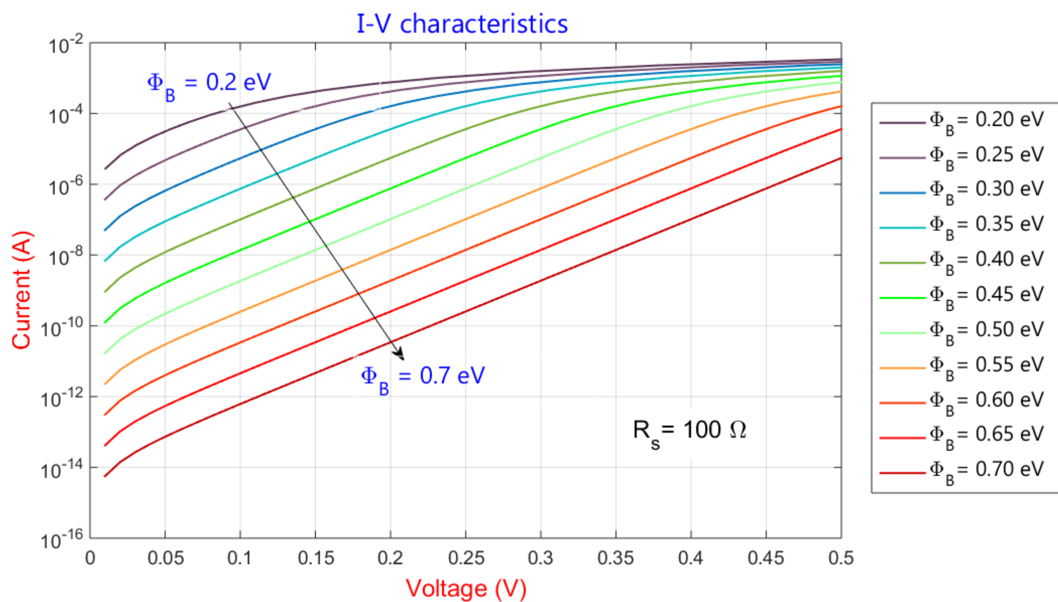

Figure 4-3 Theoretical I-V curves in semilog scale for SBDs with a series resistance of 100 Ω and η=1. To show the impact of R_s on SBDs of different material, curves were simulated over a range of barrier heights. The curves bending owing to R_s increases as Φ_B decreases.

forward bias range from 0 V to 0.5 V while the voltage range in figure (b) was narrowed to a region between 0.009 V to 0.15 V. It is apparent from the figures that the linear part of the forward current is limited to a small part of the I-V curve. This reveals a high series diode resistance which dominates in the forward bias current. The Rhoderick method was used to determine the diode parameters, barrier height and ideality factor, from the linear region of the I-V semilog plot. The extracted value of the barrier height Φ_B was 0.156 eV and the value the ideality factor η was 3.4 as illustrated in figure (b). Any change in the voltage range, even if simple, has a significant effect on the extracted values of the diode parameters. Therefore, using the Rhoderick method to assess such diodes could introduce a high level of uncertainty to the extracted parameters due to the difficulty in determining the linear region of the I-V plot.

Cibils et al.[3] examined the limitation of the Rhoderick method compared to the ideal diode and its failure in determining the fundamental parameters for the non-ideal diode case with high series resistance. They divided the plot of $\ln(J)$ vs V into three regions

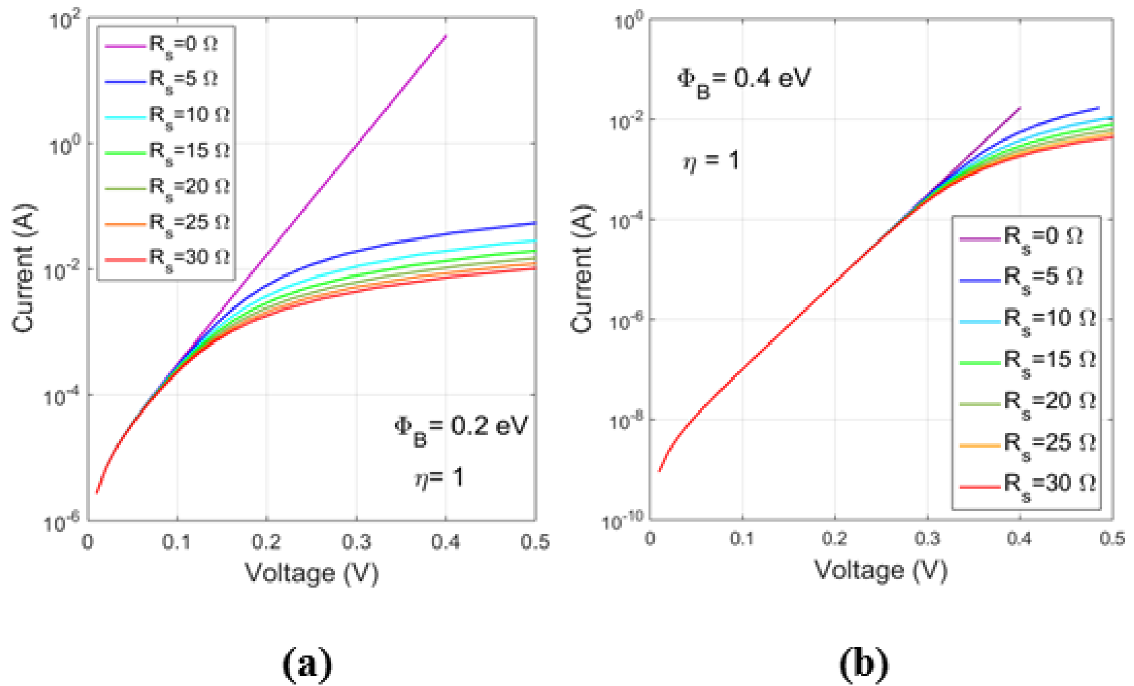

Figure 4-4 I-V characteristics of SBDs for a range of series resistance for n=1 , $A = 1.2 \times 10^{-7}\ cm^2$ *for different barrier heights (a)* $\Phi_B = 0.2\ eV$*, (b)* $\Phi_B = 0.4\ eV$*. Resistance as small as* 5Ω *can distort the linearity of the diode I-V curve.*

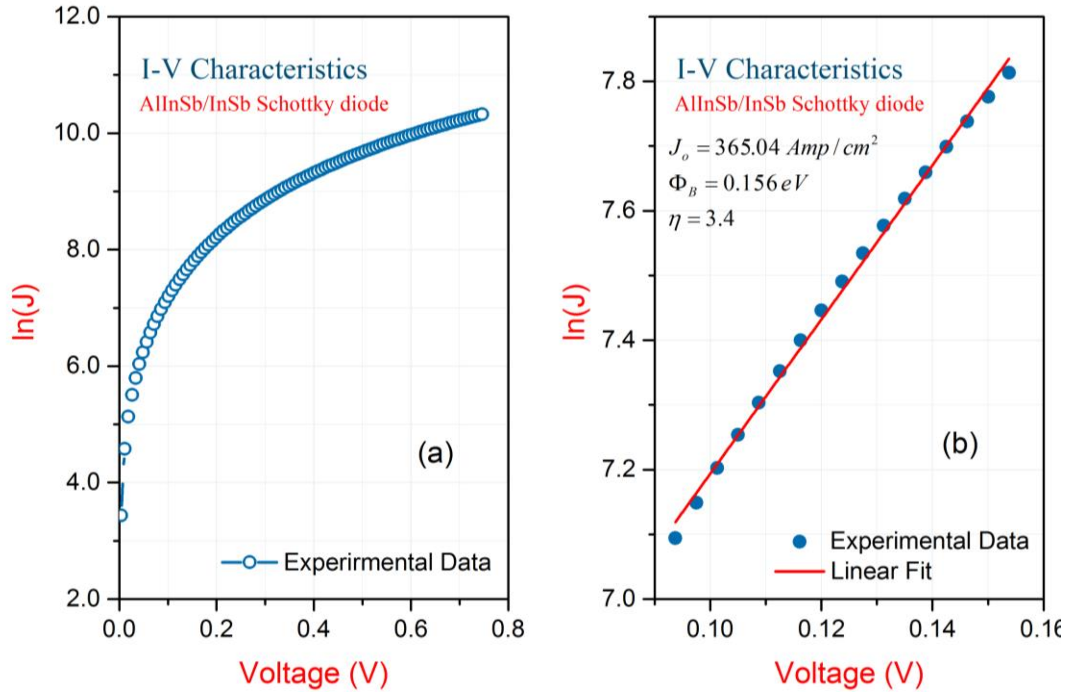

Figure 4-5 I-V characteristics of AlInSb-QW diodes at at 290K. (a) forward current vs the entire voltage range. (b) forward current at low voltage region 0.09-0.15 V that shows the best straight line over the whole voltage range.

as illustrated Figure 4-6. The first region is within the low voltage zone, extending from 0 V and ending at a certain voltage (V_{Min}). This non-linear area represents the non-exponential characteristic of Schottky diodes. The maximum limit of this region has been proven to be an increasing function of the ideality factor as in the following expression:

$$V_{Min} = 0.115\,\eta \tag{4-6}$$

Consequently, the beginning of the second region (linear) can be highly affected by a high value of ideality factor η. Therefore, the second region for a diode with large of ideality factor extends and affects the second region. Another modification to the linear region arises from the third region where the voltage drop across the series resistance affects the continuity of the liner part. As the series resistance increases, the upper limit (V_{Max}) of the second region declines. The lower limit of the third region (V_{Max}) can be determined from the expression:

$$V_{Max} \cong 0.25\,\eta\,\ln(1 + 2.5 \times 10^{-4}\frac{\eta}{RI_s}) \tag{4-7}$$

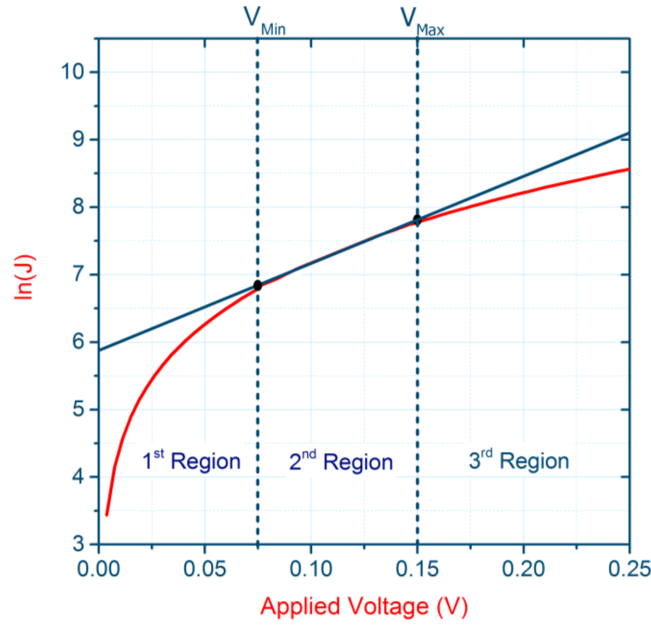

Figure 4-6 Current density vs voltage for a non-ideal AlInSb-QW based Schottky barrier diode with a series resistance (dotted line) and the liner extrapolation (sold line). The regions of Cibils et al are illustrated.

It is apparent from equation (4-7) that both ideality factor and series resistance can hugely affect the value of V_{Max}. For non-ideal diodes with high series resistance, it is very common for the calculated values of V_{Min} and V_{Max} with equation (4-6) and (4-7) to follow the following relation:

$$V_{Max} \leq V_{Min} \tag{4-8}$$

and it is apparent from the above equation that any diode following this relation does not possess the linear region in the current-voltage semi-log plot due to the overlapping of the first and third region.

To conclude, SBDs parameters can only be evaluated accurately when I-V plots show linearity over a sufficient voltage range. For SBDs with extremely low barrier height and high series resistance, the linear region in a $\ln(J)$ versus V plot disappears completely. For R_s higher than 5 Ω, the I-V curve must be corrected by using methods proposed by Norde, Cibils, Werner, and Cheung. In the sections that follow, the most common methods used to analysis SBDs with high series resistance will be described. The electrical analysis of fabricated AlInSb/InSb SBDs will be presented after the description of each method.

4.3.1 Norde Method

Norde proposed a novel method to estimate the Schottky barrier height of a diode with a high series resistance even in the absence of the straight region of a $\ln(J)$ versus V plot[5]. He proposed an empirical function $F(V)$ to represent the I-V measurements of SBDs. The Norde method assumed the case of ideal diodes only where $\eta = 1$ and a known Richardson constant A^{**} for simplicity. He also ignored the effect of the bias dependence of barrier height on his function F(V). The empirical function of Norde is defined as:

$$F(V) = \frac{V}{2} - \frac{KT}{q} \ln\left(\frac{1}{AA^{**}T^2}\right) \quad (4\text{-}9)$$

By using the modified TE model, equation (4-2), and equation (4-9), Norde function can be expressed regarding Φ_B and R_s, and for voltages higher than $3KT/q$, as:

$$F(V) = \Phi_B + IR_s - \frac{V}{2} \quad (4\text{-}10)$$

A plot of the Norde function against V results in a curve with minima as illustrated in Figure 4-7. The barrier height and series resistance can be determined by finding the values of $F(V)$, V, and I at the minimum point and then substituting the extracted values of $F(V_o), V_o$, and I_o in the following equations (4-11), and (4-12).

$$\Phi_B = F(V_o) + \frac{V_o}{2} - \frac{KT}{q} \quad (4\text{-}11)$$

$$R_s = \frac{KT}{qI_o} \quad (4\text{-}12)$$

Although the Norde method has successfully tackled the effect of diode series resistance, it has certain limitations in terms of ignoring other important factors which might affect the accuracy of the results. The main limitation, however, is to consider the ideal diode case which implies a diode of pure TE current, ignoring the effect of other transport mechanisms such as recombination current a trap assisted tunnelling of the carriers in localised states within the depletion region. Another problem with this method is that it fails to take the bias independent of Φ_B into account. Contributions of other current transport mechanisms to the diode current and/or a bias dependent barrier height can alter the curve shape and shift the location of the minimum point.

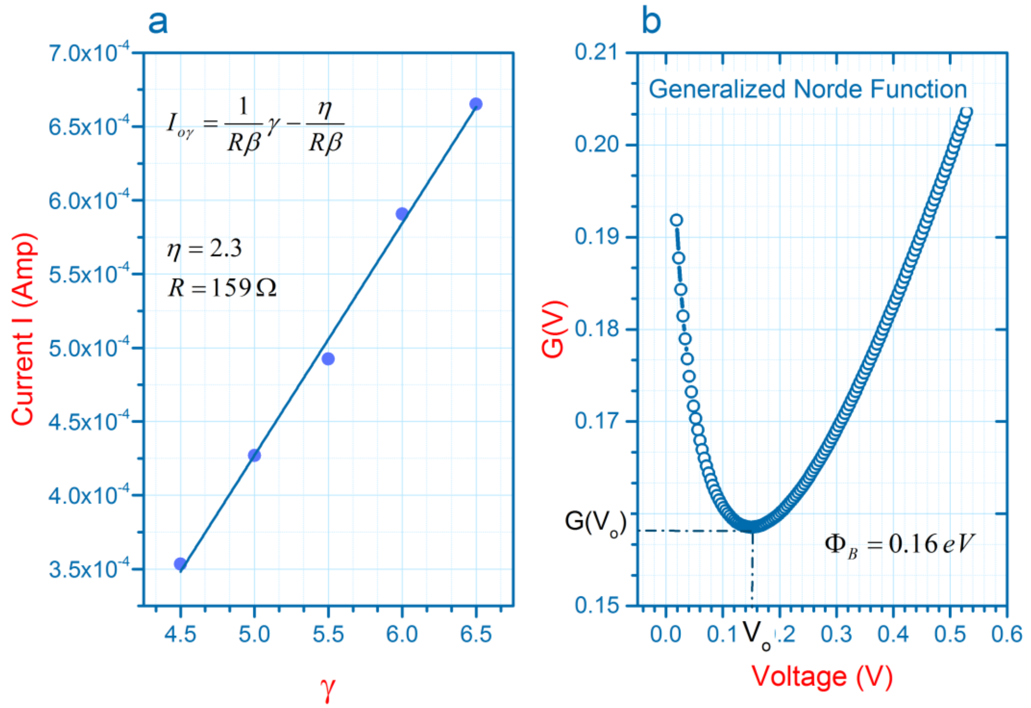

Figure 4-7 plots of an AlInSb/InSb based Schottky diode(a) Io against γ plot, used to extract η and R_s, where I_o represent the current at V_o for different values of γ. This plot is linear for γ≥4.5 (b) Th generalized Norde function G(V) vs voltages used to extract the barrier height.

McLean [11] has shown that a substantial contribution of recombination current will result in an underestimate of Φ_B while a bias-dependent barrier will result in an overestimate of Φ_BThe final limitation of this method is that it depends on one point of the I-V characteristic in determining the diode parameters. This factor can introduce another source of error to the outcomes of this approach.

Many researchers[3, 6, 8, 10] have tried to improve the Norde method to minimise sources of error and overcome its drawbacks. Some researchers have introduced the ideality factor to the Norde equation while others have used several minima points instead of one point as in the Norde method. Sato and Yasumura[6] incorporated the ideality factor η in the Norde function and expanded it to determine the values of η, Φ_B, R_s from two set of I-V measurements to be taken at different temperatures . This method is applicable to any diode with an ideality factor $1 < \eta < 2$ using the following equation [6].

$$F(V) = \left(\frac{1}{2} - \frac{1}{\eta}\right)V + \Phi_B + \frac{IR_s}{\eta} \tag{4-13}$$

Another extension to the Norde equation was described by Bohlin[10] which made it possible to calculate all Schottky barrier parameters from one set of I-V measurement of Schottky diode. His equation is known as the Generalized Norde equation.

$$G_\gamma(V,I) = \frac{\mathrm{V}}{\gamma} - \frac{\mathrm{KT}}{\mathrm{q}}\ln\left(\frac{1}{A^{**}AT^2}\right) \tag{4-14}$$

Lien et al.[8] introduced a parameter (γ) to the Norde equation to generate several Norde like functions $G_\gamma(V,I)$, where (γ) is an integer number larger than the ideality factor. The Lien et al function is given by the following expression:

$$G_\gamma(V,I) = \frac{\mathrm{V}}{\gamma} - \frac{\mathrm{KT}}{\mathrm{q}}\ln\left(\frac{1}{A^{**}AT^2}\right) \tag{4-15}$$

The values of the effective barrier height and the diode series resistance can be determined from equations (4-16 and (4-17.

$$\Phi_B = F(V_o) + \frac{V_o}{\gamma} - \frac{\mathrm{KT}}{\mathrm{q}} \tag{4-16}$$

$$R_s = \frac{\mathrm{KT}(\gamma - \eta)}{\mathrm{qI}} \tag{4-17}$$

where (γ) is an arbitrary number larger than the ideality factor. Plotting $G_\gamma(V,I)$ against I for several values of γ result in several Norde like curves. Thus, several values of $(I_{o\gamma})$ can be obtained at the minima of each $G_\gamma(V,I)$ curve. A plot of $I_{o\gamma}$ against γ results in a straight line defined by equation (4-18). The series resistance and ideality factor can be extrapolated from the slope and the intercept with the y-axis respectively.

$$I_{o\gamma} = \frac{1}{R\beta}\gamma - \frac{\eta}{R\beta} \tag{4-18}$$

where $\beta = \frac{q}{kT}$.

The generalised Norde method was used to evaluate the fundamental parameters of AlInSb/InSb Schottky diodes as illustrated in Figure 4-7. Figure (a) shows a plot of $I_{o\gamma}$ versus γ, five values of $I_{o\gamma}$ were found at five values of γ (4, 4.5, 5, 5.5, and 6). From the slope and the intercept, the values of the series resistance R_s, and the ideality factor η were found to be 159 Ω and 2.3 respectively and the value of the barrier height was

0.16 eV.The results reveal that a high series resistance degrades the diode performance. The barrier height extracted with this method is higher by 0.04 eV than the barrier extracted with the Rhoderick method while the value of the ideality factor is considerably reduced from 3.4 to 2.3. This alteration is quite reasonable due to the effect of R_S on the slope and intercept of the $\ln(J)$ versus V plot, considering the value of the slope is derived more from the resistance than the intercept value.

Another modification of the Norde method was proposed by Cibils and Buitrago[4]. They replaced the Norde Function with a new form as in the following expression:

$$F(V) = V - V_a \ln I \tag{4-19}$$

where, (V_a) is an arbitrary voltage parameter independent of the voltage and current. In a similar way to the Lien method, the current at a minimum (I_o) is found for several values of V_a. A plot of I_o against V_a results in a straight line defined by equation (4-20. With this linear relation it is possible to obtain R_S and η easily.

$$I_o = \frac{V_a}{R} - \frac{\eta}{\beta R} \tag{4-20}$$

The Cibils method was used to evaluate the series resistance and ideality factor of two AlInSb/InSb Schottky diodes with different barrier heights. The generated Cibils curves of the Schottky diode with lower barrier height whose I-V measurements are presented previously in Figure 4-1, are shown in Figure 4-8. Plot (a) represents the modified $F(V)$ against V for various values of V_a, and figure (b) shows a plot of the extracted I_o against V_a. According to this method, the values of the ideality factor and series resistance were found to be 2.63 and 131.5 Ω respectively. Although these results are in good agreement with the corrected data of Rhoderick's method $(\eta = 2.7)$ and $(R_s = 133\ \Omega)$, Cibils method can introduce errors to the extracted parameters if the I-V data is measured at large voltage steps. The Cibils method is very sensitive to the voltage steps, large voltage steps introduce an error to the I_o values and therefore the extracted parameters. Voltage steps of 3.6 mV in measurements of the diode with higher barrier height lead to a considerable overestimation in the ideality factor value.

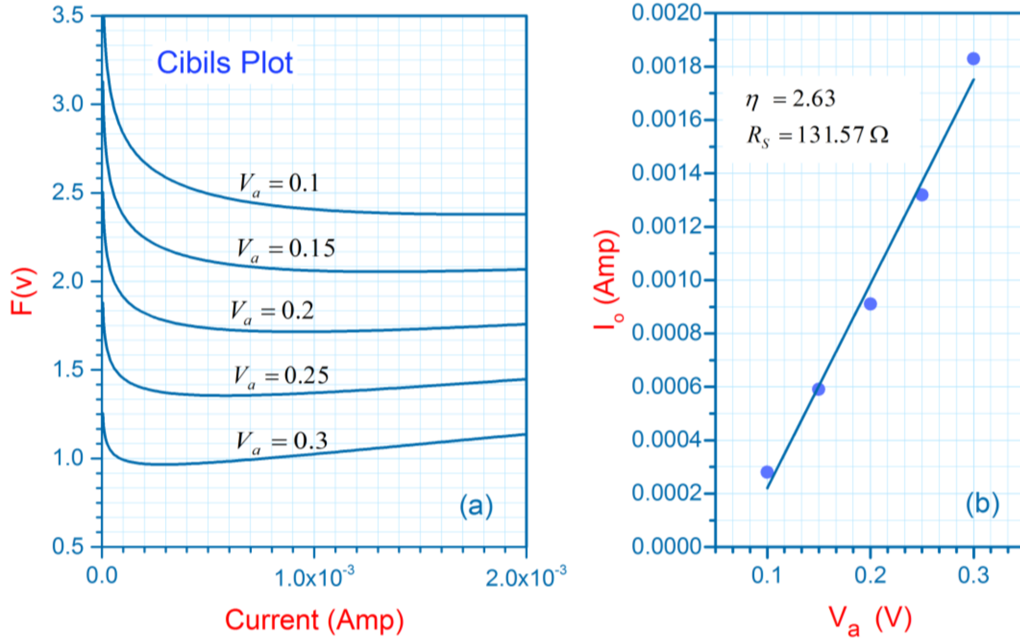

Figure 4-8 Experimental plots of an AlInSb/InSb based Schottky diode as for the Cibils method (a) Cibils function F(V) vs current at different values of Va. (b) Io against Va. where of η and R_S can be deduced.

4.3.2 Werner Method

Werner[15] proposed another approach to estimate all Schottky diode parameters $(\Phi_B, \eta,\ R_S, I_o)$ from the I-V measurements, using three different plots. One of the plots was previously used by Cheung but, Werner argued that the conductance (G) plot is the most accurate one in evaluating η and R_S. In the following, the conductance plot will only be considered. The diode differential conductance $(G = dI/dV)$ can be obtained by differentiating the current given by equation (4-2 with respect to the voltage at forward bias, this yield:

$$\frac{G}{I} = \frac{q}{\eta KT}[1 - GR] \tag{4-21}$$

which shows that a plot of G/I against G will produce a straight-line which intercepts the x-axis at $1/R_S$ and the y-axis at $q/\eta kT$. The differential conductance can be calculated from the I-V measurement. To reduce the noise impact on the differential conductance, it is important to take the measurement using small voltage steps. Once

R_S is evaluated, it can be used to correct the voltage-axis of the I-V characteristics and determine the barrier height and ideality factor following the traditional method of Roderick. The differential conductance plot of a AlInSb/InSb Schottky diode and the corrected I-V curve are shown in Figure 4-9. It is apparent that the plot doesn't exhibit linearity as suggested, due to low barrier height[9], however, it doesn't affect the intercept with the x-axis. Therefore, the extracted series resistance, 119 Ω, from the conductance plot was used to correct the I-V data and to obtain the other diode parameters, ($\Phi_B = 0.161\ eV$) and η, with the standard method as illustrated in figure (b) and were $0.161\ eV$ and 2.98 respectively. The upward curvature in the plots at high voltage reveals inaccuracy in the extracted diode parameters. To validate the accuracy of this method, the extracted diode parameters were used to model I-V characteristics and compare it to the experimental one as shown in Figure 4-10 at two different scales. The figures reveal that the modelled I-V characteristics fit well to the experimental data at high voltages and depart the fitting at low voltages which is consistent with the uncertainty in determining the diode parameters.

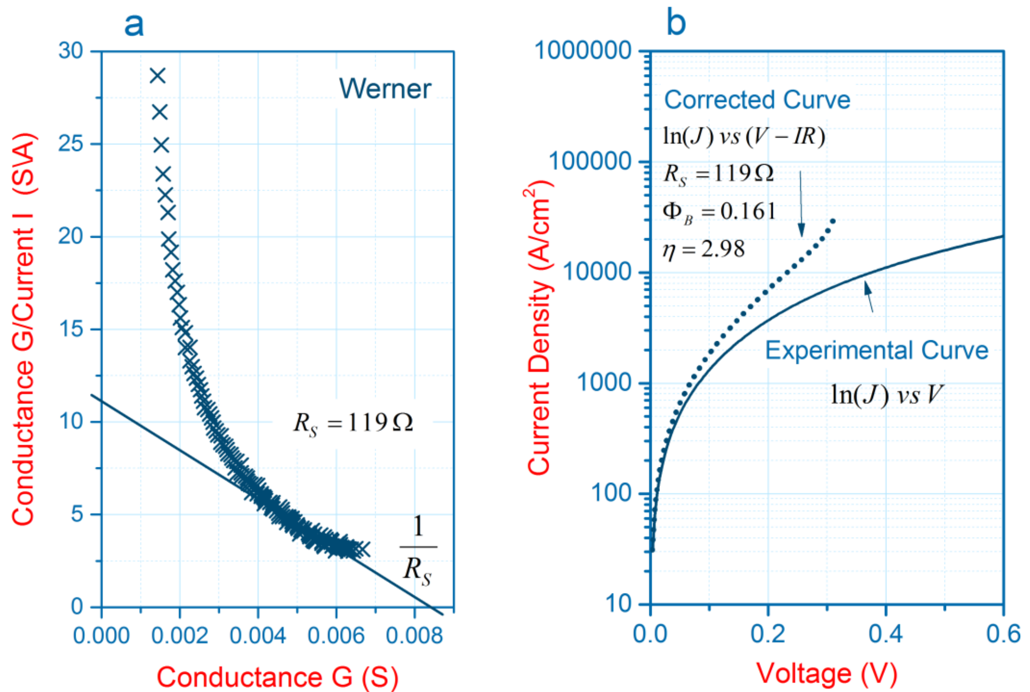

Figure 4-9 (a) Werner conductance plot of AlInSb/InSb-QW Schottky diode, and (b) the corrected (I-V) characteristics (dotted line) used to evaluate (Φ_B) and (η). G was calclated from the experimental (I-V) data.

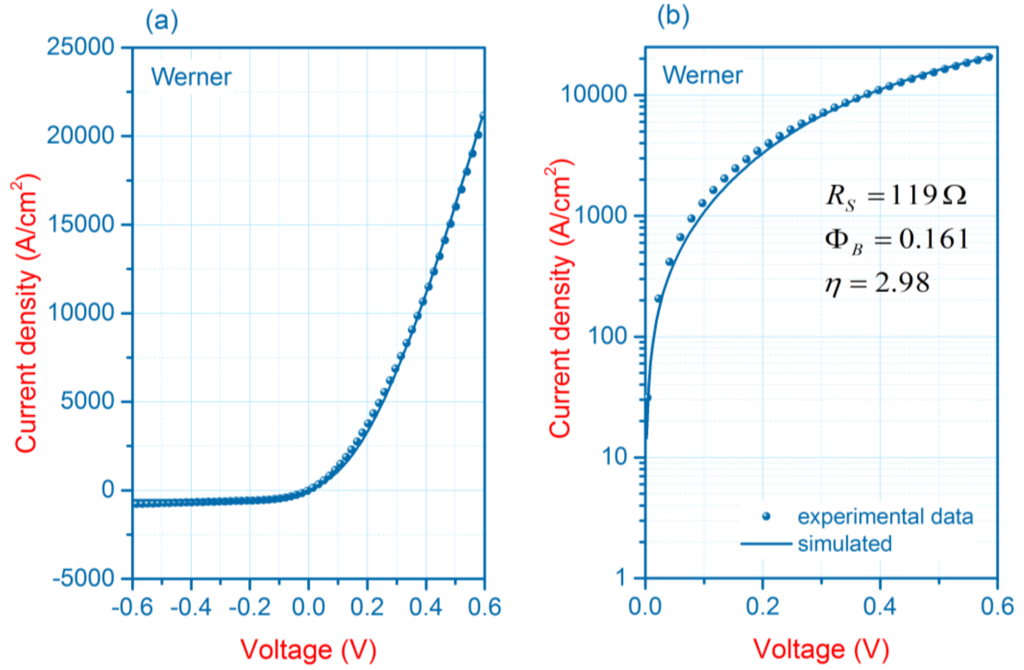

Figure 4-10 Experimental I-V characteristics of AlInSb/InSb-QW based Schottky diode compared to a modelled curve using TE model with $\eta = 2.98$, $\Phi_B = 0.161\ eV$, *and* $R_s = 177\Omega$ *obtained by Werner method. (a) Forward and reveres bias in normal scale. (b) Forward bias in semilog scale.*

4.3.3 Cheung Method

Cheung presented another approach to evaluate Schottky diode series resistance in addition to the barrier height, and ideality factor, from a single I-V measurement. Cheung method is based on the modified TE model, equation (4-2), to drive the following mathematical expressions which are known as Cheung's equations[4]:

$$\frac{d(V)}{d(\ln J)} = R_s AJ + \eta KT/q \quad (4\text{-}22)$$

$$H(J) = V - \eta \frac{KT}{q} \ln(\frac{I}{AA^{**}T^2}) \quad (4\text{-}23)$$

$$H(J) = R_s AJ + \eta \Phi_b \quad (4\text{-}24)$$

According to equation(4-22), a plot of $d(V)/d(lnJ)$ against J should yield a straight line in the downward curvature region of the I-V characteristic with an intercept and slope giving the value of η and R_s respectively. Substituting η and the data of the same voltage range in equation (4-23) yields $H(I)$. Then a plot of $H(I)$ versus J according to eq. (4-24) should result also in a straight line with a slope of $R_s A$ and intercepts the y-axis at $\eta\Phi_B$ another value of R_s can be obtained from this function. Therefore, the two values of the diode resistance can be used as a measure of these methods accuracy. Two plots of Cheung's functions for two different AlInSb/InSb Schottky diodes, and the corresponding diode parameters are shown in Figure 4-11. The two diodes of varied barrier heights were selected to show the difficulty in determining the parameters of SBDs with considerably low barrier height. Figure (a) refers to a Schottky diode with extremely low barrier height ($\Phi_B = 0.16\,eV$), and (b) to a Schottky diode with low barrier height ($\Phi_B = 0.36\,eV$). The values of the diode parameters (R_s, η, and Φ_B) obtained from the linear fit of $d(V)/d(lnJ)$ against J plot, and $H(V)$ versus J plot, are summarized in Table 4-1. It is worth mentioning that the difference in the barrier heights and series resistance is owing to differences in

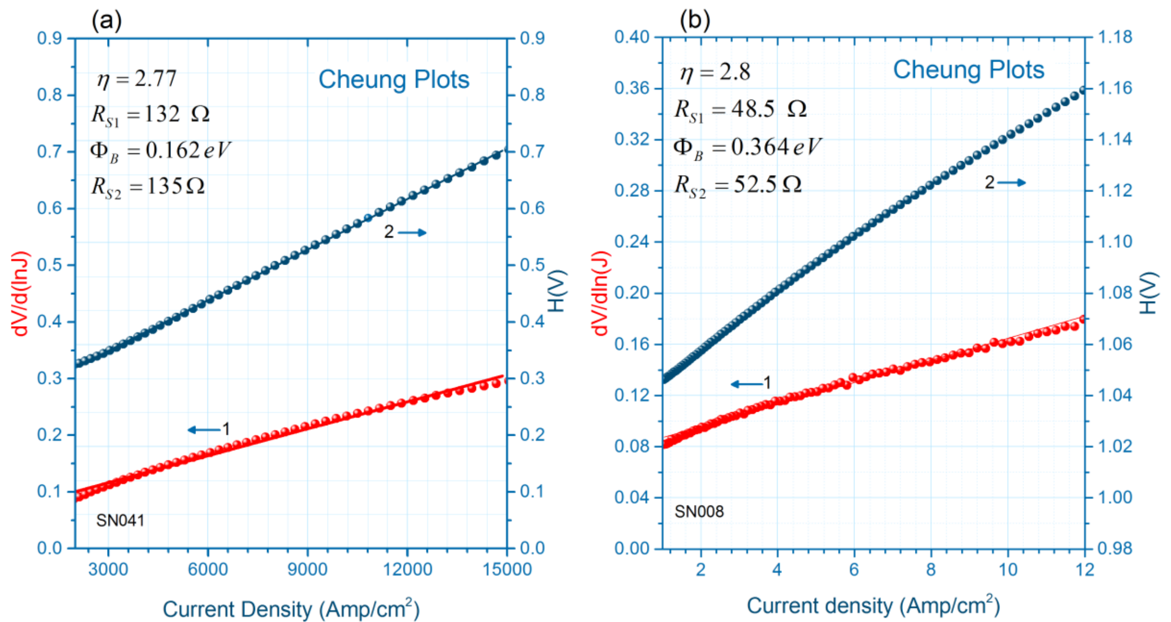

Figure 4-11 Cheung's functions H(V) and dV/d(lnJ) calculated from the experimental (I-V) measurements of AlInSb/InSb based Schottky diodes and plotted against the current density (J). The red circles and blue squares represent dV/d(lnJ) and H(V) respectively. The solid lines represent their liner fits.

Table 4-1 The parameters of two AlInSb/InSb based SBDs with different barrier heights calculated with Cheung approach.

Area (cm2)	Φ_B (eV)	η	R_{s1} (Ω)	R_{s2} (Ω)
1.2×10^{-7}	0.16	2.77	132	135
2×10^{-4}	0.36	2.8	48.5	52.5

geometry, materials and surface preparation applied for each diode. Both Cheung plots for each diode with different barrier height showed linearity over nearly the same voltage range with a slight shift in the lower voltage limit for the diode of lower barrier height. The good agreement between the two obtained values of R_S for each diode confirms the consistency of the Cheung approach. Another way to check the accuracy of the extracted parameters with Cheung method was done by fitting the experimental data to a theoretically simulated I-V curve, generated by substituting the extracted parameters in the modified TE model, equation (4-2). A comparison between the experimental and theoretical curves of $\Phi_B = 0.16\ eV$ Schottky diode is illustrated in

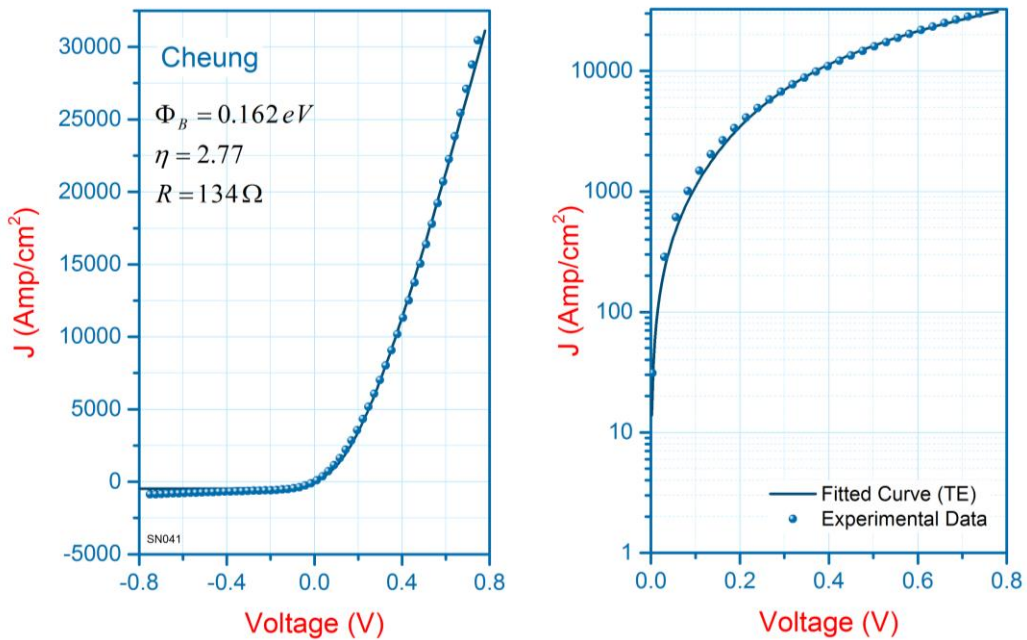

Figure 4-12 Experimental I-V characteristics of AlInSb/InSb-QW based Schottky diode compared to a simulated curve using TE model with $\eta = 2.77$, $\Phi_B = 0.162 eV$, and $R_s = 134\ \Omega$ obtained by Cheung method. (a) Forward and reveres bias in normal scale. (b) Forward bias in log scale.

Figure 4-12 in two ways. Figure (a) is a plot of J versus V over the whole voltage range -0.75 to 0.75 V whereas figure (b) shows the same data in a semilog scale in the forward bias. It is apparent that the calculated curves match very well to the experimental data but, they slightly deviate from the experimental data at low and high voltages, which reveals uncertainty in the extracted values of the parameters. Further analysis was done by correcting the I-V data by deducing the voltage drop across the series resistance from the experimental data, following a method proposed by Lien[8].

After correction, a plot of $\ln(J)$ versus $V - IR_s$ curve should result in a straight line, made it possible to determine the ideality factor and Schottky barrier height with the standard method of Rhoderick. This method was applied into two diodes to show the effect of the barrier height value on the accuracy of this method. The corrected data of the two AlInSb/InSb Schottky diodes (whose parameters are illustrated in Table 4-1) paired with the uncorrected one are shown in Figure 4-13. Plot (a) is for the diode of lower barrier height $(\Phi_B = 0.16\ eV)$ and (b) is for the diode of the higher barrier $(\Phi_B = 0.36\ eV)$. From the figure, it is apparent that the I-V characteristics of both diodes have improved after the correction, but the diode of the larger barrier height

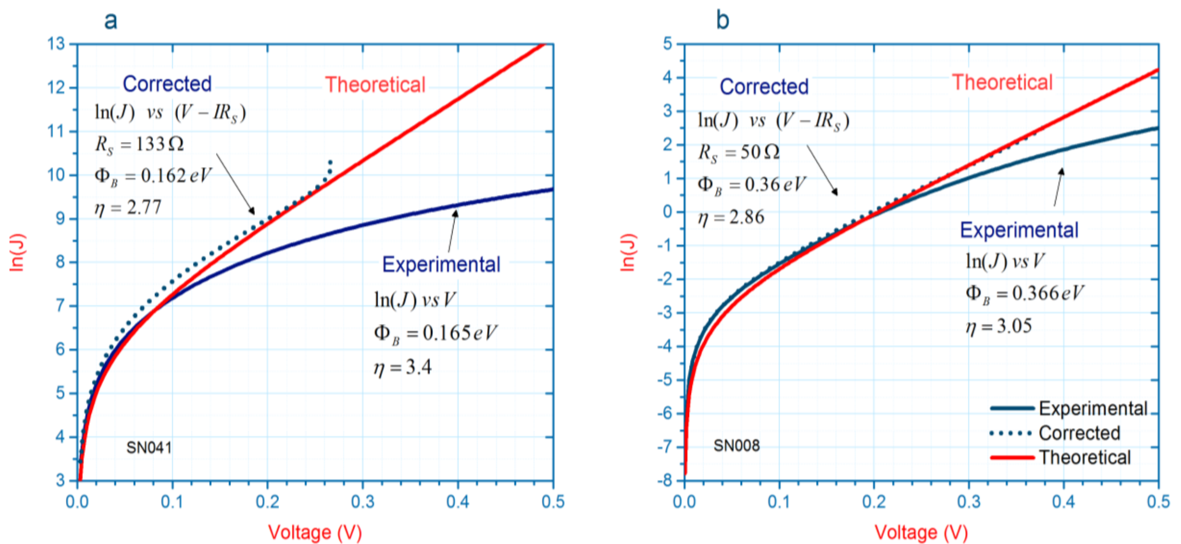

Figure 4-13 Experimental plots of ln(J) against V (sold blue lines) and their corrected plots (dotted blue lines) compared to theoretical curves (sold red lines) for two different AlInSb/InSb diodes. (a) A diode with 0.162 eV barrier height, η=2.86 and Rs=131.5 Ω, and (b) A diode with 0.366 eV barrier height, η=3.05 and Rs=50 Ω.

exhibited an excellent linearity and matches the theoretical curve over the whole voltage range. This result is in contrast to the diode with the extremely low barrier height ($\Phi_B = 0.16\ eV$) where the corrected I-V curve matches the theoretical curve at a limited voltage range and shows upward curvature at high voltage ranges. These results reveal that an accurate determination of diode parameters can only be achieved for diodes up to a certain low limits of barrier height where the semi-loge plot of I-V measurement exhibits linearity over a sufficient voltage range. The length of the linear part is a function of barrier height, ideality factor and diode series resistance.

4.4 Barrier Height and Fermi Level Pinning

The bandgap energy of both AlInSb/InSb substrates used to fabricate the Schottky diodes was determined using the expression[17]:

$$E_g = 0.17 + 1.67x + 0.43x^2 \tag{4-25}$$

where x is the Al fraction in $Al_xIn_{1-x}Sb$ alloy. It obvious that the bandgap energy of the top barrier increases as the Al content increases. Once the bandgap is estimated, Schottky barrier height can be estimated as well, assuming FL pinning. The values of bandgaps and Schottky barrier heights for both structures are illustrated in Table 4-2.

The Schottky barrier height were estimated assuming a strong Fermi level pinning at $\frac{1}{3}E_g$, and a weak FL pinning at $\frac{1}{2}E_g$. The extracted Schottky barrier height according to Cheung model are also included in the table for the purpose of comparison. From the

Table 4-2 The estimated values of the bandgap energies and barrier heights of the Schottky diodes built on different AlInSb/InSb substrates with different Al fractions compared to the experimental values of Schottky barrier heights.

Top barrier layer	$Al_{0.15}In_{0.85}Sb$	$Al_{0.2}In_{0.8}Sb$	Comments
Al fraction	0.15	0.2	
$E_g\ (eV)$	0.43	0.52	
$\Phi_B\ (eV)$	0.29	**0.35**	**Assume FL pinning at** $\frac{1}{3}E_g$
$\Phi_B\ (eV)$	**0.22**	0.26	**Assume FL pinning at** $\frac{1}{2}E_g$
$\Phi_B\ (eV)$	**0.16**	**0.36**	**Experimental-Cheung model**

table, it is apparent that the estimated barrier height $(0.35\ eV)$ of the Schottky diode based on the larger bandgap $0.52\ eV$ material is in good agreement with the experimental barrier height value $(0.36\ eV)$. This result indicates a strong Fermi level pinning at $\frac{1}{3}E_g$. However, the value of the extremely low barrier height $(0.16\ eV)$ of the SBD built on the lower bandgap material is lower than the material mid-gap energy $\left(\frac{1}{2}E_g = 0.22\right)\ eV$. The reduced barrier height suggests two possible explanations. The first explanation assumes a FL depinning so that the barrier height is following the Schottky-Mott rule, implying that the barrier height can be determined from the work functions difference of the metal and AlInSb alloys. The second explanation assumes a weak FL pinning around the mid-gap of the semiconductor, taking in consideration the effects of the barrier lowering $0.02 - 0.04\ eV$, and diode series resistance.

The energy band structures of the two AlInSb/InSb layers used to fabricate the Schottky diodes are schematically shown in Figure 4-14, (a) a base layer with a cap layer of the lower Al content, $Al_{0.15}In_{0.85}Sb$, and energy-gap of $0.43\ eV$, and (b) a base layer of a cap layer with the higher Al content, $Al_{0.20}In_{0.8}Sb$, and energy-gap of $0.52\ eV$.

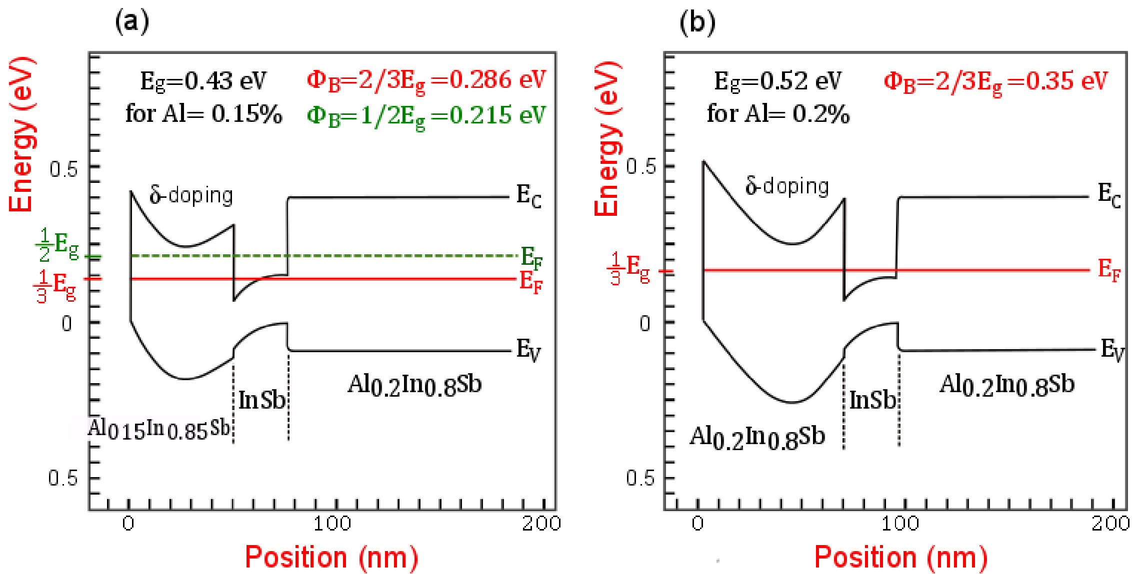

Figure 4-14 Conduction band profiles of the two AlInSb-QW heterostructure layers used to fabricate the Schottky diodes. (a) of a cap layer with a lower energy-gap (E_g = 0.43) eV due to lower Al content, $Al_{0.15}In_{0.85}Sb$ and, (b) of cap layer with higher energy-gap (E_g = 0.52) eV due to higher Al content in the alloy, $Al_{0.2}In_{0.8}Sb$.

4.5 Summary and Conclusions

In this chapter, the current-voltage I-V characteristics of two AlInSb/InSb Schottky diodes have been investigated under forward bias using various techniques. Two diodes of two extreme cases of barrier heights have been chosen to show the effect of extremely low barrier height on the extracted parameters. The obtained Schottky diodes parameters (Φ_B, η, R_s) of all the applied methods are summarised in Table 4-3. Despite the scattered results, all the analyses methods apart from Rhoderick method reveal a large diode series resistance R_s leading the diode current in forward bias. Therefore, R_s is one of the leading causes of non-ideality in AlInSb/InSb Schottky barrier diodes. The barrier height 0.36 eV of the SBD which was built on the as grown materials layer was found to follow the one-third bandgap pinning rule, indicating a strong FL pinning. However, the low effective barrier height of 0.16 eV for the SBD built on a treated material, surface etch with citric acid, indicates a suppression to the strong FL pinning at the metal/AlInSb interface.

The table is quite revealing in different ways, first, the barrier height and ideality factor for the lower barrier diode $\Phi_B < 0.2\ eV$, are correlated with the diode series resistance but the ideality factor is more sensitive to R_s than Φ_B. The overestimation in ideality factor and underestimation in barrier height obtained by the standard Rhoderick method is due to the overlapping of R_s region in the I-V curve with the low voltage area.

Table 4-3 The fundamental Parameters of two AlInSb/InSb-QW based Schottky diodes of different barrier heights evaluated using six different methods. The measurements and the calculation were implemented at 290 K.

	$\Phi_B < 0.2\ eV$			$\Phi_B > 0.3\ eV$		
Method	η	$\Phi_B\ (eV)$	$R_s\ (\Omega)$	η	$\Phi_B\ (eV)$	$R_s\ (\Omega)$
Rhoderick	3.4	0.156	N.C[1]	3.05	0.36	**N.C**
Corrected I-V	2.77	0.162	133	2.72	0.37	**50**
Norde[2]	2.3	0.16	159	2.6	0.39	**79**
Cibils	2.63	N.C	131.5	3.3	N.C	**41**
Werner	2.98	0.161	119	2.77	0.37	**41**
Cheung	2.77	0.162	131, 135	2.83	0.37	**48, 52**

1: Not considered in the method., 2: generalized equation

However, the error level between Roderick method and the modified methods has been reduced in the diode with the larger barrier height $(\Phi_B > 0.3\ eV)$.

The uncertainty in the extracted parameters are mainly due to the extremely low barrier height of AlInSb/InSb Schottky diode, and due to limitations in each method. One of the main limitations which might introduce errors into the results is the method sensitivity to current or voltage steps; large voltage steps lead to an error in determining the minimum point in the auxiliary functions of Norde and Cibils. Moreover, large voltage steps introduce noise in calculating the differential conductance of Werner method. Another important source of error is considering the hypothesis of voltage independent barrier height in all the used analytical methods. Uncertainty in the results can also attribute to the noise and measurement uncertainty.

4.6 Bibliography

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Chapter 5

Temperature-Dependent Current-Voltage Characterization of AlInSb-QW Based Schottky Diodes

5.1 Introduction

The room temperature analysis of Schottky barrier diodes based on I-V characterisation enables the extraction of several important parameters of the Schottky diodes as discussed in chapter 4, but it doesn't provide detailed information about the electron transport mechanism or the nature of the barriers formed at the metal semiconductor interface. However, temperature dependent current-voltage measurement I-V-T is a much more effective tool in characterizing the electron transporting mechanisms in the MS contacts. In the ideal Schottky barrier diode, the forward diode current is governed by thermionic emission TE which is related to the carriers emission from the semiconductor to the metal over a spatially homogeneous barrier. The generated current I according to TE theory is given by the expression

$$I = I_o \left[\exp\left(\frac{q(V - IR_s)}{\eta kT} \right) - 1 \right] \qquad (5\text{-}1)$$

where, and (I_o) is the saturation current (V) is the applied voltage, (R_s) is the diode series resistance, (η) is the diode ideality factor, and (q) is the electron charge, (k) is Boltzmann constant, and (T) is the temperature. The value of the saturation current $(I_o$ is given the expression

$$I_o = AA^{**}T^2 \exp\left(-\frac{q\Phi_B}{kT}\right) \tag{5-2}$$

where, A is the Schottky diode area, A^{**} is the semiconductor Richardson constant, and Φ_B is the effective Schottky barrier height. The understanding of the current mechanism over the Schottky barrier is an essential step into explaining the observed results. Experimentally, the effective Schottky barrier height as well as the Richardson constant can be extracted from the I-V-T measurements using a traditional Richardson plot. Ideally, for a Schottky diode governed by a purely TE mechanism, the Richardson plot, which can be generated by plotting $\ln\left(\frac{I_o}{AT^2}\right)$ versus T^{-1}, should exhibit linearity over the entire range of temperatures. However, for some real Schottky diodes, several deviations from the ideal behaviour of the Richardson plot have been reported and studied. It has been found that Schottky diodes with temperature and bias dependent barrier heights and ideality factors, show a curvature in the $\ln(J)$ verses V plot. Therefore, the extracted value of the saturation current, used to construct the Richardson plot, is extremely influenced by the selected bias range used for curve-fitting and leads to a deviation in the Richardson plot.

In many studies[1-9], analyses of temperature-dependent measurements I-V-T have deviated from the TE model. An abnormal decrease in Φ_B accompanied by an abnormal increase of η with a decrease in temperature, have been observed. The increase of the ideality factor with decreasing temperature is known as the "T_o effect" and was first described by Padovani and Sumner[9]. Another abnormality was observed in the experimental value of the Richardson constant. The experimental A^{**} was found to be far less than its theoretical value, and in several cases, it is less than the theoretical value by orders of magnitude. Many researchers have tried to find out the cause behind this deviation (abnormal behaviour) and have proposed many different explanations. Some researchers have suggested that the variance of Schottky barrier height (SBH) with temperature should follow the variance of the band gap with temperature [10, 11], but it has generally been found experimentally that this SBH variance is not in agreement with the bandgap variance with temperature [1]. Image Force effects are another

possible explanation for the temperature dependence of the barrier height and ideality factor. However, a considerable contribution from other current mechanisms such as quantum mechanical tunnelling and trap assisted tunnelling, to the diode total current, could be a potential reason for all the observed anomalies. Other researchers have proposed that the anomalous behaviour in Φ_B, η, and the Richardson plot can be explained by using Werner and Guttler's model. The model adopted an analytical potential fluctuation assuming the formation of spatial barrier height inhomogeneities at the MS interface. This proposal has been able to explain most of the abnormal behaviour based on TE theory using a Gaussian distribution function for the barrier heights [12-15]. Other researchers have used Tung's model in which Schottky barriers with laterally inhomogeneous patches of varying barrier height is used [13-18]. Modified Richardson plots based on these assumptions have been used by various researchers to verify the validity of these models.

In this chapter, the forward-bias I-V-T measurements of AlInSb/InSb-QW Schottky diodes have been analysed over a wide range of temperatures. The analysis compares a number of the various proposed theories in an attempt to explain the abnormal behaviour of the Φ_B, (η), and the Richardson constant observed.

5.2 Temperature-Dependent Measurements for AlInSb/InSb Schottky Diodes

Experimental I-V-T measurements for typical AlInSb/InSb-QW based Schottky diodes have been carried out in the temperature range 3-290 K and are represented in a semi-logarithmic plot as shown in Figure 5-1. It is apparent from the figure that; **a)** in forward bias, at biases less than 0.3 V, the current grows exponentially with the applied voltage, while at higher voltage the rate of current growth decreases due to the significant effect of series resistance; **b)** it is also noticeable that the slope of the straight-line decreases as the temperature decreases. This behaviour indicates a contribution of the thermally activated electrons to the total diode current over the entire temperature range. Although pure FE is anticipated to dominate under 50 K, however, the small slope variation indicates an infinitesimal amount of thermally activated current at low temperatures possibly due the variation of the energy gap with temperature; **c)** at reverse bias the current continues to grow as the negative voltage increases, but the rate of growth of

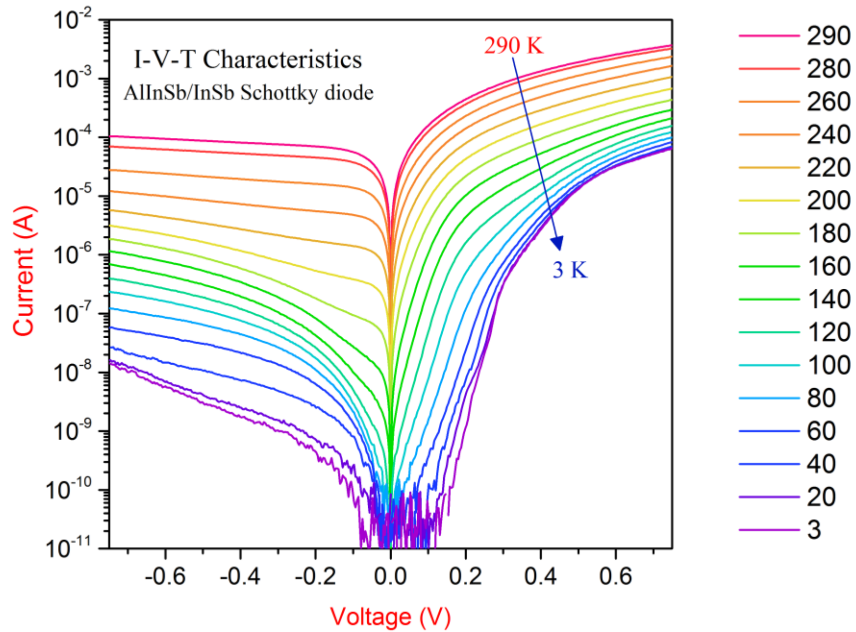

Figure 5-1 A semilog plot of the I-V characteristics for a typical AlInSb/InSb QW Schottky diode measured over a wide range of temperature, from 290 K down to 3 K.

the leakage current steadily decreases with the applied voltage, except for the curves below 50 K where pure FE is anticipated to be dominant; and **d)** at low bias, the temperature dependency of the leakage current at low reverse voltage is stronger than that at higher one. Based on these features, the current transport mechanisms of AlInSb/InSb Schottky diodes in forward and reverse bias directions will be discussed, considering various transport aspects.

5.3 Temperature Dependency of the Barrier Height and Ideality Factor

Based on the I-V-T measurements of a typical AlInSb/InSb Schottky diode, the zero-bias Schottky barrier height Φ_B and the ideality factor η have been evaluated accordingly at each temperature using TE theory. The extracted values of the barrier height and the ideality factor over the entire temperature range 3-290 K are shown in Figure 5-2. It is apparent from the figure that using this analysis both Φ_B and η are strongly temperature dependent. With decreasing temperature, the barrier height decreases steadily from a value of 0.37 eV at 290 K to a value of 0.002 eV at 3 K

whereas the ideality initially increases steadily from a value of 2.75 at 290 K to a value of 4.75 at 150 K and then rises sharply to reach a value of ~230 at 3 K. It is worth commenting that all tested devices with barrier heights of 0.34-0.37 eV showed the same behaviour, whereas devices with lower apparent barrier heights $\Phi_B = 0.16\ eV$ showed less temperature-dependence of the barrier height over the temperature range of 150-300 K. The strong temperature-dependence of the barrier height and ideality factor can be attributed to several reasons. The most common explanation is the deviation from the pure TE theory due to the contribution of other current mechanisms, mainly thermionic field emission TFE, and field emission (tunnelling, FE) through the barrier, and also recombination current in the depletion region [4, 6]. Barrier lowering due to image force effects can also contribute to the abnormal reduction in barrier height with temperature. Another possible explanation of the temperature-dependent barrier height and ideality factor is attributed to the theory of barrier inhomogeneity which assumes a formation of a laterally nonuniform Schottky contact with different barrier heights of Gaussian distribution [11, 19, 20]. In the next sections, the temperature dependency effect of Φ_B and η of the AlInSb/InSb based Schottky diodes will be discussed taking into consideration different possible explanations.

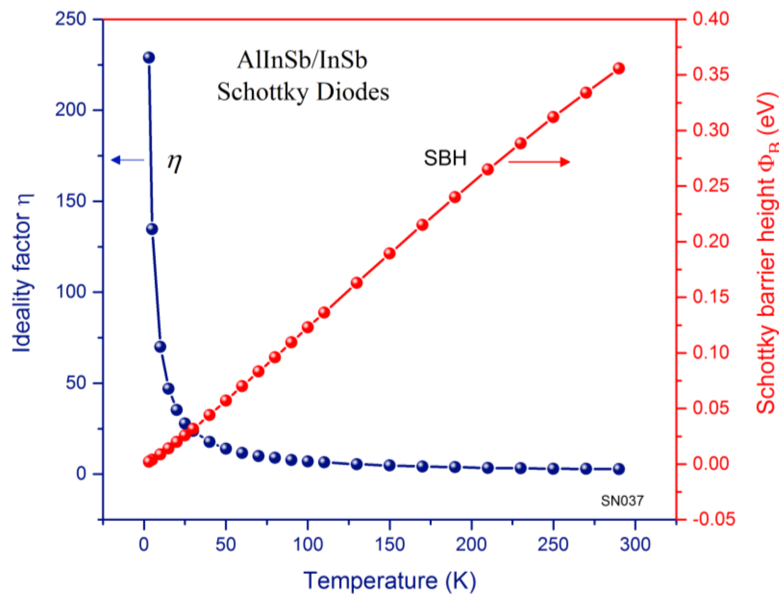

Figure 5-2 Temperature-dependence of the barrier height and the ideality factor for AlInSb/InSb-QW based Schottky diode at temperatures ranging from 3-290 k.

5.4 Temperature Dependence of the $Al_xIn_{1-x}Sb$ Energy Bandgap

For pure thermionic emission, the temperature dependence of the Schottky barrier height should follow the variance of the bandgap energy with temperature. The bandgap energy is anticipated to have larger values at lower temperatures than at higher temperature. For $Al_xIn_{1-x}Sb$ alloy, the bandgap energy $E_g(x,T)$ as a function of composition and temperature can be determined using the empirical expression [21]:

$$E_g(x,T) = 0.235 - \frac{3.2\times10^{-4}T^2}{T+170} + 1.721x - \left(\frac{4.2}{T+140} - \frac{3.2}{T+170}\right)10^{-4}T^2x + 0.43x^2 \quad (5\text{-}3)$$

where (x) is the Al fraction. The estimated bandgap energies of the high barrier layers of two different AlxIn1-xSb alloys (Al fraction 0.15 and 0.2) are shown in Figure 5-3 The estimated temperature dependent Schottky barrier heights are also included,

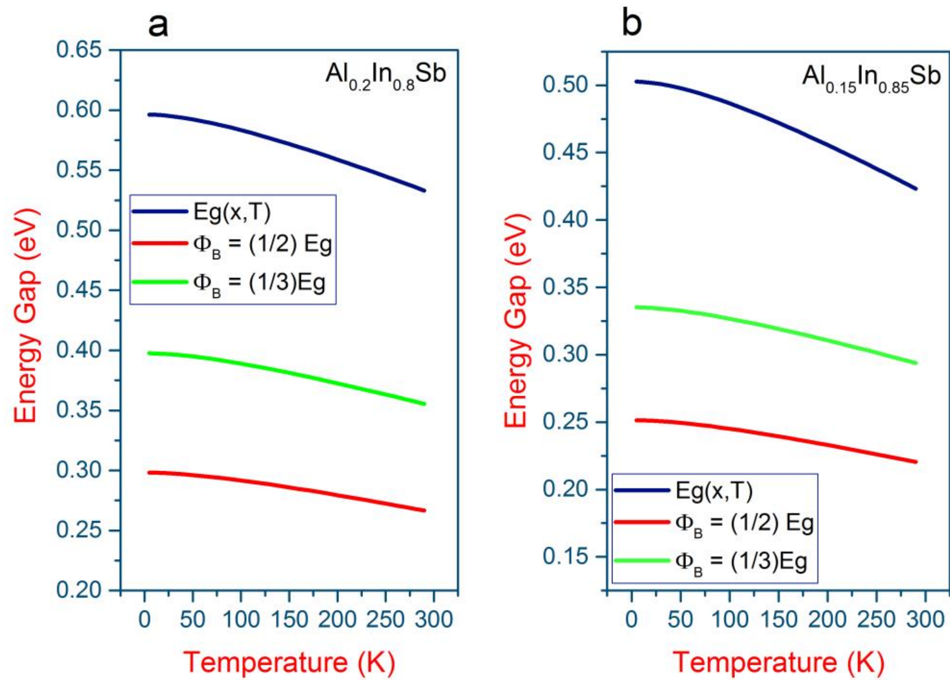

Figure 5-3 The estimated variation of AlInSb energy bandgap with temperature for (a) $Al_{0.2}In_{0.8}Sb$, and (b) $Al_{0.15}In_{0.85}Sb$ paired with the estimated Schottky barrier heights within the same temperature range.

assuming Fermi level pinning at $\frac{1}{2}E_g$ and $\frac{2}{3}E_g$. It is apparent from the figure that the bandgap energies as well as the estimated barrier heights increase as the temperature decreases. This behaviour is completely opposite to the behaviour of the extracted Schottky barrier heights which shows a reduction as the temperature decreases. Therefore, the estimated energy gaps add another anomaly to the I-V-T analysis of the AlInSb/InSb Schottky diodes.

5.5 The Effect of Image Force Lowering

Barrier lowering due to image charge is a possible explanation for the temperature dependence of the barrier height and ideality factor. The image force lowering ($\Delta\Phi_{IF}$) as a function of temperature can be expressed as:

$$\Delta\Phi_{IF} = \left[\left(\frac{q^3 N_d}{8\pi^2\epsilon_s^3}\right)\left(\Phi_B - V_a - E_F - \frac{kT}{q}\right)\right]^{\frac{1}{4}} \tag{5-4}$$

where the term $\varepsilon = kT/q \ \ln(N_c/N_d)$ refers to the energy difference between the Fermi level and the edge of the conduction band, (V_a) refers to the applied voltage, $N_c = 2(2\pi mkT/h^2)^{\frac{3}{2}}$ refers to the effective density of the states of AlInSb, and (N_d) refers to the donor concentration in cm^{-3}. In the case of the AlInSb/InSb Schottky diode of 0.35 eV zero-bias barrier height at 0.1 V forward bias, the barrier lowering due to the image force effect in the measured temperature range is illustrated in Figure 5-4 for various values of N_d. Four values of doping level have been considered since the exact value is unknown. It is apparent from the figure that the variation in barrier lowering with temperatures is too low and it is almost constant for each doping level compared to the reduction in the experimental values of the barrier height for the same temperature range. The maximum barrier reduction for the highest doping level, related to the highest doping, $N_d = 10^{17}\ cm^{-3}$, ranges from 25.4 meV at 30 K to 25.5 meV at 3 K. The low values of barrier lowering and the countless variation with decreasing temperature implies that the reduction of the experimental barrier height with decreasing temperature for the AlInSb/InSb Schottky diodes cannot be explained by image force lowering alone.

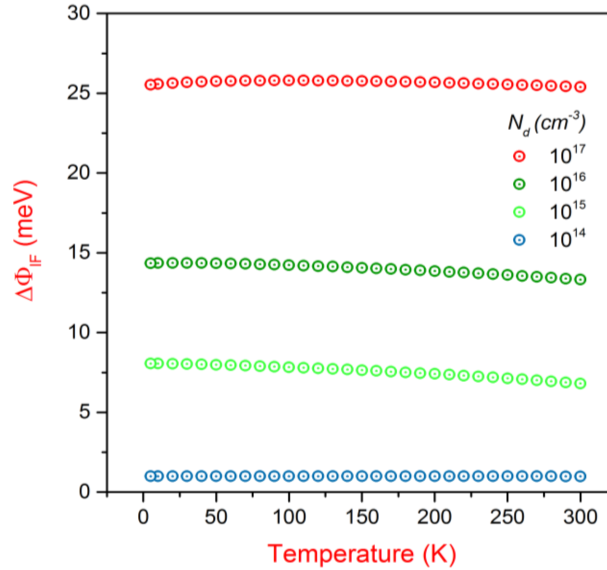

Figure 5-4 Barrier lowering due to image force as a function of temperature at 0.1 V forward bias for AlInSb/InSb Schottky diodes at various values of doping level N_d. The barrier lowering is nearly constant over the entire temperature range.

5.6 The Effect of Tunnelling Current

The contribution of tunnelling (FE or TFE) to the current of a Schottky diode is the most common explanation for the temperature dependence of the barrier height and ideality factor. For a Schottky barrier diode controlled by TFE or FE, the current-voltage relation can be expressed as:

$$I_{tun} = I_{tun.s} \exp\left(\frac{V}{E_o}\right) \tag{5-5}$$

$$E_o = E_{oo} \coth\left(\frac{qE_{oo}}{KT}\right) = \frac{n_{tun}kT}{q} \tag{5-6}$$

where (I_{tun}), and ($I_{tun.s}$) are the tunnelling current and the related saturation current respectively, (E_o) is defined as the tunnelling probability of the carrier through the barrier, and (E_{oo}) is the characteristic energy parameter which can be used to determine the relative importance of the TFE or FE mechanisms which can be expressed as[2]:

$$E_{oo} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{m^*\epsilon_s}} \tag{5-7}$$

where (m^*) is the electron effective mass, (m_o) is the electron rest mass, $(\epsilon_s = \epsilon_r\epsilon_o)$ is the semiconductor permittivity, and (N_D) is the donor concentration in cm^{-3}. It is noticeable from the above equations that the tunnelling current is a strong function of the doping concentration N_D as well as temperature. According to the theory of Pavodani and Stratton[2], the value of E_{oo} with respect to KT will help in determining which current mechanism controls the contact. For $E_{oo} \gg kT$, it is expected that FE dominates the contact current, while for $E_{oo} \ll kT$, TE is dominant. For values in between TFE dominates. Therefore, FE will be more influential at high N_D and low temperatures while TE is dominant at low value of N_D and high temperatures. TFE has a similar effect to barrier height lowering $(\Delta\Phi_B)$ which can be expressed as:

$$\Delta\Phi_{TFE} = \left(\frac{3}{2}\right)^{\frac{2}{3}} (E_{oo})^{\frac{2}{3}} (V_b)^{\frac{1}{3}} \tag{5-8}$$

where (V_b) refers to the band bending voltage. In the case of the AlInSb/InSb Schottky diode, the theoretically calculated value of (E_{oo}) was found to be (3.9) meV assuming a maximum background doping level of 10^{16} cm^{-3}, $m^*=0.014m_o$, and $\epsilon_s = 16.45\epsilon_o$. Such a low value of E_{oo} suggests a current dominated by thermionic emission. However, the experimental data reveals a much higher value of E_{oo}which suggest a substantial contribution of tunnelling current to the AlInSb/InSb Schottky diode. The high value of E_{oo} is normally attributed to the presences of high surface states due to a high density of defects and dislocations which is known to exist in this AlInSb/InSb system[22].

To determine whether the conduction mechanism is FE or TFE, the experimental values of $E_{oo}$are determined first. The experimental values of E_{oo} were determined by comparing the experimental values of η obtained from the I-V-T measurements (closed circles in Figure 5-5), to theoretically generated curves of temperature dependent ideality factors for a Schottky diode operated by FE and TFE current as illustrated in Figure 5-5. The theoretical curves were generated using equations (5-6) and (5-7) at a range of E_{oo}values which were estimated to give the best fit to the experimental data. From Figure 5-5, it is apparent that the experimental data fits to different values of E_{oo}

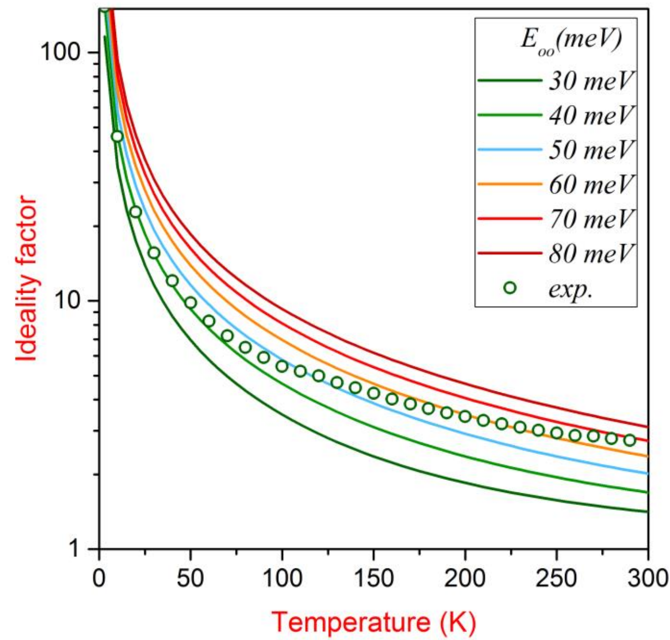

Figure 5-5 The experimental values of the temperature dependent ideality factor in the temperature range (3-290 k) compared to theoretically simulated curves at various characteristic tunnelling energies, ranging from (40-80 meV).

over the entire temperature range. At low temperatures 3-50 K, the experimental ideality factor agrees with the theoretical curve which corresponds to the characteristic energy of 40 meV while at higher temperatures 60-290 K there is a smooth transition from the theoretical curve of $E_{oo} = 40\ meV$ at 60 K into the curve of $E_{oo} = 70\ meV$ at 290 K. Such values of E_{oo}indicate a diode current dominated by tunnelling with a different energy level at each measured temperature. It is also noticeable that the experimental values of E_{oo} are much higher than the theoretical value of 3.8 eV. The high value of E_{oo} at high temperature indicates a presence of traps in the energy gap which can act as intermediate states and enhance the tunnelling probability under certain conditions. The discrepancy between the experimental and theoretical values of E_{oo}along with the observed temperature dependence of E_{oo} excludes TFE or FE as a main current.

The data were further analysed by plotting the barrier lowering $\Delta\Phi_{\mathrm{TFE}}$due to TEF against temperature as shown in Figure 5-6 .The temperature dependent barrier height lowering $\Delta\Phi_{\mathrm{TFE}}$ were calculated using equation (5-8 for the experimental E_{oo}values

paired with the theoretical values of ($\Delta\Phi_{\mathrm{TFE}}$) considering two characteristic energies of 40 eV and 80 eV, which represent the upper and lower limits of the experimental E_{oo}. The figure reveals two different issues. The first problem related to the barrier lowering is the tendency for the barrier to increase or decrease with temperature, and the second problem knowing the amount of barrier lowering at a given temperature compared with the extracted barrier height. In theory, the barrier lowering due to TFE is slightly increased with decreasing temperature as illustrated in Figure 5-6 for the two assumed values of E_{oo}, the case of 40 eV (blue dotted line) and 80 eV (red dotted line). The experimental $\Delta\Phi_{\mathrm{TFE}}$ shows a decrease with lower temperatures. Moreover, the trend of the experimental $\Delta\Phi_{\mathrm{TFE}}$ not only opposes the trend of the theoretical $\Delta\Phi_{\mathrm{TFE}}$ but also disagrees with the variation of the extracted barrier height with temperature, shown in Figure 5-2. It is also noted that the estimated values of $\Delta\Phi_{\mathrm{TFE}}$ at zero bias are too large at high temperatures and too low at low temperatures to explain the extracted barrier height. For instance, the experimental $\Delta\Phi_{\mathrm{TFE}}$ at 290 K for the two characteristic energies of 0.07 eV, and 0.04 eV are 0.155 eV and 0.103 eV respectively. Assuming a flat band barrier of 0.37 eV, the reduced barrier height related to each characteristic energy should be 0.215 eV and -0.267 eV respectively. These values are far lower than

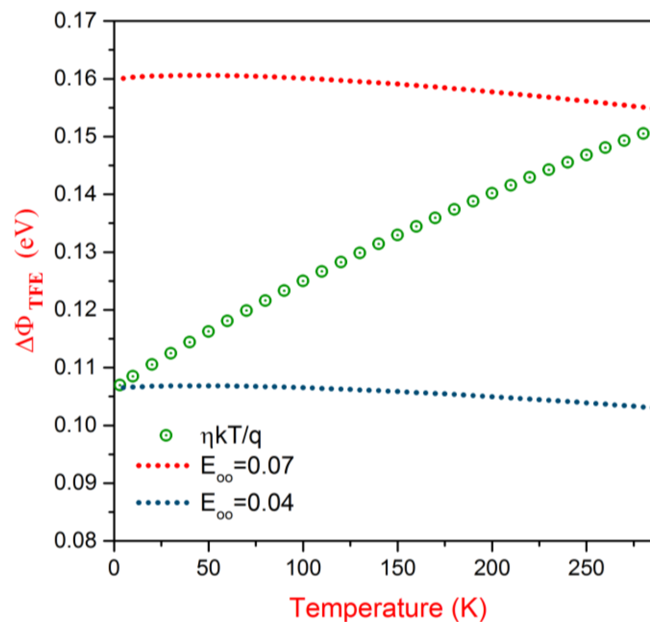

Figure 5-6 The experimental barrier lowering (green doted circles) due to TFE as a function of temperature compared to the theoretical barrier lowering values considering two different characteristics energies, dotted lines.

the Schottky barrier height extracted based on TE theory at the same temperature, which implies an overestimation in the experimental value of $\Delta\Phi_{TFE}$, and vice-versa at low temperature. The discrepancy in barrier lowering predicted by thermal field emission and the experimental values of temperature dependent barrier height imply that the barrier height lowering with decreasing temperature of AlInSb/InSb Schottky diodes cannot be explained by TFE alone. However, such behaviour can be only explained by assuming an enhancement to the AlInSb/InSb Schottky diode current by TAT via deep traps levels. A substantial defect-assisted tunnelling current can be generated with a high level of surface states. The surface and bulk defects may act as recombination centres or as intermediate states for trap-assisted tunnel currents. The TAT mechanism can raise the ideality factor and reduces the Schottky barrier height [23].

The TAT process in the forward bias is schematically illustrated in Figure 5-7.TAT is a strongly temperature dependent multi-step process which can occur in both forward and reverse biases. Under forward bias, the first step comprises tunnelling of electrons from the semiconductor Fermi level to the trap states. The next step is electrons tunnelling

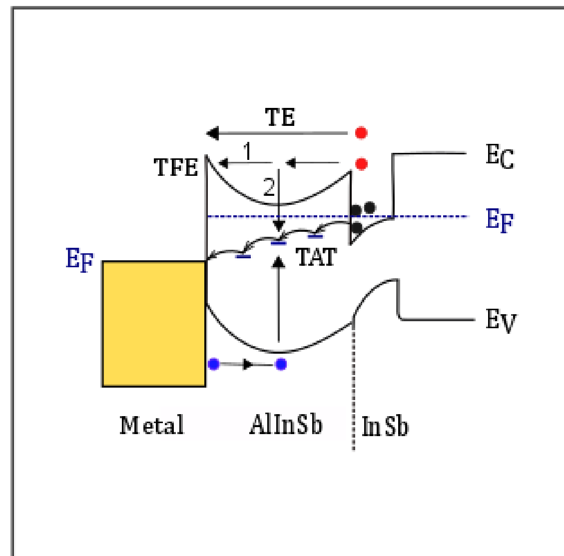

Figure 5-7 The expected mechanism for trap assisted tunnelling current across AlInSb/InSb Schottky barriers in the forward bias. Electrons hope over the trap states forming TAT. Other mechanisms; TE, TFE, and recombination current are also illustrated.

from the trap states to the metal. Under this condition electrons can tunnel through

multiple trap states before reaching the metal as illustrated in Figure 5-7. Under reverse bias, the electrons tunnel from the metal to the trap states and then from the trap states to the semiconductor. Tunnelling via taps depends mainly on the density of the traps as well as their energy distribution, therefore TAT may be a strong temperature dependent process for two reasons. The first reason is attributed to the variation of the ionized trap density with temperature which can lead to a temperature-dependent current. The second reason is attributed to the temperature dependency of the electron population around the Fermi level [24, 25]. The TAT process will be suppressed at a sufficiently low temperature. Another confirmation of the presence of trap states in the AlInSb/InSb Schottky diode is the observation of a photoconductivity effect while measuring the I-V characteristics. The current changes after switching on/off the light while measuring. Irradiating the barrier with light ionizes the traps. This will increase the number of traps involved in the tunnelling process as well as reducing the lifetime of electrons in the traps. Radiation incident on the sample can increase the TAT current.

5.7 Ideality Factor

The ideality factor of AlInSb/InSb Schottky diodes are analysed by plotting the experimental data of the tunnelling probability E_o against kT/q compared to theoretically generated curves related to the most common conduction mechanism as shown in Figure 5-8. If FE dominates, then the tunnelling probability will have a constant value. In this case, E_o is independent of the temperature and its value is nearly equal to the E_{oo}. When TFE dominates, then E_o will show less temperature dependence at low temperatures than at higher temperatures. The value E_o will be a function of temperature if TE dominates the diode current. It is apparent from in Figure 5-8 that the experimental values show abnormal behaviour since $E_o$values lie between the FE and TFE curves. Such a discrepancy is often called as T_o anomaly. Some authors have attributed this T_o anomaly to the presence of surface states, but for AlInSb/InSb diodes the deviation from the ideal case is extremely high which again suggests a substantial contribution of another conduction mechanism to the total Schottky diode current. The results indicate that the mechanism of charge transport in the AlInSb/InSb Schottky diode is neither FE nor TFE.

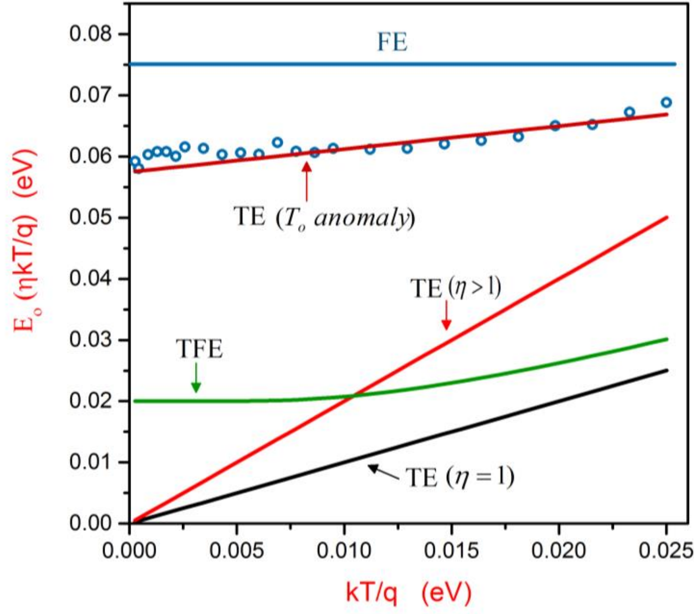

Figure 5-8 Experimental tunnelling energy parameter, blue circles, and its linear fit against kT/q for AlInSb/InSb based Schottky diode, compared to different categories of current transport mechanisms FE, TFE and TE at different conditions η=1, η>1.

5.8 Evaluation of Schottky Barrier Height From I-V-T Analysis

In order to calculate the barrier height for any Schottky diode from its I-V measurement, the Richardson constant must be known. Theoretically, the Richardson constant for any semiconductor is given by:

$$A^{**} = 120\left(\frac{m^*}{m}\right) A\ cm^{-2}\ k^{-2} \tag{5-9}$$

where, $(\frac{m^*}{m})$ is the ratio of the electron effective mass. Consequently, the theoretical value of the Richardson constant for n-type InSb is 1.68 $A\ cm^{-2}\ K^{-2}$ (assuming a value of 0.014 for the electron effective mass ratio). Based on the TE model, the Richardson constant can be evaluated experimentally from the I-V measurements taken at different temperatures. The Schottky diode saturation current should be evaluated at each temperature and then used to construct the Richardson plot which can be obtained by plotting ln $\left(\frac{I_s}{AT^2}\right)$ against T^{-1} and using:

$$\ln\left(\frac{I_s}{AT^2}\right) = \ln A^{**} - \frac{\Phi_B}{\eta kT} \tag{5-10}$$

Experimentally, the saturation current I_o can be obtained from the I-V-T measurements at each temperature individually from a $\ln(J)$ versus V plot. The intercept of this line with the y-axes at zero voltage yields the I_s value ideally. The above equation suggests that this plot should yield a straight line where both the Richardson constant and barrier height can be accurately determined from the intercept and the slop respectively. However, in many practical studies [3-5, 8, 13, 26, 27] this method has led to an underestimation of the Richardson constant as well as the barrier height. In many cases, the Richardson constant was found to be less than its theoretical value by orders of magnitude. Several studies have been done to investigate the origin of this deviation and suggesting different explanations [3, 11, 19, 28-30]. For the AlInSb/InSb Schottky diodes reported here, the Richardson plot obtained from the I-V-T measurement in the temperature range 200-290 K is shown in Figure 5-9. From the figure, it is apparent that the plot deviates considerably from linearity which makes it difficult to determine A^{**} and Φ_B in a temperature range of 200-290 K. However, the Richardson constant

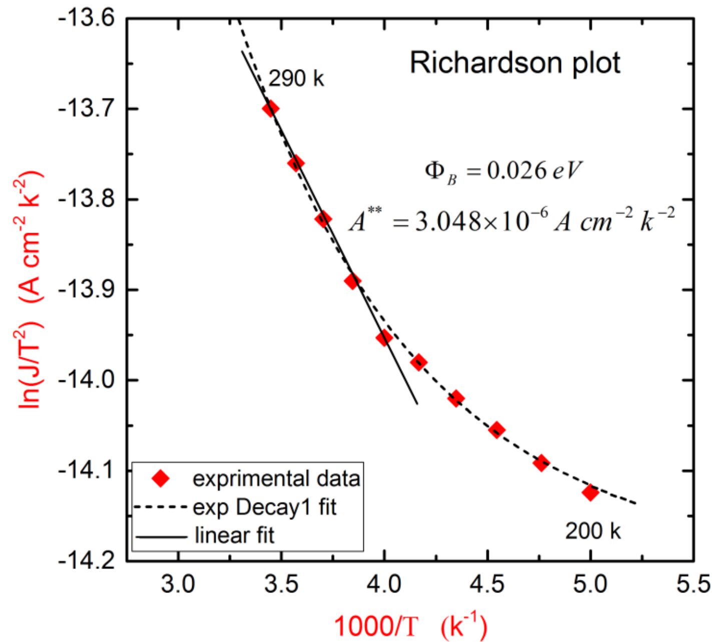

Figure 5-9 Richardson plot of AlInSb/InSb-QW based Schottky diode in temperature range of 200-290 K. non-linear behaviour is dominated and the data started to show upward curvature at 200 K.

and the barrier height obtained by using the upper temperature range 250-290 K were found to be $2.48 \times 10^{-6}\ A\ cm^{-2}K^{-2}$ and $0.027\ eV$ respectively. It is obvious that the Richardson constant is far less than the theoretical value $1.68\ A\ cm^{-2}K^{-2}$ for this material. It is also obvious that the extracted barrier height is considerably smaller when compared to the barrier height $0.36\ eV$ extracted from the I-V measurement at 290 K.

Some studies have attributed this abnormal behaviour in Richardson plots to the nature of the formed barrier. The traditional model of the Schottky diode assumes an abrupt junction with a fixed barrier height. This assumption fails to explain the observed discrepancy in the temperature-dependent diode parameters extracted from I-V characteristics based on the thermionic emission model [6, 31, 32]. Recent models have attributed this discrepancy to the formation of Schottky diodes with barrier inhomogeneities [11, 17, 18, 20]. The barrier inhomogeneities have been described in two different models. In the first model (the Werner and Guttler model) a Gaussian [6, 11, 32] or log-normal [16] distribution function is used to describe the spatial barrier inhomogeneities. The Gaussian distribution function has been used widely to explain most abnormal behaviour, such as the abnormal decrease of the barrier height and the increase of η with decreasing temperature which leads to non-linearity in the Richardson plot, and explains the difference in the barrier heights extracted by C-V and I-V measurements. The second model, known as the Tung model [17, 18, 20], assumes a MS contact with low and high barrier height regions. The low barrier regions below a critical size (comparable to the depletion region, 0.2-1μm) are proposed to get pinched-off by the potential field of the surrounding regions with higher Schottky barriers.

5.9 Temperature Dependence of Φ_B

In an attempt to solve the non-linearity in the Richardson plot for the non-ideal Schottky diode with a temperature-dependent barrier height, Missous and Roderick[28] assumed a linear temperature-dependence of the barrier height as given by

$$\Phi_B(T) = \Phi_B(0) + \alpha T \qquad (5\text{-}11)$$

where α is a temperature-dependent parameter Since the value of Φ_B extracted from the I-V measurements depends on the accuracy of A^{**}, they suggested that the Φ_B as well as the temperature-dependent parameter α can only be obtained from photoelectric or capacitance-voltage-temperature (C-V-T) measurements. According to this method,

the Richardson plot can be corrected by substituting the value of the temperature dependent barrier height given by equation 5-11 in equation (5-10 as given by

$$\ln\left(\frac{I}{AT^2}\right) = \ln(A_c^{**}) - \frac{q\Phi_B(0)}{kT} - \frac{q\alpha}{k} \quad (5\text{-}12)$$

Therefore, the corrected Richardson constant (A_c^{**}) which can be extracted from the intercept of the modified Richardson plot, can be written as

$$\ln(A_c^{**}) = \ln\left(\frac{I}{AT^2}\right)_{intercept} + \frac{q\alpha}{k} \quad (5\text{-}13)$$

Ignoring the temperature dependence of the barrier height results in an uncorrected Richardson constant value (A_{uc}^{**}) which is described as in

$$\ln(A_{uc}^{**}) = \ln\left(\frac{I}{AT^2}\right)_{intercept} \quad (5\text{-}14)$$

Thus, (A_c^{**}) is related to (A_{uc}^{**}) by the relatively simple correction

$$A_c^{**} = A_{uc}^{**} \exp\left(\frac{q\alpha}{k}\right) \quad (5\text{-}15)$$

From the I-V-T measurements of the AlInSb/InSb-QW based Schottky diode, the temperature-dependent barrier height in the temperature range of 200-290 K was used to calculate the value of α as illustrated in Figure 5-10. The temperature coefficient in this temperature range was found to be $1.14 \times 10^{-3}\, eV\, K^{-1}$. Consequently, the corrected Richardson constant A_c^{**} obtained by substituting the value of α in Eq.(5-15) was found to be $1.86\, A\, cm^{-2} K^{-2}$. This value is in good agreement with the theoretical value of $1.68\, A\, cm^{-2}\, K^{-2}$. The extrapolated value of the barrier height at zero temperature $\Phi_B(0)$ from this method was found to be $0.027\, eV$. The extracted value of the Schottky barrier height within this temperature range is in good agreement with its value obtained from the Richardson plot constructed within the same temperature range. However, any increment in the temperature range towards lower temperatures will affect both the zero-temperature Schottky barrier height and temperature coefficient. For instance, for an extended temperature range of 70-290 K, the temperature coefficient was found to be $1.25 \times 10^{-3}\, eV\, K^{-1}$ instead of $1.14 \times 10^{-3}\, eV\, K^{-1}$ and the zero-temperature Schottky barrier height was 0.0014 eV instead of 0.027. Although increasing the temperature range has raised

the corrected Richardson constant to a value of 2.3 $A\ cm^{-2}K^{-2}$, the extrapolated zero-temperature Schottky barrier height is in reasonably good agreement with the effective barrier height at 3 K which was extracted from the I-V measurement using the traditional TE method.

To conclude, the temperature dependent concept of Schottky barrier height has solved the non-linearity problem of the Richardson plot for an AlInSb/InSb based Schottky diode. Although the extracted Richardson constant and the Schottky barrier height with this method are more reasonable, the variance in their values with extending temperature range indicates different temperature coefficients for different temperature ranges. The variance in the temperature coefficient can be attributed to the presence of more than one temperature-dependent current mechanism within the different temperature ranges and that each mechanism activates differently within the full temperature range.

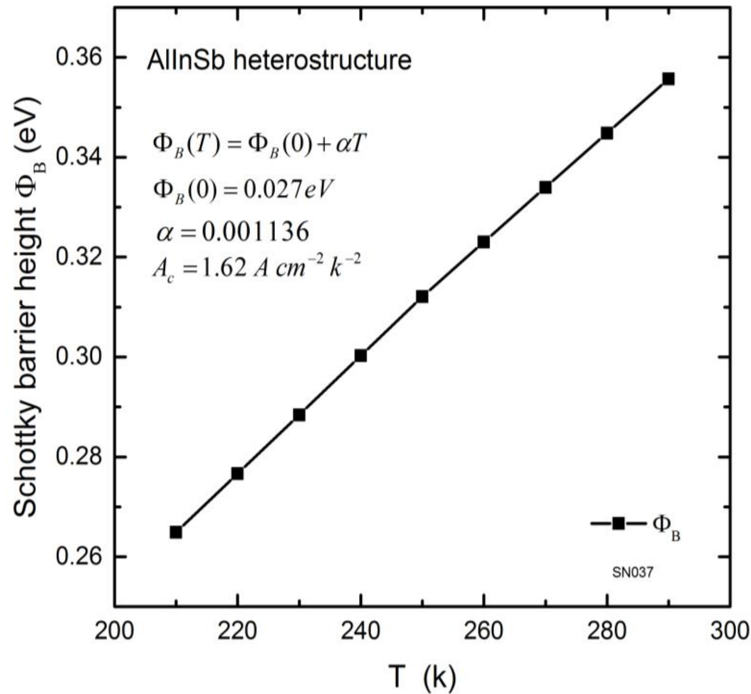

Figure 5-10 The temperature dependence of the barrier height plot obtained from I-V-T measurements with a temperature range of 200-300 K for an AlInSb/InSb-QW Schottky diode.

5.10 Flat-Band Barrier Height

Wagner et al.[33] have presented a new expression which relates the barrier height and the ideality factor of Schottky diodes, extracted from I-V measurements, to a flat-band barrier height (Φ_B^f) (zero-electrical field barrier height) in a linear relationship given by

$$\Phi_B^f = \eta\Phi_B - (\eta - 1)V \quad (5\text{-}16)$$

This shows that this can be used to derive a fundamental expression relating the measured barrier height and the ideality factor as determined from a forward-biased (I-V) measurement of a class of Schottky barrier diodes. The expression is based on an electric-field-invariant fundamental barrier height defined under flat-band conditions. The utility of this relation is the

$$\Phi_\mathrm{B}^f = \eta\Phi_B - (\eta - 1)\, V_\eta \quad (5\text{-}17)$$

where,

$$V_\eta = \frac{q}{kT} \ln\left(\frac{N_c}{N_d}\right) \quad (5\text{-}18)$$

(N_c) and (N_d) are the effective density of states and the doping concentration respectively. To correct the deviating in the traditional Arrhenius plot for the non-ideal Schottky diode, Unewisse et al. suggested a modified Richardson plot by introducing the flat-band saturation current (I_o^f) expression, given by

$$I_o^f = AA^{**}T^2 \exp\left(-\frac{q\Phi_B^f}{\eta kT}\right) \quad (5\text{-}19)$$

The modified Richardson plot can be therefore constructed by plotting $\ln\left(\frac{I_o^f}{AT^2}\right)$ versus $\frac{1}{\eta T}$ instead of $\ln\left(\frac{I_o}{AT^2}\right)$ versus T^{-1}, as given by

$$\ln\left(\frac{I_o^f}{AT^2}\right) = \ln(A^{**}) - \frac{q\Phi_B^f}{\eta kT} \quad (5\text{-}20)$$

5.11 Temperature Dependence of the Ideality Factor 'T_o Effect'

Theoretically, the ideality factor η is a constant which is presumed to be temperature-independent, but for some Schottky diodes the ideality factor has been found to be a temperature-dependent. It is believed that if the Schottky diode current is dominated by

TE and recombination current mechanisms, then η is predicted to be temperature-independent but, when the diode current is dominated by TFE, FE, or by a high level of recombination current in the space charge region, comparable with the TE current, then η is predicted to vary with temperature [34, 35]. Diodes with temperature-dependent η are believed to show what is known as the 'T_o effect'.

In 1965 Padovani and Sumner observed high values of ideality factor (about 30) at low temperatures in n-type GaAs Schottky diodes and they have shown that their I-V characteristics within a temperature range of 77-373 K could be well described by modification of equation 5-1, by introducing an excess temperature factor T_o as follows:

$$I = AA^{**}T^2 \exp\left(-\frac{q\Phi_B}{k(T+T_o)}\right)\left[\exp\left(\frac{qV}{k(T+T_o)}\right) - 1\right] \quad (5\text{-}21)$$

consequently, the temperature-dependence of the ideality factor can be expressed in the form:

$$\eta = 1 + \frac{T_o}{T} \quad (5\text{-}22)$$

This expression indicates that a plot of η versus T gives a straight line with a slope of unity and cuts the ordinate at T_o.

Several studies have been made to explain the temperature-dependence of the ideality factor. Levine [36] and Crowell [37] have shown that the temperature-dependent of η is related to the formation of a particular form of interface state density due to a non-uniform impurity distribution in the semiconductor. Levine [38] links these interface states to the formation of a slightly amorphous semiconductor layer at the metal-semiconductor interfacial region which is anticipated to be responsible for the T_o anomaly. Crowell and Rideout [39] have tried to explain this effect using tunnelling theory, while Rhoderick [35] suggested that all these effects might be the cause of the T_o effect. However, Werner and Guttler [11] postulated that the "T_o effect" is due to a Schottky diode with barrier inhomogeneity.

From experimental analysis of AlInSb/InSb-QW based Schottky diodes, the variance of the ideality factor with temperature, shown in Figure 5-11, indicates a strong temperature dependence, particularly at low temperatures. It is apparent that as temperature decreases the values of the ideality factor increase exponentially. At high temperatures, the ideality factor increases slowly from 290 K down to 150 K, and then

increases rapidly at lower temperatures down to 3 K. In order to verify the applicability of the T_o effect to the fabricated AlInSb/InSb Schottky diodes, the experimental values of ηT were plotted against T as shown in Figure 5-11. From the figure, it is apparent that the experimental data deviates considerably from the ideal case, $\eta = 1$. From the linear fit to the data over the entire temperature range of 3-290 K, the value of T_o was found to be 665 K while the slope was found to be 0.38 instead of unity. By fitting the equation to a narrower temperature range of $200 - 290\ K$, the values of T_o and the slope were found to be 562 K and 0.8 respectively. The high value of T_o indicates a strong deviation from the TE model while the lower value of the slope, less than unity, is attributed to the high value of the ideality as well as to the strong temperature-dependence. For such Schottky diodes with high ideality factor, the experimental data

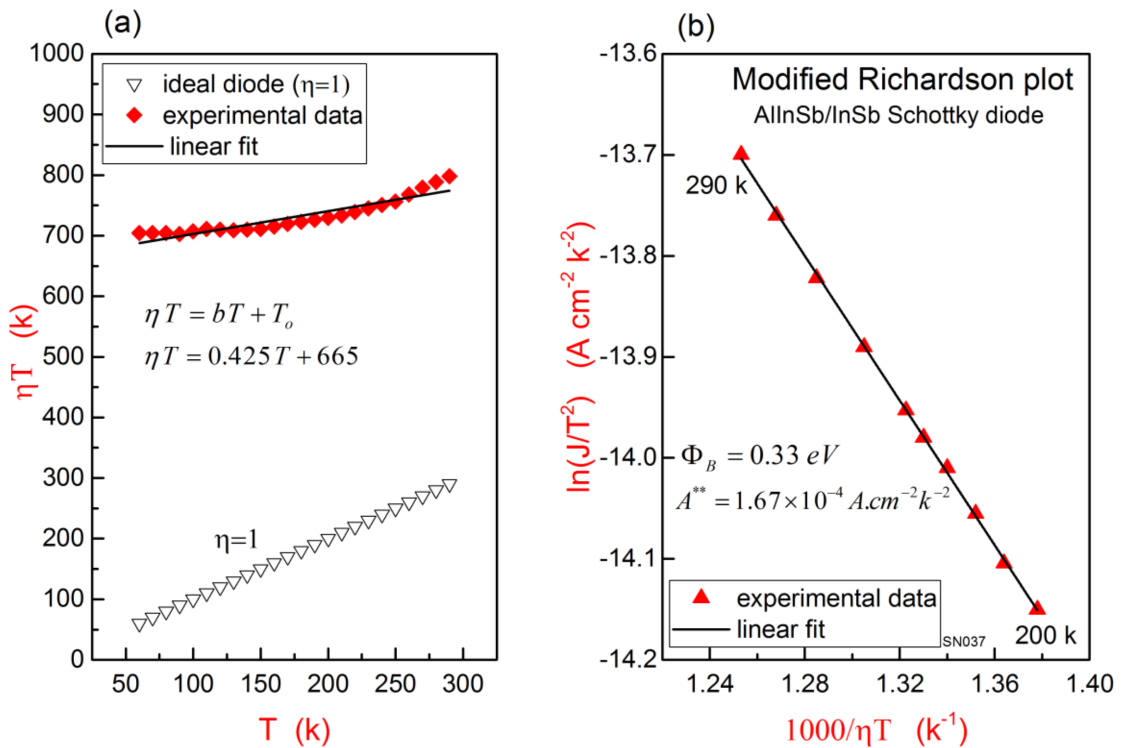

Figure 5-11 Experimental ηT vs T plot of AlInSb/InSb-QW Schottky diode in a temperature range of 60-290 K. (b) A modified Arrhenius plot of AlInSb/InSb-QW Schottky diode according to the T_o effect assumption. The plot is showing more linearity than the traditional Richardson plot shown in Figure 5-9.

can be well fitted by replacing the slope in equation (5-22) with another constant (b) [12, 13, 40]:

$$\eta = b + \frac{T_o}{T} \tag{5-23}$$

According to the "T_o concept", the Richardson plot can be modified based on equations (5-24 and (5-22 as given by:

$$\ln\left(\frac{I_s}{AT^2}\right) = \ln A^{**} - \frac{\Phi_B}{k(T + T_o)} \tag{5-24}$$

Therefore, the Richardson plot can be obtained by plotting $\ln\left(\frac{I_s}{AT^2}\right)$ versus $\left(\frac{1}{\eta T}\right)$ instead of $\ln\left(\frac{I_s}{AT^2}\right)$ versus $\left(\frac{1}{T}\right)$. In the case of a typical AlInSb/InSb Schottky diode studied here, a modified Richardson plot is shown in Figure 5-11(b). The modified Richardson plot according to the T_o concept, unlike the conventional Richardson plot, showed a good linearity, but only over a limited temperature range 200-290 K. The linearity of the modified Richardson plot according to the T_o concept suggested that it is not only the temperature-dependence of the barrier height that can alter the linearity of the Richardson plot but the temperature dependency of the ideality factor is also likely to affect this plot. The Richardson constant and the Schottky barrier height extracted from the modified Richardson plot here were found to be $79.9 \times 10^{-5}\, A\, cm^{-2}\, K^{-2}$ and $0.31\, eV$ respectively. Despite the good linearity of the modified Richardson plot, the value of the Richardson constant is still away from the theoretical value for this material $1.68\, A\, cm^{-2}\, K^{-2}$ and the effective barrier height is lower than the barrier height $0.36\, eV$ extracted from the I-V measurement at $290\, K$.

5.12 Barrier Inhomogeneity

Barrier inhomogeneity of the Metal semiconductor interface is believed to be responsible for most of the non-ideal behaviour observed in Schottky contacts. For an ideal Schottky diode, the MS interface is assumed to be atomically flat but, for real diodes, the interface was proven to be inhomogeneous. Such interfaces lead to spatial fluctuations in the built-in voltage, and the Schottky barrier, as illustrated schematically by the energy band diagram in Figure 5-12 in additional to interface roughness which

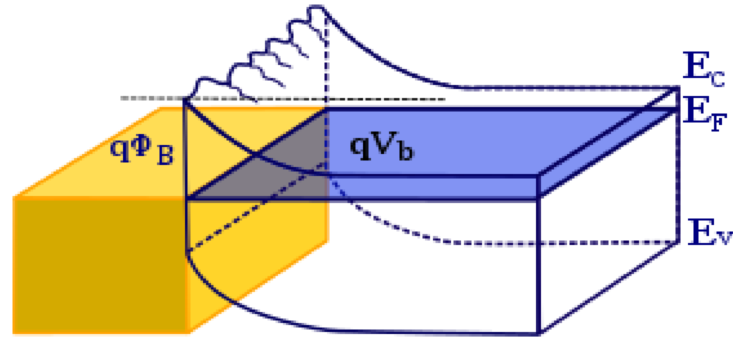

Figure 5-12 A three-dimensional energy band diagram representation of an inhomogeneous MS contact.

is related to atomic steps, defects, and grain boundary, potential fluctuations can also be formed due to the local barrier lowering due to FE at metallic diffusion spikes.

The current transport properties across inhomogeneous barriers were first investigated by Werner and Guttler [11]. They presented a new model known as the potential fluctuation model to describe the electron transport properties at inhomogeneous MS contacts, which are assumed to be greatly influenced by the spatial inhomogeneities of both barrier height and band bending. They used a Gaussian distribution $G(\mathrm{V}_d)$ to describe the band bending around a mean band bending value $(\bar{V}_d^0)$ with a standard deviation of (σ_s^0) as in

$$G(V_d) = \frac{1}{\sigma_s\sqrt{2\pi}}\ exp - \frac{(\bar{V}_d^0\ - \mathrm{V}_d)^2}{2(\sigma_s^0)^2} \tag{5-25}$$

The band bending and Schottky barrier are related by

$$\Phi_B = \mathrm{V}_d + \xi + V \tag{5-26}$$

Similarly, the barrier height is assumed to have a Gaussian distribution $G(\Phi_B)$ around a zero-bias mean Schottky barrier value $(\bar{\Phi}_B^0)$ with a standard deviation of (σ_s^0) as in

$$G(\Phi_B) = \frac{1}{\sigma_s\sqrt{2\pi}}\ exp - \frac{(\bar{\Phi}_B^0 - \Phi_B)^2}{2(\sigma_s^0)^2} \tag{5-27}$$

For a semiconductor at moderate doping level, the variance in the band bending (V_d) and the Schottky barrier height Φ_B is considered to be occurring within a small length distance comparable to the space charge region width, i.e., $< 1\ \mu m$. The potential fluctuation model predicts a temperature dependence of the effective barriers height Φ_B which can be expressed as:

$$\Phi_B = \bar{\Phi}_B^0 - \frac{q(\sigma_s^0)^2}{2kT} \tag{5-28}$$

Hence, the current density according to the traditional TE theory can now be re-written as

$$J = A^{**}T^2 exp - \left(\frac{q\bar{\Phi}_B^0}{kT} - \frac{q^2(\sigma_s^0)^2}{2k^2T^2}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{5-29}$$

According to equation (5-28, a plot of Φ_B against T^{-1} should be a straight line intercepting the ordinate at the zero-bias mean barrier height $\bar{\Phi}_B^0$ and the slope gives the standard distributionσ_s^0. It is believed that the mean barrier height $\bar{\Phi}_B^0$ extracted with this method is the same as the barrier height obtained from capacitance–voltage measurement, which is basically the flat-band barrier. Since both quantities are obtained at zero electric field, they are supposed have the same value [33, 41]. Werner and Guttler found that both standard deviation σ_s, and mean Schottky barrier $\bar{\Phi}_B^0$ vary linearly with T according to the following expressions:

$$\sigma_s^2 = (\sigma_s^0)^2 + \alpha_\sigma T \tag{5-30}$$

$$\bar{\Phi}_B^0 = \bar{\Phi}_B^0(0) + \alpha_{\bar{\Phi}_B^0} T \tag{5-31}$$

The zero-bias standard deviation σ_s^0, even if it has a small value compared to Φ_B, has a significant effect on the Richardson plot especially at low temperatures. The temperature-dependent ideality factor for an inhomogeneous Schottky diode has been found to vary linearly with temperature as in equation (5-32), where δ_1 and δ_2 are the voltage-dependent coefficients measuring the voltage deformation of the SBH distribution. The two coefficients can be evaluated from the intercept and the slope of the straight-line of inverse η versus T^{-1} plot respectively.

$$\eta^{-1} = (1 - \delta_1) + \frac{q\sigma_s^0\delta_2}{2kT} \tag{5-32}$$

It is believed that this model solved the problem of the T_o effect. They demonstrated that the excess temperature coefficient T_o in equation (5-18) represents a rough approximation of equation (5-32). Consequently, the physical value of T_o was found to be

$$T_o \approx -\frac{q\delta_2}{2k} \tag{5-33}$$

The formation of a Schottky diode with barrier inhomogeneities can simply be conformed from the linear relationship of $\overline{\Phi}_B$ versus T^{-1} plot. For a homogeneous contact this plot should be a horizontal line. However, if barrier inhomogeneities of a Gaussian distribution form then the plot of $\overline{\Phi}_B$ versus T^{-1} tilts and can be characterized by a line with a negative slope. The gradient of this line increases with temperature giving a higher value of σ_S^o. The high value of σ_S^o indicates an extremely inhomogeneous barrier. In the same way, the η^{-1} versus T^{-1} plot corresponding to the existing distribution at the contact should give a straight line with a positive value of δ_1 and a negative slope δ_2. The positive sign of δ_1 indicates an increase in the mean barrier height $\overline{\Phi}_B$ with the forward bias, while the negative sign of $\left(\delta_2 = \frac{\partial\sigma_S^o}{\partial V}\right)$ indicates a decrease in the standard deviation σ_S^o with bias. Thus, the forward bias moves the mean barrier height $\overline{\Phi}_B^0$ towards the higher side of the distribution and simultaneously narrows the distribution. A negative value of δ_2 with a positive value of δ_1 indicate that the increase of the ideality factor is caused by the voltage dependence of both $\overline{\Phi}_B^0$ through δ_1 and σ_S^o through δ_2 .

For the AlInSb/InSb-QW Schottky diode, the zero-bias mean barrier height $\overline{\Phi}_B^0$ and the standard distribution σ_s^0 were evaluated from the plot of the experimental values of Φ_B againstT^{-1}, shown in Figure 5-13. It is apparent from the figure that the data fits nicely in a straight line in the temperature range $200 - 290\ K$. Using equation (5-28, the values of the mean barrier height $\overline{\Phi}_B^0$ and the standard deviation σ_s^0 are found to be $0.59\ eV$ and $0.109\ eV$ respectively. It is obvious that the evaluated $\overline{\Phi}_B^0$ is far higher than the zero-bias barrier height Φ_B due to the large value of σ_s^0. According to this model, the temperature-dependence of the ideality factor for the AlInSb/InSb Schottky diode, as indicated by equation 5-32, can be evaluated using a plot of η^{-1} against T^{-1}, as shown in Figure 5-14 (a). It is apparent from the figure that the plot exhibits a good

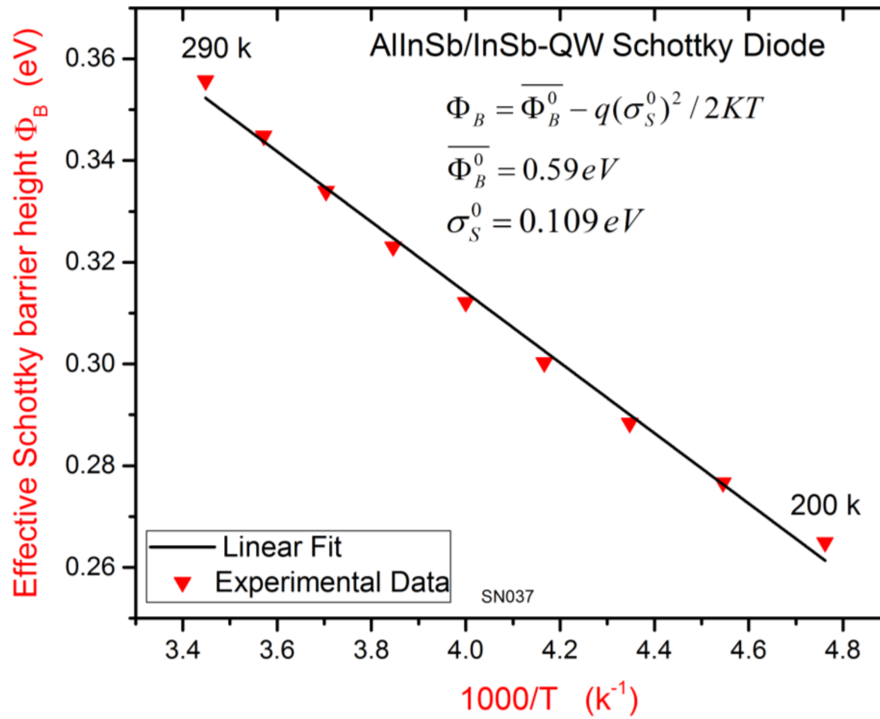

Figure 5-13 (a) The effective barrier heights Φ_B extracted from the I-V measurements against inverse T, in the temperature range $200 - 290\ K$. The values of the mean barrier height and the standard deviation estimated according to eq.(5-28 are found to be $\overline{\Phi}_B^0 = 0.59\ eV$ and $\sigma_S = 0.109\ eV$.

linearity over the temperature range 200-290 K. From the linear fit, the extracted values of the voltage coefficients (δ_2) and (δ_1) are found to be $0.089\,V$ and $0.45\,V$ respectively. Hence, the value of η can be estimated by substituting the extracted values of the voltage-dependent coefficients and the standard deviation in equation 5-32 for any temperature. It's obvious that the values of the δ_2 , σ_S^0, and T have a huge effect on η value, especially at low temperatures. Once δ_1, δ_2 , and σ_S^0 are known, the respective η can be evaluated at any temperature from equations 5-32. The simulated and the experimental values of the ideality factor in the specified temperature range are shown in Figure 5-14 (b). The simulated ideality fits well to the experimental results in the corresponding temperature range. The linear behaviour of the η^{-1} against T^{-1} plot indicates that the ideality factor is consistent with the voltage deformation of the Schottky barriers distribution as suggested by this potential fluctuation model.

The value of T_o for the AlInSb/InSb Schottky diode was found to be 562, considering a value of 0.109 for δ_2.This value agrees well with the value of 557 extracted from the T_o

effect plot over the same temperature range 200-290 K, (Figure 5-11). The good agreement between the two results confirm the validity of the physical meaning of the temperature coefficient T_o predicted by the potential fluctuation model.

The traditional Richardson plot can be modified based on Warner and Guttler's model by substituting the new effective Schottky barrier height, which is expressed by equation)5-28) for its value in equation 5-10 as given by:

$$\ln\left(\frac{I_s}{T^2}\right) - \frac{q^2(\sigma_s^0)^2}{2k^2T^2} = \ln(AA^{**}) - \frac{q\overline{\Phi}_B^0}{kT} \tag{5-34}$$

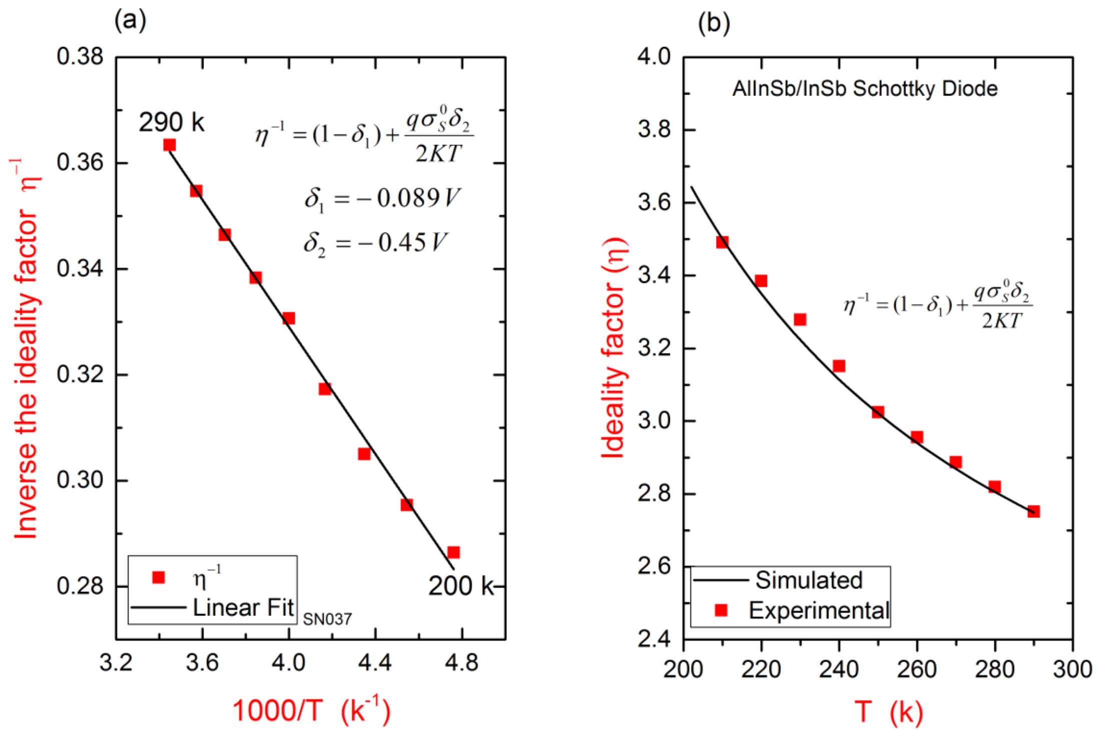

Figure 5-14 (a) A plot of the temperature- dependent ideality factor of an AlInSb/InSb-QW based Schottky diode extracted from the I-V measurements in the temperature range $200 - 290\ K$. *The linear behaviour implies that* η *demonstrates the voltage deformation of the barrier with a Gaussian distribution for the inhomogeneous contact as proposed be Werner and Guttler's model. The values of the voltage-dependent coefficients are* $\delta_1 = -0.089\,V$ *and* $\delta_2 = -0.43\,V$. *(b) the ideality factor against* T. *The squares represent the experimental data extracted from the traditional I-V analysis and the full curve is simulated using eq. 5-32. The Gaussian distribution of barrier height having* $\sigma_s^0 = 0.109\,V$.

Based on the above equation, the modified Richardson plot for the AlInSb/InSb Schottky diodes have been constructed by plotting the term $\ln\left(\frac{I_S}{T^2}\right) - \left(\frac{q^2\sigma_S^2}{2K^2T^2}\right)$ against T^{-1} in the temperature range $200 - 290\ K$ as shown in Figure 5-15. It is apparent from the figure that this method has greatly corrected and linearized the plot in the chosen temperature range. The extracted value of the Richardson constant was more accurate than the value extracted with the modified Richardson plot according to the T_o effect but, the extracted mean Schottky barrier height seems to be overestimated. From the intercept of the figure, the value of A^{**} were found to be $1.82\ A\ cm^{-2}K^{-2}$, which is very close to the theoretical value, $1.68\ A\ cm^{-2}K^{-2}$, of the n-type InSb semiconductor. The value of the zero-bias mean barrier height $(\overline{\Phi}_B^0)$ was found to be $0.59\ eV$. This value agrees very well the $\overline{\Phi}_B^0$value obtained from the earlier $\overline{\Phi}_B^0$ against T^{-1} plot. It is obvious that the extracted value of the mean Schottky barrier height is much higher than

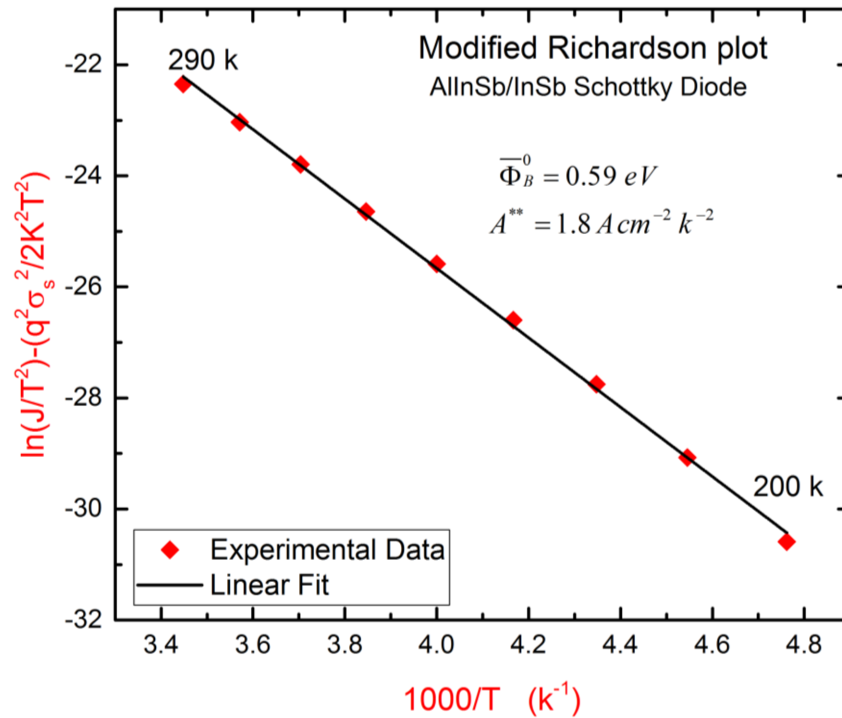

Figure 5-15 Modified Richardson plot of an AlInSb/InSb-QW based Schottky diode according to Werner and Guttler's model in the temperature range $200 - 290\ K$. *The good agreement between the extracted and the theoretical values of Richardson constant* $1.82\ A\ cm^{-2}K^{-2}$*compared to* $1.68\ A\ cm^{-2}K^{-2}$ *indicates the validity of this model over this temperature range.*

the effective Schottky barrier because of the high standard deviation. It is even higher than the energy bandgap of the substrate material which has been estimated, in chapter4, to be $0.52\ eV$. Although the good linearity of the modified Richardson plot and the accurate value of A^{**} might suggest the validity of the potential fluctuation model in explaining the anomalies of the AlInSb/InSb Schottky diode, the overestimation in the mean barrier height with this method must be considered. The model has only taken in consideration the lateral variance in the Schottky barrier heights and ignored the effect of inhomogeneity on the ideality factor, this can lead to a large source of error to the model out puts.

5.13 Summary and Conclusions

In summary, I-V-T measurements of AlInSb/InSb Schottky diodes were investigated and analysed using various methods. The Schottky barrier height and the ideality factor were found to be strongly temperature-dependent functions. Many concepts such as, temperature-dependent energy gap, image force barrier lowering, TFE barrier lowering, and tunnelling effects have been used to explain the temperature dependency of the barrier height Φ_B as well as current and ideality factor η. The analysis suggestes that the current of the AlInSb/InSb Schottky diode is dominated by thermionic field emission and trap assisted tunnelling, but the trap assisted tunnelling current dominates over the TFE current contribution in the higher temperature range.

Due to the temperature dependency of Φ_B and η, the Richardson plot of the AlInSb/InSb Schottky diodes didn't exhibit linearity over the entire temperature range 3-290 K. However, the traditional Richardson plot has been successfully corrected within a limited temperature range 200-290 K using the ''T_0 effect'' and the potential fluctuation model. The potential fluctuation model was found to give an accurate value for the Richardson constant, albeit with a slightly unrealistic corresponding barrier height.

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Chapter 6

Preliminary RF Measurements and Future Work

6.1 Introduction

On-wafer radio frequency (RF) measurements are crucial in the development, modelling, design, and application of high-frequency semiconductor devices. The characterization of RF devices includes a wide range of measurements which impacts on the epitaxial structure design, device geometry optimization (including junction capacitance and series resistance trade-off), and key figures of merit such as responsivity and cut-off frequency, which can be used as performance indicators for devices. In this work, an attempt has been made to investigate the possibility of using the AlInSb/InSb based Schottky diodes reported as a detector for Millimetre waves (mmW). The work includes design, fabrication, and characterization. The fabrication process follows the same process procedures as described in chapter three for Schottky diodes with surface channel structure, but this time using a mask designed to fabricate diodes with a co-planar waveguide (CPW) structure to enable RF measurements. The mask was designed to achieve diodes of various dimensions with three air-bridge lengths of $1, 2, and\ 4\ \mu m$ gate. Details of the mask layout and the device design can be found in appendix A. As a demonstration device characterization has been performed on very limited selected diodes only by means of DC and on-wafer Radio Frequency measurements. The on-wafer RF measurements of the realized AlInSb/InSb Schottky diode will be used to investigate the rectification performance as a function of frequency, RF power, and dc bias. An equivalent circuit model for the diode is also presented to enable analysis of the device performance.

Before device characterization, the chapter starts with an insight into the principles of millimetre waves (mmW) and non-linear detectors, followed by typical mmW figures of merit. Device characterization is presented using a diode equivalent circuit model followed by DC and RF measurements.

Throughout this chapter, suggestions are made as to where this work should proceed and expand, as time and facility availability did not permit in the time period of this current work and forms a pragmatic description of realistic future work.

6.2 Millimetre Waves

Millimetre-waves, denoted by the International Telecommunications Union as extremely high-frequency (EHF), occupy the region between the microwave and the far infrared bands of the electromagnetic spectrum (Figure 6-1). Millimetre-waves occupy the frequencies between 30 GHz and 300 GHz which corresponds to wavelengths in the range of 1-10 mm. Due to unique properties, millimetre-wave detection has received considerable attention over the past few years in security, military, and commercial applications [1-3]. The ability to penetrate clothing and organic materials makes millimetre-waves great candidates for security screening applications. This is increasingly used at airport for detecting weapons and dangerous objects. Other advantages of mmW is their low attenuation under poor weather conditions which

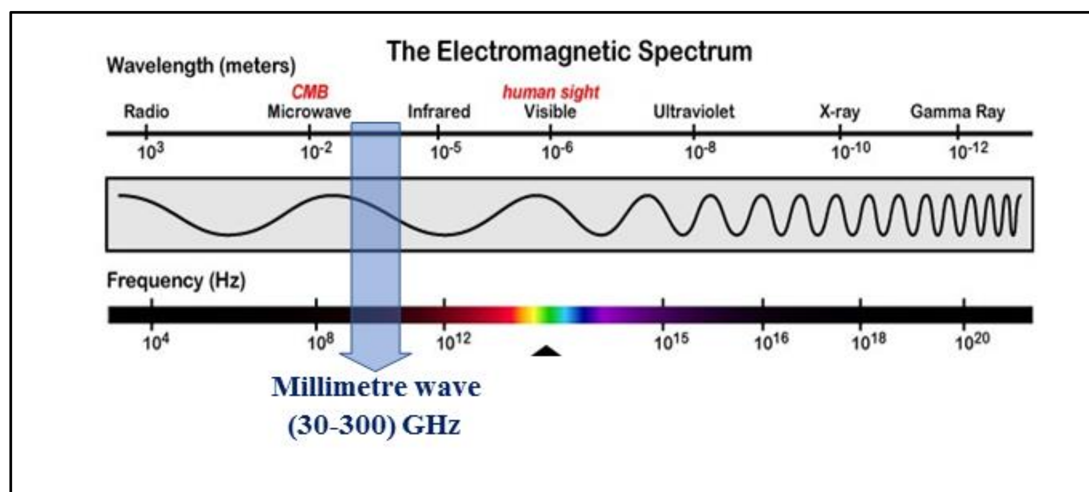

Figure 6-1 A diagram of the electromagnetic spectrum illustrating the location of the millimetre wave.

makes them excel at imaging for military applications including reconnaissance, surveillance, and target acquisition. Imaging systems utilising infrared (IR) radiation have shorter wavelengths leading to a higher image resolution, but can only work in clear weather conditions. Atmospheric conditions degrade the (IR) signal and thus prevent imaging. Therefore, mmW detectors have the advantage over IR detectors for imaging under poor weather conditions such as precipitation, fog, smoke, and dust (significant for example when landing a helicopter in challenging dessert scenarios). The usage under low-visibility in addition to day and night conditions make mmW an attractive candidate for imaging. Figure 6-2 shows the attenuation of radiation in the mmW region, compared to infrared and visible regions, in typical realistic atmospheric scenarios. Schottky diodes can act as direct detectors that operate within the millimetre and submillimetre wavelengths. Due to their high electron mobility and low noise levels at room temperature, planar GaAs Schottky diodes can be considered mature devices operating at millimetre and sub-millimetre wavelength[4]. However, the need for local oscillator power introduces complexity to the system and introduces a noise source which in turn restricts their usage at higher frequencies. Replacing a GaAs Schottky diode with a reduced barrier height Schottky diodes such as an AlInSb/InSb Schottky diode would give rise to a considerable improvement in terms of system complexity, noise level, and power consumption.

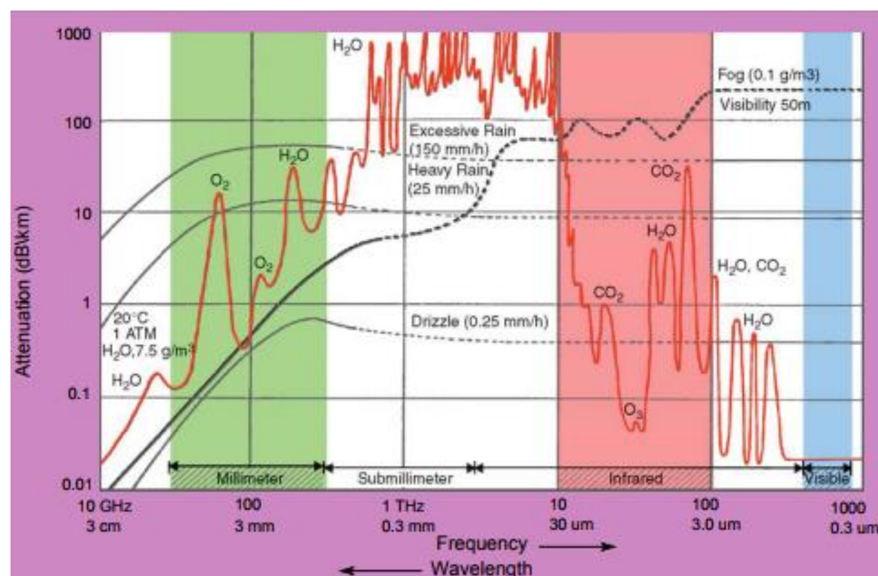

Figure 6-2 Attenuation of the electromagnetic waves by atmospheric conditions: gases; fog; and rain[2].

6.3 Non-Linear Detector

Due to their non-linear (I-V) characteristics, Schottky diodes can be used as detectors for high power measurements when the input signals are not too high for the diode to operate in the square law region ($V_{out} \propto V_{in}^2$). The rectification efficiency of high frequency detector diodes varies widely across the range of the applied voltage as illustrated in Figure 6-3. At a very low level of input power, before the knee of the I-V characteristic, the diode exhibits a nonlinear response, where the input ($V_{out} \propto V_{in}^2$). However, at higher RF power, the output voltage becomes proportional to the input voltage, ($V_{out} \propto V_{in}$). A smooth transition from the square-law response to the linear response normally occurs between −10 and −20 dBm. A high frequency power detector uses the nonlinear response of a device to convert the input DC power (P_{in}) to a (DC) voltage (V_{out}).The transfer function for small input power which defines the detector responsivity ($\Re$) is given by

$$\Re = \frac{V_{out}}{P_{in}} \tag{6-1}$$

The voltage responsivity is usually measured in units of (mV/mW) or (A^{-1}). Diode responsivity is usually measured at -20 to -30 dBm input power levels to ensure that the

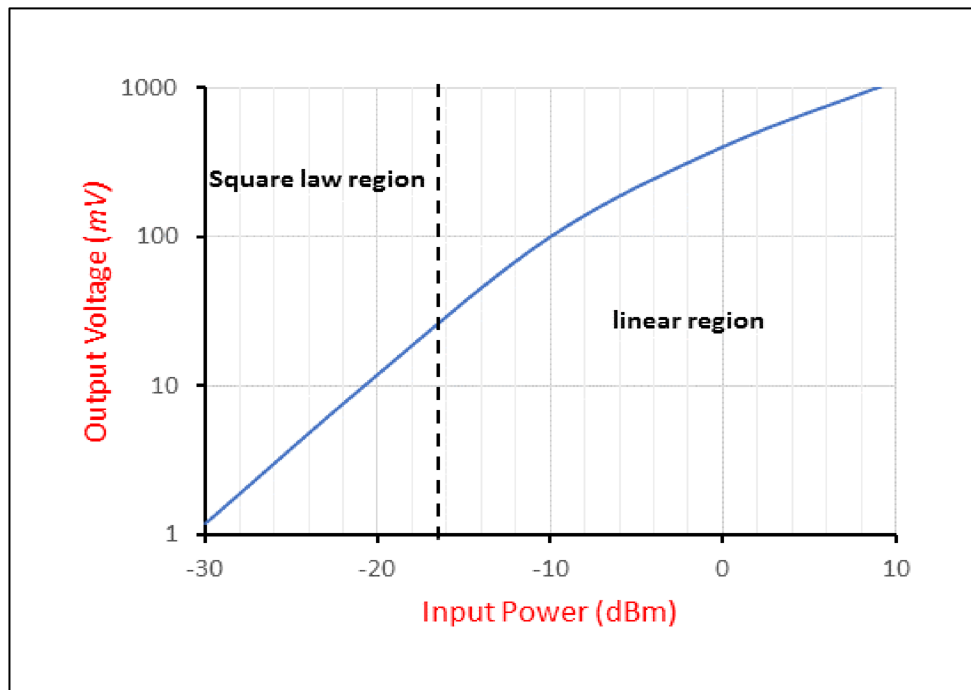

Figure 6-3 The output voltage as a function of the input power for an idealised Schottky diode rectifier.

detector is operating in the square law region. For higher input power, the detector response turns smoothly from a quadratic to a linear response.

6.4 Figures of Merit for mmW Detectors

Detector performance can be evaluated and compared through three main figures of merit, namely; sensitivity, noise level, and cut-off frequency. All these figures of merit are related to fundamental device parameters; for instance, the detector sensitivity depends on the curvature coefficient and the junction resistance, whereas the cut-off frequency is mostly affected by the value of the junction capacitance. Adjusting the device's key structural parameters can lead to a significant improvement for an individual figure of merit. For example, the device lateral scaling can raise the cut-off frequency to very high values. However, extreme lateral scaling for the device active area increases the junction resistance which in turn degrades the device noise performance. Hence, improving one feature of the detector may lead to undesirable performance in other aspects of the device, and thus reduces the device performance for a given system-level. Therefore, for any practical application, all these three main figures of merit must be considered and optimized according to the application needs. For mmW detectors, the sensitivity and noise performances are of great importance. The detector sensitivity and noise merits are linked together through a new figure of merit known as the noise equivalent power NEP which represents the smallest detectable RF power with a signal-to-noise ratio of unity. NEP is very often the most relevant figure of merit used to describe the device performance at high frequency.

In this chapter, the possibility of utilising AlInSb/InSb Schottky diodes as mmW detectors will be discussed and analysed in terms of the diode curvature coefficient. The diode curvature coefficient will be extracted from the DC (I-V) measurements. However, suggested future work should encompass evaluation of the device performance in term of NEP. Efforts can also be done on improving the NEP through manipulating the heterostructure design, device structure, and the device vertical and lateral scaling.

6.5 Diode Equivalent Circuit

Achieving the best design for high frequency detector performance requires knowledge of several parameters that describe all the diode components. Equivalent circuit analysis

is an effective way to represent the detectors components and to analyse their electrical behaviour. A typical equivalent circuit model of a diodes detector at high frequency is illustrated in Figure 4-6. The model includes the Schottky diode circuit, including parasitic components. It is apparent from the figure that the device components are divided into two parts: intrinsic components and extrinsic components. The intrinsic components, diode series resistance (R_s), junction capacitance (C_j), and junction resistance (R_j) (surrounded by the red box) represent the familiar device hybrid model which is used for low-frequency device analysis. However, the device extrinsic components are represented by a parasitic capacitance (C_p), and parasitic inductance (L_p) at the pads, connections, and substrate network. Having an equivalent circuit model can help with a precise assessment of the device parasitics and their effects on the device performance hence, it is vital for the optimization of the physical device.

In general, the diodes cut-off frequency $\left(f_c = (2\pi R_s C_j)^{-1}\right)$ which describes the diode maximum limit of frequency response, is directly affected by the parasitic series resistance (R_s), also known as the differential resistance (R_{diff}), and the diode junction capacitance (C_j). Therefore, reducing the junction capacitance through scaling

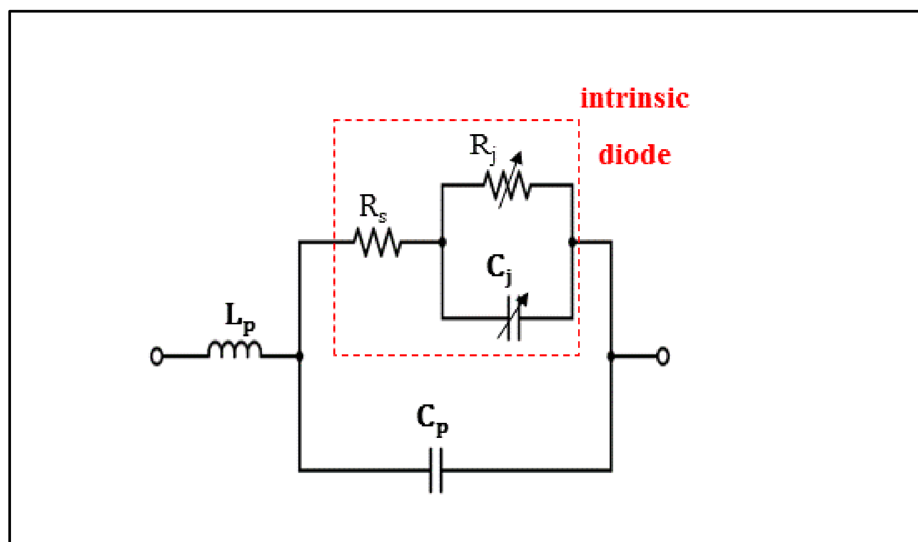

Figure 6-4 A typical diode equivalent circuit which includes the diode intrinsic and extrinsic components. The intrinsic diode components include the diode series resistance (R_s), the junction resistance (R_j), and the junction capacitance (C_j). The parasitic components include the inductance (L_p), and the capacitance (C_p).

down the anode active area is the main challenge for researchers who want to improve the diodes cut-off frequency. The diode cut-off frequency for the typical detector model is often stated as[5]:

$$f_c = \frac{1}{2\pi R_s(C_j + C_p)} \quad (6\text{-}2)$$

although this expression ignores the temperature dependency of the parasitic capacitance, bias dependence of the junction capacitance, and the high-frequency elements of the series impedance. It does however provide an easy method to calculate the virtual diode cut-off frequency that yields the best performance for high frequency circuits. Scaling down the anode area reduces junction capacitance but enhances the diode's series resistance. Therefore, choosing an anode size involves complicated trade-offs between the device capacitance and resistance. However, some researchers have shown that reducing the anode diameter can enhance the diode performance at high frequency[6].

An AlInSb/InSb planar Schottky diode with a co-planar waveguide (CPW) structure is shown in Figure 6-5. A typical model for the diode parasitic components along with the proposed equivalent circuit of the diode are shown in Figure 6-6. The junction capacitance and resistance are at the heart of the Schottky diode and their voltage their voltage dependency controls the generation of its nonlinear characteristic.

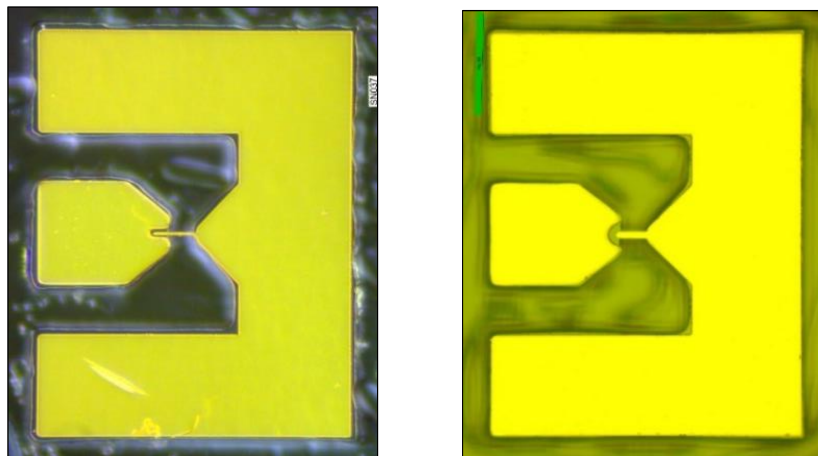

Figure 6-5 Typical images of AlInSb/InSb planar Schottky diodes with two different configurations of finger design. The device has a co-planar waveguide (CPW) structure which is normally used for S-parameter measurements.

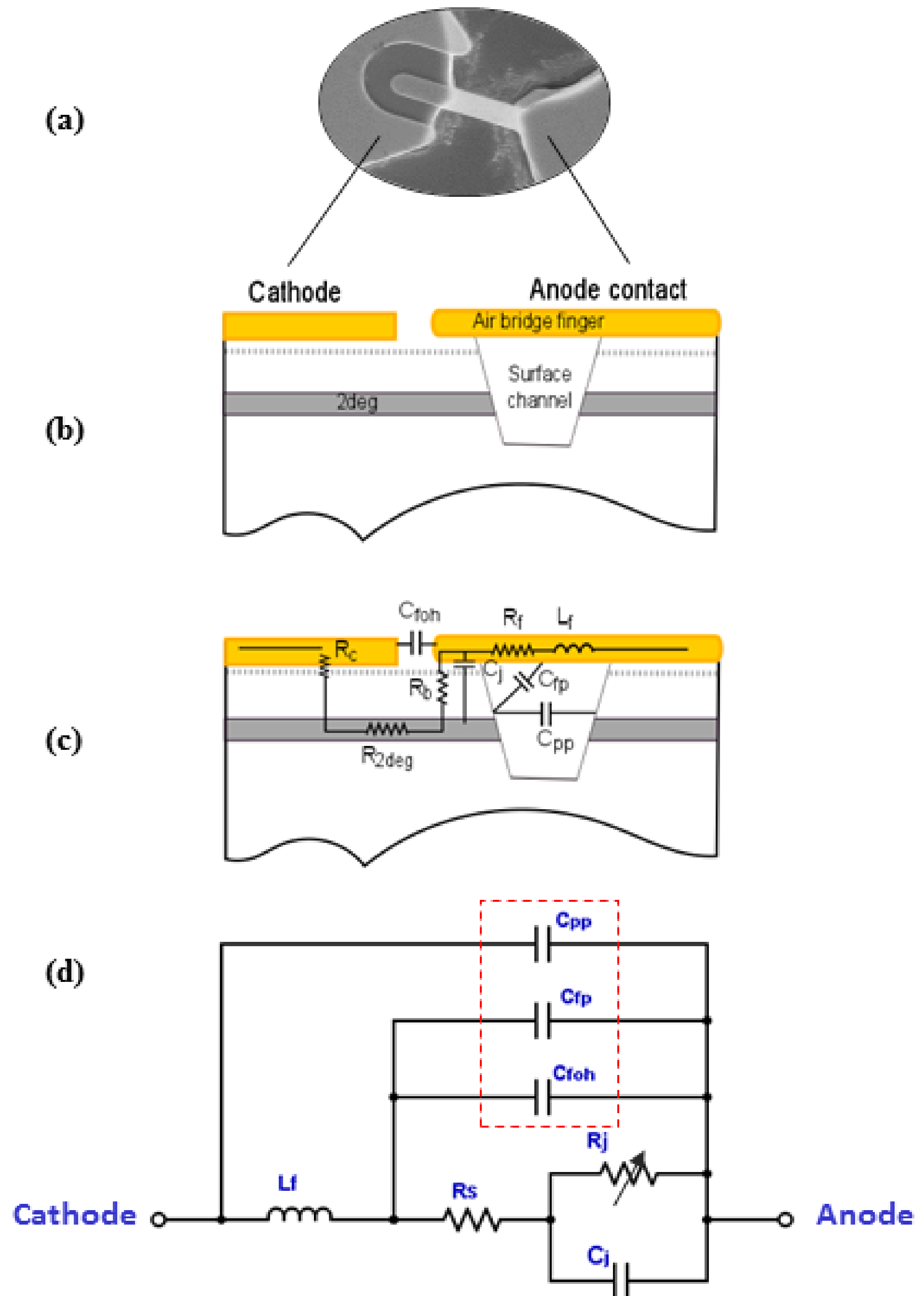

Figure 6-6 (a) Scanning electron microscope image of the planar Schottky diode active area. (b) A schematic diagram of the fabricated AlInSb/InSb Schottky diode. (c) A schematic diagram of the realized Schottky diode indicating the diode equivalent circuit elements. (d) A proposed Schottky diode equivalent circuit. The total parasitic capacitance comprises the pad-to-pad capacitance (C_{pp}), *finger-to-mesa capacitance* (C_{fp}), *and finger-to-ohmic contact capacitance* (C_{foh}). *The total resistance comprises five resistive components, anode finger* (R_p), *airbridge finger* (R_f), *ohmic contact* (R_c), *and the 2deg channel resistance* (R_{2deg}).

The total series resistance for the presented planar Schottky diode based on epitaxial material comprises four main components; the air-bridge finger resistance (R_f), the top barrier layer resistance (R_b), the spreading resistance in the 2deg layer (R_{2deg}), and the ohmic contact resistance (R_c). Therefore, the total series resistance can be written as[7]

$$R_s = R_f + R_b + R_{2deg} + R_c \tag{6-3}$$

However, the device parasitics, which can strongly degrade the device performance at high frequency, can be described by capacitive and inductive parasitic components which depend on the device material and geometry.

Generally, modelling and optimisation work only considers the parasitics in proximity to the air-channel and anode contact. The total parasitic capacitance includes three components; the pad-to-pad capacitance (C_{pp}) which represents the capacitance between the two mesa sides and depends on the distance between pads, mesa height, and substrate thickness and permittivity; the finger-to-pad capacitance (C_{fp}), which describes the capacitance between the anode finger to the mesa; and the finger-to-cap capacitor (C_{fc}) refers to the capacitance between the anode finger and the substrate surface. Hence, the total diode capacitance (C_{total}) can be obtained from the summation of the zero-bias junction and parasitic capacitances, as given by:

$$C_{total} = C_{jo} + C_{pp} + C_{fp} + C_{fc} \tag{6-4}$$

6.6 Characterization and Modelling mmW Detectors

Characterization of high frequency diode detectors requires knowing their intrinsic and extrinsic parameters which are essential in describing the diode performance. The intrinsic and extrinsic parameters can be extracted from DC and RF measurements. The DC measurement is the first step towards diode modelling which is normally used to extract the fundamental diode parameters such as the diode series resistance (R_s), ideality factor (η), and saturation current (I_s). Whereas, RF measurements are the second step towards diode modelling. The RF measurement provides information about the zero-bias junction capacitance (C_{j0}), and the diode parasitic components; series inductance (L_s), and parallel capacitance (C_p). The parameter extraction method depends on the device operation frequency. For the millimetre wave range, on wafer

direct S-parameters measurements is the most common way to measure the diodes zero-bias junction capacitance [5]. However, the parasitic inductance and capacitances can be achieved through using short and open de-imbedding techniques.

6.7 DC Measurements

The room temperature DC current-voltage characteristic of an AlInSb/InSb Schottky diode with area of $2\mu m \times 10\ \mu m$ is shown in Figure 6-7. The figure displays the measured data (triangles) and the simulated curve (red line). The simulated curve has been generated based on the proposed equivalent circuit of the diode. The good agreement between the measured and the simulated data suggests confidence in the validity of the proposed model. The fundamental Schottky diode parameters can be calculated from the I-V data as has been discussed thoroughly in chapter 4. However, the curvature coefficient (γ) and the differential resistance (R_{diff}) can also be calculated from the DC measurement.

6.7.1 Curvature Coefficient

For high-speed detectors, strong nonlinear I-V characteristics is crucial and so the curvature coefficient is one of the most important figures of merit for high-speed

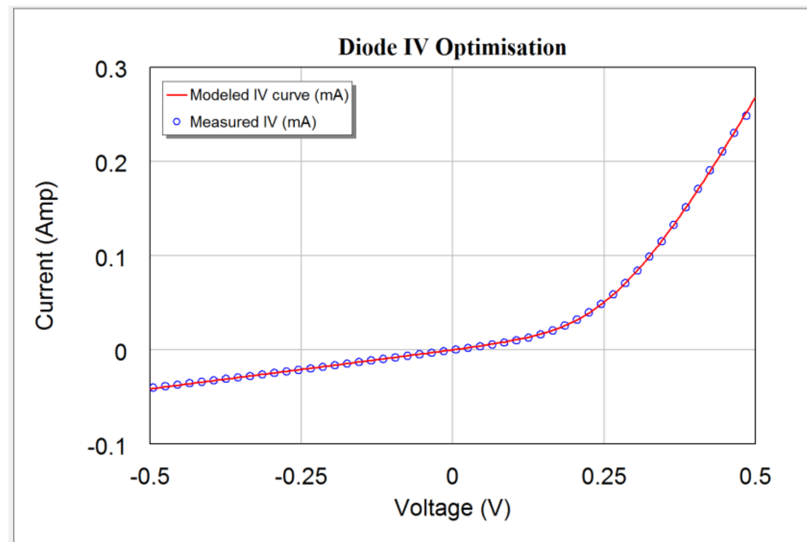

Figure 6-7 Measured I-V characteristic of a typical AlInSb/InSb Schottky diode paired with a theoretical curve which has been simulated based on an equivalent diode circuit mode.

detectors. This is mainly used to measure the devices nonlinearity and is thought to assess the detector responsivity. The curvature coefficient γ can be found from the ratio of the second derivative of the current-voltage characteristic to its first derivative as given by the relation[8, 9]:

$$\gamma = \frac{\frac{d^2I}{dV^2}}{\frac{dI}{dV}} = R_{diff}\frac{d^2I}{dV^2} \quad (6\text{-}5)$$

$$R_{diff} = \frac{dV}{dI} \quad (6\text{-}6)$$

It is apparent that the slop, (dI/dV), has its highest value at the diode drop off voltage. Therefore, Schottky barrier diodes can be better detectors if biased to a voltage higher than Φ_B. For Schottky barrier diodes, the curvature coefficient is a temperature-dependent function which can be calculated from q/nkT. Accordingly, the maximum value of the curvature coefficient for Schottky diodes at 300 K is approximately 40 V^{-1}[9].

Using the simulated I-V curve which is shown in Figure 6-8, the device curvature coefficient and differential resistance of the realized AlInSb/InSb Schottky diode are

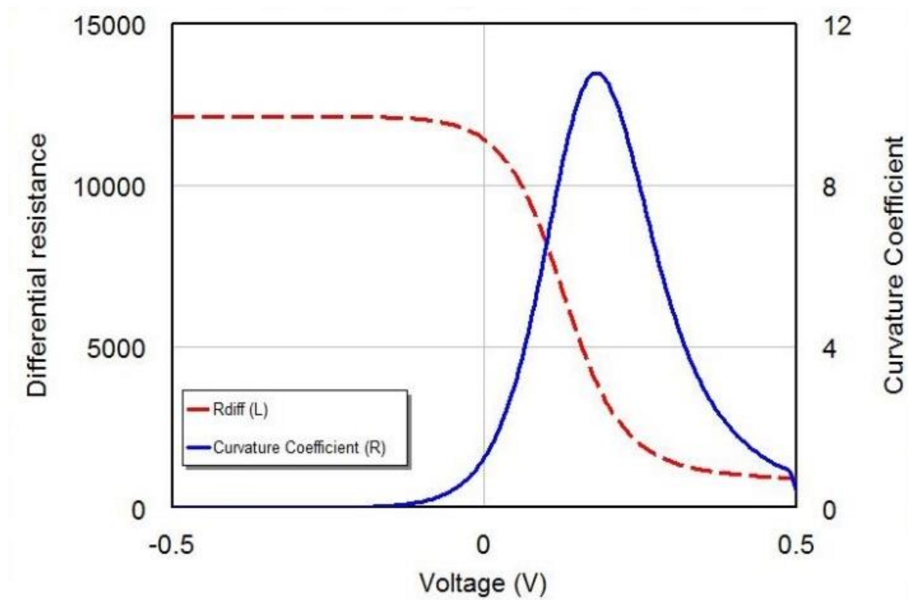

Figure 6-8 Curvature coefficient and differential resistance of the realized AlInSb/InSb based Schottky diode detector. The diode has a curvature coefficient of 11 V^{-1} at 200 mV and differential resistance of 11 kΩ at zero-bias.

calculated and presented in Figure 6-8. It is apparent from the figure that the device features a maximum curvature coefficient (γ) of 11 V^{-1} at a bias of 200 mV, and has a differential resistance of 2.5 $k\Omega$ at 200 mV and 11 $k\Omega$ at zero-bias. Although the diode shows a good curvature coefficient, additional work would need to be done to enhance the device nonlinearity through focusing on reducing the diode series resistance. Since the contact resistance (R_c) and the spreading resistance $\left(R_{2deg}\right)$, which are presented in equation (6-3), are anticipated to have small values, efforts should focus on reducing the finger resistance $\left(R_f\right)$ and the top barrier resistance (R_b). The diode series resistance can be reduced by using an array of Schottky diodes that are shunt connected. This technique has been shown to be an effective way to realize Schottky diodes operating at high frequencies. Applying this technique on silicon based Schottky diodes has raised the cut-off frequency to its upper limits[10].

6.8 RF Measurements

Radio Frequency (RF) measurements are used for high speed devices working at GHz to THz frequencies. For Schottky diodes, the RF measurements can be divided into two different types, small-signal measurements and large-signal measurements. The Small-signal measurements are normally used to describe the linear behaviour of the diode where the output and the input frequencies are the same, while the large-signal measurement is used for describing the non-linear diode behaviour where the output frequency might be disrupted as illustrated in Figure 6-9.The linear behaviour of a device can be fully described with the S-parameters measurements. However, describing the nonlinear device performance requires information about the harmonics created by the device under test (DUT) of both the current and voltage or scattered voltage signals at all ports. The degree of difficulty grows significantly as the number of the generated harmonics increases.

6.8.1 Low Signal Measurements

The S-parameter measurement is one of the most important set of figures of merit for RF low-signal measurement and is mainly used to quantify the gain, loss, and reflection of a device through measuring the amplitude and phase of the incident, reflected and

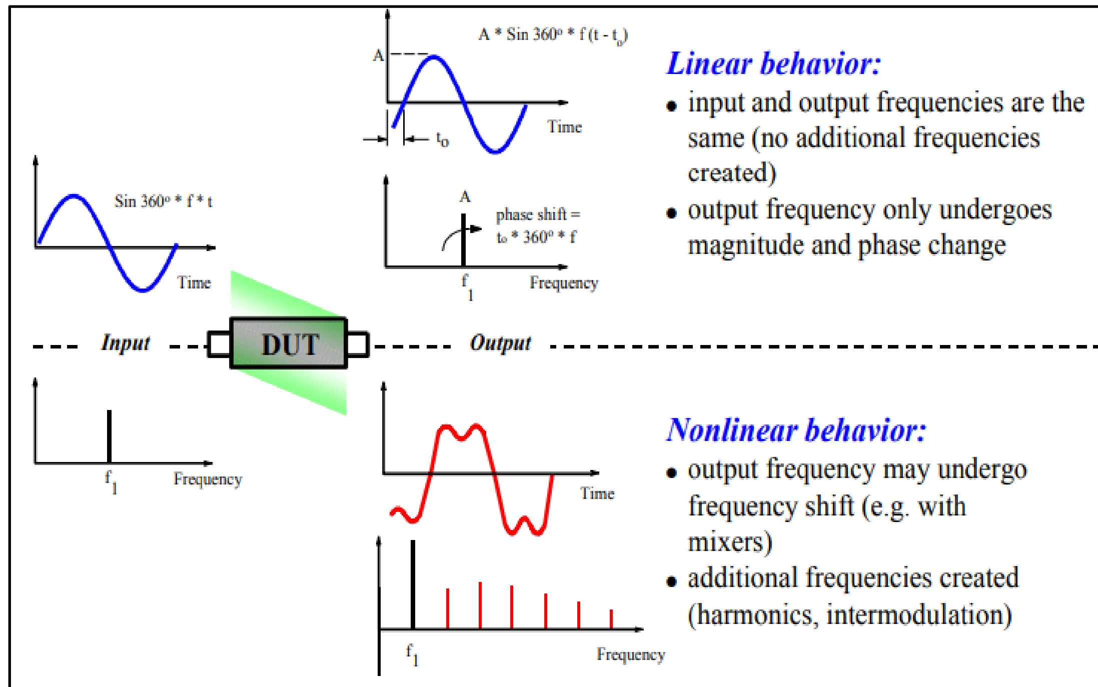

Figure 6-9 Linear vs nonlinear behaviour of a device. It is apparent that the nonlinear behaviour adds more complexity to the measurements due to the generated harmonics and intermodulation[11].

transmitted signals. The ratios between the incident signal at one port to the transmitted or reflected signal at a given port are complex numbers denoted as S-parameters and can be express as

$$S_{ij} = \frac{b_i}{a_j} \tag{6-7}$$

The subscript (*j*) stands for the input port and (*i*) stands for the output port. Therefore, the reflected coefficient (S11) refers to the ratio of the reflected signal (b1) to the incident signal (a1) on a specific port. (S21) refers to the ratio of the transmitted signal (b2) at port-2 to the incident signal (a1) at port-1; for more details see [12-14]. The s-parameters are commonly measured with a vector network analyser (VNA) and then displayed via a Smith chart (Figure 6-10), to analyse the data. The Smith chart is commonly used to convert the reflection parameters into impedances and vice-versa. The lines on the chart represent the constant real and imaginary parts of the complex impedance. The horizontal axis represents the real parts of the complex impedance that gives the resistance values which map into circles while the imaginary parts indicate the values of constant reactance which map into arcs [13, 16].

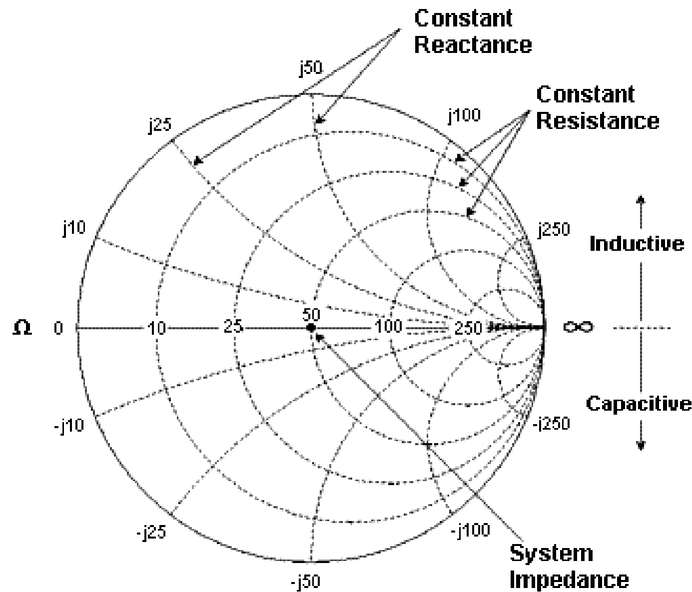

Figure 6-10 A simplified Smith chart. Every point on the Chart represents a complex impedance (Z) made up of a real resistance and an imaginary reactance. The horizontal axis represents the real impedance (resistance) which has a value of infinite (Open) and zero (Short) at the terminals and the centre represents the system impedance. The peripheral represents the imaginary component (reactive). The upper half stands for the inductance while the lower half stands for the capacitive[15].

The S-parameter measurements of a tested AlInSb/InSb Schottky diode was performed at 4 GHz with a vector network analyser (VNA) connected to a Cascade probe station provided with a ground-signal-ground (GSG) RF probe. The diode has a coplanar waveguide structure to enable GSG measurement mode with an anode size of 1 μm. Two values of reflection coefficient S11 were measured at two different biases conditions and then converted into a Smith chart as shown in Figure 6-11. The measured S11 was found to be 48.7-j2 at zero bias (red circle) while the S11 was 49-j2.17 at a DC bias of 50 mV, (green circle). The blue curve represents simulated data based on the proposed equivalent diode circuit. From the figure, it is apparent that the device is dissipating power due to the series resistance and capacitance effects. Applying a forward bias of 50 mV increases the diode sensitivity and thus slightly improves the diode performance. For the presented diode, it is expected that the highest value of the sensitivity can be achieved at a bias equal to the diode turn on voltage, which is

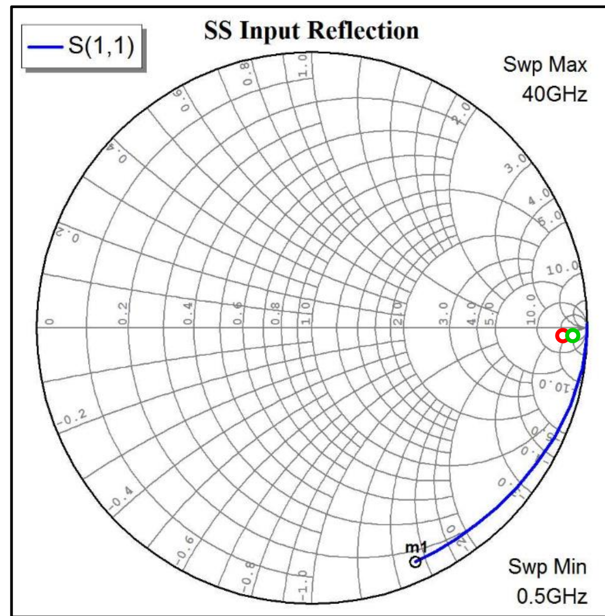

Figure 6-11 The scattering parameter S11 measured at 4 GHz for an AlInSb/InSb Schottky diode at zero DC bias (red circle), and 50 mV *DC bias (green circle). The blue curve is a simulated S11 which has been generated by sweeping the frequency from 0.5 GHz to 40 GHz. The proposed equivalent circuit model has been used to generate the data using Microwave office.*

approximately $200\,mV$. Therefore, future studies should take into consideration applying $200\,mV$ when conducting the S-parameters measurements. Reducing the effects of parasitic capacitance and series resistance would enhance the device performance of the presented Schottky diode and raise its operation frequencies. Reducing the diode series resistance has been discussed in 6.7.1. However, several measures can be taken to minimize the capacitive effect. Firstly, the parasitic of the device pads and connection should be de-embedded from the measurements using the Open and Short structures to calibrate the VNA before taking the measurements. A mask of Open and Short structure has been designed for this purpose, see 6.8.1.1. Secondly, scaling down the device active area is an effective way to reduce the junction capacitance (C_j). Furthermore, the parasitic capacitance (C_{pp}) can also be reduced by removing the high dielectric AlInSb layer around the anode active area and replacing it with an insulating layer such as SiO_2 or SiN.

6.8.1.1 Open-Short De-Embedding

Open-short de-embedding is a popular technique which is used to the effects of the parasitic components (capacitance and inductance) from the measured device operating at high frequencies. In practice, this method is reliable up to ~40 GHz (or higher depending on the tested structures size). The design of the open structure keeps the signal pad isolated from the ground pads as illustrated in Figure 6-12 (b). The open-de-embedding is mainly used to remove the effects of parasitic capacitance associated with the pads. The design of the short structure connects the signal pad to the ground pads as shown in Figure 6-12 (c). The short structure is mainly used to extract the device impedance. In this device, the only impedance referred to is the contact pads resistance.

Since extracting the parasitic components is necessary for modelling the diode equivalent circuit, future work should involve using the open-short de-embedding features to determine the device parasitics as well as removing their effect from the S-parameters measurements. This process requires taking separate RF measurements for the open and short de-embedding structures along with the RF measurements of the active device itself. The extracted parasitic elements should then be introduced to the diode equivalent circuit.

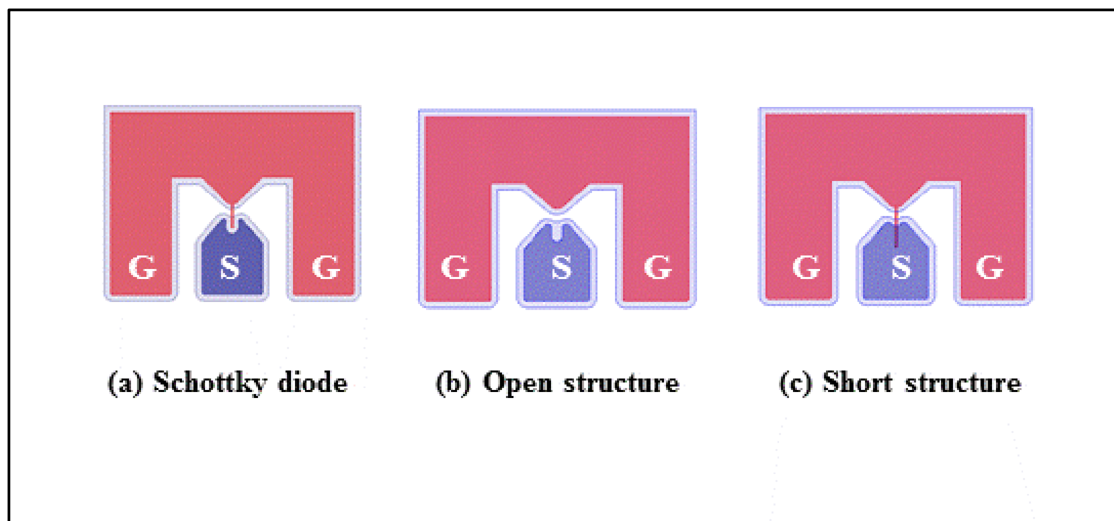

Figure 6-12 The layouts of three chosen structures from a mask which has been designed to enable RF measurements. The Structures layout of (a) Schottky diode, (b) open de-embedded, and (b) Short de-embedded. The RF pad has the arrangement of ground-signal-ground.

6.8.2 Large Signal Measurements

Although the S-parameter measurements are invaluable for characterizing the device with a linear response, such measurements are inadequate for nonlinear devices because nonlinearities generate harmonics of (Nf_o) frequencies at their output when stimulated by a continuous wave (CW) signal at a fundamental frequency (f_o). Thus, measuring nonlinear devices requires measuring the amplitude and phase values of the fundamental and the generated harmonics together with DC measurement.

When considering a periodic signal, measuring the frequency domain incident and reflected signals (i.e., a and b) at the terminals of the non-linear DUT can be used to reconstruct the voltage and current waveforms in the time domain as

$$v_i(t) = \sqrt{Z_o}\ \left(a_{i(t)} + b_i(t)\right) \tag{6-8}$$

$$i_i(t) = \sqrt{Z_o}\ \left(a_{i(t)} - b_i(t)\right) \tag{6-9}$$

where (i) is the port number, (Z_o) is the load impedance, and

$$a_i(t) = \sum_{n=1}^{N} a_{i,n} \, . \sin\left(n\omega_o t + \varphi_{a_{i,n}}\right) \tag{6-10}$$

$$b_i(t) = \sum_{n=1}^{N} b_{i,n} \, . \sin\left(n\omega_o t + \varphi_{b_{i,n}}\right) \tag{6-11}$$

The variables $a_i(t)$, $b_i(t)$, $(\varphi_{a_{i,n}})$, and $(\varphi_{b_{i,n}})$ stand for the amplitude and phase values of the power signal measured at the fundamental frequency, and the harmonics, respectively.

In this work, large-signal measurements were performed to evaluate the linear behaviour of an AlInSb/InSb Schottky diode at a fundamental frequency of 4 GHz for different power levels. The device was able to detect up to six harmonics. In this measurement a power source is used to deliver power at a certain DC bias in the middle of the anticipated working range. The incident power is increased gradually from small to large values letting the RF voltage swing to include the entire working range. Using spreadsheet analysis[2], the applied RF (I-V) locus has been reconstructed from the measured data using sinusoidal functions considering the addition of phase offset at

[2] Microsoft Excel 2016 by Microsoft for Windows.

each harmonic. The measurements were conducted at a fundamental frequency of 4 GHz for six values of input power under two bias conditions as shown in Figure 6-13 (a) at zero-bias, and (b) after applying a bias of 50 mV. When a large AC signal is applied, the operating point of the Schottky diode moves along the DC (I-V) if the device doesn't show any reactance. However, in the presence of reactance, the operating point moves in loops due to the waveforms mismatch between the measuring system and the DUT. The area enclosed by the locus stands for the power dissipated in the

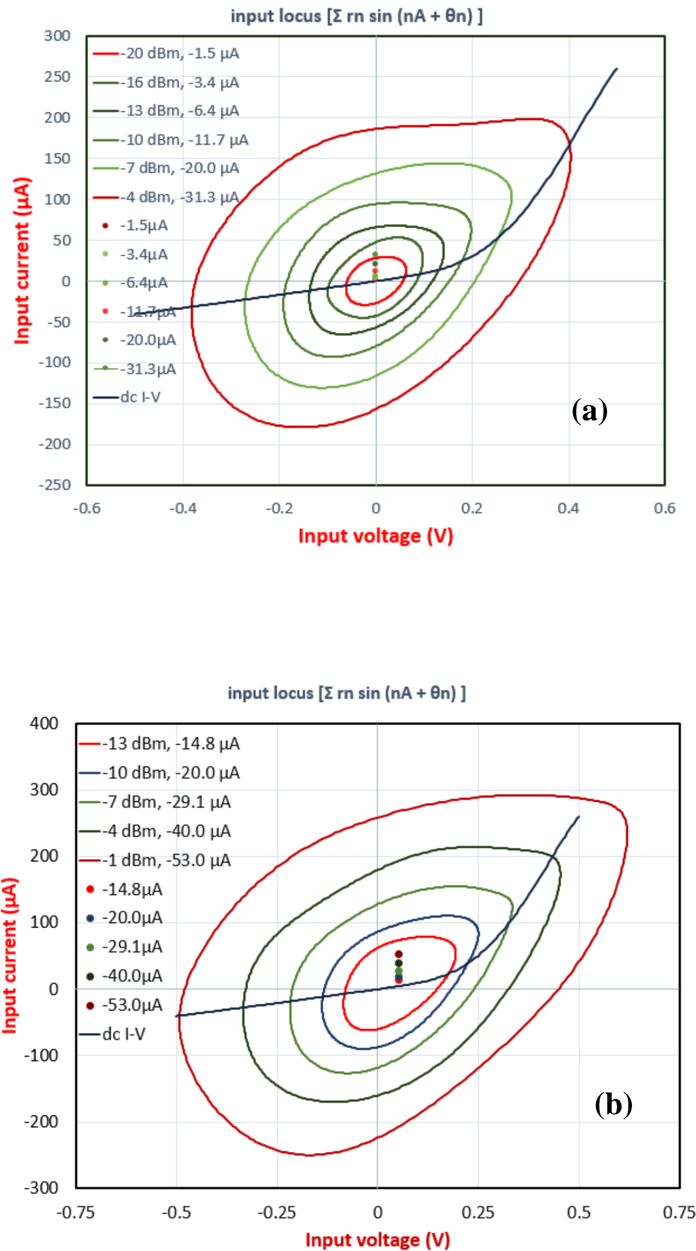

Figure 6-13 Input loci for the AlInSb/InSb Schottky diode at (a) zero DC bias, and (b) 50 mV *DC bias (towards the knee) at several input powers. Each locus refers to a certain input power. The DC current is also visualised.*

diode while the locus shape expresses the nonlinearity characteristics of the designated operating region. The higher irregular shape indicates greater nonlinearity. The phase mismatch between the current and voltage signals for the presented detector is shown in Figure 6-14. It is apparent from the figure that the current is leading the voltages which suggest a dominance of the capacitive component on the diode performance. Therefore, the power loss in the realized diode is due to the charging and discharging effect of the diode capacitance. Applying a DC bias of 50 mV has improved the diode sensitivity. It is apparent that at the same input power level, the biased diode is detecting a larger current than the zero-bias diode. For instance, the detected current at -13 dBm for the biased diode is ~300 µA compared to ~100 µA for the unbiased diode. However, the diode sensitivity can be further improved by raising the DC bias to 200 mV, where the diode has its maximum curvature coefficient.

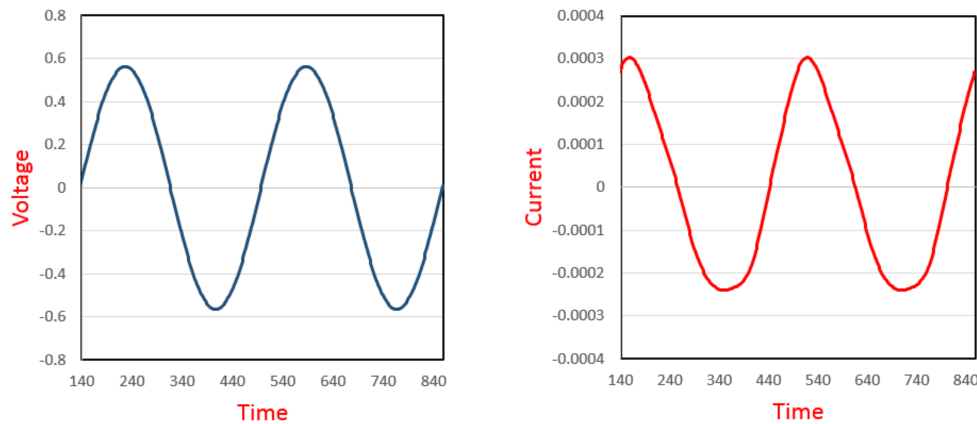

Figure 6-14 The reconstructed time domain current and voltage waveforms for the realized AlInSb/InSb detector. It is apparent that the current is leading the voltage which indicates a capacitive effect.

6.9 Summary and Conclusions

In this chapter, an initial design of a small-area AlInSb/InSb Schottky diode has been presented. The device structure is designated for RF measurements which are essential for testing the diode at high frequency. An equivalent circuit model for the realized diode has been proposed which is shown to be an effective tool in the analysis of device performance. The accuracy of the proposed model will only be confirmed when circuit components are fully defined. The device has also been partially tested using DC and RF measurements. Although the preliminary DC and RF measurements reveal the

potential of using the presented device as a detector at 4 GHz, the device exhibited a power dissipation due to the capacitance and series resistance effects. Reducing the device capacitance and series resistance is essential to minimize the power loss. Device optimization through excessive vertical and lateral scaling to the device active area can lead to a substantial increase in the device output power at high frequency. It is also anticipated that device optimization can significantly improve the diode performance towards higher range of operating frequencies. An estimated total diode capacitance of $100\ fF$ and a measured diode series resistance of $150\ \Omega$ result in a cut-off frequency around $\sim 10\ GHz$. Reducing the capacitance and resistance by halve raises the cut-off frequency to $\sim 40\ GHz$. However, device adjustments require a full description of the device components which can be achieved using Open and Short structures (already designed for this purpose for these structures). Hence, optimization of the AlInSb/InSb Schottky diode and full device characterization are one of the perspectives for future work. Future device characterization should involve looking at the noise level and device sensitivity in addition to extending the RF measurements beyond 4 GHz. For instance, looking at the device performance at 100-200 GHz will push assessment beyond more conventional devices and would demonstrate this material toward the state of the art.

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Chapter 7

Summary and Conclusions

This study provides a significant opportunity to develop our understanding of AlInSb/InSb Schottky diodes through carrying out extensive investigation of electrical I-V-T characteristics. The study has involved design, fabrication, measuring, as well as modelling tasks. Many trials were made using different epi layers and various surface treatments to achieve AlInSb/InSb-QW Schottky diodes. For this purpose, two different planar designs (elementary structure, and surface channel structure) have been reported. The devices with surface channel structure showed improved performance over the devices with elementary structure. After fabrication, the devices have been evaluated by means of I-V measurements. The I-V measurements were first performed at room temperature then over a wide range of temperature 3-290 K. In chapter 4, the room temperature I-V measurements have been used to calculate the fundamental diode parameters (barrier height, ideality factor, and diode series resistance) while the analyses of temperature dependent measurements have been presented in chapter 5. Low and large signal RF measurements have been carried out in chapter 6 to do a very basic assessment of AlInSb/InSb Schottky diodes for mmW applications. The summaries and outcomes of these chapters can be categorised as

- **Room Temperature Measurements**.

Various models (Rhoderick, Norde, Cibils, Werner, and Cheung) have been used to examine the I-V characteristics of the obtained AlInSb/InSb Schottky diodes. It has been found that in general the barrier heights of the obtained diodes can take one of two different values, ~0.36 or ~0.16 *eV*. It was demonstrated that the barrier with 0.36 *eV* height followed the theory of Fermi level FL pinning at one-third of the energy gap,

while the lower magnitude barrier was more likely to obey a Schottky-Moot rule or mid-gap FL pinning theory. The variance in the barrier height was attributed to the applied surface treatment which can alter the position of the Fermi level due to changes to the density of surface states. The analysis of room-temperature measurements also revealed a high series resistance leading the diode current in the forward bias. The value of the diode series resistance depends on the devices design, it is higher for the small area devices with surface channel structure than the larger area devices with elementary planar structure. Due to the low barrier height of the AlInSb/InSb Schottky diodes, the diode series resistance can raise the value of the ideality factor considerably. Therefore, precise calculation of the ideality factor as well as barrier height can only be achieved by ruling out the voltage drop across the series resistance from the I-V data. The simulated I-V characteristics based on the extracted diode parameters were found to fit accurately to the experimental data. Future work on AlInSb/InSb Schottky diodes should focus on determining as well as eliminating the sources behind the high diode series resistance.

- **Temperature Dependent Measurements**

The analysis of I-V-T measurements revealed that both the barrier height and ideality factor of the AlInSb/InSb Schottky diodes have strong temperature dependence. The Richardson plot was also found to exhibit nonlinearity over the entire temperature range 3-290 K. The most common effects to explain these anomalies were investigated. A temperature-dependent energy gap, image force lowering, and tunnelling effects have all been used to help explain the temperature-dependent barrier heights observed.

A temperature-dependent barrier height for the $Al_xIn_{1-x}Sb$ alloy was calculated using an empirical expression. According to thermionic emission theory, the barrier height should follow the variance of the bandgap energy with temperature. However, the value of the energy bandgap was found to increase slightly with decreasing temperature which leads to a slight increase in barrier height which reaches its maximum value 0.05 *eV at* 3 K. This behaviour opposes the experimental values which reported a substantial decrease in barrier height. Therefore, the temperature dependency of the energy gap added another anomaly to the experimental results.

Barrier lowering due to the image force effect was also calculated to clarify the temperature dependency of the barrier height. The maximum barrier lowering assuming

a doping level of $10^{17}\ cm^{-3}$ was found to be 25.4 meV at 300 K and 25.5 meV at 3 K which are far less than the experimental values observed. Due to the low values and the countless variations of barrier lowering with decreasing temperature compared to the experimental results, it was concluded that image force has a minor impact on reducing the barrier height. It is concluded that image force alone is not sufficient in explaining the experimental variation of barrier height with temperature.

Barrier reduction due to tunnelling current TFE was also considered to explain the temperature dependence of the barrier height using Pavodani and Stratton theory. The experimental value of the tunnelling constant E_{oo} was found to be much higher than its theoretical value which indicates a substantial contribution of tunnelling current to the total AlInSb/InSb Schottky diode current. However, the barrier reduction due to thermionic field emission $\Delta\Phi_{\mathrm{TFE}}$ over the measured temperature range did not match the experimental results. The theoretical zero bias value of $\Delta\Phi_{\mathrm{TFE}}$ was found to be too large to explain the experimental barrier height at high temperatures and too low to explain the experimental results at low temperatures. These discrepancies in the temperature dependence of Φ_B cannot explain the experimental results without assuming another tunnelling mechanism that enhances the diode tunnelling current.

As a result of the presence of defects in the AlInSb/InSb system, and due to the failure of image force and tunnelling effects in fully explaining the strong temperature dependency of barrier height in addition to increasing the tunnelling probability with increasing temperature, a substantial contribution of trap assisted tunnelling via trap states was concluded to be responsible for the temperature dependent barrier height of the measured AlInSb/InSb Schottky diodes. Trap assisted tunnelling current dominates over the TFE current in the higher temperature range.

Temperature dependency of the ideality factor was analysed by plotting the experimental values of $\eta\mathrm{kT/q}$ against kT/q compared to theoretically generated curves related to the most common conduction mechanisms (TE, FE, TFE). The experimental results were found to follow what is called as T_o anomaly effect. Due to the strong T_o effect, it has been concluded that the mechanism of charge transport in the AlInSb/InSb Schottky diodes is neither FE nor TFE which supports the assumption for the contribution of another conduction mechanism to the total diode current.

The Richardson plot, which is normally used to extract the barrier height Φ_B, and the Richardson constant A^{**} did not show linearity. The observed non-linearity in the plot was analysed in the light of the T_o effect and potential fluctuation model. The plot has been successfully linearized with both methods. The potential fluctuation model was found to give an accurate value for the Richardson constant, albeit with a slightly unrealistic barrier height.

- **RF Measurements**

Small area AlInSb/InSb Schottky diodes have been demonstrated to be promising candidates for microwave detectors and they still away from being used as millimetre wave detectors. The devices have been initially evaluated using DC and RF measurements. The curvature coefficient and the diode differential resistance were extracted from the DC measurements. The maximum curvature coefficient γ was found to be $11\ V^{-1}$ at a bias of $200\ mV$, and the differential resistance was found to be $2.5\ k\Omega$ at the same voltage .Two types of RF measurements, low-power and high-power measurements were conducted to test AlInSb/InSb Schottky diodes at 4 GHz. The signal was successfully detected despite the observed power dissipation through the device parasitics, series resistance and junction capacitance. Power loss due to parasitics can be eliminated through optimizing the device geometry. Device optimization via excessive vertical and lateral scaling to the device active area is expected to introduce substantial improvement to the device output power and its frequency response. Optimization of AlInSb/InSb Schottky diodes and precise characterization are one of the perspectives for future work. Future work should include using Open and Short devices to enable de-embedding of parasitic components. Precise characterization requires looking at the noise level and device sensitivity as well as measuring the device at higher frequency 100-200 GHz.

APPENDIX A

A. Designed Masks

Two photomasks[3] have been created in this study. The first mask was set for processing small-area planar Schottky diodes with surface channel structure, the design of surface channel structure have been developed to work in the millimetre and submillimetre wavelengths [1, 2]. The high operation frequency of surface channel devices is due to their low parasitic capacitance compared to other elementary planar structures. The second photomask was set for de-embedding the pad effects from the measured data practically at high frequency measurements using Open and Short de-embedding technique.

A.1 Schottky Diodes Mask

In general, the photomask has been divided into four (4"×4") masks. Each mask comprises an individual layer. The first layer is used to define the ohmic contacts, the second layer is used to define the Schottky contacts, and the third one is used to define the mesas. There is another layer to define mesa for vertical devices, but this layer was not used in this study. Alignment marks are also included in the masks to ensure precise stacking of diode elements during fabrication, cross shape marks are situated on the top corner or side of each field. The entire masks layout contains repeated patterns of three different fields of 36 $mm \times 36$ mm sample size. Each field is enclosed with an opening frame, the frame helps a lot in the alignment process and can be used as a guide for cleaving the samples. One of the three fields is dedicated to make two-terminal Schottky

[3] KLayout 0.243 has been used to create the photomasks. The designs were saved in GDS-II format and sent to Compugraphics to manufacture a standard chrome mask of 8"×8".

diodes that are used for conducting DC measurements. The other two fields are dedicated to make three-terminal Schottky diodes that are used for RF measurements. With these masks, three photolithography steps are required to finalize the devices processing. The first lithography defines the ohmic contacts, the second lithography defines the Schottky contacts, and the last lithography defines the mesas and air bridges around the Schottky fingers. The layout of each field will be described in the next sections

A.1.1 Two-Terminal Schottky Diodes

The field layout of the two-terminals diodes which were patriculry designed for conducting DC measurements is illustrated Figure A-1(a). The field is divided into four groups of diodes, the first three groups are dedicated for micron size devices. These devices can be defiened with standard photolithography. The fourth group is dedicated for submicron diodes. Defining the submicron devices requires an electron-beam lithography. Generally, each diode has two contact pads, one for the ohmic contact and the other is for Schottky contact. The contact pads were designed with a relatively large area 80×70 μm to enable electrical bonding without peeling off. The effective Schottky contacts were designed in finger-like shapes in three different widths 1, 2, and 4 μm and six different lengths 1, 2, 4, 6, 8, and10 μm for each single width. The distance between the finger and the ohmic was also constructed in two different values 2, 4 μm. A snapshot of a two-terminal Schottky diode with a finger of 2 μm length and 2 μm width and a separation of 2 μm is shown in Figure A-1 (b). All devices in the same group have the same finger length and each row has five identical diodes, has the same finger width and length and the same Schottky-ohmic separation gap. The Schottky-ohmic separation gap was set to be 2 μm in the upper six rows and 4 μm devices in the lower six rows. To enable devices identification, all the devices dimensions were labelled to left of each row. The label for a device with of 10 μm length, 2 μm width, and of 2 μm gap was set to be 10L2W2G.

A.1.2 Three-Terminal Schottky Diodes

Two separate fields have been designated for three-terminal Schottky diodes. Devices in each field have two different configurations. One of the fields has of separate devices and the other field has chains of connected devices. The field layout of the separate

devices is illustrated in Figure A-2, and the layout of the connected devices is illustrated in Figure A-3. In the of three-terminal designs, a coplanar waveguide structure (CPW) has been introduced to the Schottky diodes to enable GSG measurements. However, the effective small-area Schottky contacts geometries (width, length, gap) and devices arrangements are the same of the two-terminal devices that have been described in A.1.1.

A.2 Open-Short Mask

In RF measurements, a measured signal with a calibrated probe represents the response of the device under test including parasitics effect, capacitance and inductance, associated with probe pads. To get an accurate response for device under test, pad parasitics must be removed. An Open and Short technique[3] is one of the common methods for de-embedding the pad parasitics. A new photomask with open and short features was created to achieve parasitics de-embedding measurements. The mask has 10 repeated fields stacked in two rows. Each field is divided into four devices. The first devices group contains the Open and Short patterns and the other three groups contain three-terminals Schottky diodes. The fingers geometries (width, length, gap) and devices arrangements are the same as the two-terminal devices that have been described in A.1.1. The layout of a whole field is shown in Figure A-4. The figure shows a 3-terminal diode and their Open and Short patterns.

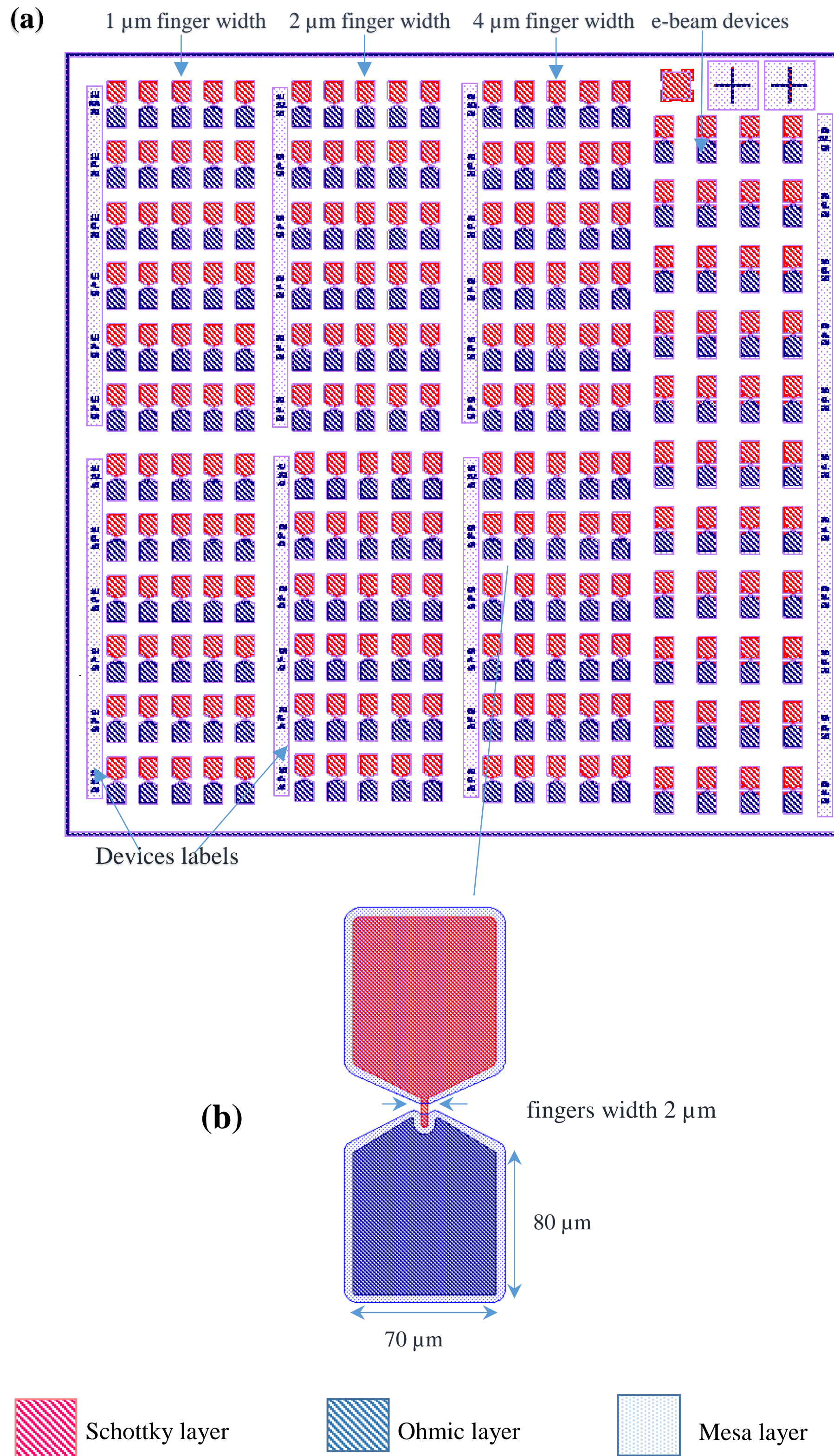

Figure A-1 Two snapshots for (a) a field of 2-terminals Schottky diodes showing the two layers designated for Schottky and ohmic contacts. (b) two-terminal Schottky diode with a finger of 2 µm length, 2 µm width, and finger-Schottky gap of 2 µm. The mask layers, Schottky, Ohmic, and mesa are illustrated.

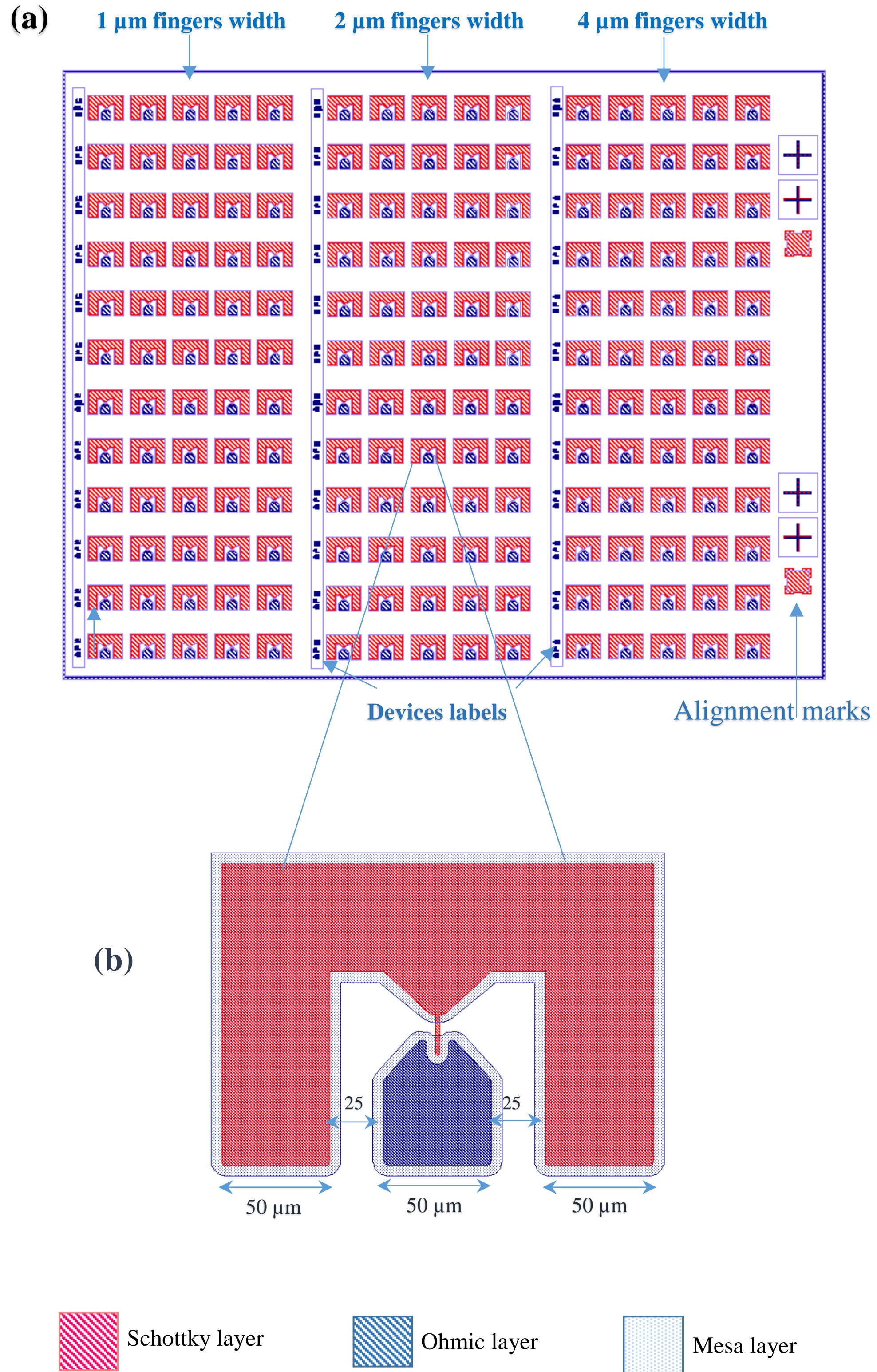

Figure A-2 Two snapshots for (a) a field of three-terminals Schottky diodes, and (b) a three-terminal Schottky diode with a finger of 8 µm *length and 2* µm *width and a finger-Schottky gap of 4* µm*. The mask layers, Schottky, Ohmic, and mesa are shown.*

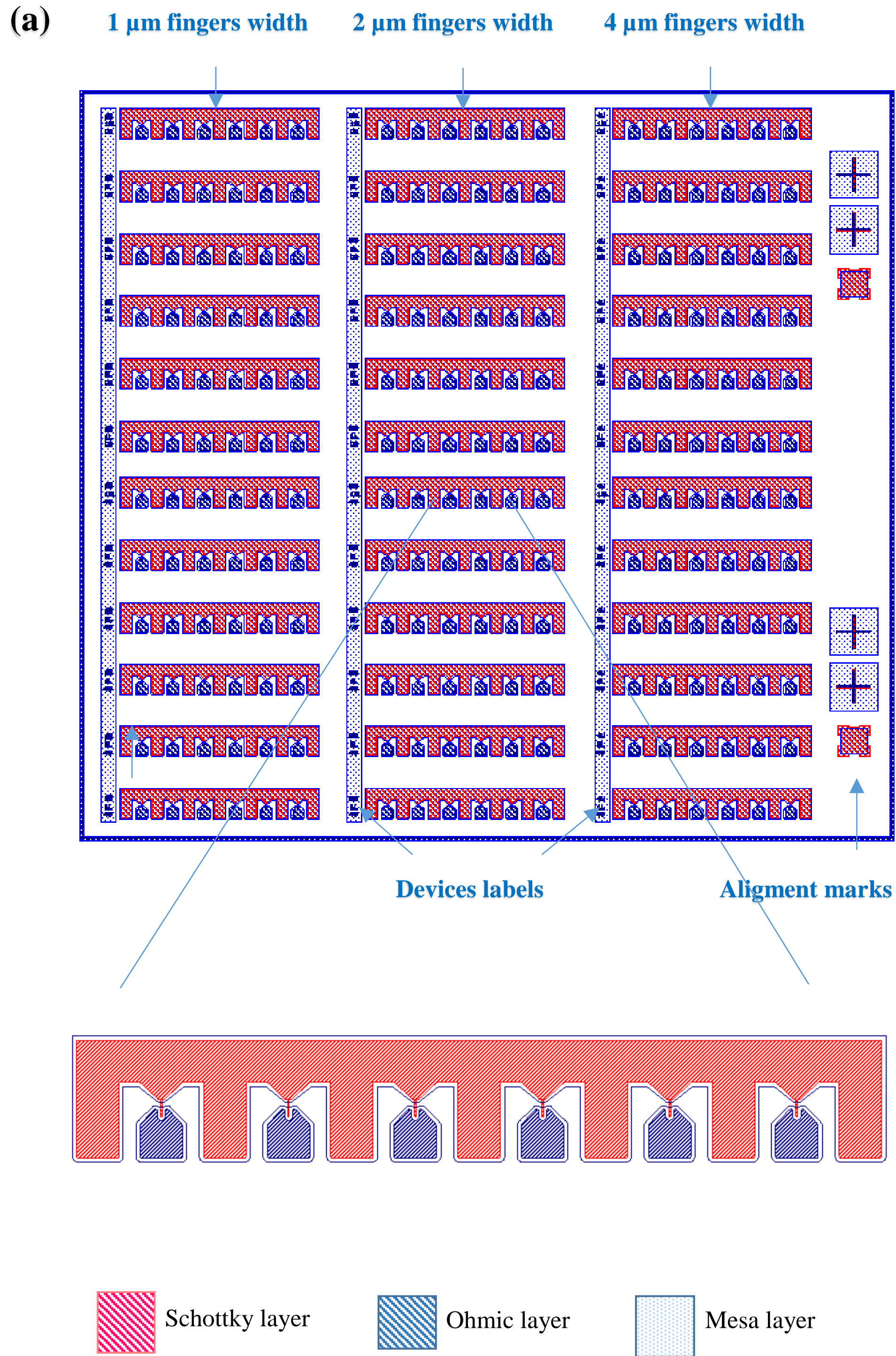

Figure A-3 Two snapshots for (a) a field of 3-terminal Schottky diodes, and (b) a chain of two-terminal Schottky diodes with a finger of 10 µm *length, 2* µm *width, and finger-Schottky gap of 4* µm*. The mask layers, Schottky, Ohmic, and mesa are illustrated.*

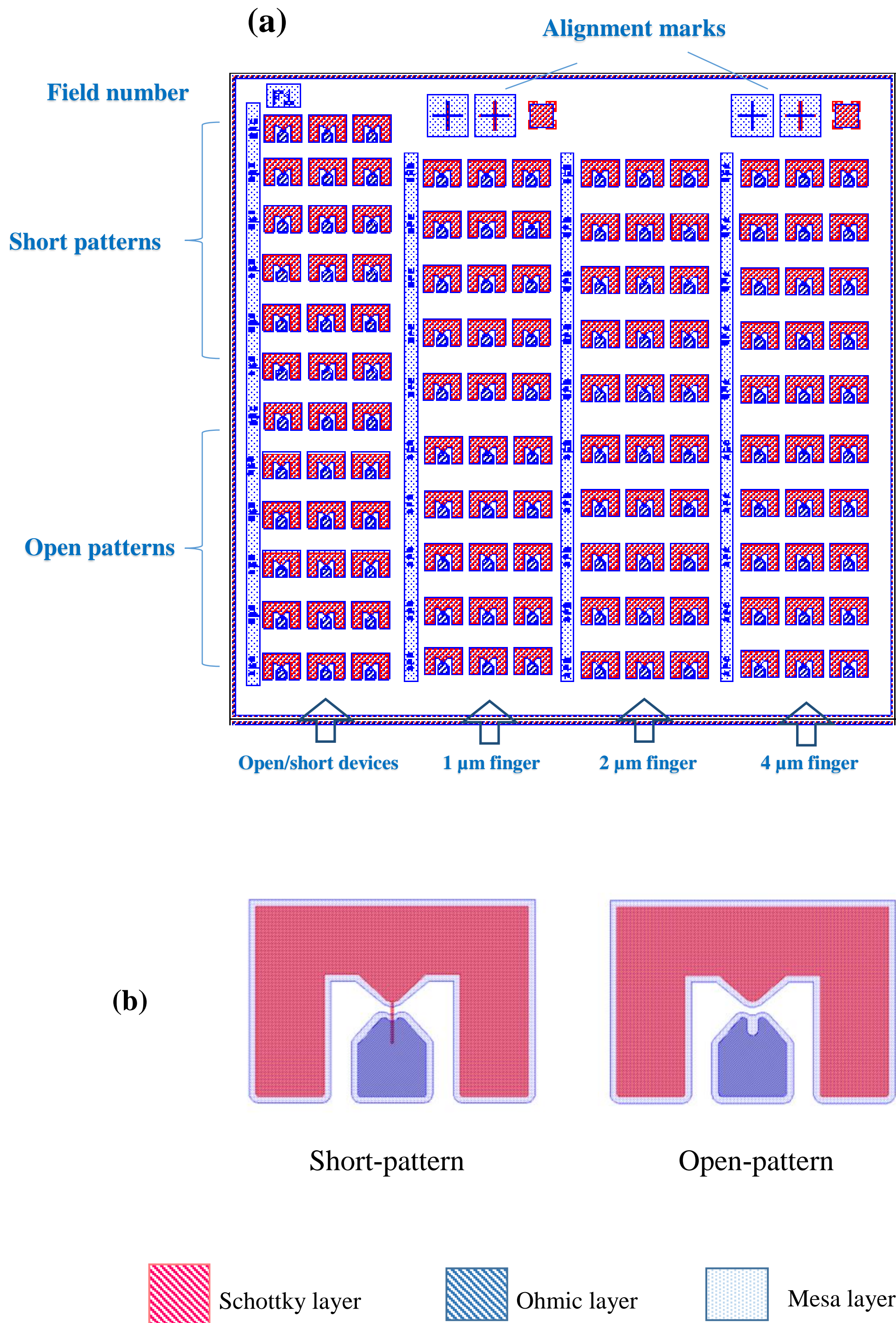

Figure A-4 Two Snapshots for (a) field layout of Open and Short de-embedding technique and (b) Open and Short patterns.

A.3 Bibliography

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