Design and Application of an Advanced Fully Active Harmonic Load Pull System Using Pulsed RF Measurements and Synchronised Laser Energy.

A thesis submitted to Cardiff University
in candidature for the degree of

Doctor of Philosophy

by

Michael Anthony Casbon

Division of Electrical and Electronic Engineering
School of Engineering
Cardiff University
United Kingdom

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Abstract

The objective of this work was to advance the design of Active Harmonic Load-Pull systems to facilitate accurate modelling of RF semiconductors, with specific regard to time dependant behaviours.

Pulse capability is added, to extend the thermally safe operating region, investigate thermal behaviour, and reduce the thermal loading on the system components. The safe operation region extension is demonstrated with a GaAs die, the thermal aspects of behaviour are illustrated with GaN on SiC, GaN on Si and GaN on diamond die.

A violet laser is added, which releases some types of trapped charge, helping to reveal the full potential of the device. The thermal transient response of the device is thereby exposed, and the trap filling times may be studied. The application of this to GaN die with and without Source Coupled Field Plates is described. The relevance of the light wavelength is briefly investigated.

A novel wafer probe station is described, providing access to the backside of the wafer for photonic trap release and the measurement of hot electron electroluminescence, as RF measurements are conducted on the front side.

Replacing the drain RF and DC circuits with a fixed resistor, and stepping the gate voltage allows the device to be held at any point on the load-line and then moved to another, here this demonstrates that the residual “knee-walkout” on a GaN on SiC part with an optimised source coupled field plate is not a thermal effect, and must therefore be due to trapped charge, despite the field plate.

A low loss diplexer/ bias tee combination with very good DC supply memory properties is described, demonstrated with a InAlN/GaN die at Ka band.

Accurate measurement of harmonics is vital to waveform engineering. Here a novel method of increasing the effective dynamic range of the system is presented.

Acknowledgements

Firstly I would like to thank Prof. Paul J. Tasker for his support and guidance, he can now add "*teaching an old dog new tricks*" to his distinguished record. I would also like to thank my colleagues and fellow students at Cardiff, and express the hope that I have repaid the co-operation and support they have given me.

The WIN Semiconductor corporation of Taiwan provided privileged access to prototype devices, enabling many of the comparative studies performed herein, as did UMS. Without their help this work would not have been possible.

The Welsh Assembly Government must also be thanked, their funding of the "Green Communications" strand of the Knowledge Transfer Centre project indirectly enabled me to follow these studies.

Some of the work described has been carried out on research grants from the EPSRC, notably the measurements of Hot Electron Luminescence, performed in collaboration with Dr. T. Brazzini of the Centre for Device Thermography and Reliability at Bristol University.

My family have been very patient, and I hope I have not neglected them too badly these last few years.

Lastly I would like to mention P. E. Irving MBE, whose book "Tuning for Speed" gives a good grounding in a rigorous and holistic approach to engineering design and was an early inspiration for me. His maxim "*Simplicate and add lightness"* provides food for thought in all engineering disciplines, and is notably applied here to the design of the Ka-V band diplexer.

List of Publications.

M.A. Casbon, P.J. Tasker and J Benedikt, "*Waveform Engineering beyond the Safe Operating Region*" IEEE CSIC Symp. Dig., Hawaii, HI, Oct 16-19, 2011, pp. 37-40.

Wei-Chou Wang, Chia-Hao Chen, Jhih-Han Du, Ming-Hung Weng, Che-Kai Lin, Chieh-Chih Huang, Chien-Chih Chang, Shih-Hui Huang, Yi-Feng Wei, Yao-Chung Hsieh, Michael Casbon, Paul J. Tasker, Wen-Kai Wang, I-Te Cho, Walter Wohlmuth, "*Development and Control of a 0.25μm Gate Process Module for AlGaN/GaN HEMT Production*" CS MANTECH Tech.. Dig., New Orleans, May 13-16, 2013.

M.A. Casbon, P.J. Tasker, "*Filter-less Diplexer Enables Active Harmonic Load-pull at Ka Band*" 81st ARFTG Conference, Seattle WA, June 2013

M.A. Casbon, P.J. Tasker, Wei-Chou Wang, Che-Kai Lin, Wen-Kai Wang, W. Wohlmuth "*Advanced RF IV Waveform Engineering Tool for use in device technology optimization: RF Pulsed Fully Active Harmonic Load Pull with Synchronized 3eV Laser*" IEEE CSIC Conference, Monterey CA, Oct 2013

S.Piotrowicz, O.Jardel, E.Chartier, R.Aubry, L. Baczkowski, M.Casbon, C.Dua, L.Escotte, P.Gamara, J.C.Jacquet, N.Michel, S.D.Nsele, M.Oualli, O.Patard, C. Potier, M.A.Di-Forte Poisson, S.L.Delage, "*12W/mm with 0.15μm InAlN/GaN HEMTs on SiC Technology for K and Ka-Bands Application*" Tampa FL, 2014

M. A. Casbon, P. J. Tasker, "*Comparison of Sampler and VNA based Large Signal Measurement Systems (LSNA) Under CW and Pulsed Operation*", 85th ARFTG Conference, Phoenix, Arizona, May 2015

T. Brazzini, M. A. Casbon, H. Sun, M. Uren, J. Lees, P. J. Tasker, H. Jung, H. Blanck, M. Kuball, *"Electroluminescence of hot electrons in AlGaN/GaN High Electron Mobility Transistors under radio frequency operation"* Applied Physics Letters 106, 213502 (2015)

T. Brazzini, M. A. Casbon, H. Sun, M. Uren, J. Lees, P. J. Tasker, H. Jung, H. Blanck, M. Kuball, *"Study of hot electrons inAlGaN/GaN HEMTs under RF Class B and J operation using electroluminescence"*, Microelectronics Reliability (2015)

M. A. Casbon, T. Brazzini, P.J. Tasker, M.J. Uren, M. Kuball, *"Simultaneous Measurement of Optical and RF Behavior under CW and Pulsed Fully Active Harmonic Load-Pull"*, 87th ARFTG Conference, San Francisco, California, May 2016

T. Brazzini, M. A. Casbon, M. J. Uren, P. J. Tasker, H. Jung, H. Blanck, M. Kuball, *"Hot-Electron Electroluminescence Under RF Operation in GaN-HEMTs: A Comparison Among Operational Classes."* IEEE Transactions on Electron Devices, May 2017, Volume 64, Number 5, page 2155

Table of Contents

Abstract		iii
Acknowledgements		v
Publications		vi
Table of Contents		vii
Chapter 1	Introduction	1
1.1	Historical Background & Outline	1
1.2	Structure of the Thesis	3
Chapter 2	Thermal Phenomena	9
2.1	Thermal Properties and Memory Effects	9
2.2	GaN on SiC devices	10
2.3	GaN on Si devices	12
2.4	Extension of the Safe Operating Area	18
2.5	Conclusions	18
Chapter 3	Trapped Charge Effects	21
3.1	Trapped Charge memory and Knee Walkout effects	21
3.2	The influence of 3eV light on trapped charge	23
3.3	Source Coupled Field Plates	28
3.4	The Effect of Intensity and Wavelength	31
3.5	Evaluating Trap Filling Times	34
3.6	Conclusions	35
Chapter 4	DC supply Memory and Multiplexing	37
4.1	DC supply Memory	37
4.2	Bias Tee Design	37
4.3	Frequency Diplexers and Multiplexers	40
4.4	Very Low Loss Diplexers and Multiplexers	42

4.5	A Fully Filter-less Multiplexer and Bias Tee for Active Harmonic Load Pull	52
4.6	A Ka-V band combined waveguide adaptor, diplexer and bias tee.	55
4.7	Conclusions	60
Chapter 5	Investigating Residual Walkout	63
5.1	Constant Load Measurements	63
5.2	Evaluating Possible Thermal Effects	63
5.3	Deep and Surface Trapping	65
5.4	High Speed Resistive Drain Load Testing	66
5.5	GaN on SiC Example	67
5.6	Separating the Effects of VDS and VGS using 3eV light and Waveform Engineering	70
5.7	Using RDL and extreme duty cycles to determine trapping time constants	79
5.8	Conclusions	82
Chapter 6	A Pulsed Active Harmonic Load Pull system	83
6.1	The Advantages of a Pulsed Fully Active Harmonic Load-Pull System	83
6.2	Principle and Method of Operation	90
6.3	Pulsed Measurements at Higher Fundamental Frequencies	96
6.4	Output Characteristic Measurement	98
6.5	Conclusions	100
Chapter 7	Harmonic Measurements & Dynamic Range	103
7.1	Improving the Accuracy of Harmonic Measurements Over Significant Dynamic Range	103

7.2	Conclusions	110
Chapter 8	Combined Optical and RF Measurements	111
8.1	Hot Electron Electroluminescence under RF Operation	111
8.2	The Optical and RF Wafer Probe Station	115
8.3	Measurement of Hot Electron Electroluminescence	118
8.4	Conclusions	123
Chapter 9	Applying the Methodology	125
9.1	Evaluating GaN on Diamond Devices	125
9.2	The Load-pull Measurements	125
9.3	Class F Performance	129
9.4	Pulsed Active Harmonic Loadpull Measurements	131
9.5	Applying the 3eV Laser	132
9.6	Conclusions	135
Chapter 10	Conclusions	137
10.1	Conclusions and Further Work	137
References and Bibliography		141
Glossary		145
Appendix A	Thermal Platform Design and Construction	149
Appendix B	Adding Pulse Capability to Fully Active Harmonic Load-pull Systems	199
Appendix C	DC Switching & Measurement during Pulsed Operation	209
Appendix D	Examination of GaN on SiC Devices	227
Appendix E	Examination of GaN on Si Devices	233
Appendix F	Examination of High Power GaN on Si Devices	237
Appendix G	Construction of a High Speed Resistive Drain Load	245

Chapter 1 Introduction

1.1 Historical Background & Outline.

As the demand for information services continues to develop, so the demands placed upon wireless transmission systems increase. More information must be transmitted in a given spectral bandwidth, and the energy consumption must be reduced to save costs, increase battery lifetimes and reduce CO_2 emissions. It is only possible to achieve these aims by gaining a deeper understanding of the semiconductors being used, enabling improved efficiency without degrading the linearity of the system. The intention of this work is to demonstrate several improvements and extensions to active load pull systems which assist in gaining that understanding, paving the way for what might be termed "Precision Waveform Engineering". The application of the work is demonstrated by describing practical examples which were carried out to solve commercial problems.

Every amplifier has a non-linear transfer characteristic to a greater or lesser extent, in some transmission schemes such as FM radio the issue is side-stepped by maintaining a constant output power, in others the amplifier is operated well below saturation point so yielding acceptable linearity, at the expense of energy consumption.

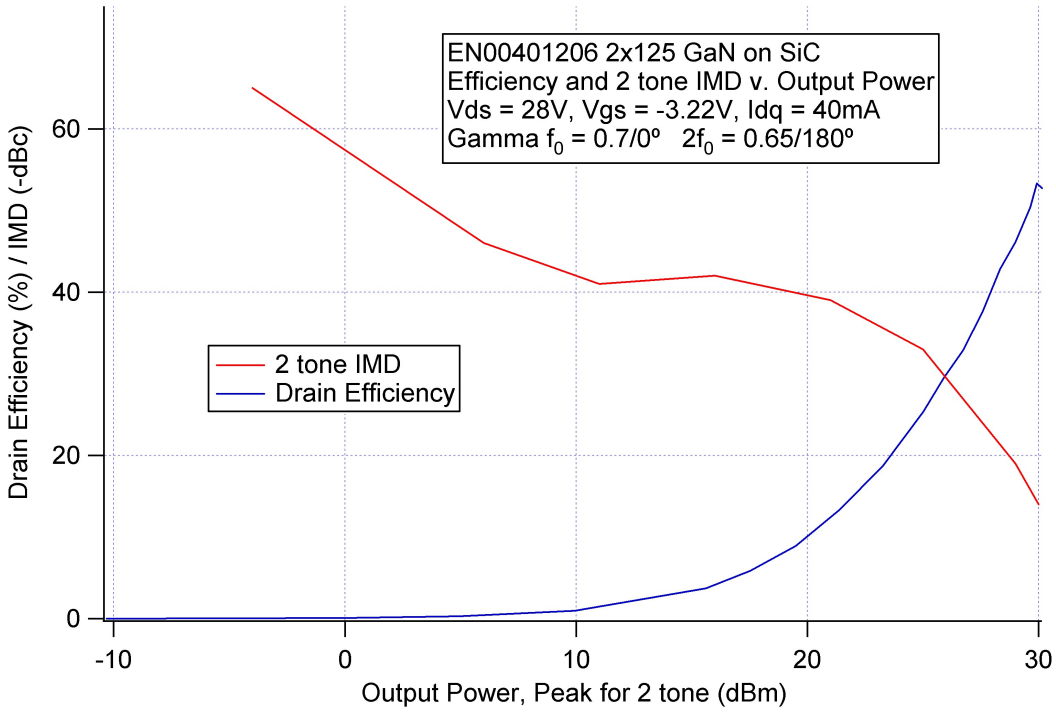

Figure 1.1 Typical Drain Efficiency and Linearity v. output power curves.

It is this second group where work has been focussed for many decades, an early tool to be developed was pre-distortion correction, whereby a low power circuit block on the input to the amplifier deliberately distorts the signal in the opposite manner to the amplifier, so the overall effect is a linear signal. A significant area driving this technique was terrestrial analogue television broadcast, the complex nature of these signals requires a high degree of linearity, the main carrier is amplitude modulated to convey brightness, a sub-carrier is phase modulated to convey the colour information, and the sound information is transmitted by a frequency modulated third carrier, though this is amplified separately on larger stations (the addition of stereo sound added a new QPSK carrier). The crowded UHF and VHF airspace used for such signals mandates stringent control of out of band inter-modulation products, in addition to the need to avoid distortion of the signals themselves, requiring operation well below saturation and subsequent poor efficiency. With output powers in tens of kWs and efficiencies less than 10% early systems needed vapour-phase cooling systems with massive heat exchangers, which themselves needed many kWs of energy to function, resulting in overall efficiencies around 5%.

Work with pre-distortion on Klystron amplifiers in the 1970's and 80's enabled the Klystrons to be driven further into the non-linear region, improving the amplifier efficiency to around 35%, a reduction in overall energy consumption for a large station with four 50kW channels from around 4MW to 1MW. A side effect of driving the Klystrons further into compression was that significantly more input drive power was required. As the semiconductor amplifiers used as drivers had to deliver more power it became impractical to use ultra linear class A designs with 0.5 to 1% efficiency, so the driver amplifiers were also included in the pre-correction. A problem soon emerged, it became apparent that the instantaneous output power depended not only upon the input power, but also upon *what the input power had been* prior to that instant - the devices exhibited memory.

Memory effects make pre-distortion correction significantly harder, since in order to calculate the pre-distortion required at an instant, the operating conditions of the recent past must be allowed for. Several different mechanisms are involved, each with different time constants; these are

i. Thermal memory

ii. Trapped charge memory

iii. DC supply memory

Existing Active Harmonic Load-Pull systems provide excellent detail of the steady state behaviour [1], but yield no information regarding these memory effects. The instrumentation described in this work allows these effects to be separated and thus quantified, the first step to designing circuits to accurately compensate for them.

A related problem in GaN devices is "knee walkout" [3], where the dynamic load-line does not achieve the expected minimum voltage across the device under RF conditions. The phenomena increases rapidly with the drain bias voltage and prevents full use of the high breakdown voltage capabilities of GaN. Again the cause can be thermal or trapped charge effects, the instrumentation developed here helps to differentiate between these, and for the device manufacturer provides a way to evaluate different device structures and processes [7, 24].

1.2 Structure of the Thesis.

With the intention of improving the flow of the reasoning and conclusions presented, extensive use of appendices is made. Much of the technical detail of the equipment and process of the measurements has been removed from the direct path while still being available if of interest. It is expected that this will also assist any who wish to reproduce or extend the instrumentation described.

While an attempt has been made in chapters 2, 3 and 4 to deal separately with the three types of memory effect, since one of the aims of this work is to enable differentiation between the types then inevitably some cross discussion must take place. A further complication is that some interaction may occur, if, for example, a trapped charge effect reduces the efficiency of a device then the operating temperature will increase, causing

a further reduction in performance - this will introduce a degree of sensitivity to the duty cycle and cooling arrangements which may lead to misdiagnosis of the root cause.

Chapter 2

Chapter 2 deals with Thermal Memory. The addition of pulse measurement capability to the fully active harmonic load-pull system using a VTD SWAP X402 receiver is described, with details in chapter 6 and Appendix B. It is applied to extend the measurement space beyond the continuous mode thermally safe operating region, investigate thermal behaviour by varying the duty cycle, and reduce the thermal loading on the test bench components. Measurements of GaN on silicon and silicon carbide substrates are compared.

Temperature controlled vacuum chucks are a regular feature of wafer probe stations, their use to make stable and comparable measurements at die level is routine. The thermal platform is described in Appendix A, which integrates with a universal RF device test fixture, allowing stable measurements to be made on packaged devices without the need to fabricate special fixtures, and also allows the performance variation with temperature to be measured. In order to extend its capabilities the fixture may be fitted with microstrip 5:1 impedance transformers, presenting a 10 Ohm impedance to the package terminals [14]. Critical points were the ground connection between the device and the RF circuits, the positioning of the temperature probe as close as possible to the packaged die, and the ability to precisely adjust the fixture to accommodate variations in package dimensions. The success achieved in meeting these goals is demonstrated by the measurement of Nitronex 50W and Sumitomo 40W GaN transistors.

Chapter 3

Chapter 3 deals with trapped charge memory effects, their investigation is assisted by the addition to the system of a violet (3eV) laser, synchronised to the pulse timing circuits. The effect of this is to sweep some types of trapped charge from the device, helping to reveal the full potential of the device, exposing the thermal transient response of the device to accurate measurement, and allowing the trap filling times to be studied. The effectiveness of this is shown by illuminating GaN on silicon carbide devices with

and without source coupled field plates. The DCIV curves are also affected by trapped charges, the laser is also applied to this problem.

Some of the trapping mechanisms have very long time constants, far greater than can be measured using the VTD SWAP X402, these are measured using data-logging power meters and DAQ units.

Chapter 4

Chapter 4 deals with DC supply memory; in itself this is fairly brief, as this aspect of design is entirely under the control of the system engineer. The measures taken to minimise such effects during device characterisation are discussed, concentrating on bias tee and diplexer design. The active harmonic load pull of a GaN HEMT at Ka band is included to illustrate the principles.

Chapter 5

From considering the results obtained in Chapters 2 and 3, it can be seen that when operating a GaN on SiC device at high DC bias voltages there is still a residual walkout effect, even on a source coupled field plate die in pulse mode with the 3eV laser engaged. It has been suggested that the cause might be inescapable nanosecond time scale thermal effects due to the dissipation involved in traversing the loadline, this being concentrated entirely within a microscopic sub-region of the channel under the gate, or alternately due to extremely fast charge trapping effects. To attempt to shed some light on this debate the simple (in principle) apparatus in Chapter 5 was built. By replacing the normal DC bias circuit and RF load with a resistor the device can be suspended at any point on the loadline, and then moved rapidly to another, specifically the problem "knee" region. The principal of the circuit is not in itself novel, but the speed of measurements attained and the addition of the laser permit new areas to be explored. Here this is used to show that the residual walkout does not depend upon channel heating effects, but entirely upon voltage, and must therefore be a trapped charge effect.

The addition of a Zener diode in parallel with the channel clamps the maximum drain voltage the device can experience, the equipment can then be used to show that while excessive negative gate voltages and high positive drain voltages can give rise to apparently similar trapping effects in GaN on SiC, the reaction to 3eV illumination is

significantly different, so it can be concluded that the charge trapping mechanism is different for the two situations.

Chapter 6

In this chapter the advantages, principals and applications of a pulsed fully active harmonic load-pull system are considered, including extending the Safe Operating Region during load-pull, examining thermal memory effects and other aspects of device design such as finger spacing. It is also shown that this system can quantify changes in pulse droop with VSWR, which could provide critical information for radar system designers before expensive commitments are made. Further practical details are to be found in Appendix B and C, techniques for switching the RF and DC are detailed. A current overload circuit is described which reduces the risk of damage to both the device under test and the test equipment, this system has the advantage over similar commercially available apparatus in that it also switches off the RF energy supplies in the event of an overload.

Chapter 7

In order to provide a useful tool for circuit designers it is required to take load-pull sweeps over a substantial dynamic range when generating look up table models, this is of particular importance with GaN devices as they exhibit a very soft compression characteristic, due to their distorted I-V curves. While operating near compression it is straightforward to obtain accurate measurements of the relatively high levels of harmonic signals, however, as the f_0 output power is reduced the harmonics drop at greater rates as defined by the intercept point relationships, resulting in noisy and unstable measurements. In Chapter 7 a novel method of increasing the relative power of the harmonics at the receiver is presented which has some advantages over previously employed techniques, this will help to realise the ever higher expectations of precision which are being placed upon Waveform Engineering measurement systems.

Chapter 8

A novel combined Optical and RF wafer probe station is described in this chapter, it was designed and built with the intention of facilitating measurements of trap release

effects, and also the electro-luminescence effects which GaN devices have been shown to exhibit [27]. The key feature is robust and repeatable access to the backside of the wafer, permitting extreme low light microphotography and spectroscopy, while simultaneously performing the full repertoire of active harmonic load pull techniques. The design suffers no discernible compromise in performance compared to a conventional manual wafer probe station, being stiff, rugged and easy to use, it would also be well suited for performing long term soak tests.

Chapter 9

In chapter 9 the techniques developed in this work are applied to help characterise a new technology, GaN on diamond. As well as assessing the RF performance, these methods are ideal for analysing the thermal properties, the key aspect of this material. The very small temperature changes experienced by the device, due to the excellent thermal conductivity of the diamond, revealed some interesting differences in the pulsed RF behaviour depending whether or not the drain bias was also pulsed. Previously these changes have been obscured by larger thermal effects.

Chapter 10

The conclusions formed during the work are collated here, together with discussions on how various aspects could be taken further.

Chapter 2 Thermal Phenomena

2.1 Thermal Properties and Memory Effects.

Since the behaviour of a semiconductor device is influenced by the temperature of the channel region, e.g. fig 2.1, and evidently the temperature of that region is controlled by the amount of heat being dissipated, then it is no surprise that the operating conditions experienced in the immediate past will influence the present behaviour, as a finite time is required for the temperature to change. Since a great deal of the overall temperature gradient between the channel and the ambient sink is in the very small region surrounding the channel, these effects can be rapid, spreading up into the micro-second region [Chapter 6, fig 6.11], however, since large metallic heatsinks may be employed as the final step to the ambient then several minutes may be needed to reach reasonable thermal equilibrium following a step change.

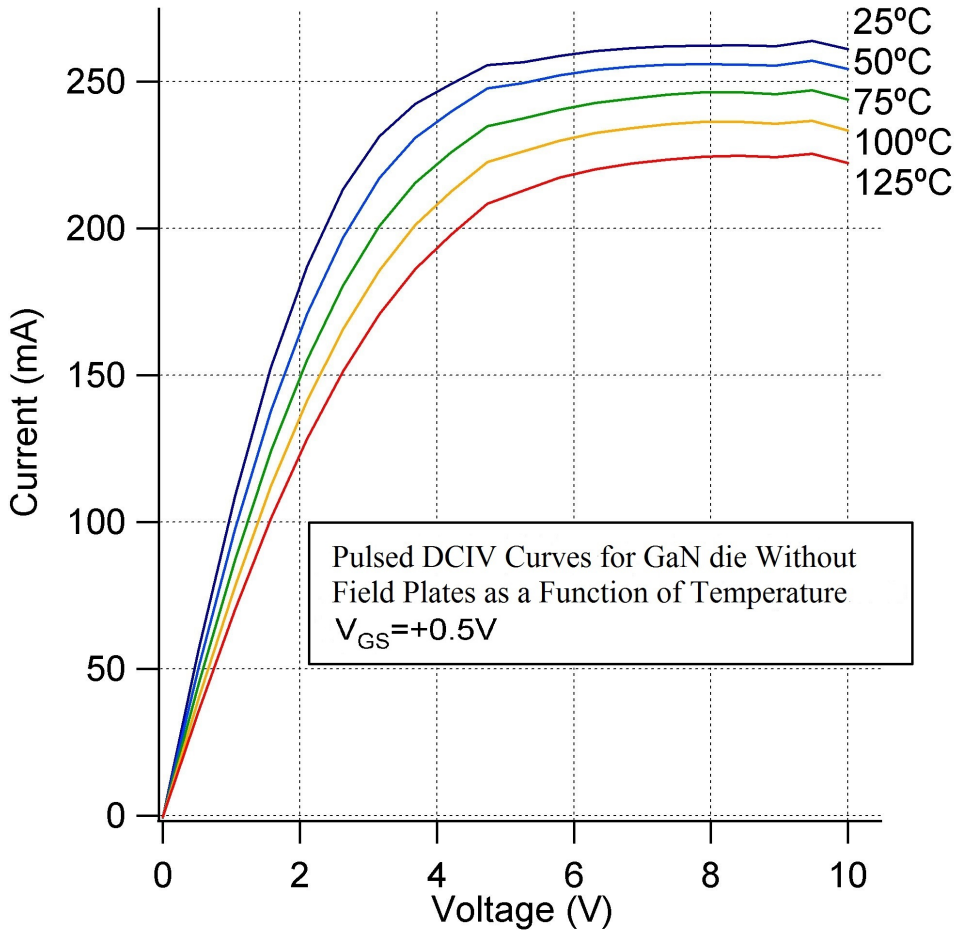

Figure 2.1 DCIV curves with temperature for a GaN on SiC device.

Clearly this problem splits into different areas of responsibility, the device manufacturer can only advise system designers on heatsinking arrangements, and in turn the system designer must depend upon the device manufacturer to optimise the thermal design of the device. Fortunately this behaviour depends mainly upon macroscopic physical structures, and so consistency can be expected, deviations are probably due to significant defects such as voids in the die attachment or distortion of the package flange, which must be eliminated for the sake of reliability rather than pre-corrected for.

The addition of the thermal platform to the load pull system (appendix A) allows measurements to be repeated at different temperatures and so establishes the baseline thermal behaviour, adding the pulse capability allows us to introduce a step change into the operating conditions and so expose the transient behaviour. Varying the duty cycle of the applied RF allows us further control over the channel temperature.

2.2 GaN on SiC devices

When working with GaN on SiC these thermal effects are quite limited, due to the high thermal conductivity of the SiC (360 to 490 W/(m·K)) combined with the efficient operation of the GaN. The results shown in fig 2.1and fig 2.3 are taken from a WIN semiconductor die measured on wafer, it is discussed in depth in Appendix D (GaN on SiC), [7] and [9].

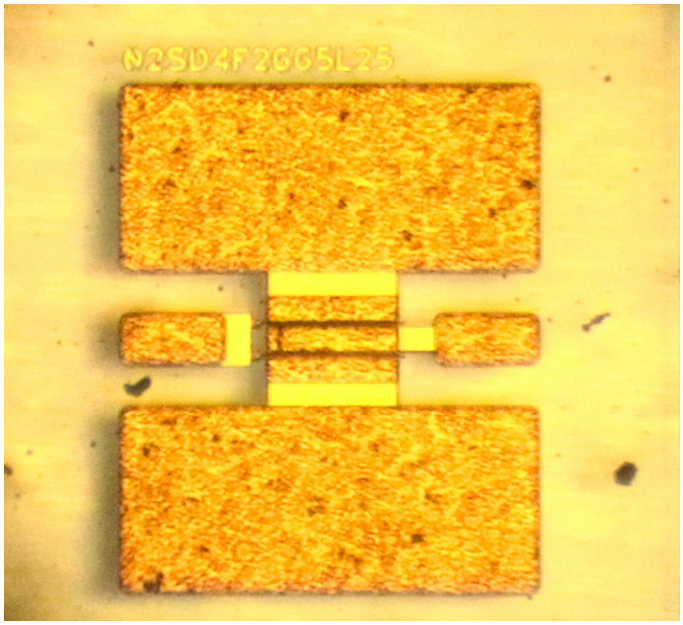

Figure 2.2 The WIN semiconductor GaN on Silicon Carbide device.

The DCIV behaviour is influenced by temperature, as seen in fig 2.1 above, but the change is quite modest in comparison to some of the knee walkout effects which can be found, fig 2.3.

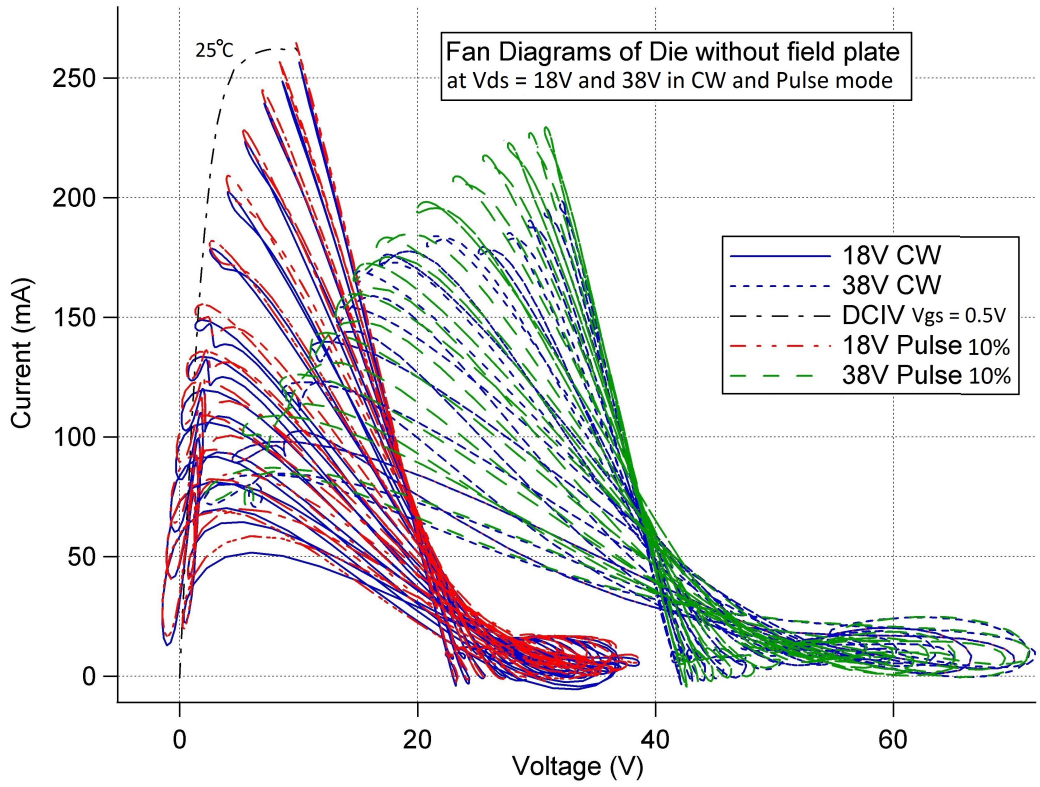

Figure 2.3 Dynamic loadlines for a GaN on SiC device under CW and 10% duty cycle pulse.

The curves in fig. 2.3 compare the behaviour under pulse versus CW at 18V and 38V drain bias. At 18V there is little difference, particularly at the shallower lines which represent the correct RF operation region. Moving to 38V substantial knee walkout is observed (chapter 3), resulting in significant thermal dissipation even at the optimum efficiency load, yet changing to 10% duty cycle has no major effect except at the steep loadlines well away from the optimum loads. We can conclude from this that the walkout seen here is not due to thermal effects with time constants of more than a microsecond. It has been suggested that thermal effects could occur on a nanosecond scale, occurring inevitably during the course of the loadline transit, that this is not in fact a significant cause of the effect seen here is demonstrated in chapter 5 “Constant Load Measurements”.

2.3 GaN on Si devices.

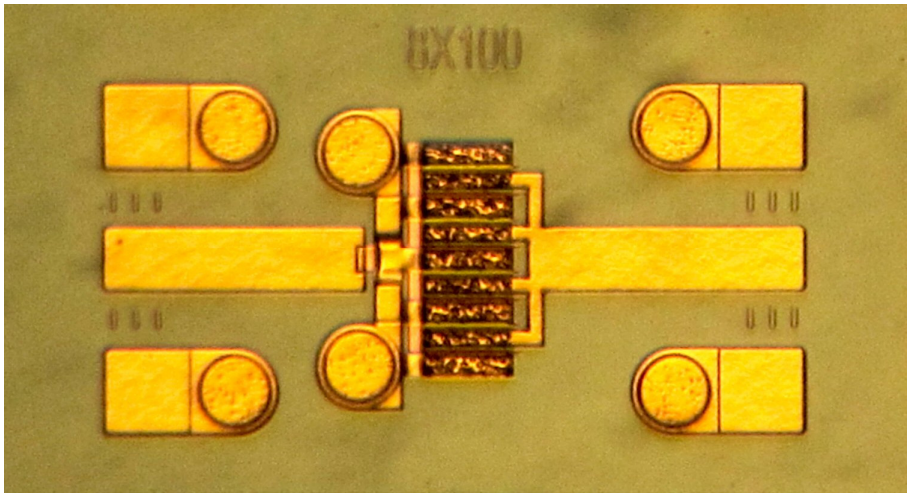

Figure 2.4 The 8x100 GaN on Silicon MMX device.

If similar tests are carried out on GaN on Si devices [appendix E] then the lower thermal conductivity of the silicon substrate will be apparent (149 W/(m·K)). The DCIV traces measured with 500us pulse width and 1% duty cycle show the expected drop in current with increasing temperature, fig 2.5.

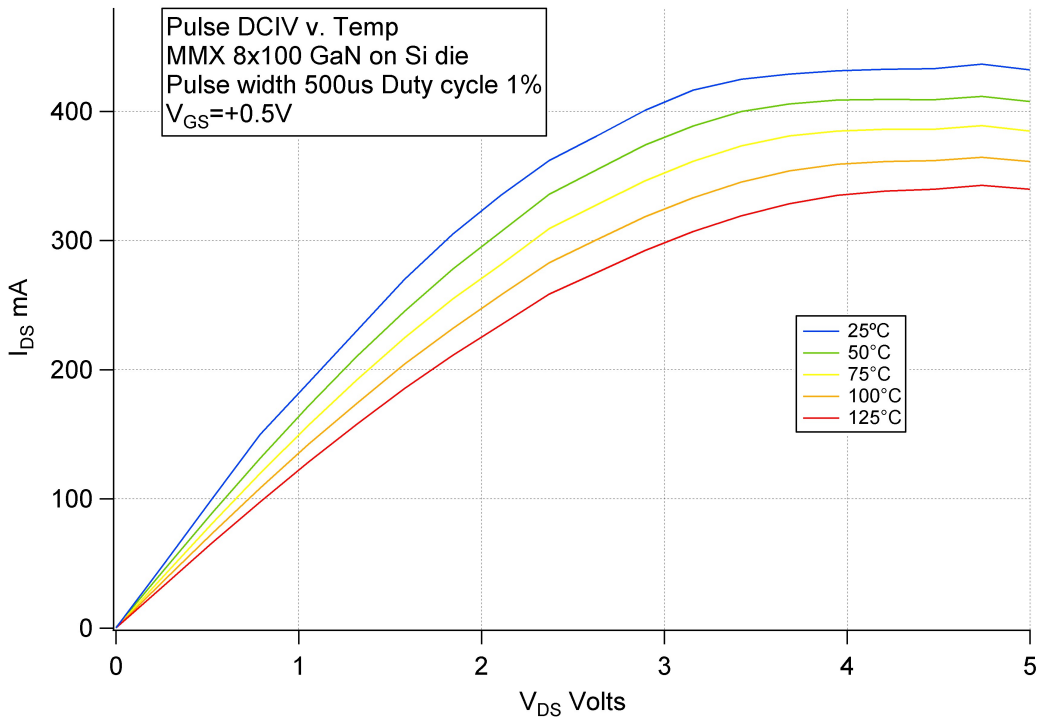

Figure 2.5 Pulsed DCIV curves with temperature for a 8x100 GaN on Silicon device 500us pulse width 1% duty cycle.

If we compare now the RF load-lines under pulse and CW we see an increased thermally induced drop at the steeper, low impedance load-lines, fig 2.6.

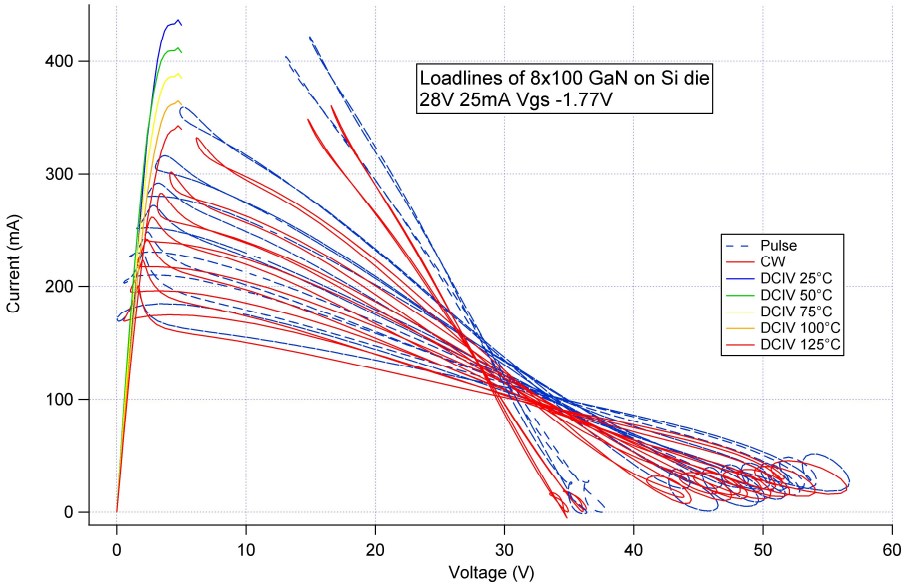

Figure 2.6 Loadlines for a 8x100 GaN on Si MMX device under pulse and CW.

If we look in detail at the load-lines in the efficient region however, fig 2.7, it can be seen that the device is still performing well, and in fact is approaching the DCIV quite closely. An interesting aspect of this device is that the efficiency is reduced by the onset of poor pinch-off rather than knee-walkout, it can be seen that as the maximum drain voltage increases the minimum current achieved rises.

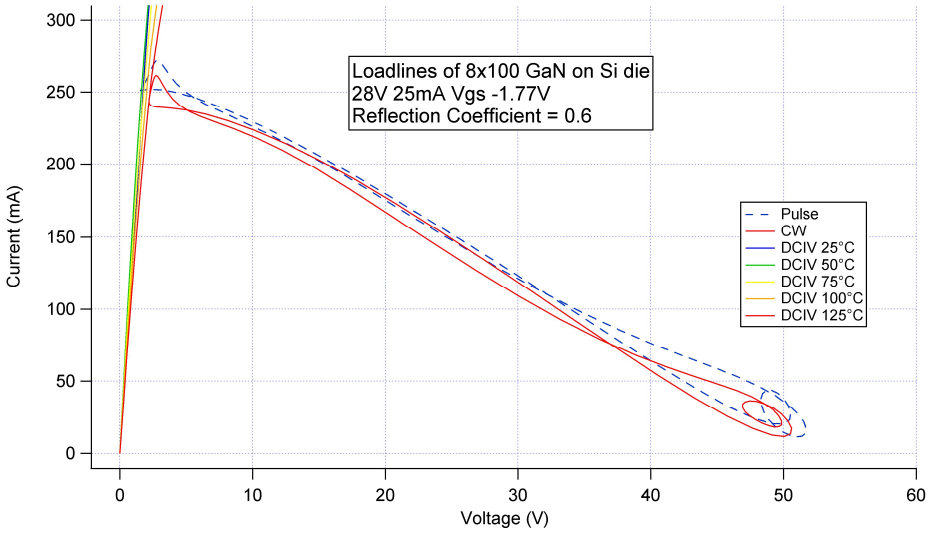

Figure 2.7 Load-lines under pulse and CW conditions for a 8x100 GaN on Si MMX device, Γ=0.6. RF pulse 10us 10% duty cycle, DCIV 500us 1% duty cycle.

The device being measured here is not designed to work at higher drain bias voltages, so it is not possible to see if knee walkout would commence at such voltages. A larger device capable of working at higher voltages but built with the same basic process was therefore measured next, the tests are detailed in Appendix F. The device has a rather unusual layout, fig 2.8, this tandem style helps to spread the thermal load and equalise phasing, air bridges are used to crossover the links joining the two gate and two drain conductors.

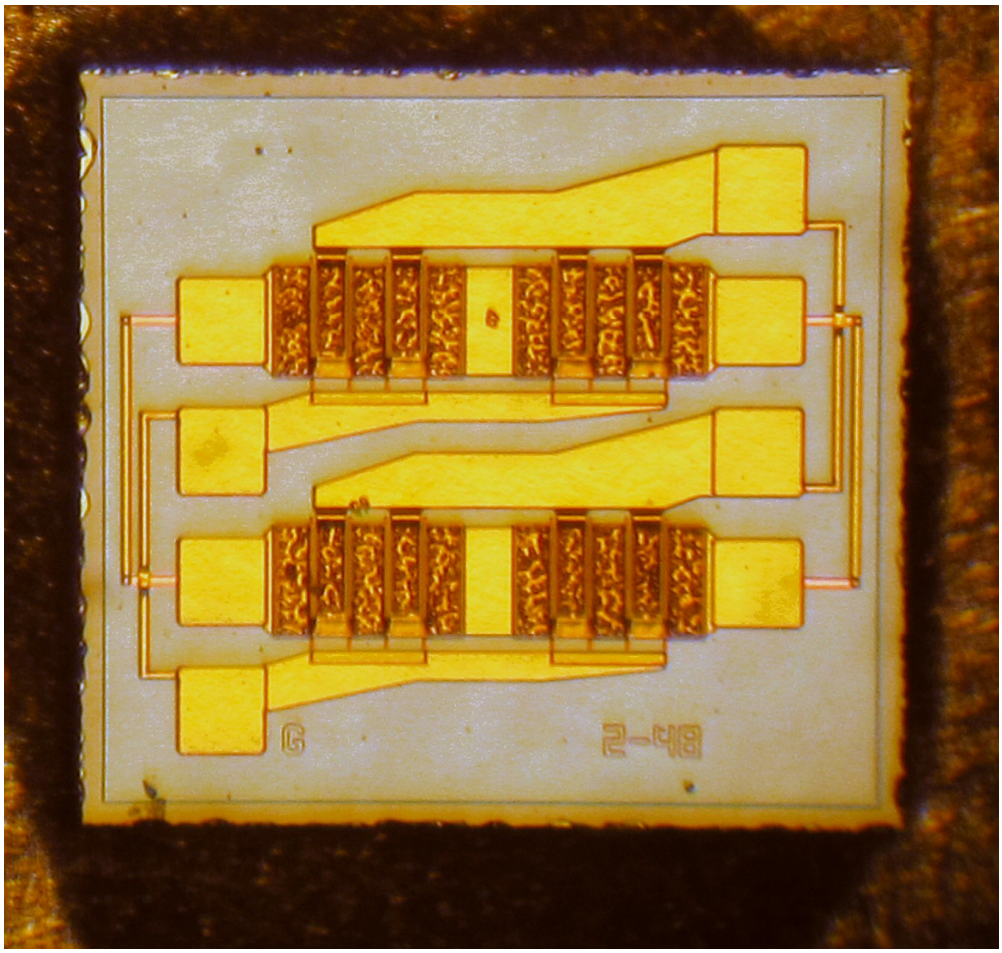

Figure 2.8 The larger GaN on Si device (MMXB die).

Figure 2.9 shows the DCIV traces versus temperature for this higher voltage device, measured under both pulse and continuous operation.

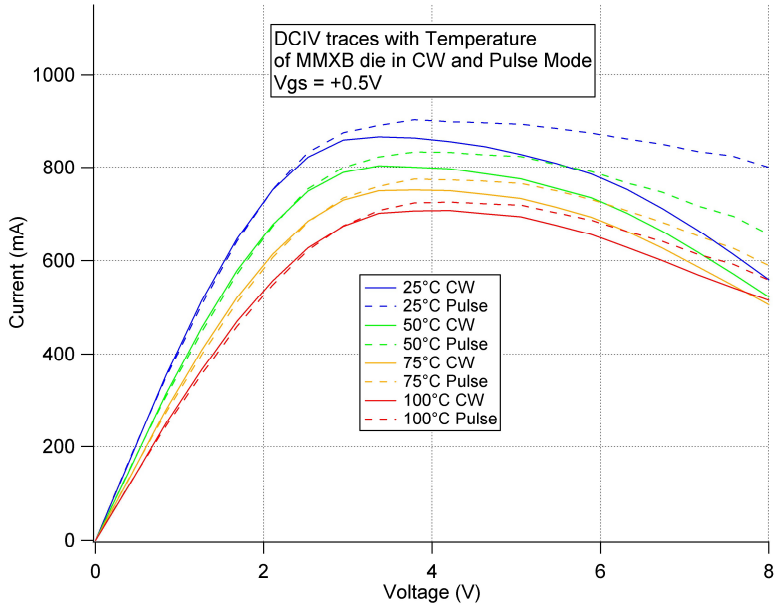

Figure 2.9 DCIV traces with temperature for GaN on Si MMXB device under pulse and CW operation. Pulse width 500us, duty cycle 1%.

Clearly the poor thermal conductivity of the GaN layers and silicon substrate is limiting the CW mode performance, even at the low drain bias voltages used for these DCIV tests. If this device were to be used in a transmission scheme which had linearity requirements and significant fluctuations in the peak to average ratio of the signal it would be no great surprise if thermal memory degraded the linearity.

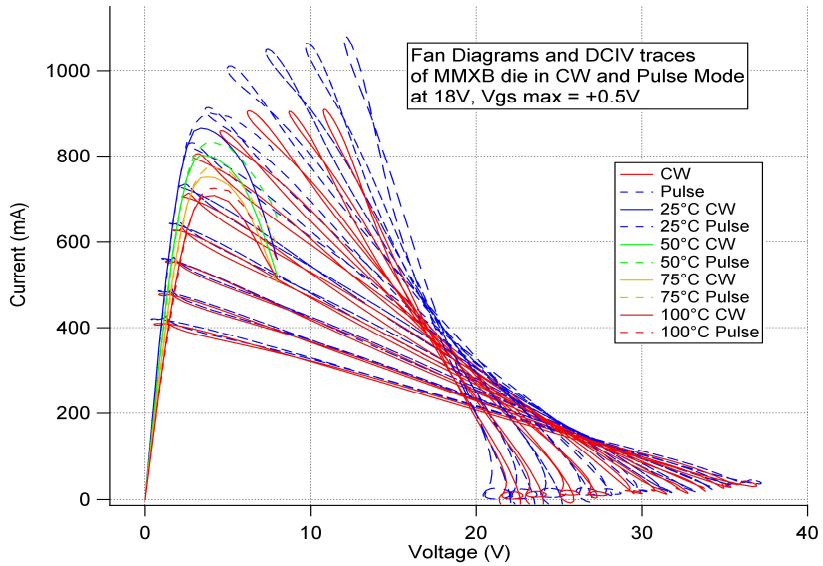

Figure 2.10 Loadlines for a GaN on Si MMXB device at 18V drain bias. RF pulse width 10us, duty cycle 10%. DCIV pulse width 500us duty cycle 1%.

If we consider the load-lines this view is confirmed; figs 2.10, 2.11 & 2.12. At 18V drain bias there is little difference between the pulse and CW load-lines for the high impedance loads (fig 2.10), as with the previous GaN on Si device. At 28V (fig 2.11) there is already a difference even at the highest impedance lines. When the drain bias is increased to 38V (fig 2.12) the device is clearly under strain in CW mode, V_{DSmin} has increased to 10V at I_{ds}=600mA, whereas in pulse mode the efficient high impedance load-lines still approach the DCIV curves. Due to the rising dissipation only the three most efficient load-lines were measured in CW mode at 38V, it was felt to be highly probable that the device would fail and damage the wafer probe if the higher dissipation lower impedance lines were attempted.

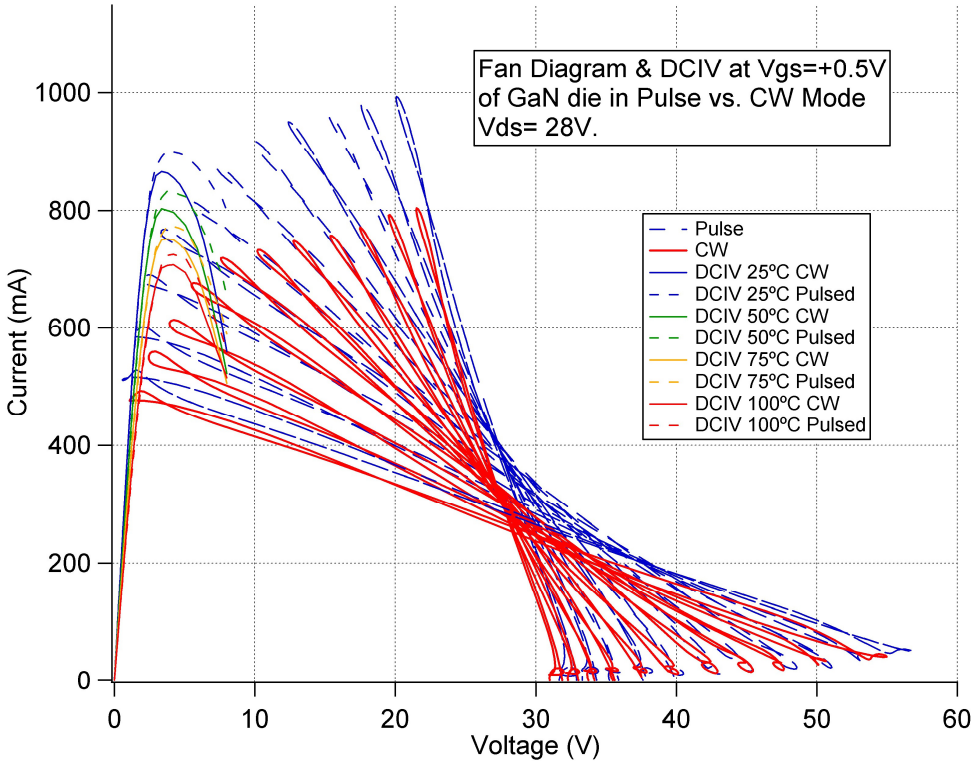

Figure 2.11 Loadlines for a GaN on Si MMXB device at 28V drain bias. RF pulse width 10us, duty cycle 10%. DCIV pulse width 500us duty cycle 1%.

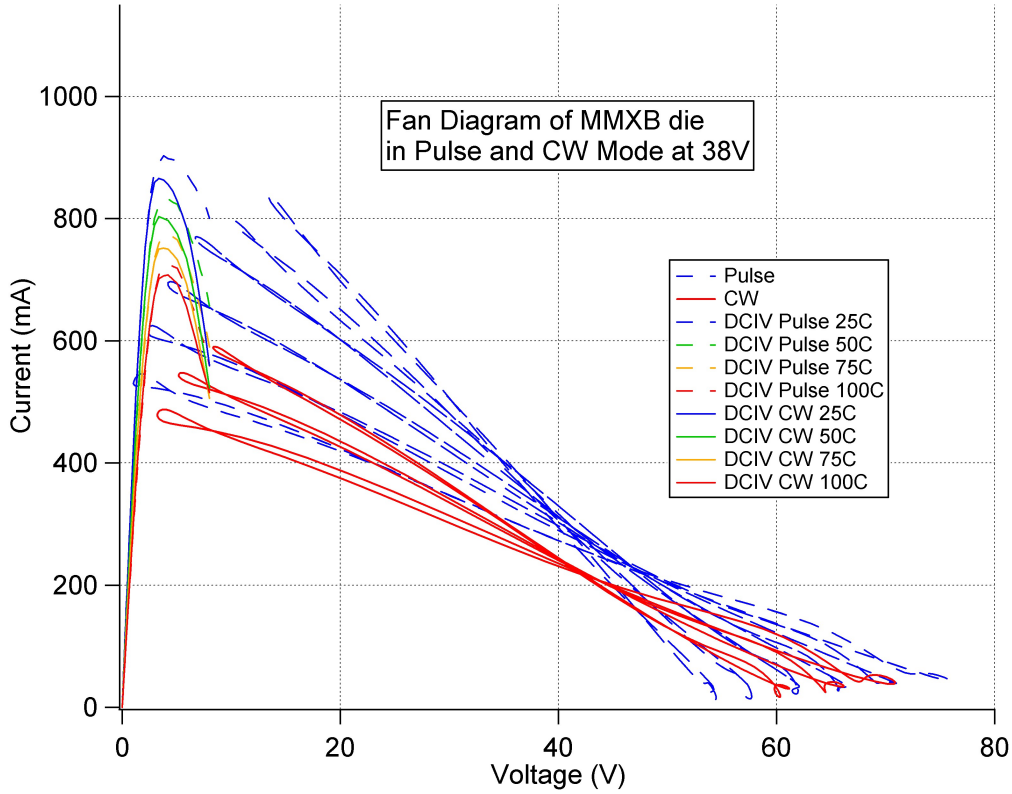

Figure 2.12 Loadlines for the GaN on Si MMXB device at 38V drain bias. RF pulse width 10us, duty cycle 10%. DCIV pulse width 500us duty cycle 1%.

While this larger GaN on Si device is clearly under strain in CW mode at 38V drain bias, the pulsed load-lines still come commendably close to the DCIV lines. It seems quite reasonable to conclude that it would be practical to use this device in a scheme with a high peak to average power ratio, as long as the thermal memory could be either ignored or compensated for. It is also apparent that performing a load-pull characterisation on the device in CW mode would carry a high risk of entering an area of the Smith chart which would damage or destroy the part, and also the wafer probe - and would not in any case return data which would be useful to the designer of pulsed or envelope tracking equipment. The last consideration alone is adequate reason to incorporate pulse capability into a load-pull system.

With regard to the idea of heating effects on a nanosecond timescale being mainly responsible for knee walkout, the fact that switching to microsecond scale pulse mode almost entirely relieves the walkout indicates that such a nanosecond scale effect is not significant in this case. (See also chapter 5, “Constant Load Measurements”).

2.4 Extension of the Safe Operating Area.

When conducting load-pull measurements it is inevitable that the device will be taken to areas of the Smith chart where it is subjected to stress, due to extremes of voltage, current or heat. Since the usual purpose of load pull characterisation is to map out the response of a new device the exact location of these dangerous regions will only be known in hindsight, anything which improves the chance of the device (and an expensive probe for on-wafer tests) not being damaged is useful. As mentioned briefly above while discussing fig 2.12, measurement under pulsed RF conditions greatly reduces the thermal stress that a device is under when measured in class B or similar modes. When testing in Class A this situation is reversed of course, the thermal dissipation would be higher during the RF blanked periods unless the DC is switched as well. In general devices for Class A are designed to withstand permanent operation at the DC bias point, typically being GaAs or VDMOS with a much larger die area for a given power, however some radar designs push the devices beyond this CW limit, again pulsed characterisation with switched DC is essential for such parts. A detailed discussion of this and related topics can be found in Chapter 6.

Recently it has been suggested that measuring loadlines representing a negative resistance could provide useful information for improving the performance of measurement based device models, this would result in very high heat dissipation during the measurements, it is likely that operating in pulse mode will keep this within safe limits and enable such tests.

2.5 Conclusions.

It has been shown in this chapter that adding pulse capability to an active harmonic load-pull system is highly desirable for at least the following reasons:

i) Thermally induced knee walkout can be easily distinguished from charge trapping induced problems and quantified, as it responds to duty cycle variations.

ii) Accurate data can be gathered for modelling pulsed and envelope tracking applications.

iii) A greatly increased thermal safety margin reduces the risk of device failure and subsequent test equipment damage, especially during the initial exploration phase.

The above points are expanded upon in chapter 6, “Advantages of a Pulsed Fully Active Harmonic Load-pull System”.

The benefits of Waveform Engineering are also highlighted by the way in which the cause of low efficiency is identified when measuring the devices on silicon substrates. If only traditional power and efficiency measurements were available it would be all too easy to assume that trap induced knee-walkout was occurring once the thermal effects were accounted for, when in fact poor pinch-off was the cause. Ultimately these tests allow an extra layer of characterisation enabling an idea of the formation of a parasitic conduction layer in the silicon base [24], this was proven by backside etching away the silicon from under the channel region and infilling with epoxy, and finally resolved by improving the process, another success for the Waveform Engineering concept.

Chapter 3 Trapped Charge Phenomena

3.1 Trapped Charge Memory and Knee Walkout effects.

It is well established that as semiconductor devices operate charge may become trapped in several different ways, as a space charge, attached to the surface or injected into the insulating regions [2, 13]. The presence of these charges will affect the behaviour of the device, causing the "knee" of the RF-IV characteristic to "walkout" from the DC-IV [3], as shown in fig. 3.1. Clearly the increase in the minimum drain-source voltage will reduce the available RF voltage range, reducing output power capability and degrading efficiency.

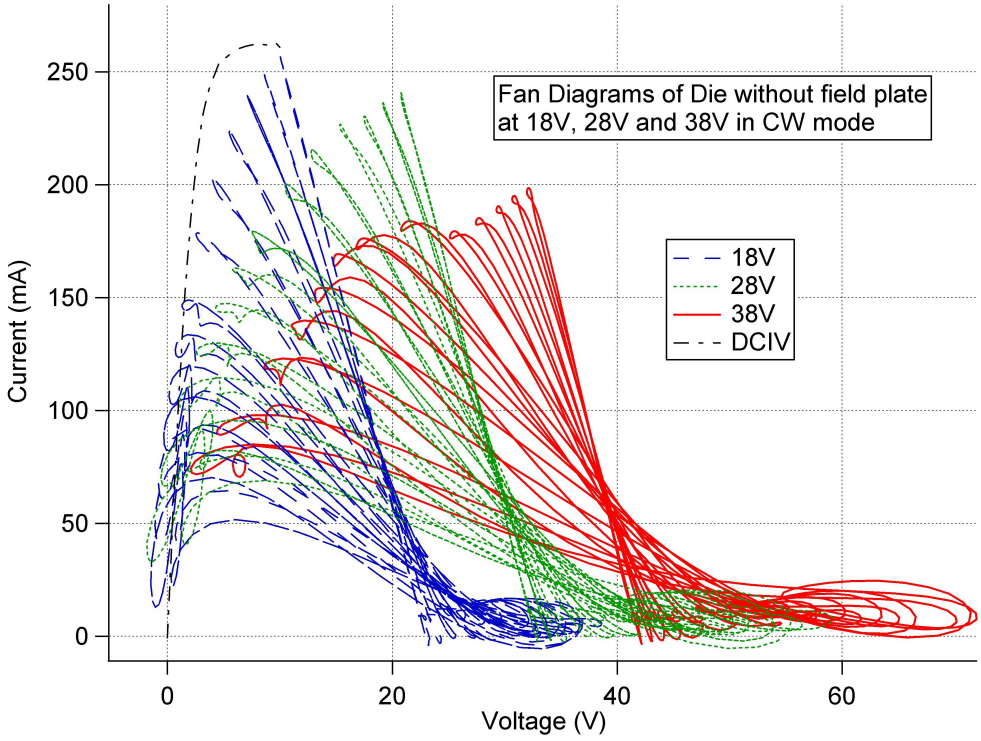

Figure 3.1 "Knee Walkout" in a Win GaN on SiC 2 x 125 device.

Different operating conditions will tend to fill or empty these trap sites and so the response of the device to a given stimulus will depend upon the previous operating conditions, it will exhibit memory. The use of active harmonic load pull systems to investigate these conditions under CW operation is well established [10], here we show how isothermal pulsed load pull measurements can isolate these characteristics [5,6], and further demonstrate how a synchronised laser can be used to empty some types of these traps [9], allowing the filling time to be easily measured. Thermal effects can

present very similar symptoms (chapter 2), the laser clearly separates the effects of trapping, allowing the true cause of a memory effect to be pinpointed.

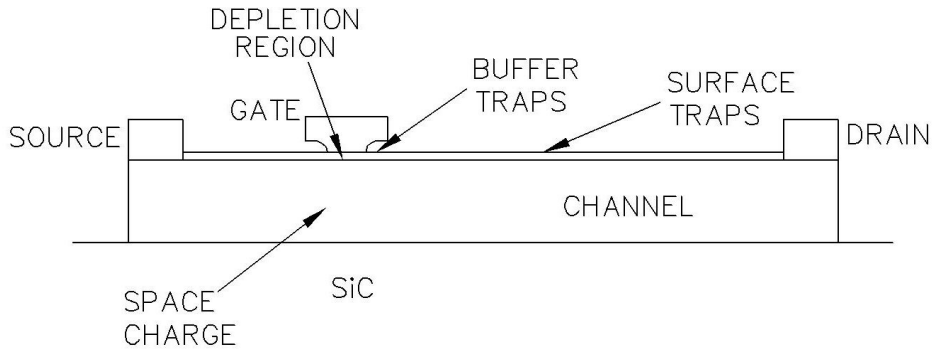

Figure 3.2 A simplified view of a FET showing possible trap sites. [13]

It was shown in chapter 2 (fig. 2.3 and 3.3) that examples of a GaN on SiC FET (fig 2.2) showed a significant knee walkout which did not respond to the duty cycle changing from 100% to 10% at normal operational loads, clearly some mechanism other than micro-scale heating is responsible.

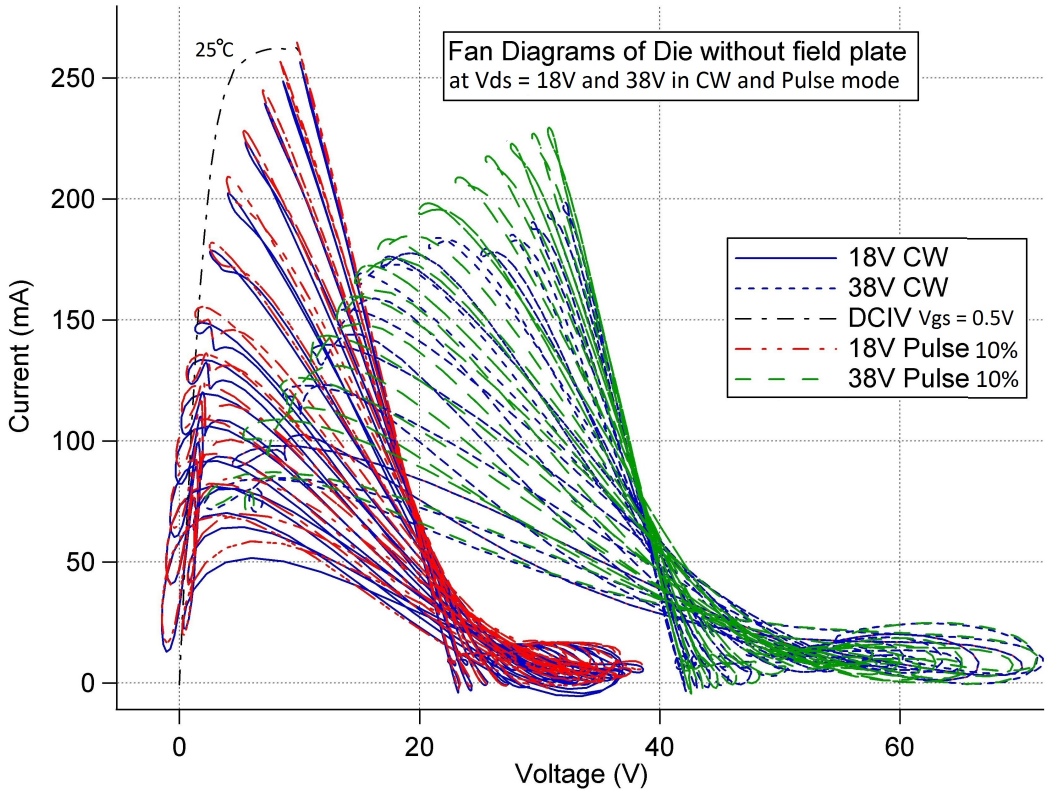

Figure 3.3 Dynamic loadlines for a Win GaN on SiC 2 x 125 device under CW and pulse, 10µs pulse length, 10% duty cycle.

Another method of investigating this is to change the bias conditions, so changing the locus of the dynamic loadline.

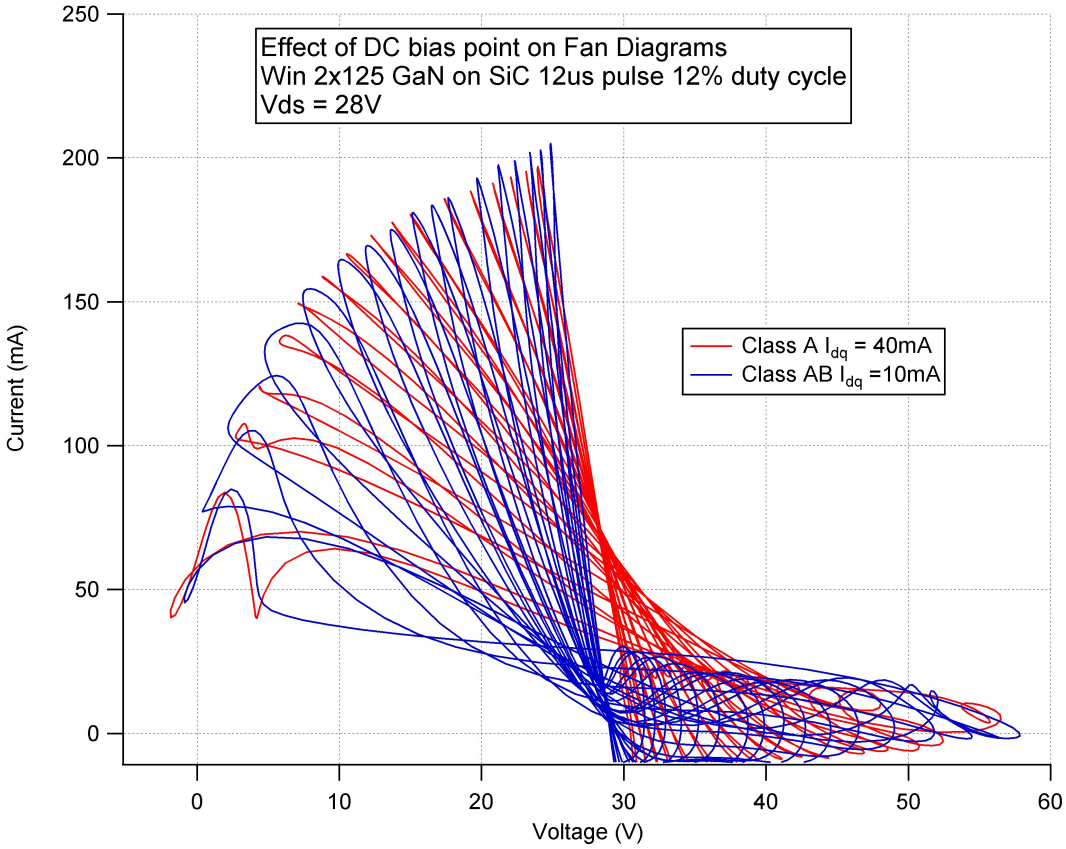

Figure 3.4 The effect of DC bias point on knee walkout for a GaN on SiC FET.

Since the duty cycle of the pulse measurements shown in fig 3.4 is 12%, the die temperature is predominantly determined by the quiescent DC dissipation, 1.12W for the nominally Class A lines against 0.28W for the Class AB lines. Furthermore the area underneath the loadlines in fig. 3.4 represents the heat dissipated during the RF pulses, so we can see that by changing from Class A bias operation to Class AB we have significantly changed the temperature without changing the voltage or current extremes, but the knee walkout is almost unaffected, this graph clearly suggests that the peak RF voltage is the key factor for this device.

3.2 The Influence of 3eV light on trapped charge.

It has been shown before that light can influence trapping behaviour [4], so with this in mind a 3eV solid state laser was obtained and mounted to the wafer probe station with optics to concentrate the output at the wafer probe tips (fig. 3.5).

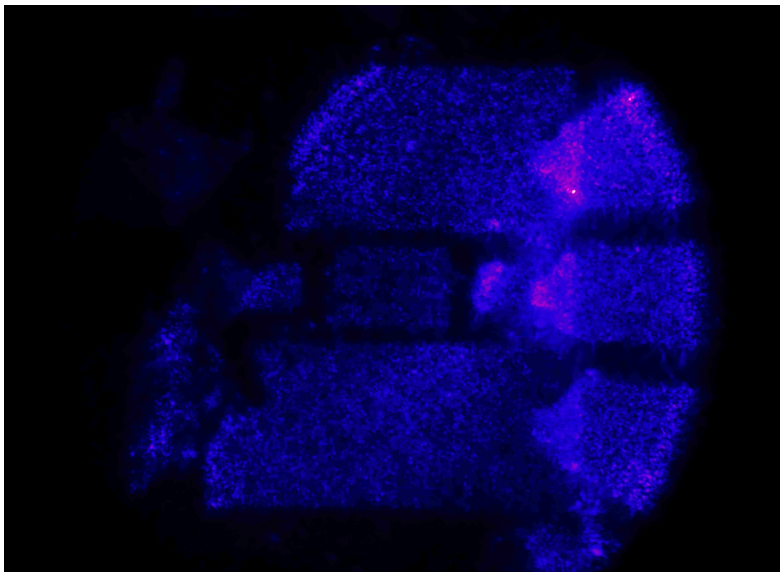

Figure 3.5 A GaN device under 3eV illumination.

To minimise possible direct photo-electric effects it was synchronised to the pulse timing circuits, such that the laser was only on while the RF was off. [9], this was achieved by using an IC intended for driving the gate of large, low frequency MOSFET devices. Applying this light to the Win 2x125 GaN on SiC device studied in Chapter 2 yields the results seen in fig. 3.6

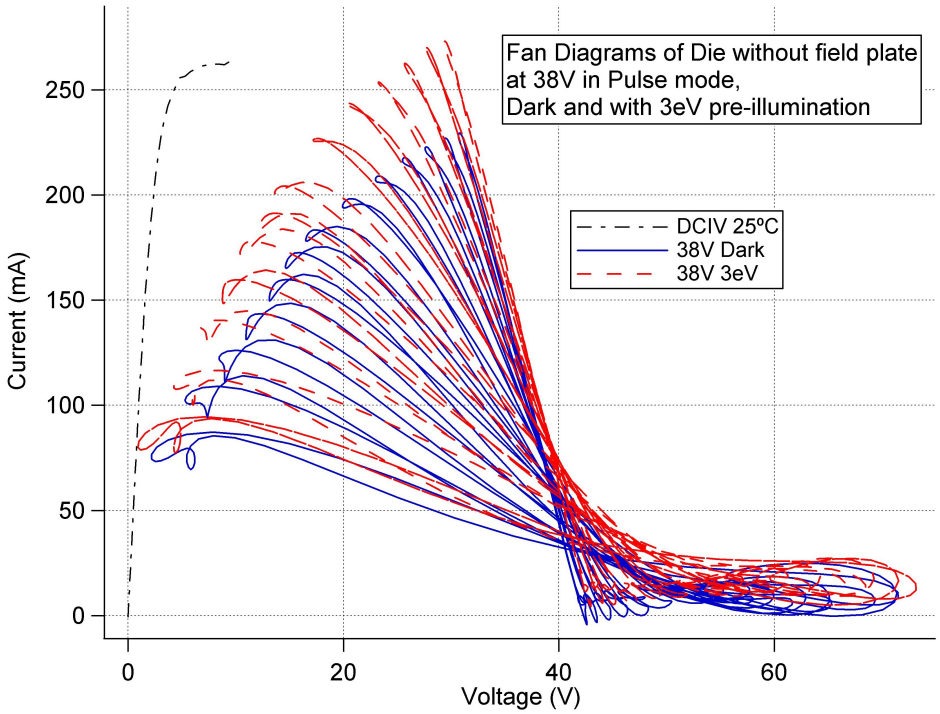

Figure 3.6 The effect of 3eV illumination upon a Win 2x125 GaN on SiC die Pulse length 10µs duty cycle 10%.

While changing between CW and 10% duty cycle had no measurable effect at the shallower lines, the laser produces a marked increase in voltage range at all load values. The low power of the laser being used (20mW) produces a minimal thermal effect, so it is reasonable to assume it is affecting trapping levels within the device.

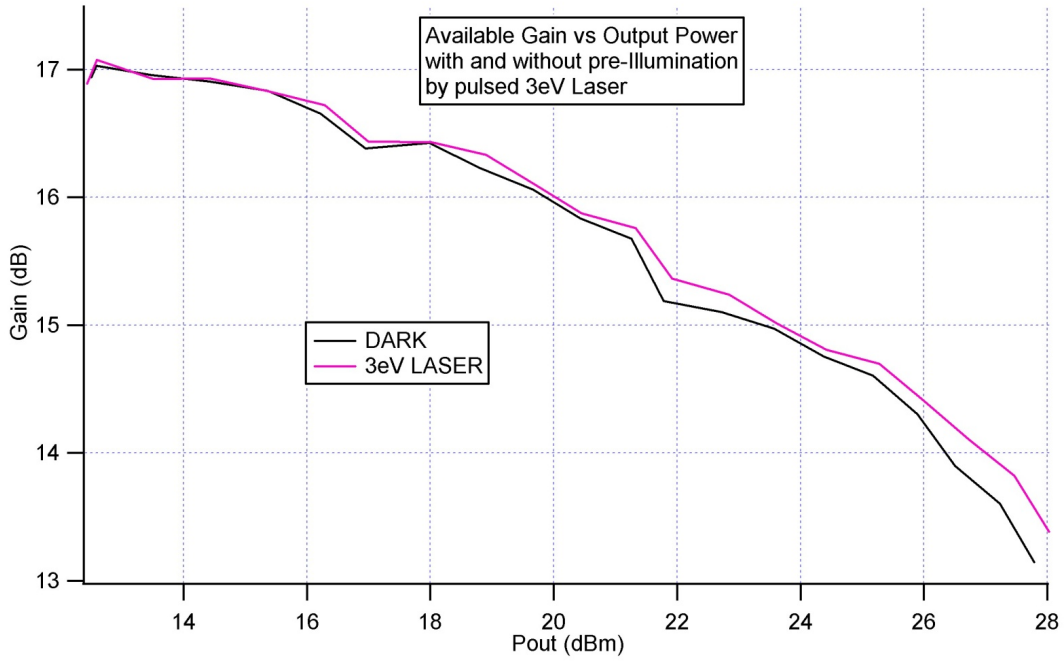

Figure 3.7 Power sweeps without and with 3eV illumination.

To confirm that we are not seeing a change in the general behaviour of the device due to the 3eV light the measurements shown in fig. 3.7 were taken, by measuring the gain against output power with and without the laser they clearly show that the small-signal gain is unaffected. Since the behaviour is only affected as the loadline engages with the knee region we can conclude that the laser improves the performance in this area, which can only be due to releasing trapped charge.

It was observed while adjusting the bias for the RF tests that the DC characteristics were erratic at low drain voltages, very slow DC IV measurements gave the results which are shown in fig 3.8, [8, 9].

Here the gate voltage is held constant at -2V and the drain voltage stepped up and down, the current is allowed to stabilise at each point, this can take 30 seconds. If the device has been subjected to high power RF operation prior to this test then the first time the drain voltage is raised the lowest (blue dotted) curve is followed. If the voltage

is then reduced the higher (green dashed) path is followed. Clearly there is a significant hysteresis. Raising the voltage for a second time the intermediate (red dashed) path is followed. Subsequent excursions will follow the red and green loop, until RF drive is applied, whereupon the lowest blue path will be followed for a single event.

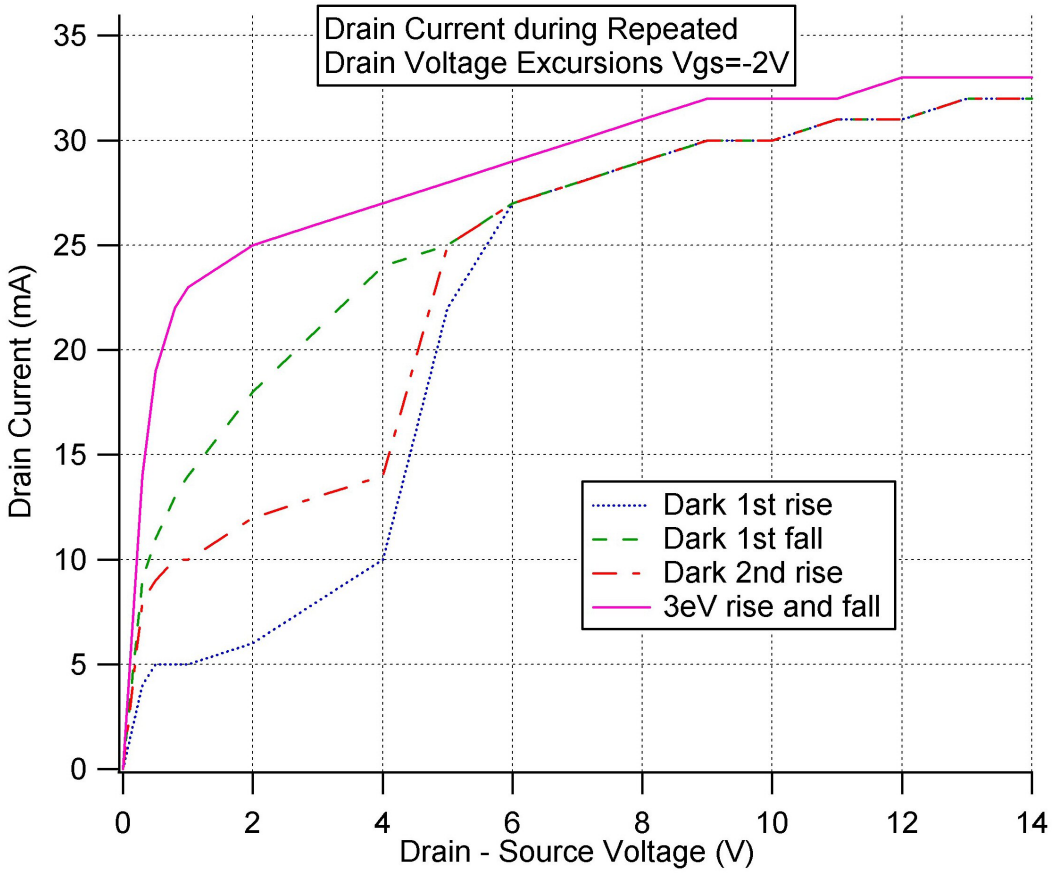

Figure 3.8 DC I-V Hysteresis due to charge trapping.

For this behaviour to be due to a thermal effect would require a higher degree of thermal sensitivity than has been seen, and also a positive temperature coefficient, the opposite of the observed characteristic, a far more likely explanation is charge trapping.

If we apply the laser immediately the characteristic changes, the highest path in fig 3.8 is followed, the response to each drain bias voltage step is immediate, and there is no sign of hysteresis, confirming that this is not thermally related.

As mentioned above, the time taken for the current to stabilise (without the laser) can be considerable, in order to quantify this a DAQ was employed to record the voltages and currents over time rather than taking a snapshot, resulting in the plot shown below in fig 3.9.

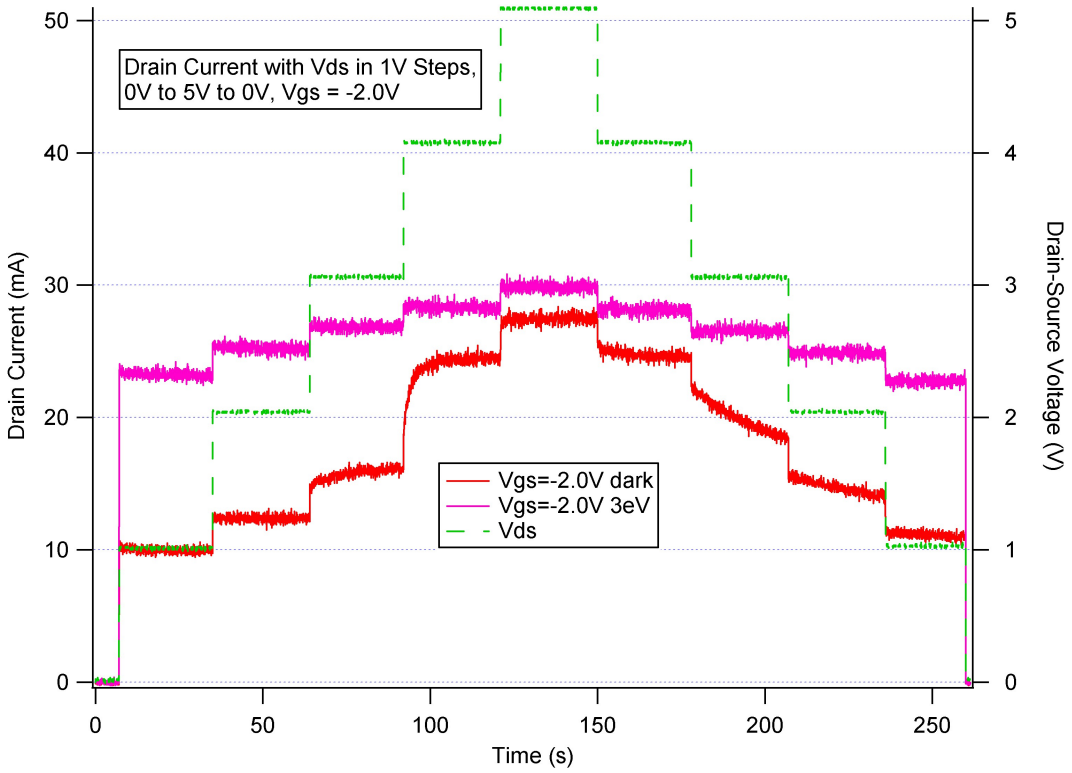

Figure 3.9 Ids stabilisation time at Vgs = -2V.

It is apparent that Ids is strongly dependent upon time, so we would expect considerable non-linearity due to trapped charge memory if we were to operate the device in this region. Once again the 3eV laser has a marked effect, both on the current and the time constant, repeating the test for other gate bias voltages shows the extent of this phenomena, fig 3.10.

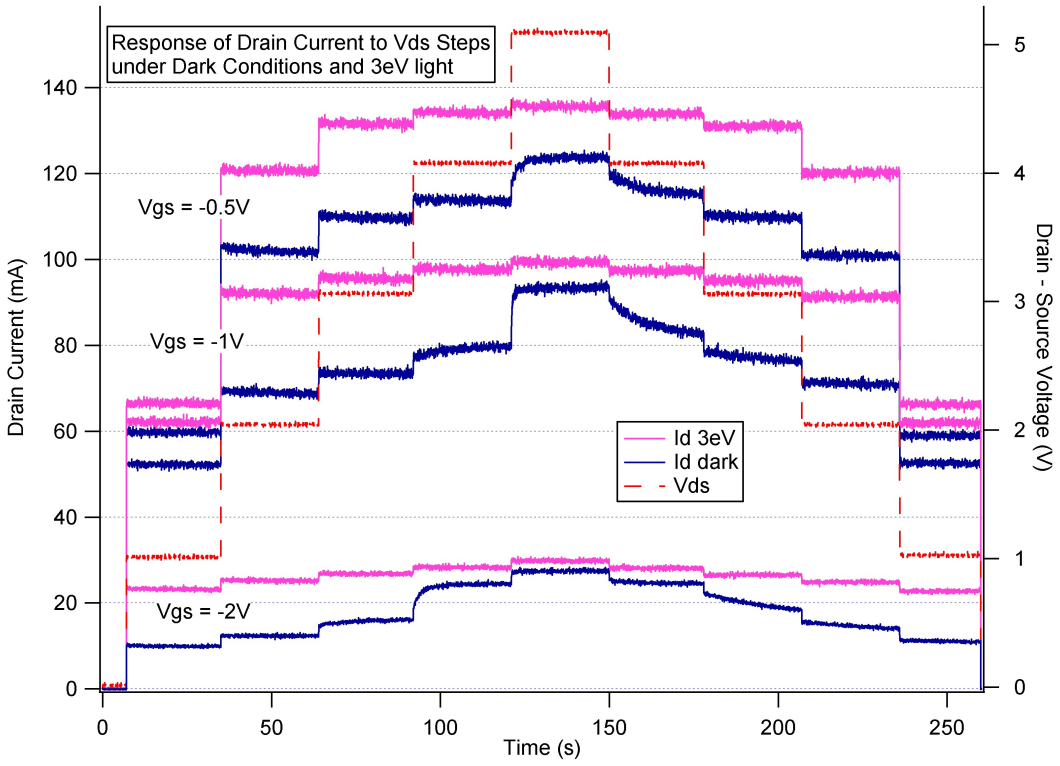

Figure 3.10 Ids stabilisation time at Vgs = -2V, -1V and -0.5V.

It is apparent from the above graphs that the charge trapping is a complex process, from the very low post RF operation initial curve seen in fig 3.8 we must conclude that the high voltages seen in RF operation induce a high level of trapping, yet figs 3.9 and 3.10 clearly show that some traps can fill at low drain voltages (2 to 4V) but start to empty as Vds exceeds 4V. It is likely that we are seeing the effect of different trapping mechanisms.

3.3 Addition of Source Coupled Field Plates.

In view of the accumulated evidence of charge trapping a number of different designs of source coupled field plates were used [7], resulting in the performance seen in fig 3.11. Here we see a dramatic improvement in pulse performance compared to the non-SFP die, and when the laser is activated there is very little difference. It can be concluded that the field plate has minimised the charge trapping which affects the performance of the non-SFP die.

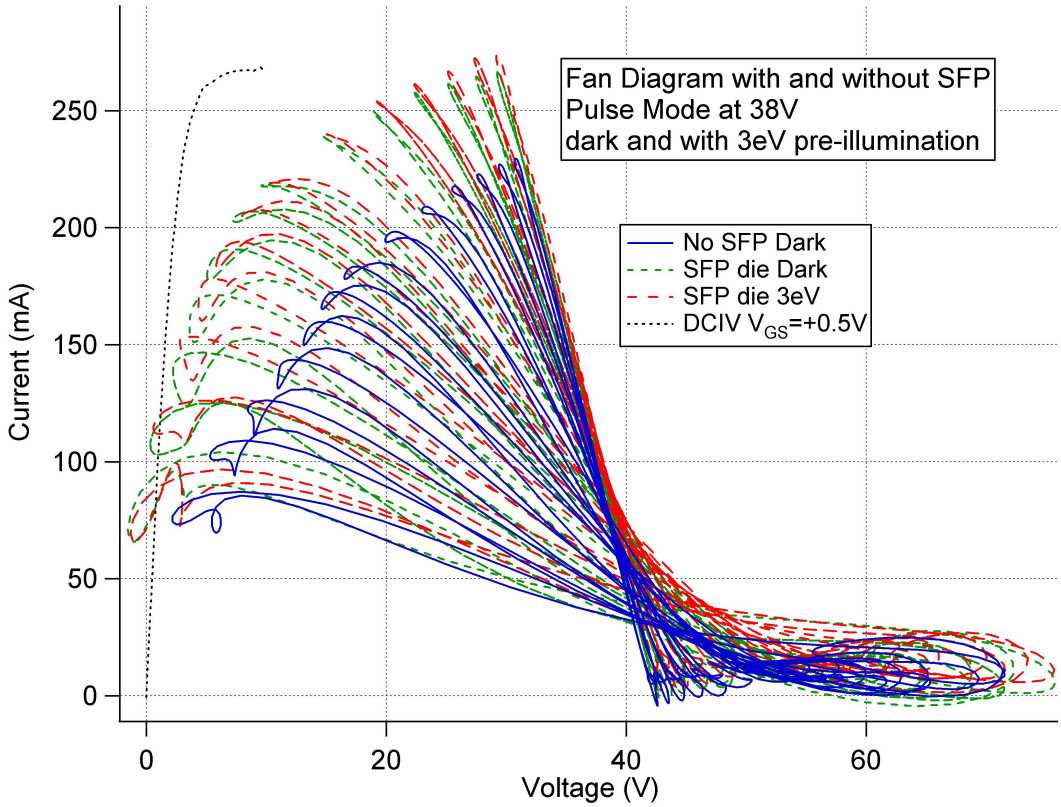

Figure 3.11 Comparison of Win GaN on SiC 2x125 die with and without Source coupled Field Plates (10us 10% pulse).

Figure 3.12 shows a similar test, but comparing the SFP and non-SFP die in CW mode, and also the SFP die in pulse operation. Around the higher impedance lines of the efficient RF operating region there is little difference between pulse and CW operation for the SFP die, moving to the low impedance lines we see the CW performance fall away as the heat dissipation increases. It can be seen that the effect is not as pronounced as for the non-SFP die, presumably the improved efficiency of the SFP die due to the reduced trapping results in a lower operating temperature, and consequently an improvement in thermal behaviour.

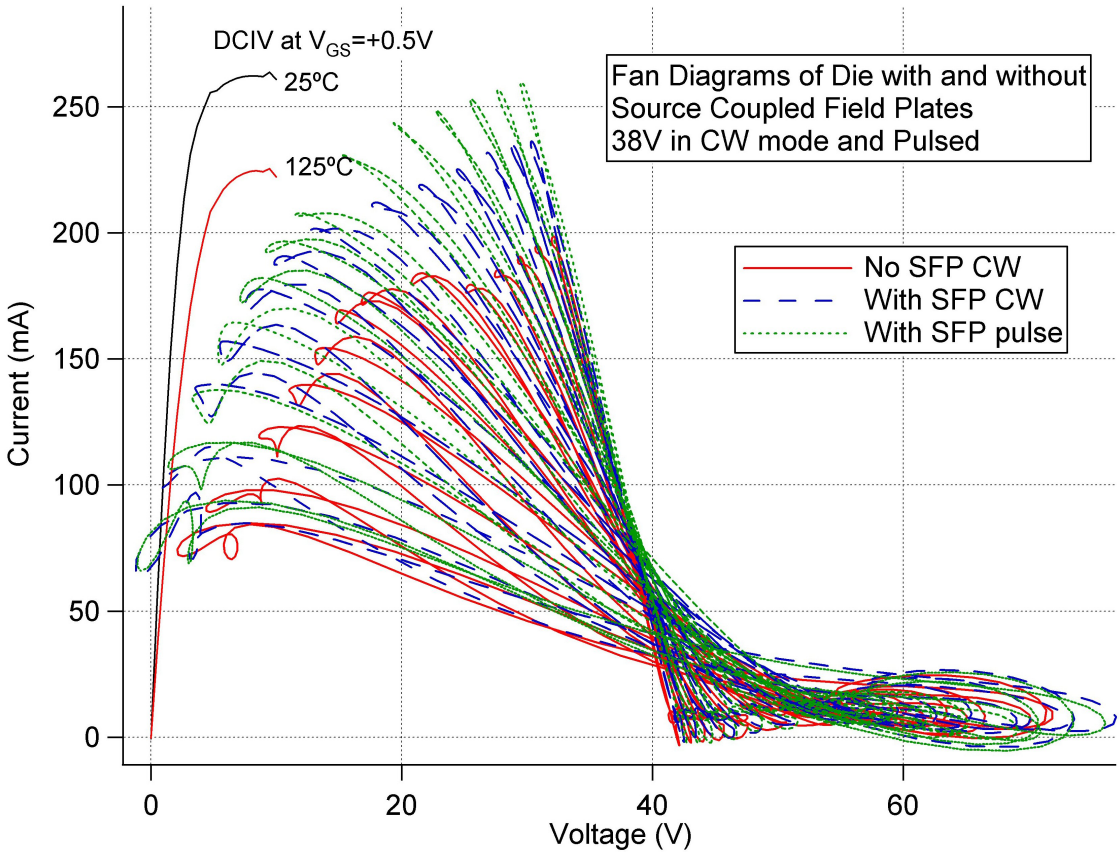

Figure 3.12 Comparison of Win GaN on SiC 2x125 die with and without Source coupled Field Plates (CW & 10µs 10% pulse).

It can be seen that the RF loadlines still fall short of the DC IV lines, even operating in pulse mode, with 3eV pre-illumination and a source coupled field plate, in view of the modest temperature rise estimate made above, it seems this must either be a trapping effect which the laser cannot relieve, possibly of the type discussed in [13] "Buffer Design to Minimise Current Collapse in GaN/AlGaN FETs" (Uren, Möreke and Kuball) or a nano-scale heating phenomena, this is discussed in chapter 5.

The application for these techniques is evidently in the development of new technologies, and they have been successfully applied to a new GaN on silicon process being developed by Glasgow University. With the technology in its infancy dramatic knee walkout was seen even with a modest 10V drain bias, applying the 3eV light restored a great deal of the lost performance (fig. 3.13), clearly indicating the nature of the problem, the first step to a solution.

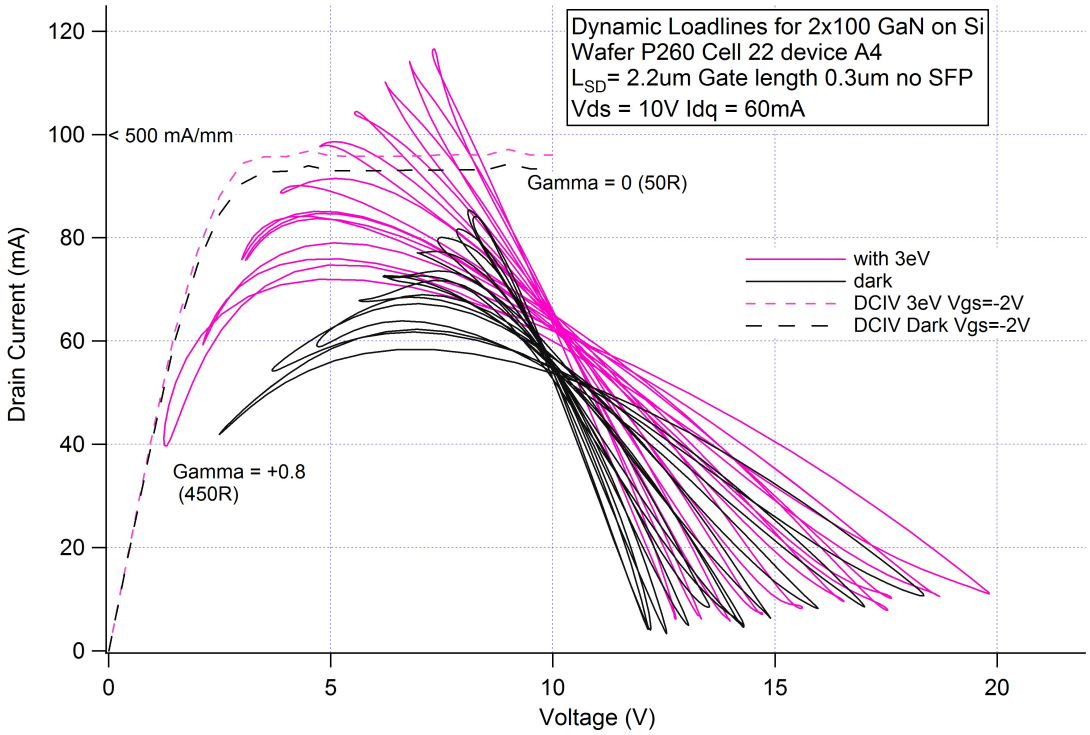

Figure 3.13 Dynamic load-lines for a 2x100 GaN on Si prototype device fabricated by Glasgow University, no SFP, dark and with 3eV illumination.

3.4 The Effect of Intensity and Wavelength.

The wavelength of the laser used in these initial tests was not selected by a rigorous process, it was the shortest wavelength available and was found to work well, clearly a full understanding of the relative sensitivity against wavelength would be helpful; possibly the energy threshold for different types of trap could be identified. Ideally a Tunable Light Source (TLS) could be used to provide a continuous scan across the spectrum, however such an instrument is not currently available to us. As a step towards this goal a range of LEDs was assembled, mounted so as to permit consistent connection to a fibre optic cable, the other end of which could be attached either to a spectrometer or to the Optical/RF wafer probe station described in Chapter 8. Originally developed for Electroluminescence measurements from the underside of the wafer, [27] this novel probe station allows the end of the fibre optic cable to be precisely positioned beneath the device under test, in this instance giving a complete and even illumination to the channel region through the transparent SiC substrate [28].

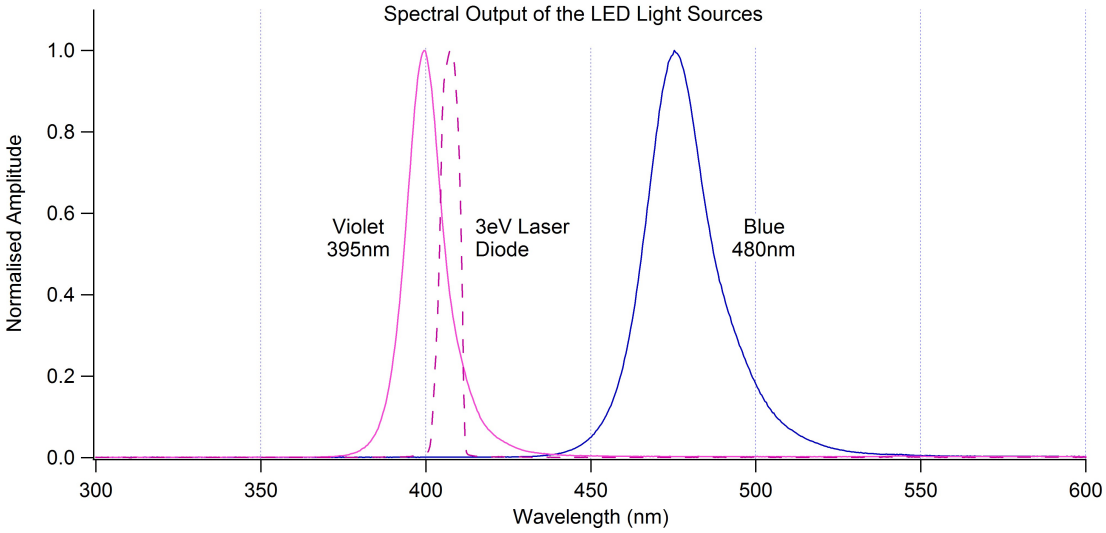

Figure 3.14 The output spectrum of the LEDs and the 3eV laser diode measured with an Oceanoptics Maya 2000 pro spectrometer.

Each LED was attached in turn, and the intensity against LED current characteristic noted for each one by means of an Ocean Optics Maya pro spectrometer. The spectral outputs are shown in fig 3.14, the 3eV Laser diode has a much narrower bandwidth.

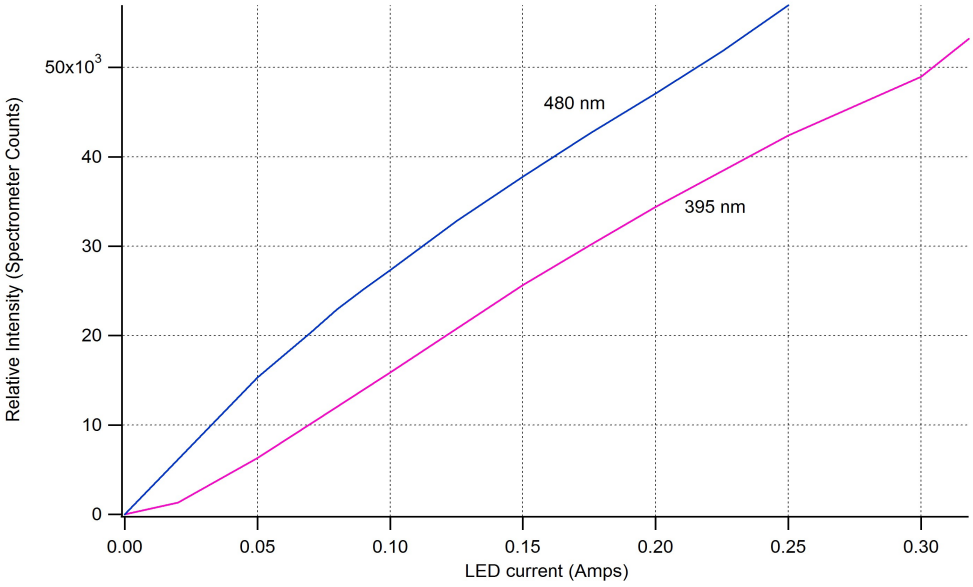

Figure 3.15 Relative intensity against current for 480nm and 395nm LEDs.

With this information (fig. 3.15) saved, the fibre optic can be attached to the wafer probe station and the effect of the different wavelengths compared. It was found that light of 480nm wavelength had very little effect, while light from the next available LED, 395nm, had a pronounced effect (fig. 3.16).

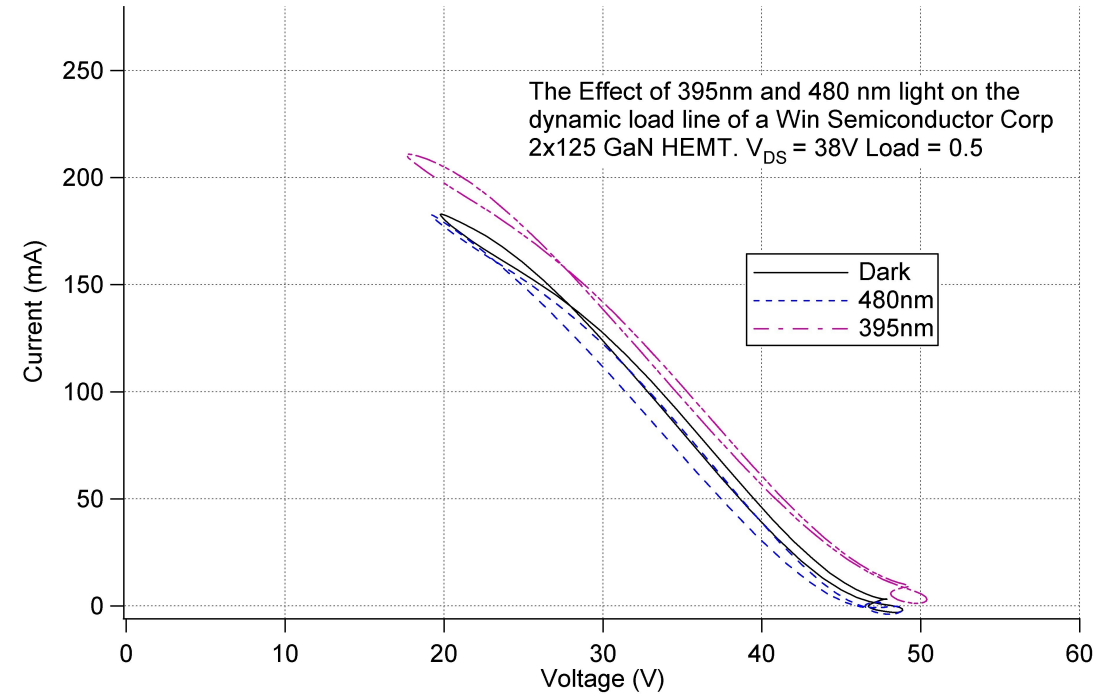

Figure 3.16 The effects of different wavelength light on the DLL of a GaN HEMT.

We can also consider the effect of intensity, plotting the dynamic load lines at different LED currents, shown in fig. 3.17 for the 395 nm LED.

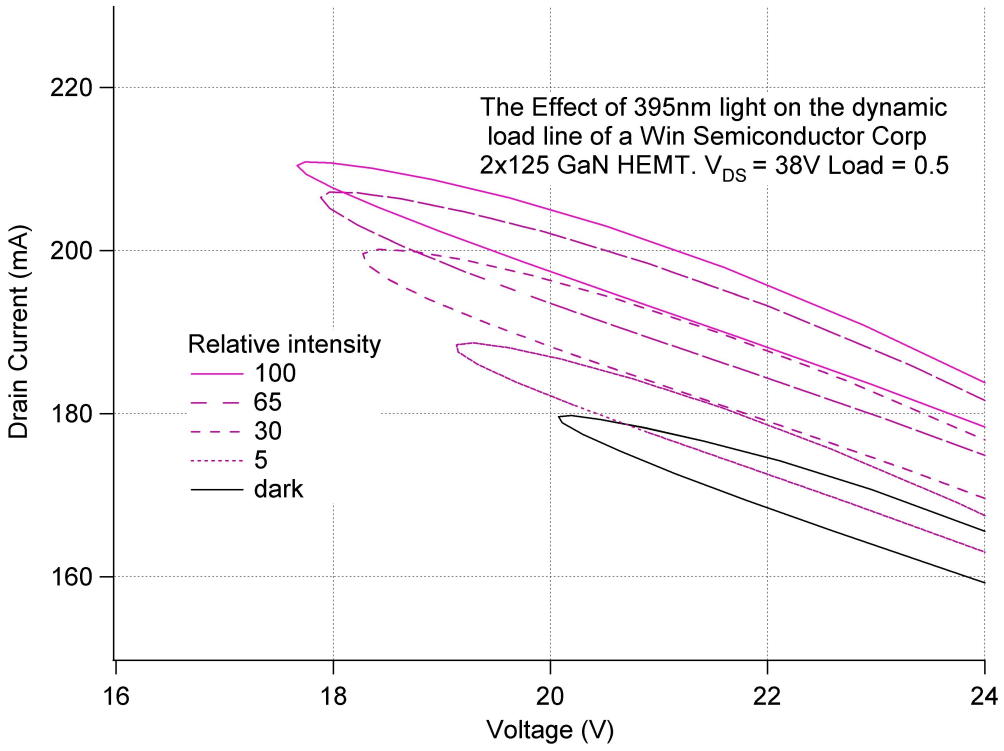

Figure 3.17 The effect of intensity of 395nm illumination on knee walkout.

Clearly the first 5% produces a significant effect, to produce a further effect of similar magnitude requires six times the intensity, and this diminishing return continues as the intensity increases to the maximum available. From this we can conclude that our light sources are powerful enough to release most of the susceptible traps.

It is evident from the load-lines there is still a significant difference between the DCIV curves and the RF performance, it may be more than one type of trap is present, some of them not being susceptible to release by illumination, or possibly requiring higher energy photons, this is considered further in Chapter 5

3.5 Evaluating Trap Filling Times.

If we run the device in CW mode and lengthen the time scale of the pulse controlling the 3eV laser then monitoring the output power with a data-logging power meter reveals the response times.

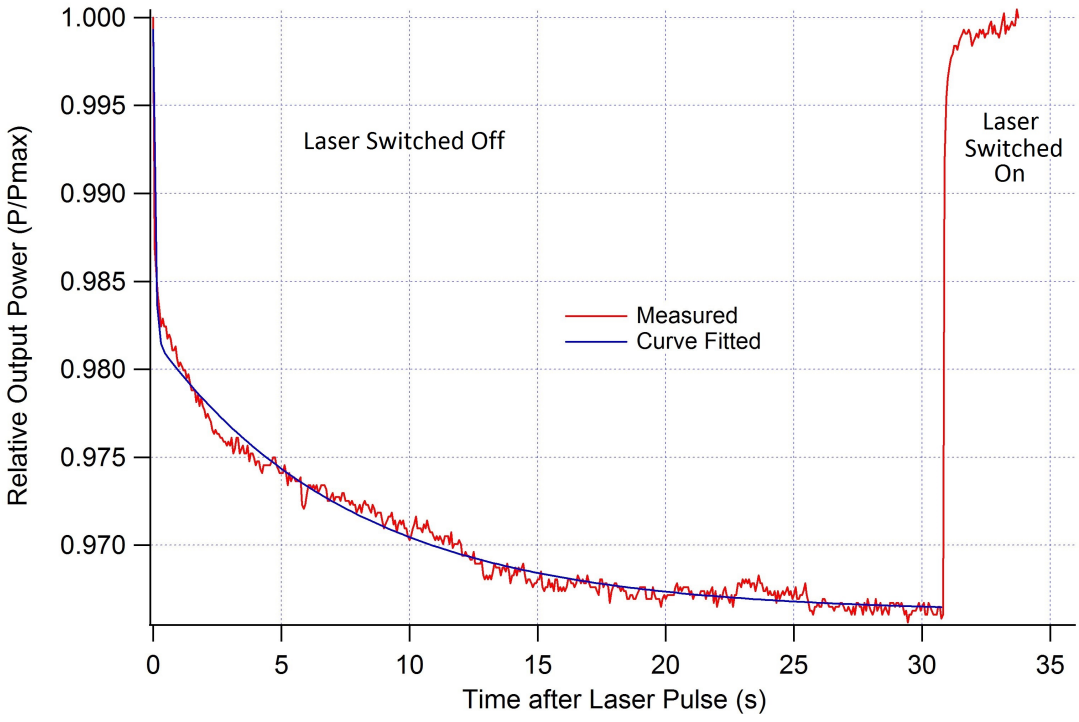

Figure 3.18 Response time of a GaN on SiC die when 3eV laser is removed.

Figure 3.18 shows how the output power takes around 30 seconds to stabilise when the 3eV laser goes off, while the response to it turning on is much faster. The same graph

could in theory be obtained by applying an RF pulse to a device which had been allowed to soak in a quiescent state, however this would probably involve thermal changes too, obscuring the result. The change in thermal load between the two states in this measurement is trivial, and so can be ignored. From this graph the time constants can be extracted, possibly for use in pre-correction algorithms. A double exponential curve fitted line is also shown in fig. 3.18, which gives an acceptable fit, the equation is:

$$\text{Power} = 0.9662 + 0.01751e^{(-13.42t)} + 0.0156e^{(-0.1296t)}$$

There would seem to be at least two mechanisms involved, one very fast and one much slower.

3.6 Conclusions.

It has been shown in this chapter that some instances of knee-walkout are undoubtedly due to charge trapping, and that the charge trapping is predominantly influenced by the peak RF voltage between drain and source (see also Chapter 5, where a method for determining which parameters and which parts of the load line trajectory are responsible for trapping effects is discussed). The potential for using a pulsed 3eV laser to assess the degree of trapping, and consequently the effectiveness of remedial measures, has also been shown. The practical application of this technique is documented in "Development and Control of a 0.25μm Gate Process Module for AlGaN/GaN HEMT Production" Wei-Chou Wang et al, *CS MANTECH Tech.. Dig*., New Orleans, May 13-16, 2013 [7].

It is clear from this work that light can influence trapping behaviour, however, since GaN HEMTs will almost certainly be fitted with a source coupled field plate and air bridges to ground the inner source contacts, it is likely that these will shield some areas of the device from the light, applying the light from underneath minimises these effects.

In order to further the investigation and application of these effects a combined Optical/RF wafer probe station was built, this is discussed in Chapter 8. It incorporates full backside access, a fibre optic coupling and a sub-starlight micro-camera, permitting a wide range of investigations. The fibre optic coupling was originally intended for spectroscopy on electro-luminescence, however it also provides a very suitable method of applying the light for trap release investigations, giving a thorough and uniform

illumination to all regions of the device, and also facilitates quantifying the light level, by means of the spectrometer. Using this equipment it was shown that the wavelength of the light used is significant, at 480nm there was no measureable effect with the devices being measured, whereas at 395nm the effect was marked. [28]

Chapter 4 DC Supply Memory and Multiplexing

4.1 DC supply memory.

As the current drawn from the drain bias DC supply varies the voltage presented to the device will inevitably vary, due both to ohmic resistance and reactive elements in the circuit, unless operating in Class A, with a constant bias current, this may influence the RF performance [19]. The phenomena is a property of the surrounding circuitry rather than the semiconductor device itself, so control of this behaviour is solely in the hands of the system designer, and is really a matter of good supply rail management.

Normally the resistive element of the impedance would be positive, causing the bias voltage to drop as the power peaks, leading to increased compression. In "Linearity improvement in RF Power Amplifier system using integrated auxiliary envelope tracking system" [16] Yusoff et al show that some benefit can be obtained by synthesising a negative source impedance for the drain bias, but the topic is only raised in this work to show how it is minimised in our measurements.

4.2 Bias Tee design.

Cardiff University developed a novel bias tee arrangement utilising a pair of 90° hybrid couplers [12], this has proven to be very effective at decoupling the RF and baseband signals.

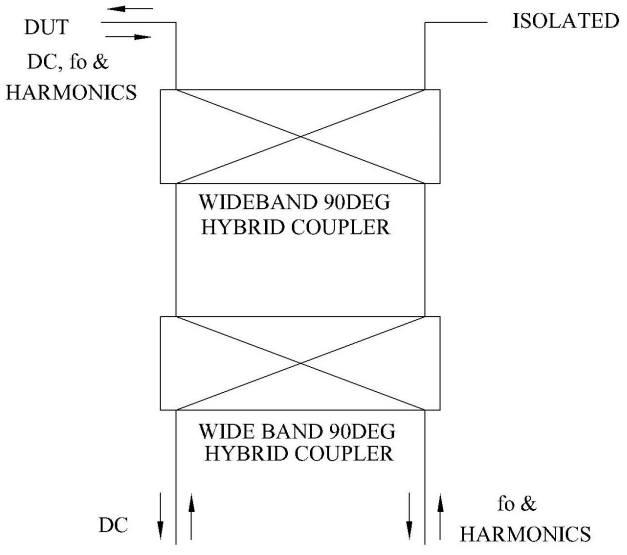

Figure 4.1 The 90° hybrid couple based bias tee.

It exploits the fact that within the operating band of the hybrids RF signals entering a port are split between the two outputs of that coupler, [11] Fig 4.2, and subsequently pass into the second coupler with a phase relationship which causes them to recombine and emerge at the diagonally opposite port of the second coupler, Figs 4.3 & 4.4, whereas there is a DC and baseband path from the fourth port of the second coupler through to the RF input port of the first coupler. A fuller explanation can be found in chapter 4 of "Novel High Frequency PA Design System", J. Benedikt [23].

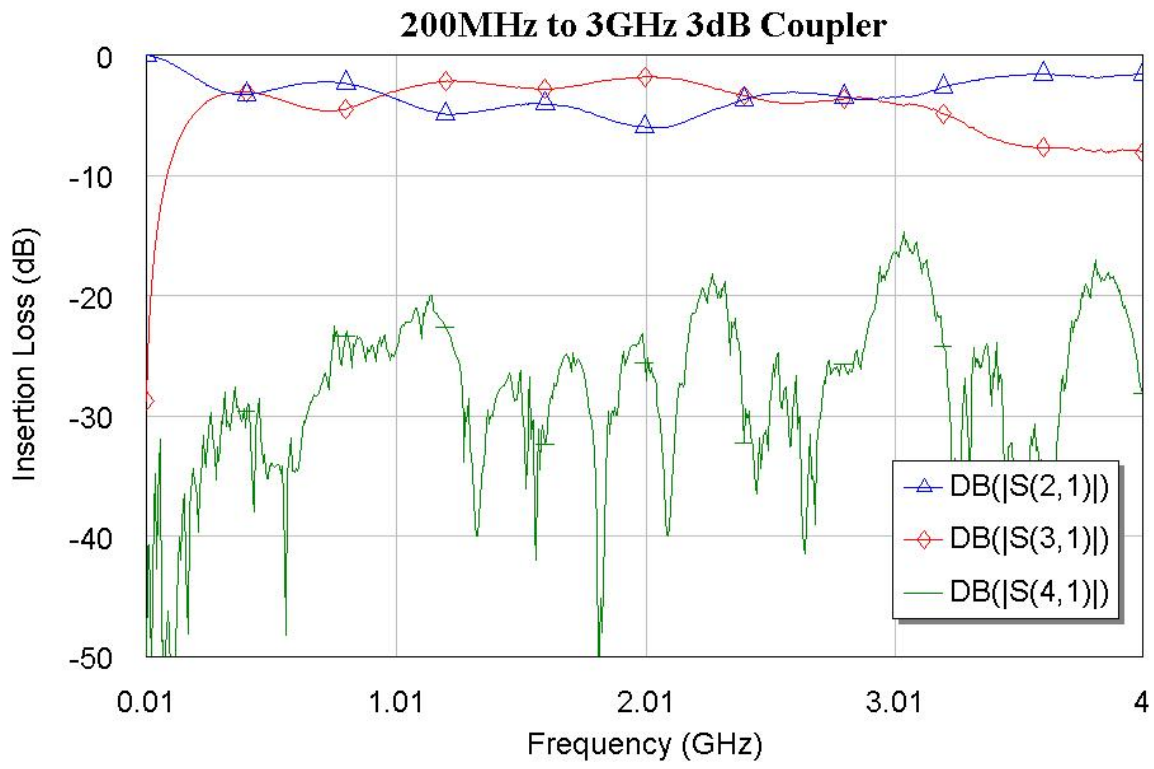

Fig 4.2 The nominal 3dB split and DC path (S_{21}) of a wideband hybrid coupler.

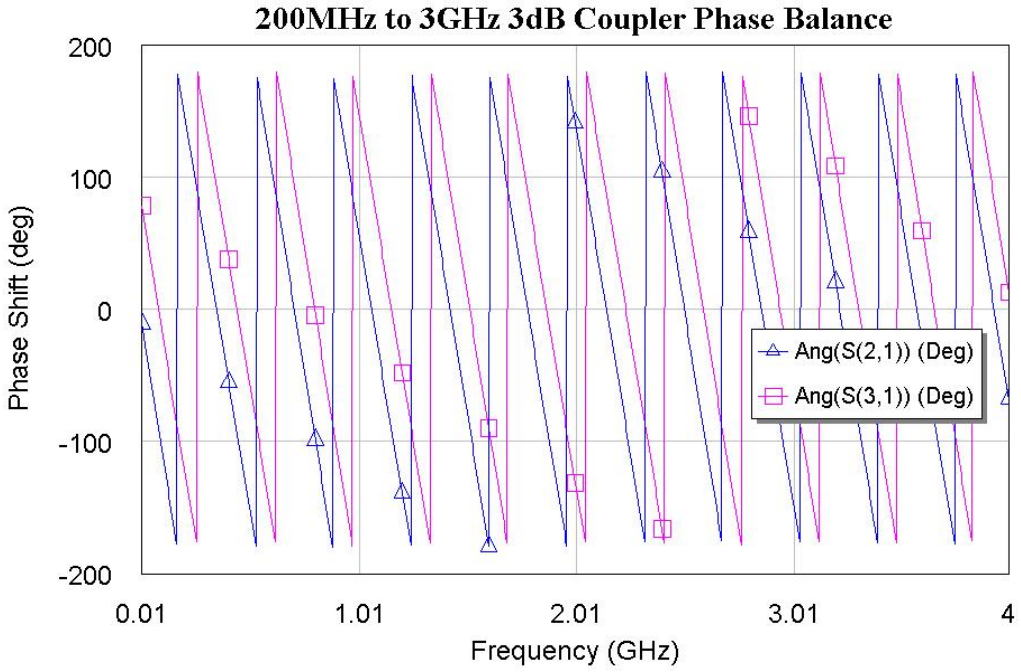

Fig 4.3 The constant phase difference of a 90° hybrid coupler's outputs.

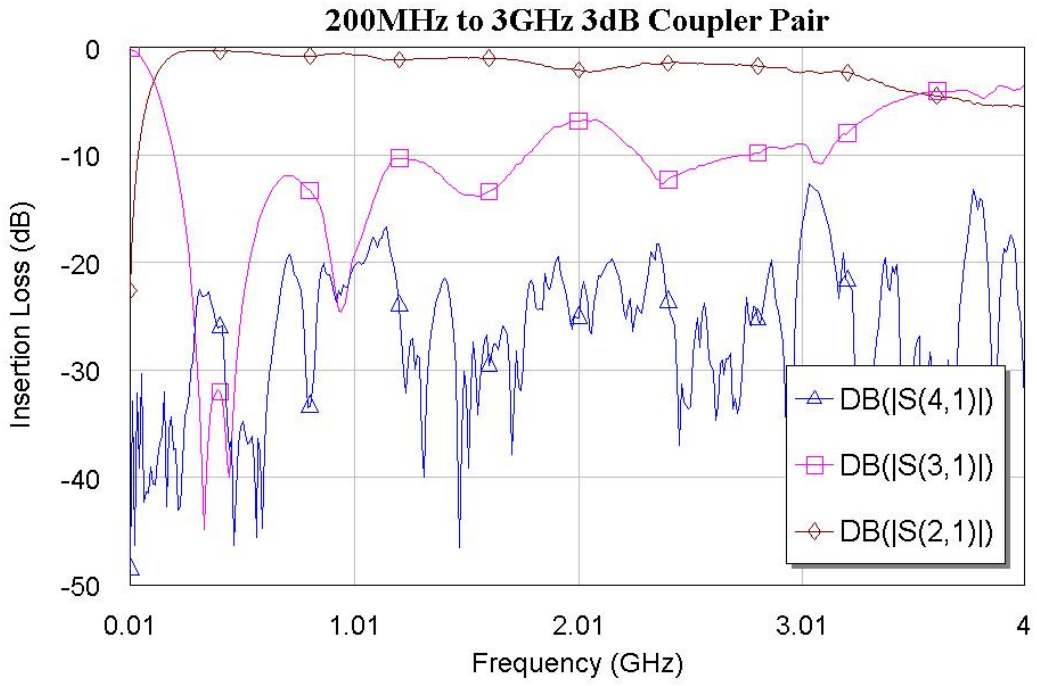

Fig 4.4 The recombining action and DC path (S_{31}) of a pair of hybrid couplers.

The RF conductors through the couplers are typically broad stripline tracks, Fig 4.5, composed of thick high conductivity copper, resulting in a very low DC resistance, and an insignificant inductance at typical baseband frequencies.

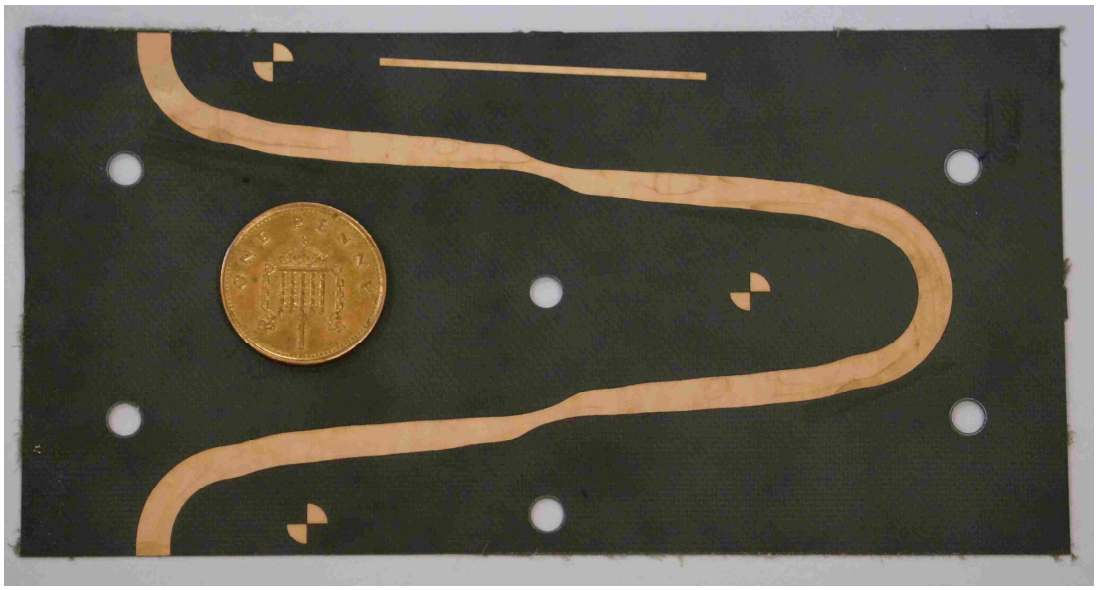

Figure 4.5 The inner conductor of a 1 to 13GHz hybrid coupler realised in stripline.

The non-resonant nature of the frequency splitting provides a very benevolent environment for the device, there are no sharply resonant structures to provoke oscillation, and the series inductance in the DC path is very low, greatly assisting in pulse operation. In practice it has been found that a DC blocked 50 ohm load on the DC port helps to ensure low frequency stability, and some DC measurement equipment benefits from an in-line RF filter, as the isolation of the couplers is imperfect.

4.3 Frequency Diplexers and Multiplexers.

Further development has seen the bias tee incorporated into the frequency diplexer of the load-pull system, where low pass filters are incorporated between the couplers (fig.4.6). The fundamental and DC pass through these filters into the second coupler where they are separated, while all the harmonic signals are reflected back into the first coupler where they emerge from the fourth port.

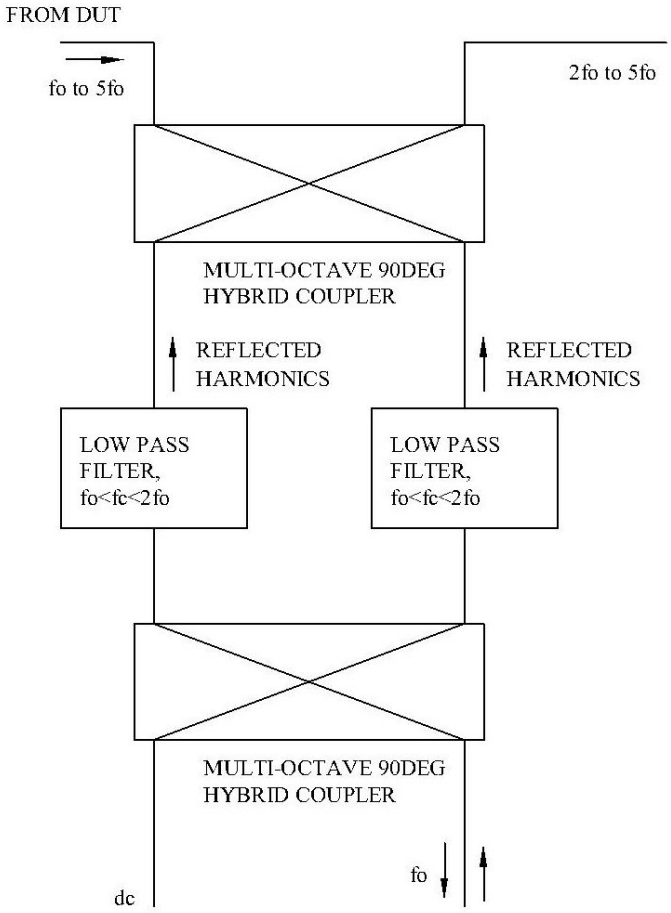

Figure 4.6 A single stage harmonic diplexer, incorporating a DC bias tee.

If further separation of the harmonics is required a second stage is used, with suitably higher frequency filters (fig 4.7). All the active load-pull signals follow the reciprocal path, it should be noted that harmonics above the operating band of the coupler will be reflected back to the DUT. The couplers used for the second stage do not need to include f_0 within their bandwidth, so lower loss, narrower bandwidth parts may be used at this point. The extra circuitry does not impact upon the DC performance, or upon the f_0 load pull power requirements. Harmonics generated by the f_0 load-pull amplifier will be diverted to the DC port, so again care must be taken to ensure these do not affect the DC measurement equipment.

More stages may be added if required but in practice the circuit in fig. 4.7 will allow adequate control over f_0, $2f_0$ and $3f_0$, while the insertion loss through the measurement couplers and the diplexers provides a reasonable termination for the higher harmonics.

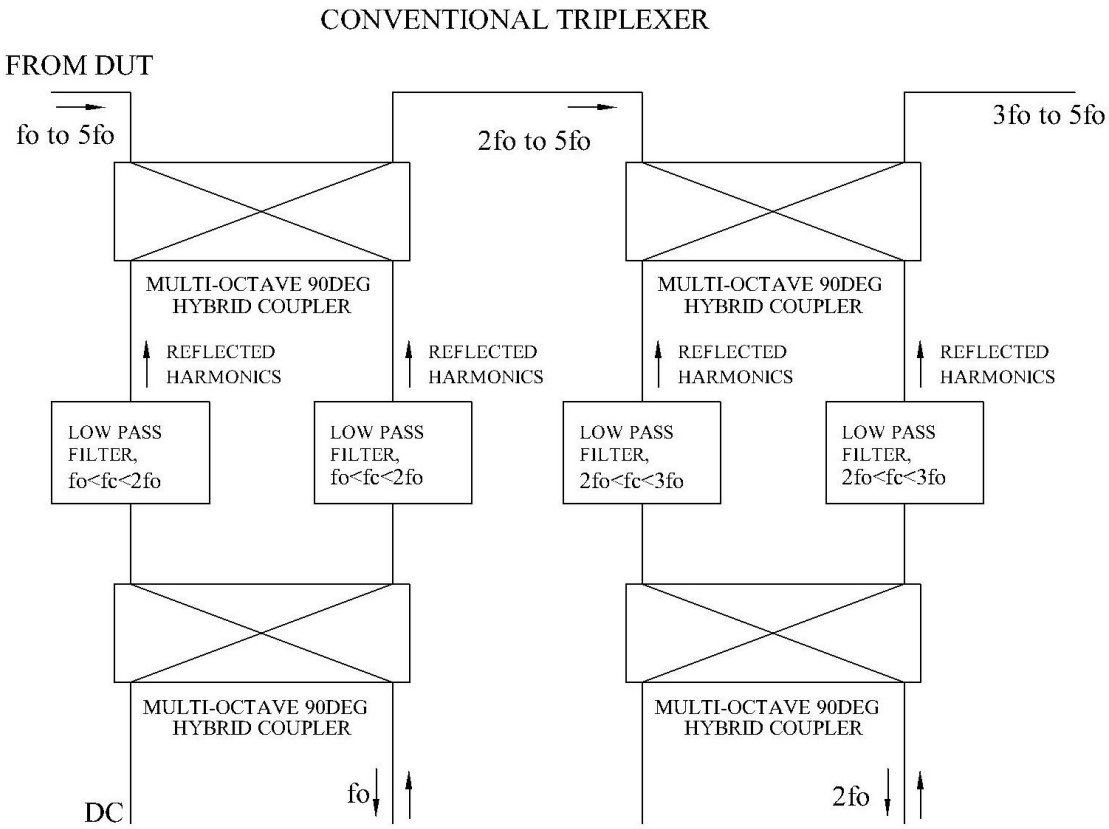

Figure 4.7 A triplexer or multiplexer may be formed by adding a second stage.

4.4 Very Low Loss Diplexers and Multiplexers.

The established circuits shown above work very well for fundamental frequencies up to 18GHz, but beyond this the necessary components, notably coaxial filters, cannot be sourced. Above 18GHz filters are usually realised in waveguide, and consequently do not possess the DC path required for the first stage, fig 4.8 shows a custom manufactured coaxial 20GHz low pass filter and it's inner conductor, clearly illustrating the scale of the problem.

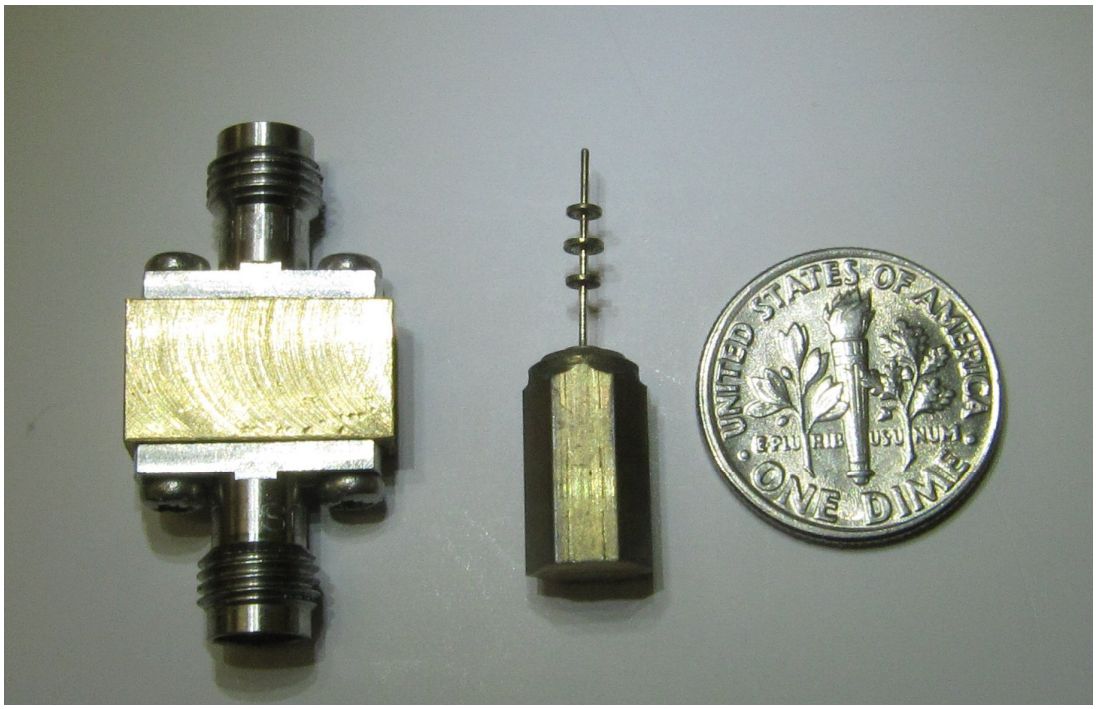

Figure 4.8 A 20GHz low pass filter and its inner conductor.

It would of course be possible to use the simple bias tee shown in fig. 4.1 and follow it by a diplexer or triplexer with waveguide filters, but the wideband couplers needed typically have insertion losses of 1.5dB at such frequencies, so adding an extra pair will double the size of the load pull amplifiers required. Although the test cells likely to be encountered above K band frequencies will be small, the low impedance of their internal capacitances results in probe tip impedances closer to the edge of the Smith chart than might be expected (fig 4.9), especially since it is necessary to pass beyond the optimum operating point to accurately define the contours, so relatively high powers must be injected. If we consider the case of a III-V Labs AlInN/GaN on SiC part with a gate length of 0.15um and a 2x75um structure, loads approaching Γ=0.9 were needed to achieve a maximum output of +26dBm at 30GHz, with a drain bias voltage of 20V and a quiescent drain bias current of 30mA.

From the established equations;

$$P_{OUT} = P^+ - P^-$$

and

$$P^- = |\Gamma|^2 P^+$$

then

$$P^- = |\Gamma|^2 P_{OUT}/(1-|\Gamma|^2) \qquad \text{where } P_{OUT} = 0.4\text{W and } \Gamma = 0.9$$

giving

$$P^- = 0.9^2 \text{ x } 0.4/(1 - 0.9^2) = 1.7\text{W}$$

While the above figure is perfectly reasonable, in order to deliver this to the wafer probe tip the following typical circuit losses must be overcome,

Wafer probe	1.5dB
Connecting cable	0.5dB
Directional Coupler	1.5dB
Bias Tee	3dB
Diplexer	4dB
Circulator	1dB
Total	11.5dB

To deliver 1.7W through this attenuation would require an amplifier power of 24W, not a practical proposition. A similar calculation applies to the second harmonic load pull signal, except that all the loss figures are worse, especially that of the diplexer stage where the signal is reflected from the filters. Although the level required at the probe tip is much lower than that for the fundamental, the power level available from amplifiers at 60GHz is also much lower, so the control of the second harmonic is also impractical using this method.

“Filter-less Diplexer Enables Active Harmonic Load-pull at Ka Band”, M. Casbon, P.J. Tasker, [17] describes how the cyclic behaviour of 3dB couplers was fully exploited to form a compact low-loss diplexer, allowing fully active harmonic loadpull to be

performed at a higher frequency than with previous methods, enabling the full characterisation of the III-V Labs 2x75 AlInN/GaN part considered here.

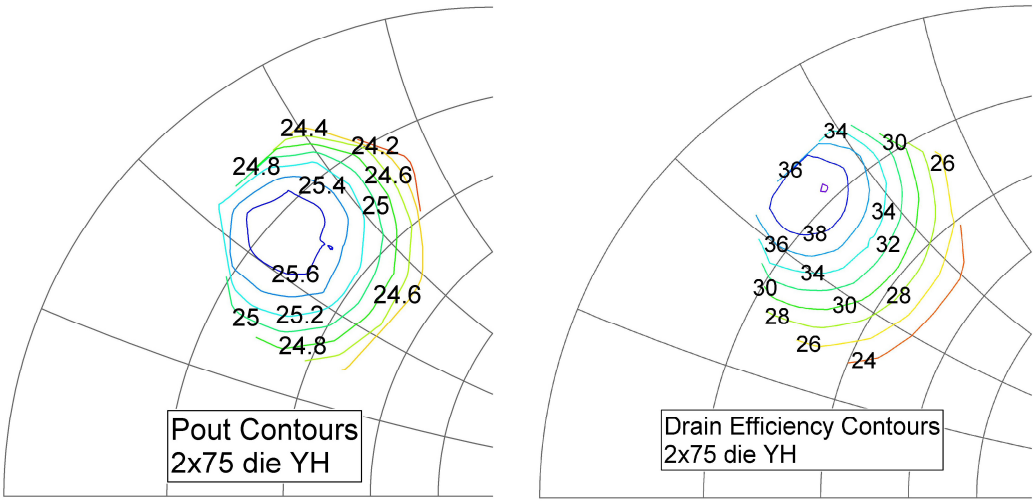

Figure 4.9 Power (dBm) and drain efficiency contours for a III-V Labs 2x75 AlInN/GaN on SiC die at 30GHz.

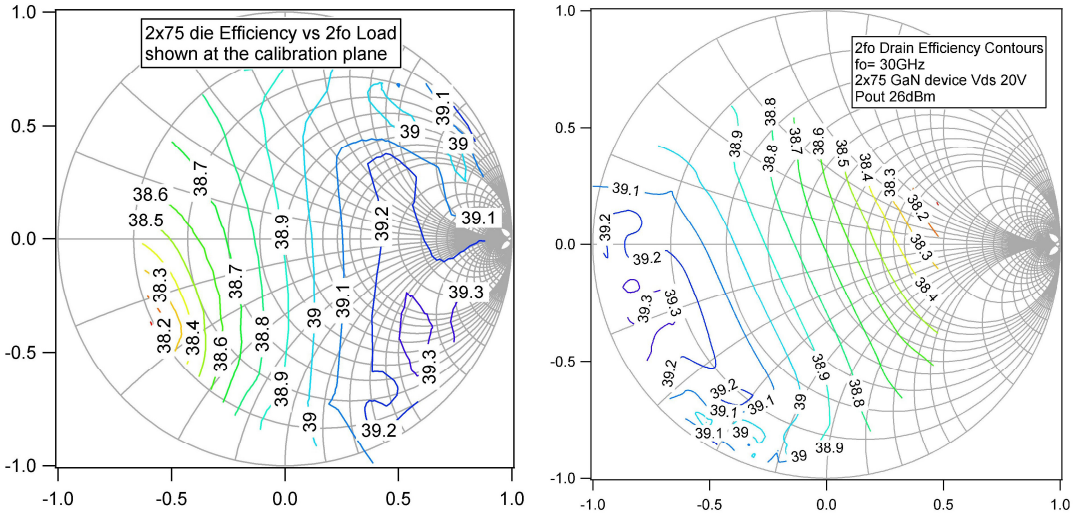

Figure 4.10 Drain efficiency against $2f_0$ load, calibration plane and de-embedded.

Here single section octave bandwidth couplers centred at the measurement fundamental are used, these have much lower insertion loss than the wideband type required for the conventional diplexer. At f_0 the signal from the DUT is split by the first coupler, and recombined by the second coupler, emerging at the diagonally opposite port as before. If we go down in frequency then the coupling falls to zero at DC giving a direct path, as in the bias tee design of fig 4.1. On increasing the frequency until the coupling lines

become a half wavelength long at $2f_0$, the coupling falls nominally to zero (fig 4.11), so the signal passes entirely to the direct DC coupled port of the first coupler, and similarly to the DC coupled port of the second coupler (fig 4.12).

A further bias tee is needed to separate the DC and $2f_0$ signals, but this is only exposed to the much lower power levels present in the even harmonics, and does not feature in the f_0 loss budget.

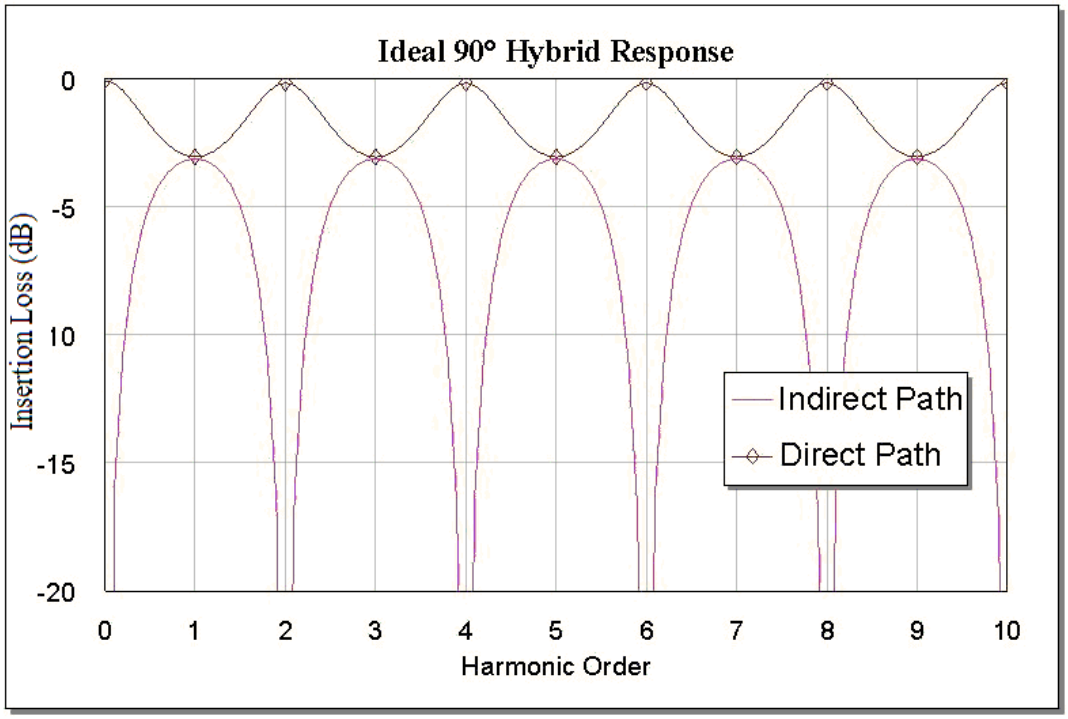

Figure 4.11 The cyclic response of a single ideal λ/4 90° Hybrid coupler.

It is clear from fig. 4.11 above that this behaviour is not limited to f_0 and $2f_0$, if the frequency is increased to $3f_0$ then the coupling is again at a maximum, the signal will be split by the first coupler and recombined by the second, emerging at the diagonally opposite port. It does in fact cycle around as far as the construction of the coupler permits, all the even harmonics appear at the DC coupled port, all of the odd harmonics appear at the diagonal port.

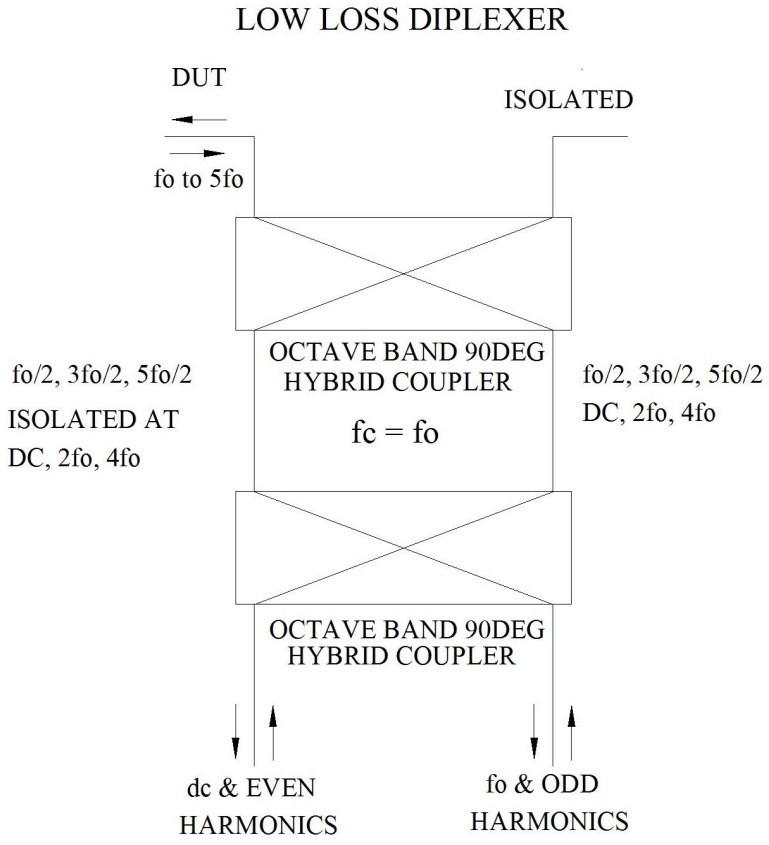

Figure 4.12 The filter-less diplexer design.

The circuit shown in fig 4.12 would ideally result in the performance shown in fig. 4.13 below.

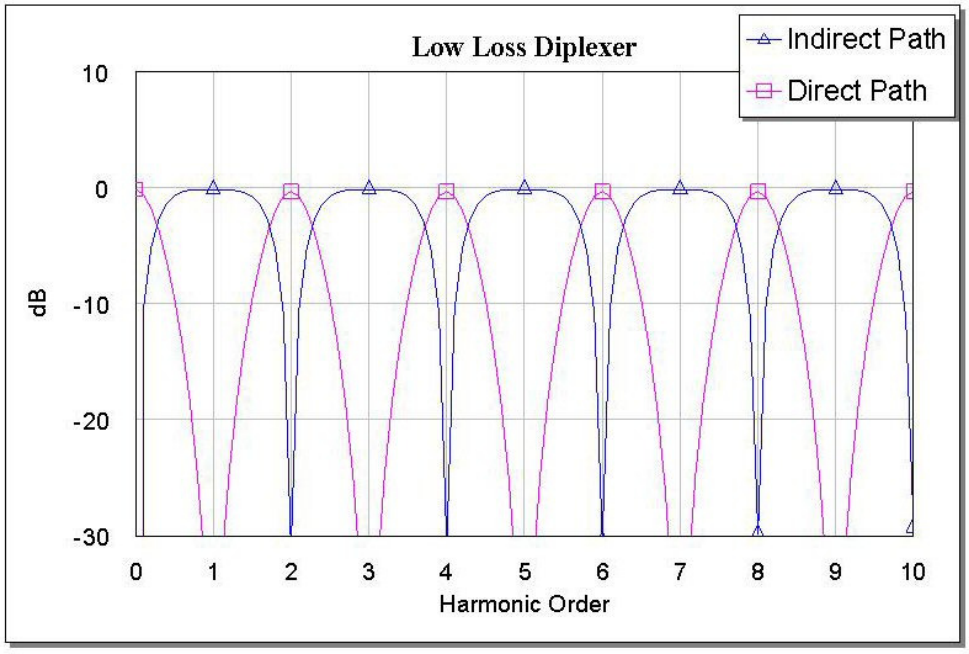

Figure 4.13 The cyclic diplexing response of a pair of ideal λ/4 90° hybrid couplers.

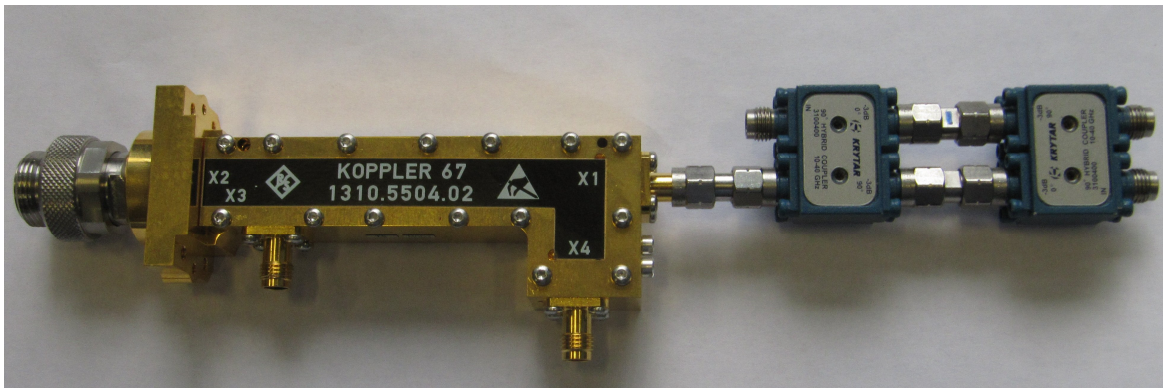

Figure 4.14 A pair of hybrids mounted directly to the directional coupler.

The small size of the components at these high frequencies means that everything except the f_0 load pull amplifier could be mounted directly onto the wafer probe station's positioners, with the barest minimum of connecting cables, further minimising the losses. Together these methods allowed Fully Active Harmonic Load-Pull to be carried out at higher frequencies than had previously been practical, and produced the results described in [15], [17], and reproduced in figs. 4.9 and 4.10 above.

The filter-less diplexer method has also found application at lower frequencies, in circumstances where the very low insertion loss has been critical, such as performing harmonic load-pull with passive tuners. The example shown in fig. 4.15, as well as being much more compact than the wideband coupler and filter version, has an insertion loss of only 0.25 dB at the f_0 frequency of 1GHz, compared to 0.75 dB. Since the signal must pass both ways through the diplexer in a passive system this means the maximum achievable reflection coefficient is 0.94, compared to 0.7 for the filter version, a very significant improvement, especially since the load target for the specific task was 0.74.

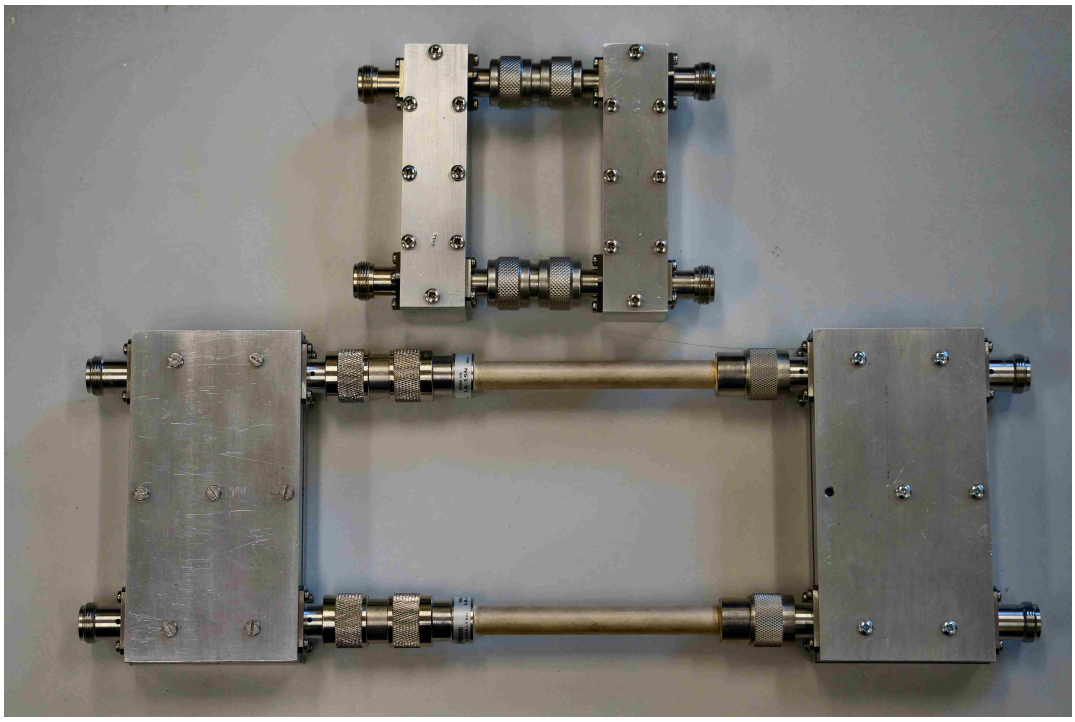

Figure 4.15 A 1GHz “filterless” diplexer, and a conventional filter/wideband hybrid version.

It should be noted that the second harmonic and the DC are not separated by this circuit alone, some type of bias tee is required, but since this can be placed after the diplexer it does not affect the fundamental loss. For the application discussed here a part was made, tailored to give optimum performance at the exact frequency of operation, fig. 4.16, this has a lower loss than the double hybrid design.

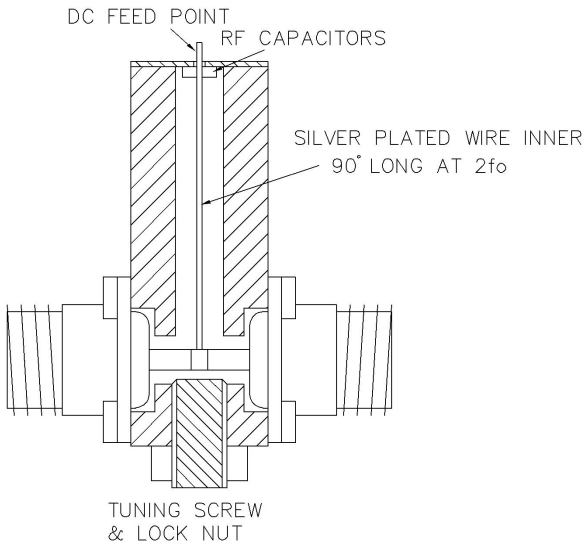

Figure 4.16 Cross section of the low loss λ/4 bias tee.

One end of a simple high impedance line a quarter wavelength long at $2f_0$ was shunted across the RF line, at its opposite end microwave grade ceramic capacitors were used to create an RF short circuit, which was of course transformed to an open circuit at the point of connection to the RF line. Using silver plated wire for the line inner kept loss to a minimum, the DC connection was then made at the RF short. The tuning screw allows the return loss at $2f_0$ to be optimised, and its hole allows a soldering iron to be inserted to join the internal components. The need for a lossy DC block was avoided by terminating the RF line in an adjustable open circuit, realised by sliding a ceramic tube into the open line end. By this method a reflection coefficient of 0.8 was realised at $2f_0$.

It is apparent that the performance of the hybrid couplers outside of their normal working frequency range is critical to the function of these circuits. While octave bandwidth 90º hybrid couplers are available from a number of commercial sources it is difficult to obtain knowledge of their RF behaviour beyond the specified operating band. To ensure the optimum performance was obtained from this circuit Ansoft's HFSS 3D EM simulator was used to design hybrids tailored to suit, ensuring that the $\lambda/2$ frequency was exactly where it was expected to be, and that a good input return loss was maintained at the harmonic frequencies - not a priority for general purpose components. A traditional crossover layout was used, fig. 4.17, and since the conductor strips are relatively short (80mm) they were supported solely at their ends, by the conductors of the N-type RF connectors. Aluminium housings were milled from solid to provide robust mountings for the connectors and form good earth planes surrounding the inner conductors. Precision machining of these housings was relied upon to maintain the correct separation between the inner conductors.

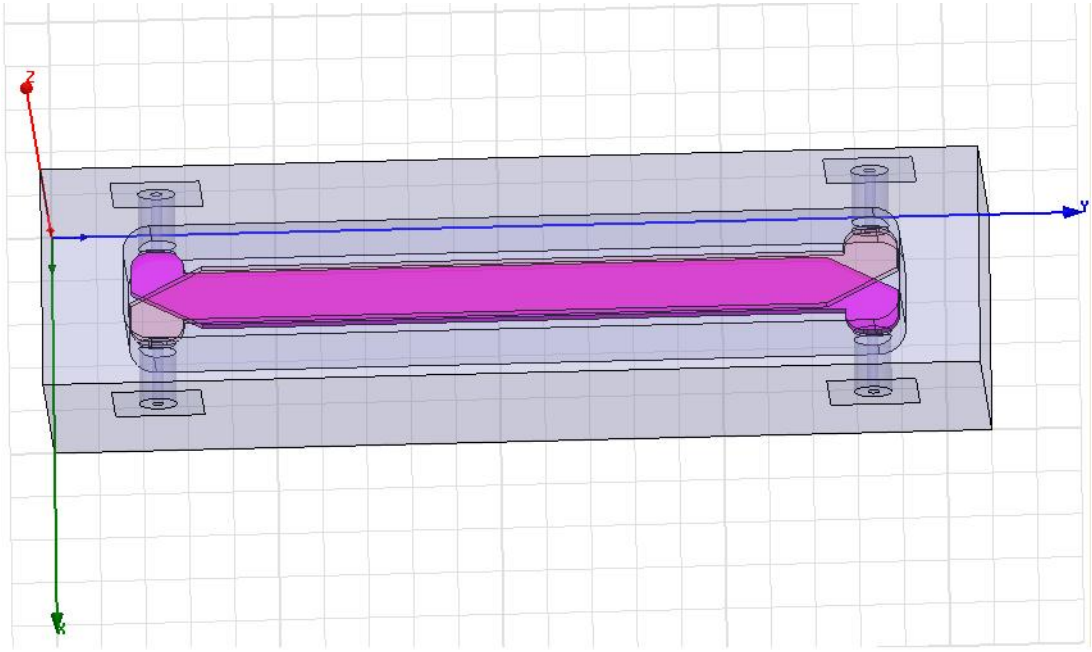

Figure 4.17 Ansoft HFSS 3D EM simulation of the hybrid design.

The inner conductors were formed from 16SWG (1.6mm) high conductivity copper sheet by CNC electrical discharge wire cutting, 1.3mm holes were then drilled in the edges to engage with the pins of the RF connectors, giving a good mechanical support prior to soldering. After machining the inners were cleaned, polished to a mirror finish, and then silver plated to minimise conduction losses.

4.5 A Fully Filter-less Multiplexer and Bias Tee for Active Harmonic Load Pull.

To extend the work above, a fully filter-less multiplexer and bias tee was built to realise a compact, low cost Fully Active Harmonic Load Pull System allowing control of the second and third harmonics.

Splitting the second harmonic, $2f_0$, from the DC bias can be achieved by using a pair of hybrid couplers with a working band which includes the $2f_0$ frequency, these will function as a bias tee as described. To minimise the losses air coupled octave band parts were used, due to the cyclic performance of these parts they will also function effectively at the other even harmonic frequencies, which are passed to this section by the first stage.

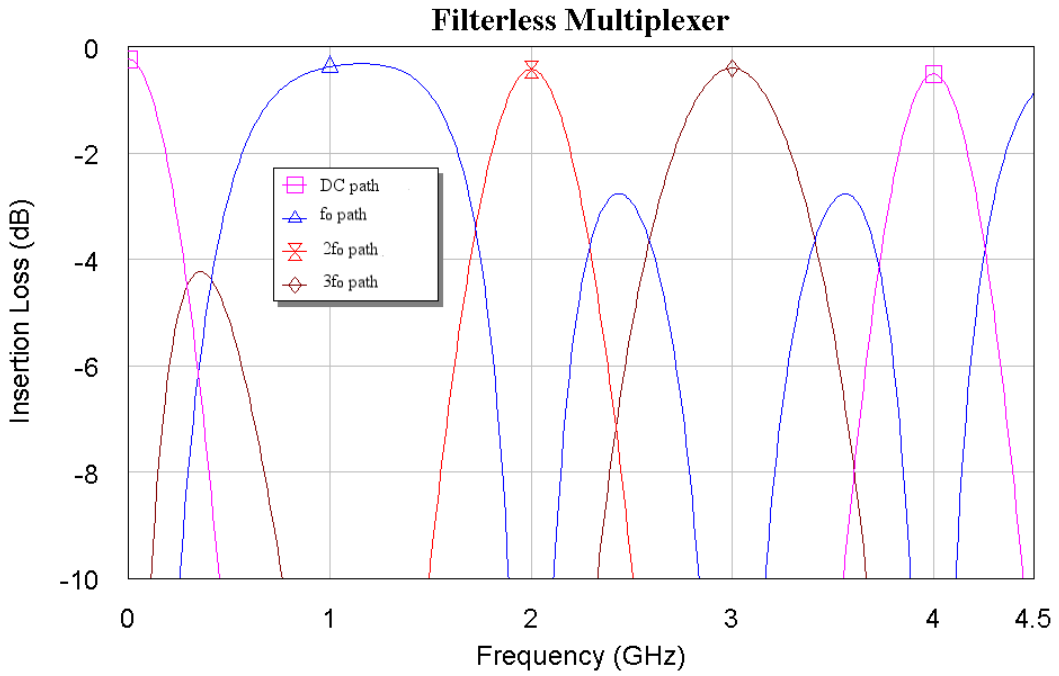

Figure 4.18 Prediction of Filterless Multiplexer Performance.

To separate the fundamental, f_0, from the third harmonic, $3f_0$, we can a use pair of octave band hybrid couplers with a centre frequency, f_c, of $3/2f_0$, the result is that at $3f_0$ the coupled lines will be $\lambda/2$ long and consequently the coupling will have fallen to zero, so $3f_0$ will be passed to the DC port of the second coupler. f_0 however, although not at the band centre, is within the working, octave, bandwidth of these couplers,

therefore it is split and recombined as described above and emerges from the other output of the coupler, as shown in fig. 4.19 below.

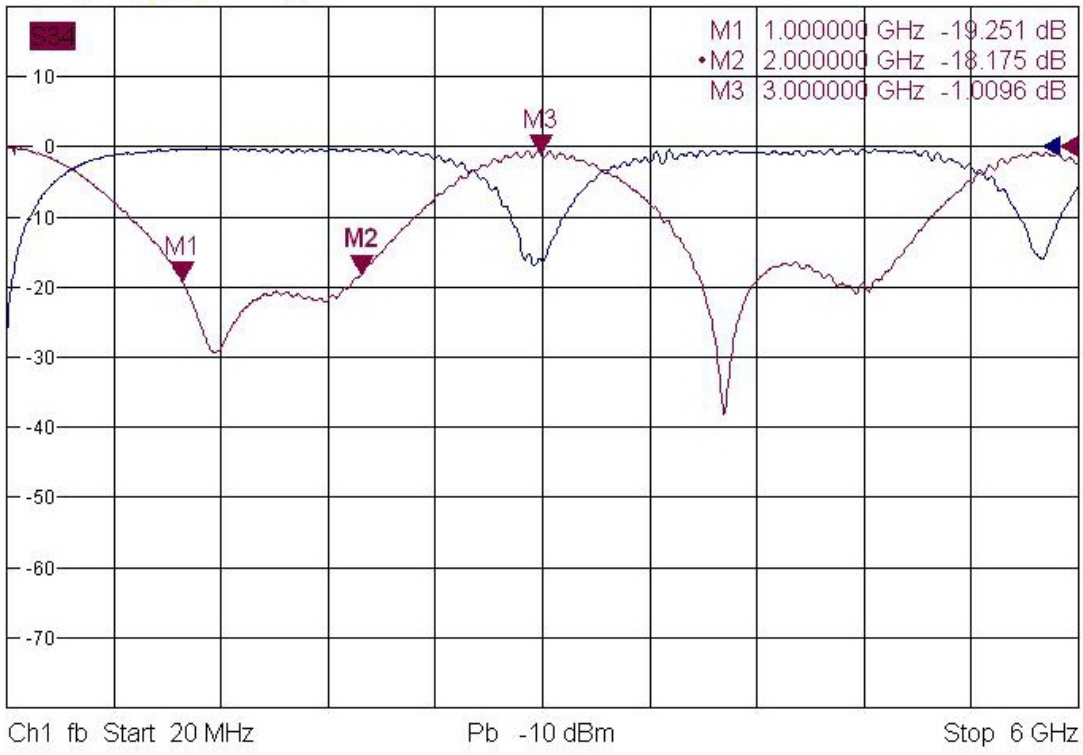

Fig. 4.19 90° Hybrid coupler where f_c = 1.5GHz and f_0 = 1GHz.

Clearly the λ/2 zero coupling frequency and the insertion and return losses are key to the success of this technique, so the parts used here were designed and manufactured using the methods described above, once the cross sections of the lines and the connector feed-outs have been optimised it is a trivial task to scale the line lengths to obtain the desired operating frequency.

In this way we can create a compact five port network (not including the three coupler ports which are terminated in 50 ohm ballast loads), one of which goes to the DUT, and the other four are the DC bias, f_0, $2f_0$, and $3f_0$ connections, using only low loss, non-resonant components. Figure 4.20 shows the final multiplexer, as well as being compact the connections fall in a line, which simplifies the overall setup. A further practical advantage is that the distance from the D.U.T. connection plane to the RF and DC connection plane does not change with frequency, while the filters in the traditional multiplexer, also seen in figure 4.20, become shorter as their cut-off frequency rises, which complicates arranging the parts in a rack system.

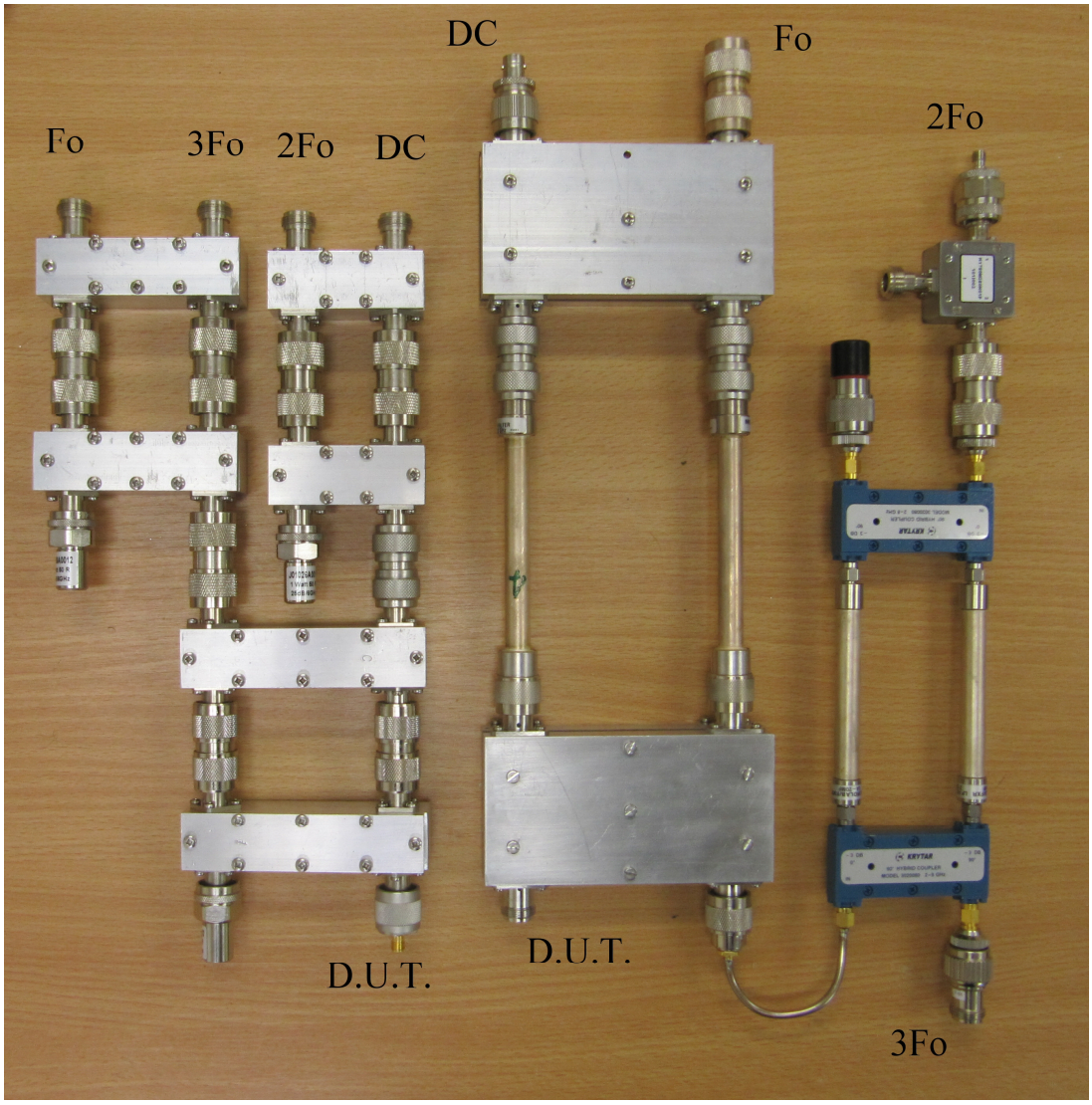

Fig. 4.20 Filterless (left) and traditional multiplexers (right).

In fig. 4.21 below we see the measured results for the filterless multiplexer, which conform well to the prediction seen in fig. 4.18.

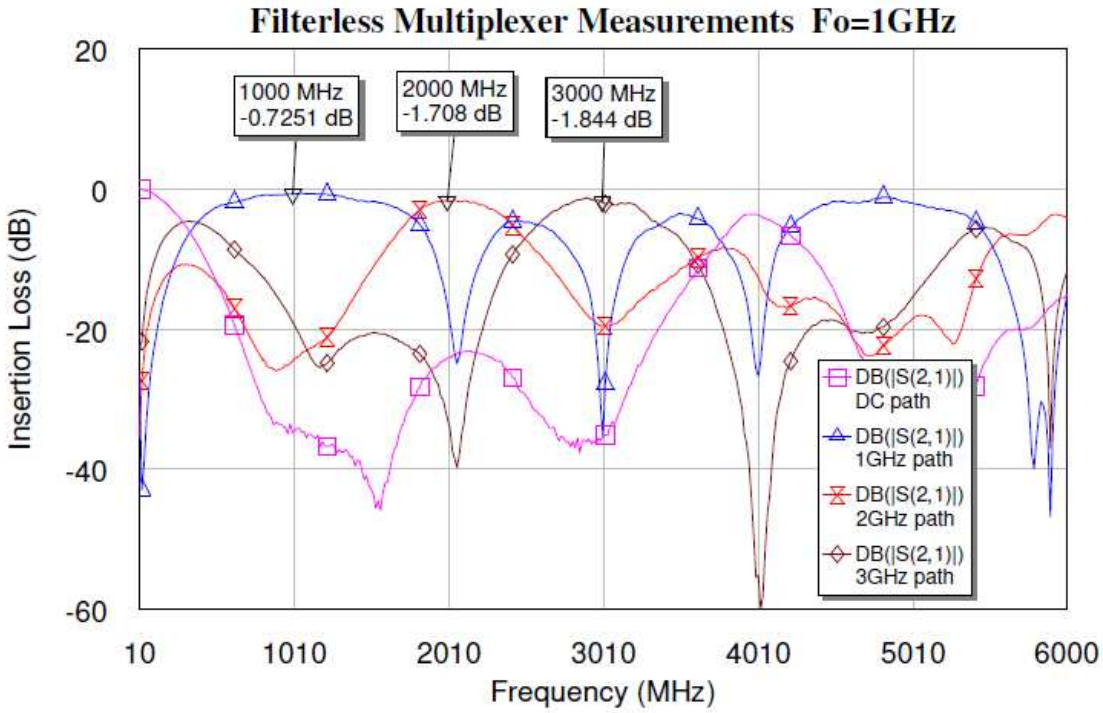

Fig. 4.21 Measured results for the multiplexer shown in Fig. 4.20.

The results shown here are for an assembly using discrete connectorised air-spaced couplers, however it would be quite practical to fabricate a stripline version with all of the couplers formed on a single sheet, resulting in a very compact and economical low loss multiplexer.

4.6 A Ka-V band combined waveguide adaptor, diplexer and bias tee.

While the Ka-V band hybrid diplexer discussed above, and shown in fig. 4.14, worked adequately for the task in hand, with the rapid rate of development in this field devices were soon presented which required load-pull power beyond the limits of the available amplifiers, requiring an even lower loss solution. At these high frequencies (Ka band is 27 to 40GHz and V band 40 to 75GHz) any cable length, connector or interface causes significant loss so the more integration that can be achieved the better.

A higher power 56 to 70GHz amplifier was sourced, the output of which is a WR15 rectangular waveguide, equipped with a transition to a 1.85mm connector, having a loss of 0.5 dB, and requiring a male to male adaptor to connect to the hybrid coupler diplexer. In order to turn this problem into an advantage an integrated solution was designed, performing the tasks of frequency duplexing, DC blocking and bias injection.

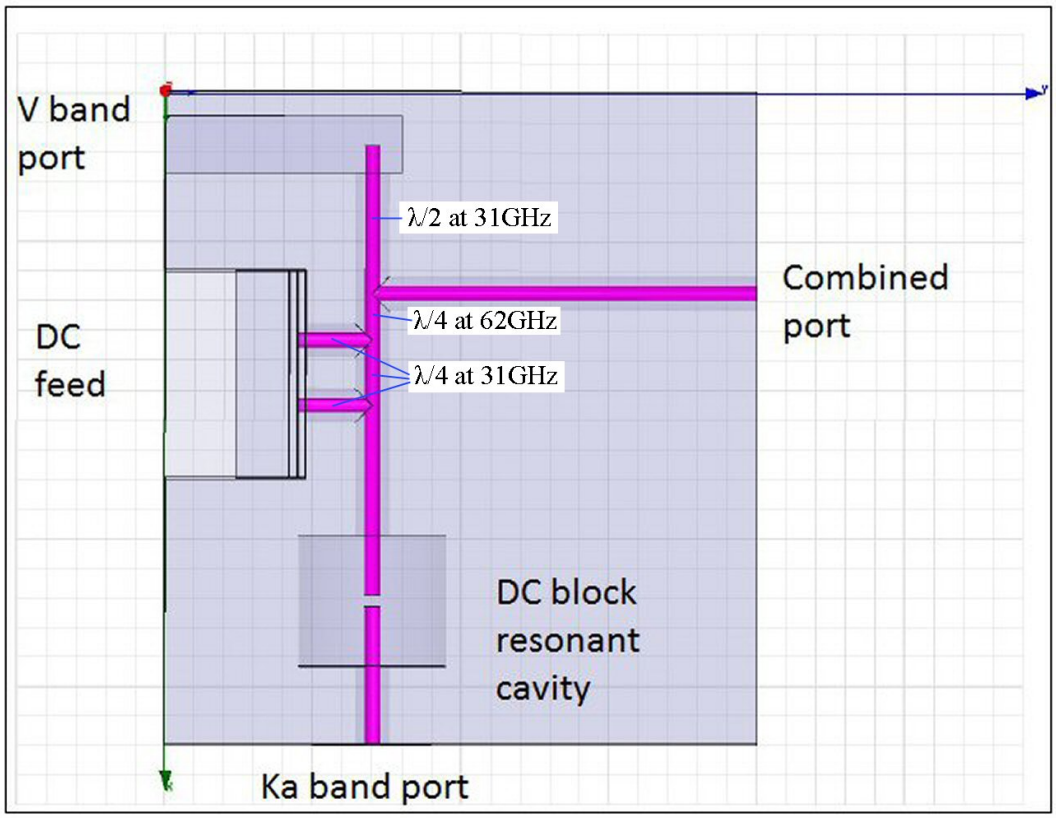

Figure 4.22 Ansoft HFSS 3D EM model of the proposed Ka-V band diplexer.

Extensive use is made of λ/4 lines, which will transform between open and short circuits at the fundamental frequency, but have no effect at their second harmonic. Starting at the combined output connector in fig. 4.22 and working backwards, the inner line comes to a Tee, the upper arm of which extends to become the launch pin of a WR15 waveguide transition, efficiently coupling the V band signal into the 50 Ohm coaxial structure. The distance between the inner Tee and the transition is set to be λ/2 at Ka band, so that the open circuit at the tip of the pin is rotated around back to an approximate open circuit at the Tee junction, so this extension does not unduly influence the fundamental power, and is of course a DC block to the V band amplifier.

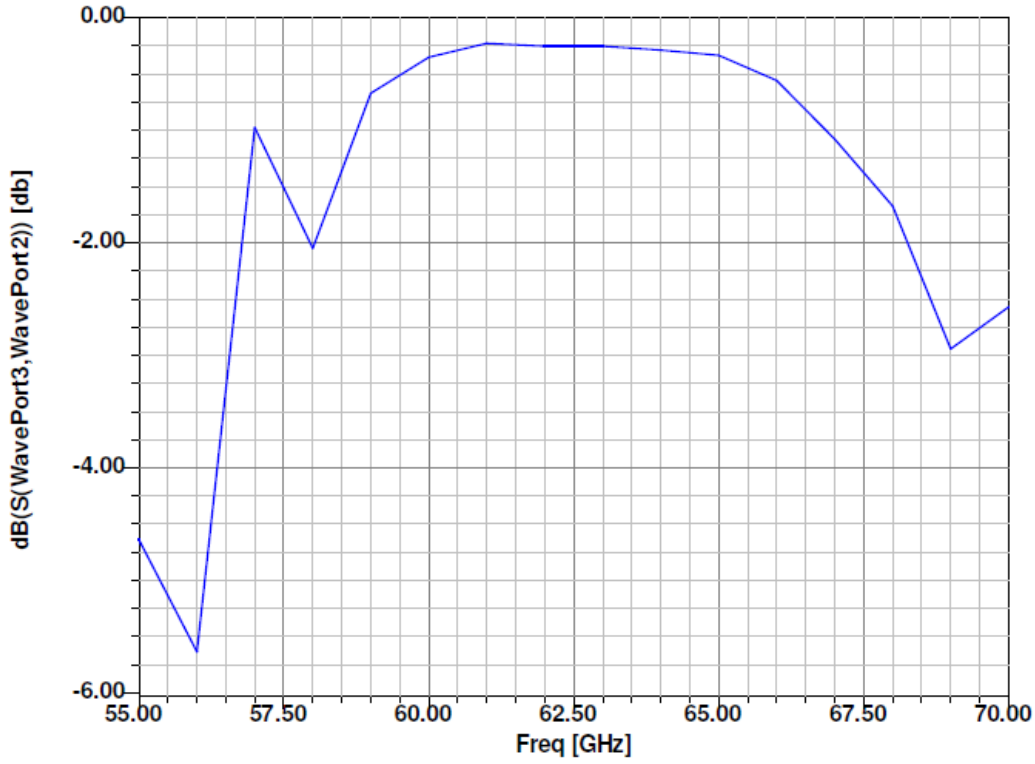

Figure 4.23 Insertion loss from the V band waveguide port to the combined port.

The V band signal must be prevented from travelling down the lower arm away from the output port, and DC must be fed to the inner line, both of these needs are met by the pair of shorted λ/4 (Ka band) stub lines branching off from the lower Tee arm. The short circuits are formed by RF duroid capacitors supplemented by lumped components, creating an RF free terminal for attaching the DC bias feed, and at the fundamental they are transformed to open circuits at their junctions with the main inner line, allowing the Ka band fundamental waves to pass unimpeded. The spacing between the lines is also λ/4 (Ka), so that any slight mismatch wave reflected from the first stub will tend to be cancelled out by the similar wave coming from the second stub, improving the match at the fundamental and so widening the usable bandwidth.

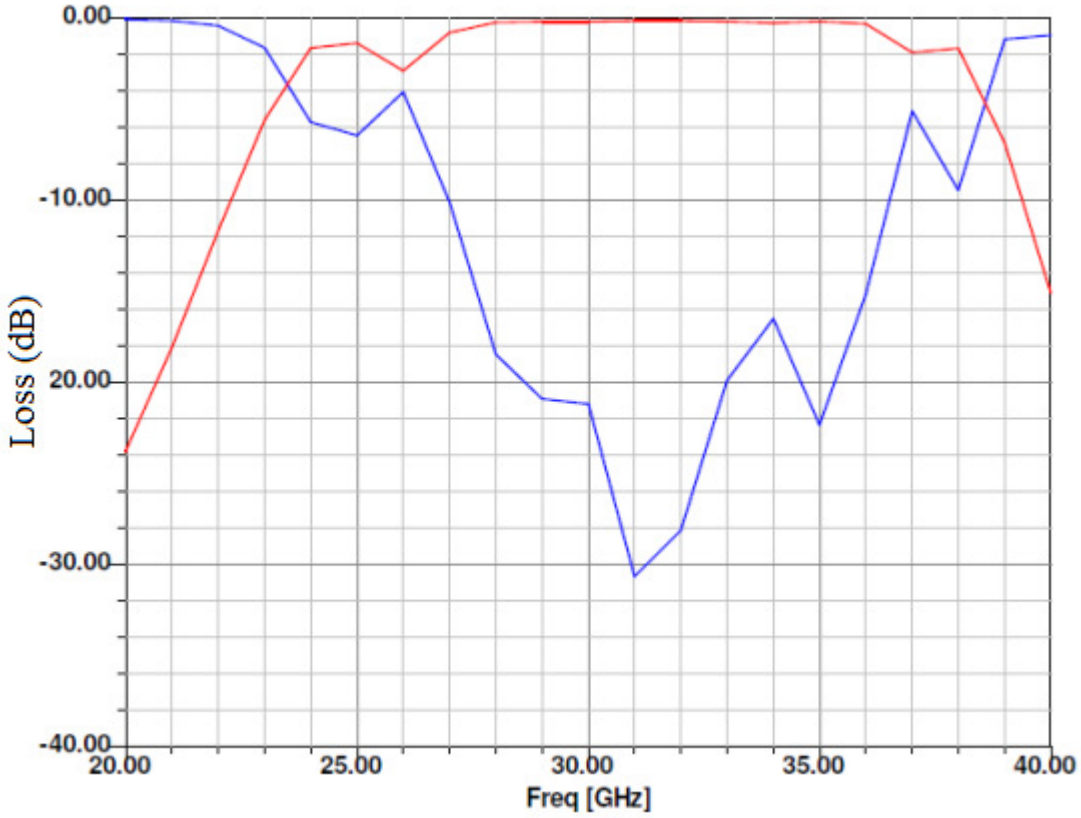

Figure 4.24 Ka band insertion loss (red) and return loss (blue) modelled in HFSS.

For the second harmonic V band signals the situation is reversed, the stub lines have become approximately λ/2, and so present short circuits across the main inner line, reflecting the V band signals back towards the output Tee junction. The distance from the output Tee to the first stub line is set as λ/4 at V band, so that the short of the stub appears as an open circuit at the Tee, so the V band energy from the second harmonic amplifier is all directed to the output connector. The electrical distance between the stub lines is λ/2 at V band, so energy which leaks past the first and is reflected by the second will reinforce the reflection from the first, reducing the loss away from the band centre.

The structure so far will efficiently direct energy in the upper region of V band (55 – 67GHz) from the waveguide port to the output port, and signals at Ka band injected into the lower port will also pass to the output port. One more function is required, a DC block to the Ka band port, this was realised by a resonant cavity formed in the outer material, with coupling stubs at each end, efficiently coupling the fundamental Ka band energy across, while blocking the DC.

The component described has been simulated in Ansoff HFSS, with promising results, and the parts needed drawn in Solidworks 3D, it has not yet been physically realised and tested. The line lengths have been adjusted empirically in order to achieve the required bandwidth.

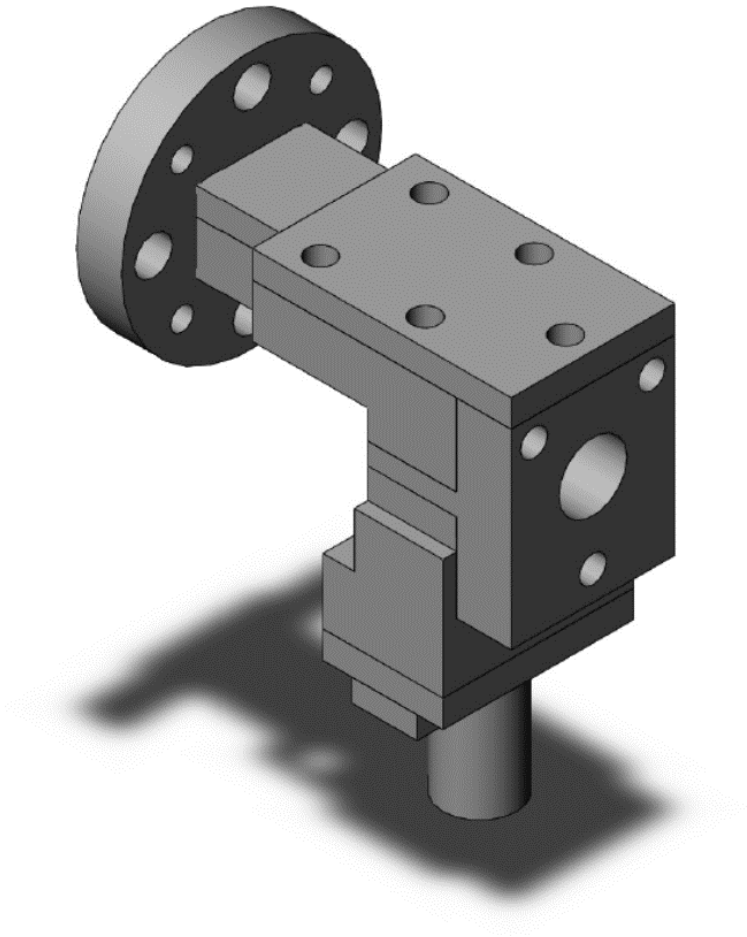

Figure 4.25 Solidworks assembly drawing of the proposed Ka-V diplexer.

For the inner connections to be made, a complex assembly is required, with the parts made to the highest precision. The combined port is the smooth bore hole seen in the vertical face (fig. 4.25), which would be tapped to accept a Southwest Microwave Inc.1.85mm pin launch connector, the depth has been designed to allow a standard production part to be used as an inner pin, avoiding the need for precision turning and electroplating. Similarly the Ka band port has a 2.9mm flange mount pin launch, the inner pin projecting directly into the DC block resonator chamber.

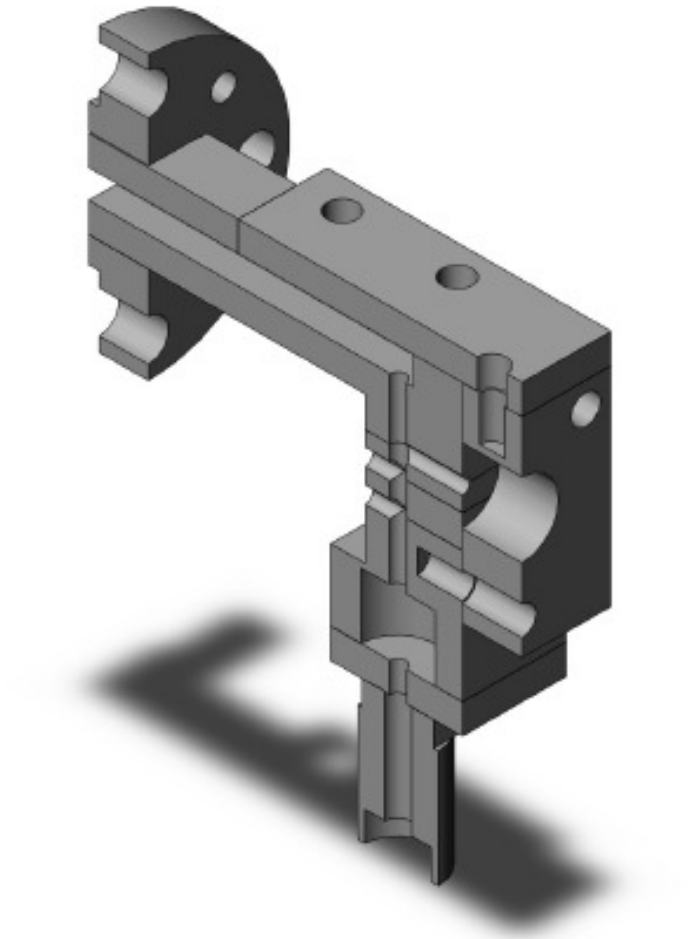

Figure 4.26 Section through the proposed Ka-V band diplexer, inner not shown.

4.7 Conclusions.

DC bias memory effects are a function of the system, not the device, so therefore it must be the responsibility of the circuit designer to ensure that the realised performance is adequate for the intended application. While this is normally a case of ensuring adequate supply decoupling to avoid a reduction in linearity from the theoretical optimum [19], it has been shown previously that a degree of linearity improvement can be obtained by the synthesis of a negative impedance for the drain bias [16].

The multiplexing techniques developed at Cardiff provide an effective low impedance supply over the baseband frequency range [12] for use during the characterisation process, and a low loss diplexing function allowing low power active harmonic load pull at Ka band [15]. By extending the technique to full multiplexing a very compact

low loss structure can be assembled for a much lower cost than the traditional assembly, with the potential for even lower cost stripline construction.

Specialised coaxial/waveguide diplexer designs will assist in raising the possible power level for Ka band load pull measurements.

Chapter 5 Investigating Residual Knee Walkout.

5.1 Constant Load Measurements.

There remains a significant knee walkout effect at higher drain voltages in the GaN on SiC HFET devices considered in chapters 2, 3 and 4 which is not affected by duty cycle, the 3eV laser or the improvements to the source coupled field plate (which successfully emulates the effect of the laser to a large degree). Various possible causes have been advanced, the objective here is to determine the contribution, if any, that each makes. The principle used is very simple, realising it in practice is somewhat harder. It is an extension to higher frequencies of the principle of measuring the device into a purely resistive load, as is typically used in classic AC design. The advent of high voltage logic ics and high speed, high resolution ADCs allows such measurements on a nanosecond timescale, thereby revealing the cause and extent of transient effects and facilitating the measurement of the time constants.

5.2 Evaluating Possible Thermal effects.

It has been shown by comparing pulse and continuous signals (chapter 2) that for this GaN on SiC device the walkout is not significantly affected by the average amount of heat being generated. Confirming this, figure 5.1 below shows fan diagrams for a device under Class A and AB bias conditions, the heat dissipation is significantly higher under the Class A bias condition, yet the knee walkout is for practical purposes identical.

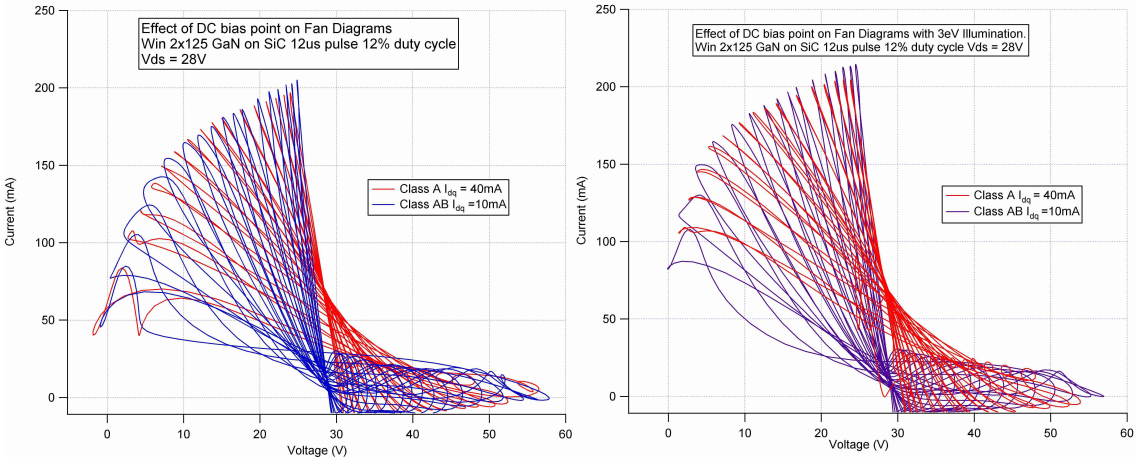

Figure 5.1 Effect of bias point on knee walkout, dark and with 3eV illumination.

Although the amount of current slump at very low load impedances is improved, around the 8V region where we would like to drive the RF load, there is no improvement in walkout under class AB. Activating the 3eV laser has a similar effect on both conditions, a slight improvement.

However, to approach the knee region from pinch off a real transistor must pass through a high dissipation phase, even in a high efficiency mode, resulting in a short burst of energy being applied to a very small region. Figure 5.2 shows an idealised representation of such a device, with a peak current of 100mA and a peak voltage of 100V, in accordance with accepted practice the waveforms are out of phase so that for most of the cycle no power is lost. Each state change must take a finite time however, and so the device must spend time with substantial heat being generated right in the channel region. This problem will worsen as the frequency rises, since the number of transitions per second increases, as is well established from microprocessor and switch mode PSU practice.

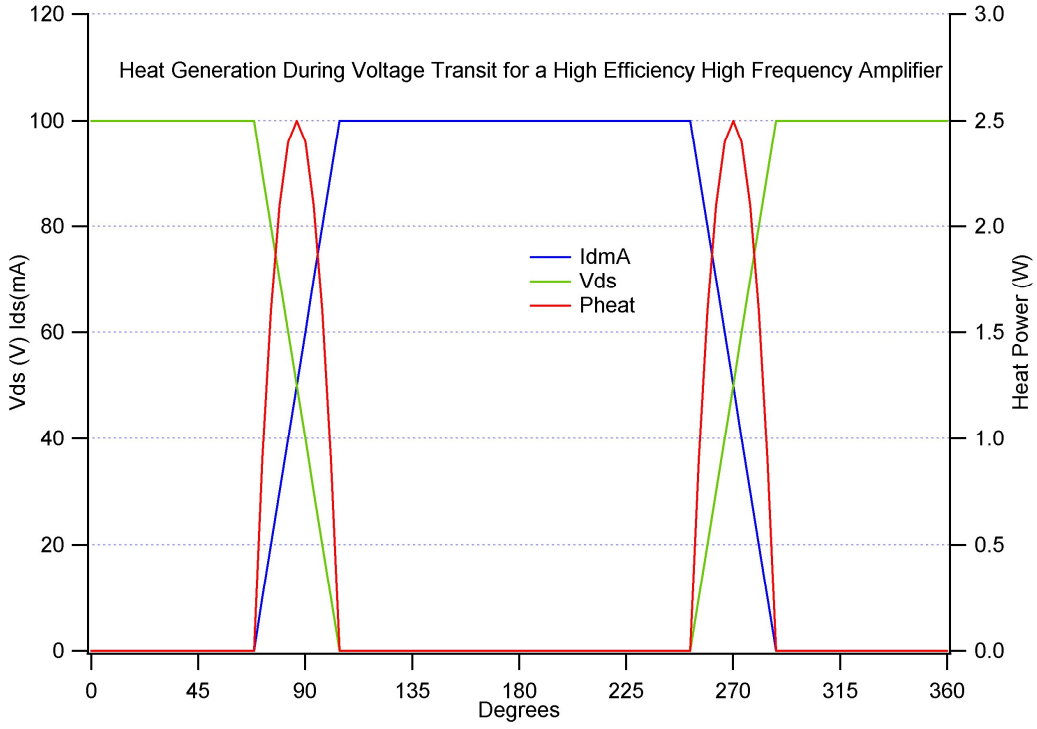

Figure 5.2 Typical switching losses in a high efficiency RF amplifier.

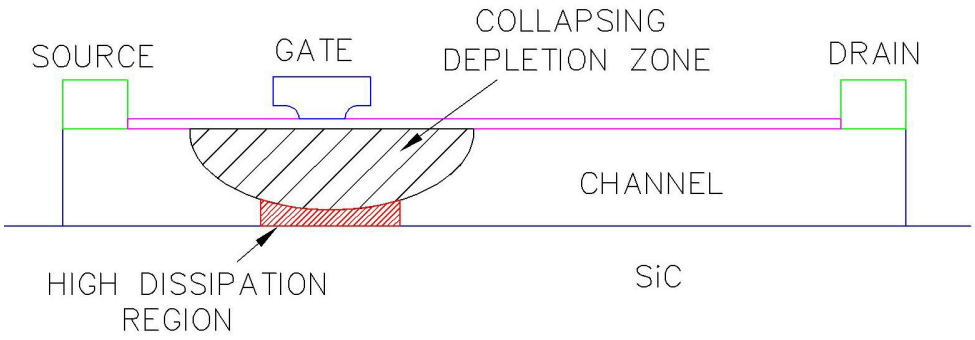

Figure 5.3 A possible "hot spot" under the gate.

As the depletion region begins to withdraw, the area of the channel under the gate is subjected to almost the entire voltage and all of the current, possibly causing a hot spot which is then sustained by its own raised resistance.

5.3 Deep and Surface Trapping.

An alternative possibility is charge being forced into the materials by the high voltage and subsequently reducing the available channel cross section, possibly in a region that the 3eV laser cannot physically reach, possibly at energy levels above 3eV, possibly in such a time frame the laser cannot clear them (i.e. at f_0 period speeds).

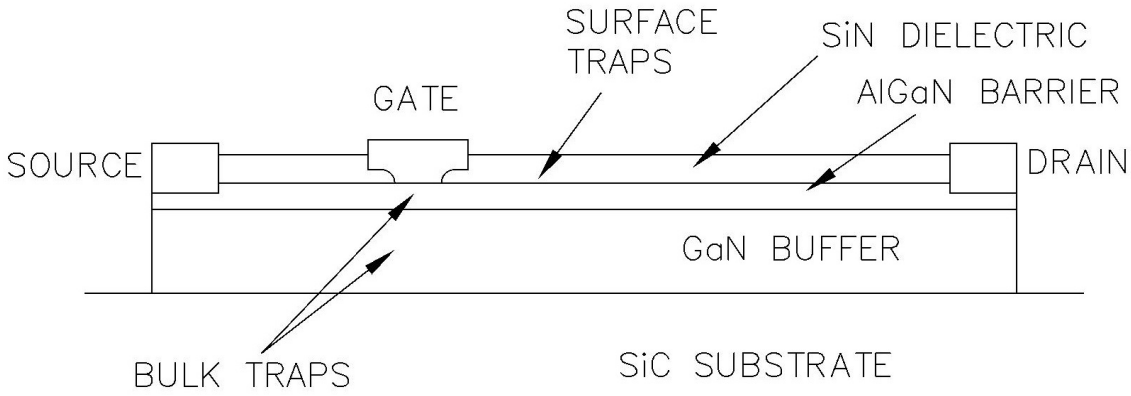

Figure 5.4 Potential trap sites in a GaN on SiC HEMT.

As discussed in chapter 3, there are several locations where charge may become trapped in a GaN HEMT [13], the main ones being within the bulk of the GaN buffer or AlGaN barrier, particularly under the gate region, also along the surface of the AlGaN beneath the SiN dielectric passivation between the gate and drain. Since these are due to different physical causes it is to be expected that they will exhibit different behaviour with time and sensitivity to stimuli such as voltages and light. The apparatus described

here can help to discern the effect each type of trap is having, and the effectiveness of countermeasures.

The evidence so far seems to show a reliance on maximum drain voltage experienced, and an insensitivity to any change in the average thermal conditions, the work described below can help to resolve such questions.

5.4 High Speed Resistive Drain Load Testing.

An apparatus was assembled (fig. 5.5) which allows further distinction between the various causes of knee walkout, by allowing any point on a selection of load-lines to be accessed and held at will. The RF load is replaced by a resistor from the supply rail to the drain, and the voltage at the resistor/drain terminal is monitored (see appendix G for full details).

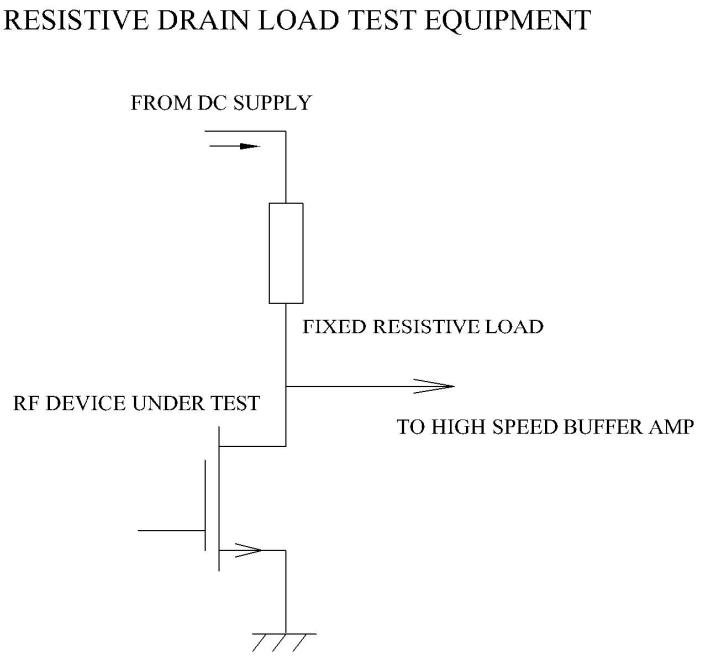

Figure 5.5 The basic schematic of the Resistive Drain Load apparatus.

In effect we now have all harmonics terminated in the same impedance, including DC (0fo), so we can create various scenarios which should show a marked difference in response according to which of the theories is in control.

The main objective in building the apparatus was to study the change in V_{DSmin} under different conditions, the device can now be held at any point on the load line and then

moved to the maximum conduction region (V_{GS} >= 0V) in a nano-second time-scale to reveal the extent of V_{DSmin} increase caused by each region of the load-line.

In practice this is achieved by using a high speed rail to rail comparator to drive the gate. The positive terminal of the comparator's supply is grounded and the magnitude of that supply then governs the negative voltage swing at the gate, see Appendix G for full details.

5.5 GaN on SiC example.

Following on from the work in Chapter 3, if we consider the loadlines of an example of the GaN on SiC die fitted with an optimised Source Coupled Field Plate (fig 5.6) we see the results in fig. 5.7 below. Operating in pulse mode with 10µs pulse width and 10% duty cycle the current fails to reach the level expected from the DC IV lines by a considerable margin, approximately 185mA rather than 220mA at Γ=0.7, activating the 3eV laser does not give a significant improvement. A series of resistive drain load measurements were taken based on this condition.

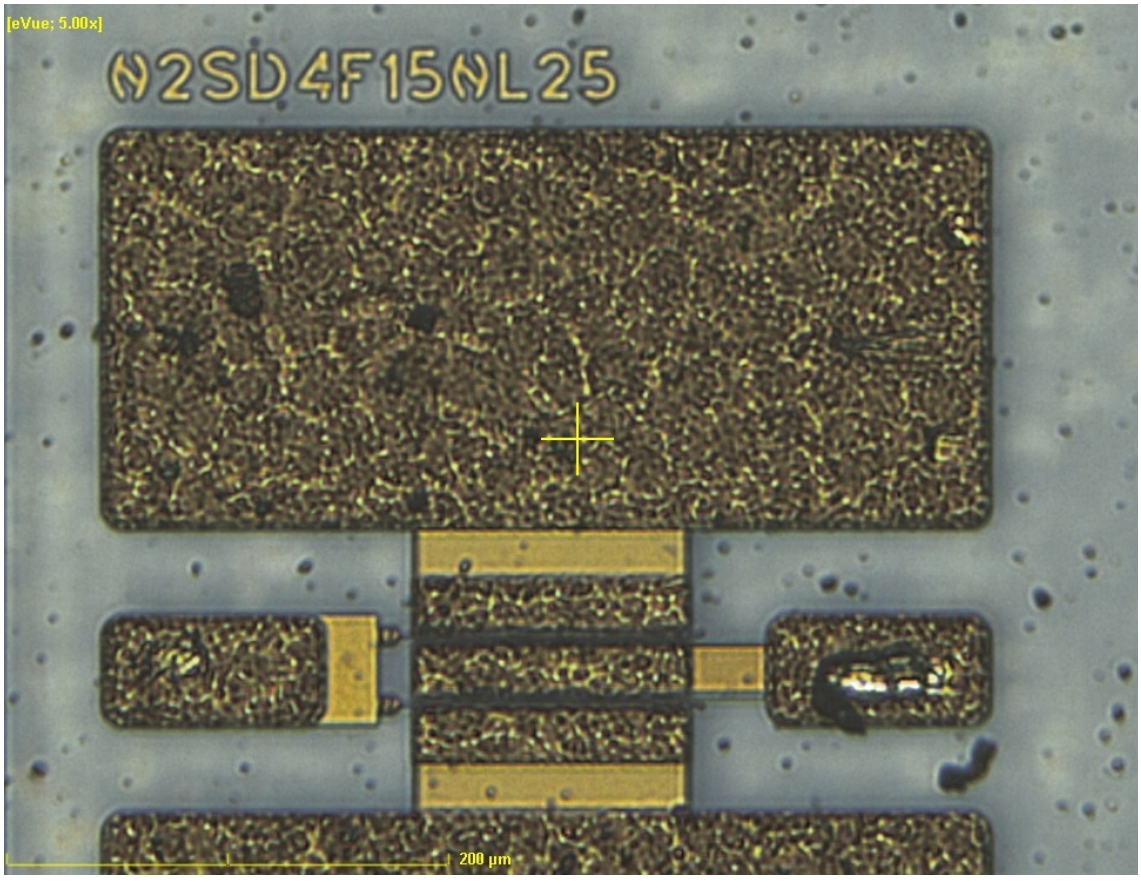

Figure 5.6 The Win 2x125 GaN on SiC test cell used for these tests.

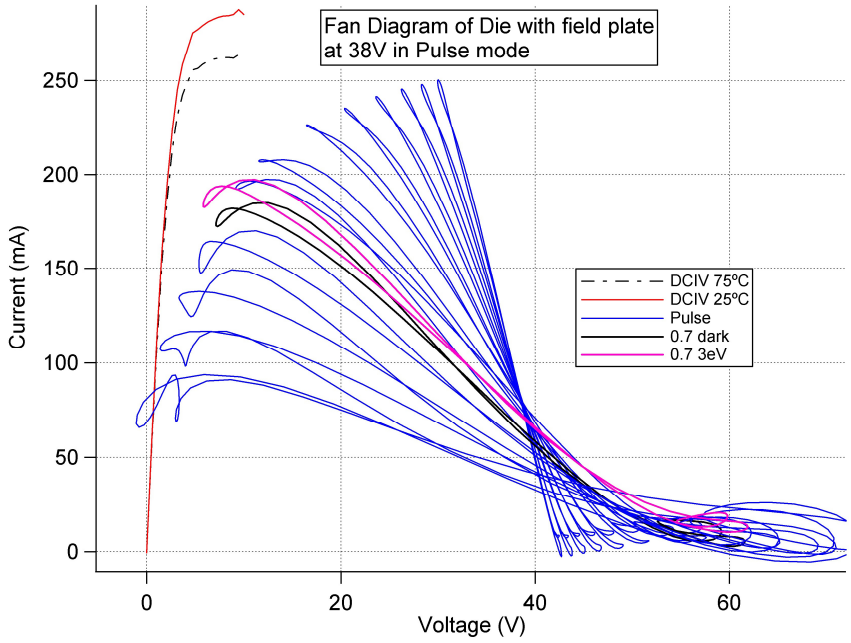

Figure 5.7 Loadlines for a GaN on SiC die, highlighting Γ=0.7 lines.

The drain resistor used was 285 Ohms, this is equivalent to a reflection coefficient of 0.7 in a 50 Ohm system, V_{DD} was set to 50V and V_{GS} switched between 0V and a range of negative values from -1.5V to -4.5V in 0.5V steps at a pulse repetition rate of 100KHz with a 20% duty cycle, that is the device was conducting for 2us, and nominally off for 8us each period.

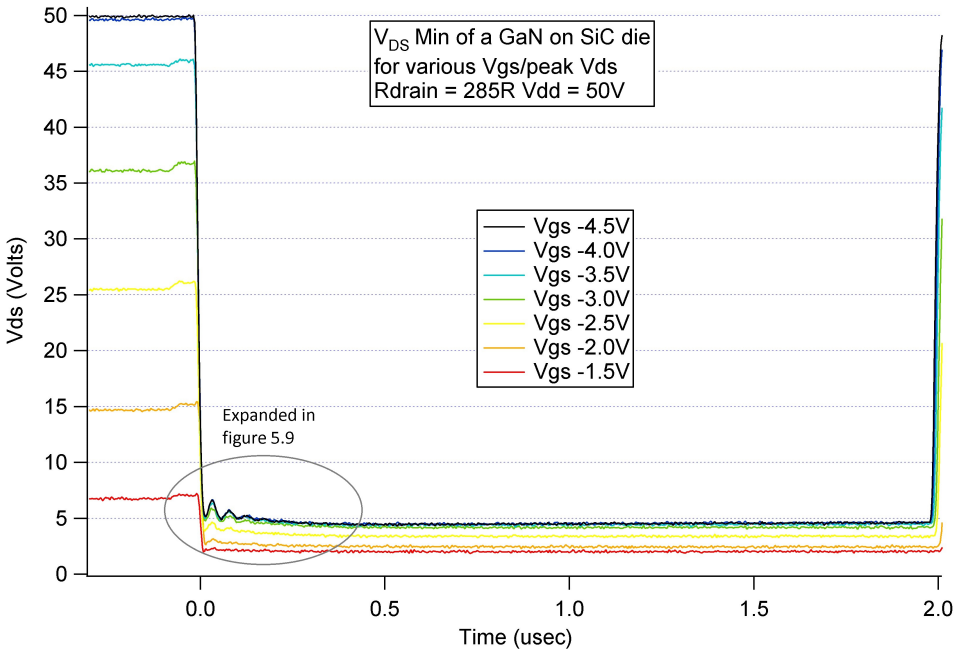

Figure 5.8 V_{DSmin} for a GaN on SiC die for various values of V_{GS}.

It is immediately apparent from fig. 5.8 that there is a link between the maximum value of V_{DS} and the subsequent minimum value, seen in close up in fig 5.9 below. As V_{GS} approaches pinch off, around -3.5V, then there is no further increase in V_{DS}, and indeed we see from fig 5.9 that the increase in V_{DSmin} also stops.

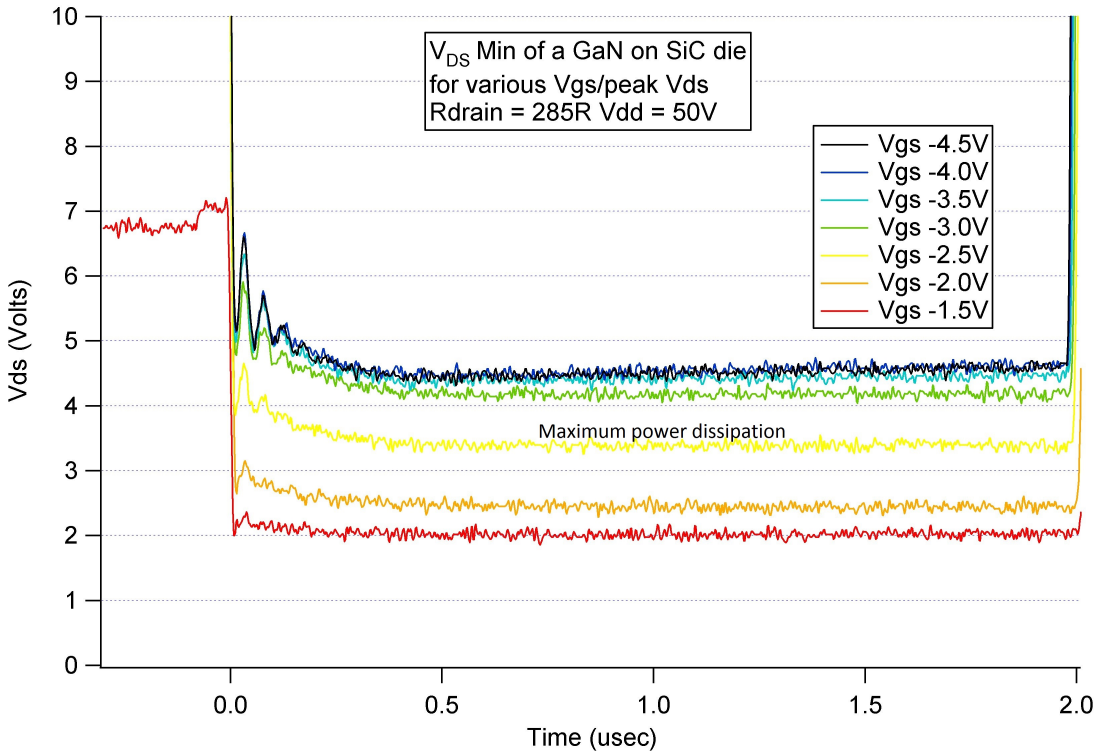

Figure 5.9 Close up of V_{DS} min for a GaN on SiC die for various values of V_{GS}.

If we consider the thermal dissipation in each case it is apparent that there is no link to temperature, at both extremes of V_{DS} the power dissipation in the die is low, in accordance with power transfer theory maximum heat is generated in the die when $V_{DS} = V_{DD}/2$, represented by the yellow trace in figs. 5.8 and 5.9. If this was a thermal phenomena this trace would have to represent one extreme during the "ON" phase, yet it is central, with cooler measurements either side, and if maintaining the maximum possible power dissipation for 8us fails to trigger a thermal reaction it would seem highly unlikely that transiting this region in a matter of nano or pico seconds could do so. It is therefore safe to conclude that this is some form of trapping effect.

5.6 Separating the Effects of V_{DS} and V_{GS} using 3eV light and Waveform Engineering.

Considering the root cause of the trapping effect it must be remembered that two parameters are changing during these measurements, V_{DS} and V_{GS}, some means of differentiation is very desirable. As mentioned above, once V_{GS} reaches -4V there can be no further increase in V_{DS}, so if we extend the measurement space we can see the effect of V_{GS} alone, fig. 5.10. The relationship is clearly not straightforward, as V_{GS} rises through the range which controls $V_{DS\ max}$, there is an increase in V_{DSmin} , but the rate of increase falls to zero as pinch off is approached and $V_{DS\ max}$ limits, only to increase again as V_{GS} decreases past -7V.

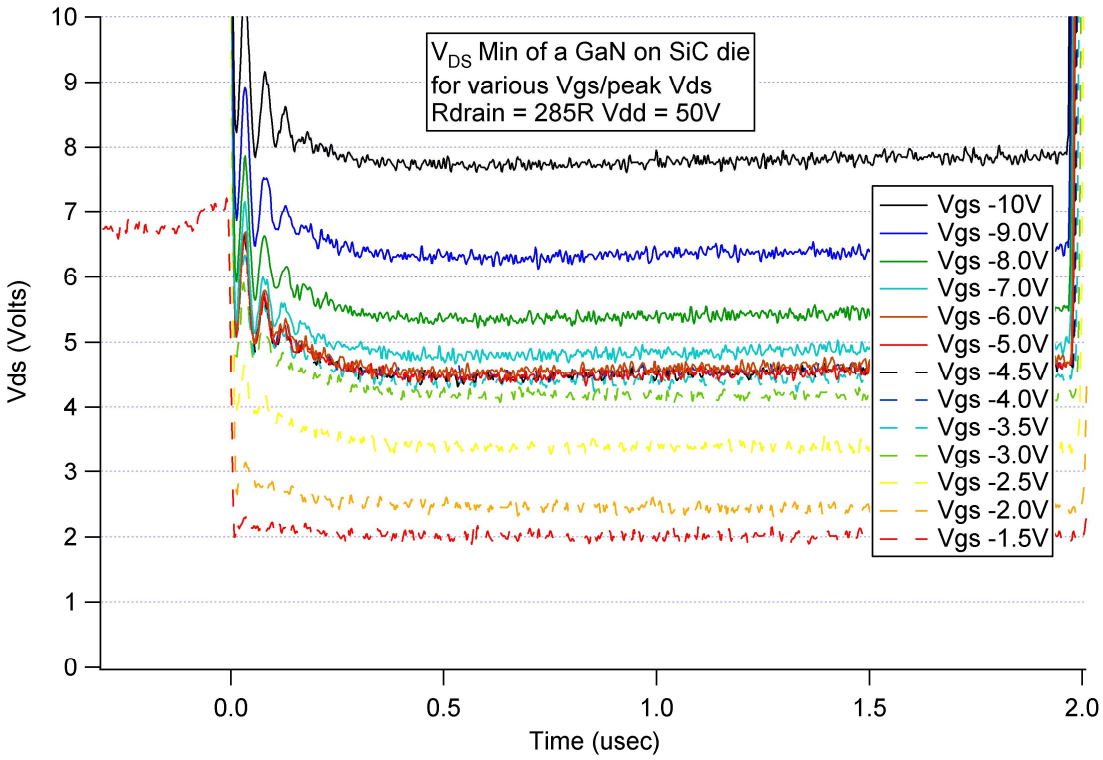

Figure 5.10 The effect of high V_{GS} on minimum V_{DS}.

It would appear that two different phenomena are being activated here, one linked to V_{DS} and the other to V_{GS}. In order to investigate this further an addition was made to the apparatus, a 5V6 Zener diode was placed in parallel with the DUT, as shown below in fig. 5.11, the auxiliary FET being used to switch the Zener in and out as required.

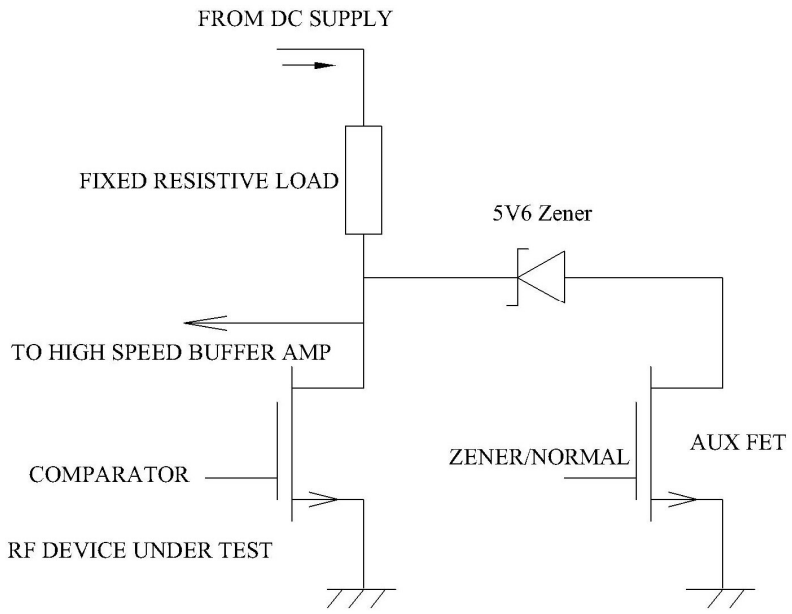

Figure 5.11 The Resistive Drain load equipment with the Zener diode in place.

Now V_{DSmax} can be clamped to nominally 5.6V, yet the "ON" phase of the measurement when V_{GS} is equal to or above 0V is as before. If the tests are repeated then the results are as shown in fig. 5.12.

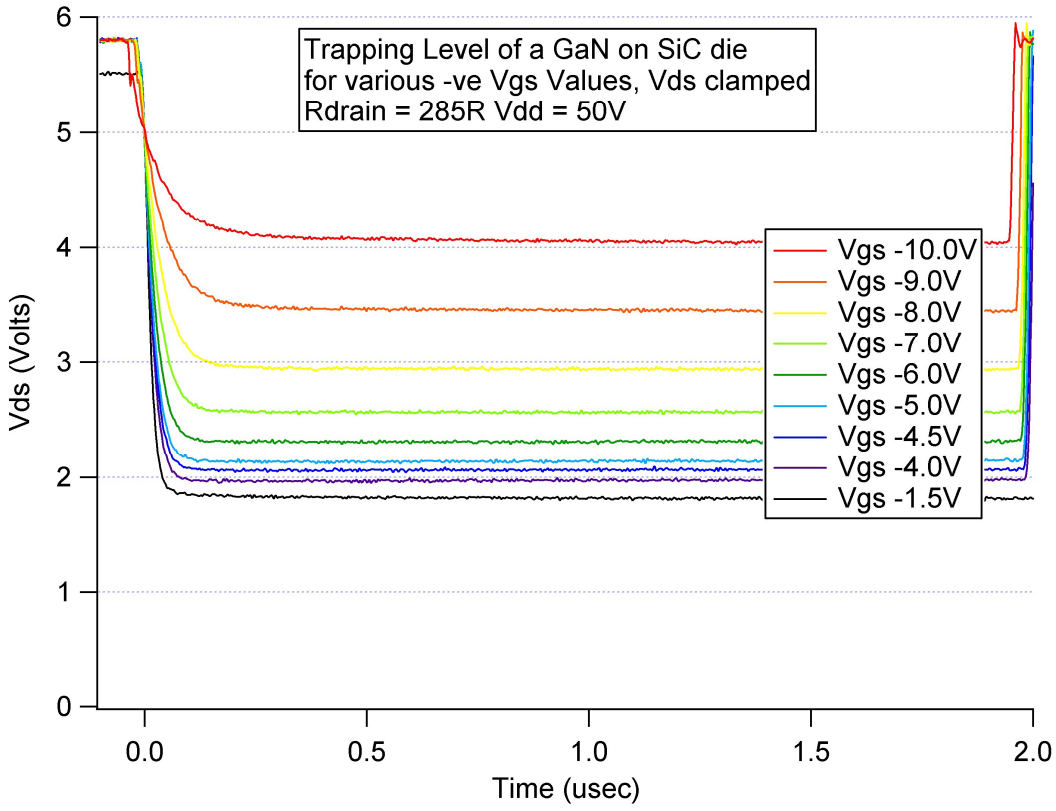

Figure 5.12 The effect of high V_{GS} on V_{DSmin}, V_{DSmax} clamped to 5.6V.

By effectively isolating V_{GS} in this way it becomes apparent that there is now little increase in V_{DSmin} over the range of V_{GS} values between conduction and pinch-off, so V_{DS} must be the dominant factor in this region. As V_{GS} decreases past -6V, once again we see V_{DSmin} climbing at an increasing rate, as V_{GS} related trapping begins to intensify. If we plot $V_{DS\ min}$ against V_{GS} during the off state it is clear that there is a plateau region after V_{GSoff} has reached pinch off (fig. 5.13).

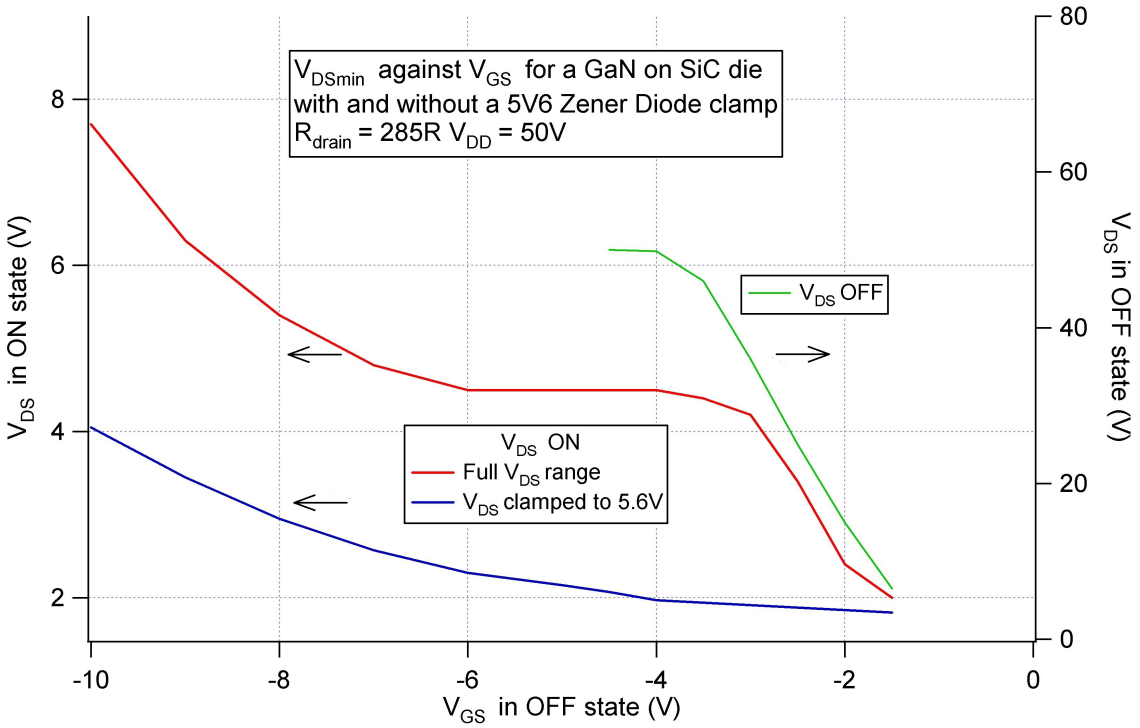

Figure 5.13 $V_{DS\ min}$ against V_{GS} during the off state.

It is also apparent that once V_{DSoff} is clamped by the Zener diode then the relationship becomes straightforward.

The work above only measures the total trapping level, and while it is apparent that both V_{GS} and V_{DS} can affect this, it is not clear whether there are two independent mechanisms or if the two fields are affecting the same cause of trapping. To investigate this the 3eV laser can be used, it can be seen from fig. 5.7 that this only has a relatively minor effect on the RF load-lines of the field plate equipped die, if we zoom in on the relevant region of the graph, fig. 5.14, we can see an approximately 1.2V change in V_{DSmin}, so if we are dealing with the same phenomena it should have a similar effect here also.

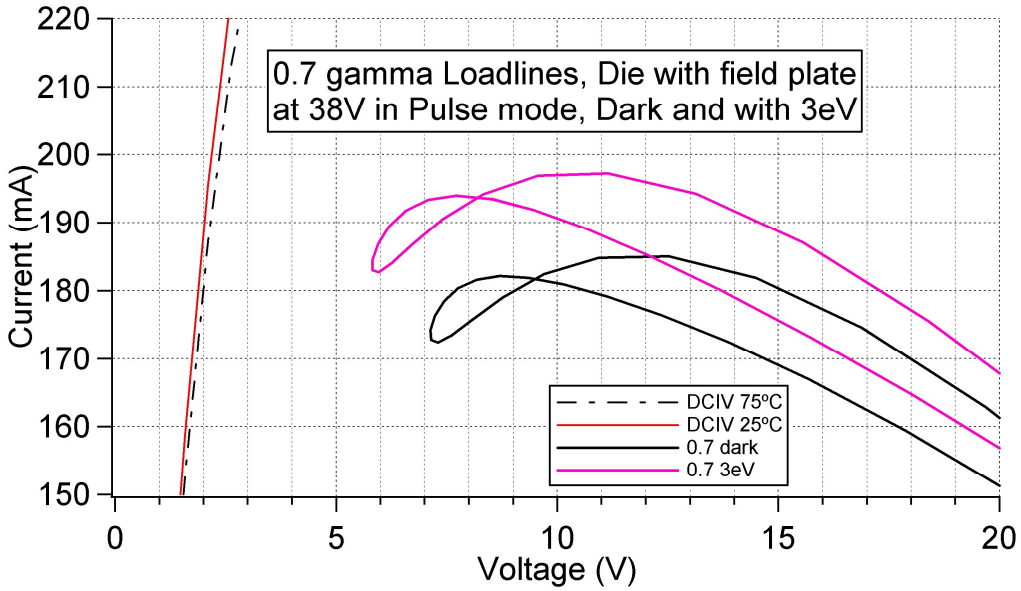

Figure 5.14 The effect of the 3eV laser on the V_{DSmin} of the Γ=0.7 loadlines.

Regarding the resistive load tests shown in fig. 5.15 we are certainly in the right space, it is difficult to make an absolute comparison between the two tests, due to the harmonic looping of the RF test and the rapid initial recovery seen in the resistive test, but the relative change is consistently around 1.2V.

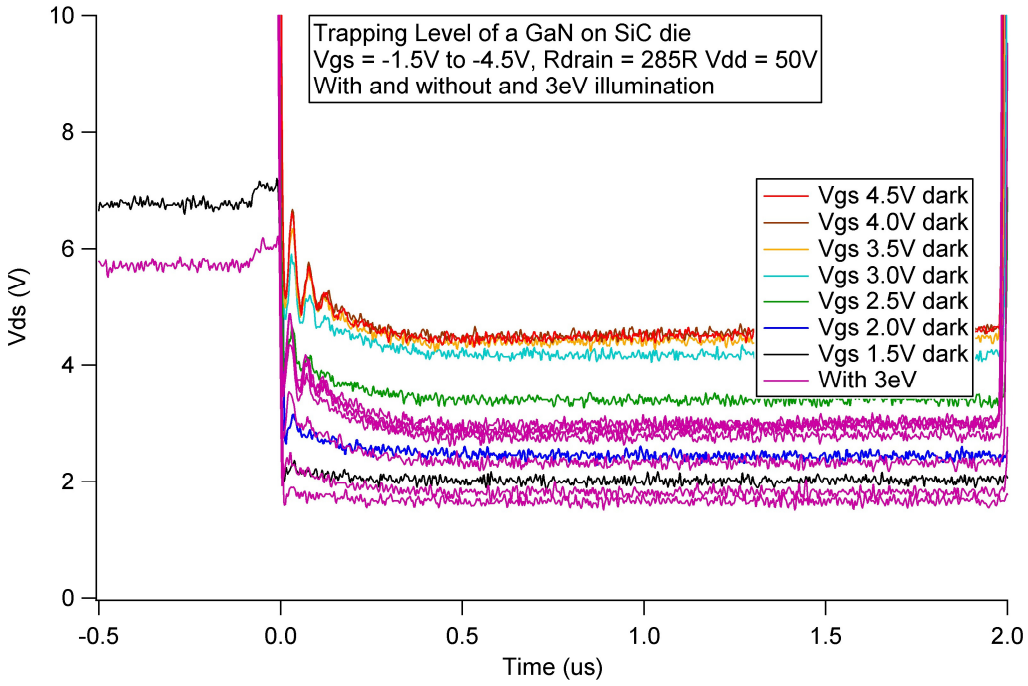

Figure 5.15 Effect of 3eV laser on V_{DS} induced trapping level.

In fig. 5.15 we clearly see that while the laser can improve the trapping level generated in the V_{DS} dominant region, (-1.5V > V_{GSoff} > -4.5V) it cannot eliminate it.

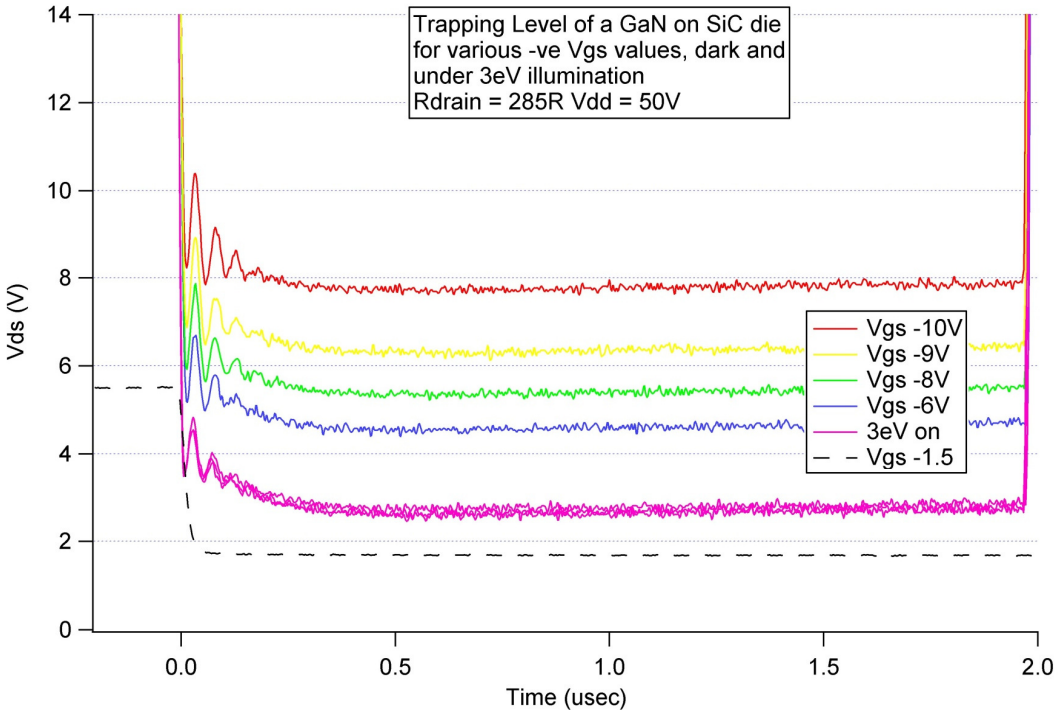

Figure 5.16 Effect of 3eV Laser on V_{GS} dominated trapping.

If we consider the traces for the more extreme values of $V_{GS,}$ a different picture emerges (fig. 5.16), the laser can return the device to the same state regardless of V_{GS}, also implying that the residual trapping we see under RF operation is due to V_{DS}.

If we now bring the Zener diode clamp into play and consider the responses when V_{GS} = -10V we can see that this is confirmed, fig. 5.17.

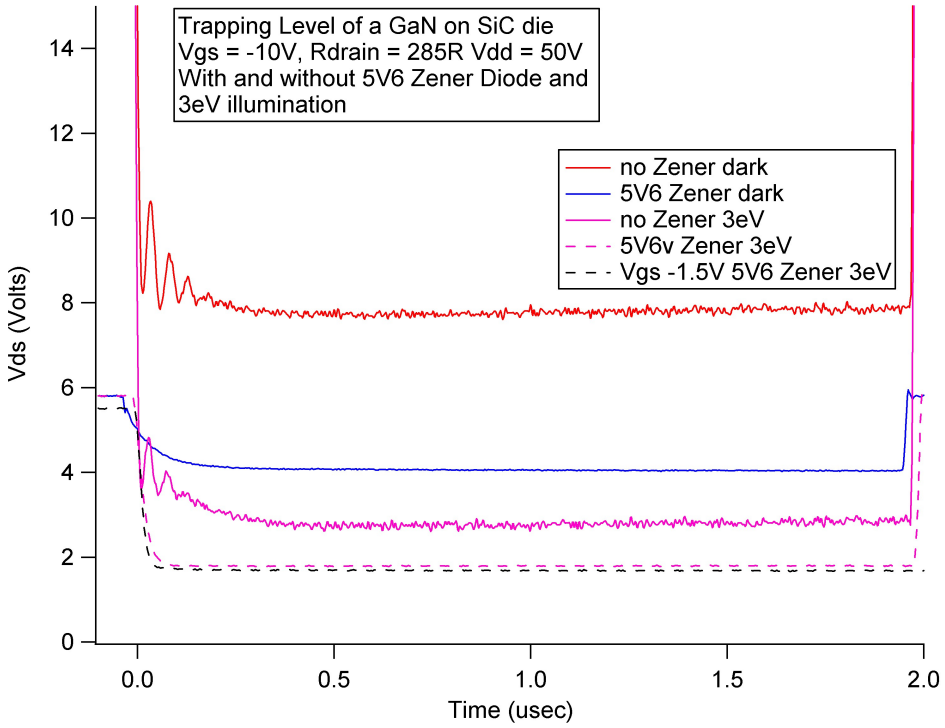

Figure 5.17 Effect of 3eV laser on V_{GS} induced trapping level.

The red trace in the above graph (fig. 5.17) shows V_{DSmin} for the device at V_{GS} = -10V without the Zener, switching on the laser changes this to the solid purple trace, the laser cannot wholly remove the trapping when V_{DS} is allowed to reach its normal operating level.

The blue trace shows the device still at V_{GS} = -10V, but with the Zener clamping V_{DS}, the trapping level is of course lower, and when the laser is activated (dashed purple) the trapping is effectively eliminated in a nanosecond timescale. The black dashed trace is with Zener, laser and Vgs = - 1.5V, as trap free a state as can be realised.

From these results it is concluded that the V_{GS} induced trapping must be physically different to the V_{DS} induced trapping, and since the trapping induced by high V_{GS} values can be almost fully released by the 3eV laser it seems unlikely that this is responsible for the residual knee walkout seen in the RF tests, which does not respond significantly to the laser. In order to investigate this some load-pull and harmonic source-pull tests were conducted, if we consider a fundamental only input voltage waveform and the resulting dynamic transfer characteristic (figs. 5.18 and 5.19) it is apparent that the majority of the negative trajectory is not in itself necessary, it is only there because the device is being driven from a sinusoidal source and a large positive input is required to

drive the device to a highly conducting state for a large percentage of the cycle, and to hold it pinched off for the remainder. If it were the case that the negative voltage was causing trapping which duly opposed the current flow that the positive voltage was trying to enable, then a more sophisticated drive scheme might be very advantageous.

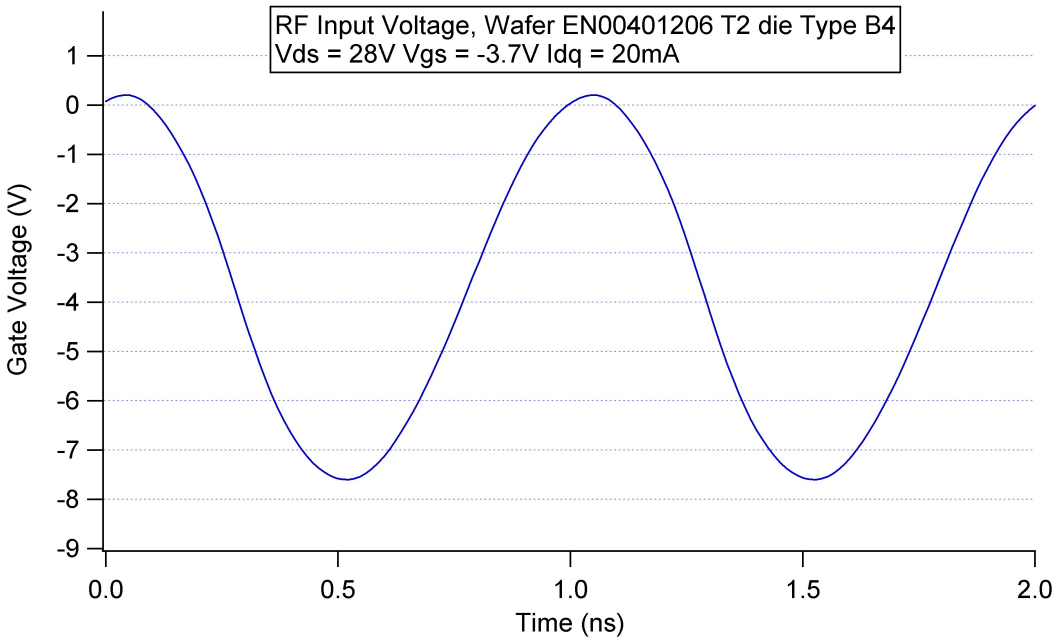

Figure 5.18 Input voltage waveform to drive a GaN die into compression.

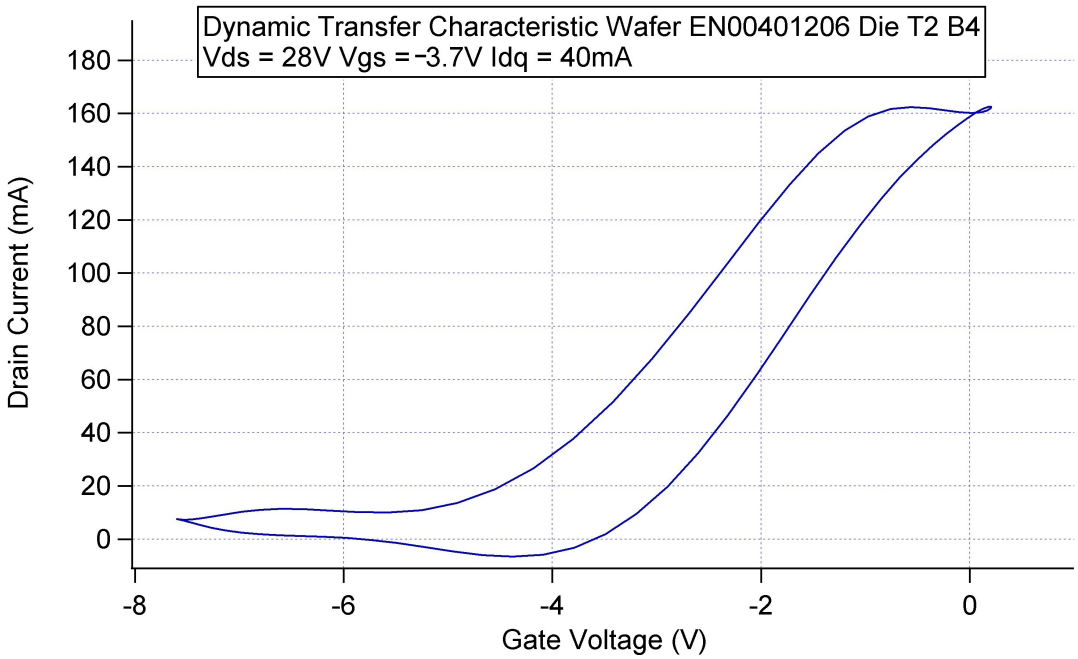

Figure 5.19 Dynamic Transfer Characteristic resulting from V_{GS} in Fig. 5.18.

If we now change the DC bias voltage so that a greater RF voltage swing is required to reach the same positive peak value, we can examine the effect of an increased negative voltage, figures 5.20 and 5.21.

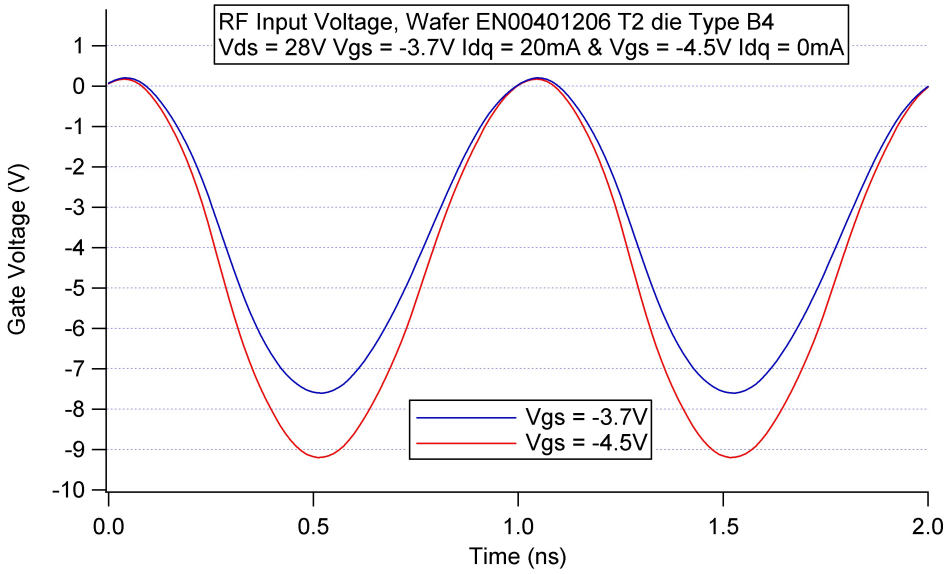

Figure 5.20 $V_{GS\,RF}$ under Class AB and C operation.

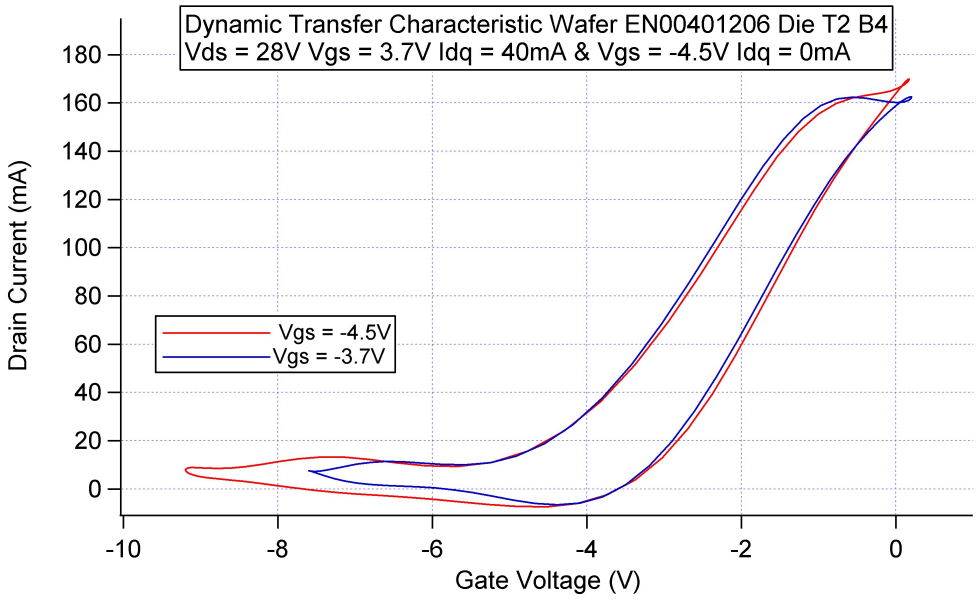

Figure 5.21 Dynamic Transfer Characteristics for Class AB and C operation.

Regarding figure 5.10, we could expect that the effect of the increased negative gate voltage would be an increase in V_{DSmin} of the order of 1.5V and an equivalent reduction in I_{DSmax}, however, from figure 5.21 we can see that the peak current is actually increased, possibly because the thermal dissipation is reduced.

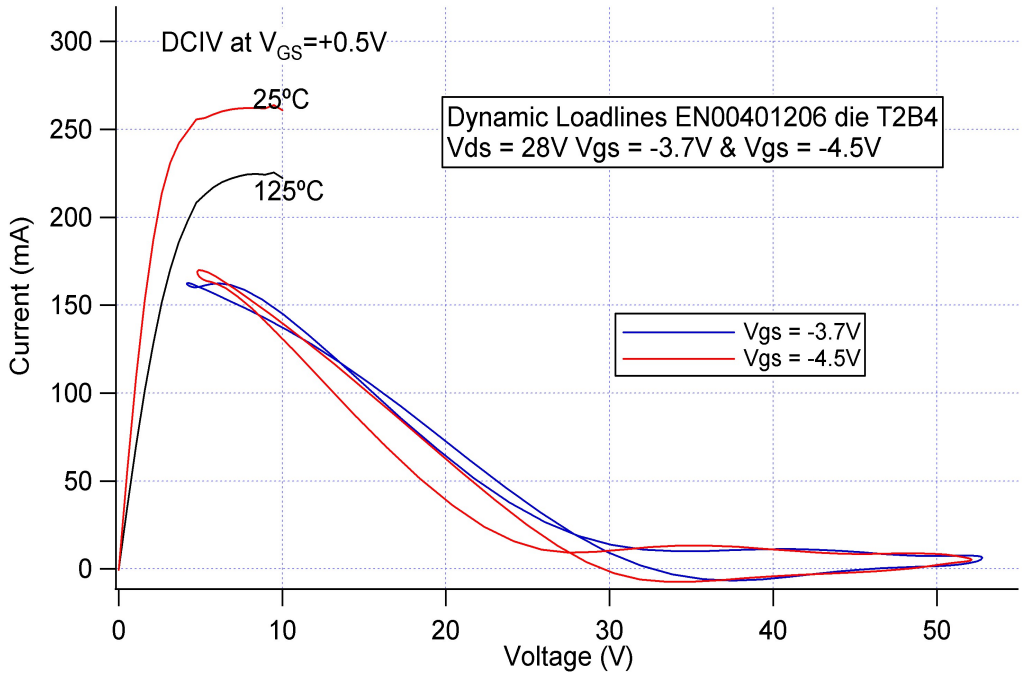

Figure 5.22 Dynamic loadlines for Class AB and C operation.

It is apparent from Fig. 5.22 that the greater negative excursion resulting from operation in Class C is not having the detrimental effect that might be expected after examining the drain load test results, it may be that the filling and emptying time constants are such that the average level is low under RF operation, or that the RF walkout is predominantly due to V_{DS} generated trapping, the latter is supported by the reaction to 3eV light. Considering figures 5.14 through to 5.17 we see that the laser cannot remove the RF walkout completely, fig 5.15, nor can it remove V_{DS} generated trapping completely, whereas trapping due to V_{GS} can be more effectively reduced, figs 5.16 and 5.17, which implies the V_{GS} phenomena is not the key factor in the walkout.

It is apparent from fig. 5.19 that voltages below -4.5V and above 0V are not needed to generate the required output current, it should be possible to substitute an engineered input waveform without the extremes of voltage, and it has been demonstrated by M. Haynes et al in “High Efficiency PA design Strategy at X-band” [22] that a substantial improvement in power gain and consequently power added efficiency of a GaAs die can be realised by adding a $2f_0$ input signal in such a relative phase that the negative excursion is reduced and the positive excursion enhanced. It seems reasonable to conjecture that this approach may also have a reliability benefit by reducing stress and

V_{GS} induced trapping, although no immediate effects have been shown here the potential of the technique has been demonstrated.

5.7 Using RDL and extreme duty cycles to determine trapping time constants.

Another possible use for the RDL circuit is to study trap filling and clearing times, if the device is left in a condition considered to empty traps for a very long period, and is then subjected to a filling condition for various lengths of time the resulting level of V_{DSmin} gives an insight into the filling time constant.

By observing the decay of V_{DSmin} it was found that for this device a period of 300s was sufficient to reach equilibrium, to be certain the ON period was set to 1000s, achieved by adding a number of divide by 10 74 series TTL gates to the pulse generator output of the Picoscope 4227 sampling oscilloscope used for these measurements. The very rapid OFF pulses required were generated using the pulse timing circuit developed for the VTD SWAP load pull system, which produces pulses from 2 to 400µs in response to a falling edge trigger signal (Appendix B). In this way extreme duty cycles up to 500,000:1 can be generated, and the 4227 sampling window can be set independently to study either rapid events close to the filling pulse, or the whole inter-pulse period with reduced time resolution.

OFF pulses between 2 and 100µs were found to cover the filling range, as seen in fig. 5.23. Although considerable measurement artefacts are present the underlying pattern can be discerned, if the post pulse maximums are plotted separately and analysed the time constants for the filling function can be extracted, these should be independent of the absolute values, fig. 5.24.

It was found that a double exponential function was needed to give a good fit, resulting in the following equation:

post pulse of t seconds,

$$V_{DSmin} = 2.23 - 0.28181e^{(-11789t)} - 0.14417e^{(62201t)}$$

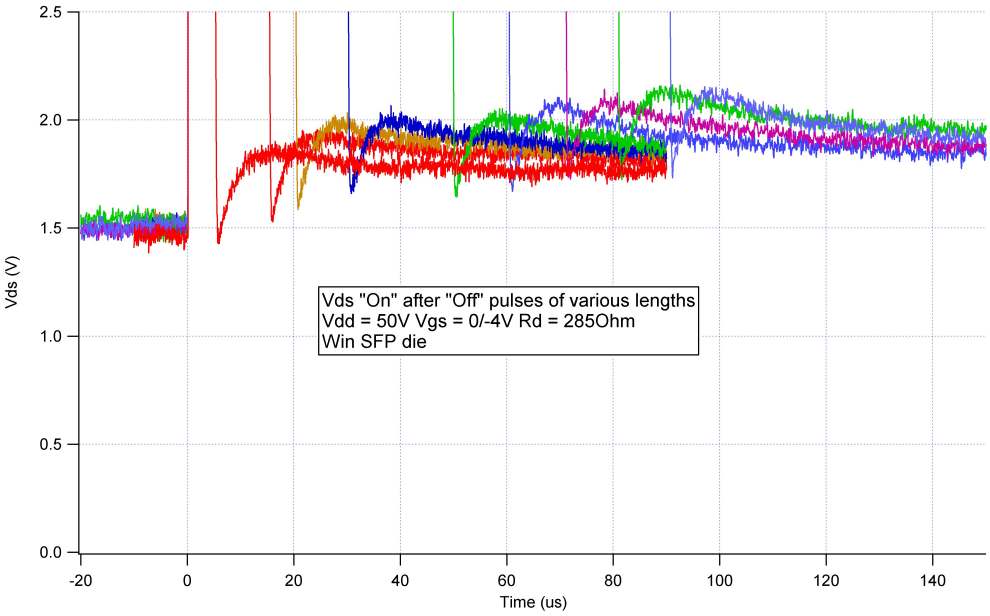

Figure 5.23 V_{DSmin} against "OFF" period for a GaN SFP die.

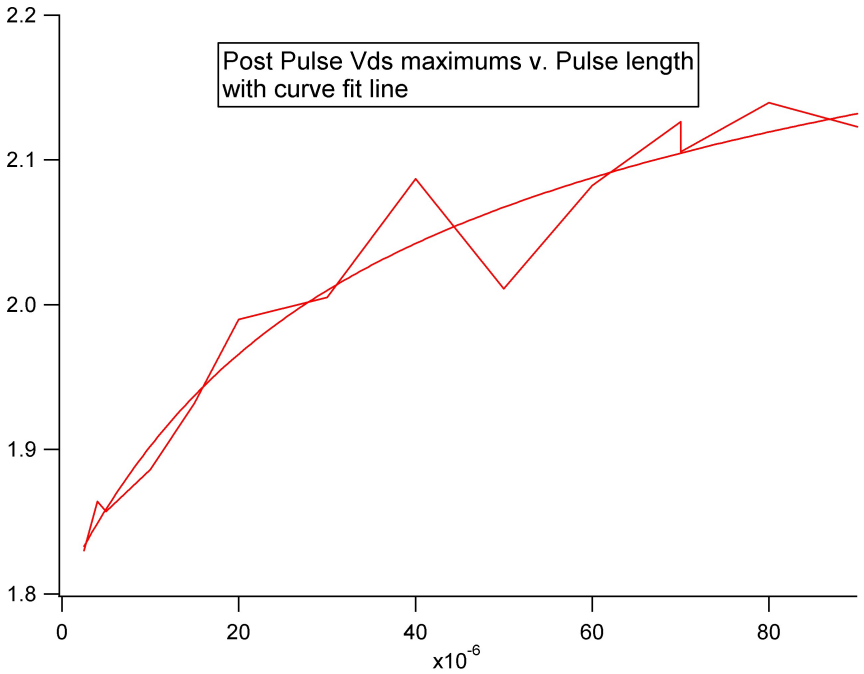

Figure 5.24 Post pulse V_{DSmin} maxima and a curve fitted line.

Clearly much work remains to be done to conclude this topic, which is presented here as a field for future work. Similarly the basis for measuring the clearing time constants can be demonstrated, since we have shown that trapping is maximised after approximately 100µs, if we subject the device to a 200µs filling pulse and then observe the decay time we can curve fit the decay function, figs. 5,25 and 5.26.

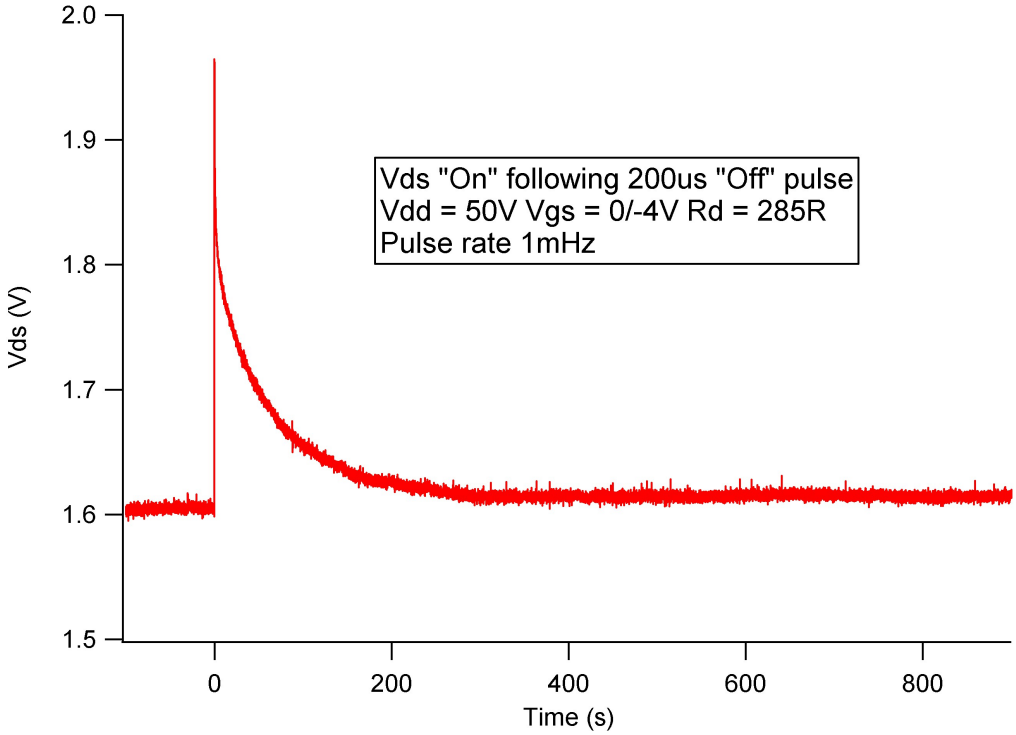

Figure 5.25 V_{DSmin} decay after a 200µs trap filling pulse.

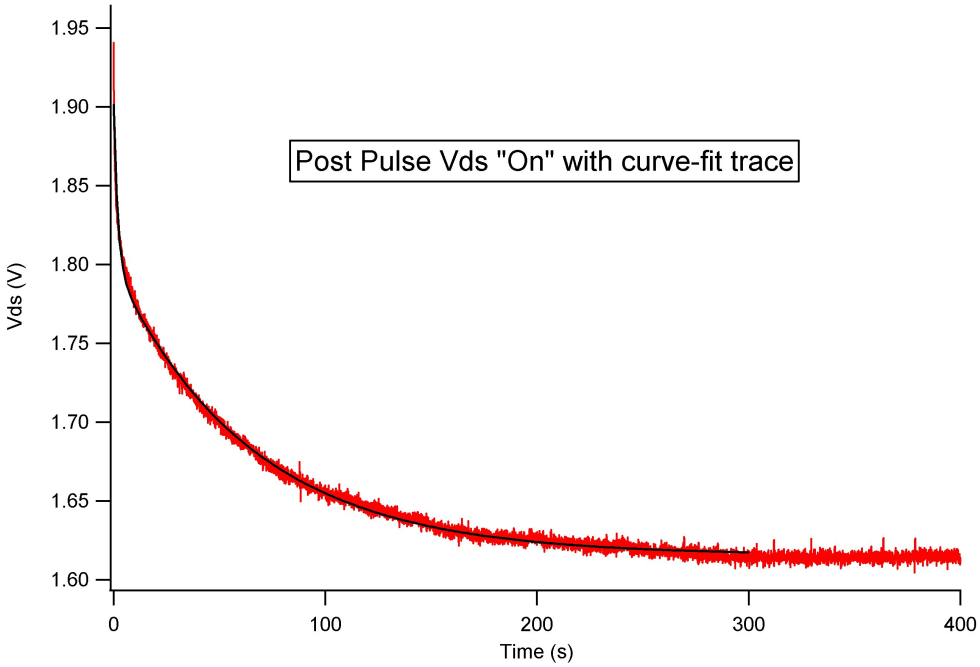

Figure 5.26 Double exponential function curve fitted to V_{DSmin}.

Once again a double exponential function is needed to obtain a good fit:

post pulse $V_{DSmin} = 1.6148 + 0.18355e^{(-0.015177t)} + 0.10044e^{(-0.48751t)}$

5.8 Conclusions.

The work shown here demonstrates that by careful development of the circuit the basic technique of using a fixed resistance in the drain feed can reveal a great deal about the behaviour of a device, notably the existence or otherwise of thermal effects and how the different voltage parameters affect the trapping levels. For the GaN on SiC HFET device used for this study, the residual knee walkout is due to trapping effects, and is not a thermal phenomena.

The additions of the 3eV laser and the Zener diode clamp enables the separation of the trapping causes, and how these relate to RF performance. It has been shown that for the GaN on SiC HFET used for this study V_{DS} is the primary cause of trapping which impacts upon the RF performance.

The potential for further development to allow trapping time constants to be extracted has been shown.

Chapter 6 A Pulsed Fully Active Harmonic Loadpull System

6.1 The Advantages of a Pulsed Fully Active Harmonic Load-Pull System.

Looking at the complexity of the pulsed Fully Active Harmonic Load-pull system (fig 6.6) it is apparent that there needs to be a good reason to go to these lengths, in fact there are several, each compelling in their own right, together it is hard to imagine why this feature would be omitted from a new system.

i. The device may be stressed beyond continuous operation limits, essential for some systems such as pulsed radar and modulated supply schemes.

ii. There is a reduced risk of damaging the device during measurement, even when the intention is to use the device for a CW design as the effective Safe Operating Region is extended during the test phase.

iii. The thermal loading on the test bench is reduced, as the power output levels of devices for X band and K band rises it is becoming increasingly difficult to source components which can operate with the high VSWR and DC loads of an FAHLP system.

iv. The thermal properties of the device may be investigated by examining the behaviour under various conditions

In light of these advantages it is not surprising that pulse systems have been implemented before, in “Very small duty cycles for pulsed time domain transistor characterization” [18] De Groote et al discuss the advantages of a pulsed measurement system based upon a sampling receiver; notably how this system can maintain its dynamic range under pulsed operation unlike the VNA based LSNA systems. Dynamic load-lines are extracted and the importance of including good harmonic data is shown. The loadpull system used is however passive, and as such can only exert limited control over the harmonic terminations. During the course of this work a pulsed system with active control up to the third harmonic was implemented, allowing “fan diagrams” of load-lines over a range of impedances to be drawn with $\Gamma 2f_0$ and $\Gamma 3f_0$ equal to Γf_0, as seen in the right hand side of fig 6.1. For Γf_0 values near zero there is little difference of

course, but as the fundamental load resistance increases relative to the harmonic loads then the harmonic currents increase and alter the load-line, making the end points ill-defined.

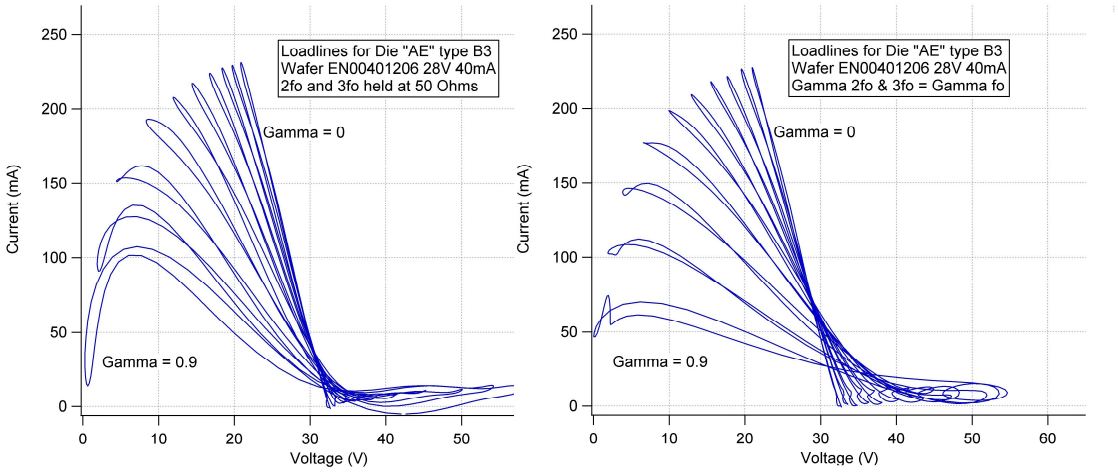

Figure 6.1 Comparison of fan diagrams with the load for $2f_0$ and $3f_0$ held at 50R (left), and taken to the same load as f_0 (right).

Also, by controlling the harmonic loads data can be taken in different operational modes such as Class F and Class F^{-1}, without the need to fabricate hardware circuits. With a passive system the loss between the remote termination and the device tends to prevent the necessary high reflection coefficients being achieved at the harmonics, a problem which gets more severe as frequencies rise. It also becomes possible to extract the data needed for the new Continuous Modes of operation [21] used for broadband amplifier designs, where an offset in the angle of the harmonic termination is countered by an offset of the fundamental load. With this equipment the harmonics may easily be swept to reveal the relationship between reactive fundamental and harmonic loads, and the resulting effect on the waveforms examined.

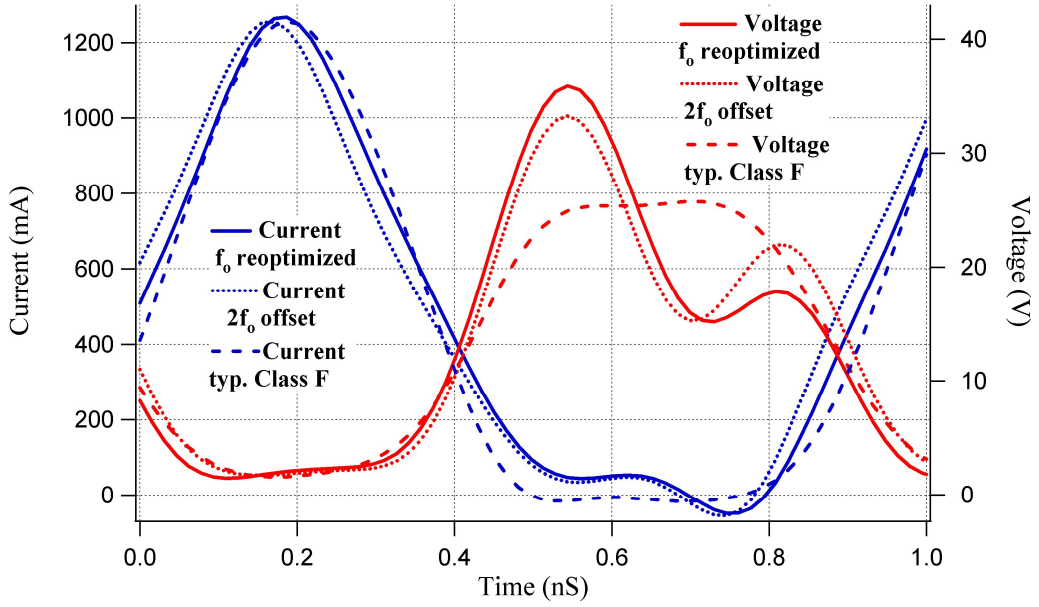

Figure 6.2 Investigation of Continuous Mode Operation with GaAs die.

In fig 6.2 above we see that by changing the angle of the second harmonic load the voltage waveform is altered, a significant voltage is present as the current begins to flow around 800ps resulting in reduced efficiency. In accordance with Continuous Mode theory, introducing a reactive component to the fundamental load can alter the voltage waveform to recover the performance. Examining these diagrams highlights the potential dangers of exploiting Continuous Mode techniques with GaAs, the peak drain voltage is much higher, jeopardising the die, here again, Pulsed Fully Active Harmonic Load Pull makes quantifying this risk a straightforward process.

As has been previously observed [20], GaN devices tend to be thermally limited, that is to say their breakdown voltage is high (typically 200V) so that power dissipation and subsequent channel temperature rise governs the useful power output. If the final application does not require continuous operation then substantial cost and size savings may be made by briefly driving the devices well beyond their continuous safe operating region in pulsed operation or in modulated bias schemes such as Envelope Tracking, in order to do this representative data must be gathered. While data gathered at lower drain bias voltages may be extrapolated, the effective output capacitance (C_{ds}) of GaN FETs changes with voltage (fig. 6.3), so this can only be an approximation, and no allowance will be made for the trapping induced knee walkout (chapters 3 and 5) which is likely to occur in such devices.

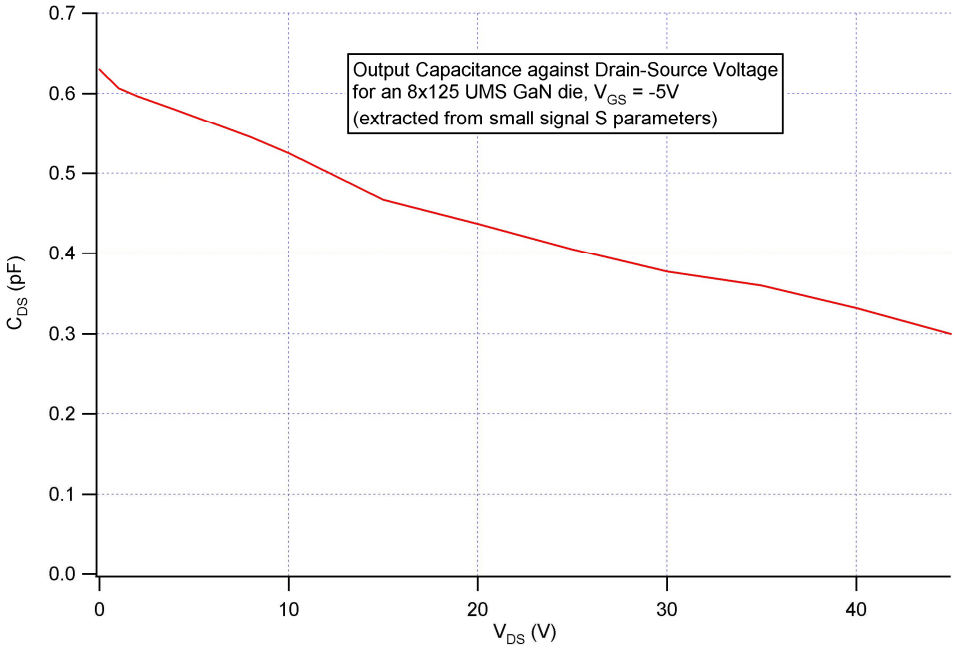

Figure 6.3 Variation of C_{DS} with V_{DS} for a UMS 0.25um 8x125 GaN die.

Even when the intention is to gather data for continuous operation it is easy to stray into thermally dangerous regions of the Smith chart if the device is not already well understood, mapping the load initially under pulse operation allows the safe operating region to be defined without degrading the device.

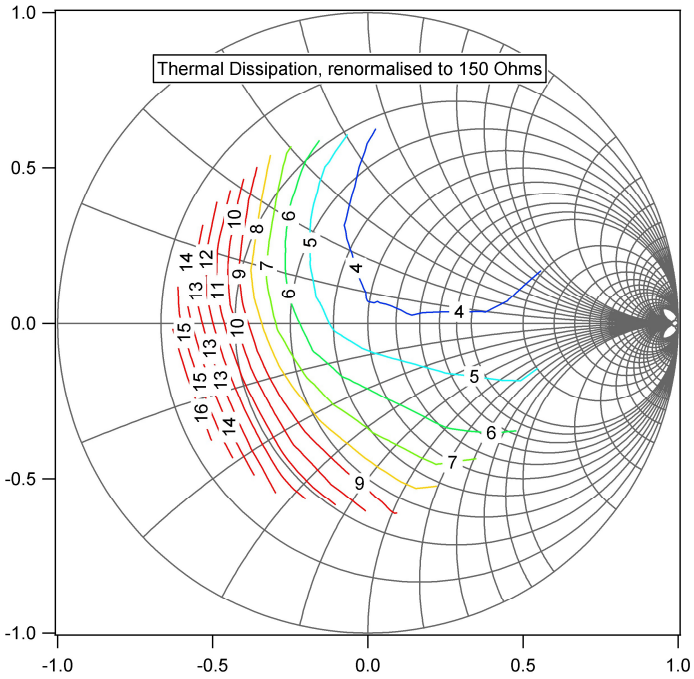

Figure 6.4 Thermal dissipation against Load Impedance contours.

The thermal contour diagram (fig. 6.4) illustrates the instantaneous dissipation as a function of output load for a certain device, any attempt to operate the device continuously in the regions shown dissipating more than 8W would permanently damage this particular part. Whilst conducting load pull measurements, as well as intentional mismatches, there is also the risk of accidentally presenting damaging loads to the device, an active system can even go well outside the Unity Gamma circle. Experience has shown that with a 10% duty cycle there is a very good chance of the device surviving mistreatment at an extreme level that would certainly cause damage if applied continuously.

When considering the thermal loading on the test bench components it is important to bear in mind that in an active load pull system, the output power is in fact the difference between the forward and reverse waves, if the target load differs substantially from the system impedance then the voltage and current waves present will be much higher, fig. 6.5. Once again this has been exacerbated by the introduction of GaN, the high supply voltages normally used mean that the target loads for small parts suitable for on wafer testing are likely to be higher than 50R.

Consider a part which is expected to produce an output power of 5W when optimally matched with a 50V drain bias, the load (Z_L) is likely to be around 250R, in a system with a characteristic impedance (Z_0) of 50 ohms this is a reflection coefficient (Γ) of

$$\Gamma = (Z_L - Z_0)/(Z_L + Z_0) = (250-50)/(250+50) = 0.66$$

The output power (P_{out}) is the difference between the power passing from the device to the ballast load (P^+) and the power injected by the loadpull amplifier (P^-)

$$P_{out} = P^+ - P^- \quad (1)$$

Setting P_{out} to the expected 5W we know the forward power P^+ is given by

$$P^+ = P_{out}/(1 - |\Gamma|^2) = 5/(1 - 0.66^2) = 9W \quad (2)$$

And since the output is the difference between the forward and reverse waves,

it follows from (1) that

$$P^- = P^+ - P_{out} = 9 - 5 = 4W \quad (3)$$

The circulator is one component likely to cause problems in high frequency systems, these are normally specified for a 50 Ohm system, with power travelling solely between two ports. In the example given above we have 9W travelling in one direction from the device to the load, and 4W in the other from the loadpull amplifier to the device, so we would see the equivalent heating as from a 13W unidirectional flow, therefore a part rated at 10W CW would not be adequate to test this device to 5W under CW conditions. Clearly if we change to a 10% duty cycle scheme then the average heating is reduced to 10% of 13W, a mere 1.3W.

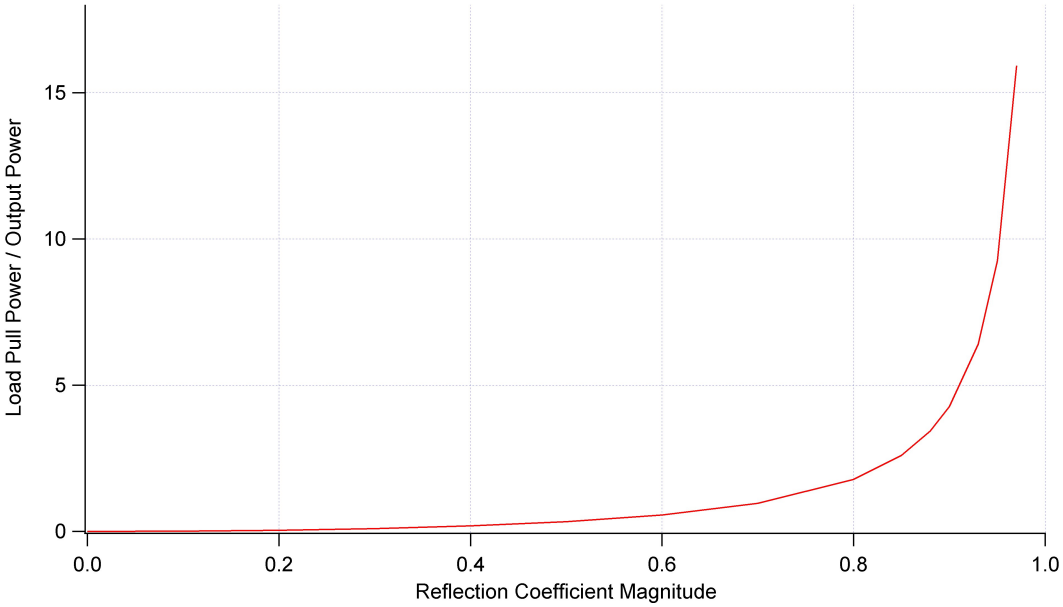

Figure 6.5 Load-pull power requirement against Reflection Coefficient.

An established point worth repeating here is that when calculating the attenuation required between the RF paths and the receiver inputs no allowance should be made for the duty cycle, as the power limit is governed by the compression level of the receiver, so only the peak signal level is considered, a reduction in the average power gives no benefit. The power rating of the attenuators themselves may be reduced however, this reduction becomes helpful at higher frequencies (above 20GHz) where loosely coupled probes suffer from poor directivity and high power attenuators are not available. A typical probe coupling factor is -10dB, while attenuators with power ratings above 1W could not be sourced. Considering the example above once more, we see that while measuring this part at 5W, 9W would be passing in the forward direction, so 0.9W would be coupled off and dissipated in the 1W attenuator, not only a rather inadequate

safety margin for such expensive components, but the temperature rise may alter the characteristics of the attenuators between calibration and measurement, giving rise to errors in the results.

At lower frequencies the parts being measured could well deliver several hundred Watts into very low impedances, even using broadband transformers as described in “High Power Active Harmonic Load-Pull System for Characterization of High Power 100Watt Transistors”, Aboush et al [14] this can require forward and reverse waves around 500Watts. Clearly it would be advantageous to reduce the loading on the test load and circulator, also the DC bias supply requirement, perhaps less obviously, the transformers and cables may also fail or change their properties under the thermal load of CW operation. Again the thermal load on the attenuators between the measurement couplers and the receiver ports would be excessive unless couplers with a coupling factor of at least 30dB could be used. While sourcing or fabricating such parts is straightforward below 10GHz, the 14 bit oscilloscope based measurement systems have a dynamic range around 45dB so accurate calibration with over 30dB of attenuation permanently in place would be challenging, however systems based on VNAs such as the R&S ZVA67 have much greater dynamic range, around 60dB, and could accommodate this.

6.2 Principle and Method of Operation.

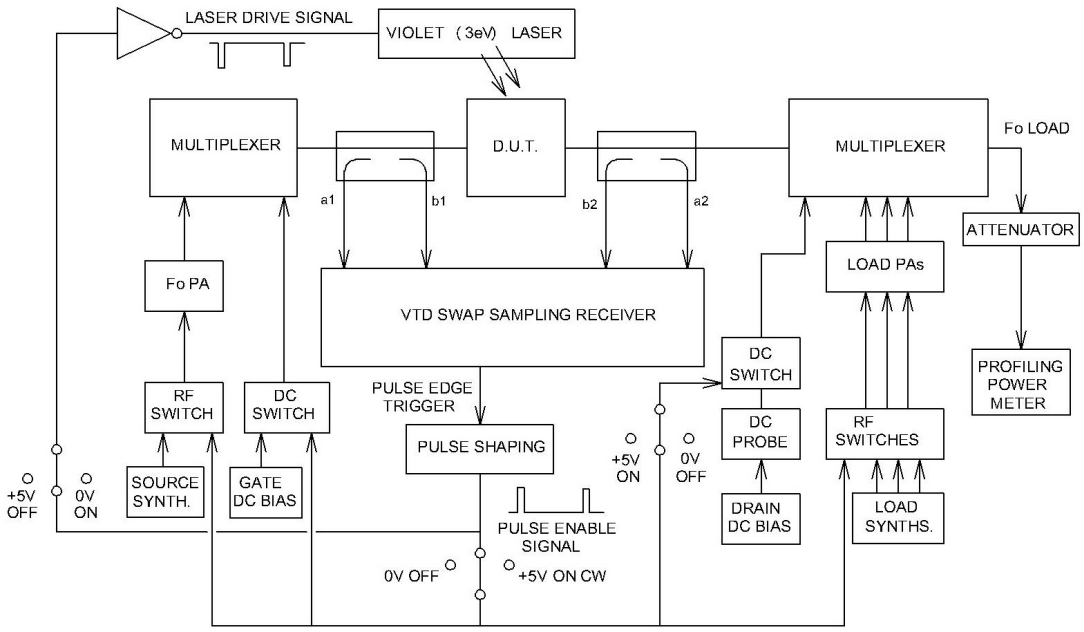

Figure 6.6 The pulsed Fully Active Harmonic Load Pull system.

The first pulsed FAHLP system was based upon a VTD SWAP receiver, this is a sampler based system and provides considerable control over the size and timing of the sampling, it is also capable of assembling a large record from a number of small samples, this flexibility combined with an external RF timing and switching circuit enables pulses as short as 1us to be used, with duty cycles ranging from 1/256 to continuous [18].

The VTD receiver outputs a falling edge trigger signal marking the beginning of each sampling period, this signal must be converted into a control signal to operate RF switches placed in each of the RF drive signal paths. With the addition of an inverter we also have the signal to operate the laser, as described in Chapter 3. Switches may also be placed in the DC bias feeds if required. A timing circuit was developed (presumably along similar lines to that used by VTD) which permits the active period of the pulse to be varied from 1us to 256us, so utilising the full capabilities of the VTD system. An important and useful feature is the changeover switch, this permits the RF operation to be changed from CW to pulse without making any changes to the sampling regime, and facilitates powering off the device. In this way a direct comparison can be made

between the two modes to confirm that the system is functioning correctly, fig. 6.7, and a simple way of simultaneously switching off all the RF drive signals is very useful in a FAHLP system. For a full description of the system see Appendix B.

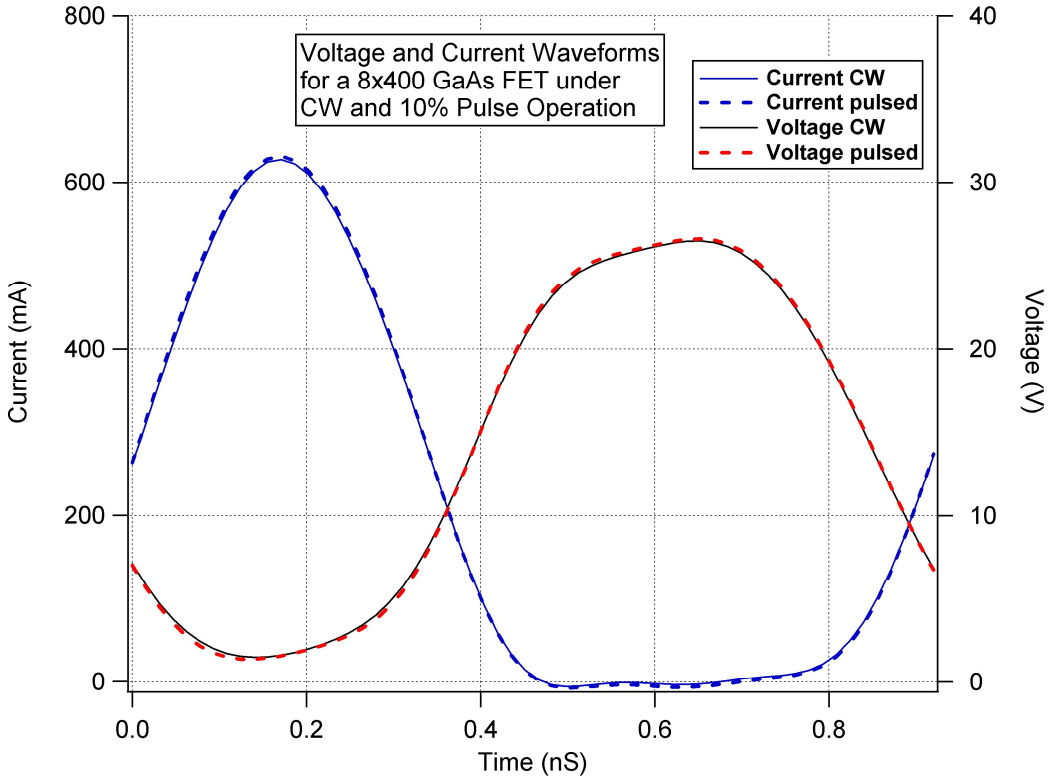

Figure 6.7 A 8x400 GaAs FET die measured under CW and 10% duty cycle pulse operation.

The ability to switch between pulse and CW also allows investigation into the thermal behaviour of the device under test, for example comparing differing device geometries, in fig. 6.8 below we see the performance of two 10x125 GaN die fabricated on the same wafer, but one has 25um finger spacing and the other 65um.

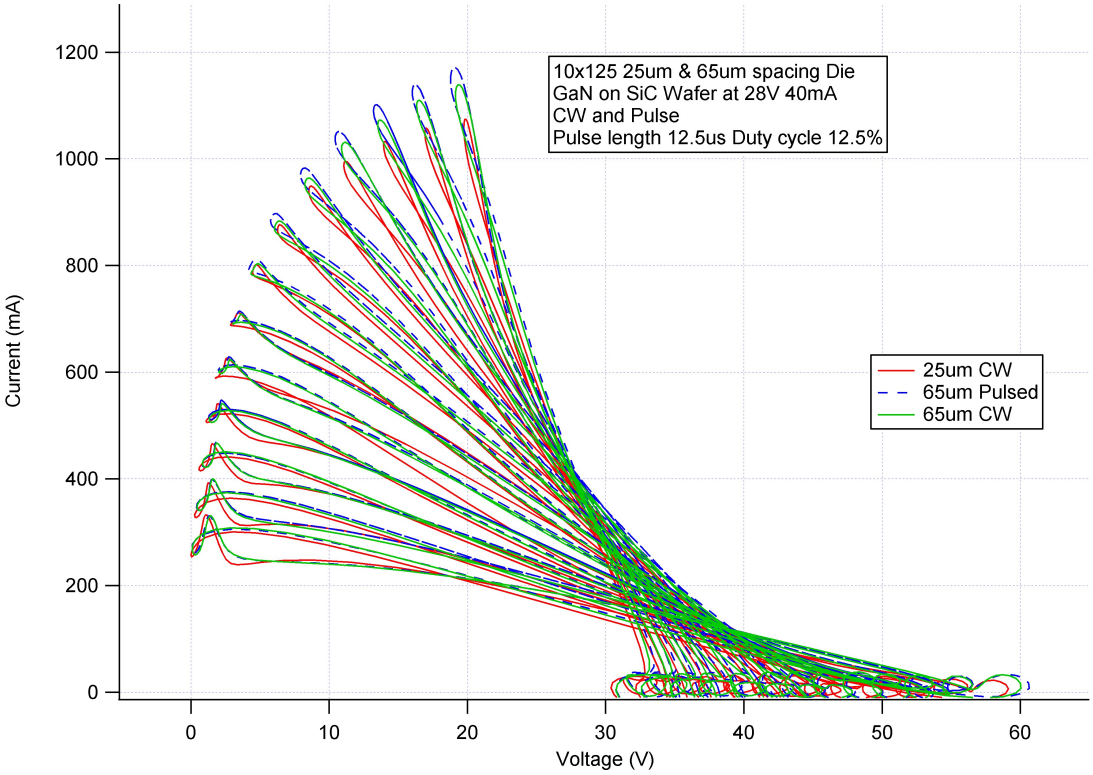

Fig 6.8 Fans diagrams showing RF load-line behaviour for 25um and 65um spaced Win 10x125 GaN on SiC die.

We see here the dynamic load-lines for a 900MHz drive signal as the load impedance is swept from a Γ of -0.6 to +0.6 in a 50 Ohm system. There is little difference between pulse and CW for the 65um part, so we can conclude that the finger spacing of 65um is adequate to allow good performance, however the 25um spaced device is showing significant collapse as the load drops below 50 Ohms under CW operation, switching to pulse mode fully restores the performance to the same level as the 65um part in pulse mode (load-lines not shown for clarity), so it can be safely concluded that the collapse is due to thermal effects. It may be that the advantage of smaller size and subsequent lower parasitic elements of the 25um part outweigh the loss of CW performance for a particular application, use of this equipment makes an informed decision possible.

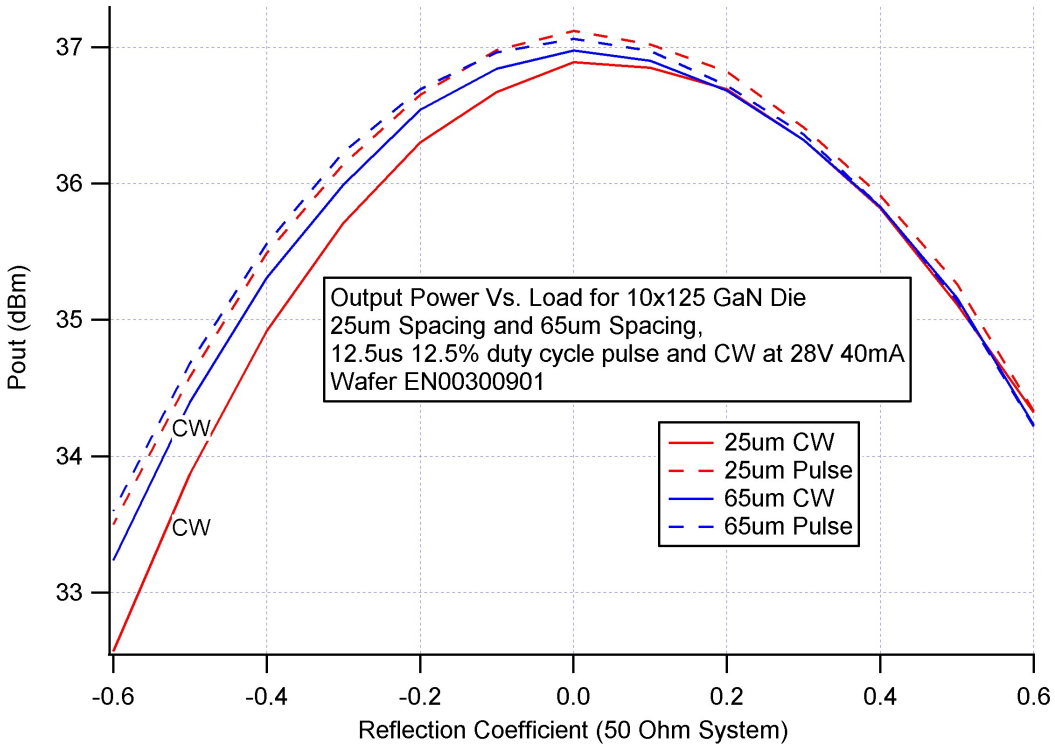

Figure 6.9 Output power against reflection coefficient under CW and Pulse conditions.

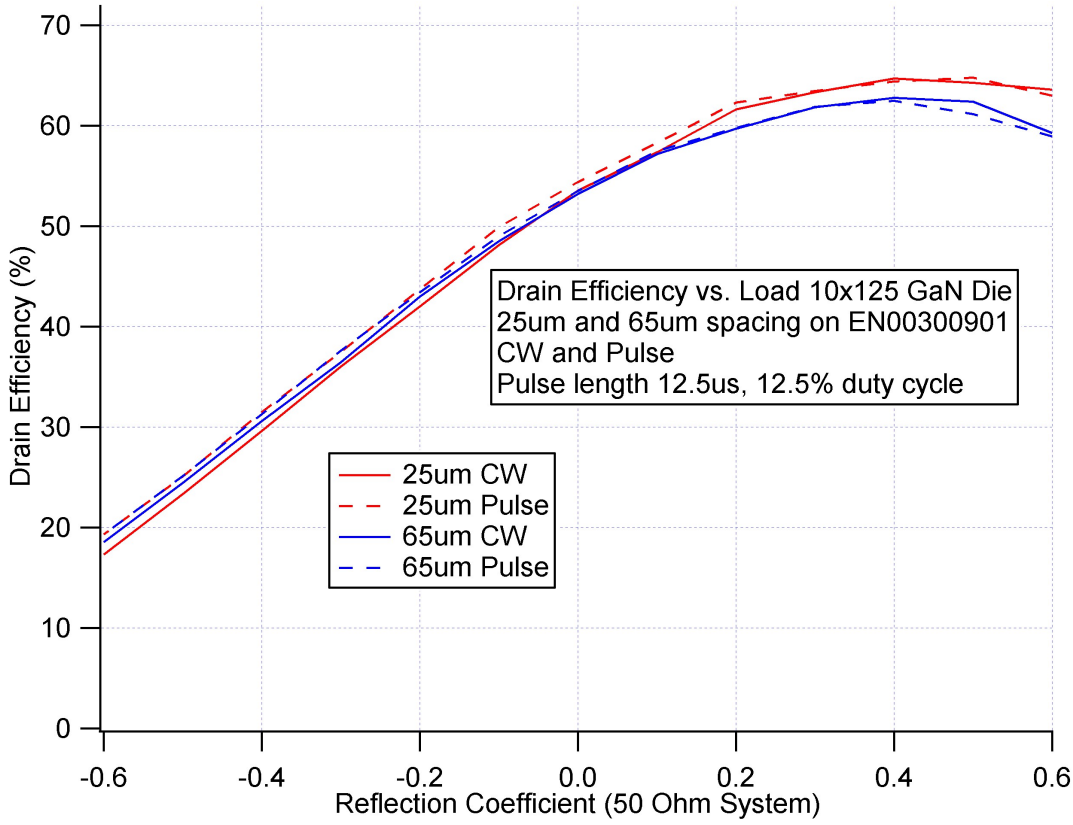

Figure 6.10 Drain Efficiency vs. Reflection Coefficient.

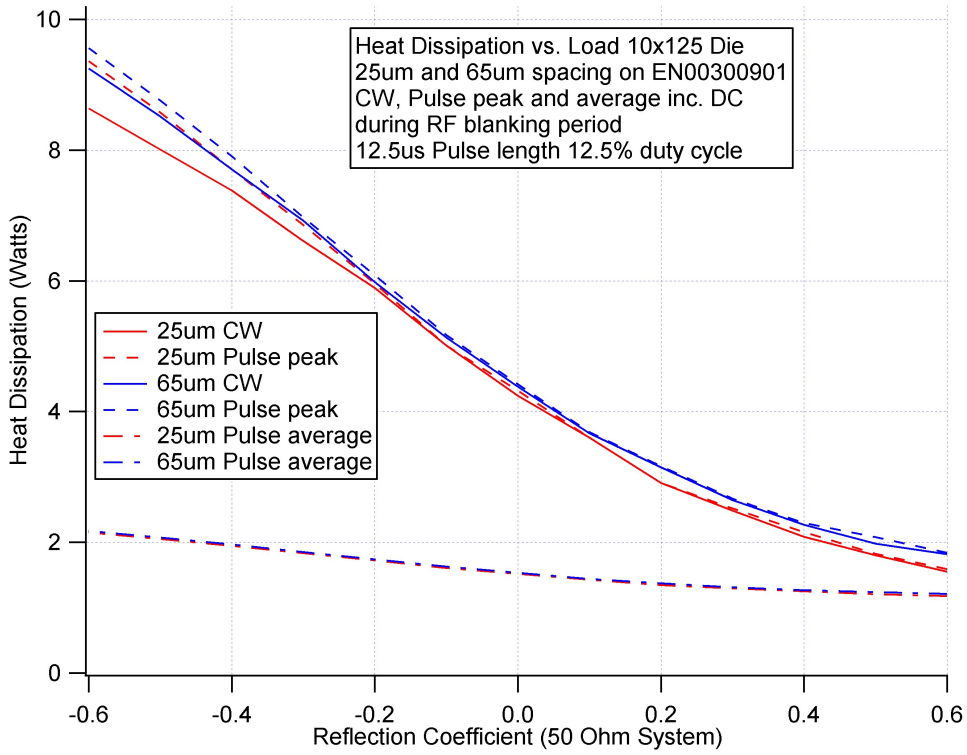

Figure 6.11 Thermal Dissipation vs. Reflection Coefficient.

If we take a slice along the real axis of the Smith Chart (figs. 6.9, 6.10 and 6.11 above) we see the output power, drain efficiency and heat dissipation changing with the load impedance, it is apparent that the thermal collapse is only significant well away from the optimum region (0 to +0.2), confirming that it is reasonable to say that the 25um spacing is adequate for most applications.

Figure 6.11 clearly illustrates the thermal advantage of a pulsed system for exploring the outer bounds of the devices behaviour, while the peak dissipation in pulse mode is slightly higher due to the higher output power, the average power is greatly reduced, from a thermal perspective it would be quite safe to investigate loads below -0.6 gamma. Note that the average values include DC dissipation during RF off periods.

For applications with a high peak to average power ratio and complex systems such as envelope tracking the heat dissipation can be kept low, but even so if linearity is important and it is necessary to pre-distort the input signal to correct the output waveform, then in order to do this optimally the time constant of the thermal performance must be known, the pulsed AHLP can extract this by measuring the decay along the pulse crest with the profiling power meter (Ladybug 870A).

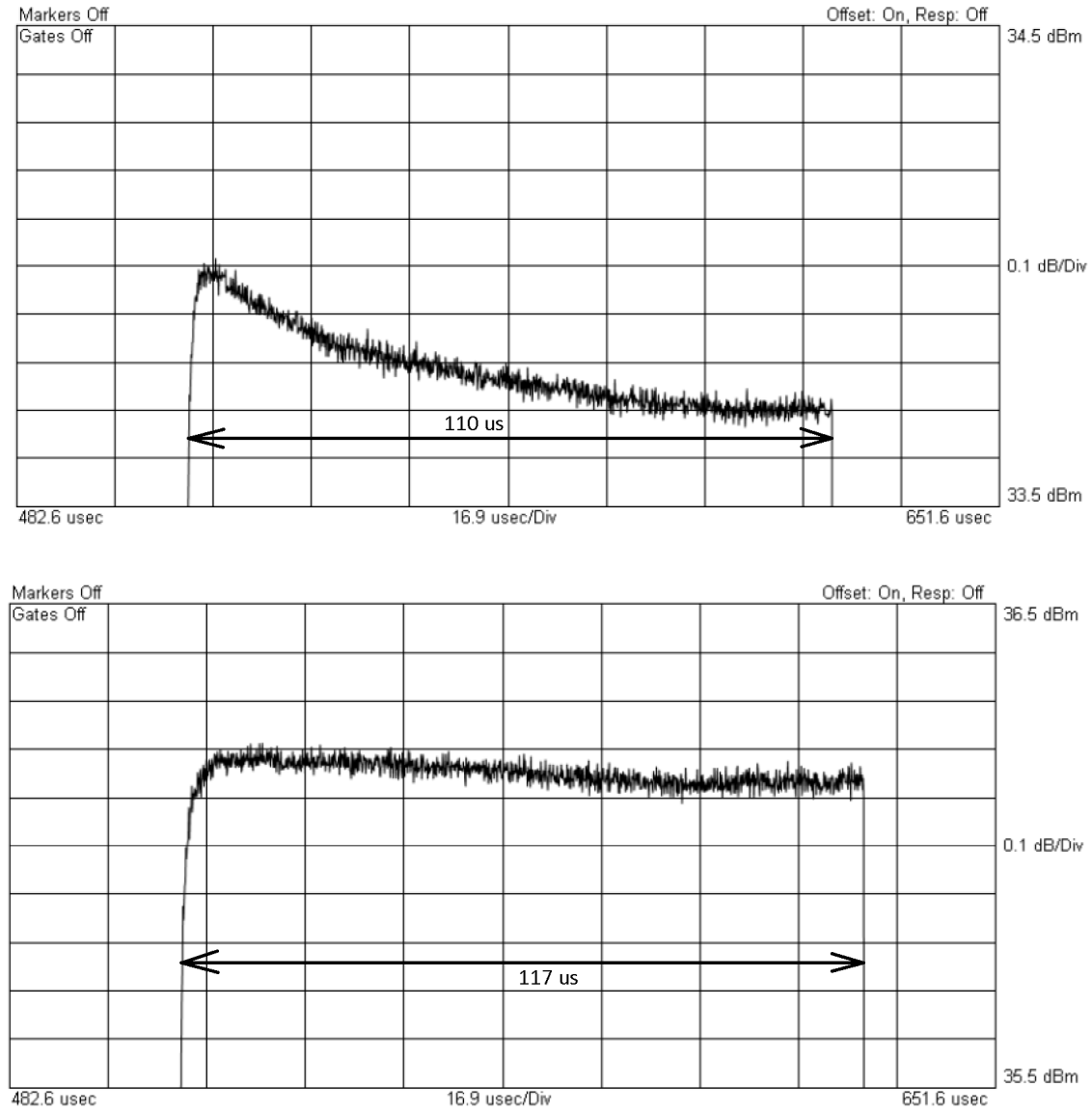

Figure 6.12 Relative output power against time 10x125 25um GaN die, mismatched and matched.

For the graphs reproduced above (fig. 6.12) the overall pulse time was lengthened to 256uS, and the pulse period increased until the performance was stable, it can be seen that this takes around 90uSec. The effect of mismatching on the profile of the pulse can clearly be seen, this may be of vital importance if designing a pulsed system where the load is not tightly controlled – either through changing external circumstances or perhaps in a wideband unit where optimum loading cannot be maintained across the full band. Potentially a system could fail overall acceptance if the extra thermal droop is not acknowledged during the early design stages, by using a pulsed load pull system to fully characterise the device, expensive rework and delays can be avoided.

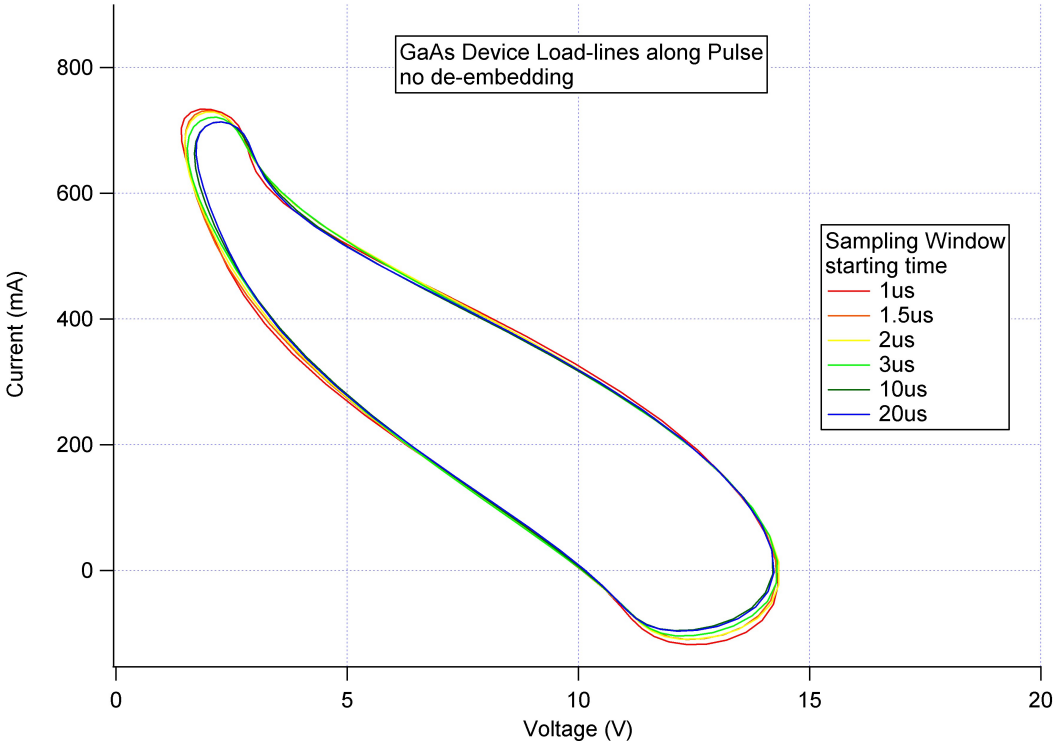

Figure 6.13 Load-lines for a GaAs device measured along a pulse.

As mentioned earlier, a potentially useful feature of the VTD SWAP is its ability to move a narrow measurement window along a pulse, fig 6.13 shows loadlines measured along a pulse for a GaAs die, the reduction in power with time is clearly visible, and is evenly balanced at the two extremes of the lines. Examining such plots may well shed light on the root cause of the droop, should the DC centre be changing or the distortion be predominantly at one end of the line.

6.3 Pulsed Measurements at Higher Fundamental Frequencies.

The VTD SWAP based system can only measure up to 18GHz, so to make pulsed harmonic measurements at X band and above something else is needed. The new Rohde & Schwarz ZVA 67 network analyser not only contains four phase locked sources and eight receiver channels, but it can also sample in pulse mode. It is unable to stitch multiple samples together however, so using a short pulse duration will result in a loss of dynamic range [18]. Fortunately the ZVA has excellent dynamic range in CW mode, generally permitting calibration with the attenuation needed for full power operation left in situ, so even though the increase in measurement bandwidth needed to operate in

pulse mode (200KHz for a 10us active RF window, compared to 100Hz or even 10Hz for CW) degrades the noise floor it is still possible to make useful measurements, with the application of averaging, fig 6.14. The construction of a system based on the ZVA67, and also one using an Agilent PNA-X VNA, is discussed in Appendix B.

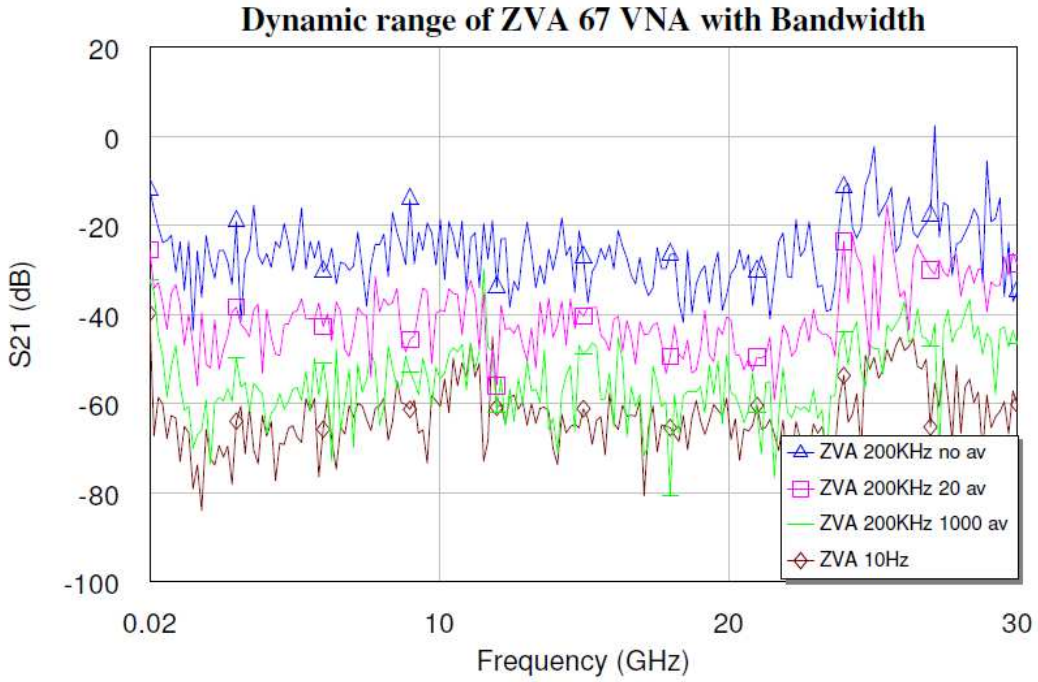

Figure 6.14 S_{21} Noise floor - Dynamic range variation of a ZVA 67 with bandwidth and averaging. Coupling factor to main line is 50dB.

To prove the accuracy of the measurements a series of test were carried out with the ZVA and SWAP systems on a Win Semiconductor Corporation 10x125 GaN on SiC HFET, fig 6.15, the power and efficiency optimums of which straddle 50 ohms, allowing direct measurement of the voltage waveform with a Tektronix sampling oscilloscope as well as via the measurement system samplers [25].

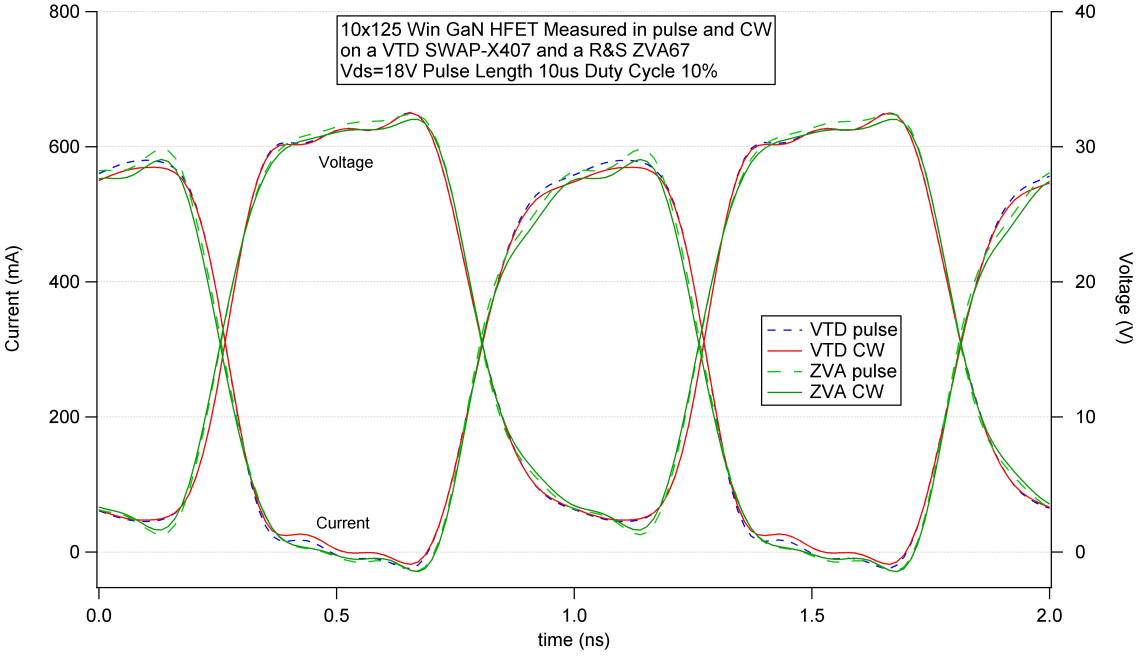

Figure 6.15 Comparison of output current and voltage waveforms of a 10x125 GaN HFET, measured in pulse and CW on a VTD SWAP-X407, a R&S ZVA67 and a Tektronix DSA8200.

Allowing for the slight differences in the load impedances at the higher harmonics we see excellent agreement. The VTD and ZVA waves are all aligned by the phase of the input voltage wave, so the measurement of propagation delay is also very consistent.

6.4 Output Characteristic Measurement.

A technique which has begun to be exploited is the measurement of the output characteristics of devices by using an active load pull system to inject a reverse wave at the fundamental, with no stimulus at the input. The subsequent response at the fundamental and the harmonics reveals a great deal about the non-linear behaviour caused by the output varactor. It has proved possible to actively load pull the second harmonic signal generated by the varactor, so the effect upon the fundamental can be conveniently analysed.

Figure 6.16 below shows the response of an LDMOS part, with the second harmonic load impedance pulled to the value previously found to give optimum efficiency in normal operation, and enough reverse fundamental power supplied to generate the appropriate voltage excursion. Clearly a significant amount of energy is being

transferred to the second harmonic, which must reduce the efficiency in normal operation, this test shows conclusively that this energy transfer is caused by the output section of the device, presumably the varactor inherent in the design.

While it is not essential to carry out this test under pulse conditions, it does involve injecting substantially more reverse power than normal loadpull measurements, therefore it is prudent to use a pulse set up to reduce the risk of damage to the device and the test equipment.

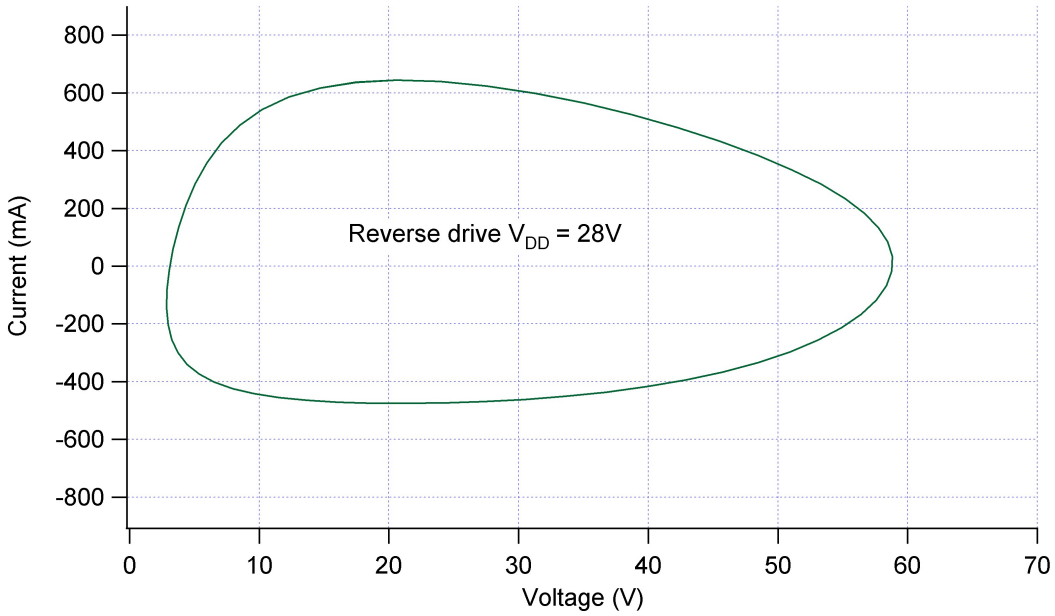

Figure 6.16 The output characteristic of an LDMOS device subjected to reversed power drive.

While GaN HEMTS do not suffer from this problem, the reverse wave injection technique does allow us to examine the capacitive current flowing in the output circuit under high power conditions. Figure 6.17 shows the effect of de-embedding a 0.2pF capacitor from a UMS 4x100 device. The capacitance can be determined in other ways of course, notably from small signal measurements, this high power method has the advantage that it can be done with the same test set up as the RF characterisation.

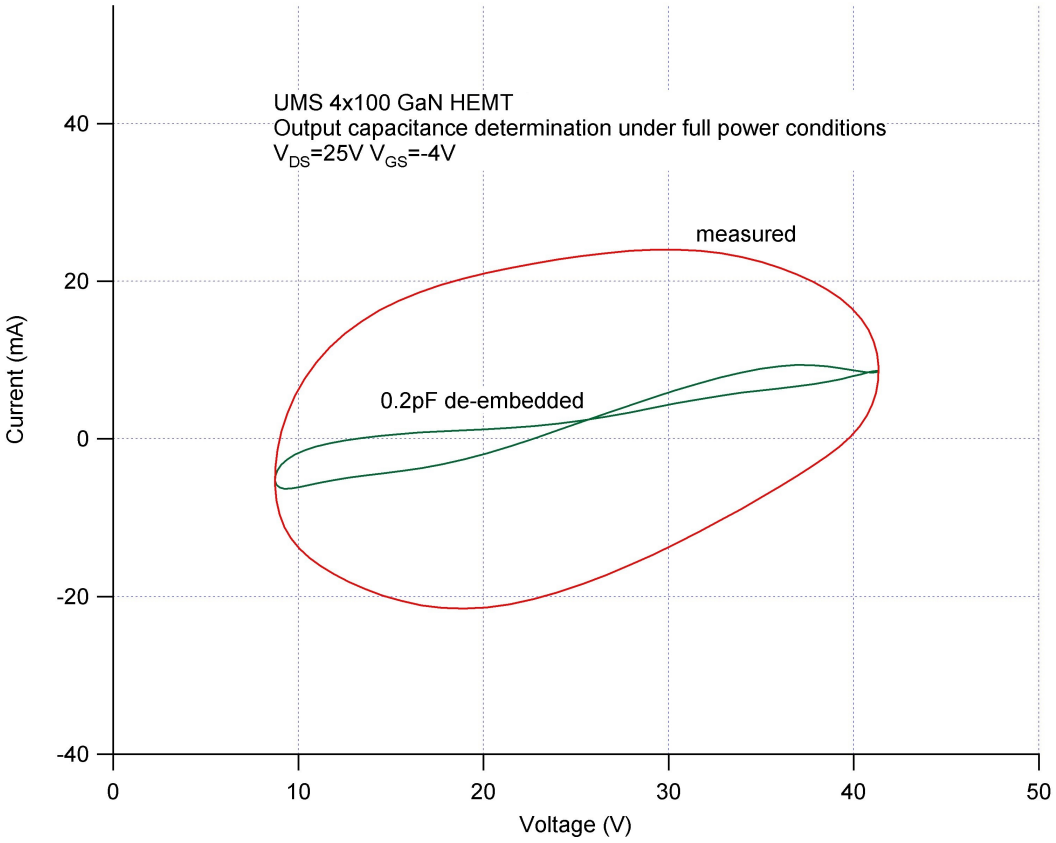

Figure 6.17 Using Reverse Power Injection to determine effective Output Capacitance under high power conditions.

6.5 Conclusions.

It has been shown in this chapter that not only is pulsed Fully Active Harmonic Loadpull a practical technique, it offers a number of important advantages over both CW FAHL and pulsed passive loadpull systems:

1 The area of the Smith Chart where the device can be operated is greatly extended, reducing the risk of damage to the device and test equipment

2 The device may be stressed beyond its continuous limits, essential for gathering data for pulsed operation, modulated bias systems such as Envelope Tracking, and some high peak to average power ratio systems.

3 By contrasting CW and pulse performance the thermal properties of devices can be measured and compared, allowing designers to make informed decisions.

4 The maximum operating power level of the system can be increased, important for low frequency high power devices, and for high frequency devices where component size and hence power rating is restricted by the wavelength.

The reduced power dissipation enables novel tests such as reversed drive to be carried out with minimised risk, helping to shed new light on device behaviour.

It has also been suggested that, in order to gather full data for device modelling, negative slope load-lines could be used to map the top right hand quadrant of the I-V plane where high voltages and high currents are both present. The very high power dissipation involved would certainly damage the majority of devices if attempted in a continuous mode, it is possible that by operating in a low duty cycle pulse mode these regions could be explored.

It has been shown that accurate pulsed FAHLP systems can be implemented using both time domain sampler based and frequency domain VNA receivers.

Chapter 7 Harmonic Measurements & Dynamic Range

7.1 Improving the Accuracy of Harmonic Measurements over Significant Dynamic Range.

The Waveform Engineering techniques pioneered at Cardiff can only realise their full potential if accurate measurements can be made of the harmonic components of the waveforms. Care must be taken that the receivers are not compressing and so introducing their own harmonic products, and that the signal levels are high enough to escape the noise floor of the system (see "Very small duty cycles for time domain transistor characterization," de Groote et al [18] for a detailed treatment). For measurements over a small range of input drive power this is fairly simple, careful calculation of the attenuation required to be placed between the receivers and the directional couplers is all that is required, to give good results.

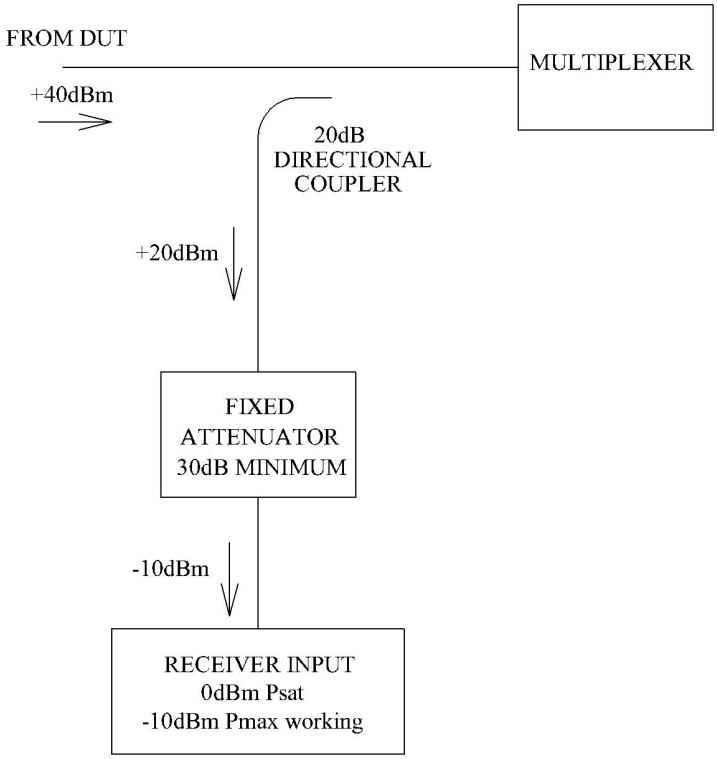

Figure 7.1 Example calculation of the minimum permissible attenuation.

In the example shown in fig. 7.1, in order to calculate the attenuation required to reduce the +40dBm signal travelling through the main line to the -10dBm maximum level

acceptable at the receiver port, the required power in dBm is simply subtracted from the starting power,

So Attenuation = +40 - (-10) = 50dB

If we assume the directional coupler has a coupling factor of 20dB then a further 30dB must be added to protect the receiver and give accurate results.

It is most important to bear in mind when performing this calculation that if the load impedance is being pulled significantly away from the characteristic impedance of the system, the power travelling along the mainline will be much higher than the net output power of the device, since

$$P_{OUT} = P^{+} - P^{-}$$

If this is overlooked then the receiver may well be overloaded, leading to inaccurate results and even permanent damage to the equipment.

The situation becomes more complicated when we wish to make measurements over a significant range of fundamental input powers, a necessity for generating useful measurement based look up table models for system design. With GaAs devices the issue was still controllable, the straightforward compression behaviour of such devices means that a 10dB range of fundamental power is all that is required, there being no notable change in behaviour with further reduction in power. Once again GaN devices introduce a new problem, the soft compression characteristic of these parts means that a 20dB power range is a realistic minimum, fig 7.2.

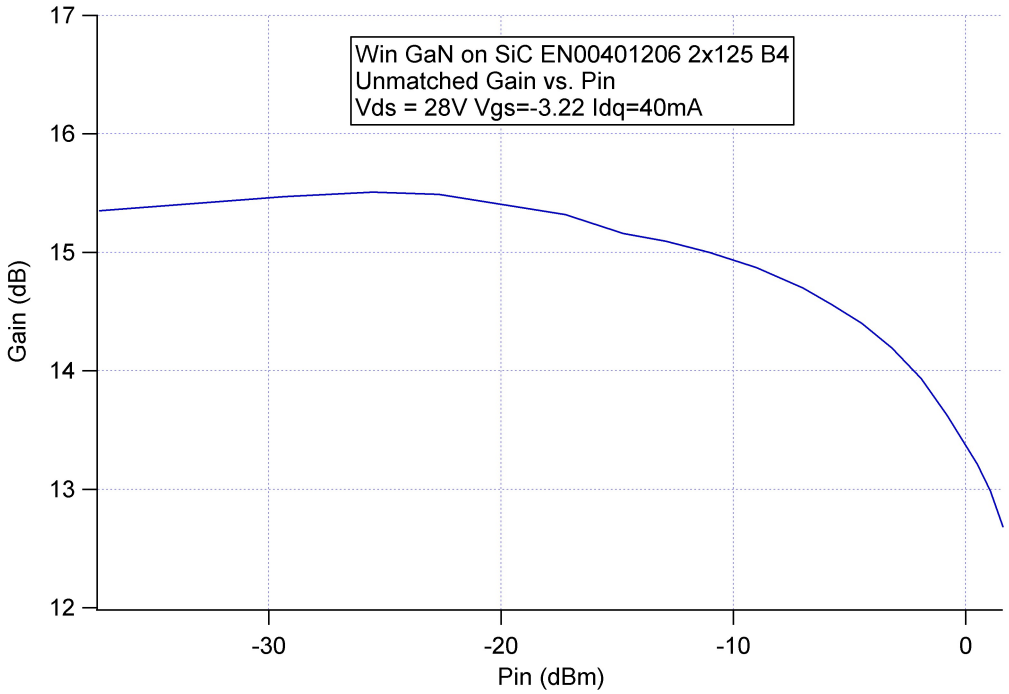

Figure 7.2 The "soft" compression typical of GaN devices.

If our receiver has a 60 dB range between saturation and the noise floor, and we position the maximum fundamental power 10 dB below saturation, then with a 20 dB reduction in drive power, and the load moved to give up to a 3dB reduction in gain, our fundamental is only 27dB above the noise floor. The harmonic components of the waveforms will have reduced at a faster rate than the fundamental according to their order, at twice the rate for $2f_o$, three times for $3f_0$, four times for $4f_0$ and five times for $5f_0$, in line with intercept point theory, therefore they will be below the noise floor. Figure 7.3 shows the measured harmonic output levels from a UMS 8x150 GaN device measured on the R&S ZVA system at 5.4GHz. Despite the excellent dynamic range of this system in CW mode, $5f_0$ is only measurable over a 10dB range of input power, operation in pulse mode would reduce the dynamic range of this VNA based system, (chapter 6,[6],[18]). Figure 7.4 shows the reduction in dynamic range resulting from increasing the bandwidth from 10Hz to 200KHz, necessary to perform measurements inside a 10µs pulse, at least 500 averages are needed to recover most of the information.

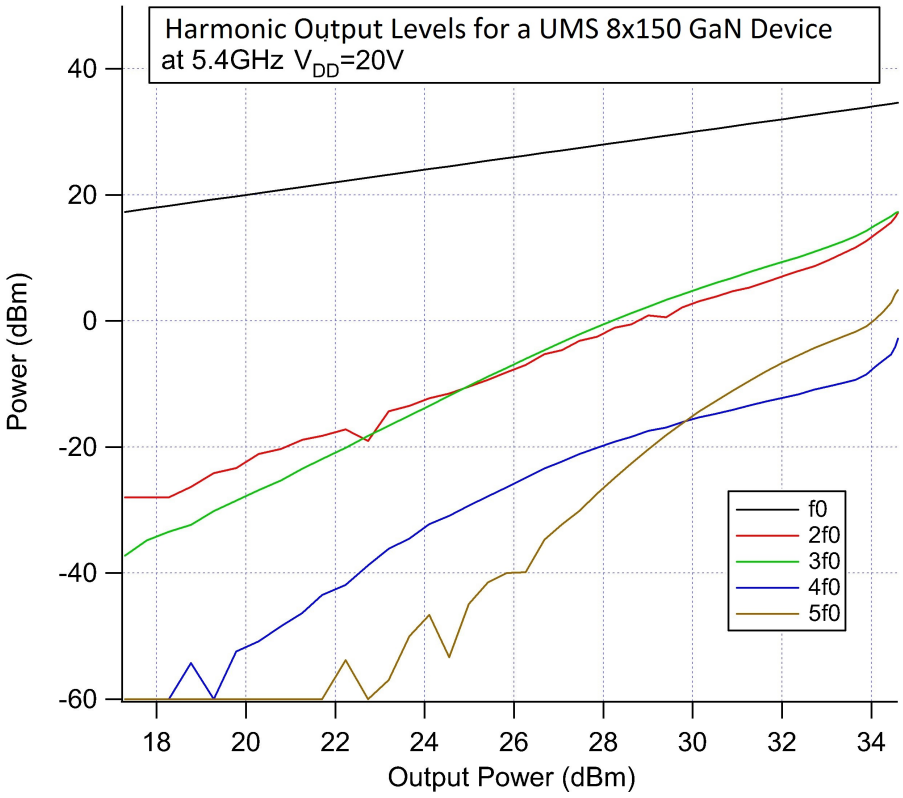

Figure 7.3 Harmonic output levels from a UMS 8x150 GaN device (R&S ZVA).

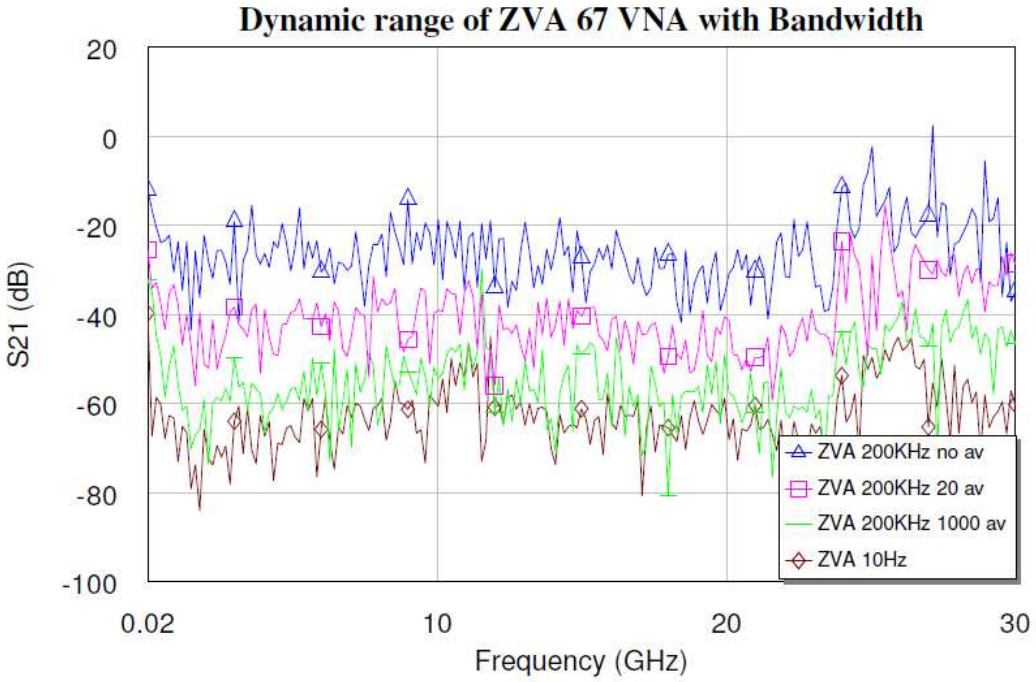

Figure 7.4 Dynamic range variation of a ZVA 67 with bandwidth and averaging. Input power +10dBm, coupling factor to main line is 50dB.

The calculations performed on the measured b_2 transmission waves also involve the a_2 reflection wave, which is nominally zero if the termination is 50Ω, noise on this signal will scatter the apparent termination value before b_2 properly hits the noise floor, causing problems converging on the target if under active control and potentially disrupting simulators trying to use the data subsequently. The problem is not insurmountable, the simplest solution being to change the attenuation level as the power level is changed, however this is time consuming and prevents a fully automated measurement sequence, there is also a greater risk of operator error damaging the equipment or producing invalid results.

Introducing a positive frequency response slope into the receiver path is an obvious improvement, and this can be effected, for example, by the vestigial loop couplers utilised by VTD, [26] or by using a much higher frequency λ/4 hybrid operating below its nominal working band, as in figure 7.5.

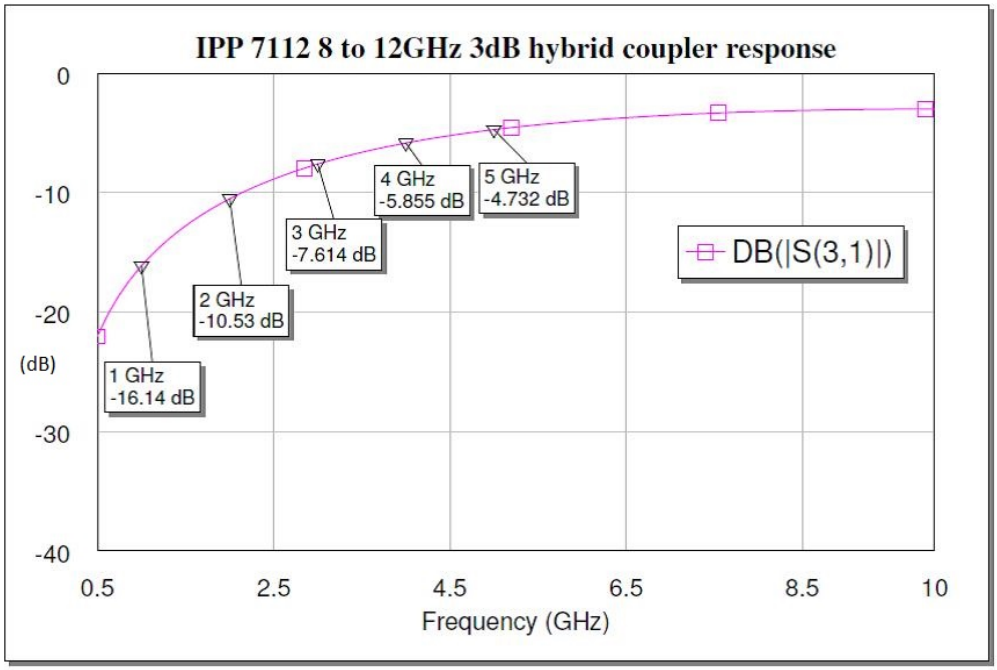

Figure 7.5 Wideband response of an 8-12GHz 3dB hybrid which could be used for equalisation at lower frequencies.

An equalising system with a sloping characteristic is however fundamentally vulnerable to drift, and ones choice of slope tends to be limited. The solution presented here overcomes these problems, possessing a stepped characteristic less prone to drift, and allowing the ratios of the steps to be chosen at will.

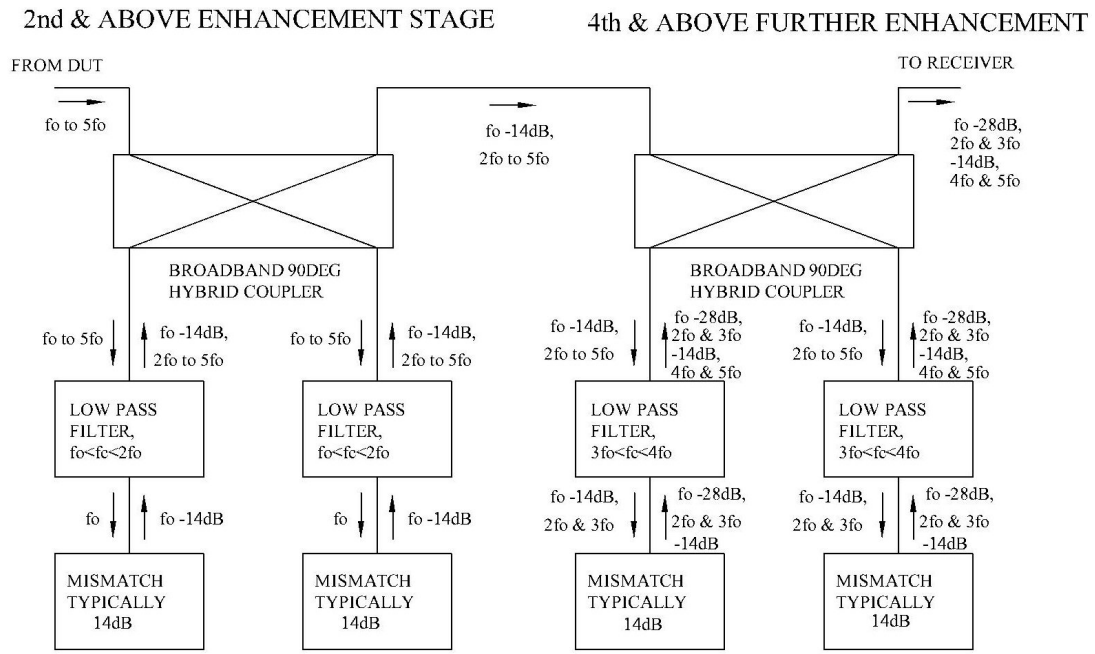

Figure 7.6 A stepped response attenuator for dynamic range compression.

The signal to be analysed is normally passed through a fixed value attenuator selected such that the signal entering the receiver is at the optimum level. In order to attenuate the fundamental without affecting the harmonics a wideband hybrid coupler is used (fig. 7.6), the signal from the sampling directional coupler is passed into one port, causing it to split and appear equally at both of the coupled ports. Each coupled port is fitted with a low pass filter, with a cut-off frequency such that the fundamental passes through but the harmonics are reflected back.

Considering the harmonics first, they are reflected back from the filters into the coupler in the correct phase and amplitude relationship to recombine and emerge from the fourth port of the coupler, attenuated only by the incidental insertion losses of the coupler and filters. The coupler fourth port is then connected to the receiver input (fig.7.6 shows this passing to a second stage to further enhance the higher harmonics).

The split fundamental signals pass through the filters, to the output of each filter is fitted a mismatched load in order to reflect a specific proportion of the fundamental back towards the coupler. In this way the fundamental signals re-enter the coupler where they recombine and emerge from the fourth port of the coupler, joined with the harmonics once again, but now reduced in relative amplitude by the value of the return loss of the mismatched loads. The effect is illustrated for a range of load values in fig. 7.7.

Considering the first stage of the diagram, utilising 33.3 ohm loads which give a VSWR of 1.5:1 which is return loss of 14dB, then the fundamental will be attenuated by a nominal 14dB, now if we reduce the fixed attenuator by 14dB to maintain the fundamental level at the receiver at the same level as before, we have effectively lowered the noise floor for the harmonics by 14 dB.

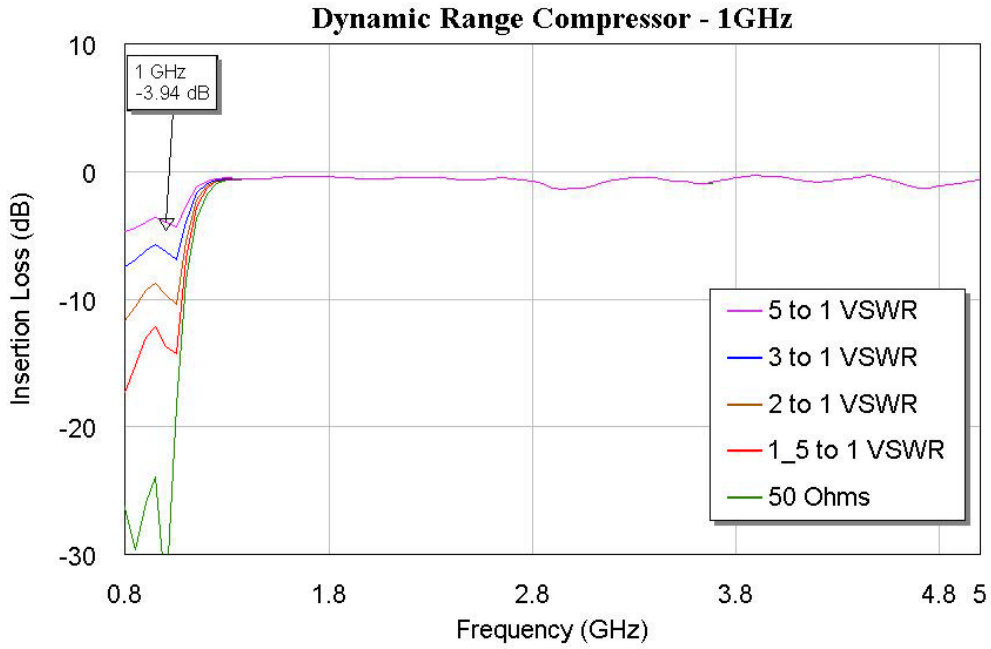

Figure 7.7 The effect of various loads on the selective attenuation.

If we were able to utilise ideal components then we would have full control of the relative levels of the components, however, since real hybrid couplers do not possess infinite isolation, trying to introduce more than 20dB of adjustment with a single stage will be problematic, the leakage from the input to the output port will be similar in magnitude to the signal reflected from the mismatches, giving rise to destructive or constructive interference which will be frequency dependant, this effect can be seen in the lower traces of fig. 7.7.

In fig. 7.6 the process is taken a step further by adding a second stage to further enhance the higher harmonics in particular, this could also be used to further enhance the second and third whilst maintaining a flat fundamental band response, but this is not an essential feature for most situations. For the example shown in fig. 7.1, the two stage circuit would have a nominal attenuation of 28dB at f_0, requiring a further 2dB to avoid

compression in the receiver, in practice the insertion loss of the various couplers and filters would be likely to add this amount of attenuation.

7.2 Conclusions.

The large dynamic range needed to adequately capture the behaviour of GaN HFET devices cannot easily be achieved by a system with a flat frequency response, to capture accurate harmonic information at the lower power levels some form of equalisation is required, or the system must be reconfigured between the high and low power measurements. When a VNA based system is operated in pulse mode the dynamic range of the receivers is greatly reduced by the need to shorten the sampling window to fit within the "RF ON" period of the pulse [18], this can be recovered to some degree by the use of averaging but there is still a reduction in performance. The use of equalisation techniques such as that described here will give much improved harmonic measurements, particularly when measuring across a significant range of fundamental frequency powers.

Sampler based systems such as the VTD SWAP can maintain their dynamic range by assembling a large record from a number of different pulses [18], at the expense of measurement speed. Use of a dynamic range compressor such as that described here will permit either enhanced dynamic range or shorter measurement times.

Chapter 8 Combined Optical and RF Measurements

8.1 Hot Electron Electroluminescence under RF Operation.

In Chapters 3 and 5 it was shown that photons of the appropriate energy can influence the trapped charges of a GaN device, it is also known that devices can emit photons, and a number of measurements were undertaken in collaboration with Bristol University, investigating electroluminescence of hot electrons in AlGaN/GaN HEMTs under RF operation [27]. While these were successful, being the first reported measurement of electroluminescence under RF operation, some practical difficulties had to be overcome as most modern GaN devices have a source coupled field plate over the gate region, and devices with more than two channels will usually have air bridges to ground the inner source conductors, effectively blocking light to and from a substantial proportion of the channel. Since the SiC wafer is transparent it is possible to illuminate from the underside, which ensures full exposure for trap clearing, and to gather sufficient light for accurate spectroscopy on the electroluminescence, measurement from the underside is essential.

The Renishaw InVia spectrometer which was used for the spectral analysis is a physically large instrument which requires extensive in-situ alignment, necessitating assembling the RF equipment around it. The immediate practical solution was to employ a cast iron 90^{o} angle plate with a hole through the vertical face, permitting the wafer to be mounted vertically, and the spectrometer to be focussed on the reverse substrate face of the die, while the wafer probes contact the front face. While feasible, this arrangement has a number of drawbacks. Secure yet easily moved probe mounts must be provided, also a microscope viewing the top face to enable the placement of the probe tips on the die pads. In view of the success of the measurements, and some other possible applications, it was decided to design and assemble a specialised Opto-RF wafer station, intended from the outset to give simultaneous access to both sides of the wafer, and to facilitate active harmonic load pull control during optical measurements.

In a typical commercial wafer probe station no thought at all is given to the possibility of rear access to the die, the X-Y table and vacuum chuck essential for rapid testing of whole wafers precludes such access, and even if they are removed the substantial base plate of the station itself is too close to the measurement plane to allow a microscope

and camera to be fitted between them. In an attempt to overcome this problem the objective mount and camera adaptor seen in fig 8.1 was made.

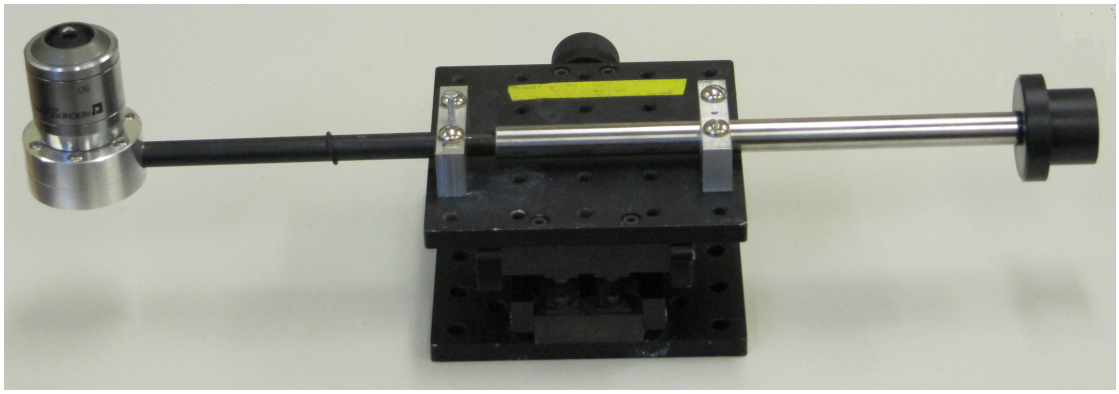

Figure 8.1 An inverted objective mount and camera adaptor.

Traditionally microscope objective lens were made so as to form the magnified image approximately 160mm behind the lens, so that objectives could be interchanged with ease, facilitated by the adoption of a common thread of outer diameter of 0.7626 inches and 36 threads per inch, known as “Society Thread” after the Royal Microscopical Society of London. The standard survived from 1839 until late into the 20th century, with mechanically compatible German and Japanese standards being developed, but with the electronic age came a requirement to route the light to different receivers, impractical with such a short predetermined focal length. The solution was to change to “infinity corrected” objectives which do not project an image, an extra “tube lens” must be inserted to create the image, this method has the advantage that the distance between the objective and this tube lens can be varied at will, permitting movable mirrors to be used to “switch” the light if required. In the mount shown here full advantage is taken of this design change, a surface silvered mirror is mounted at 45° below the objective, and directs the light along the tube into the camera lens. Focus adjustment is performed by means of the “lab jack”.

The objective used was a Reichert-Jung x50 ideally suited for this task, fig. 8.2, as its markings show it is fully corrected (Plan, Epi), produces a parallel light beam output (∞,0) and has a long working distance (LWD), which is essential as the lens must be focussed through the wafer substrate. Originally intended for florescence work, it is a concentric design, with a secondary optical system around the outside of the actual objective to permit the stimulating light to be directed at the sample, for the intended

application this can be used to direct light for trap clearing purposes. An interchangeable x10 example was also obtained.

Figure 8.2 The Reichert-Jung x50 objective lens.

By replacing the vacuum chuck with a platform mounted on pillars it was possible to install this assembly on a Signatone probe station, fig. 8.3, it can be seen that the result is rather congested. The adjustment of the lab jack proved to be too coarse for practical use, it was extremely difficult to focus, and this arrangement entails moving the entire camera assembly, precluding an extra camera mount, the result being rather too mechanically unstable for this precision application. Nevertheless some images of the underside of a Win GaN on SiC die were obtained, using a Sony NEX-5 camera with a 200mm zoom lens, Fig 8.4. The concept of using a fixed X,Y camera and moving everything else to suit it was validated, of course, once set the wafer probes and topside microscope do not need to move either, it is only necessary to position the die sample precisely.

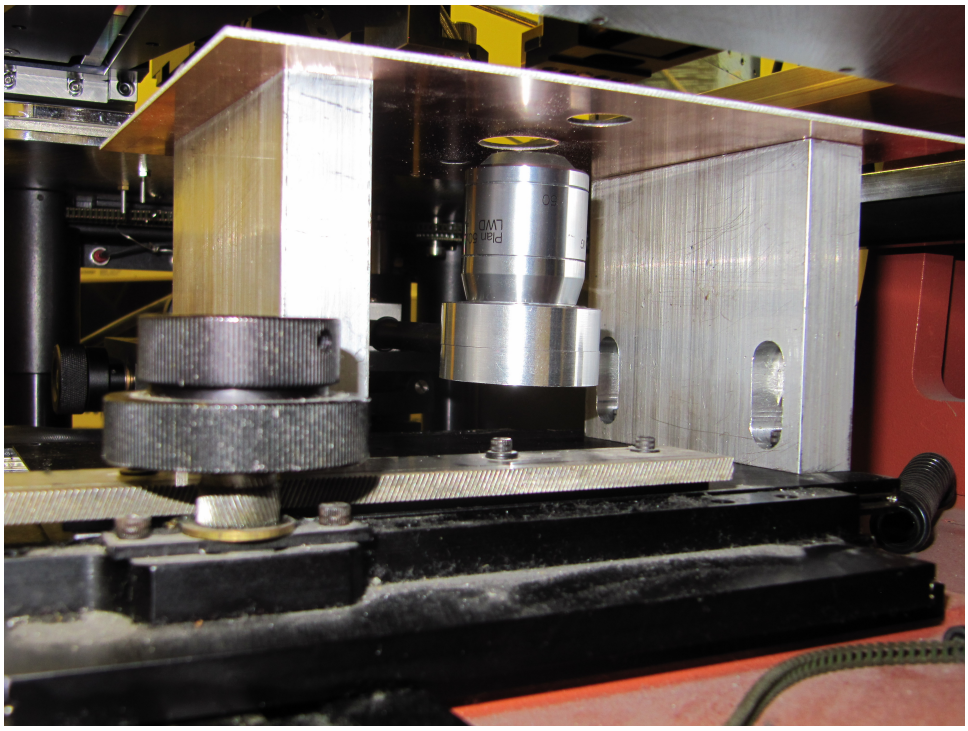

Figure 8.3 The Reichert-Jung objective mount on a Signatone probe station.

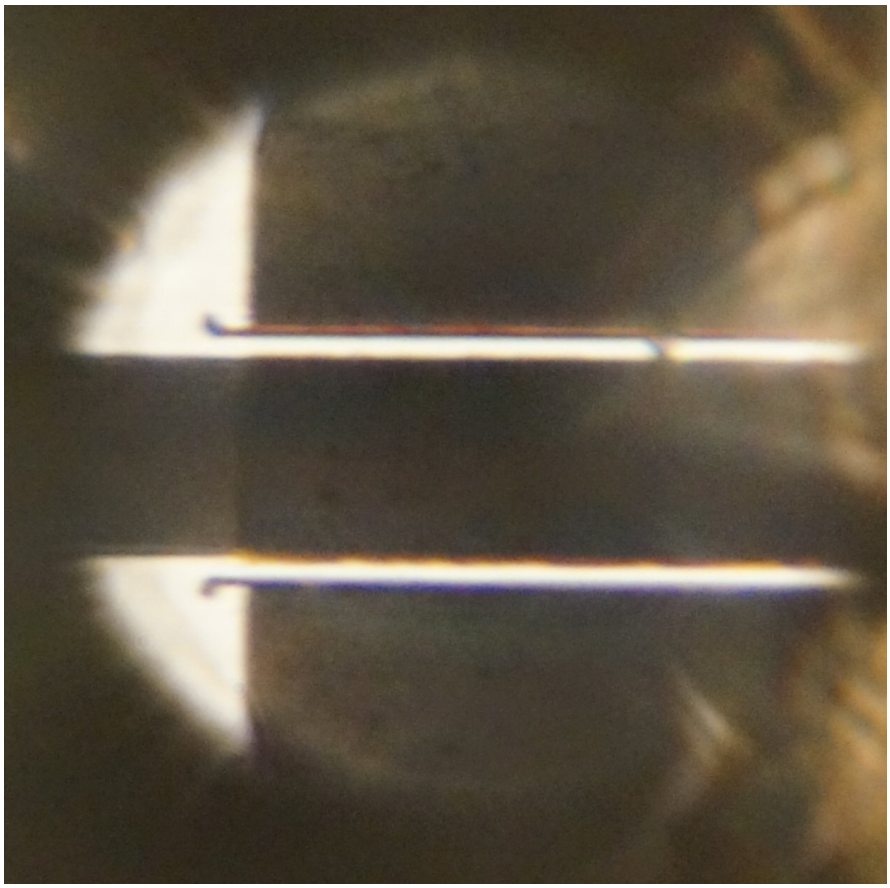

Figure 8.4 The reverse side of a Win GaN on SiC HEMT. The gate/source separation can just be seen on the top channel.

8.2 The Optical & RF Wafer Probe Station.

Following this work it was concluded that a complete redesign was needed, with rear access considered from the outset, the result is shown below in fig. 8.5.

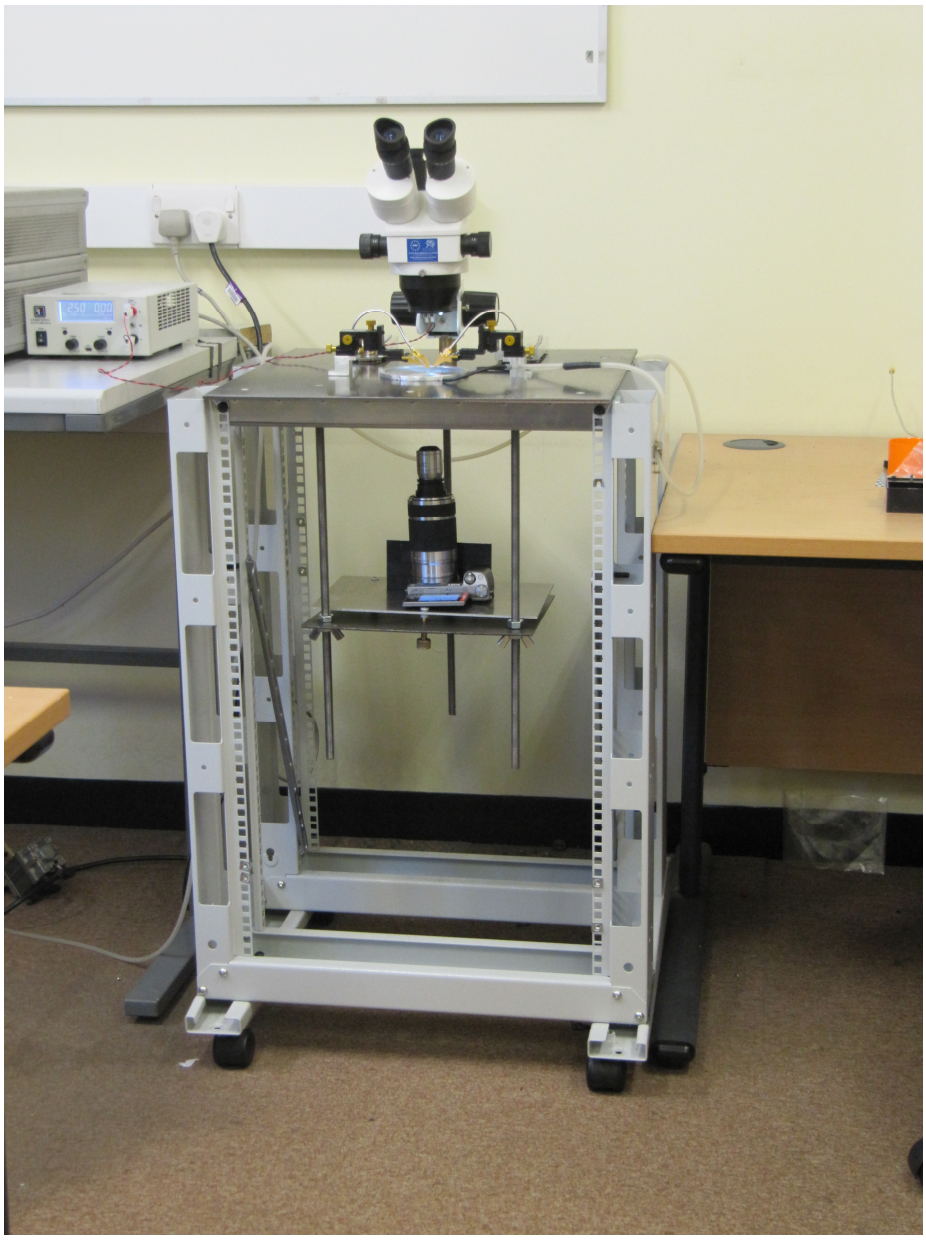

Figure 8.5 The combined Opto/RF probe station, with a Sony NEX5 camera and the Reichert - Jung 50x objective lens.

A 6mm mild steel plate forms the main deck, a 40mm hole allows the objective to pass through from the underside, while the optical top side microscope and the micropositioners for the wafer probes are securely bolted down around the hole. Three 500 mm lengths of M12 studding are screwed into the deck, projecting down and supporting the camera platform, the height of this platform can easily be adjusted allowing a wide range of equipment to be installed as required.

In order to allow a fine focus adjustment a third focus platform is held above the camera platform by means of three very fine pitched brass screws, (M8 x 0.5) with 19mm diameter knurled knobs, making adjustments smaller than 0.1mm quite practical. It is also possible to aim the objective by contra-rotating the screws.

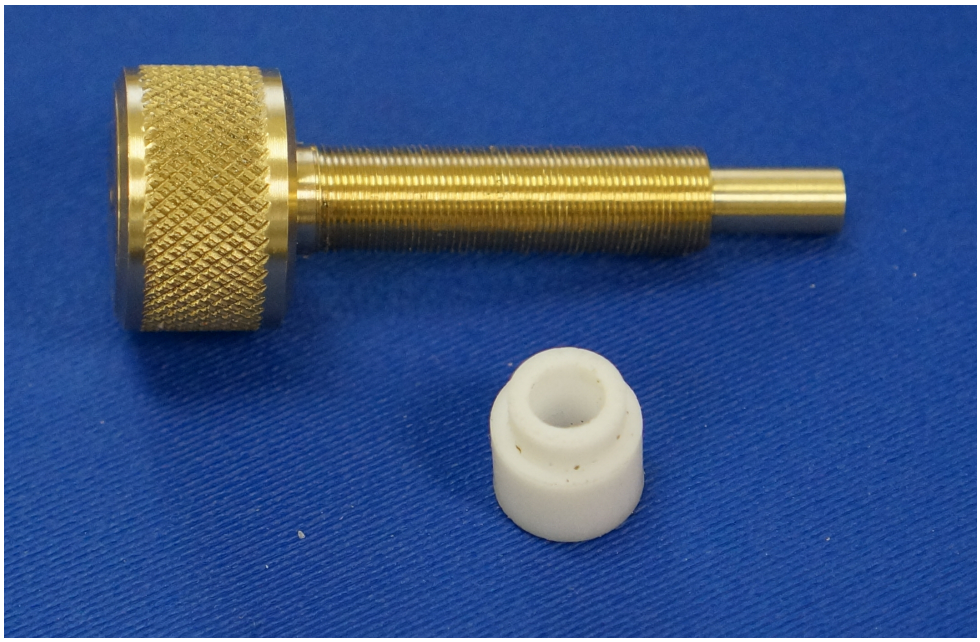

Figure 8.6 One of the fine focus screws and its PTFE bush.

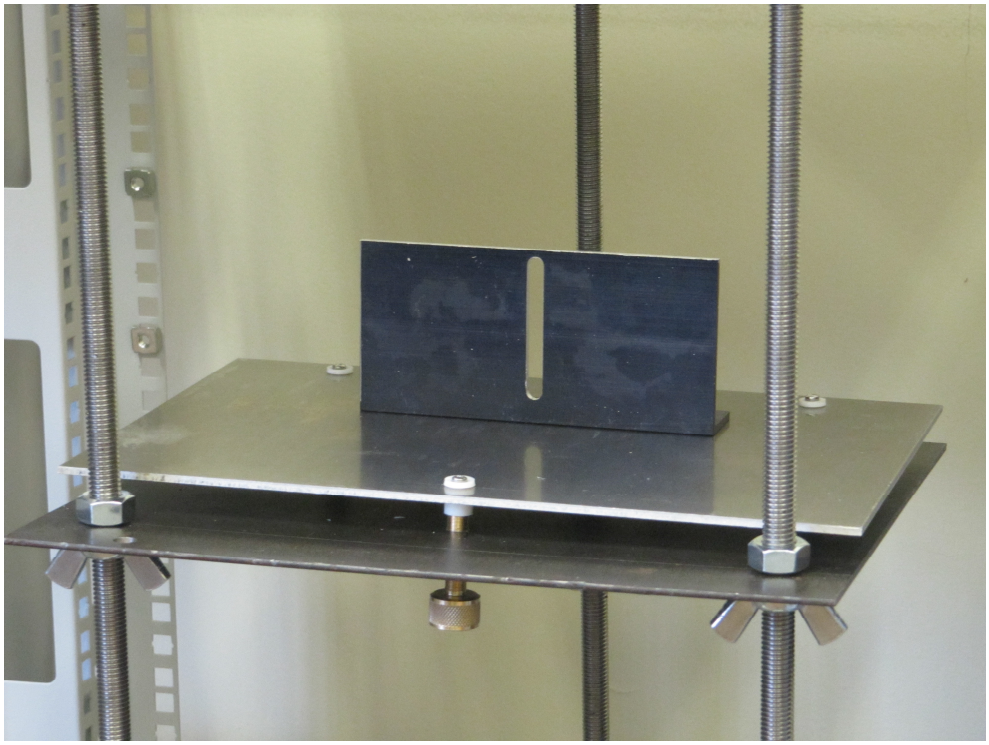

Figure 8.7 The movable camera platform, focus platform and camera bracket.

To mount the wafer a custom vacuum chuck was made, fig 8.8, this has three vacuum ports on the top surface to clamp the wafer uniformly, while a groove machined into the lower face secures the whole to the main deck.

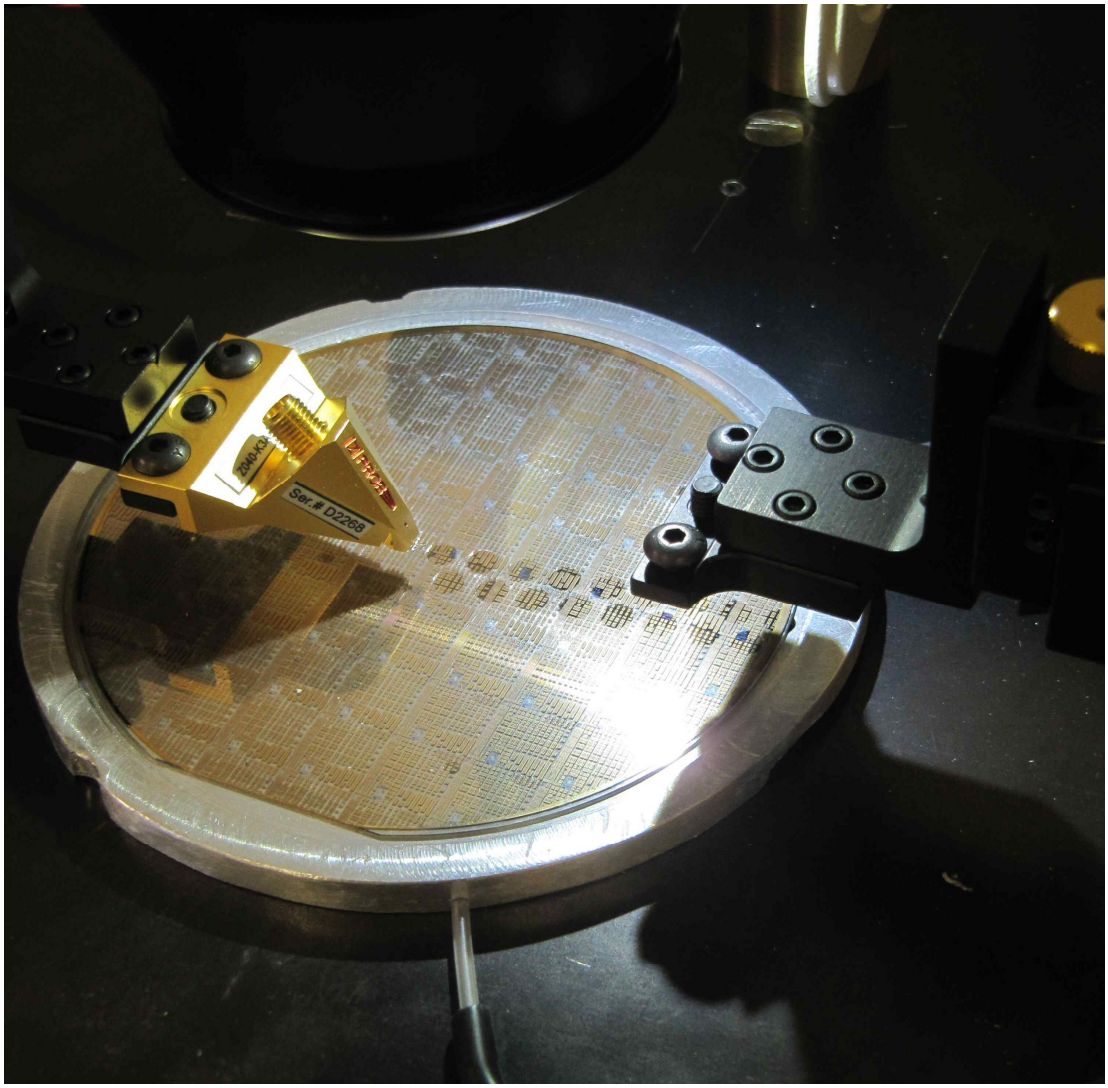

Figure 8.8 The custom vacuum chuck in position.

A pattern of holes can be seen through the wafer, the concept being that, by rotating the chuck relative to the wafer and deck, a hole can be positioned below any part of the wafer that is to be measured, while maintaining reasonable heatsinking performance. Also visible, along the lower rim, in the shadow of the right hand positioner, is the end of a relief machined into the lower surface around the pattern of holes, which reduces the effective thickness of the chuck plate to 2mm permitting the nose of the objective lens to get closer to the underside of the wafer.

Enough space is available behind the micropositioners to mount a pair of dual directional RF couplers, forming a compact and secure calibrated RF section.

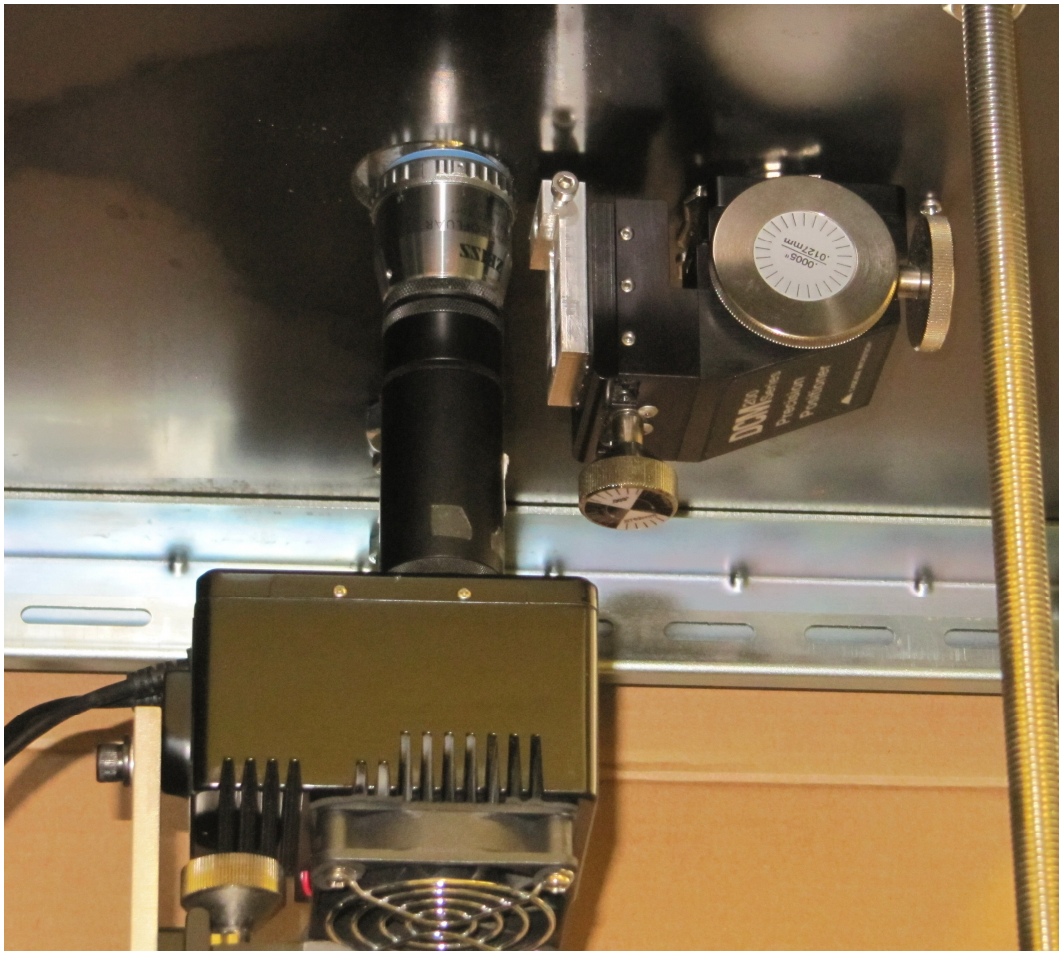

Figure 8.9 The Opticstar DS-142M in place beneath the main deck.

8.3 Measurement of Hot Electron Electroluminescence.

In collaboration with Dr T. Brazzini of Bristol University, an Opticstar DS-142M thermo electric cooled CCD camera was fitted to the platform Fig. 8.9, and a UMS GaN on Silicon Carbide wafer containing an array of device sizes and test structures was placed on the vacuum chuck. Initially a 2x75 device was chosen, with a DC bias of 25V and 15mA, electroluminescence was seen, shown as a monochrome image in Fig. 8.10. The alignment and focusing controls proving adequate for the task, although it must be conceded that the interaction of the X,Y and Z function made the process more difficult than it would be with independent controls.

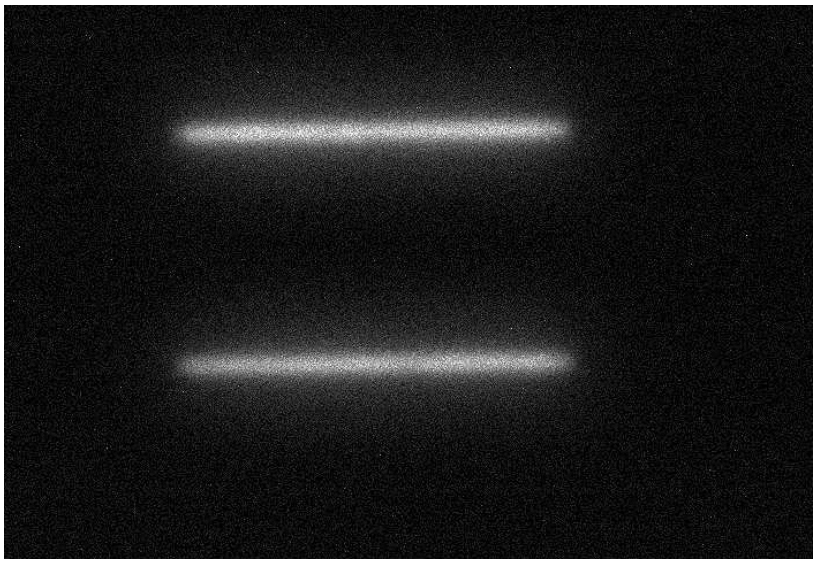

Figure 8.10 Electroluminescence viewed from the back of a UMS 2x75 GaN HEMT (monochrome).

The view seen in fig. 8.10 is cropped down from the full frame, losing around 80% of the available pixels, to counter this a new x63 Zeiss objective was substituted. As a further aid to precise focusing over the field of view this lens has adjustable “cover slip compensation”, intended to correct for varying thicknesses of microscope slide cover slips in conventional microscopy, since we are viewing the device channel through the silicon wafer, this is effectively our cover slip. When used with a UMS 4x100 die the image now occupies most of the frame, fig 8.11.

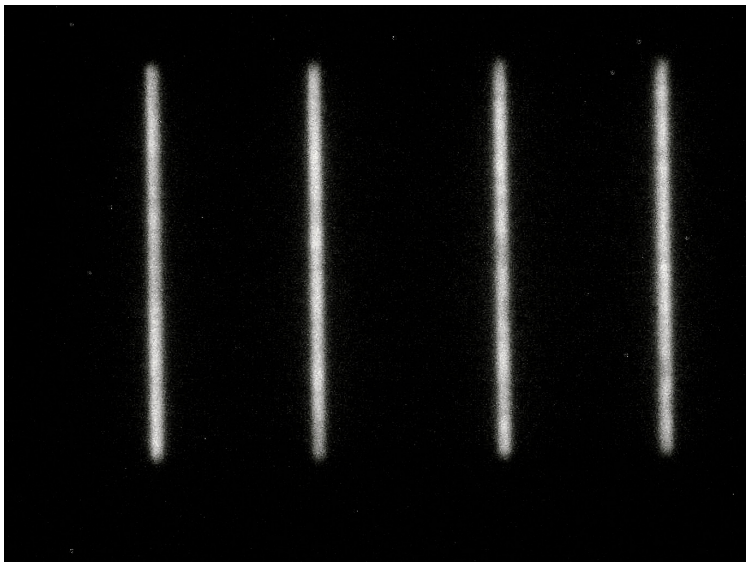

Figure 8.11 Electroluminescence viewed from the back of a UMS 4x100 GaN HEMT, with a x63 objective (monochrome).

In order to measure the emitted spectra under different DC and RF conditions [27] a fibre optic cable was attached to an XYZ positioner and installed as an alternative to the camera.

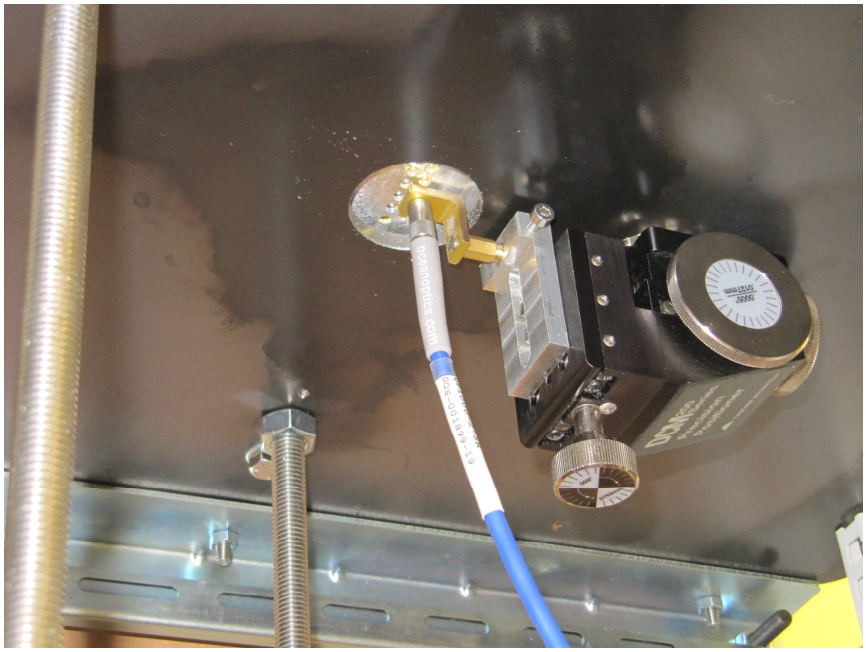

Figure 8.12 The fibre optic cable held in place by the micro positioner.

Since the die is small compared to the diameter of the cable, the cable can be positioned very close to the backside of the wafer precisely beneath the channel region so that a good proportion of the emitted light should enter the cable and be propagated along it.

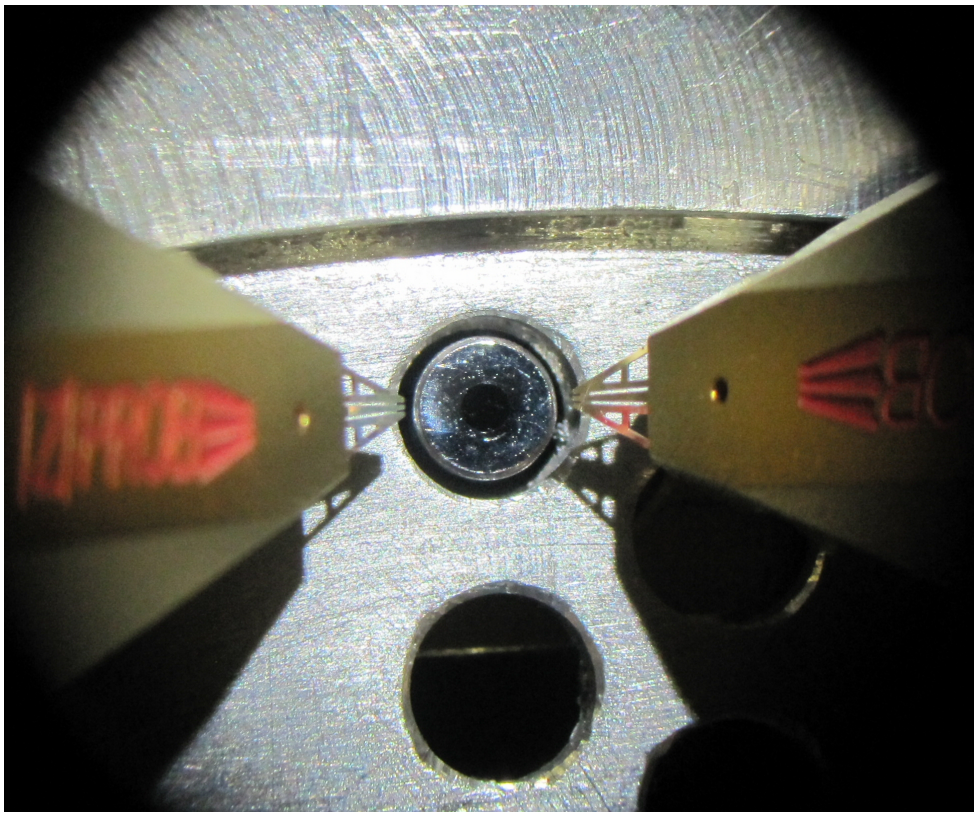

Figure 8.13 The fibre optic cable in place on the vacuum chuck, with the Cascade Z-probes.

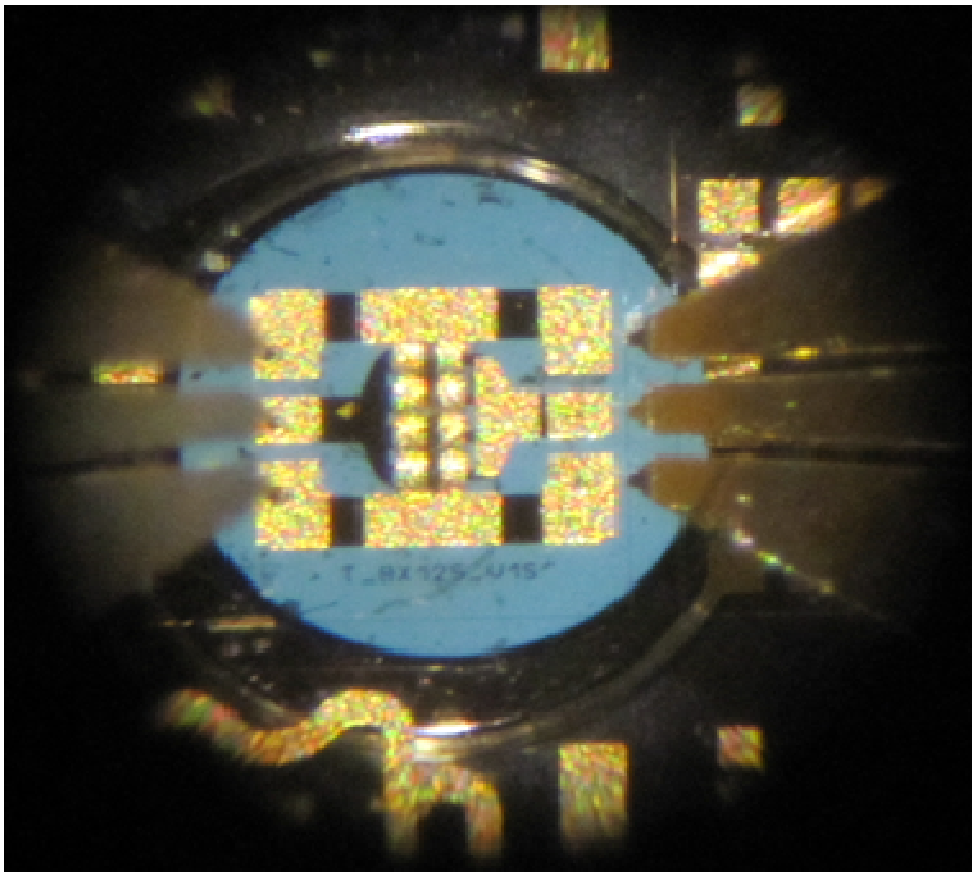

Figure 8.14 The end of the cable (illuminated from the opposite end) under the die.

For the first attempt at spectroscopy an Oceanoptics Maya 2000 pro spectrometer was attached to the other end of the cable to analyse the light and hence reveal the temperature of the hot electrons in the channel region. It was found with the 2x75 device that there was not an adequate signal to noise ratio to permit worthwhile measurement. Evidently the 8x125 device will put out more than four times as much light, and using a droplet of microscope oil on the end of the cable improved the optical coupling considerably.

It was found that under the DC operating point condition there was certainly enough light captured to work with, fig. 8.15, however, the light output drops under RF operation which prevents accurate analysis, particularly with modes like Class F.

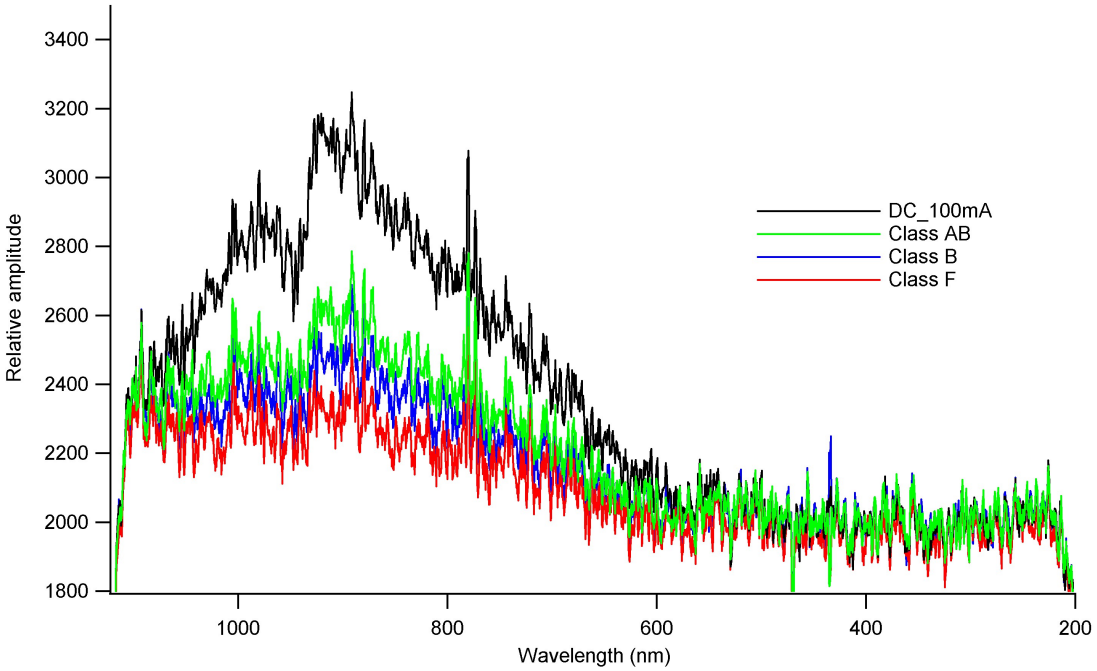

Figure 8.15 Spectra from the UMS 8x125 GaN HEMT under DC and RF, measured with Ocean Optics Maya 2000 pro portable spectrometer.

Oceanoptics offer a similar spectrometer with a Peltier effect cooled detector, the QEpro which has a lower noise floor and is able to discriminate more effectively. Once this device was fitted in place of the Maya then much better results were obtained, the QEpro is able to use integration periods of tens of minutes thanks to its cooled sensor, allowing results such as those shown in fig. 8.16 to be collected. These low noise level results can be processed satisfactorily to calculate the electron temperature, and a study was made of the UMS 8x125 in different modes, detailed in “Study of hot electrons in

AlGaN/GaN HEMTs under RF Class B and Class J operation using electroluminescence" [29]. The active harmonic control of this equipment was essential to collect the data, different modes and power levels can be measured with no disturbance to the die and fibre optic alignment, greatly facilitating relative measurements.

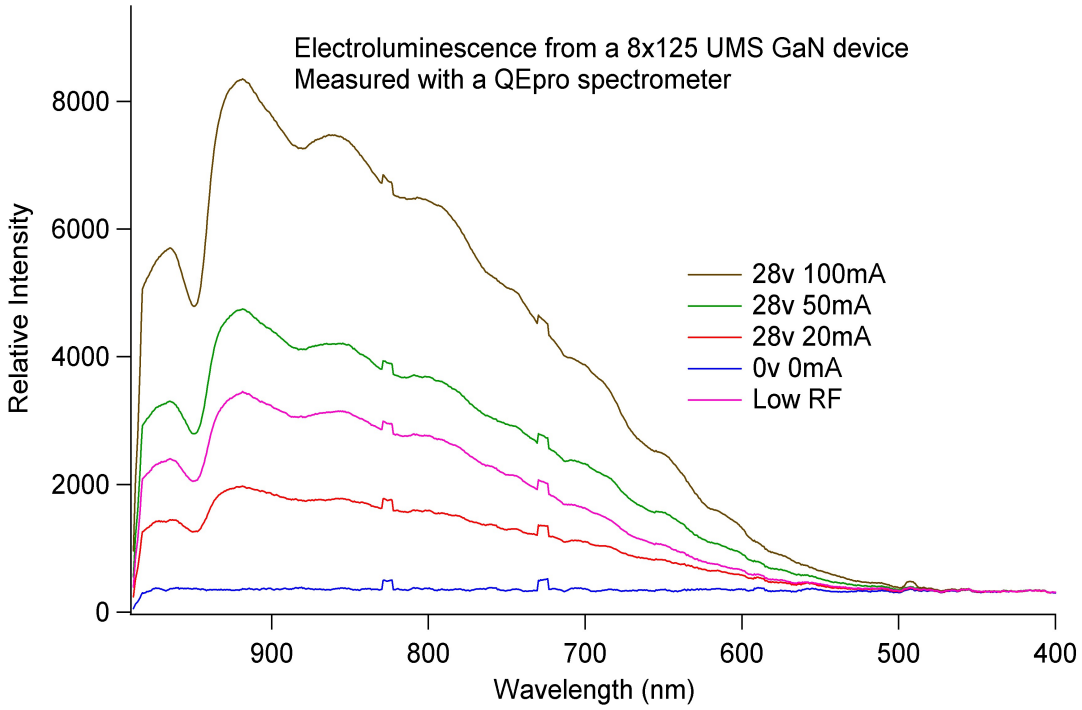

Figure 8.16 Spectra from the UMS 8x125 GaN HEMT under DC and RF, measured with Ocean Optics QEpro portable spectrometer.

The fibre optic mount would also be a very suitable way of attaching a Tunable Light Source (TLS), for investigating the wavelength relationship of the trap release processes, fig. 8.14 shows how effective this would be at illuminating the entire underside of the device. As a precursor to such a project, a number of different wavelength LEDs were mounted so as to be attachable to the fibre optic, enabling a basic study to be made of wavelength and amplitude sensitivity, see Chapter 3 [28].

8.4 Conclusions.

It has been shown that a combined Optical and RF measurement wafer probe station is a practical and useful proposition, by starting the design from a blank sheet the result was a station which worked well as an RF probe station while facilitating a variety of optical tests.

The top-side optical microscope together with the securely mounted micro-positioners and RF couplers made RF calibration and measurement just as manageable as on a commercial wafer station, the stiff, cross-braced box beam construction showing no signs of flex or vibration. The lack of an XY table did not really affect operation, the required die could be placed within a few microns of the wafer probe tips by manually sliding the vacuum chuck along the base table. The design would also be suitable for long term tests, in this application an XY table can be a source of failure, being vulnerable to knocks and vibration.

Once the backside camera and topside RF components had been aligned the initial luminescence measurements were made with ease, the concept of tilting the focus plate to give XY control worked well, and moving all three screws the same amount to focus was reasonably workable. A separate extra fine focus only control, ideally motorised, would be a useful feature. Once set the focus and XY position were stable, so consistent, repeatable measurements can be expected. It is the intention to investigate whether the luminescence emanates from different regions of the channel under RF and DC operation, which will require extreme consistency since the channel is only 5um long.

Changing from the camera to the spectrometer and vice versa proved straightforward, it is only necessary to remove the fibre optic cable mounting bracket from the micropositioner to allow the camera objective to be positioned. In a similar way the camera plate can be lowered on the M12 studs and slid to one side to fit the spectrometer cable, if the upper locknuts are not moved the plate can easily be repositioned when required.

Chapter 9 Applying the Methodology

9.1 Evaluating GaN on Diamond Devices.

A further opportunity to prove the value of the characterisation techniques described here arose with the advent of GaN on diamond devices, the excellent thermal conductivity of diamond (1000 – 2000 W/(m·K)) has the potential to greatly enhance the cooling of GaN devices, allowing a reduction in finger pitch, which would not only make devices more compact, but also reduce the phase discrepancy between fingers across a die, permitting a simpler, less branched manifold in a high power device. Realising these advantages has proved troublesome however, the GaN and diamond lattices do not align well, which can give a high thermal resistance across the boundary [30], and the GaN layers themselves have a relatively poor thermal conductivity (130 W/(m·K)), so the thickness of material between the active channel and the diamond must be kept to a minimum, if any advantage is to be had.

Sample devices were provided under an EPSRC project, EP/P00945X/1, fabricated by Sheffield University on a diamond substrate grown by Element Six, a company specialising in synthetic diamonds. The devices showed rather inconsistent DC properties when measured by Bristol University, with more gate and drain leakage than would be desired, but with a number of usable devices. A typical good device was selected for RF testing, broadband small signal S-parameter measurements, and high power active harmonic load-pull at 1GHz fundamental. Since the expected improvement in thermal behaviour is the motivation for developing GaN on diamond, the pulsed FAHLP system described in the preceding chapters should be ideal for analysing these devices.

9.2 The Load pull measurements.

At this low frequency (f_0 = 1GHz) the effect of the output capacitance can be neglected, and measurements made along the real axis. If the second and third harmonics are both shorted to 0Ω then scalable measurements can be taken by the automation facility of the Mesuro software, greatly speeding the process. Rather neater fan diagrams would be produced by pulling the harmonics to the same load as the fundamental (Chapter 6, fig. 6.1), but presently this can only be done one load at a time, a very time consuming process.

Tests were commenced at a low drain bias voltage of 10V, and repeated in 5V stages, up to 30V, only the 10V, 20V and 30V results are shown in fig 9.1. The DCIV line shown is for V_{GS}=0V, the highest measured, whereas the RF gate voltage was taken up to +1V, causing the RF load-lines to exceed the DC line.

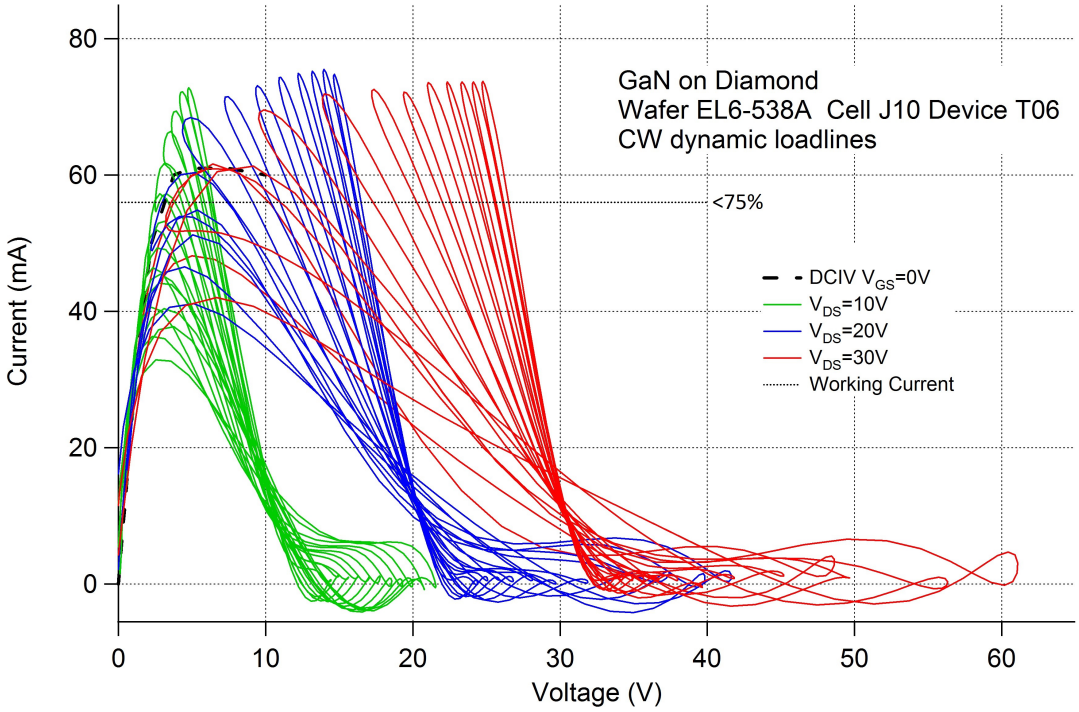

Figure 9.1 Fan diagrams for a 2x50 um GaN on diamond device, wafer EL6-538A.

The load-lines show a quite modest knee walkout, even at 30V drain bias, this is difficult to quantify however, as the knee softens into a curve as it moves. If we draw a line on the graph representing a typical working current at 75% of the peak current (56mA), and add lines joining the tips of the load-lines then we can establish a measure of the walkout by noting the voltage at the intercept for each drain bias setting, and calculating the difference between them, fig. 9.2.

We can now establish a figure of merit by comparing the achievable RF voltage swing to the ideal, which would be twice the drain bias voltage. If the knee did not walkout then this value would tend towards 2 with increasing drain bias voltage, as the effect of V_{DSmin} became relatively smaller, if the walkout was severe then the value would fall, indicating the device was not suitable for use at higher bias voltages. It can be seen in

fig. 9.2 that for this device the figure of merit improves as the drain bias rises from 10V to 20V, and then holds steady, so the device is good, if not excellent.

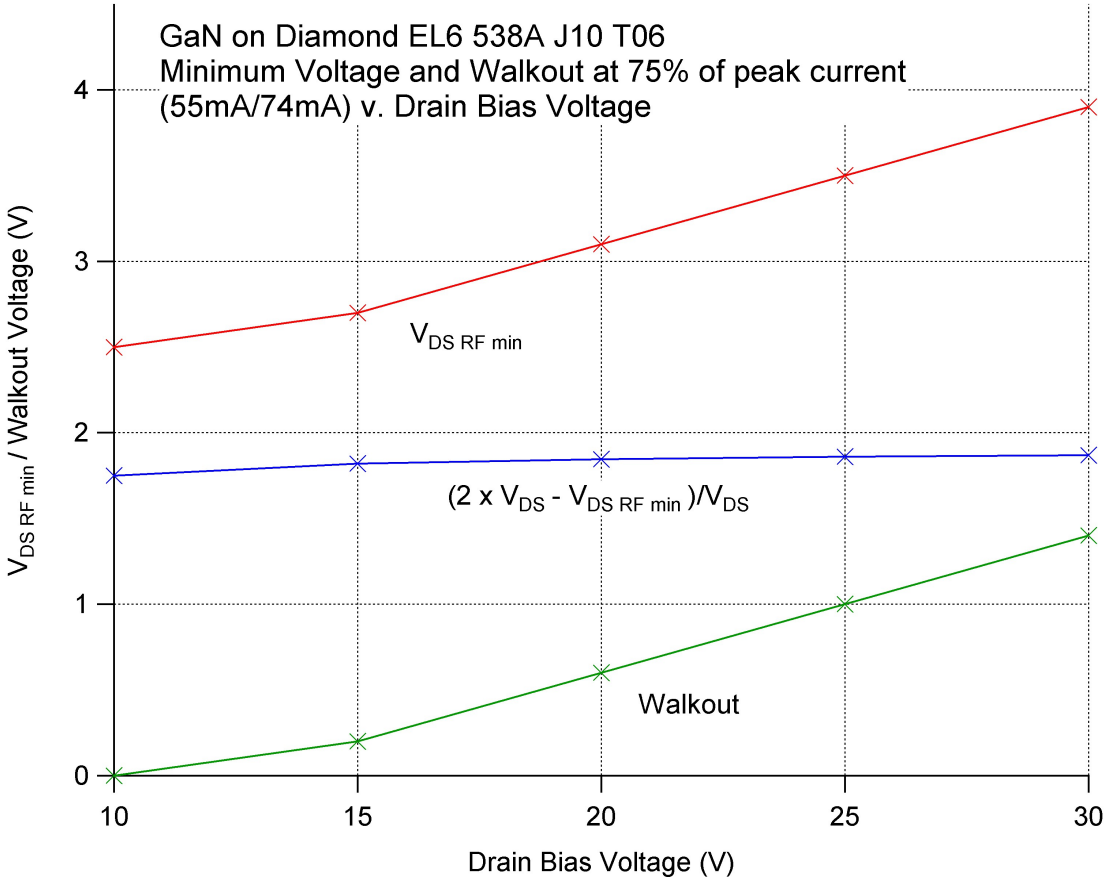

Figure 9.2 Change in minimum RF Voltage with Drain bias Voltage.

The devices supplied were all 2x50 um, which is not ideal as the optimum load value is so high that the measurements are taking place in the highly compressed region of the Smith Chart real axis, between Γ=+0.9 and +1. While adequate load-pull power is easily available at these frequencies, a small convergence error in the load reflection coefficient translates into a significant change in resistive load, making the measurements rather erratic at the extremes. Since the input and output powers are calculated from the difference between the forward and reverse waves at each port, we will be dealing with the small difference between two very large values, an inevitably error prone situation, especially if it is desired to fully circumscribe the optimum efficiency loads. Nevertheless acceptable results were achieved, however the observation was made to the fabricators that 2x125 um devices would improve measurement accuracy.

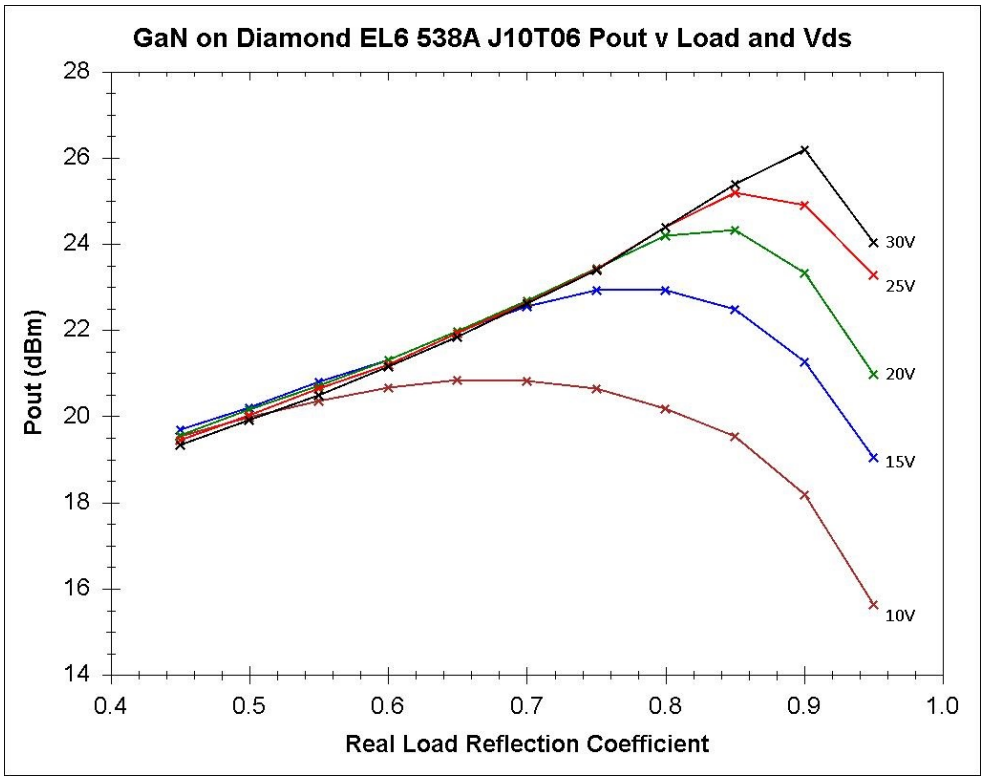

Figure 9.3 Output power against load and drain bias voltage.

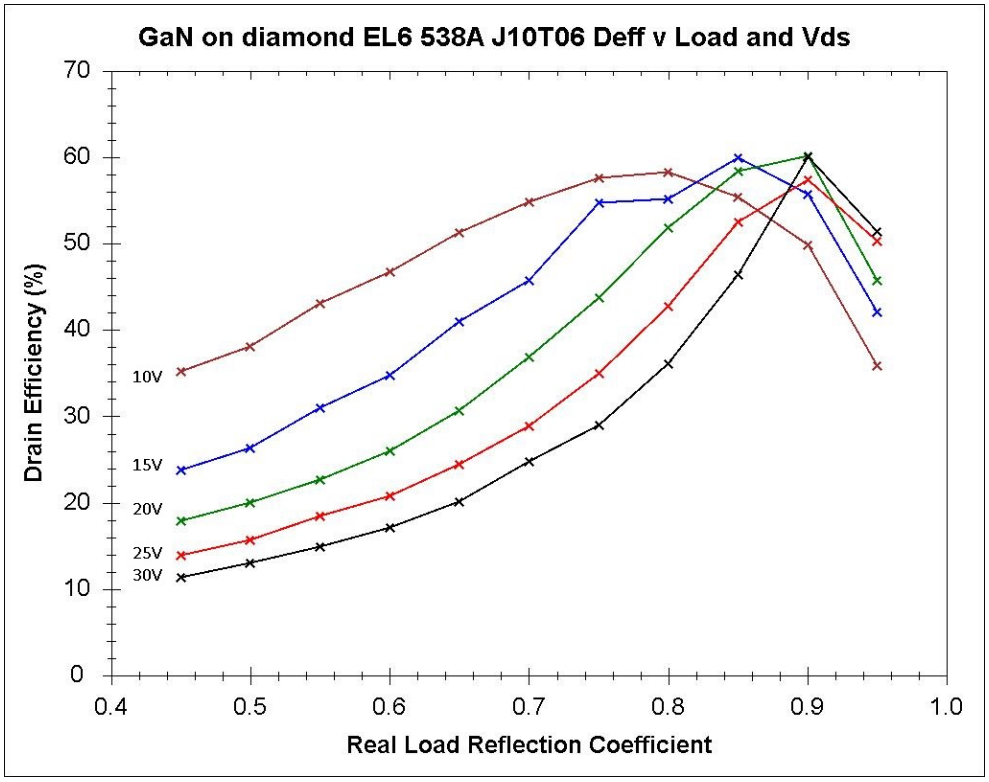

Figure 9.4 Drain efficiency against load and drain bias voltage.

Considering fig. 9.3 and fig. 9.4, we can see that the maximum output power is increasing with drain bias, while the maximum efficiency is relatively constant, as predicted by the calculation results shown in fig. 9.2. It is also clear that the small

device size is making measurements difficult above 20V drain bias. If the breakdown voltage of the devices is high enough to permit operation at 40V or 50V, then the performance could not be accurately assessed with this equipment.

9.3 Class F performance.

To give a practical assessment of the device performance it was driven into class F with a drain bias voltage of 28V, figs. 9.5 and 9.6 show the output power and drain efficiency contours, while fig. 9.7 shows the load-line with a fundamental reflection coefficient of 0.92, equivalent to resistive load of 1200Ω. It can be seen that performance is up to the expected commercial standard, with an output power very close to 4W/mm and an optimum drain efficiency over 70%.

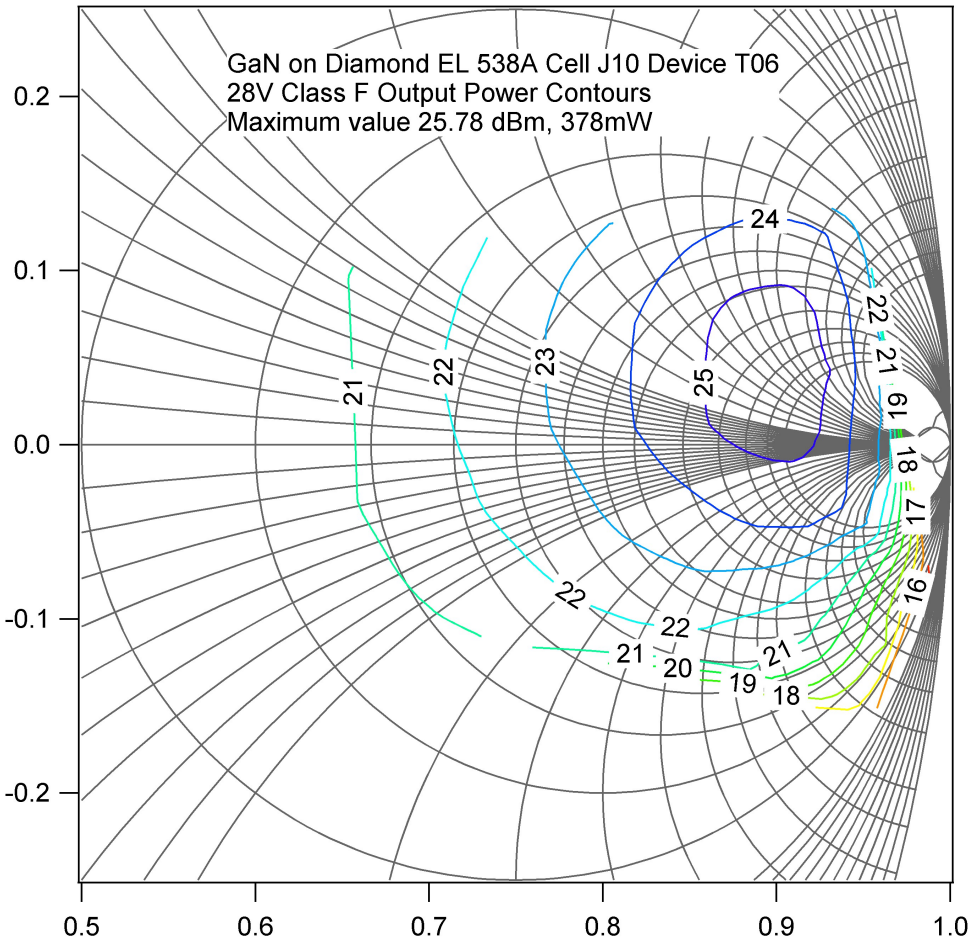

Figure 9.5 Output power contour for GaN on diamond 2x50 device.

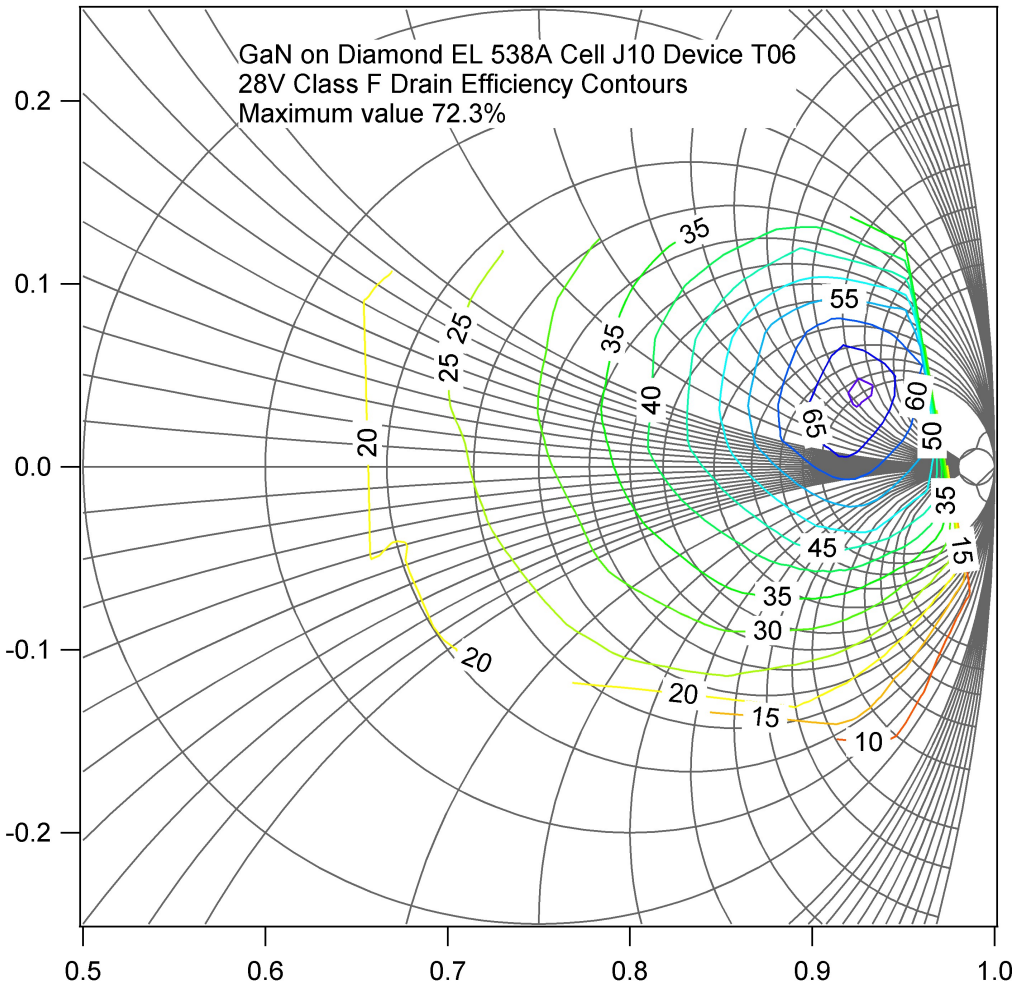

Figure 9.6 Drain efficiency contours for a GaN on diamond device in Class F.

The optimums sit slightly above the real axis, as expected due to the device output capacitance and the probe pads, and are slightly distorted due to the high real impedance. The load-line shown in fig 9.7 below was measured on the real axis, so the efficiency is slightly worse than the optimum found by the load sweep. It can be seen that the device is behaving well, it is pinching off in the negative half of the input wave, and the peak current is tracking the DCIV line.

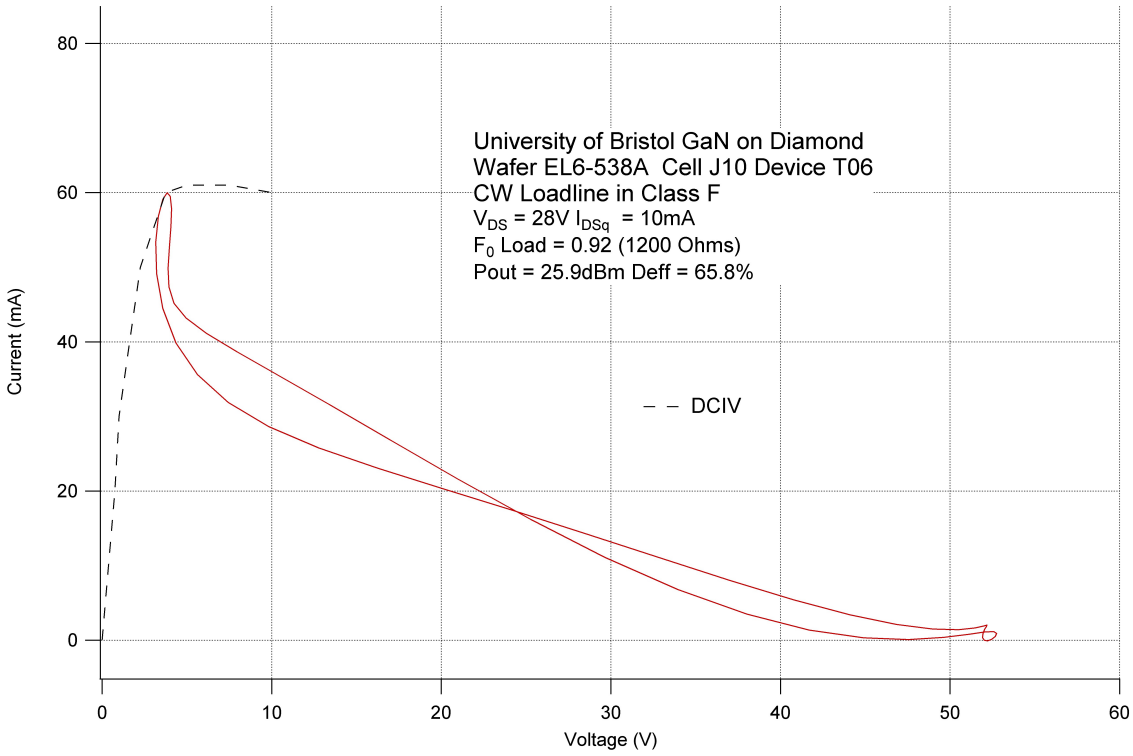

Figure 9.7 Dynamic load-line for a 2x50 GaN on diamond device in Class F.

9.4 Pulsed Active Harmonic Loadpull Measurements.

With the basic assessment complete the more advanced features of the pulsed FAHLP system can be used, fig. 9.8 shows the effect of switching from CW to a 15% duty cycle and pulse width of 15us. It is usual for Class B/AB performance to improve in pulse mode, since the power dissipated as heat in the device will be significantly lower, with a consequently lower channel temperature, however this device consistently showed higher output power in CW operation, and the power is further reduced if the drain bias is pulsed as well as the RF.

If the drain bias is switched with the RF then the power is reduced across the entire impedance range, however if the drain bias is left on during the RF blank period much of the performance is recovered at the normal operating load region. A possible explanation is that the thermal performance is as good as expected, so that there is negligible gain from pulse operation, and some type of charge trapping effect is causing a drop in performance. It may well be that such effects occur in devices made on the more usual silicon and silicon carbide substrates, but there the improvement due to the lower temperatures masks the reduction due to trapping. An obvious step is to deploy the 3eV laser, to try and isolate the trapping effects.

9.5 Applying the 3eV Laser.

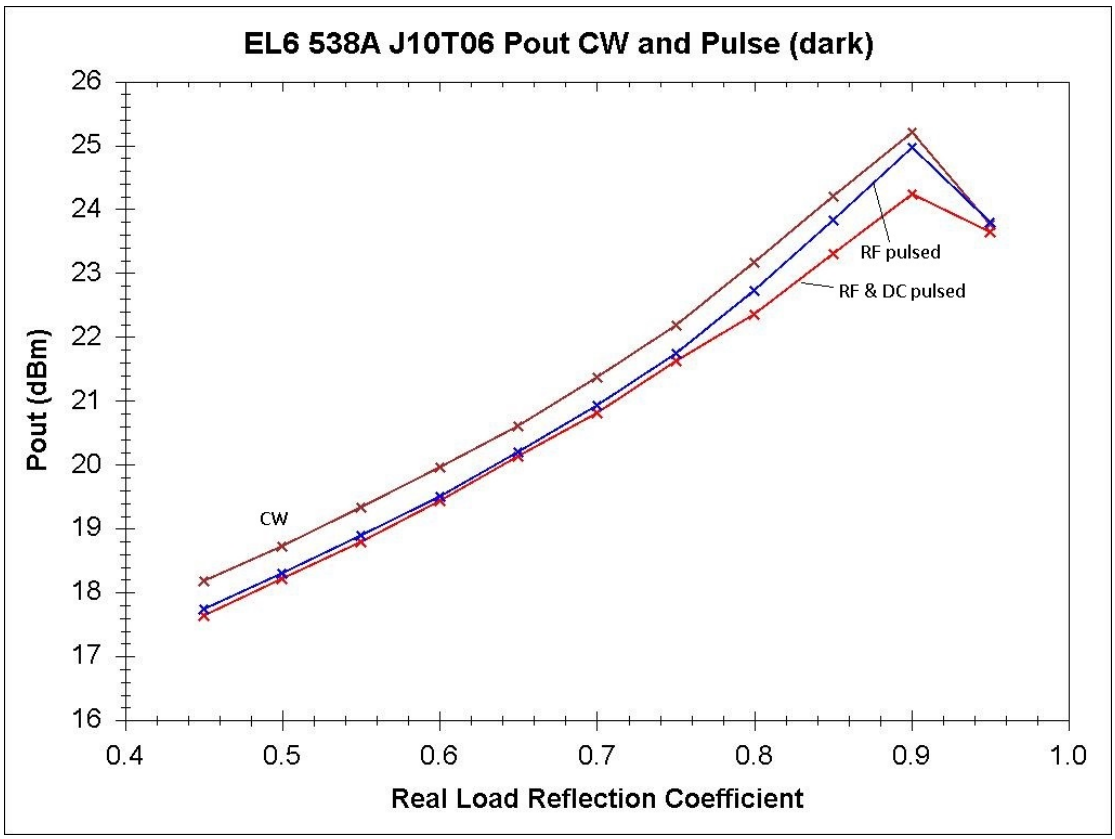

Figure 9.8 Variation of output power with load, in pulsed and CW operation.

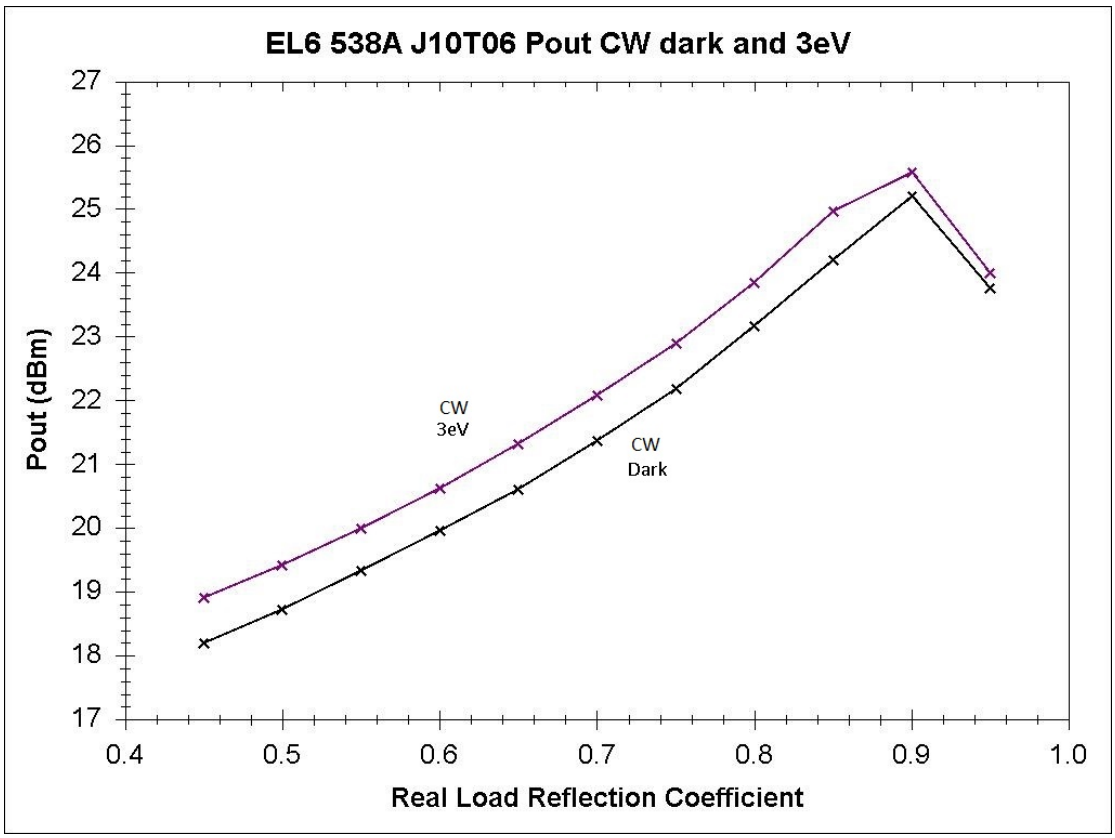

Figure 9.9 Variation of CW output power with load, dark and with 3eV light.

Despite the relatively low levels of knee walkout displayed by this device there is a significant increase in output power when the 3eV laser is activated (fig. 9.9), approaching 1dB at the low impedance loads, lessening as the impedance rises. If the pulse test is repeated with the laser operating then we see an interesting picture, fig 9.10.

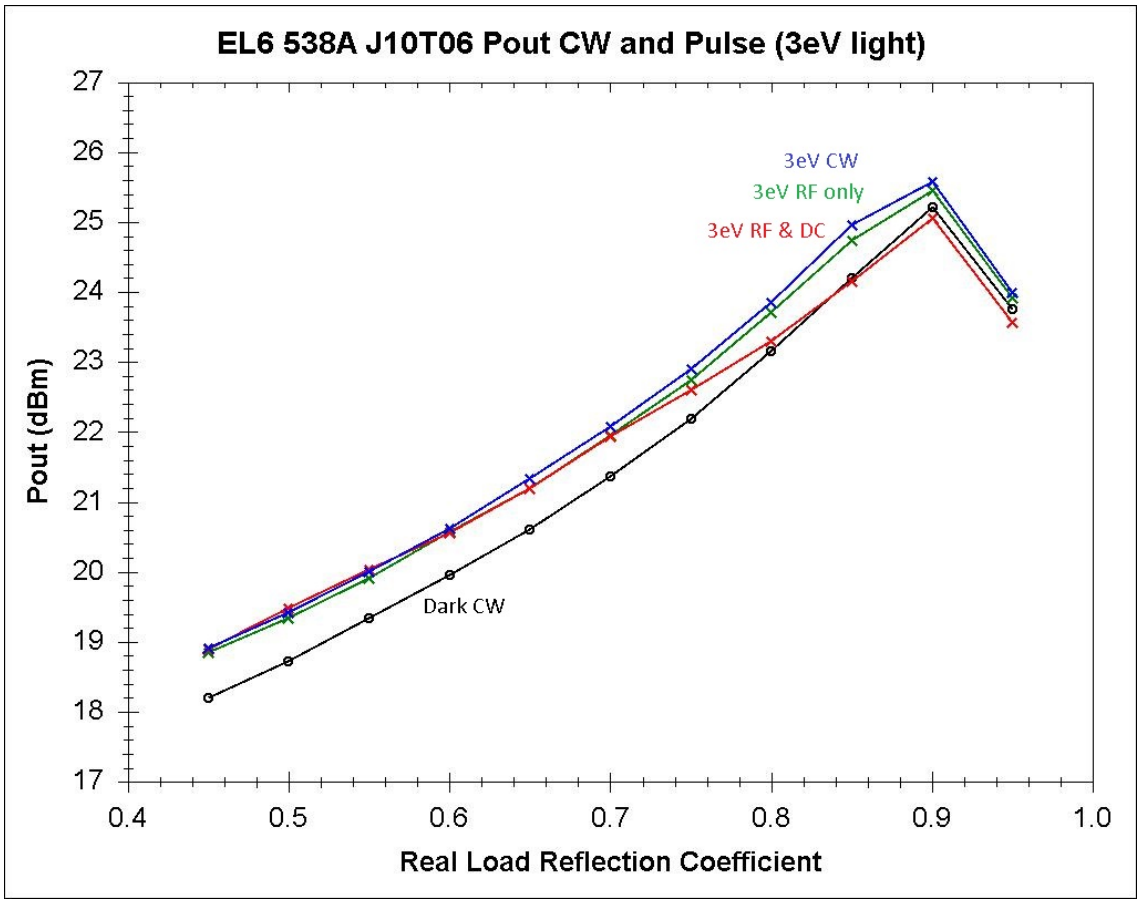

Figure 9.10 Variation of output power with load under pulsed and CW operation with 3eV illumination.

The variation between pulse and CW at low impedances is eliminated by the 3eV light, but as the load impedance rises towards the normal operating region the output levels diverge once more, though the difference is much reduced over the dark condition, 0.5dB rather than 0.95dB (fig. 9.8). It would seem that the device is showing two different types of trapping behaviour, one of which is easily wiped by the 3eV light, and one which is more persistent. Some factor must be changing as the load impedance rises, fig, 9.11 shows the dynamic input voltage against output current at the lowest impedance load ($\Gamma = 0.4$) and the optimum Pout load, ($\Gamma = 0.9$), it can be seen that the input voltage range is nearly constant for the two extremes.

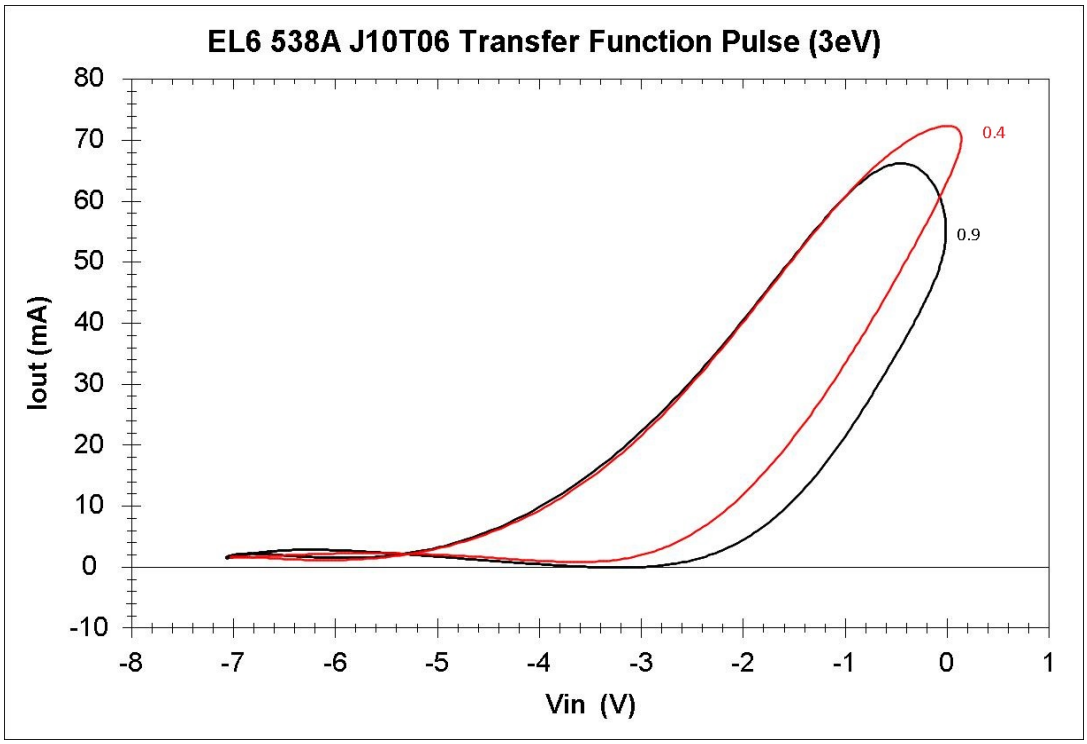

Figure 9.11 Transfer function for pulsed RF and DC with 3eV illumination.

If we consider the output dynamic load lines (fig. 9.12), then we see a very large change in output voltage range, 23V to 32V for Γ = 0.4, and 4V to 50V for Γ = 0.9.

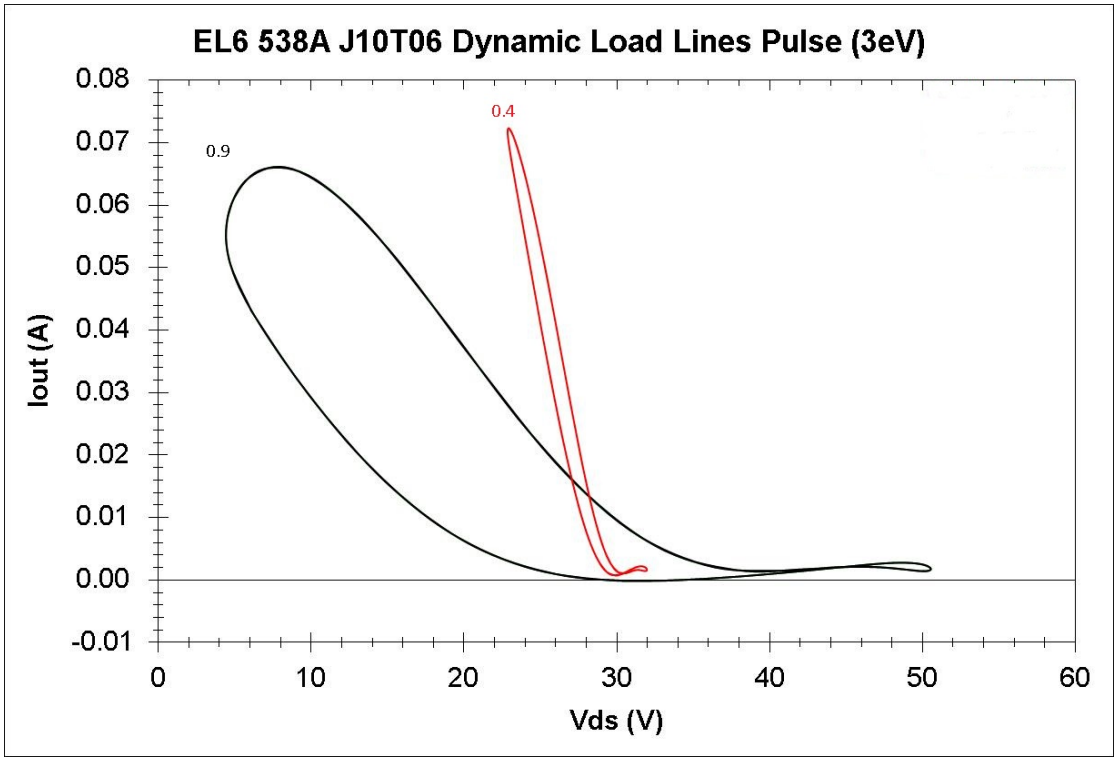

Figure 9.12 Dynamic Load Lines for pulsed RF and DC with 3eV illumination.

It was shown in Chapter 5 that high drain voltages can give rise to trapped charges which are resistant to release by 3eV light, whereas gate – source voltage induced traps may be released entirely by such illumination. The results shown here are consistent with those findings, though this does not explain the difference seen when the drain bias is pulsed along with the RF, compared to only the RF being pulsed. The electrostatic fields within the device are very different in the two situations, with the drain bias removed there is no large potential gradient over most of the channel, and it has been demonstrated that such a gradient can remove trapped charge [9, Chapter 3 fig. 3.8]. It would be very interesting to see the effect of pulsing the gate bias voltage as well as the drain bias, though at the time of writing this facility is not available. Two conditions should be considered, taking the gate bias to ground during the blanked period, and also a condition often used in actual systems, taking the gate bias further negative during blanking, this would determine whether it is simply the absence of the drain bias potential gradient allowing traps to remain undisturbed during the blanking period, or whether the negative gate bias can cause greater trapping without the presence of the drain bias gradient.

9.6 Conclusions.

It has been shown that Waveform Engineering techniques used with pulsed fully active harmonic load-pull and 3eV illumination can reveal very useful information to assist with process development, and should therefore help to expedite the introduction of new technologies. The exact cause of a problem may not be immediately apparent from such measurements, but with the rigorous application of the scientific method, the ability to make detailed assessments of the interaction between various parameters gives the device physicist a unique insight into the effects of changes to the process.

Chapter 10 Conclusions

10.1 Conclusions and Further Work.

In this work it has been shown that the addition of pulse capability to a fully active harmonic load pull system is a practical proposition [5], the resulting combination is a versatile and accurate [25] way of assessing the performance of semiconductor devices, both for the purpose of process improvement [9] and circuit design. The system has been used to evaluate a number of different devices and aspects of their design, including the performance of source coupled field plates [7] and the effect of finger spacing on thermal performance. A comparison between silicon and silicon carbide as substrates has also been made, which led to the finding of a parasitic conduction layer in the silicon device and subsequently improvement to the production process [24]. Together these factors show that the addition of pulse capability to an AHLP system should be considered, especially in view of the reduced thermal loading and extension to the safe operation region discussed in Chapter 6.

The addition of the pulsed 3eV laser as described in Chapter 3, adds a new dimension to device evaluation, as many types of charge trapping behaviour can be influenced by this light and may be used to isolate the root cause of problems. A practical example of this has been documented and the possibilities for extracting filling time constants explored. It is believed that using a tunable light source rather than a fixed wavelength laser will permit the specific energy level of the trapped charges to be evaluated, helping to identify the physical mechanisms responsible. A Newport TLS-300 system with its xenon bulb can provide near monochromatic energy into the low UV region, and should be ideal for this purpose. As a step towards this, it was shown that light of 480nm wavelength had no appreciable effect, while at 395nm the effect was marked, however the abruptness of the threshold and the effect of light beyond 395nm remain to be determined.

The resistive drain load work discussed in Chapter 5 is only the beginning of the possible applications for this method, different tests can be devised to examine many aspects of device behaviour. It has been used here to show that the residual knee walkout experienced in Win GaN devices is definitely due to charge trapping phenomena and not thermal effects. It has also been shown that the trapping induced by

excessive gate-source voltage involves a different process than trapping caused by high drain-source voltage, in the case of the GaN on SiC devices tested. The use of the method to measure trap filling times by means of extreme duty cycle signals has also been demonstrated. Ideally, if some method of interlacing this type of measurement pulse within a controllable RF signal could be developed then measurements of trapping behaviour under specific operating conditions could be made. It should be possible to carry out measurements with a resistive drain load using a commercial parameter analyser such as the Keysight B1500, possibly by measuring the current drawn directly from an SMU supplying the DC bias, or perhaps by using an additional SMU to measure the voltage at the drain terminal. Using a sinusoidal input waveform to control the gate voltage will permit fan diagrams to be plotted at frequencies far below those of conventional RF loadpull, enabling study of the frequency dependence of knee walkout.

A useful method for extending the upper frequency limit of fully active harmonic load pull using existing components has been put to practical use (Chapter 4), allowing work with a fundamental frequency of 32GHz to be performed [17]. The work has shown that active load-pull is capable of working to higher frequencies than passive load-pull, as well as being the method of choice at lower frequencies where the tuners become large and expensive. In the past, since the physical size of the circuits at VHF and UHF facilitates hand tuning of live circuitry, and, at VHF at least, oscilloscopes may be directly attached to nodes, the high cost of the very large tuners required meant that only rudimentary theory was applied, followed by extensive periods of bench tuning. Since the ZVA system can work down to 20MHz, and high power broadband VHF amplifiers are easily obtainable, there is now no reason why precise load pull data should not be available to the design engineer at these frequencies.

Accurate and dependable techniques for evaluating the DC parameters under pulse operation have been demonstrated as have methods for switching the DC and providing ultra fast protection against excessive current, Appendices B and C.

As well as conventional load pull work, some of the other possible applications this type of equipment is capable of have been discussed, such as source pull and reverse power injection measurements combined with harmonic load pull. While it is not essential to perform the latter under pulse operation in all cases, the reduced loading on the test

device and the measurement system greatly reduces the risk of damage. The extension of the over-current trip to also switch off the RF drive is most important for reverse injection testing, as this is the major source of energy.

The Opto/RF wafer probe station discussed in Chapter 8 is a novel facility, and will allow detailed and reliable investigation into the trap release effects described in chapters 3 and 5. By permitting a fibre optic cable to be brought precisely into position under the die the design can ensure total illumination of the device, either by a LED or a tunable light source. Adopting this approach also allows a spectrometer to be used to measure the intensity of the light, so that a collection of different wavelength LEDs can be characterised for intensity against current, and then the trap releasing properties of each assessed against current. In this manner the sensitivity can easily be quantified.

The chief purpose of the Opto/RF station was to facilitate backside microphotography and spectroscopy of the electro-luminescence phenomena described in chapter 8 and "Electroluminescence of hot electrons in AlGaN/GaN High Electron Mobility Transistors under radio frequency operation", T. Brazzini, M. A. Casbon et al [27], the resulting design will greatly assist in furthering this and similar work. The unique ability to take precision optical measurements while simultaneously performing fully active harmonic load pull techniques will yield fresh insights into device behaviour. It is expected that it will show the EL being emitted from different regions of the channel under RF and DC operation as the electric field profile varies. It is also anticipated that a different type of emission may occur when the RF takes the drain voltage to extreme levels, the beginnings of catastrophic voltage breakdown may be detectable. The spectrometer should be able to isolate this if it occurs, since it is expected to be of narrow spectral width, easily distinguished from the broad spectrum EL emissions.

As Waveform Engineering has gained acceptance and become a mainstream evaluation and diagnostic tool expectations of accuracy have risen, significant decisions are being taken based on these methods. In conclusion it is felt that the work presented here will promote and support an era of Precision Waveform Engineering, during which a precise and detailed knowledge of the real-time behaviour of microwave devices will come to be taken for granted.

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Glossary

AlGaN Aluminium Gallium Nitride.

AHLP Active Harmonic Load Pull, load pull with active control of the harmonic loads, the fundamental load maybe actively or passively controlled, although the latter is properly termed hybrid load pull.

AM Amplitude Modulation, the modulation of a carrier wave by varying its amplitude.

Class A An amplifier with the DC bias quiescent current set to half of the expected maximum value is said to operate in Class A. Provides best linearity and small signal gain at the expense of efficiency.

Class B For Class B operation an amplifier is biased to the threshold of conduction, so that the positive half of the input signal causes current to flow. The even harmonics must be terminated in a low impedance. Gives better efficiency than Class A but with greater harmonic distortion and lower gain.

Class AB A compromise between Classes A and B, a small quiescent current is set, reducing the distortion of B while maintaining better efficiency than A.

Class C For this mode the input bias voltage is set below the conduction threshold, so that the output conducts for less than half of the signal cycle. Better efficiency than Class B but with greater distortion and lower gain.

Class F If the odd harmonics of a Class B amplifier are presented with an open circuit and the input driven so as to switch it between saturation and pinch off it is said to be in Class F. The drain voltage waveform should approximate a square wave, with a half wave rectified current flowing during the low voltage period only. Best efficiency and output power, but with lower gain and worse distortion than Class A.

Continuous Mode The efficient modes described above rely on the harmonics being terminated in open or short circuits, evidently in a practical circuit this cannot be maintained if the amplifier is to operate over a range of frequencies. It was observed that the fundamental load could be rotated away from the real axis to counter the rotation of the second harmonic load. Provides good efficiency over near octave bandwidths.

CW Continuous Wave, a signal, usually sinusoidal, of constant amplitude and frequency. Older texts may use Carrier Wave, where the frequency or

	amplitude are modulated with information for broadcasting, the average power and frequency remaining constant.
DAQ	Data AcQuisition unit, an instrument for collecting values of voltage and current and transferring them to a digital storage medium.
DCIV	Charts of output current (I) against output voltage (V) measured with varying direct current (DC) values.
DLL	Dynamic Load Line.
DUT	Device Under Test.
FAHLP	Fully Active Harmonic Load Pull, implies all loads are controlled by active means.
FET	Field Effect Transistor.
FM	Frequency Modulation, the modulation of a carrier wave by varying its frequency.
GaAs	Gallium Arsenide.
GaN	Gallium Nitride.
HEMT	High Electron Mobility Transistor.
HFET	Heterostructure Field Effect Transistor.
InAlN	Indium-Aluminium Nitride.
Ka band	Radio frequency band defined as from 26.5 GHz to 40 GHz by the IEEE.
Knee walkout	The angle formed in a DCIV curve by the sloping constant mobility line and the horizontal constant velocity line is referred to as the knee. Under RF operation charge traps and self-heating may cause this knee to move down in current and increase in voltage, known as walking out.
LED	Light Emitting Diode.
LDMOS	Laterally Diffused Metal Oxide Semiconductor.
LSNA	Large Signal Network Analyser.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
PET	Polyethylene terephthalate.
PTFE	Polytetrafluoroethylene.

QPSK	Quadrature Phase Shift Keying, a modulation scheme allowing the transmission of two bits of information per phase shift of 0°, 90°, 180° or 270°.
RF	Radio Frequency.
SFP	Source coupled Field Plate, an extension of the Source electrode, passing over the top of the Gate electrode to modify the electrical field pattern.
Si	Silicon.
SiC	Silicon Carbide.
SiN	Silicon Nitride.
TEC	Thermo-Electric Cooler.
TTL	Transistor-Transistor Logic.
UHF	Ultra High Frequency, radio frequency band defined as from 300MHz to 1GHz by the IEEE, although the ITU regard the upper bound as 3GHz.
UMS	United Monolithic Semiconductors.
V band	Radio frequency band defined as from 40GHz to 75GHz by the IEEE.
VDMOS	Vertically Diffused Metal Oxide Semiconductor.
VHF	Very High Frequency, radio frequency band ranging from 30MHz to 300MHz.
VSWR	Voltage Standing Wave Ratio.

VTD SWAP X402 – a four channel sampler based receiver manufactured by Verspecht-Teyssier-DeGroote.

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Appendix A (provided for information only)

Universal RF Transistor Test Fixture with Active Temperature Control.

Introduction

Section A1 The RF Fixture
- 1.1 Mechanical Design Considerations
- 1.2 RF Transformer Design
- 1.3 Calibration & Testing
- 1.4 High Power Testing

Section A2 The Chassis & Cooling System
- 2.1 The Design outline
- 2.2 Pump Characterisation
- 2.3 Chassis Design
- 2.4 Peltier Effect Devices
- 2.5 Thermal Performance Assessments

Section A3 The Control Electronics & Remote Link
- 3.1 Design Parameters
- 3.2 Temperature Monitoring
- 3.3 Control
- 3.4 Loop Gain & Delay
- 3.5 Remote Control Link

Section A4 Overall Testing
- 4.1 Relationship of Gain, V_{GS}, I_{DS}, & Temperature
- 4.2 Swept power Measurements

Section A5 Conclusions and Future Work

Introduction

The purpose of this project was to provide the university with a versatile fixture for the characterisation of radio frequency transistors. In addition to mounting a wide range of device packages, some method of temperature stabilisation and control is required.
To reduce the power levels needed to make the device measurements, wideband microstrip transformers are used to lower the system impedance from 50 ohms to 10 ohms [14, Zaid Aboush, “High Power Active Harmonic Load-Pull System for Characterization of High Power 100Watt Transistors”].

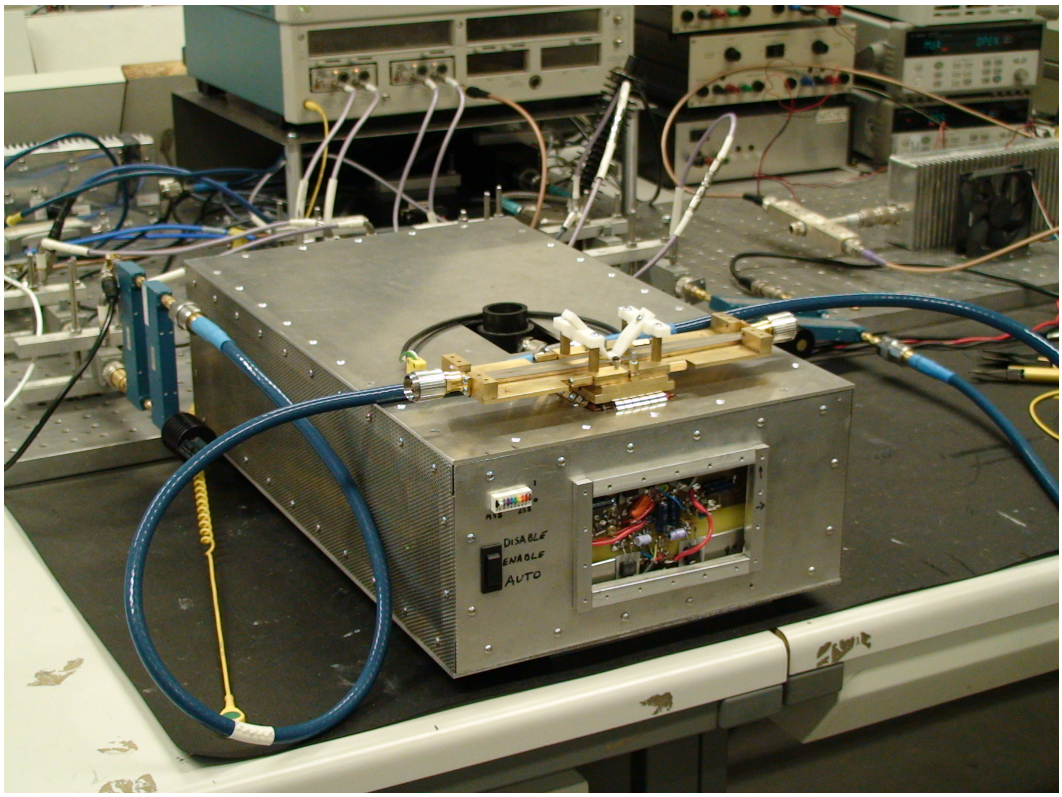

Fig AI.1 The fixture in place with the High Power measurement system.

In order to make accurate measurements some method of characterising the transformers is necessary, so that the calibration plane can be transferred from the APC-7 coaxial connectors to the device tabs. Calibration standards were manufactured for this purpose, a short circuit and three 10 ohm line sections to enable TRL calibration over the 800MHz to 18GHz frequency range. A pair of 50 ohm adaptors and matching standards were also constructed, for measuring low power devices.

It became apparent that the project comprised of two largely independent parts, the cooling system and the RF fixture. Since it is inevitable that a number of different device mounting blocks will be necessary to accommodate the different device package flange widths, the resulting physical break between the device mount and the cooling system makes a logical place to split the design tasks.

The RF fixture itself consists of a number of copper mounting blocks to which microstrip RF transformers can be attached, in such a way that individual variations in package dimensions can be catered for.

The cooling system must keep the flange of the device at a constant temperature, set either locally or via a digital link. Since a conventional passive cooling system cannot cool below the ambient temperature, and to give more precise control, an active system utilising some form of heat pump is required, Peltier effect Thermo - Electric Coolers (TEC) were chosen to form the pump. The design of the electronic system to control the TECs was separated from the mechanical and thermal design of the cooling system, giving three largely independent areas of work;

The RF fixture
The chassis and cooling system
The active control electronics

These three areas are detailed in turn below.

A1: The RF Fixture

A1.1 Mechanical Design Considerations

The first task undertaken was to survey the packages used by the various manufacturers and assess how many different mounting blocks would be required. Although historically there is a very wide range of shapes and sizes the more modern devices tend to fall into two groups, 6mm and 10mm flange widths. Within these groups there is a range of flange lengths and mounting hole pitches, but multiple mounting holes can be made in each block, and in fact it was found that all the devices thought likely to be measured could be accommodated with only two blocks. Some new devices in older style packaging have 0.25 inch flanges, so a third block to accommodate these was also made.

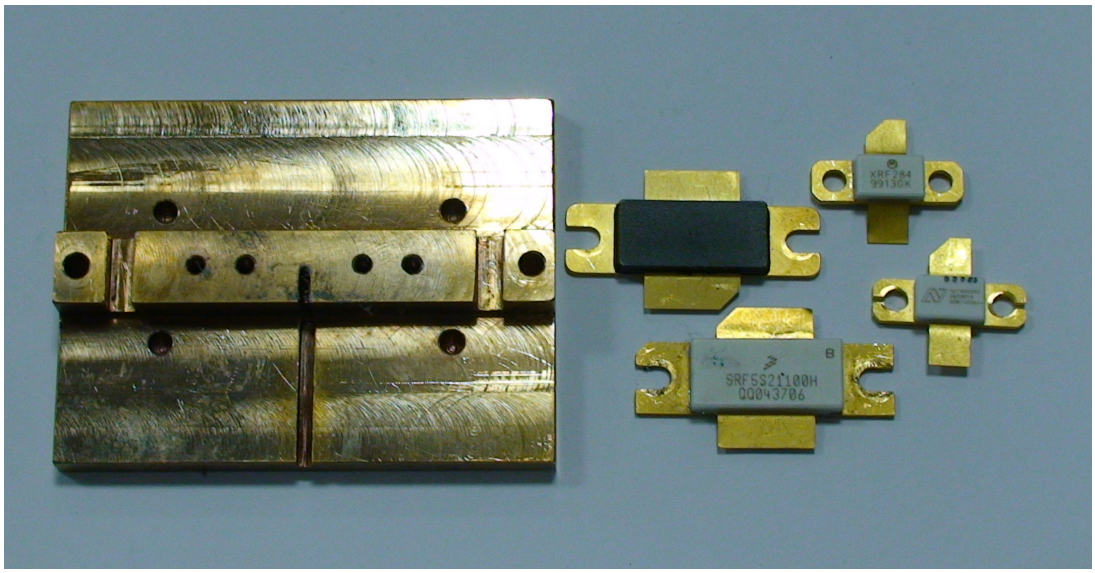

Fig A1.1.1 The 10mm width block and a selection of devices, LDMOS and GaN.

It is essential that an excellent ground connection is made between the earth plate of the transformer and the mounting block, especially in the area of the device flange, and yet it is necessary to be able to adjust the height of the transformers on the block to cope with different style packages and the tolerance range of each package.

To meet these conflicting requirements the mounting face of each transformer was relieved such that three islands remained, one centrally along the top edge in the region of the flange, and one along the bottom of each outer edge. When the transformer is pressed against the mounting block, these three constraints permit only one solution in the three dimensions, and so it is inevitable that all three islands make contact, in this way a solid ground connection is ensured adjacent to the device flange. To improve the reliability of the connection, gold on top of silver was electroplated onto the components.

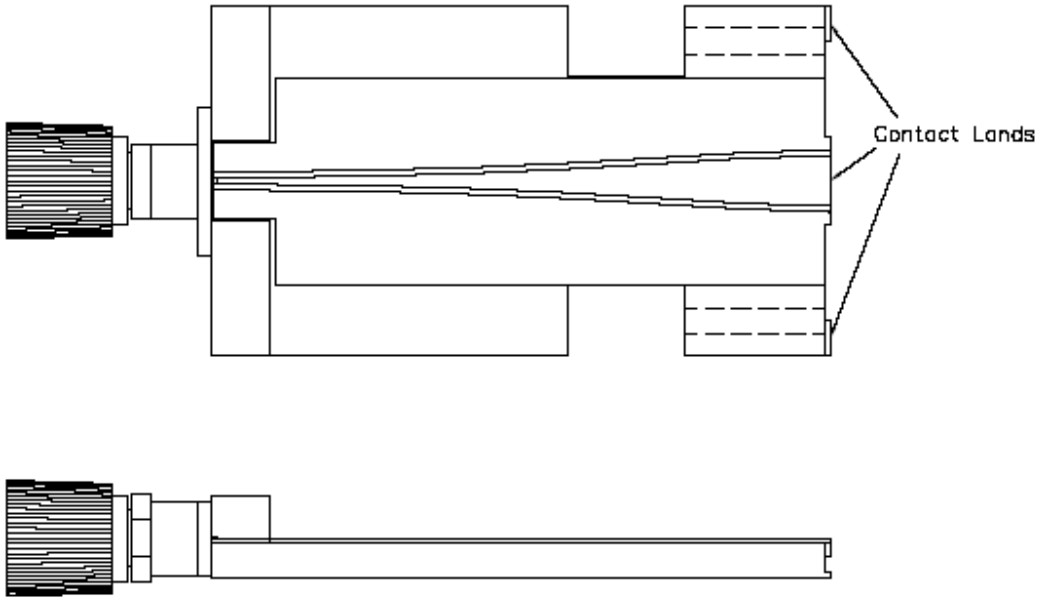

Fig A1.1.2 *The 10 ohm Transformer Base, showing the three contact lands.*

The height of the mounting block flange area has been set such that with the transformer lowered as far as possible the lowest tab heights expected will be in alignment. To assist in adjusting the transformer height accurately two M3 X 0.5 set screws are fitted through each transformer. With the transformers loosely clamped, the screws may be turned to raise the height of the microstrips relative to the flange in a controlled manner, one full turn representing 0.5mm change. In order to prolong the life of the mounting blocks, steel balls are fitted at the points where the screws will contact.

To evaluate these concepts a mock up was constructed in aluminium, and this was found to function as expected. Two minor points were noticed; that it was desirable to put the height adjustment screws as close as practical to the clamping faces, to give as straight a lifting force as possible, rather than a levering effect, and that the tensioning nuts on the clamping screw were too short for easy manipulation. Both of these points were addressed in the final transformer design

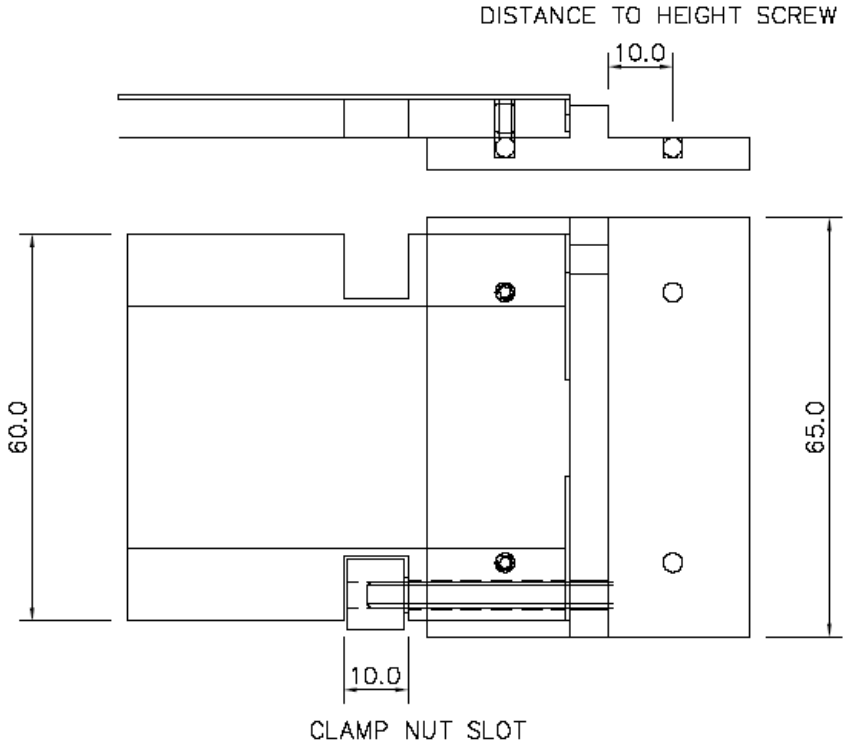

Fig A1.1.3 *The aluminium mock up showed the height screws needed to be closer to the device land, and that longer tensioning nuts would be easier to operate.*

It is vital that a good electrical contact be maintained between the tabs of the device under test and the transformer conductors, as well as affecting the RF measurements, loss of gate bias voltage to a depletion mode transistor would result in device failure due to uncontrolled channel current. Enhancement mode RF FETs are also likely to fail in this circumstance, as leakage from the channel to the gate will rapidly build up enough charge to allow a large drain current to flow.
To avoid such problems sliding wedges of a low dielectric constant material (PET) were supported on a bridge arrangement such that pressure can be applied to the device tab, holding it firmly against the transformer trace.

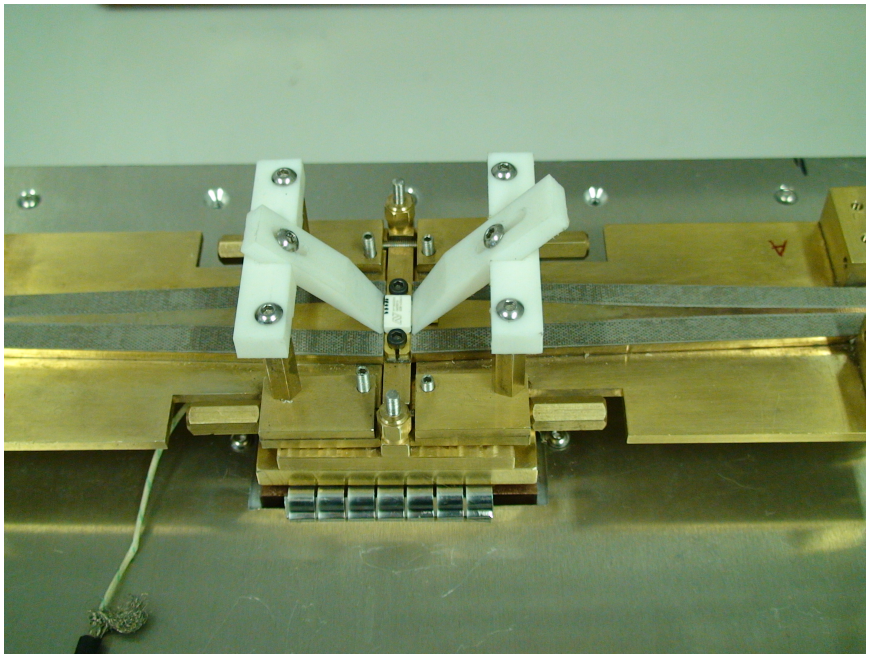

Fig A1.1.4 *The Device Tab Clamps in place on a Nitronex GaN device.*

EM modelling using Ansoft's HFSS indicated that these wedges would have no significant effect on the RF behaviour, even so all calibration measurements were made with them in place, so that they will be taken into account correctly.

A1.2 RF Transformer Design

One of the main RF design requirements is to reduce the 50 ohm impedance of the test equipment down to 10 ohms, which is much closer to the typical output impedances expected of high power RF devices. The amount of RF energy required to create optimal matching conditions is greatly reduced by this approach. [14, Zaid Aboush, "High Power Active Harmonic Load-Pull System for Characterization of High Power 100Watt Transistors"]. The transformers are required to have very wide bandwidths, due to the range of fundamental frequencies used and the need to include as many harmonics as practical. The design goal was 800 MHz to 18 GHz. Tapered line sections were used to give the shortest length possible for the bandwidth and transformation ratio. The microstrip substrate was chosen to give a close match between the 10 ohm line width and the tab width of the intended transistor packages, to minimise step discontinuities. For devices with significantly different tab widths a different set of transformers would be needed. A quantity of 0.020" thick Taconics RFP-35, a ceramic loaded PTFE/glass weave laminate, was available with 0.5 oz/square foot copper foil on one face, with 3mm thick copper on the other; this gives a very good combination of mechanical and electrical properties, as listed in table A1.

Part no.	Composition	ε_r	tan δ	Volume Resistivity	Surface Resistivity
RF-35P	PTFE ceramic - glass	3.5	0.0025	10^8 Mohm/cm	10^7 Mohm

Table A1

To facilitate simple and accurate calibration of the fixture it was specified that APC-7 connectors be used. The APC-7 connector is a high precision part, specifically intended for laboratory use. The genderless construction of the RF contacts allows a device under test to be inserted into a calibrated system without the need to add or remove adapting parts, and the clearly defined mating plane allows precise phase measurements.

Fig A1.2.1 *The APC-7 Connector showing the genderless contact faces, the threaded retaining rings screw back into each knurled nut, so a male or female thread can be set on any part.*

Once the S-parameter blocks for the transformers have been extracted they may be used to mathematically remove the effect of the transformers from measurements performed at the coaxial ports to reveal the performance of the device under test, a process known as de-embedding. A reliable and repeatable calibration of the rest of the system may be carried out at the APC-7 plane using commercial standards, and then transferred to the microstrip ends of the transformers. A significant advantage of this de-embedding approach is that the exact impedance of the microstrip calibration standard lines is not important; as the extracted files are independent of this factor (the impedance must however be consistent across the set of standards).

To permit rapid and accurate design of the microstrip transformer sections and the launch from the APC-7 connectors to the microstrips, use was made of Ansoft's High Frequency Structure Simulator (HFSS) and AWRs Microwave Office.
The line widths for 50 ohms and 10 ohms were found using the microstrip calculator in Agilent's Appcad program, and verified in both Microwave Office and HFSS. Microwave Office was then used to model a circuit comprised of seven linearly tapered line sections

connected in series, the open end of the first section was locked at the 50 ohm width, the open end of the final section to the 10 ohm width. The lengths of all the sections were then locked together and the widths at each junction set to give an approximation to a transformer taper.

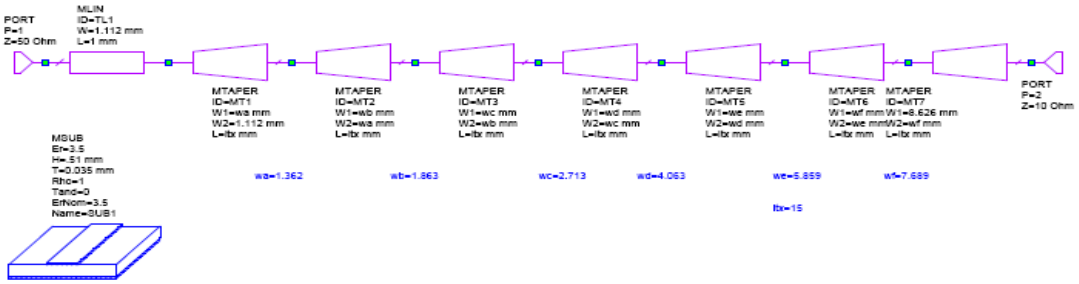

Fig A1.2.3 *The MWO schematic of the taper simulation, variables in blue.*

The optimisation feature of Microwave Office was then used to produce a compact taper giving a good return loss over the band of interest. Optimization is very rapid, as there are only six width variables and a common length value. Note that the characteristic impedance of Port 2 is set to 10 ohms.

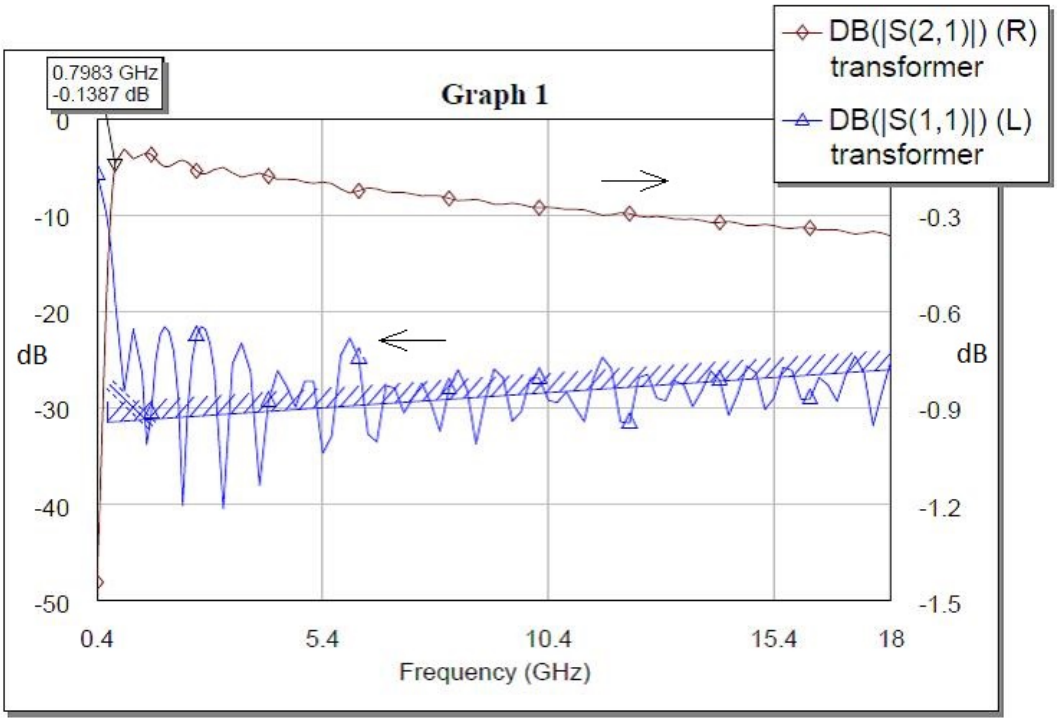

Fig A1.2.4 *MWO graph showing Insertion loss, Return Loss and optimisation goals.*

In order to verify this process the final shape was analysed in the 2.5D EM simulator integral to Microwave Office, and also exported to HFSS for a full 3D simulation. Good agreement was obtained throughout.

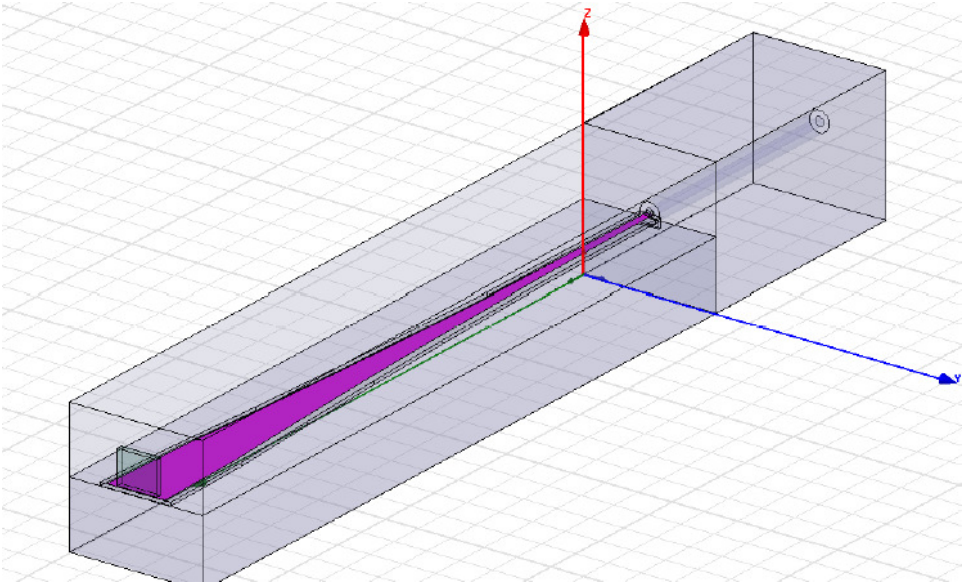

Fig A1.2.5 *The Ansoft HFSS 3D Model of the 10 ohm Transformer & APC-7 Launch.*

The method used here is very fast and takes into account the gradual change in guide velocity, which occurs as the microstrip aspect ratio changes, a factor which greatly complicates the realisation of calculated tapers. The resulting taper is comprised of simple geometric shapes, aiding rapid EM modelling and fabrication.

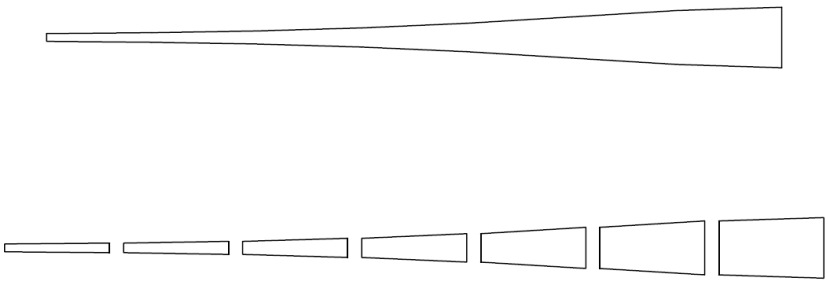

Fig A1.2.6 *The final taper and its segments.*

A1.3 Calibration & Testing

To make meaningful measurements it is necessary to account accurately for the behaviour of the transformer sections, this is done by performing a "TRL" calibration to extract a 12 term error correction model. ("*Applying the 8510 TRL calibration for non-coaxial measurements" Agilent product note 8510-8A*).

TRL stands for Through-Reflect-Line, and refers to the type of standards used to perform the calibration;

Through means connecting the test ports together, either directly or via a length of line.

Reflect means a high reflection standard, either open or short circuit, whichever gives the greater accuracy in the particular situation.

Line means a length of transmission line of the correct impedance, which must be between 20° and 160° longer than the Through standard at all frequencies of interest, since when the electrical line length is 180° no unique solution exists. Several different line lengths are therefore needed to cover our band of interest.

The fixture has been designed to permit direct connection between the two transformers, which will serve as the Through standard. To form the Line standards pieces of the same copper backed substrate used for the transformers were mounted on 16mm, 10mm and 6mm wide brass blocks with 10 ohm tracks running from face to face. A strip of Kovar alloy soldered across this to protrude 1mm each side gives a good contact to the transformer tracks. Gold on silver plating was applied to ensure reliable contact. The 10mm length will permit operation from 900 MHz to 7.2 GHz, the 16mm from 560 MHz to 4.5 GHz and the 6mm from 1.5 GHz to 12 GHz. Once the length increases beyond 180^{o} the line becomes usable again until 360^{o} is approached.

Fig A1.3.1 *The 10 ohm line references, also shown left is a low impedance line.*

.A de-embedding routine created in ADS by Dr Peter Wright was used to extract the S-parameters of the transformers for each line standard. An S-parameter file was obtained for each of the three standards, each one having discontinuities every time the electrical length of the line approached a multiple of 180°.

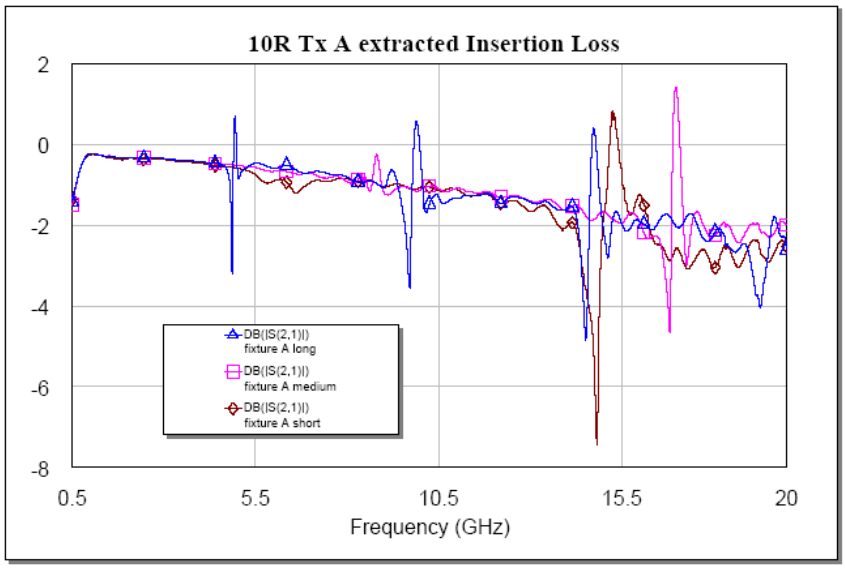

Fig A1.3.2 *S21 of TxA for each of the lines, showing the cyclic discontinuities.*

By consideration of the above graph a line section was selected for each frequency; a composite S-parameter file was then assembled covering the whole of the frequency range.

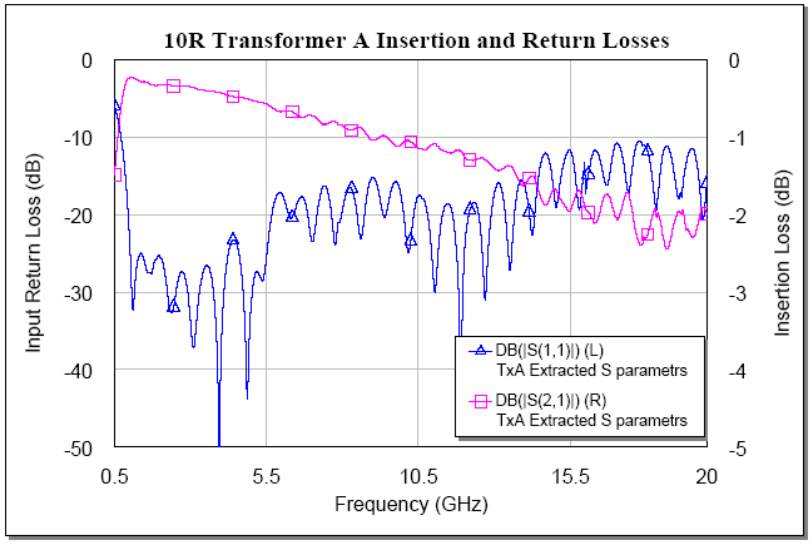

Fig A1.3.3 *The composite S-parameter file for TxA.*

Using MWO the composite S-parameter files were assembled "back to back" and then compared with the physical back to back measurement. Very good agreement was obtained, confirming that the mathematical processes have been carried out correctly.

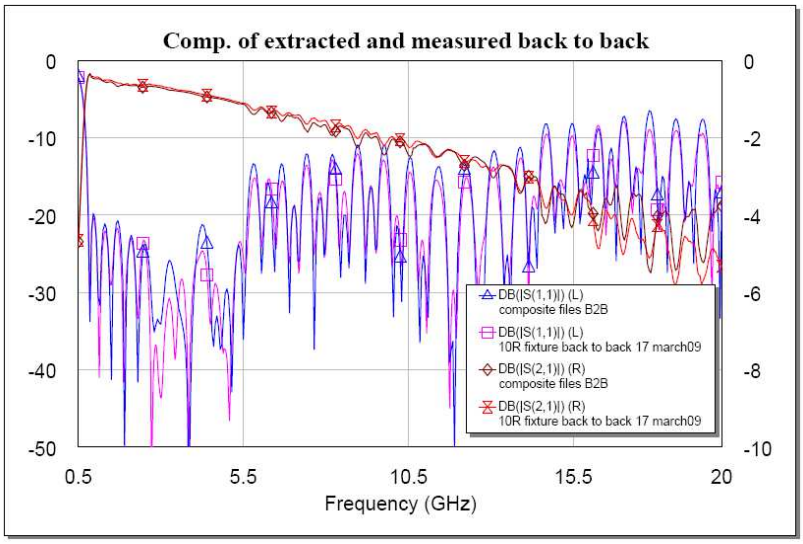

Fig A1.3.4 *The extracted S parameter files connected together compared with the measurement of the physical transformers connected in the same fashion.*

The 50 ohm adaptor sections were also measured at this time using three 50 ohm line standards, 6mm, 10mm and 16mm.

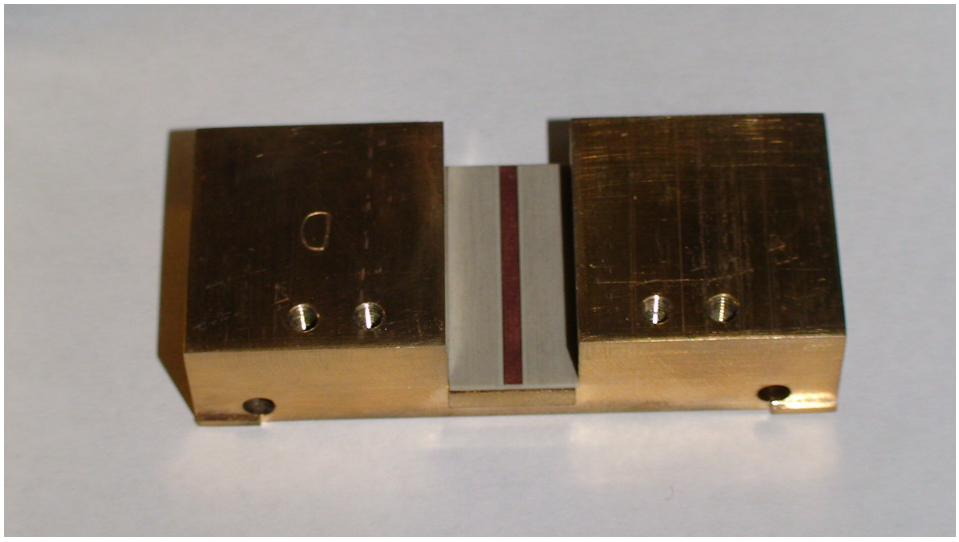

Fig A1.3.5 *One of the 50 ohm adaptors seen without the APC-7, the three earth lands can be seen on the device mating face.*

Dr Peter Wright's ADS routine was again used to extract S-parameter files for the 50 ohm adaptors and the process detailed above was used to select parts of each file to use to form composite full frequency band S-parameter files.

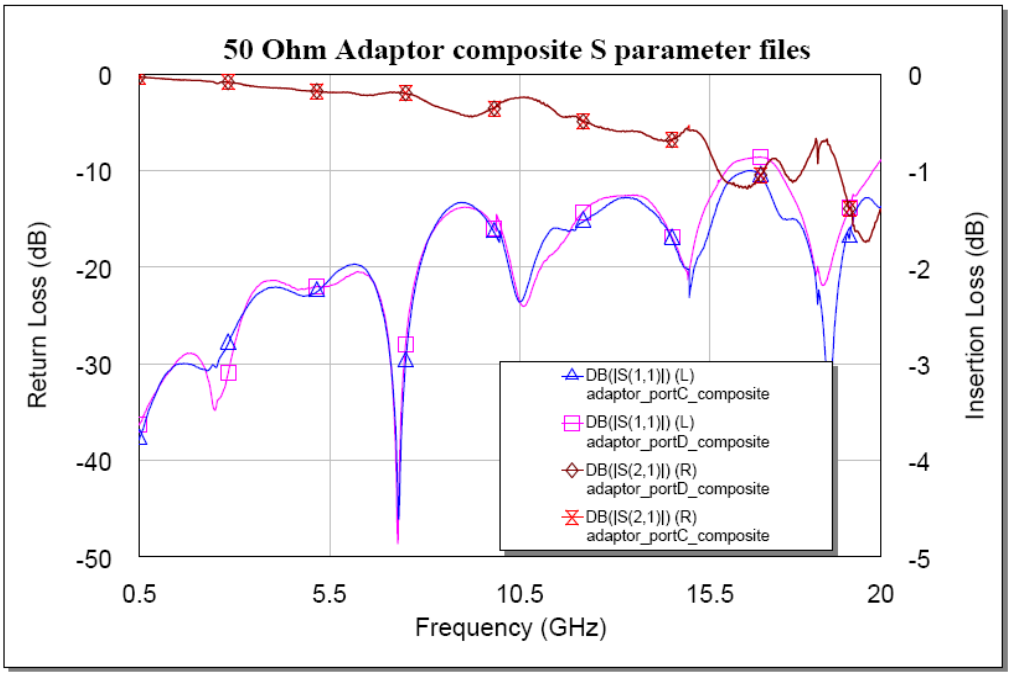

Fig A1.3.6 *The composite S-parameter files for the 50 ohm adaptors.*

A1.4 High Power Testing

The system was fitted with a Freescale PRF5S21100, a 100 Watt LDMOS part, using the 10mm device mounting block. A passive tuner was used to give the correct load impedance, obtained from earlier measurements made with the solid type fixture. The device was then driven to 80 Watts output power. This represents considerably higher thermal and electrical loads than the initial applications the fixture was designed for, 45 Watt GaN parts. Not only is the DC drain current and forward RF power higher, but a large reverse wave is needed to pull the load from the 10 ohms of the transformer to the 2 ohms of these large devices.

A K type thermocouple was fitted into the groove machined in the device mount for this purpose, enabling the temperature of the underside of the device flange to be monitored. The cooling system was in purely passive mode for this test, that is to say the TEC was removed from in between the clamping plates.

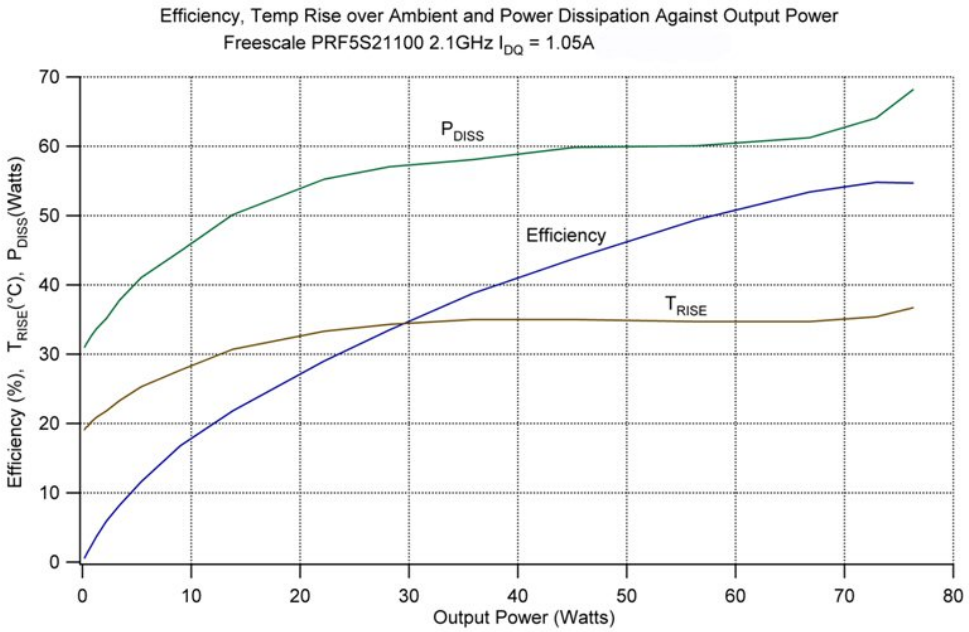

Fig A1.4.1 *Results for a 100W LDMOS part with the fixture in passive cooling mode.*

The results above show that the passive cooling system is capable of coping with the 100W LDMOS device.

It is possible to calculate the die temperature by using the manufacturer's supplied thermal resistance figure, see fig. A1.4.3 below. It is interesting to note that the die temperature is largely constant over a considerable power range, unfortunately not covering the backed off level typically used for linear applications. It seems possible that thermal memory problems could be sidestepped in a phase shift keying modulated system by restricting the range of permitted shifts to ones which stay within this level temperature window. Once the efficiency stops improving with increasing output power then the dissipation and hence die temperature climb again.

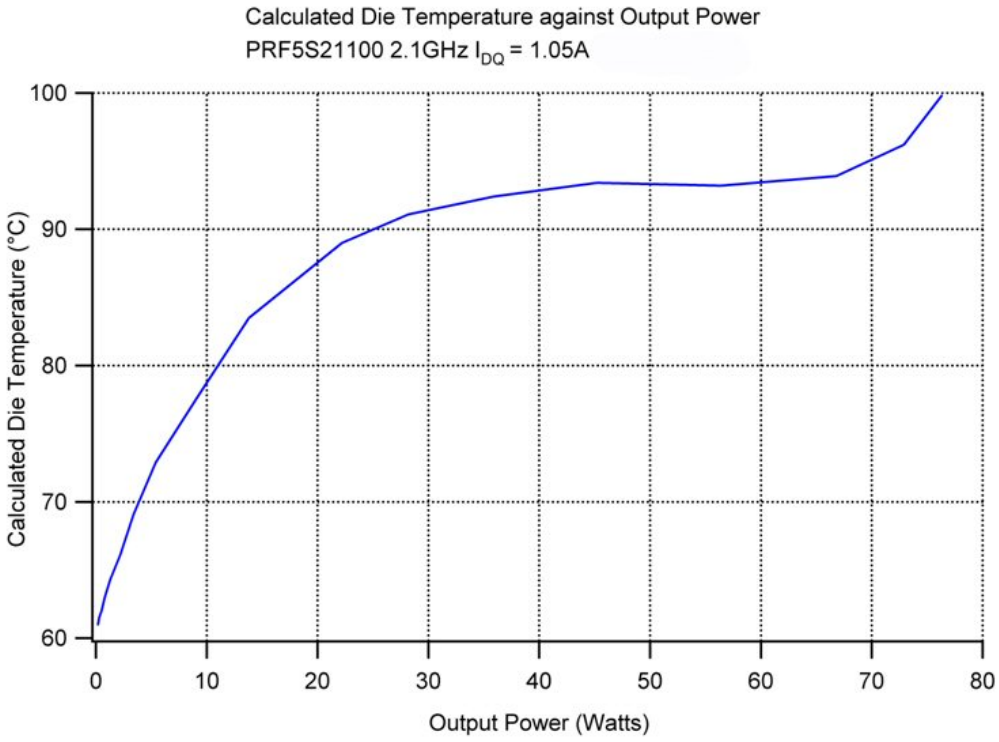

Fig A1.4.3 *Die Temperature against output power for the 100W LDMOS device.*

After the transformers and the passive elements of the cooling system had been proven in this way the Peltier was placed in position and the cooling control system prepared for testing.

A2: The Chassis & Cooling System

A2.1 Design Outline

It was realised early on in the project that the cooling targets were unlikely to be met by attempting to pass the heat from the device mount to the air via a Peltier effect device fitted with a passive metal heatsink. Peltier devices only work efficiently with relatively small temperature gradients across them, and contribute a good deal of heat to the thermal load. The decision was taken that a liquid intermediate stage would be used, allowing a lower thermal impedance sink to be used while keeping the working height low.

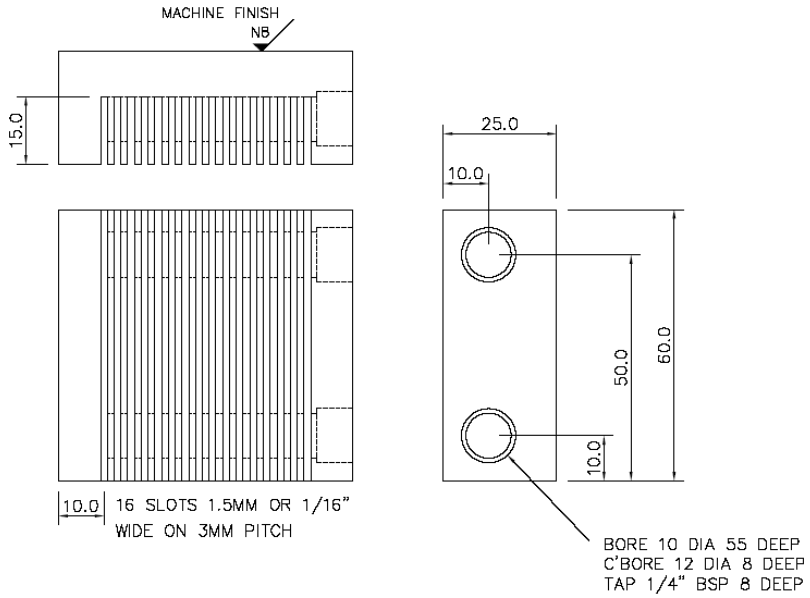

Fig A2.1.1 *The Tellurium Copper Heat Exchanger.*

The liquid heat exchangers needed for this project were designed in copper, to give a very high surface area and a low flow resistance. Pure high conductivity copper is very difficult to machine, its ductile nature causing it to flow then tear, rather than cutting cleanly. The use of 99.5% pure copper with 0.5% tellurium added gives excellent machining characteristics with no significant change in the thermal or electrical properties. The mating surface for the TEC was finished by lapping on 1200 grit abrasive paper laid over a granite surface plate. It is vital to achieve uniform thermal contact across the face of the TEC,

otherwise some cells will be subjected to very high temperature differences, causing inefficiency at best and possibly catastrophic failure.

The advent of very powerful desktop computers has led manufacturers to produce a variety of high performance cooling components at very low cost, and the use of these commercial off the shelf (cots) parts was regarded as desirable as long as performance or reliability was not compromised. In particular heatsinks based on multiple heatpipes can be obtained for a small fraction of their usual cost, these have a very low thermal resistance, ideal for removing heat from sources such as Peltier coolers. A five pipe “Scythe” cooler with integral fan was obtained; the manufacturers claim a thermal resistance of 0.13°C/Watt for this item.

To confirm the specifications a number of power resistors were attached to the heat pipe cooler and the following results obtained, fig A2.1.2. It can be seen that in this instance very good performance is seen, the measured figure of 0.11°C/Watt actually exceeding the manufacturers claims, fig A2.1.3.

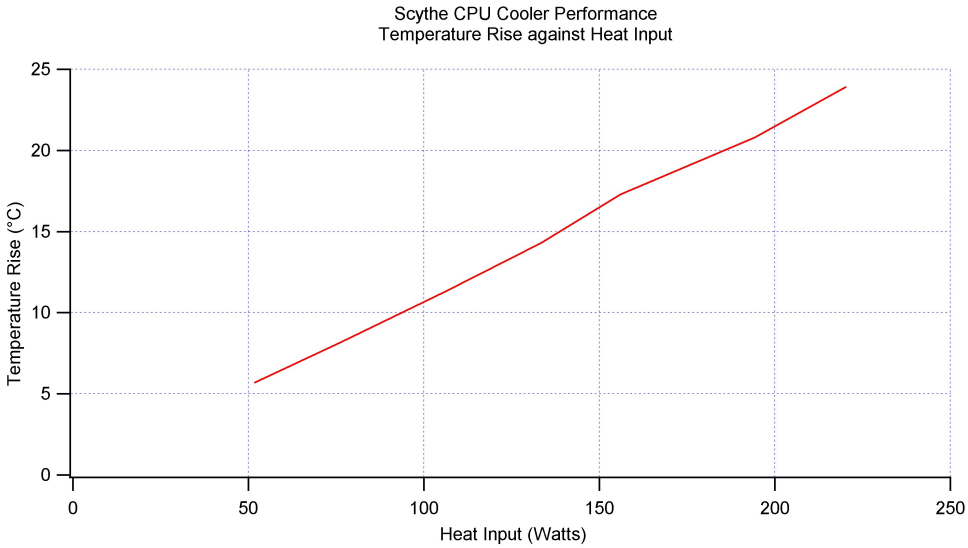

Fig A2.1.2 *Scythe cooler temperature rise against heat input.*

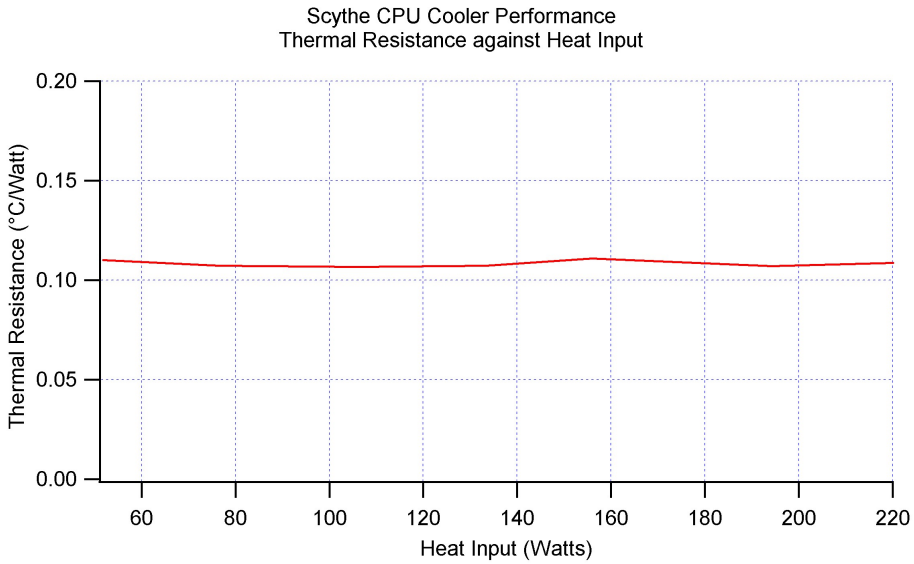

Fig A2.1.3 *Scythe cooler thermal resistance.*

To form the secondary cooler one of these heatpipe sinks and one of the tellurium copper liquid heat exchangers were clamped together in such a way that a second Peltier device could easily be inserted between them at a later date.

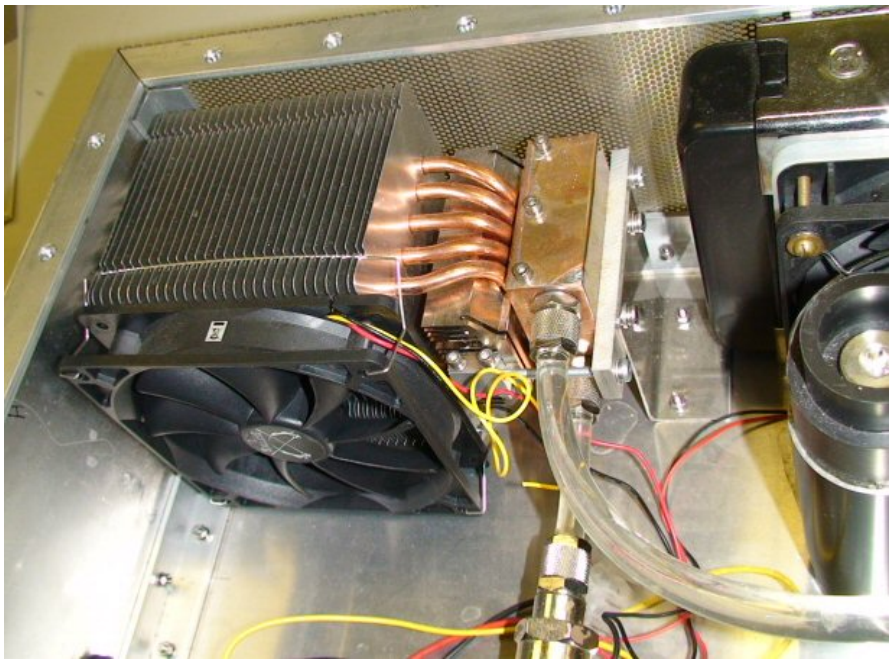

Fig A2.1.4 *The "Scythe" heat pipe cooler clamped to a Tellurium copper heat exchanger.*

A high performance air to liquid exchanger was available, fitting neatly into the proposed chassis this was ideal for the task of primary heat exchanger. A small coolant pump was also available, this was adopted subject to satisfactory performance appraisal.

A2.2 Pump Characterisation

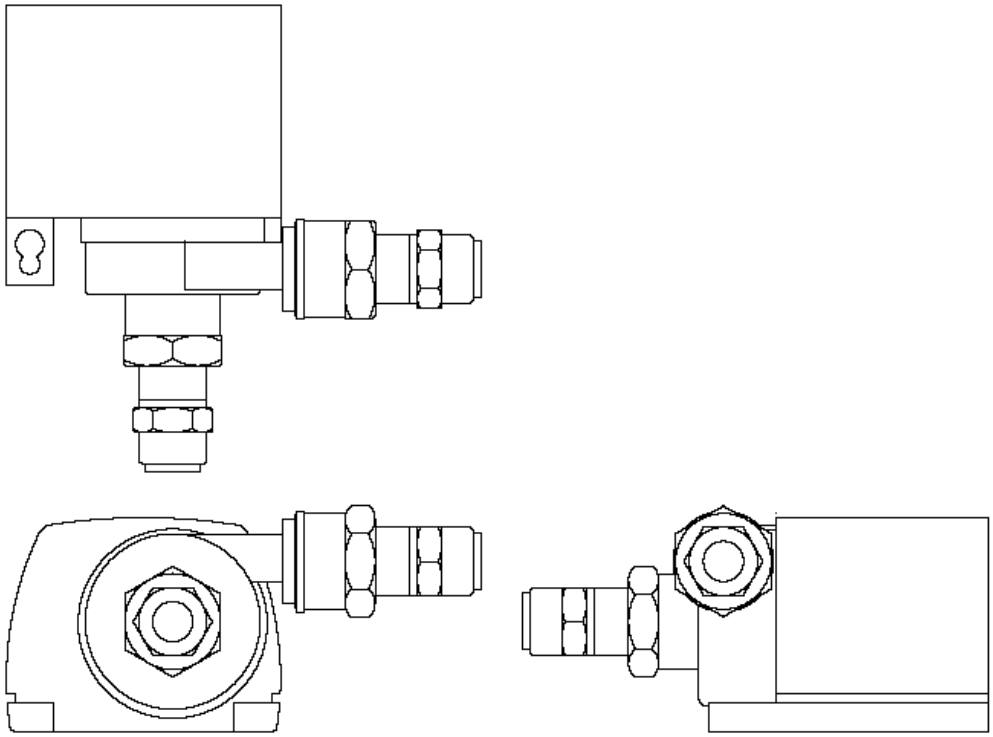

Fig A2.2.1 *The small 12Volt DC pump used for the cooling system.*

In order to predict and analyse the behaviour of the cooling system it is necessary to understand the behaviour of the pump. The published data is very limited and cannot be regarded as accurate. A number of simple tests were carried out, measuring the static head against supply voltage and the flow rate against various heads. It was found that the manufacturers stated static head of 1 metre was very optimistic, barely half this figure being achieved in reality, underlining the importance of verifying the performance of COTS items.

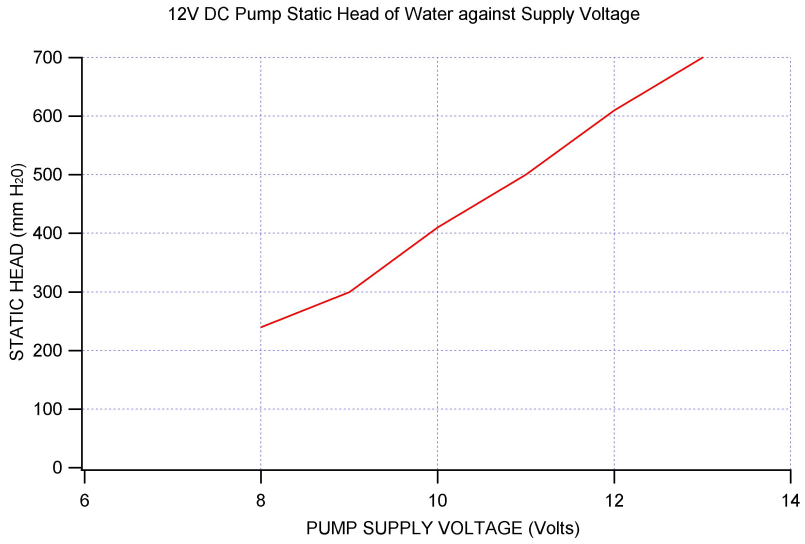

Fig A2.2.2 *Graph of static head against voltage.*

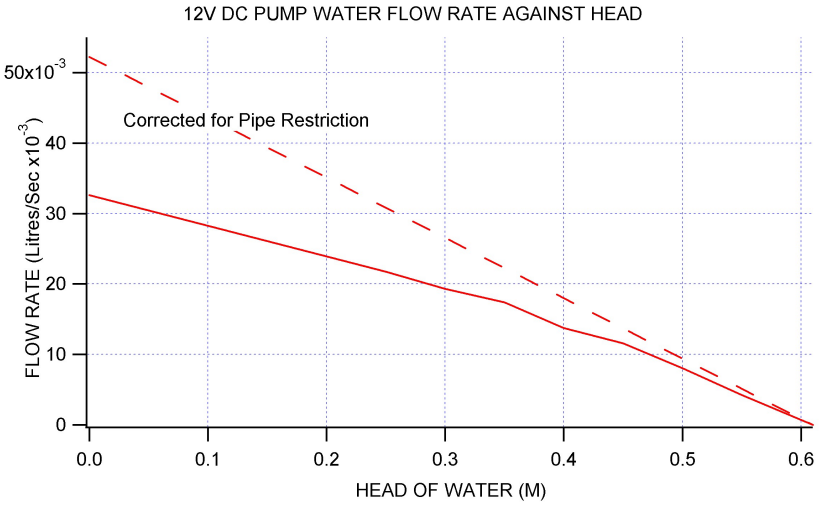

Fig A2.2.3 *Water flow rate against head.*

There is a reduction in flow caused by the piping for the flow rate measurements, at least one metre of pipe is needed to measure the flow at a height of 1m, the error will be more significant at the higher flow rates seen at the lower heads. A corrected line is shown, joining the zero flow point and the flow at zero head *with no pipe attached.* The data gathered should be adequate to predict the cooling capability of the system, or define an adequate pump specification.

A2.3 Chassis Design

Some method is needed to link the components of the cooling system into a stable and practical structure. As well as holding the parts together, the structure must protect operators from hot surfaces and low impedance current sources. Since the unit will operate with high power RF equipment the electronic control systems within must be adequately shielded.
Commercially available chassis units did not meet the specific requirements of this project without excessive compromise, so a custom chassis was designed.

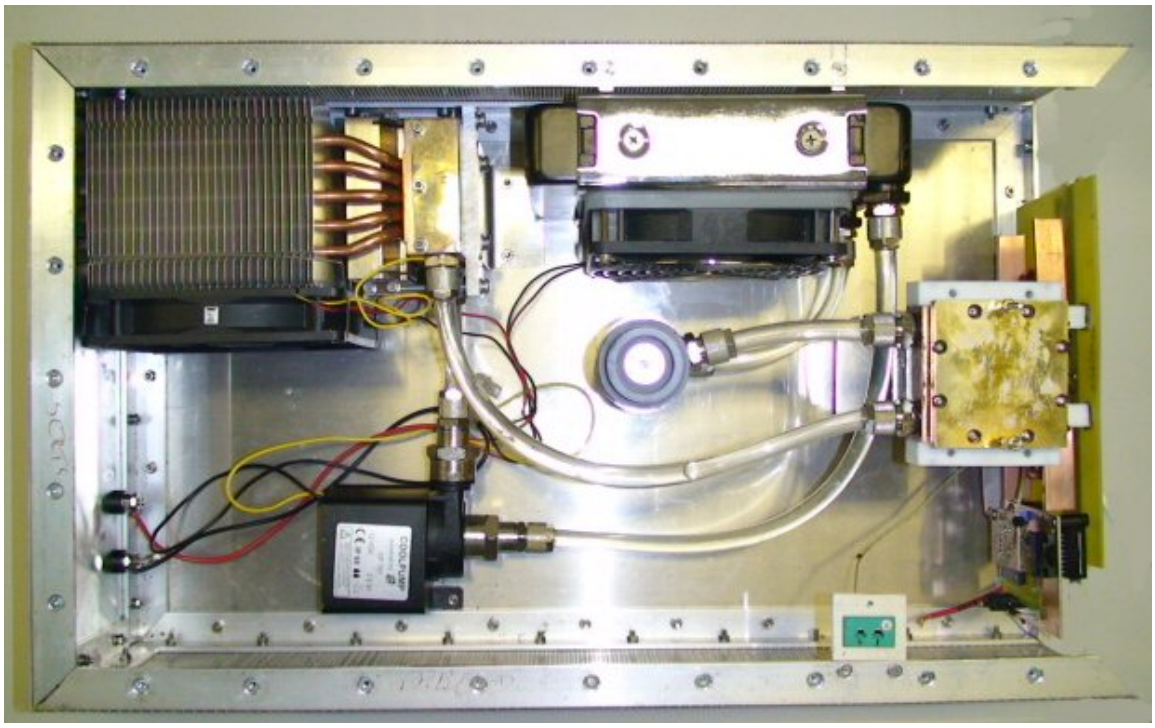

Fig A2.3.1 *The Fixture Chassis at an early stage in the project.*

The base of the chassis is made from 3mm aluminium plate, which is adequately rigid and thick enough to allow countersunk screw heads to be buried in the bottom face, so that the unit does not damage any laboratory furniture or other equipment it is placed upon. All of the cooling system components are attached directly or indirectly to this plate. Aluminium angle extruded sections are fitted around the periphery of this plate, providing added strength, and allowing the attachment of the front, rear and side panels. The side panels are made from 1mm aluminium, the front and rear panels are made from stainless steel

perforated sheet, permitting a free flow of air, while maintaining electrical screening and operator safety.

Angle sections are also fitted to the junctions of the side, front and rear panels, also along their top edges, permitting the secure attachment of the top plate. Made from 3mm plate, this provides a sturdy surface through which the active face of the primary heat exchanger extends. The various RF device mounting blocks are attached to this heat exchanger, and the top plate provides mechanical support for the RF transformers and associated equipment connected to them.

A2.4 Peltier Effect Devices.

The Peltier effect device is becoming widespread in application, allowing prices to drop considerably; some 276 Watt parts were sourced from Custom Thermoelectric Inc for $36-50. Use of these large devices extends the capability of the system, however, the high currents required to fully exercise them pose significant design challenges.

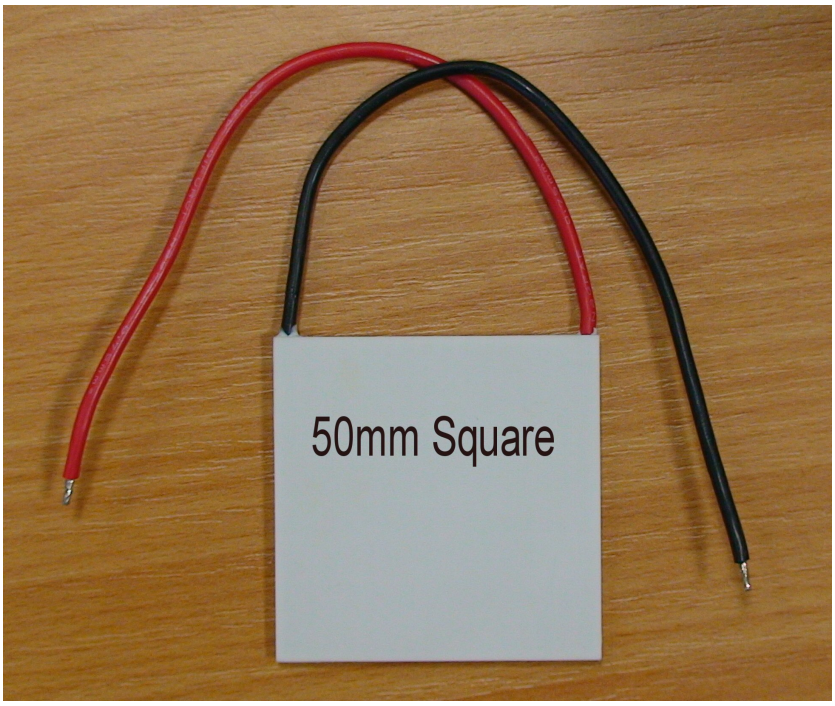

Fig A2.4.1 *The 12711- 6M31-26CW Peltier Device from Custom Thermoelectric inc.*

The relatively large dimensions of these parts precludes fixing them with thermal epoxy, their coefficient of thermal expansion is so different to that of copper that either the Peltier device would mechanically fail, or the epoxy joint would fail, probably causing the Peltier to fail through over heating. Some arrangement of mechanical clamping is required, using thermal grease to aid heat transfer and facilitate any relative expansion and contraction. It is vital the clamping surfaces are very flat, otherwise mechanical stresses may damage the Peltier device, and areas of its surfaces not in good thermal contact with the metal faces will get much hotter or colder than the adjacent regions, leading to reduced performance and possibly failure. A graphite based thermal transfer compound was used to optimise heat flow.

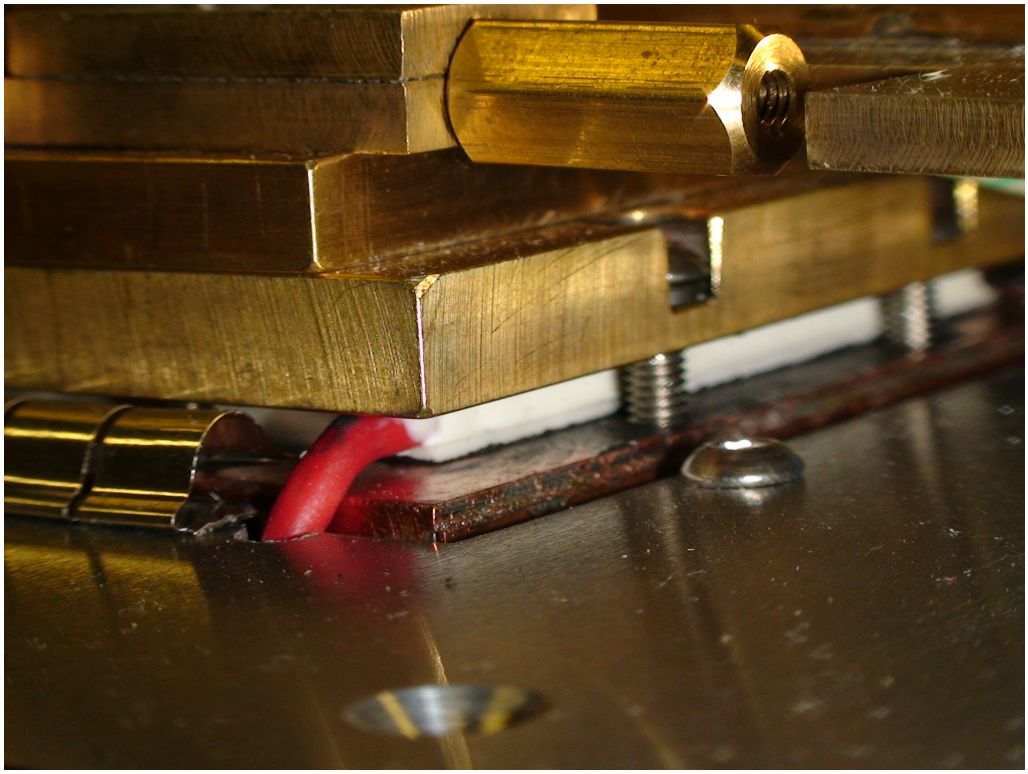

Fig A2.4.2 *The Peltier device in place, traces of the graphite compound can just be seen.*

It was originally intended to clamp the primary Peltier directly between the liquid heat exchanger and the device mounting block in use at the time. However, the surface flatness requirement for the clamping faces, and the need to apply the clamping force in an even, controlled manner suggest that repeated changing of the device block would lead to failure

of the Peltier device. To overcome these problems an additional metal block was inserted between the device mounting block and the Peltier device, this will form a permanent clamp around the Peltier, and the various device mounting blocks may then be attached to this block as required.

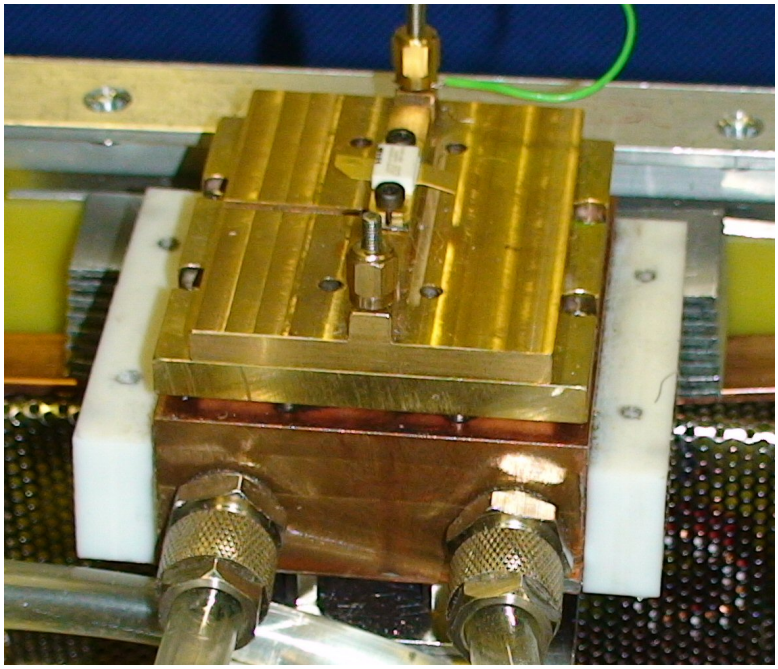

Fig A2.4.3 *The complete device mount, Peltier clamp and heat exchanger assembly.*

The primary water heat exchanger is mounted to the chassis via PET plastic blocks, to minimise heat transfer to and from the chassis lid, which is 3mm aluminium. To maintain electrical screening it was necessary to add the beryllium copper spring fingers seen in the earlier picture, fig A2.4.2.

The metal clamping screws present a direct path for heat to flow in the opposite direction to that which is required, the thermal resistance of this path must be kept as high as practicable. The screws used are A4 grade stainless steel, a relatively poor thermal conductor, the resistance has been increased further by placing nylon washers under the heads of the screws. The use of nylon screws was rejected due to their inferior strength; it was felt unlikely that a consistent clamping force would be obtained. Similarly ceramic

screws were rejected due to their brittle nature, even if trials were successful they may well fail in service due to the strains applied when changing transformers or attaching cables.

A2.5 Thermal Performance Assessments.

In order to gauge the likely performance of the overall system a preliminary test was carried out on the cooling system in a passive mode. The resistor assembly used in the heat pipe cooler tests was fitted in place of the TEC and connected to a DC supply such that 180W was injected into the face of the primary heat exchanger. The system was then left with the pump and fans running until the temperature stabilised, at which time measurements were taken at various points around the loop.

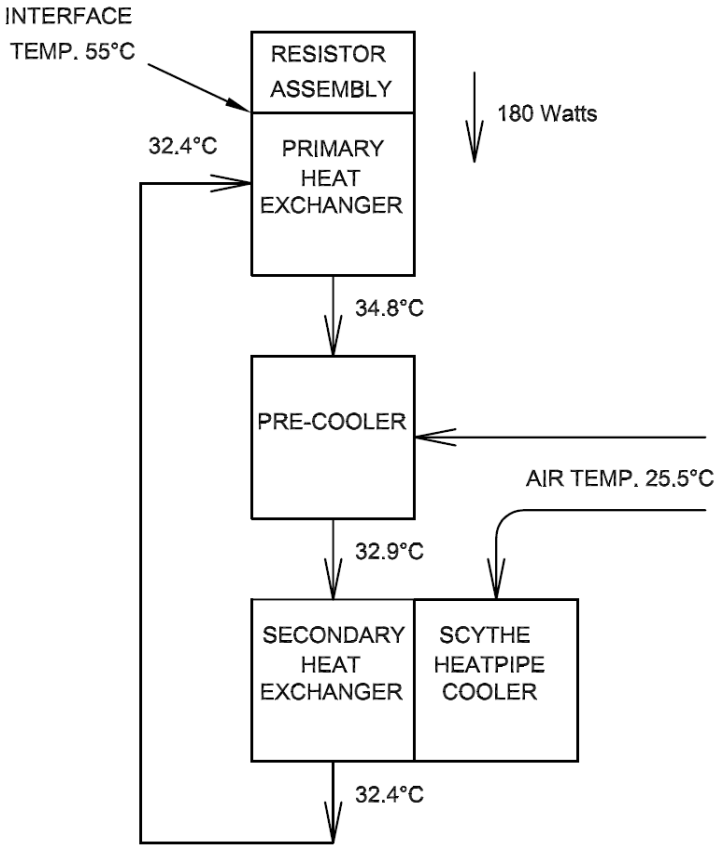

Fig A2.5.1 *Finding the Thermal Resistances of the Primary Heat Exchanger and the overall loop.*

Using the figures obtained from the above test we can see that the thermal resistance of the Primary Heat Exchanger is given by;

$\theta_{phx} = \Delta T\ °C/\text{Heat flow}$

$= (T_{interface} - T_{inlet\ water\ temp})/\text{Heat flow}$

$= (55 - 32.4)/180$

$= 0.125°C/W$

Similarly that for the overall loop is given by;

$\theta_{loop} = \Delta T\ °C/\text{Heat flow}$

$= (T_{interface} - T_{air\ temp})/\text{Heat flow}$

$= (55 - 25.5)/180$

$= 0.164°C/W$

It should be remembered that the heat flow at this point will include the thermal load imposed by the TEC, as well as the energy to be removed from the RF device. The maximum cooling power of the complete system can be found by looking at some of the early results taken while stabilising the control loop (see section 3.4). Before a stable solution was found the system would oscillate between full cooling and full heating, since the thermal mass involved is known the rate of temperature change reveals the rate of energy extraction.

The graph shown in fig. A2.5.2 shows that a temperature variation of approximately 12°C is experienced, over a period of 30 seconds when rising and over 56 seconds when cooling. The asymmetry is due to the TEC being far more efficient at heating than cooling, as the thermal load from powering the TEC is added to the pumped energy in heating mode, this is discussed further in section 3. The target temperature used for this test was chosen to be close to ambient, otherwise heat flow directly from the device mount will influence the result, it can be seen from the graph in section 3.4 that with a set point of 60°C the TEC heating period is longer than the cooling period, despite the greater heating efficiency.

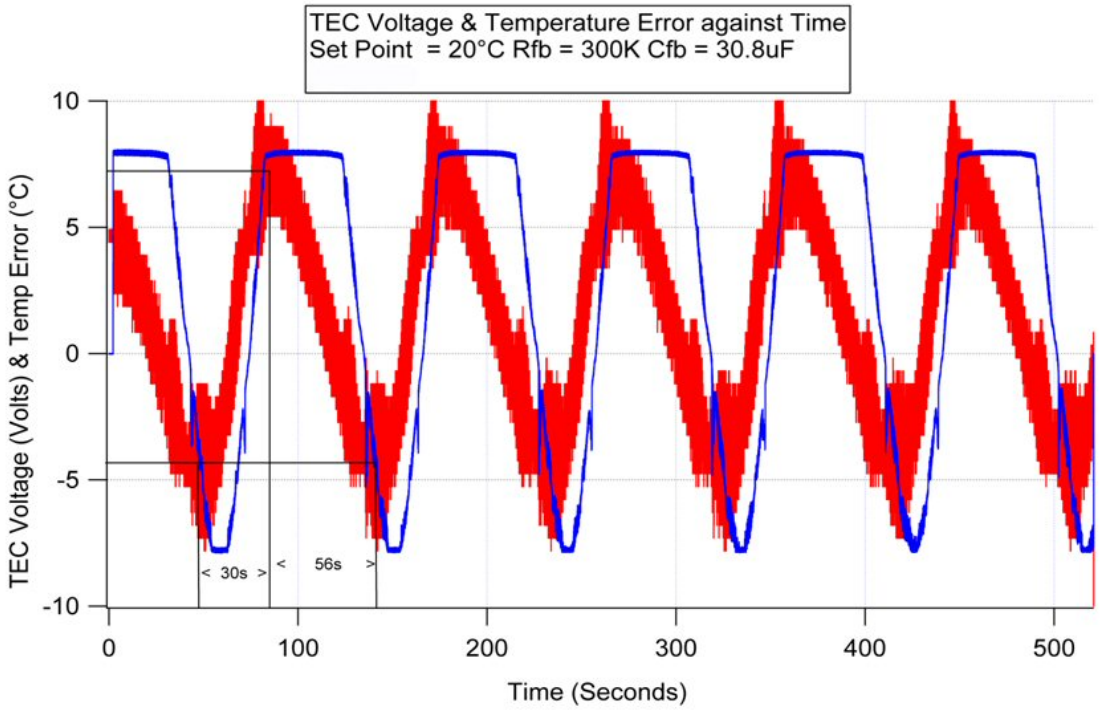

Fig A2.5.2 *The unstable behaviour of the loop in this condition reveals useful information.*

The Cooling power is given by;

Cooling Power = Temperature Change x Mass x Specific Heat/Time

= -12 x 355 x 0.389 / 56 where: Mass of device mount = 355g

= -29.6 Watts Specific Heat of copper = 0.389J/g°C

Similarly;

Heating Power = Temperature Change x Mass x Specific Heat/Time

= 12 x 355 x 0.389 / 30

= 55 Watts

The TEC voltage is limited by the TEC+ and TEC- inputs to ±7.5 Volts, resulting in a maximum current of around 12A, this could be increased by altering the resistive dividers on these inputs to allow a greater current to flow.

A3: The Control System and Interface

A3.1 Design Parameters

In order to maintain the device flange at the required temperature it is necessary to monitor the actual temperature and then adjust the current through the Peltier device as required, it was also a design goal that remote setting of the target temperature be possible via a digital link. Remote monitoring of the temperature and status of the fixture would also be desirable.

A3.2 Temperature Monitoring

Disturbance to the cooling performance must be minimal, so a compact sensor is vital. High RF energy levels may also be present, so a good degree of EMC immunity or the ability to filter the signal easily is a prerequisite. It was decided to utilise a thermocouple to achieve these aims, the thermocouple itself is small and robust, and the twinned wires may be passed around ferrite cores to block common mode RF signals by increasing the impedance.

The voltage from a thermocouple junction is small, and does not relate linearly to temperature measurements in degrees Celsius or Kelvin. Fortunately, these issues have been addressed by Analog Devices Inc, whose AD595 “Monolithic Thermocouple Amplifier” integrated circuit provides a complete solution to using K type thermocouples. The AD595 output is 10mV/°C and as well as being very accurate includes useful features such as open circuit couple alarm. It is straightforward to use the output from the AD595 for input to the feedback loop and status reporting via digital link.

A channel was machined into both the 6mm and 10mm package mounting blocks to allow the tip of the thermocouple to contact the device flange.
A small PCB was made to mount one of these circuits, connecting to the main control board via an 8 pin header. A K-type thermocouple socket was fitted to the top plate of the chassis and connected to the PCB. A K-type thermocouple fitted to the device mount can be

plugged into this. A screened metal casing was fitted to the rear of the K type socket to house the amplifier PCB, and a screened extension lead made to connect between the amplifier pcb and the header on the control pcb.

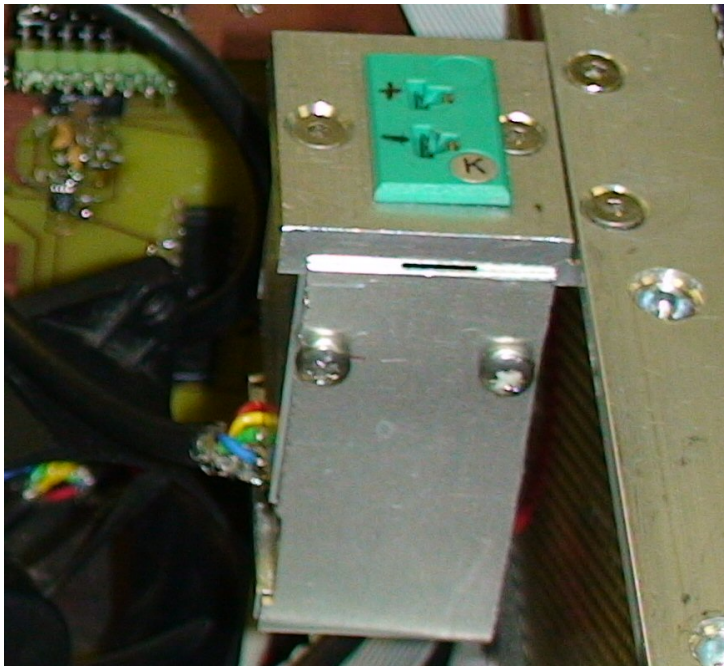

Fig A3.2.1 *The final position of the Thermocouple Amplifier Assembly.*

A3.3 Control circuit

The control circuit compares the actual RF device flange temperature with a reference value and then adjust the current through the Peltier effect devices to control the actual temperature. It is based upon the Linear Technology Corporation LTC1923 integrated circuit, a dedicated Peltier effect device controller. Intended originally for use in laser communication links, this device can both heat and cool, driving the Peltier in a switched mode full bridge configuration. The reference point is set by a DC voltage input, provided by a Digital to Analogue Converter. The digital input can be either set locally by means of a switch bank, or remotely controlled over a digital link, conveniently meeting the project aims. A full set of alarms and monitoring outputs are included in the LTC1923, enabling a high degree of sophistication to be realised.

The digital link was realised simply and economically by the inclusion of a National Instruments USB data acquisition card.

The output stage uses switched mode operation for increased efficiency, which will be vital in this high power application, to reduce the cooling load on the control transistors and to reduce the size and cost of the mains power supply. The TEC requires a smooth current flow, so the bridge driving circuit functions differently to those commonly used for motor drives, where only two arms of the bridge are active for each voltage polarity, and discrete full voltage pulses are applied to give maximum torque and minimum stall speed. Use of such a circuit with a TEC will result in inefficient operation as heat flow is reversed during the off period, (Application Notes for Thermoelectric Devices, Melcor inc 1/12/1992) and can even cause mechanical failure of the TEC due to thermal shock. The LTC1923 circuit functions as two separate switch mode controllers, with the TEC connected between their outputs. As the FET gate signal duty cycle varies, the DC voltages mirror each other, at 50% the voltages will be equal and no current will flow, either side of 50% one voltage will increase and the other will decrease, the relative polarity changing as 50% is traversed. When well away from the set point the gates are no longer pulsed, instead diagonal pairs switch on continuously to give maximum cooling or heating.

The LTC1923 is equipped with FET gate driving circuits intended for use with supply voltages up to 5 Volts, adequate for the small Peltiers used for solid-state laser cooling. The present application calls for higher voltage and current levels, up to 15 Volts and 22 Amps, so some reconfiguration is required, the datasheet provided by Linear Technology for the LTC1923 gives some useful guidance for doing this, and some modelling was done using LTspiceIV to find suitable values for the inductors and capacitors.

Selecting suitable transistors for the high power bridge proved simple enough, Vishay SUP65P06-20 “P” channel parts and Harris RFP50N06 “N” channel parts were chosen, based mainly on channel resistance and switching speed. Finding low loss inductors capable of filtering the switched mode current proved a rather harder task. Commercial 22uH 5Amp parts were obtained, these were wound with 21 turns of 18 SWG (1.2 mm) copper wire. Alternative windings of 7 turns of 14 SWG (2mm) wire were made in order to

get as close as possible to the LTspiceIV indicated value of 10uH, while keeping the flux level within the original design limit of the core. The resulting inductors measured 8uH.

It can be seen from the graph below that the ripple current through the TEC is insignificant with filter values which give a reasonable inductor/capacitor ripple. The larger inductors slow down the settling time from switch on, however this is of no importance in this situation.

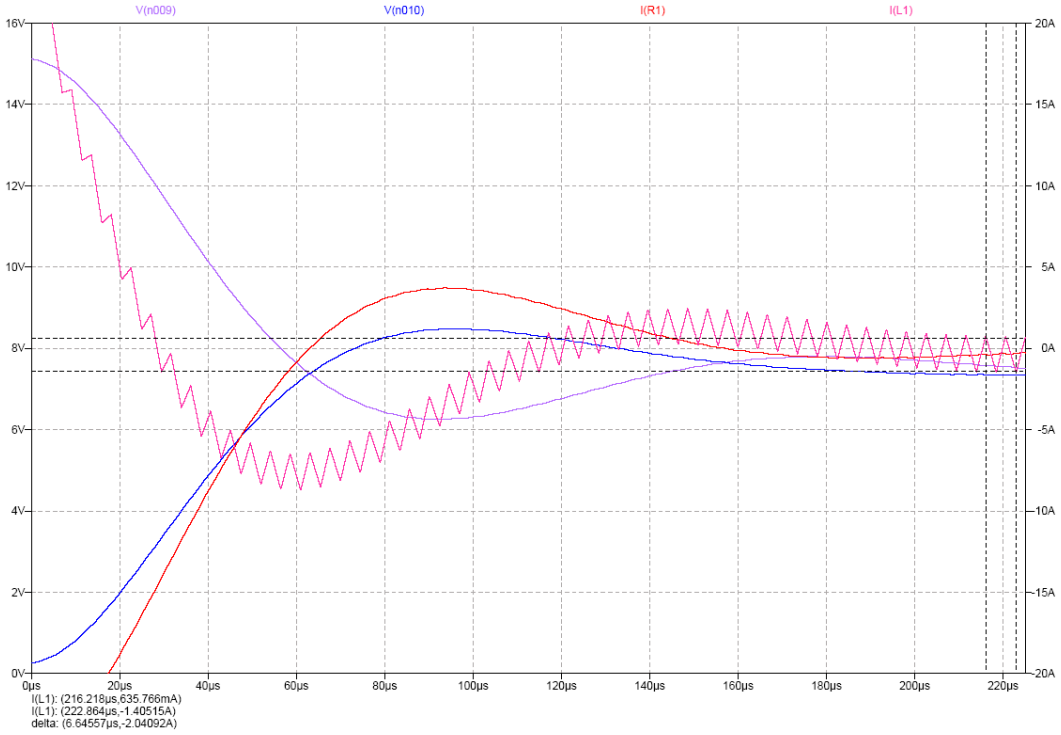

Fig A3.3.2 *LTspiceIV model of the bridge circuit, V(09) and V(10) are the voltages at each end of the TEC, I(R1) is the TEC current, I(L1) is the current in the filter inductor, when L1 = 8uH and duty cycle = 50%. The ripple current is 2.0A.*

To permit the control of the higher voltages and currents Microchip TC4427 FET drivers were added between the gate drive outputs of the LTC1923 and the gates of the FETs. The TC4427 is capable of running from a 16V supply and switching 16V outputs, whilst maintaining 5V input operation. Selecting P and N channel FETs capable of withstanding 15V gate-source bias resulted in a very simple architecture, however to achieve satisfactory operation some expansion of the high power circuit suggested in the LTC1923 datasheet was required.

Using the 4427 driver chips removes the slew rate control feature of the LTC1923, which when directly driving small FETs can control the back EMF generated by the inductors. The very rapid switching speeds given by the TC4427s can cause voltage spikes well over 100V to appear, as well as being undesirable from an interference perspective these would require much higher voltage FETs to be used, which would have a higher "on" resistance due to the longer channel, giving inferior performance. To clamp these spikes Schottky diodes were fitted in a "freewheel" configuration, allowing the current from the inductor to continue to flow either to ground or to the supply rail, effectively limiting the spikes to Vsupply + Vf(diode) and Ground – Vf(diode), where Vf(diode) is approximately 0.4 Volts.

It was decided to install a TTL logic circuit between the LTC1923 and the TC4427 drivers, using a 7408 quad two input AND chip and a 7414 hex inverter the N(a) gate signal was used to generate all four gate signals, providing a simple hardware guarantee that series pairs cannot be switched on simultaneously (fig.A3.3.4). The opportunity was also taken to add an enable line which can be used to switch all the FETs off, this was connected to the fault outputs of the LTC1923 and the AD595 thermocouple chip, as the LTC1923 does not shutdown the FETs when in fault mode, it merely provides a signal that external action is required.

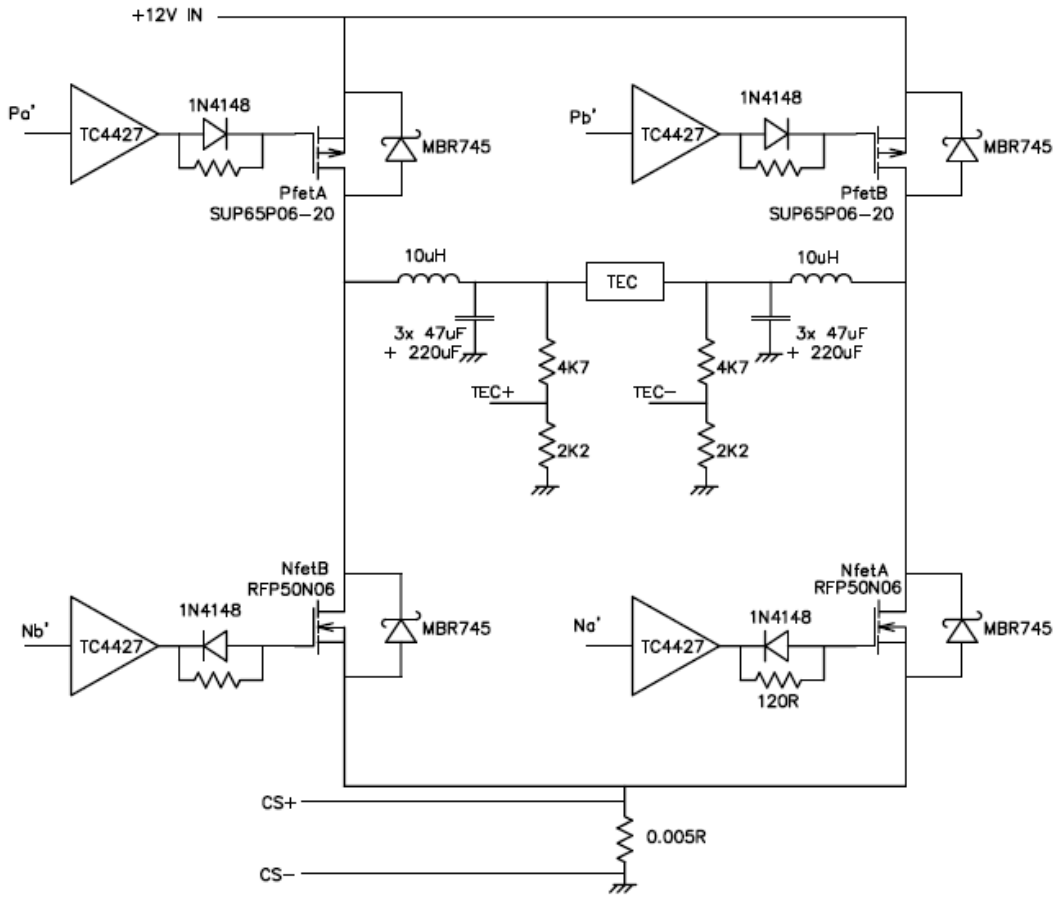

Fig A3.3.3 *The FET bridge used to drive the TEC.*

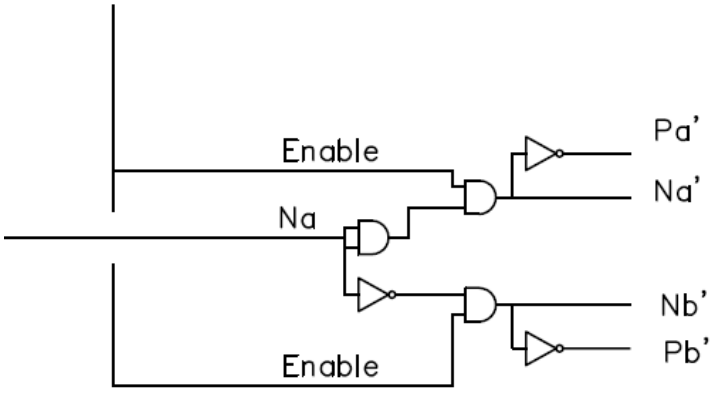

Fig A3.3.4 *The gate drive signals fanned out from the original Na signal by hardware.*

A consequence of not using all the internally generated gate signals is that the delay inserted by the LTC1923 between one pair of FETs switching off and the other pair on is

lost. Resistors were inserted between the TC4427 outputs and the FET gates, paralleled with 1N4148 high speed diodes such that the gate capacitances of the FETs would have to charge through the resistor to reach the on threshold, but would be rapidly discharged via the diodes when switching off. With this modification in place the circuit achieved stable operation, with an air cooled TEC having a very short thermal lag.

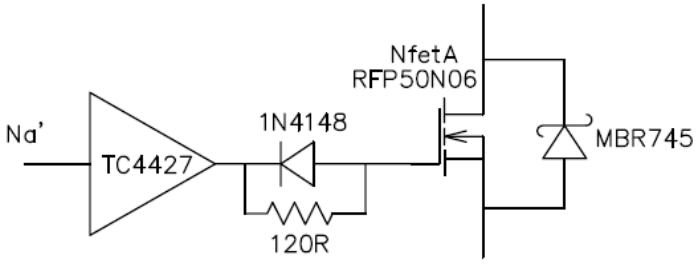

Fig A3.3.5 *FET switch on is delayed by the action of the series resistor and the gate capacitance, switch off is faster due to the diode (diode reversed for P channel FETs).*

To provide the reference a parallel input DAC was chosen, an LTC1450, this has 12 bit resolution and can be configured in "pass through" mode, which allows easy manual operation when used without the remote control link, this was very useful in the initial testing phase. The action of the control circuit tries to set the output from the AD595 thermocouple amplifier to be equal to the output from the DAC, so since the AD595 produces 10mV/°C, this is the output which must be generated by the DAC. The gain and reference level for the DAC were configured to give a maximum output of 2.56V, since the TEC has a maximum operating temperature of 120°C the most significant bit was set permanently low, restricting the maximum temperature to 125°C. The least significant bit is not needed, as it represents only a 0.05°C step, it was felt that the 0.1°C resolution resulting from using the middle 10 bits was more than adequate. A temperature is therefore set by entering the required number of tenths of a degree, for 70°C the binary code for 700 would be imposed on the DAC input.

A3.4 Loop Gain & Delay

Once the control circuit was connected to the rest of the fixture it was possible to begin to finalise the control loop timing and gain parameters, to find the best compromise between rapid response to step changes and stable operation. A simple single pole delay was chosen, as the full range of applications and attachments cannot be fully predicted, so the complex balance of higher order designs might well become upset. The thermal mass of the copper TEC clamp and device mount is significant, some 355g, requiring 138 Joules of energy per 1°C change, therefore the control loop time constant must be much longer than that for the LTC1923's original application, solid state laser cooling.

Upon initial testing a continuous swing between maximum cooling and maximum heating took place, implying that as well as a longer delay much reduced loop gain was required. The asymmetry seen here is due to heat loss directly from the device mount.

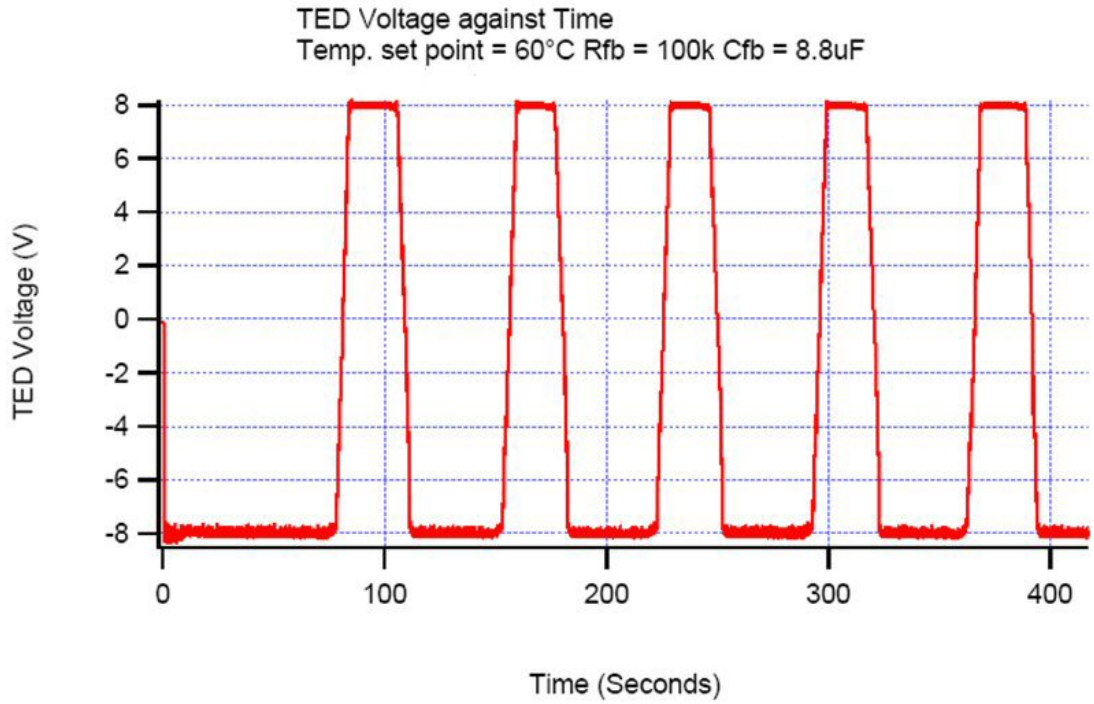

Fig A3.4.1 *Initial tests showed the TEC voltage oscillating between the limits.*

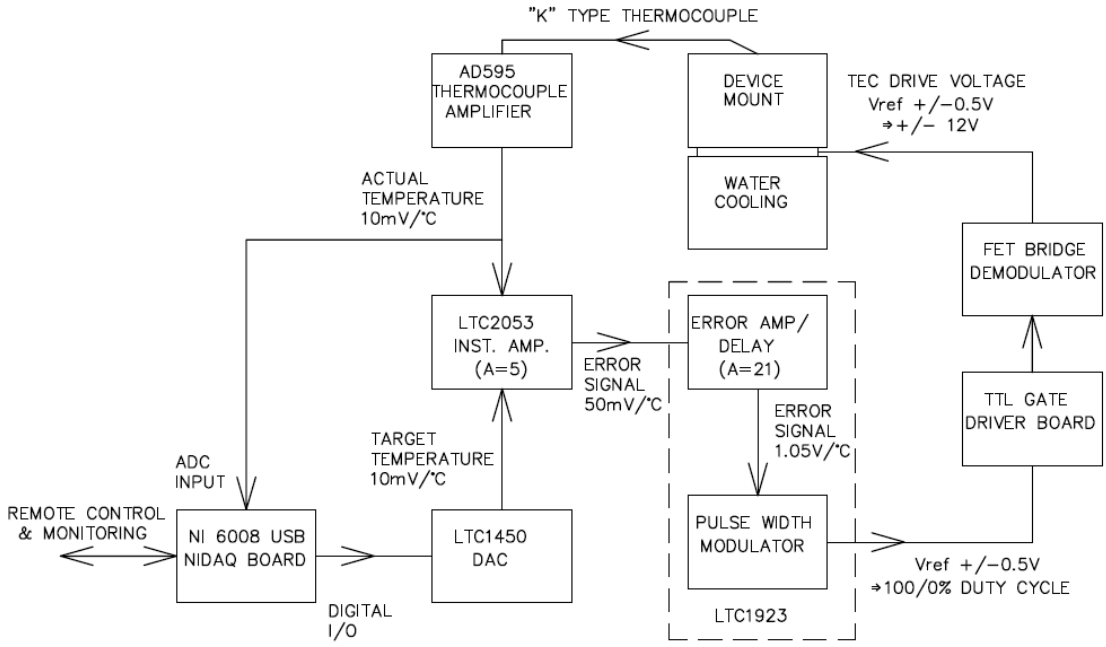

Fig A3.4.2 *Simplified block diagram of the control loop, showing the final gain values.*

The thermocouple output is amplified and linearised by the AD595, the result is fed to the LTC2053 zero drift instrumentation amplifier for comparison with a target voltage produced by the LTC1450 DAC, and also to one of the NIDAQ ADC channels for remote monitoring. The LTC2053 output is passed into the error amplifier inside the LTC1923, the feedback and input circuits of which are used to provide the loop delay and a further voltage gain. The output from the error amplifier is referenced to 1.0V and compared with a 0.5V to 1.5V ramp, the result of this forms a pulse width modulated signal, the duty cycle of which changes from 0% to 100% as the error signal changes from Vref -0.5V to Vref +0.5V. The TTL gate driver board fans this signal out to the bridge FETs, where a 0% duty cycle results in -12V (full heating) and 100% in +12V (full cooling).

Increasing the TEC driver supply voltage from 5V to 12V greatly increases the gain of the modulator/demodulator formed by the ramp comparator in the LTC 1923 (±0.5V for 0 to 100% duty cycle) and the FET bridge (0 to 100% for ±12V out), this can be considered as a switched mode amplifier with a gain of ±12 over ±0.5, that is 24. To compensate for this the gain of the input instrumentation amplifier was reduced from 10 to 5 by changing its

feedback resistor chain, and the 100K arm of the delay loop increased to 500K, reducing the error amplifier gain to 10M/500K + 1, that is 21. With these gain values a difference of 0.5°C between the target and actual temperatures is all that is required to send the controller to full heating or cooling.

Once this was done, and the size of the delay capacitor increased, the loop was found to respond to step changes with a damped ringing, indicating that the gain was now approximately correct but a further increase in delay was needed. Increasing the capacitance to the maximum allowed by the physical constraints of the circuit gave an acceptable result.

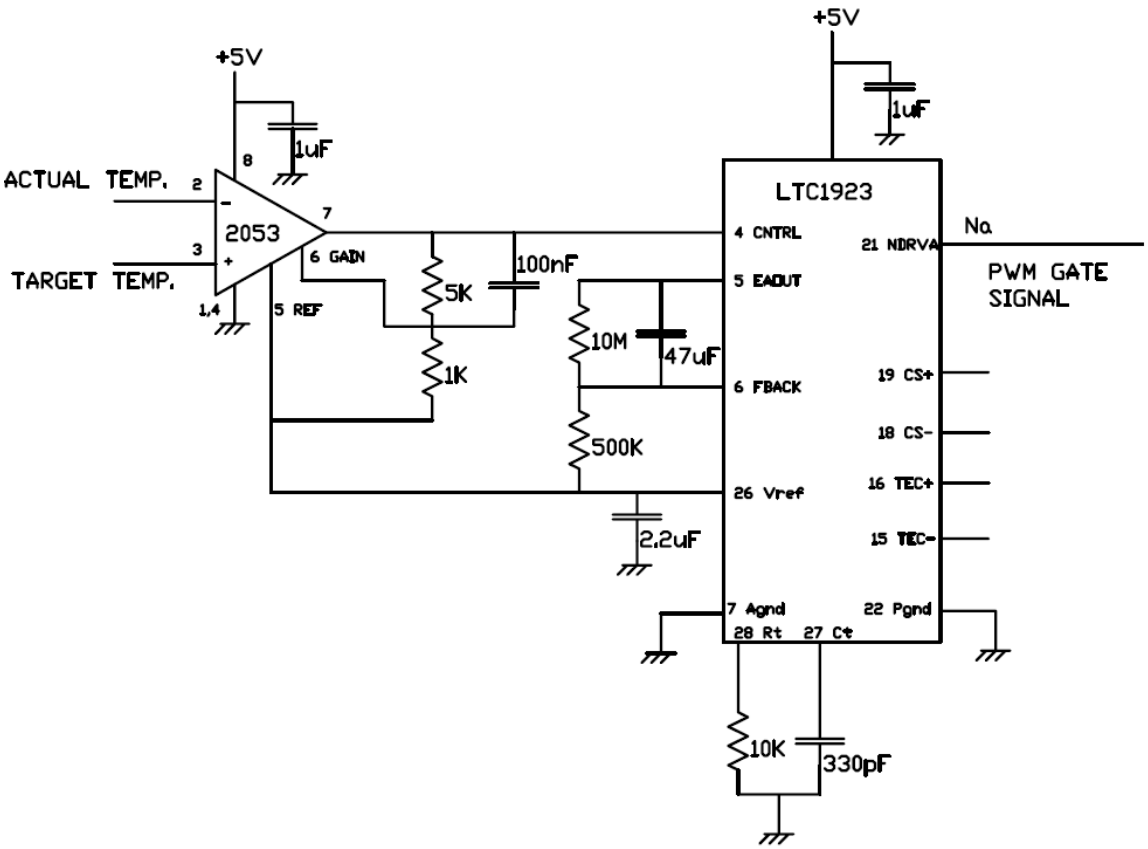

Fig A3.4.3 *The amplification, delay and pulse width modulation circuits of the control loop.*

The type of capacitor used proved vital to the performance, initially 2.2uF 0603 case ceramics were used, but as the overall value increased to 30.8uF without properly damping

the loop these became impractical. The choice is limited by the bipolar performance needed, solid aluminium parts promised a compact high value, but considering the leakage current showed they could not be used in parallel with a 10M Ohm resistor. The final choice was tantalum, the required bipolar performance being realised by placing a pair of 47uF parts in opposing series.

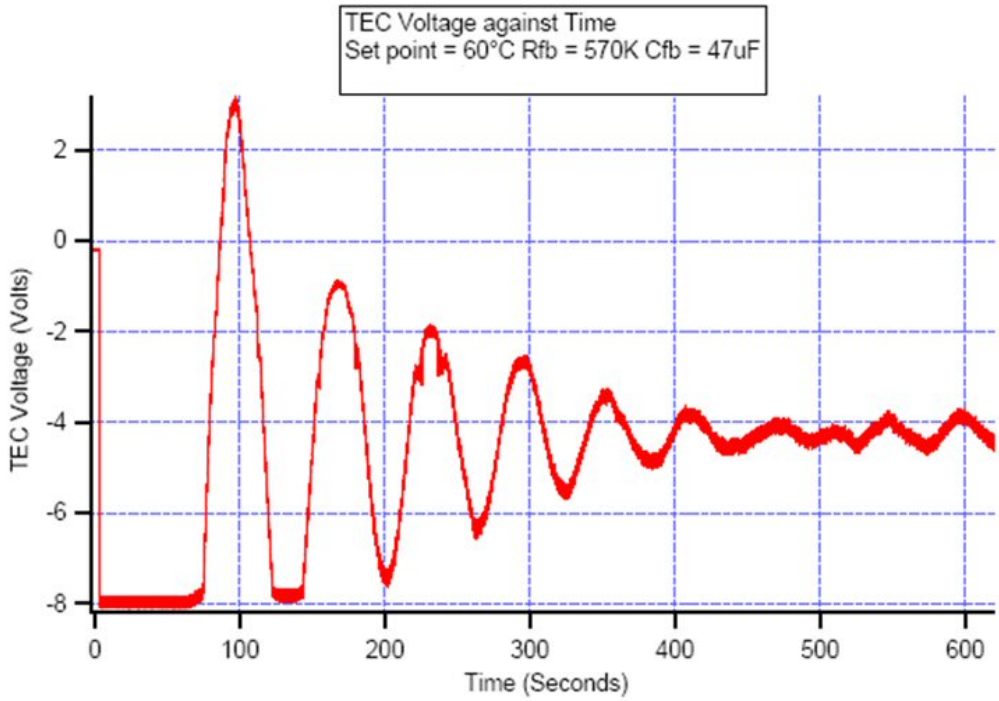

Fig A3.4.5 *TEC voltage against time with 47uF tantalum capacitors.*

When the system was configured for real measurements it was found that the loop behaviour improved, this is due to the position of the thermocouple junction. For the initial loop tests the junction was fitted underneath one of the device block clamp nuts, once moved to its proper slot in the centre of the block the thermal delay was reduced. The behaviour in real test situations can be seen in the graphs below, taken during the power sweep tests discussed in section 4.2.

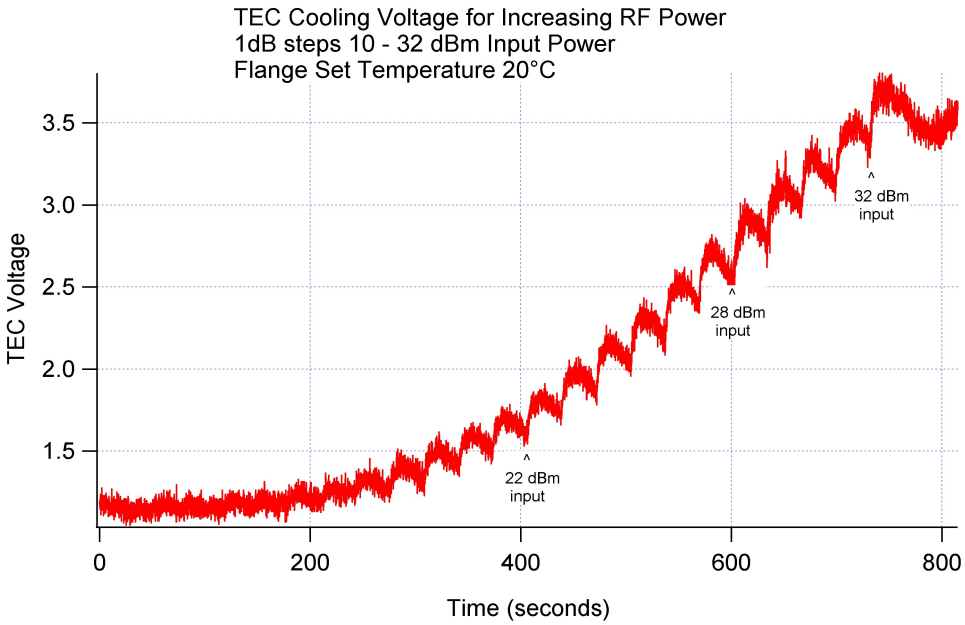

Fig A3.4.6 *The cooling effort increasing with thermal input.*

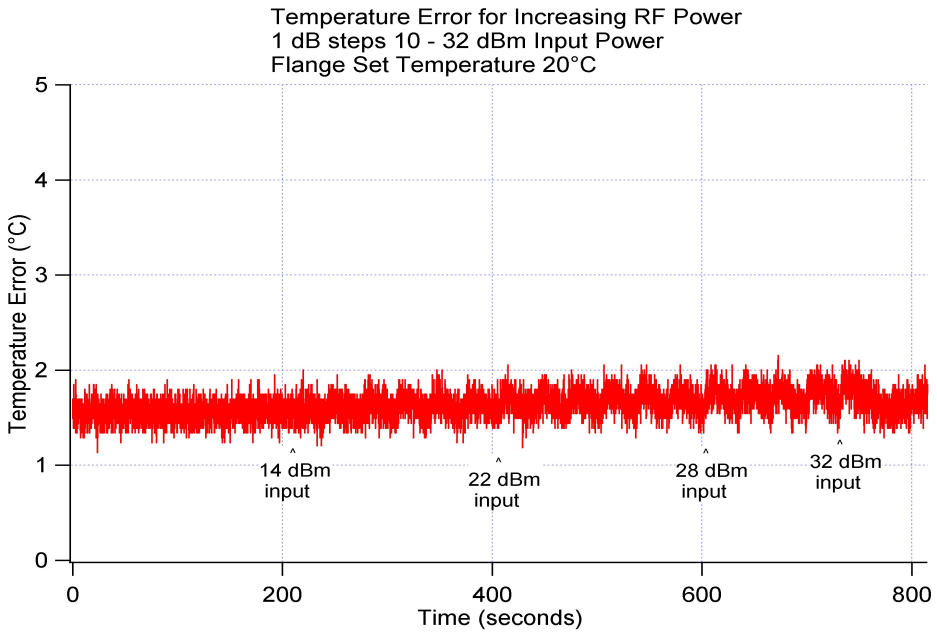

Fig A3.4.7 *The device flange temperature is held very accurately.*

It can be seen that the noise level appears rather high, the performance seen here is the limit of the NI ADC, 7mV, compared to the Thermocouple amplifiers output of 10mV/°C. To improve on this it would be necessary to change the ADC or insert a buffer amplifier with a voltage gain of 10, so making the noise of the ADC equivalent to 0.07°C as opposed to 0.7°C.

A3.5 Remote Control Link

The part chosen for the remote link was a USB-6008-OEM, with 12 digital I/O lines, 4 differential analogue inputs, 2 analogue outputs and an event counter.

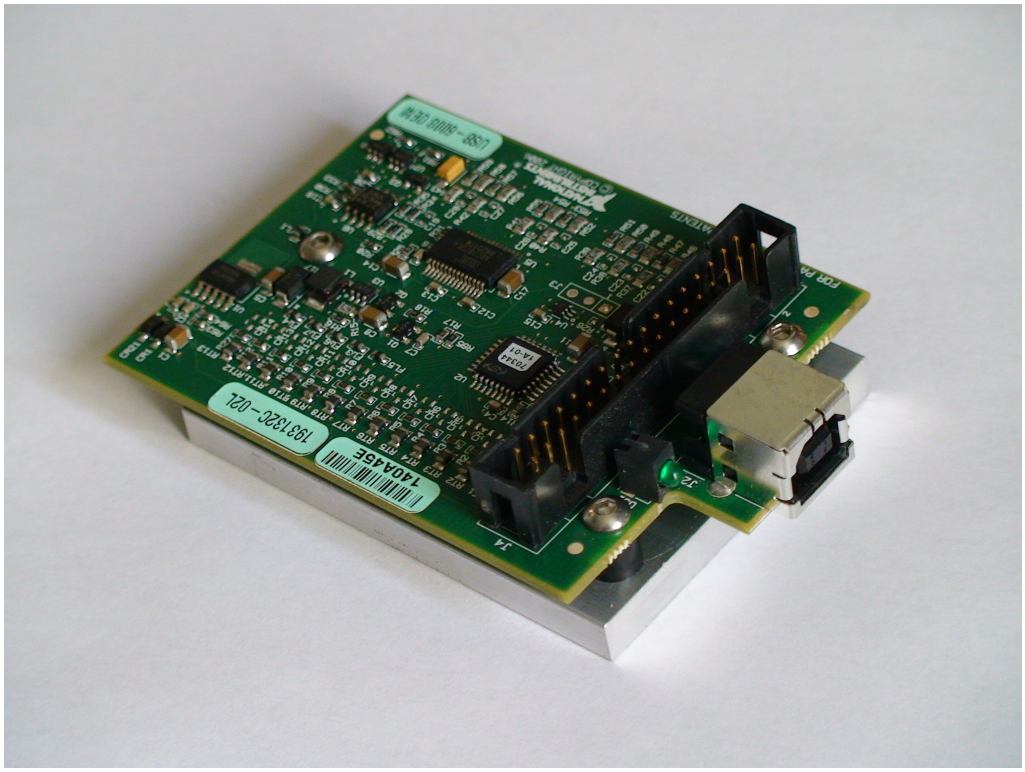

Fig A3.5.1 *National Instruments NI 6008-USB on mounting plate.*

Ten of the digital lines were used to drive the temperature reference DAC, one was used to control the enable line of the output FETs and the last was configured as an input and used to monitor the enable line. Since the enable line is also pulled low by a fault signal from either the AD595 (open circuit thermocouple) or the LTC1923 this provides a useful system monitor function. The Mode Select switch changes between on, off and remote controlled operation.

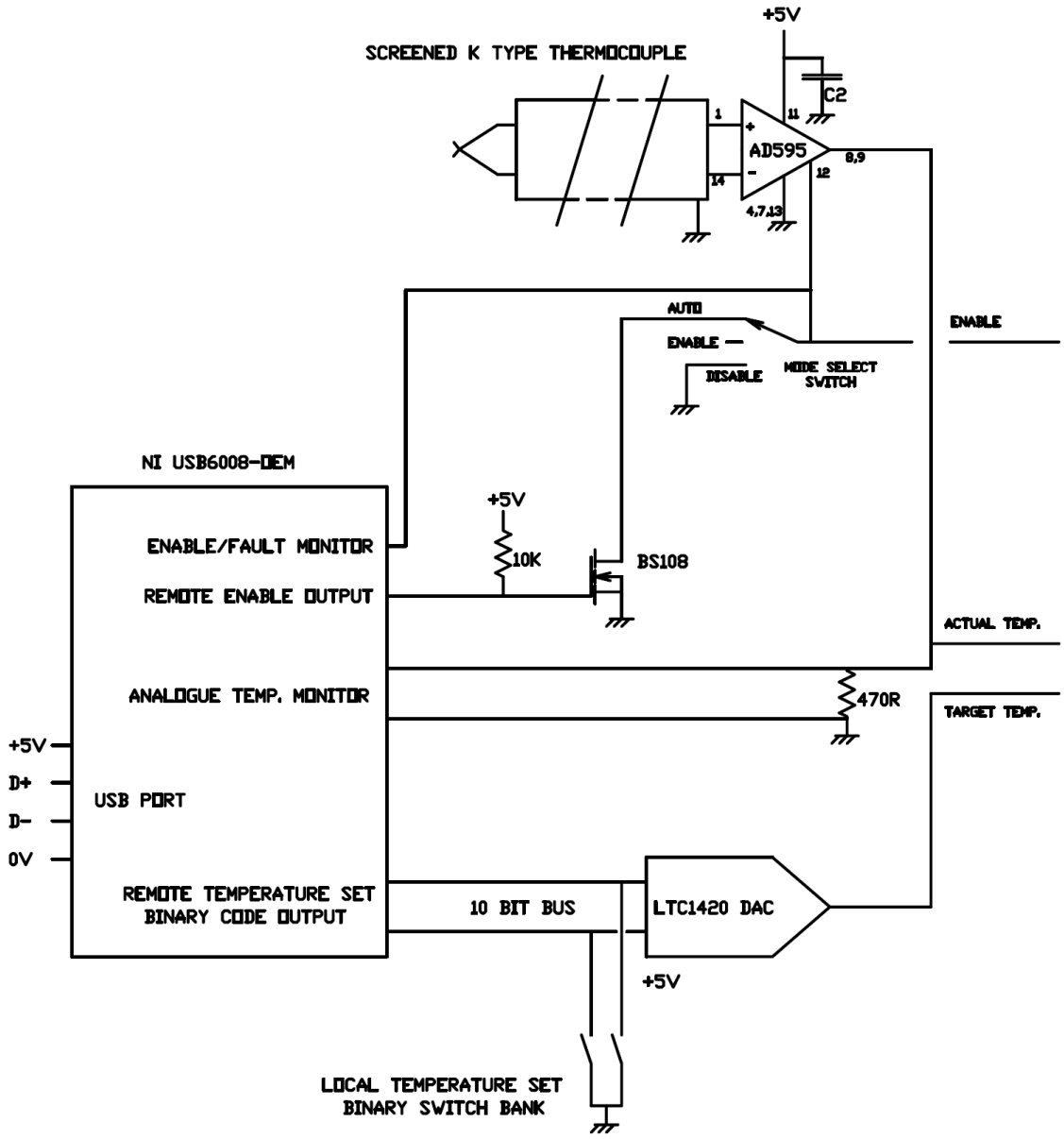

Fig A3.5.2 *The interface and measurement circuits.*

One of the differential analogue inputs was used to monitor the output of the AD595 thermocouple amplifier, providing a convenient way to monitor and record the device temperature when in use. It was found that the AD595 could not control the ADC input, examination of the relevant datasheets revealed that the ADC has an open circuit voltage with respect to ground of 1.4V, and an impedance of 144K Ohms, while the AD595 in single rail mode can only sink current to ground via a 50K resistor, for voltages below 2.5V. Applying Ohm's Law shows that we should expect a minimum voltage around

350mV, preventing measurements below 35°C. The AD595 is capable of delivering up to 5mA, so the problem was resolved by placing a 470R resistor to ground from the output pin. The voltage caused by the ADC input is pulled down to 7mV by this, allowing measurement down to 1°C, but the current drawn is only 2mA at the maximum operating temperature.

Incorporating a buffer amplifier as discussed in section 3.3 would also address this problem, but it should be noted that many op amps have a similarly restricted current sink capability in single supply mode. The scaling up of the signal would of course scale down this problem, and also the AD595 output current at high temperatures would be reduced, resulting in a smaller self heating error. It might seem that the obvious answer is to implement a negative supply rail, as this would also permit the measurement of sub-zero temperatures, however this would potentially result in reverse biasing of the LTC1923 inputs, which is not permitted.

It would be possible to work below 0°C with this equipment, the cooling water would not freeze, as it would be heated by the TEC to above ambient, however it would result in considerable condensation and icing on the RF circuitry unless measures were taken to seal the area from the atmosphere.

A4: Overall Testing

A4.1 The Relationship of Gain, VGS, IDS and Temperature.

Once the system was complete a Nitronex NPTB00050B was fitted to the 6mm device block and used to explore the systems capabilities. The basic active load pull equipment was used for this, but in passive 50 Ohm mode, resulting in nominal 10 Ohm impedances at the device tabs.

The first test was to measure the dc characteristics at various temperatures.

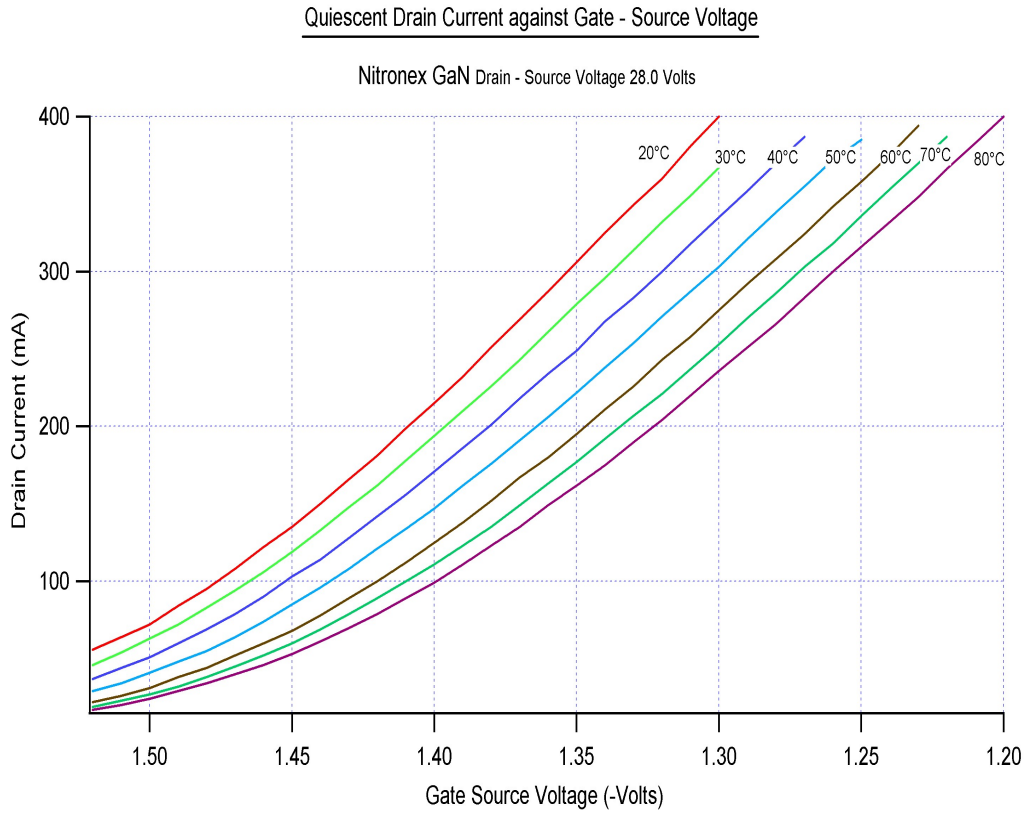

Fig A4.1.1 *Relationship of IV curves to temperature.*

The information shown here would be of great help when designing practical amplifiers, the variation in Ids resulting from a simple fixed voltage bias circuit can easily be seen, equally the swing in Vgs needed to keep Idq constant with temperature can be found. It should be noted that the required swing changes with the target current.

A4.2 Swept Power Measurements.

A power amplifier was then added to the input side to permit large signal measurements. As well as the RF performance the cooling system performance was monitored, the results of which are shown in Section 3.4.

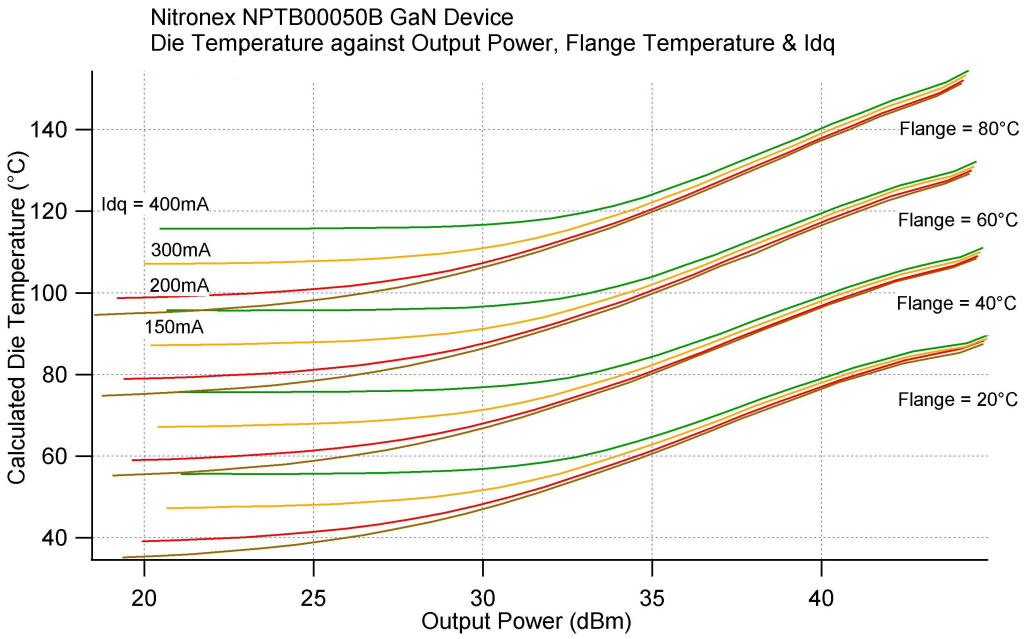

Fig A4.2.1 *The Calculated Die Temperature against Output Power and Flange temperature.*

A4.3 Active Harmonic Load Pull Measurements.

To demonstrate the system in its intended role, a Sumitomo EGNB045MK device was fitted and characterised. Figure 4.3.1 below shows the contours for output power and drain efficiency against load impedance. Clearly, by moving the system impedance out to 10 Ohms (Γ=0.66) the 5:1 transformers are well suited to this device.

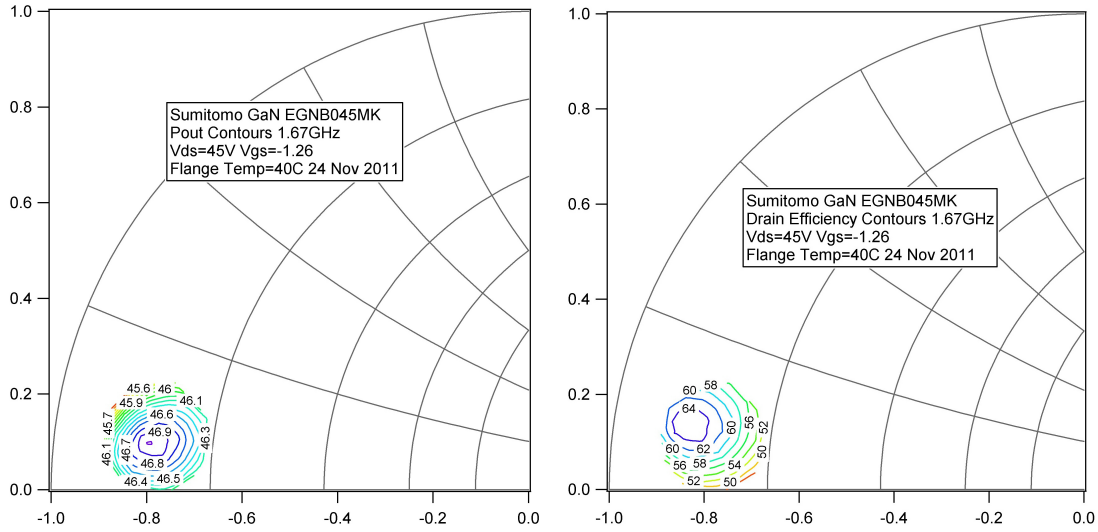

Figure A4.3.1 *Output power and drain efficiency contours for a Sumitomo GaN device.*

To illustrate how temperature will affect the device we can plot maximum available gain against output power across a range of quiescent currents and temperatures, fig. 4.3.2, and similarly, output power against input power, fig. 4.3.3. Considering these graphs will assist the system designer in finding the optimum quiescent point, determine what, if any, compensation is needed, and appreciate well before final testing how the system environmental requirements will impact the RF performance.

Even if we discount the ability to measure at different temperatures, this equipment brings a welcome degree of precision to this sort of measurement, the output power varying by a ratio of 200:1 would cause a passive heatsink to drift enough to distort the measurements.

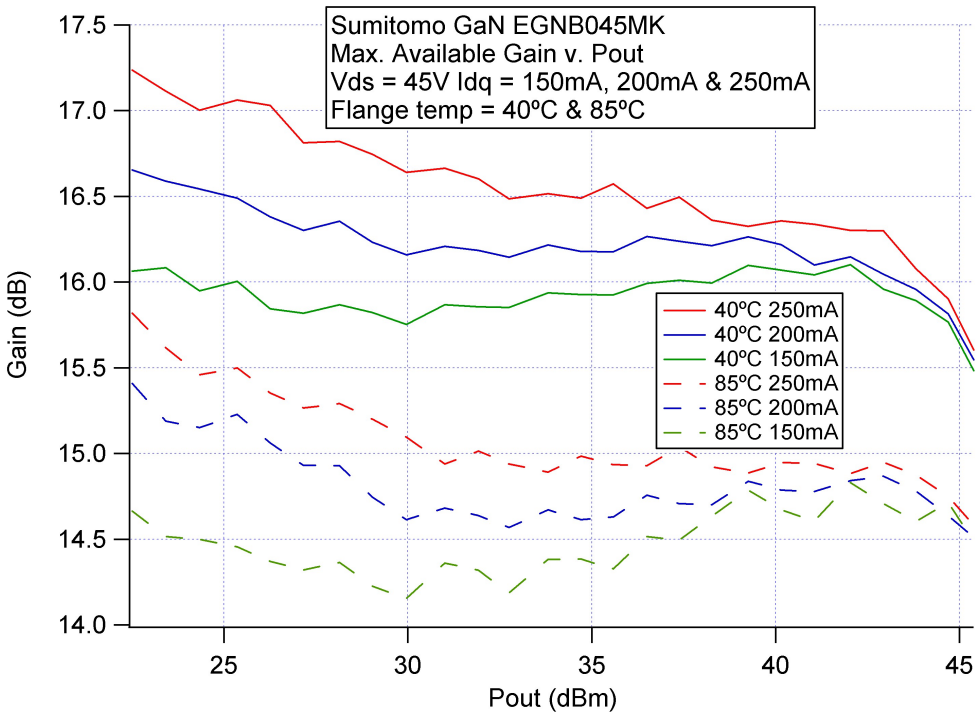

Figure A4.3.2 *Maximum available gain against output power for a range of temperatures and quiescent currents.*

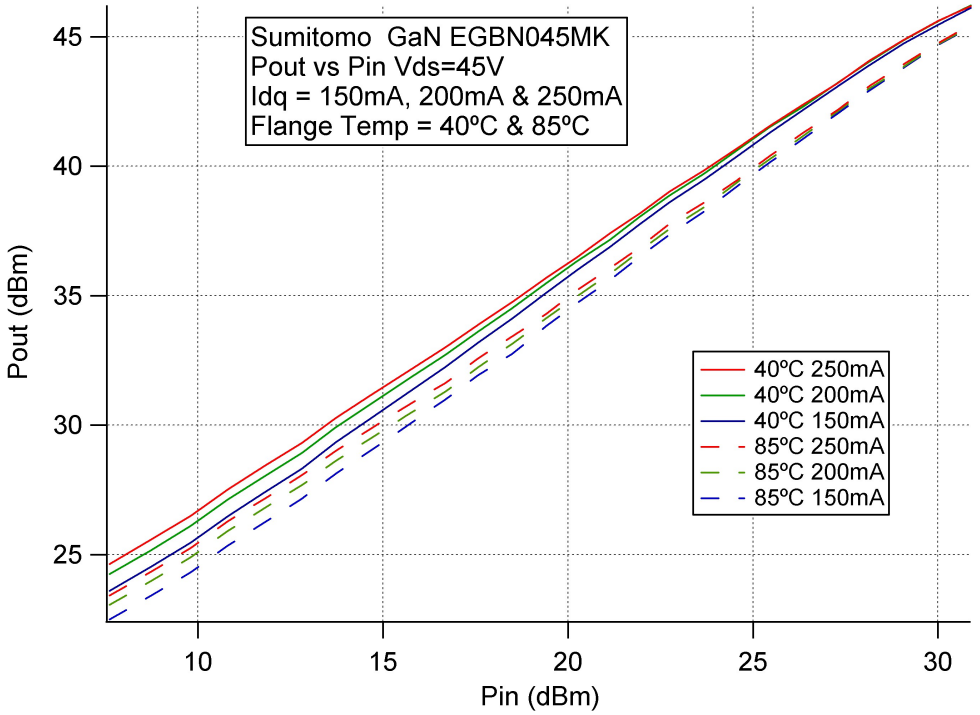

Figure A4.3.3 *Output power against input power for a range of temperatures and quiescent currents.*

A5: Conclusions and Future Direction

Work progressed well, the RF performance of the fixture agreed well with the modelled predictions, and it is well suited to its intended future role. The usefulness of a controlled measurement temperature has been clearly illustrated, and the repeatability proven.

A5.1 The RF Fixture and Components

These performed to expectations and handled large RF and DC powers well.

A5.2 The Cooling System

With a heat input of 186 Watts the cooled face temperature rose 21°C above ambient, which is a thermal resistance of 0.166°/Watt. The unit has now been used for RF device measurements, and has proved capable of handling powers past the design target.

A5.3 The Control Circuit

One of the main difficulties with the project proved to be the LTC1923 Peltier control chip. A more stable system could possibly be achieved using a microcontroller for the loop, this type of circuit has been successfully implemented in the past for amplifier AGC and ALC designs, and should adapt well to this application.
In closing, the project has met the objectives, and has delivered a practical tool for use in further research. The initial RF measurements show that with careful measurements considerable insight into temperature related device behaviour can be gained.

It also becomes clear that temperature control is vital for accurate characterisation work, the variation in device behaviour seen here would introduce considerable uncertainty if not managed.

Appendix B

Construction of the Pulsed Fully Active Harmonic Load Pull System.

Figure B.1 shows the first Pulsed Active Harmonic Load Pull system as used in "Waveform Engineering Beyond the Safe Operation Region" [5] and referred to in chapter 2. Adapting the technique to work with the Rohde & Schwarz ZVA 67 and the Agilent PNA-X vector network analysers is also discussed.

B.1 General Design

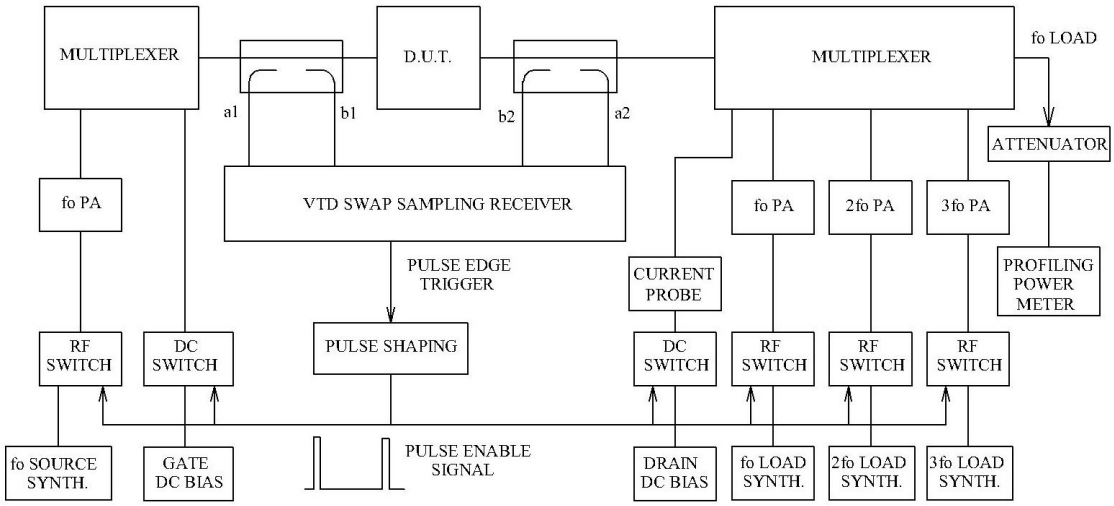

Figure B.1 Block schematic of the VTD based pulsed fully active harmonic loadpull system.

The system is based on the established fully active harmonic loadpull practice [1], but here is built around a VTD SWAP sampling receiver. In line with usual practice four samplers connected to directional couplers are used to measure the a_1, b_1, a_2 and b_2 waves. S-parameter and scaling factor corrections are applied to this data and the DC information added, allowing the real time voltages and currents at the device current generator plane to be calculated. The load impedance presented to each harmonic can be controlled separately by changing the phase and magnitude of a reverse wave fed into the output of the DUT via the multiplexer shown in fig B.1.

The SWAP lends itself to pulse work very well, its principle of operation permits very low duty cycles to be employed without the reduction in dynamic range which would be experienced by a VNA based system [6]. The width of the sampling window can be set

independently of the overall record size, samples are taken from multiple pulses and stitched together to create the complete record, so dynamic range is maintained at the expense of measurement speed [6].

B.2 Pulse Timing Control

The SWAP controls the system and sends out a falling edge trigger signal to synchronise the other components. Internal to the SWAP is the ability to control the sampling window width, repetition rate, overall record size, and the delay between the trigger signal and the start of the sampling window. The result is a very powerful and versatile system, which can have overall pulse lengths up to 256us, and move a sampling window as narrow as 1us anywhere along that pulse time. There is however no control over the actual RF pulse blanking, the pulse ON period and subsequent duty cycle must be controlled by external hardware. A simple analogue timing circuit was used, Fig B.2.

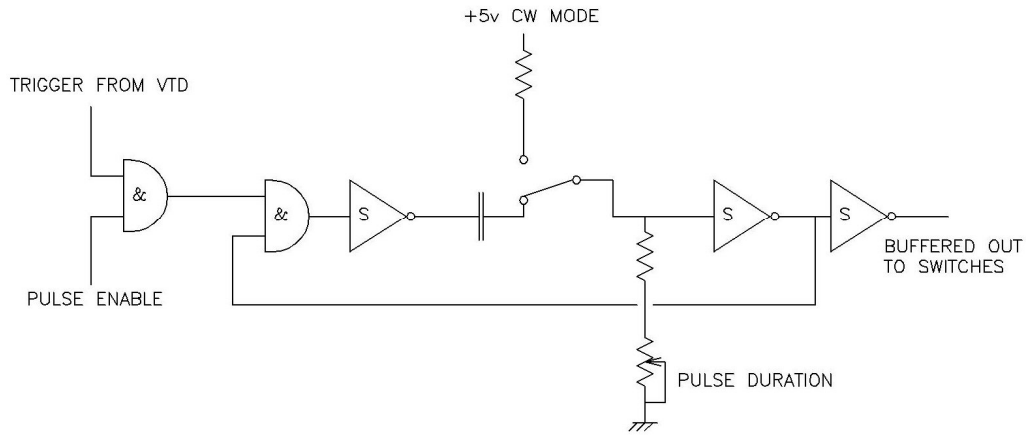

Figure B.2 Schematic of the pulse timing circuit.

The first AND gate permits an electronic enable signal to be applied from an external logic controller, such as a DAQ unit used for current measurement, and also provides a means of automatic shutdown in the event of an overload. The second AND gate prevents long pulses being terminated prematurely when the 50% duty cycle trigger line from the VTD goes back HIGH. Assuming the ENABLE line is HIGH then a negative edge from the VTD causes the output of the AND gates to go from HIGH to LOW, and consequently the output of the first Schmitt trigger inverter to go HIGH.

If the selector switch is set to PULSE then a current will flow through the timing capacitor and variable resistor combination, causing the input of the second Schmitt trigger to go above its ON threshold, taking its output LOW and switching on the RF signals. After a set time controlled by the position of the variable resistor, the capacitor charges and the current drops, whereupon the Schmitt trigger input falls back below its OFF threshold and the RF switches are turned off, ending the pulse.

It proved in practice to be a simple matter to set the time to the required value by means of a standard oscilloscope equipped with calibrated time cursors, the variable resistor chosen was a fifteen turn precision wirewound type which gave good sensitivity and resolution. By using low temperature coefficient parts for the timing components satisfactory stability was obtained.

The selector switch used is of the centre OFF type, so that PULSE, OFF and CW can simply be chosen, without altering any of the sampling parameters or other operational conditions. Being able to directly compare the pulse and CW behaviours is very useful, both for checking that the sampling synchronisation is correct and for assessing temperature dependant behaviour of devices. The ability to swiftly isolate all the RF drives and drain DC bias simultaneously proved invaluable on several occasions while developing the controlling software.

B.3 DC Bias Supply Measurement.

Clearly we must have accurate knowledge of the DC conditions as well as the RF signals if we are to make any useful deductions from our measurements, this is a simple enough task under CW operation, the remote controlled power supply units which are used incorporate precision measurement capabilities, and will pass the information over the controlling bus system. Once allowance is made for the voltage drop in the bias feed circuits, which is easily found by routine DC equipment, the data can be included with the RF data to produce the loadlines, waveforms and efficiency contours. If we move to a modulated carrier this is no longer the case, the power supplies will indicate the average DC current rather than the current flowing during the RF pulse.

A reasonable approximation of the pulse current, Ipulse, can be found by calculating back from the average value, Iav, allowing for the duty cycle and quiescent drain current, Idq;

Ipulse = (Iav - Idq) x 100/(duty cycle) + Idq

Several assumptions are made here however, notably that we are dealing with an essentially square waveform, and that the quiescent current is not affected by the RF operation. Since the average temperature of the device is likely to be altered, the second of these conditions cannot be relied upon, and the first certainly warrants careful case by case scrutiny. A further drawback is that changes along the length of the pulse cannot be measured, the ability to "profile" along a pulse is an important aid to understanding thermal time constants, and other memory effects. Far better then, to provide some real time measurement capability for the DC as well as the RF.

Measuring the DC on the output side presents some challenges, the drain bias voltage range for modern GaN devices frequently extends up to 50V, and higher values have been used, particularly in the pulse type applications we might well be evaluating devices for. Commercially available DAQ systems typically have a common mode voltage limit of 5 to 10V, so while these can be applied directly to a current shunt resistor on the gate side this method cannot be used on the drain. Using voltage dropper chains either side of the shunt resistor would reduce the measured voltage difference in the same ratio as the common mode reduction, so for a given sensitivity the series voltage drop would need to be proportionally higher. On the gate side it is normal to fit a relatively high value series resistor (typically 10 ohms) to help with low frequency stability, so it is natural to use this for current sensing as well. Fig. B3

The problem is not unique to our system, and high-side current monitor ics are commercially available. A typical example is the AD8210 by Analogue Circuits, this incorporates a precision fixed gain differential voltage amplifier having two current outputs, with a precision instrumentation amplifier which converts the first stage output current into a proportional ground referenced voltage ranging between 0 and +5V, it is then a simple matter to measure this voltage with an ADC.

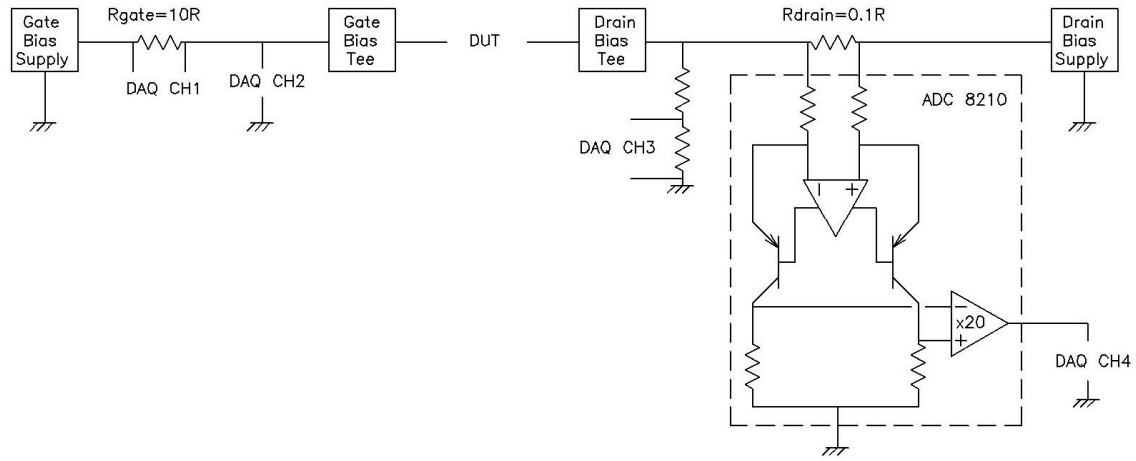

Figure B.3 DC Current sensing circuitry for pulsed operation.

The gate circuitry shown in fig B.3 will work with either enhancement mode or depletion mode devices, a differential bipolar ADC input is connected across the resistor to sense voltage drop and so allow the current to be calculated, while a second ADC measures the voltage allowing for the drop across the resistor. The latter feature is most important when measuring GaAs devices, when a DC current may flow in either direction and a higher value series resistor may be used for power limiting purposes, the changes illustrated in fig B.4, where R_{GS} = 400R, must be correctly accounted for to gain a valid assessment of the device's operation.

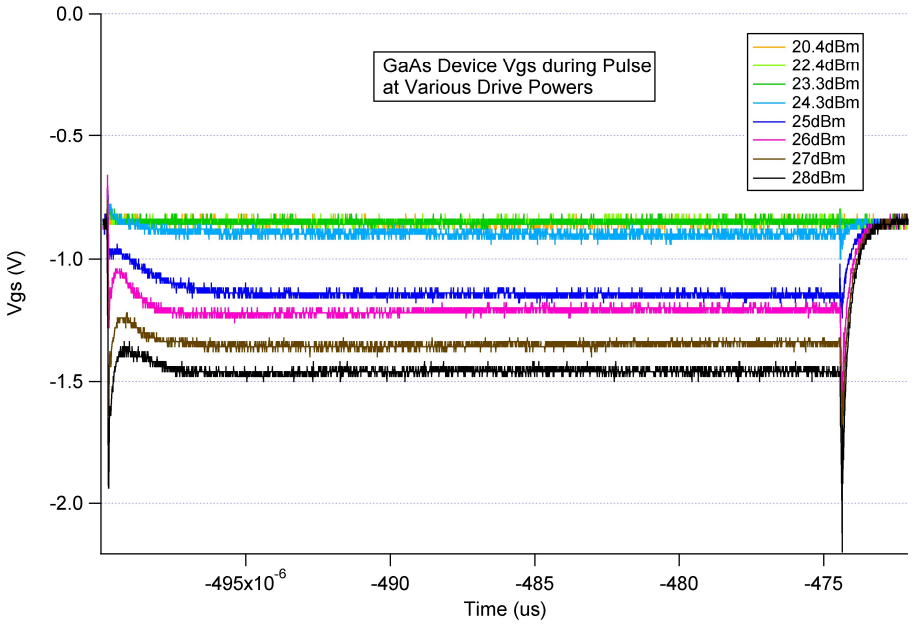

Figure B.4 Typical change in Vgs when a GaAs device is driven into compression.

It is obviously undesirable to have significant voltage drop in the drain feed, not only will this need to be correctly measured to give accurate results, but the change in device terminal voltage as the operational conditions are changed will distort the power output contours and gain compression curves, the 0.1R part shown in fig B.3 will cause a 250mV drop in the supply when 2.5A is passing, and give rise to the maximum 5V output from the ADC8210, which has a fixed voltage gain of 20.

The performance of the ADC used is key to the success of the system, it is highly desirable to measure the four DC parameters V1, I1, V2 and I2 simultaneously. The majority of commercial high speed multiple input data acquisition units (DAQs) sample their inputs sequentially, potentially measuring each parameter under different conditions, and the quoted maximum sampling rate is divided by the number of inputs in use, caveat emptor! The unit chosen for our system, the Agilent U2531A, has four balanced inputs which all sample at the same time point, and all four can be run at the quoted maximum sampling rate of 2M samples per second simultaneously. The basic sampling rate would allow us to profile a pulse at 0.5μs intervals, however, the clock of this DAQ runs at 48MHz, and sampling can be delayed from the trigger signal by any number of clock ticks, if we take a sample, increase the delay count by one and sample again 23 times we can build up a picture of the current at 48MHz resolution (20.8ns).

Calibration is performed by attaching resistive loads in place of the DUT, and comparing the reading of the DAQ to the reading given by the DC supply metering circuits, a scaling factor is then calculated which can be applied to subsequent measurements. Performing a second measurement with the DUT terminals open circuit allows any zero offset to be found, and also the voltage sensor to be calibrated.

During measurements it was found to be helpful to have a high speed oscilloscope connected to the output of the current sensor, this provides real time monitoring throughout the pulse and helps to ensure that a stable and accurate reading is being obtained from the ADC. The purple trace in figure B.5 shows the relatively slow response time of the ADC8210 compared to the green trace, which shows the switch pulse signal, this means no measurements can be taken for 2us after the start of the pulse.

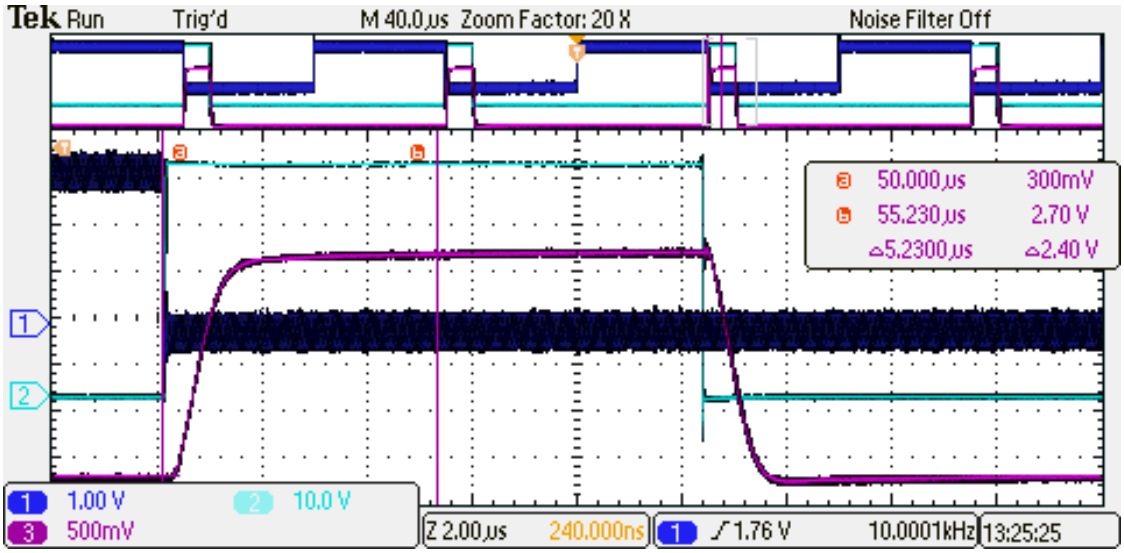

Figure B.5 Typical timing and DC current monitor waveforms.

The relatively slow response of the 8210 was acceptable for the original work planned for the system, however it became apparent that some of the thermal and trapping effects under investigation included responses within the first period of the pulse, and so in due course a faster version was designed, this is described in Appendix C.

B.4 Adaption to R&S ZVA67 system

The Rohde and Schwarz ZVA67 VNA contains all the components needed for a low power active harmonic load-pull system, eight high dynamic range receivers and four synthesisers driven from a single reference giving excellent phase stability, Mesuro Ltd have proved that by controlling the unit with appropriate software the result is an outstanding FAHLP system. Since removable front panel links are used to connect to the internal directional couplers it is a straightforward matter to use remote couplers and amplifiers, resulting in a highly versatile system for high power and on wafer work.

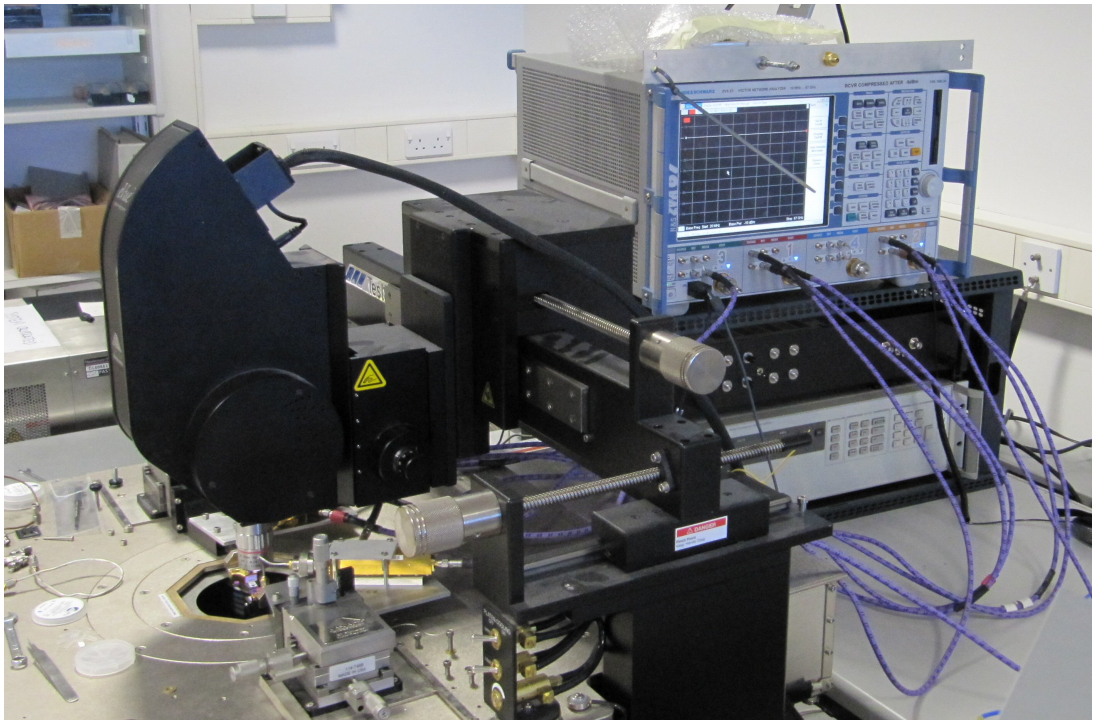

Figure B.6 The R&S ZVA67 based system.

Fig. B.6 above shows the ZVA together with the cascade probe station used for high frequency on wafer measurements, the black panelled unit in the rack underneath the ZVA is the university designed modulator described below. High stability cables connect the ZVA's receivers to directional couplers mounted on the RF probe positioners, improving discrimination between high reflect cal standards and terminations which results in more accurate calibrations. Insertion loss from the load pull amplifiers to the DUT can also be reduced by this method, which is most important as frequencies increase [17].

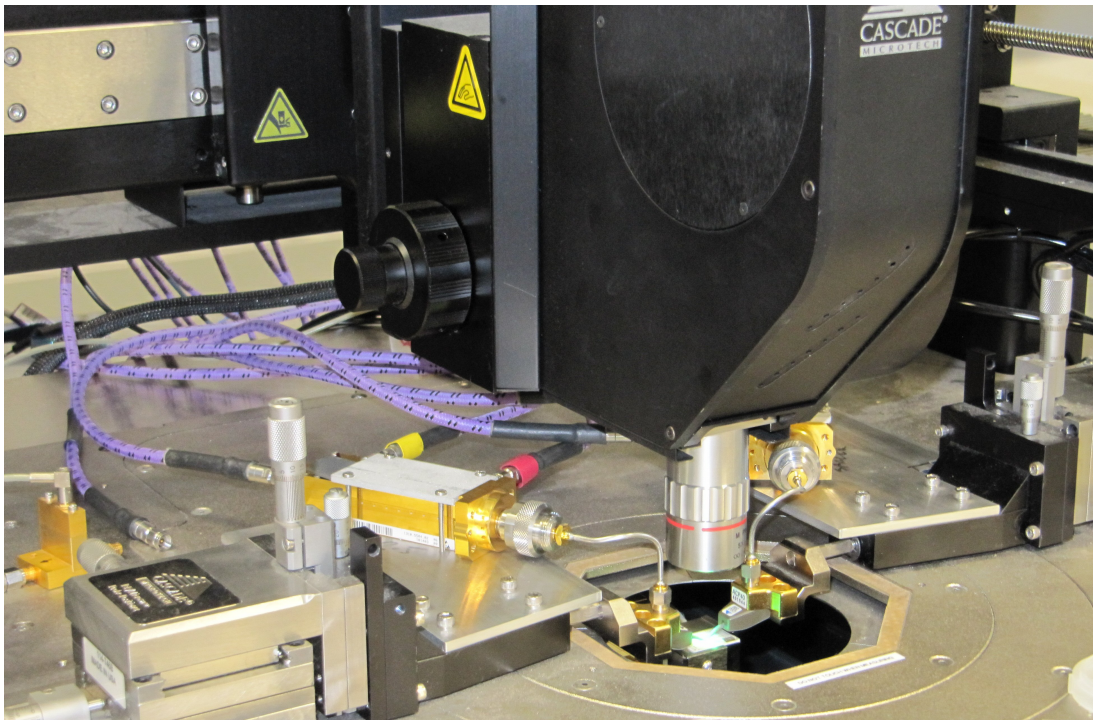

Figure B.7 Remote couplers are used to improve accuracy.

The ZVA also includes the ability to control the timing and width of the measurement windows, but cannot perform the synchronised switching of the internal sources required for a pulsed measurement system. A timing signal is available from a back panel connector however, and it is a relatively straightforward task to process this and link it to a version of the VTD based modulation system described above.

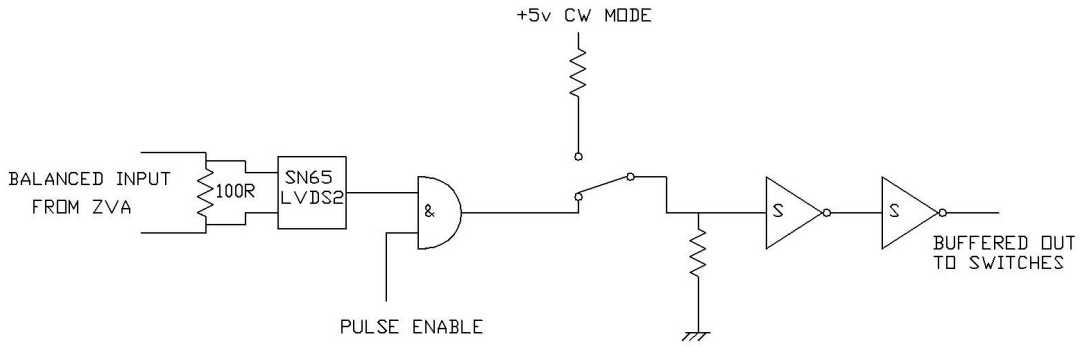

Figure B.6 The ZVA external pulse modulator schematic.

The timing output from the ZVA is a balanced signal in the LVDS format, and as such must be converted to an unbalanced 5V TTL signal to drive the RF switches. A specialised converter IC, the SN65LVDS2 is an ideal way of doing this, the output from

this is then AND combined with an enable signal from the controlling computer via the Agilent U2531A DAQ before passing through the manual control switch to the RF and DC switch buffers. As with the VTD system this permits direct comparison between Pulse and CW measurements, and gives a useful way of simultaneously switching off the RF forward drive and load-pull signals.

The modulation circuitry was assembled into a 2U 19" rack case, together with DC current and voltage sensing units for the gate and drain bias supplies and an Agilent U2531A DAQ as used for the VTD system to give a compact self-contained unit.

B.5 Adaption to the Agilent PNA-X VNA

The Agilent PNA-X VNA is similar in many ways to the ZVA, however while it has four measurement ports it does not contain four sources so for active harmonic load-pull additional external sources must be used. It does not include the pulse operation features of the ZVA, however there is a measurement trigger input, so in contrast to the ZVA which controls the system it can be used with an external pulse timing circuit. The concept was proven by Dr T. Williams of Mesuro ltd with the assistance of the author in adapting the external hardware.

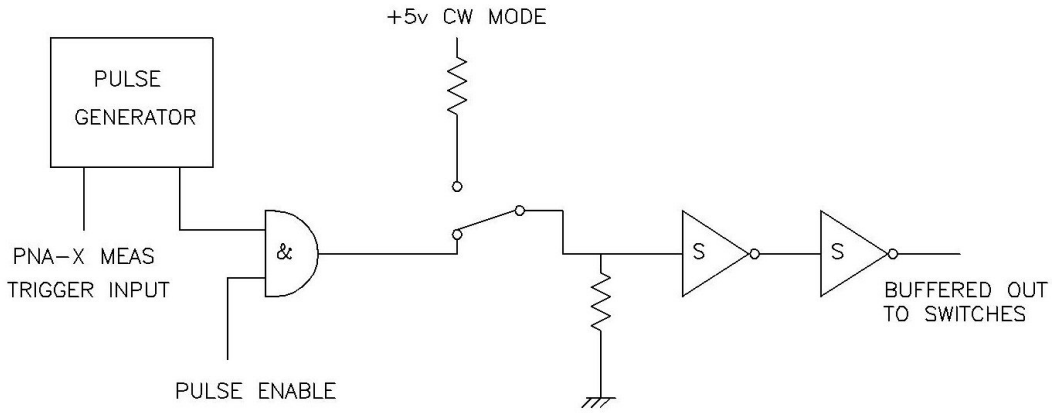

Figure B.7 The PNA-X RF modulator and measurement trigger circuit.

An Agilent 81150A Pulse Function Arbitrary Generator was used to drive the circuit shown in fig. B.7, this has two independently variable synchronous outputs which can be used to ensure the RF and DC are stable before the measurement commences and also permits a limited degree of profiling to be carried out. The enable line is retained as before, to give software control of the RF, and to provide an overload shutdown facility.

Appendix C

D.C. Switching and Measurement during Pulsed Operation.

The ability to switch the DC bias in time with the RF pulses allows different thermal transient scenarios to be examined, and is particularly useful for Class A bias conditions, where the device might be excessively heated while running without RF. Either the drain bias can be switched on and off, or the gate bias can be switched between pinched off and the required quiescent setting.

While simple in principle, achieving a rapid clean change of state requires close attention to the supply memory considerations discussed in chapter 4, "DC supply memory, Bias Tees, Diplexers and Multiplexers", and to the circuit design.

Clearly it is vital to obtain accurate measurements of the DC parameters if the device performance is to be appraised in a meaningful way, this poses a significant challenge, some solutions to which are presented here.

C.1 Drain bias switching.

Switching the low voltages used for GaAs is relatively straightforward, several manufacturers produce high speed FET driver ICs which work up to 15V rails, and power FETs are available which can withstand such a rail voltage across the gate-source junction. In its simplest form such a switch could be realised by inserting a P-channel power FET in the high-side of the supply and driving its gate with a driver such as the Microchip TC4427 (fig C.1). Note that in this common Source mode the switching function is inverted, so this must be accounted for in the driving circuit.

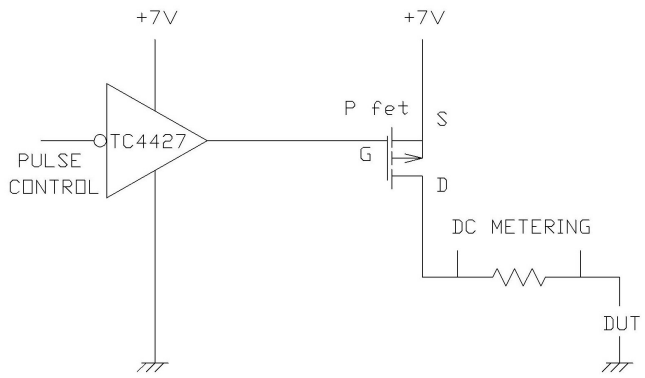

Figure C.1 A basic switching system suitable for low voltage GaAs devices.

P-channel FETS do not give the same combination of Rds_{on}, Ids_{max}, and switching speed which can be obtained from N-channel parts, so it would be beneficial to use the latter, however since the switch must be in the high-side then an N-channel part must operate in Source follower mode, so the gate must be taken above the RF drain supply by a good margin, at least 4V, to switch ON, and pulled down close to 0V to cause full switch OFF, ideally within a few nanoseconds. When working with GaAs this does not cause a problem as the driver ic can be operated from a suitably higher supply rail, as in fig. C.2. Note that this circuit does not invert the drive signal.

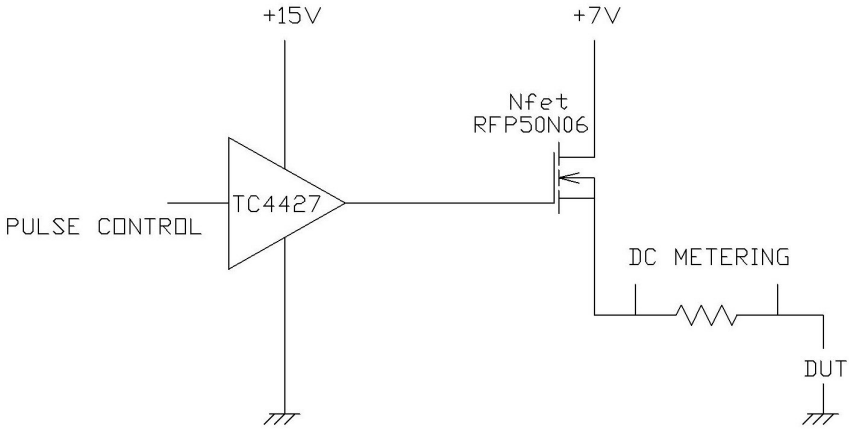

Figure C.2 A switching system suitable for low voltage GaAs devices using an N channel FET.

If a supply rail higher than approximately 10V is required then this circuit cannot be used, due to the limitations of the driver ic and, since it is good practice to slowly ramp up V_{ds} when starting to measure a new device, the V_{gs} limit of the FET switch element. The issue is exacerbated by the requirement to measure a single device at multiple drain bias voltages, which means that somehow the gate drive levels should automatically track the drain bias. Fortunately this by no means simple feat has been neatly encapsulated by Linear Technology in their LTC4440-5, this device can work with drain supplies up to 60V, and has an integral voltage booster which tracks the source voltage.

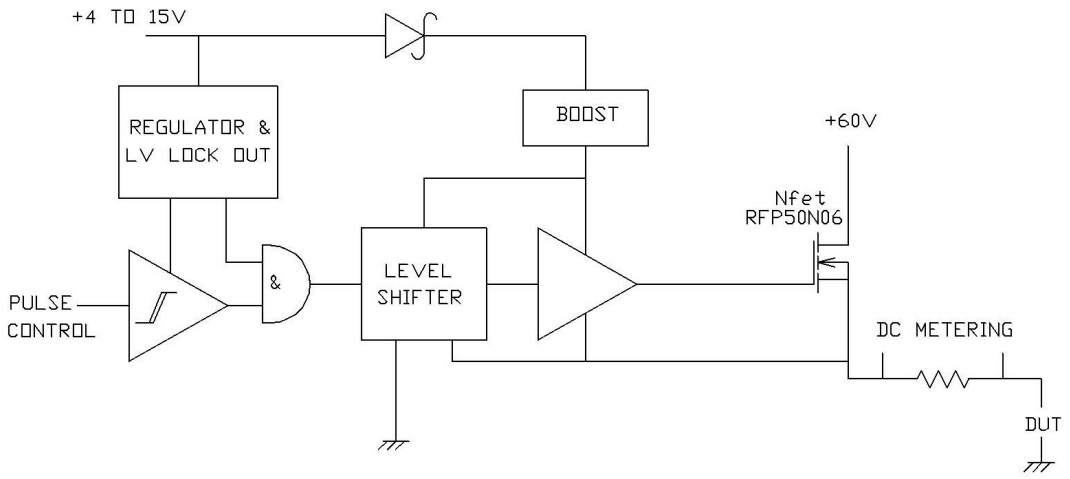

Figure C.3 A switching system suitable for devices with drain bias up to 60V.

The circuit shown in fig. C.3 illustrates how the complex function of the LTC4440-5 simplifies the task of driving the high-side N-channel FET, apart from the addition of the bootstrap diode the circuit is no more complex than the standard driver. Very particular attention must be paid however to minimising the inductance in the gate drive path, also to grounding and the decoupling of supplies.

C.2 Very High Voltage Switching.

The rapidly evolving GaN device market meant that the 60V limit of the LTC4440-5 circuit became inadequate, and so a discrete version had to be devised (fig C.4). The LTC4440-5 also suffered from the shortcoming that the internal boost pump used to generate the switch FET gate voltage only functions if a rapid pulse is being processed, it cannot function correctly for DC or very slow pulses, a problem that was also addressed by the circuit in fig. C.4.

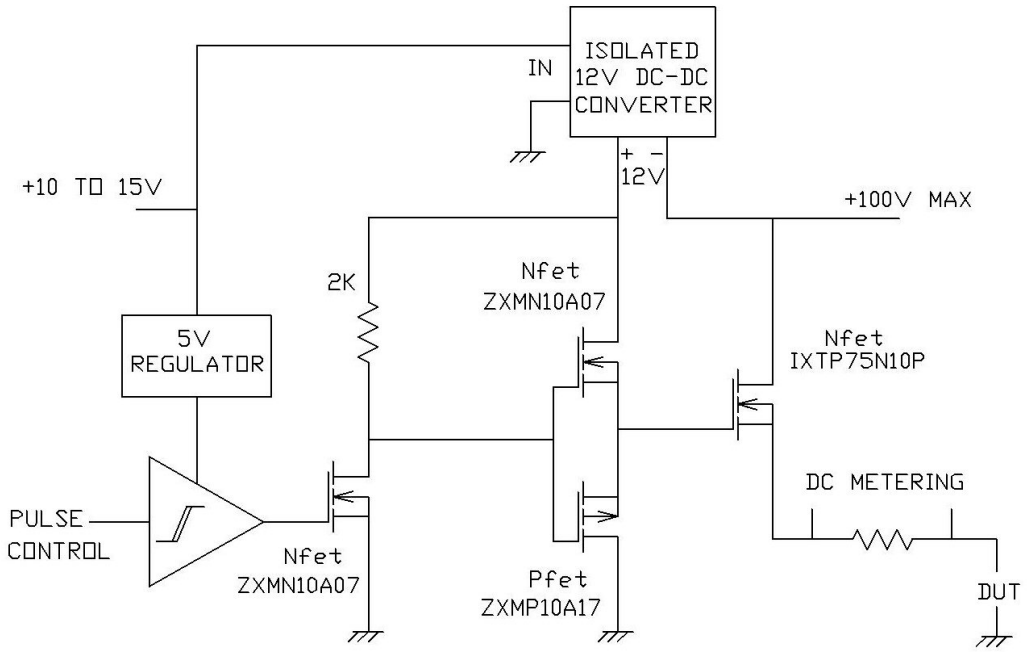

Figure C.4 A 100V capable fast rise time Drain Bias Pulser.

The above circuit uses a commercially available miniature DC-DC converter module to generate a gate voltage sufficiently in excess of V_{dd} to ensure full turn on of the output FET. The first ZXMN10A07 provides the voltage gain from the TTL logic level input, the following complimentary pair of devices provide the current gain to rapidly switch the output FET, which according to the manufactures datasheet has a typical input capacitance of 2250pF. The internal capacitance to the input side of the DC-DC converter must also be charged and discharged for each cycle, so a low impedance drive capability is required. A point to note is that the chosen output device has a current rating of 75A continuous, and 200A pulse, which is excessive for the application in hand, however the factor governing the choice is the low $R_{DS(on)}$ of 21mΩ, this keeps the voltage drop to the DUT to a minimum.

The achieved propagation delay, rise and fall times shown in figures C.5 and C.6 are satisfactory for the application, being around 200ns, 500ns and 100ns respectively, clearly the fall time benefits from relying on an active element in the first stage, whereas the rise time is set by the 2K pull up resistor.

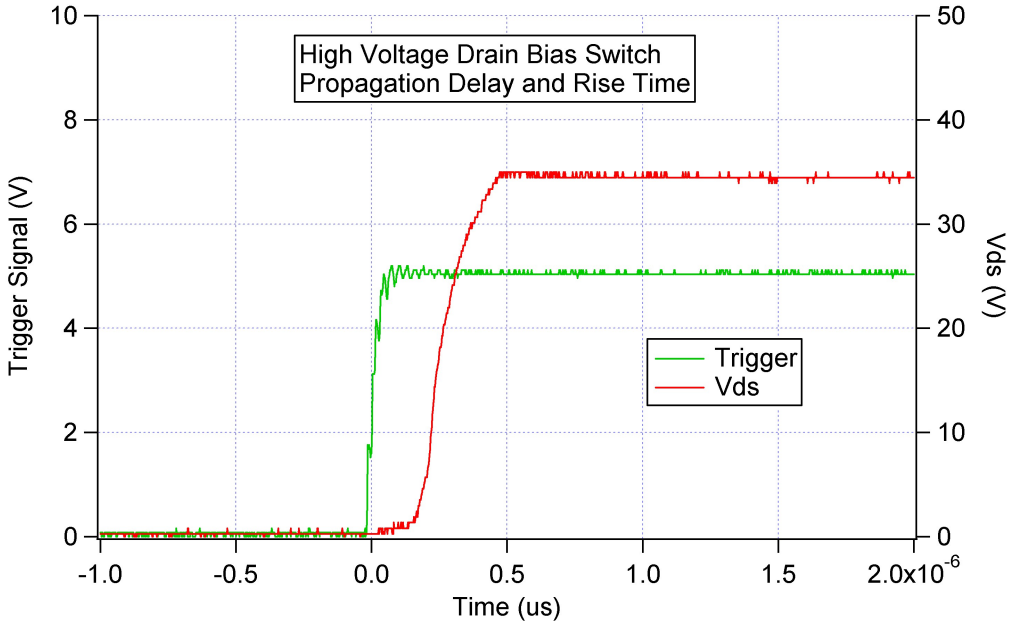

Figure C.5 High Voltage Drain Bias Switch Delay and Rise Time.

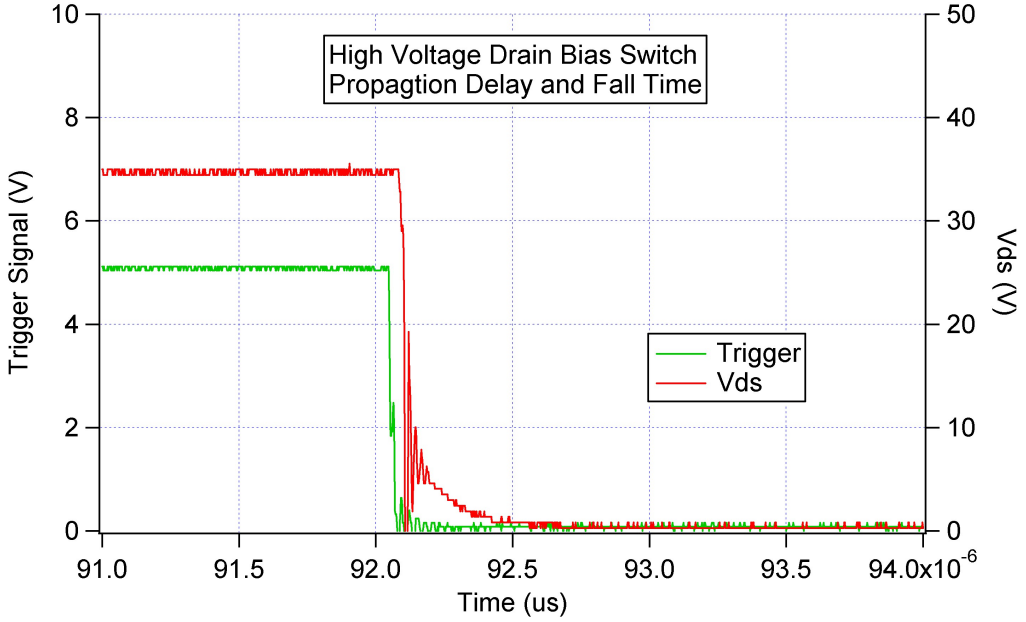

Figure C.6 High voltage drain bias switch delay and fall time.

The circuit does not have an inherent voltage limit other than the insulation breakdown voltage of the chosen DC-DC converter, which for the Recom inc. RI-1212S used here is stated as 1000V, it is simply a matter of using higher voltage transistors to increase the limit should that be required - note that this will inevitably lead to an increase in $R_{DS(on)}$ so it should not be done without good cause.

C.3 Over Current Protection.

The high cost and fragility of wafer probes is well known and, as is discussed in chapter 6, part of the motivation for implementing a pulsed measurement system may well be to reduce the average power dissipated in the probes, and so extend the practical measurement envelope. However should the worst happen a failing device will almost certainly present a short circuit across the drain probe, which will then be damaged beyond repair by the resulting DC current flow. While bench power supplies have a current limit circuit which can be set just above the expected normal current, in practice there is enough energy stored in the decoupling capacitors to destroy the probe even if the limiting circuit can respond quickly enough. As fig C.7 below shows the result can damage not only the DUT and the probe, but also spread contamination across the wafer, clearly some means of effectively limiting the current would be highly desirable, and since we now have a high speed switch in our circuit it is an obvious step to use this to disconnect the supply.

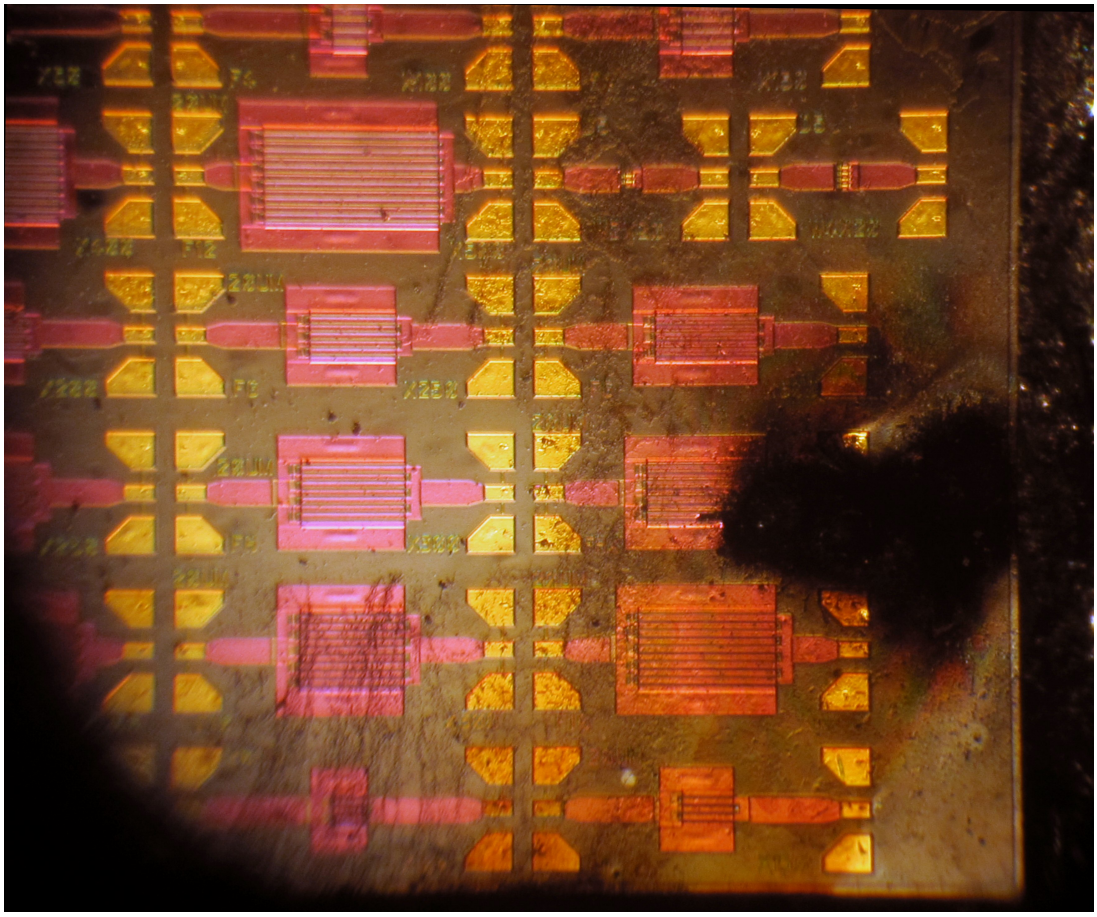

Figure C.7 A GaAs die following a failure under power.

“Electronic Fuses” are available commercially, however these will not switch off the RF power, which may well be high enough to sustain an arc long enough to damage the wafer probe. In order to achieve the fastest response time a number of sensing methods were considered, the most obvious being to link to the output from the current measurement circuit, but this has the drawback of requiring a voltage drop across a series resistor to function, and since the circuit might be used on a CW only system this would be unwelcome. Current sensing using Hall effect sensors is widely established, and these do not necessitate a series resistance, the current carrying conductor is simply placed adjacent to the sensor allowing the magnetic field to influence it. Aside from the lack of voltage drop this method has the advantage of good electrical isolation, ideal not only for high DC levels but also providing excellent common mode immunity for pulsed bias signals.

A number of parts are available commercially, though it quickly became apparent that most were far too slow, with response times measured in milliseconds rather than microseconds. One part stood out, the ACS712 from Allegro Microsystems inc., this device encapsulates the sensor, the coupled conductor and the linearising buffer circuitry to produce the output signal, greatly facilitating construction of a consistent, stable and sensitive system. The specified response time is 5us [manufacturer’s data], which is faster than the ADC8210 resistor based device can respond when working with pulsed supplies.

Three different current range parts are available, 5A, 20A and 30A, these current ratings indicate when the output signal will compress, the damage threshold is 60A for all the parts so there is no risk of damage during an overload event. A 5A part giving an output sensitivity of 185mV/A was used for the following tests.

In order to generate a trip signal at an adjustable threshold the output from the ACS712-05 was passed to an LT1719 high speed comparator and a pair of dual input AND gates, the first of which acts as a latch, the second than gates the control signal passing to the bias and RF switches (fig C.8). A push-button switch is used to reset the latch, and an LED indicates when the system is active.

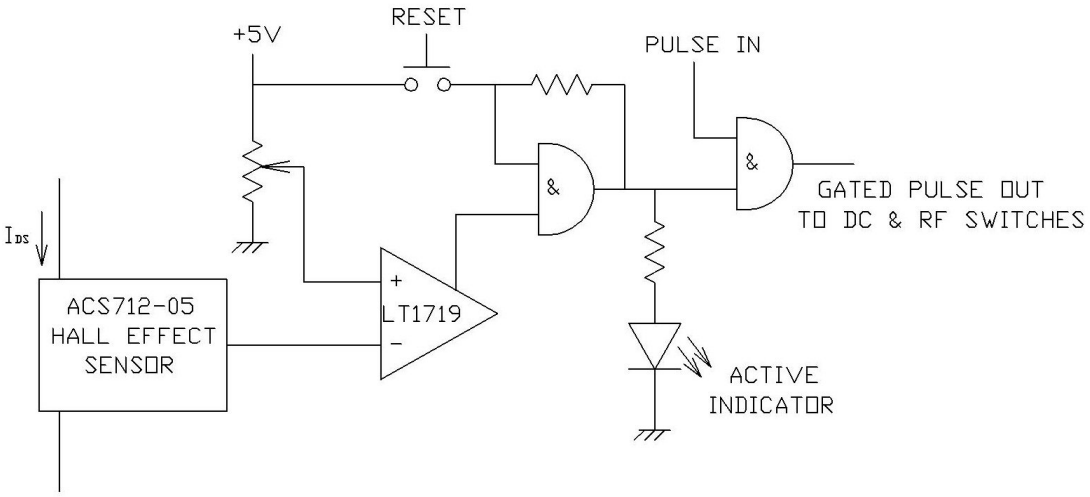

Figure C.8 The Hall Effect based current trip circuit.

Once assembled the response time was measured by connecting a 50 ohm resistive load via the high voltage switch described above, and measuring the voltage across the load as a single pulse was applied. The degree of overload was varied by changing the applied voltage. The response time was found to depend to great degree upon the overload factor, ranging from a few microseconds to several hundred microseconds, see fig C.9.

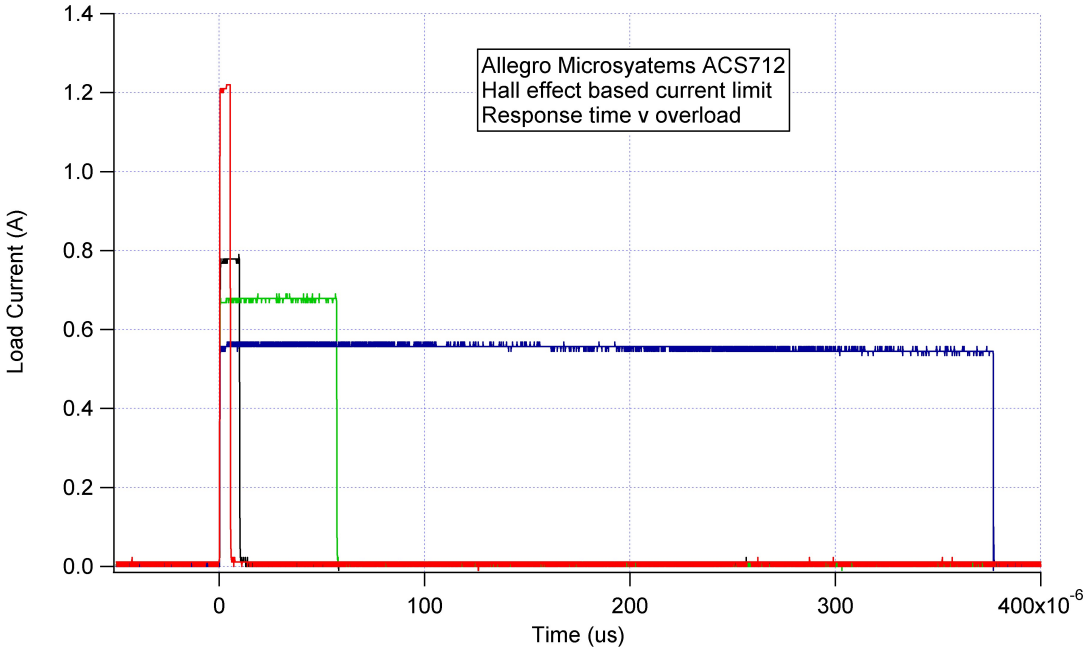

Figure C.9 Response time v. overload of a Hall effect current trip circuit.

Clearly the above response is not ideal, however the circuit was used to test several die with drain biases up to 58V, none of these die failed, however a control software crash occurred which caused a trip of the current limiter for no obvious reason. It is quite likely that the circuit saved the die and wafer probe from damage due to loss of control of the signal generators or bias supplies.

C.4 DC measurement during pulsed bias operation.

In Appendix B the problem of measuring the DC parameters during pulsed RF operation is discussed, if the drain bias is pulsed as well then the situation worsens as the common mode rejection response of the monitoring circuit becomes critical. The ADC8210 chip used in the early stages proved to be rather inadequate, the sudden large drain voltage change caused a large spike in the output voltage, which took around 8usec to settle, precluding measurements with pulses shorter than 10µs. A different chip is available, the Linear Technology LT2940, fig c.10, which offers faster measurements, better CMR performance, a lower forward voltage drop and also a higher maximum operating voltage of 100V. It does not however provide a voltage output suitable for direct sampling, the output is in the form of a +/- 200µA proportional current which must be converted and buffered before being fed to the ADC. From the manufacturer's datasheet the frequency response is highest into a 1K ohm load, which will result in a voltage of +/-200mV. For this application bipolar capability is not needed, so this resistor can simply be connected between the I_{MON} pin and ground, with no positive offset. Similarly a single rail op-amp buffer can be used provided it is of the rail-to-rail type to avoid distortion at very low currents, the high speed Analog Devices ADA4500 was selected. With a bandwidth of 10MHz, a maximum input bias current of 2pA and excellent noise performance the ADA4500 also uses a "novel zero-crossover distortion circuitry" which maintains linearity over the full rail-to-rail input range and is "excellent for driving ADCs" to quote the manufacturer.

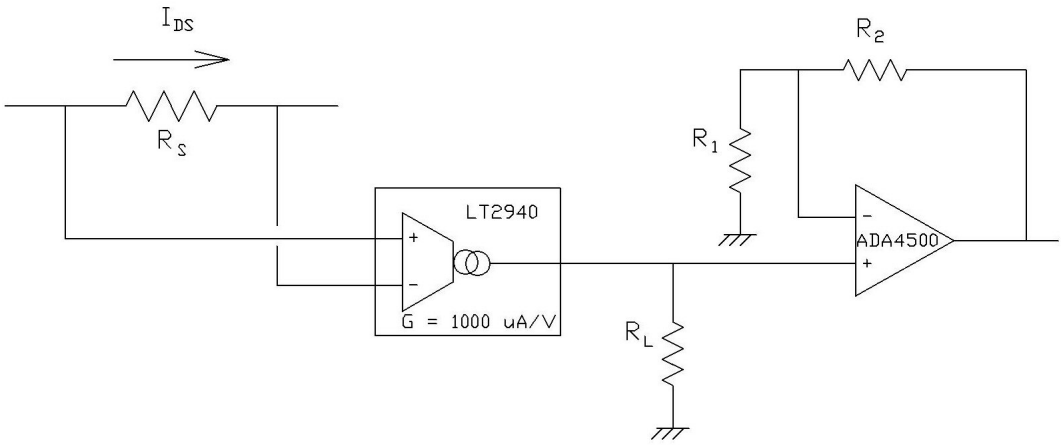

Figure C.10 high speed, high side LT2940 based current probe.

Using a single rail supply does mean that a non-inverting amplifier topology must be used, rather than the generally preferred inverting/virtual earth style, the performance of the ADA4500 is such that this does not appear to have caused a problem in practice.

As mentioned earlier the maximum measurable voltage, E_{max}, across the sensing element, R_s, is +/- 200mV, so the value of R_s for a given maximum design current can simply be found from Ohm's law, in this case I_{max} is required to be 2A, therefore:

$R_s = E_{max}/I_{max} = 0.2/2 = 0.1R$

The optimum value of R_L is taken from the LT2940 manufacture's datasheet as 1K, which will result in an input voltage range to the ADA4500 of 0 to 200mV from the output current of the LT2940, this then needs to be amplified to a suitable level for sensing by an ADC, in this case the maximum output of the ADA4500, +5V.

Evidently then the required voltage gain, A_V, is given by;

$A_V = V_{OUTmax}/V_{INmax} = 5/0.2 = 25$

And from established operational amplifier theory,

$A_V = R_2/R_1 + 1$

So

$R_2/R_1 = A_V - 1 = 25 - 1 = 24$

Values of 47.5K and 2K were used for R_2 and R_1 respectively, final calibration can be performed at the software stage. For the prototype component tolerances accumulated such that the overall ratio came out at 2.507V/A, very close to the ideal 2.5V/A, see fig. C.11.

The departure from the linear seen at the low end of the various lines (fig C.12) is due to the low voltage present on the sensed line, the manufacturer's datasheet stipulates that this must be above 4V, and the observed non-linearity is in that region, in practice this is unlikely to be a problem.

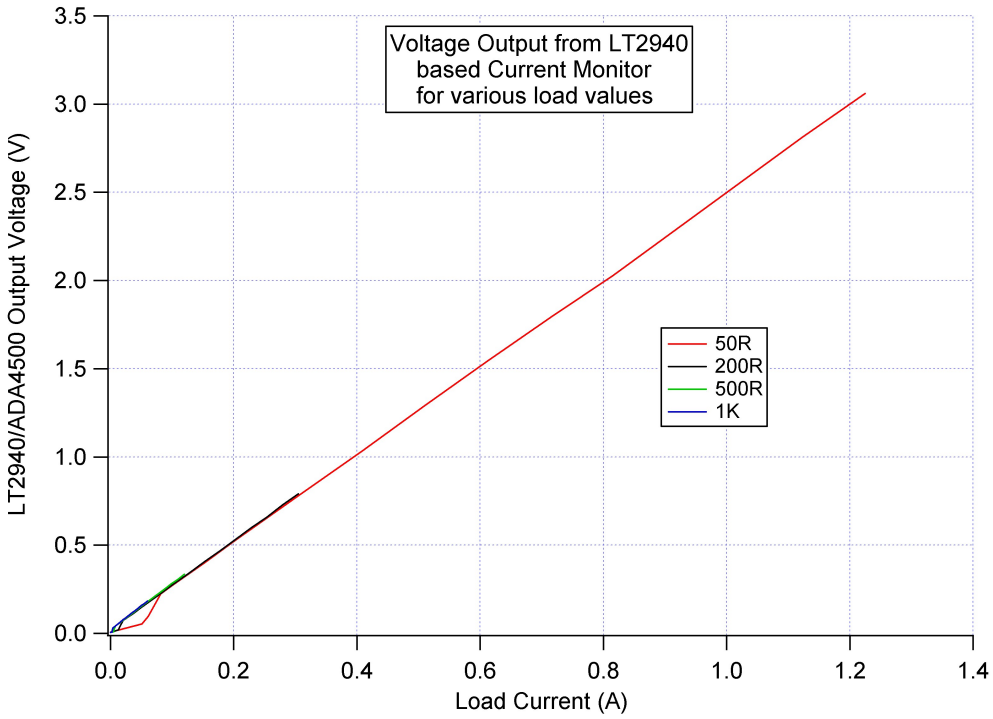

Figure C.11 Output voltage to the ADC against line current.

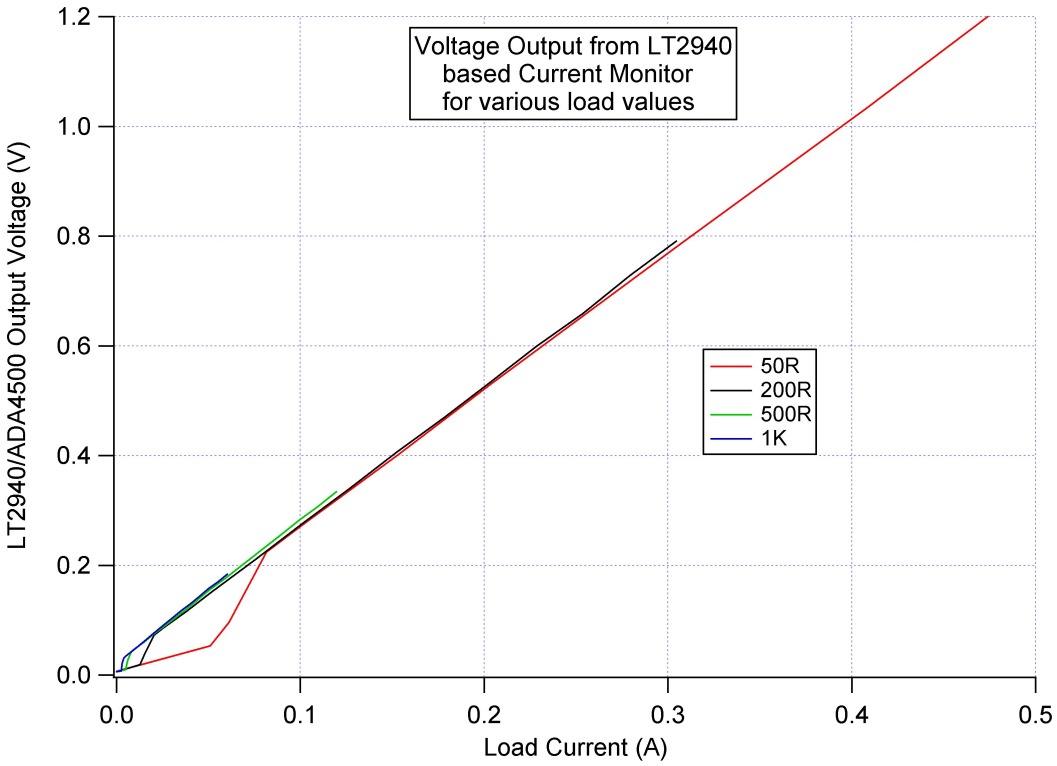

Figure C.12 Output voltage to the ADC against line current, zoomed in.

The response time was measured by applying a resistive load and comparing the monitor circuit output directly to the load voltage, it can be seen from fig C.13 below that at high currents the new circuit comfortably outperforms the ADC8210 version, particularly when the drain bias is pulsed, measurements can be taken with confidence between 2µs and 5µs, whereas the ADC8210 circuit can only be read after 5µs (the LT2940 measurement was taken with a 10µs V_{DD} pulse). However at low currents it was found that the situation was reversed, the performance of the LT2940 degraded rapidly (fig C.14).

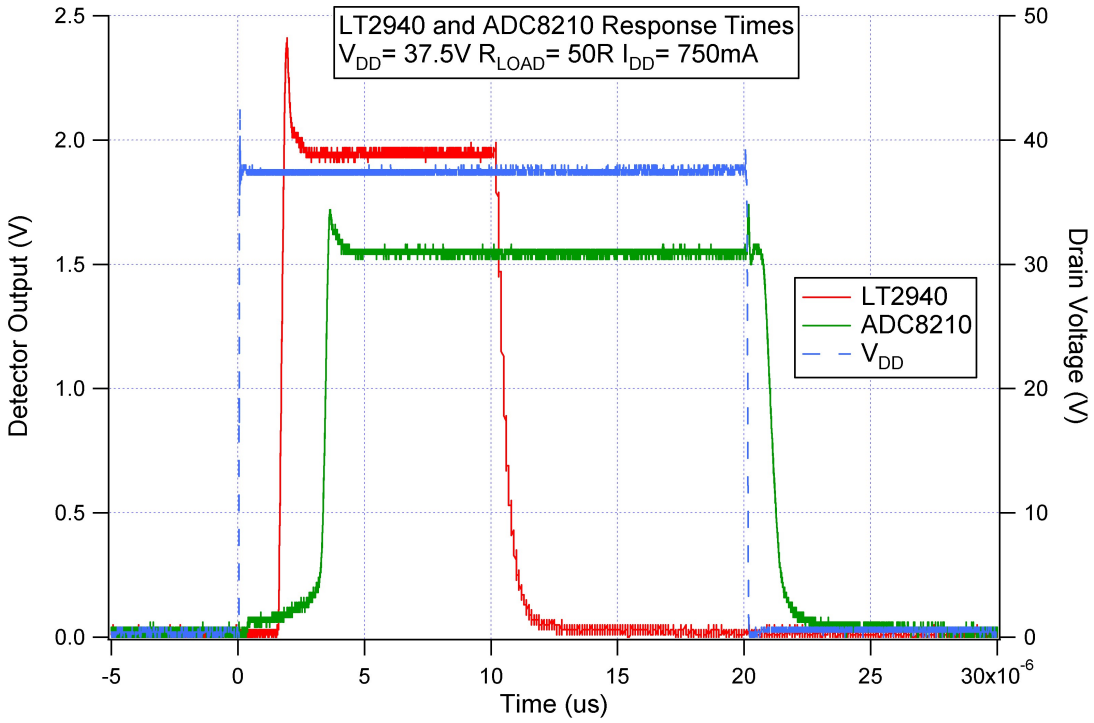

Figure C.13 The response times of the LT2940 and ADC8210 circuits.

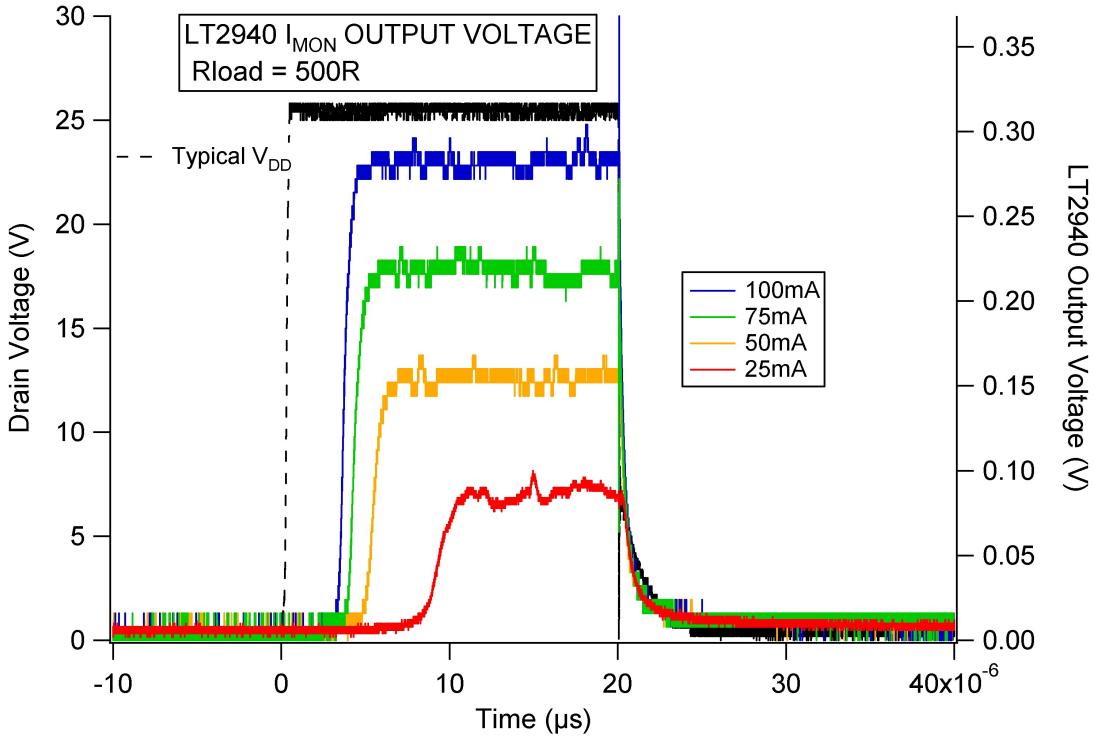

Figure C.14 Response times of the LT2940 at low currents, sensor after the DC bias switch.

In view of this the sense resistor was moved to the supply side of the switch, so that it was no longer subjected to the high change in common mode voltage. Concern that the relatively high capacitance of the switching FET might distort the readings proved groundless, and the result was a greatly improved response at all loads. At low currents the rise time delay is greatly reduced, fig. C.15, a reliable sample could be taken at 5µs even at 25mA.

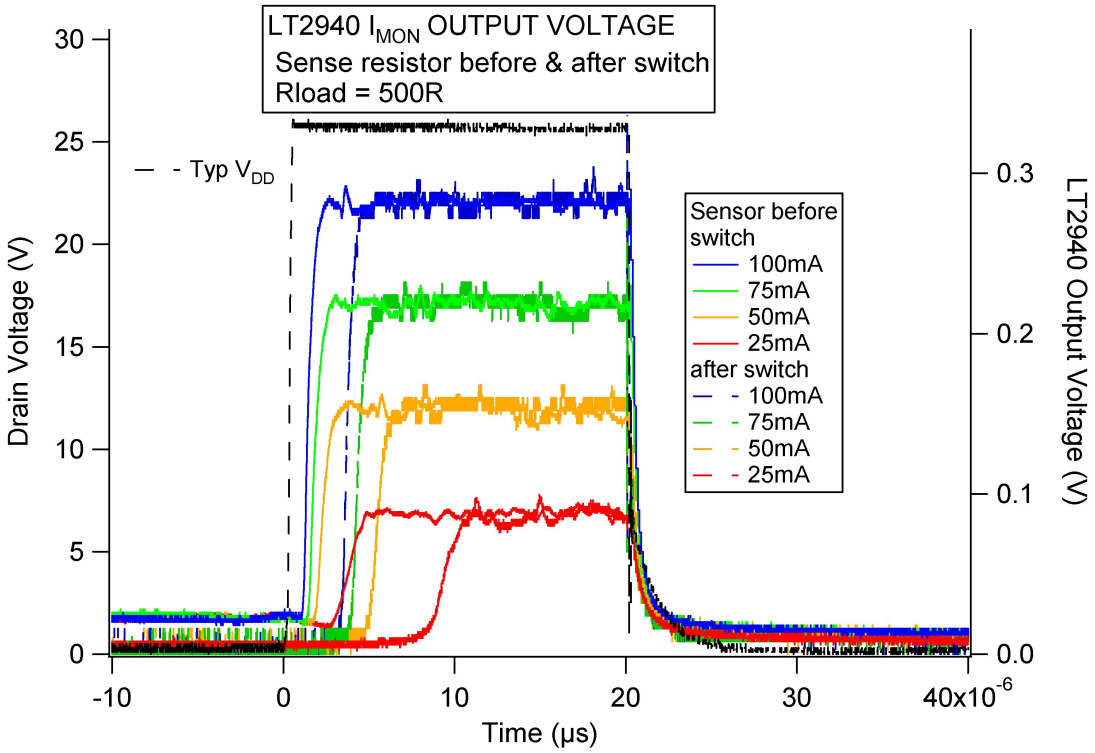

Figure C.15 Response times of the LT2940 at low currents, sensor before and after the DC bias switch.

At currents above an amp the overshoot is eliminated, again allowing sampling much earlier in the pulse, generally after only 2.5µs, fig. C.16.

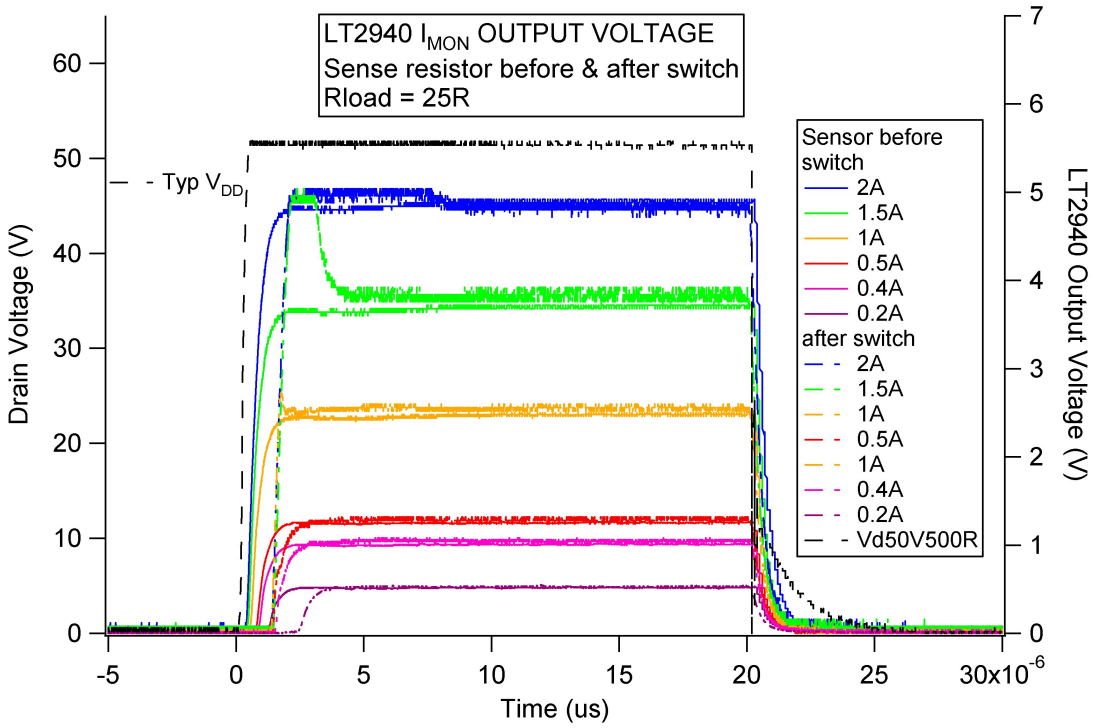

Figure C.16 Response times of the LT2940 at high currents, sensor before and after the DC bias switch.

C.5 An integrated Switching, Measuring and Limiting solution.

With acceptable solutions to the three required functions it is a logical step to integrate them into a single unit, this not only simplifies setting up the equipment but it also allows the performance to be optimised. With timings moving into the nanosecond region interconnecting cables can slow response times and lead to “ringing” after step changes so they should be eliminated where possible.

In the circuit above we have only used a small part of the LT2940’s capabilities, it also has a voltage monitor input used to produce an instantaneous power signal similar to the current signal, and a comparator intended to provide an alarm indicator when the measured power level exceeds an adjustable threshold. Unfortunately the comparator is not particularly fast, and when trying to prevent the kind of damage seen in fig C.7 time is most definitely of the essence. With this in mind the integrated version used the LT1719 comparator from the Hall effect circuit to take advantage of its 4.5ns response time. The logic gate latch from the Hall effect circuit (fig. C.8) had also proved to be fast and reliable, so this too was incorporated into the new system.

The final output stage is slightly different, as we no longer need to provide an external gated pulse signal to the DC switch, and we do not need the pulse conditioning Schmitt trigger on the gate of the common source N-FET (fig C.4). Changing the second AND gate of fig. C.8 to a NAND gate and taking its output to the gate of the common source device effectively combines these functions (fig. C.17).

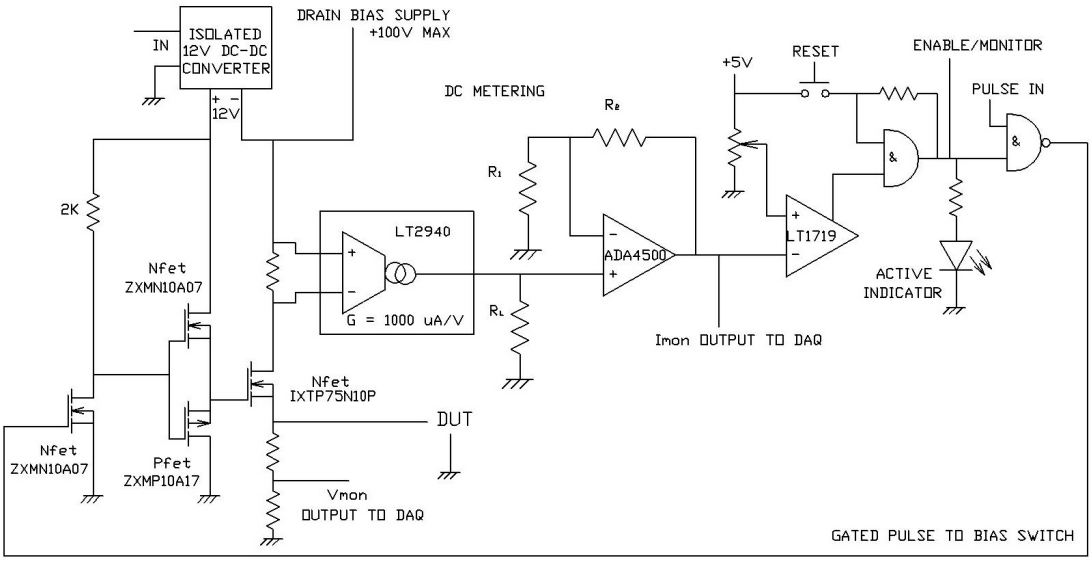

Figure C.17 The integrated Bias Switch, Current Meter and Overload Trip.

The ENABLE line is used to inhibit the RF switches, and can also be used for software monitoring of the trip state. It would be a simple matter to use a digital line from the DAQ to provide a software RESET facility, though this should be connected through a monostable or capacitor to avoid the trip being disabled by the RESET line being held high.

C.6 Gate Bias Switching

In large power amplifiers it is common practice to perform blanking by switching the low voltage, low current gate supplies rather than the high current, high voltage drain supply, whether the intention is to conserve DC power or reduce RF noise output this is an attractive choice as small SMD transistors can easily cope with the currents and voltages involved allowing compact high speed circuits to be realised. When working with enhancement mode devices with a positive gate bias the task is almost trivial, especially with VDMOS and LDMOS devices with effectively zero gate current, since the bias supply is likely to have an output impedance of several hundred ohms or more a

FET can be used to short this to ground with no ill effects. To minimise noise output and to avoid possible Class C operation the driving stages should also be gated, and ideally the RF source too.

With depletion mode devices with negative bias supplies such as GaAs and GaN the problem is more complex, not only will some form of logic level shifting be essential to drive from a positive TTL/CMOS logic system, but the required function is to switch between two different negative voltages rather than one voltage and ground. A solution to this problem was developed during the Resistive Drain load work discussed in Chapter 5 and Appendix G, using an Analog Devices ADG3123 logic level shifting i.c., see fig. C.18.

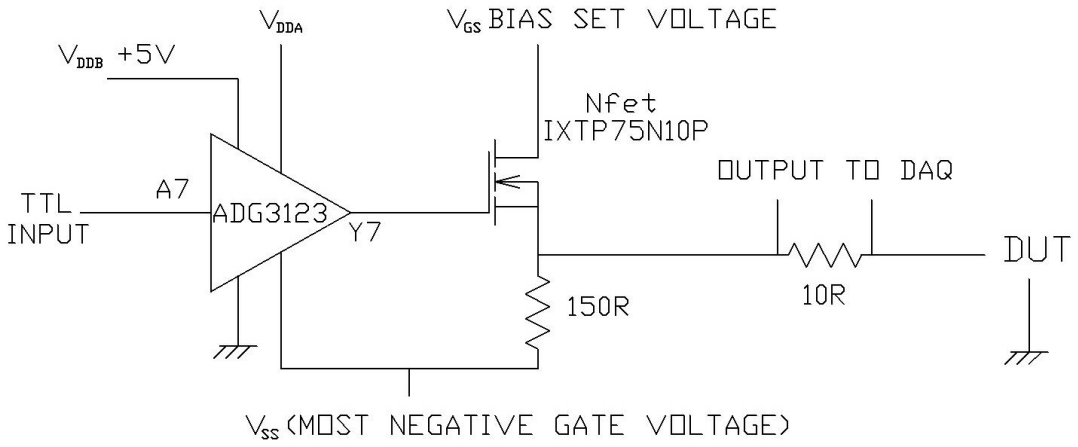

Figure C.18 A gate bias switching circuit for depletion mode devices.

.A logic signal applied to pin A7 of the ADG3123 will cause pin Y7 to switch between V_{DDB} and V_{SS}, causing the output of the N type FET to switch between V_{SS}, which should be chosen to ensure adequate pinch off, and $V_{GS\ set}$, which should be adjusted to achieve the desired bias set point. When using load pull software $V_{GS\ set}$ would be generated from the bus controlled PSU normally used to provide the steady state gate bias so that normal functionality is preserved, the usual DAQ monitoring circuit can be used to measure the voltage and current during operation.

Appendix D

An Examination of GaN on SiC devices using the pulsed AHLP apparatus.

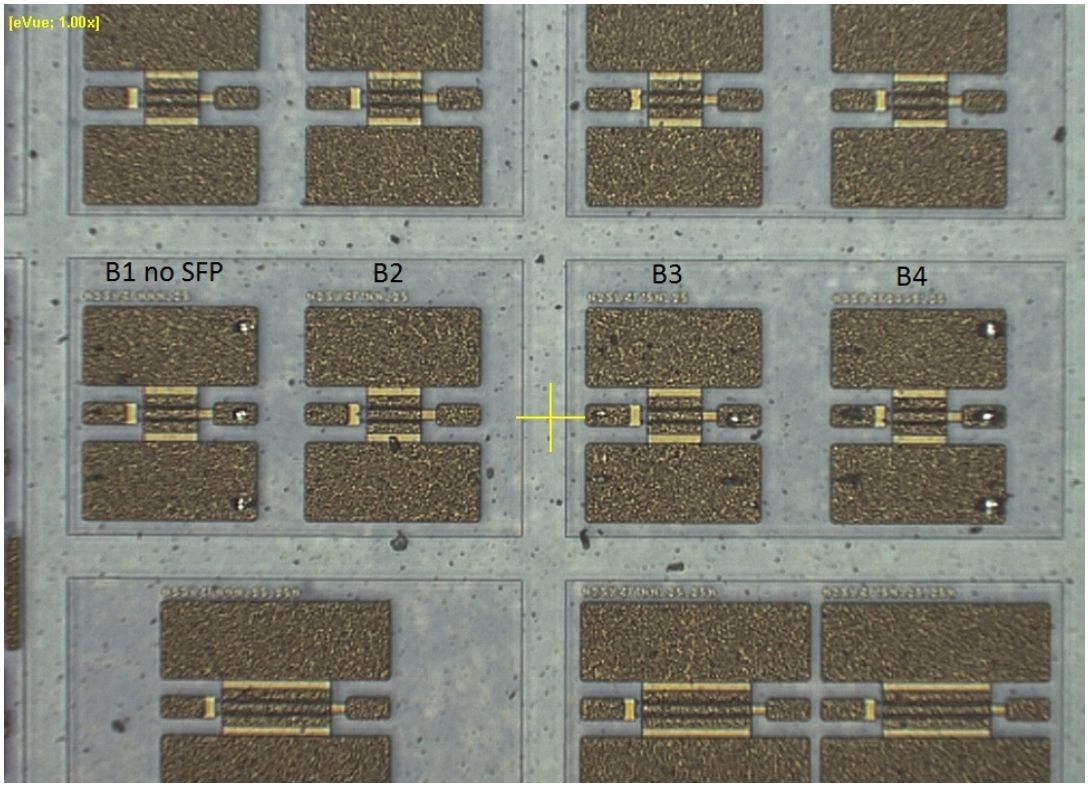

Figure D.1 The row of four different Win 2x125 GaN on SiC devices, part of an array repeated 48 times across the wafer.

D.1 Introduction

A series of tests was undertaken on behalf of the WIN Semiconductor Corporation of Taiwan, to assist in the development of their GaN on SiC product range. As part of this series three different designs of Source Coupled Field Plate (SFP) were compared, along with a similar die without an SFP. The results and conclusions of these tests were published in "Development and Control of a 0.25µm Gate Process Module for AlGaN/GaN HEMT Production" [7], and were also referenced in "Advanced Waveform Engineering Tool for use in device technology optimization: *RF Pulsed Fully Active Harmonic Load Pull with Synchronized 3eV Laser"* [9].

An SFP is a metal plate deposited over the gate region of a device, insulated from the gate and channel but connected to the grounded source. The intention is to assist in clearing away trapped charges from the gate region and so allow the channel to rapidly resume full conduction as the device becomes biased on. Clearly there is the possibility of negatively impacting other aspects of performance, notably the gate-source capacitance and hence the practical upper frequency limit for the device. The objective of these tests was to establish the style of SFP design which would provide adequate charge clearing with the minimum of disturbance to the RF performance.

D.2 Methodology

The test devices were provided on a full thickness 4” SiC wafer without a metal backing on the reverse, it can be seen from the shadows in fig. D.1 that these wafers are transparent to the visible light spectrum. The four different designs were fabricated in a row adjacent to each other, with the objective of keeping all other aspects of the process identical for practical purposes. The pattern of four devices formed a small part of an array of designs, this array being repeated over the surface of the wafer, a total of 48 complete arrays being available.

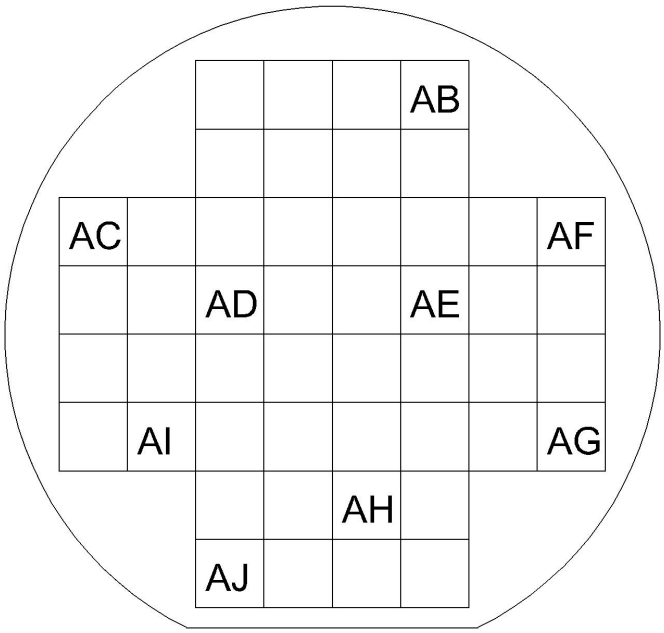

Figure D.2 Location of the test cells chosen for testing on wafer EN00401206.

As a first step nine arrays were chosen, spaced across the wafer as shown in fig D.2, this serves a dual purpose, it allows a typical device to be chosen, and also gives an insight into the consistency of the process. The labels shown are purely arbitrary and simply identify the arrays during these tests. The die themselves were identified as type B1, without an SFP, and B2 to B4 with the three different style SFPs, hence a die is described by its array letters and type designator, e.g. “AH B1”. The array letters are unique to this wafer, so the EN00401206 identifier is implied.

The VTD based Pulsed FAHLP system described in Appendix B, reference [5] “Waveform Engineering Beyond the Safe Operating Region” and reference [9] was employed. A fundamental frequency of 900MHz was used for the RF tests, this is high enough for phenomena such as knee walkout to be apparent, but low enough to permit accurate measurement of the higher harmonics and to simplify the de-embedding process. Since the objective is to study trapped charge problems a 10μs pulse width with a 10% duty cycle was used, effectively eliminating thermal effects from the results, as seen in chapter 2.

In order to identify a set as typical, the B2 die of each of the designated arrays was measured at various loads along the real axis with a drain bias of 28V. Plotting the various dynamic loadlines on the same axes forms what is known as a fan diagram, which is a useful way of presenting a great deal of information simultaneously, see fig. D.3 below.

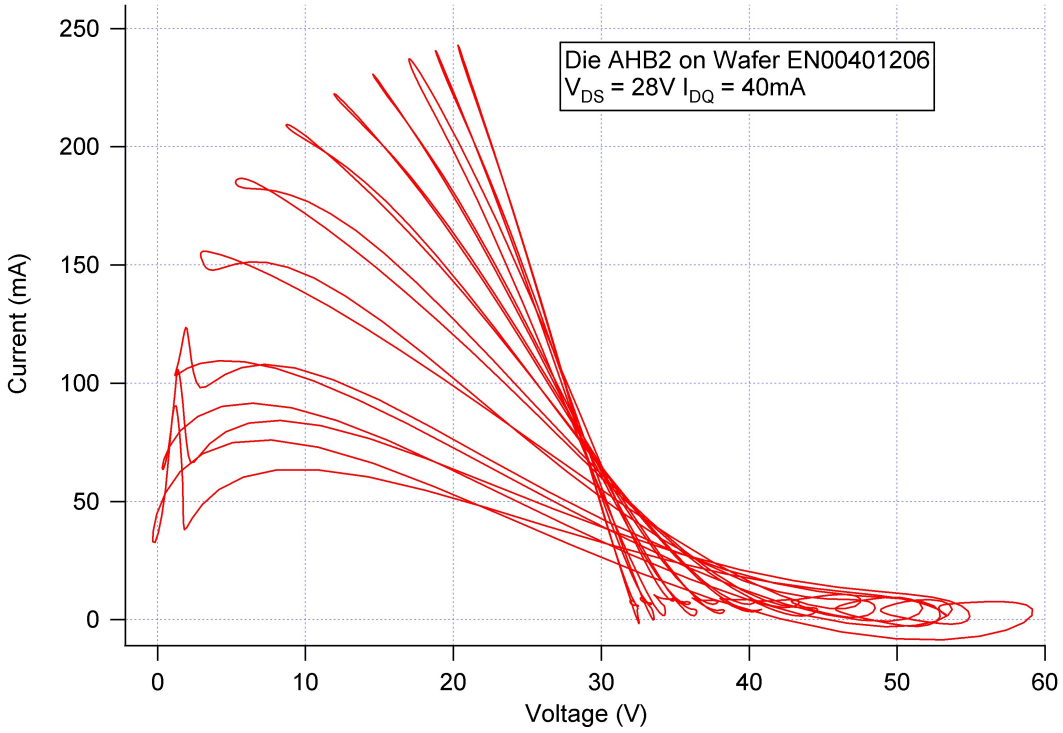

Figure D.3 Fan diagram of type B2 die from array AH with 28V drain bias.

By examining the above diagram it is easy to determine the load which should be used for an application, the shape of the knee can be seen clearly allowing a compromise between voltage swing and maximum current to be selected. In this case a load of Γ = 0.7 (283R) was chosen as the likely design target, so all of the type B2 die were compared at this load, fig D.4.

It can be seen that the characteristics are very similar, so the process control must be good. Die AH was chosen as the most representative, its loadline is shown in black in fig D.4. A range of tests was then carried out on all four of the AH die, at drain bias voltages of 18V, 28V, 38V and 48V. DCIV measurements were also taken to reveal the degree of "knee walkout" taking place, though in the case of the B1 die shown in fig. D.5 it is very apparent that the total lack of an SFP is resulting in severe walkout, increasing the drain bias results in a decrease in the output power and consequently a complete collapse in efficiency.

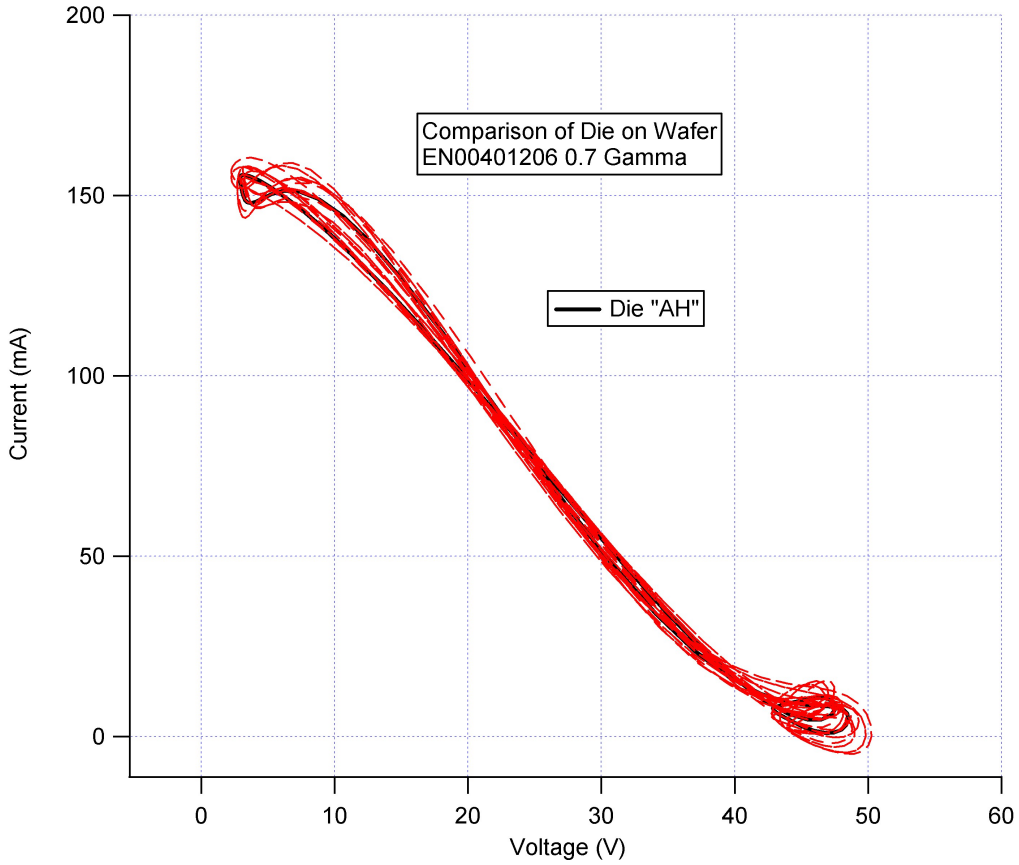

Figure D.4 Γ=0.7 loadlines for all of the designated type B2 die.

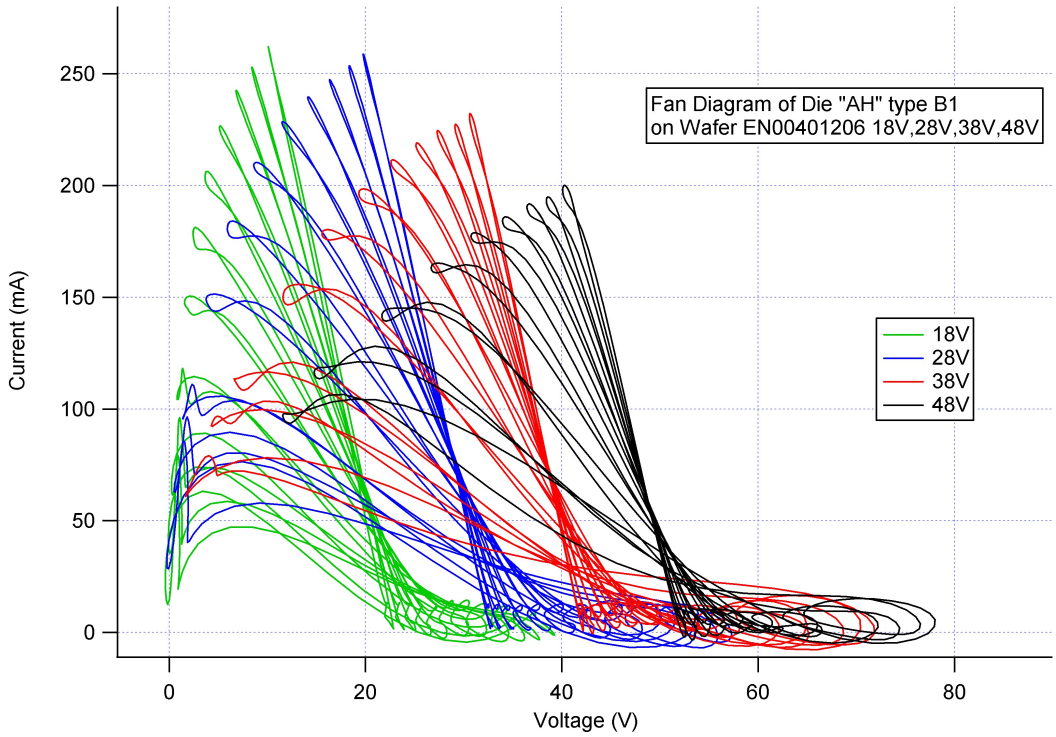

Figure D.5 Fan diagram of type B1 die at various drain bias voltages.

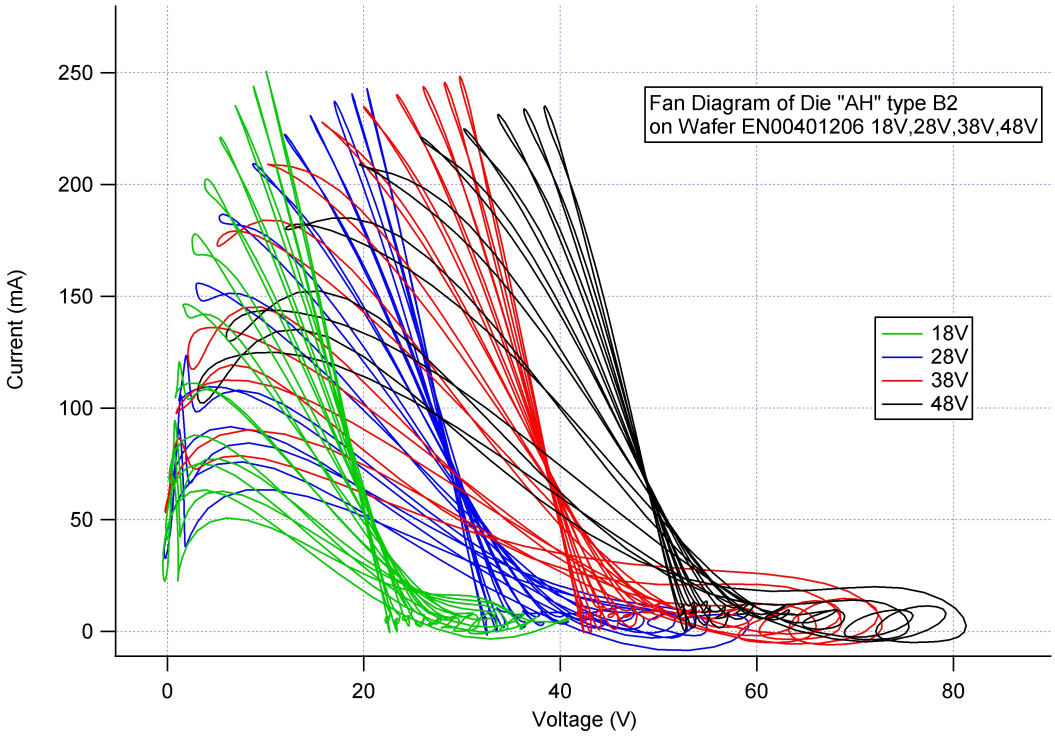

Figure D.6 Fan diagram of type B2 die at various drain bias voltages.

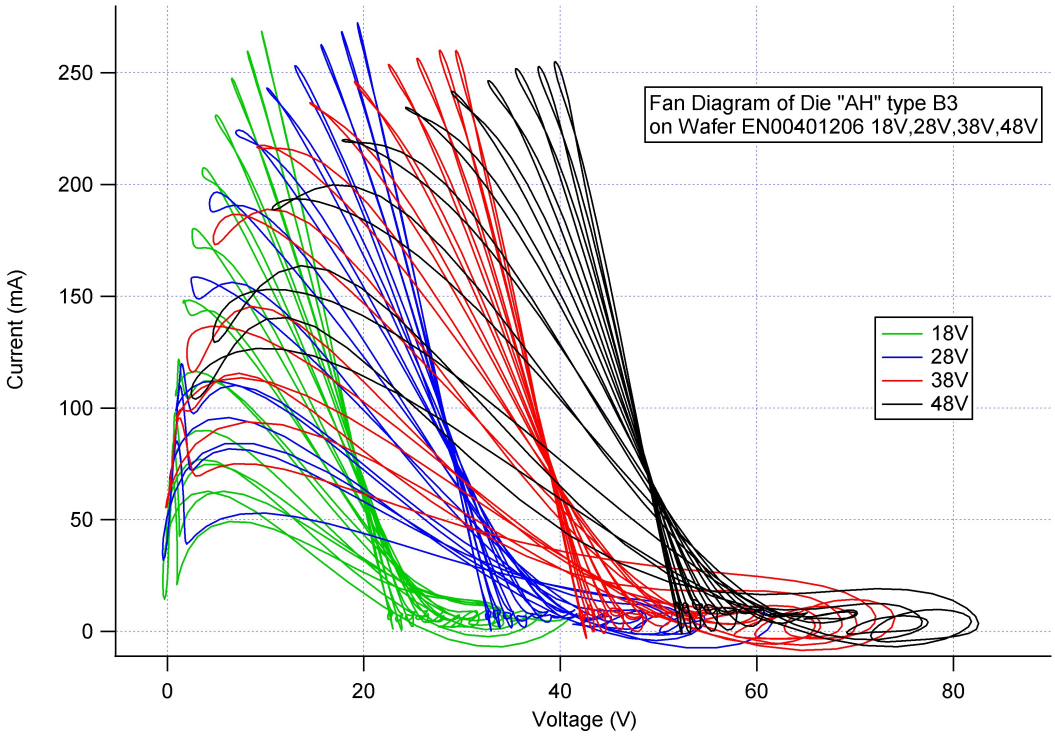

Figure D.7 Fan diagram of type B3 die at various drain bias voltages.

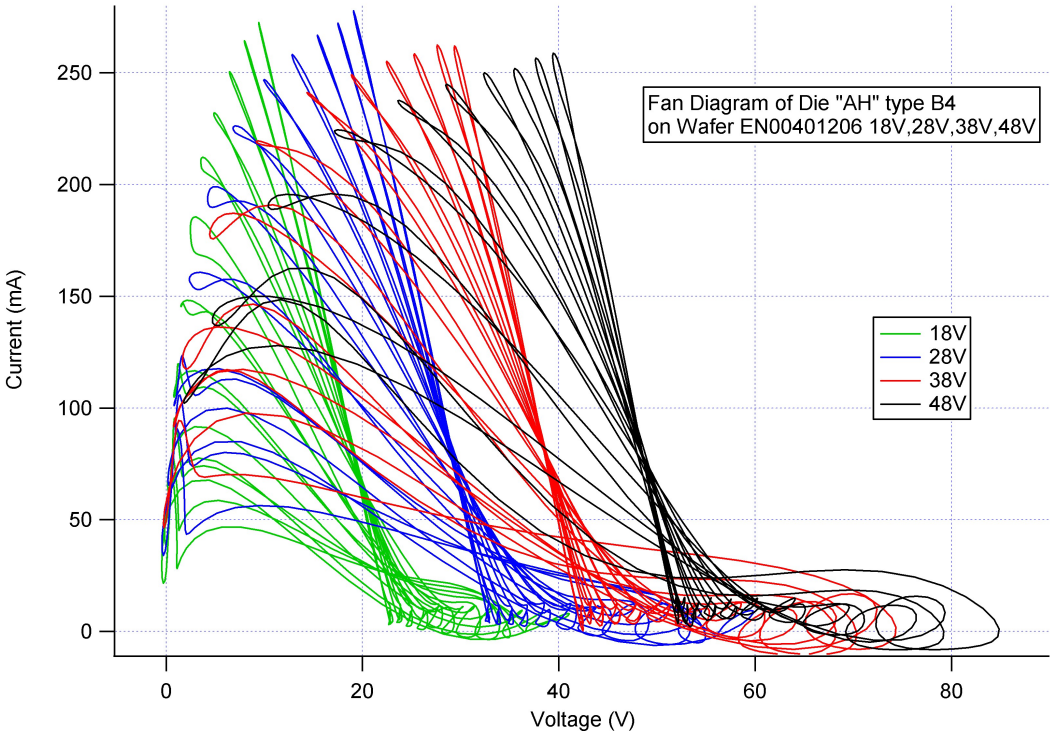

Figure D.8 Fan diagram of type B4 die at various drain bias voltages.

Regarding figs. D6 to D8, it is apparent that the Type B2 SFP results in a considerable improvement in the high bias voltage loadlines, and Type B3 and Type B4 are better still. A full analysis of these results and details of the structures are presented in reference [7].

Appendix E

Examination of a GaN on Si device using the pulsed AHLP apparatus.

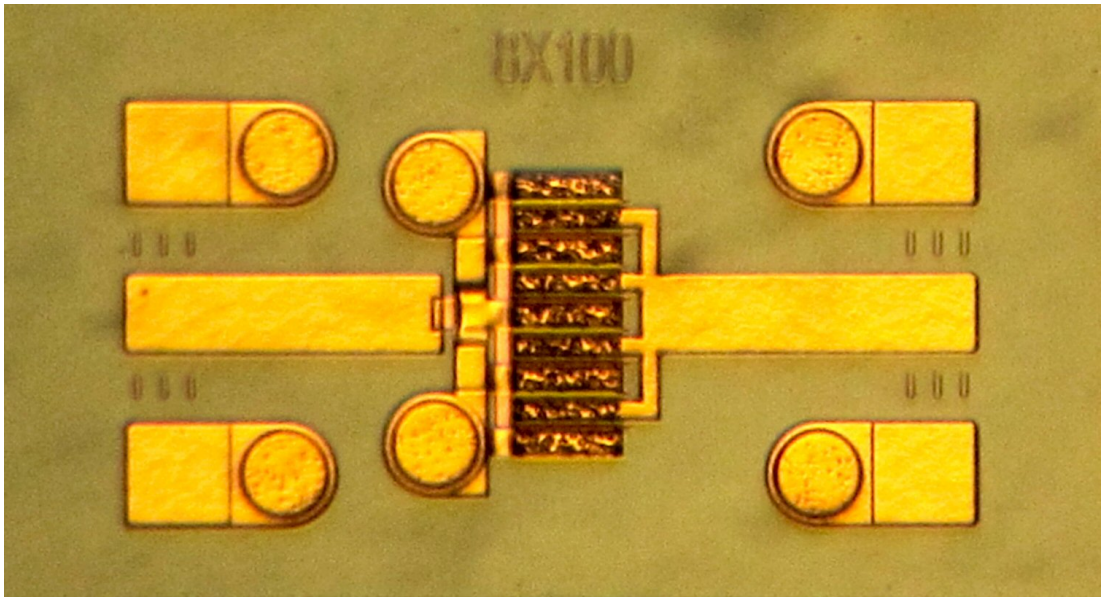

Figure E.1 8x100 GaN on Si device.

A device manufactured from GaN on silicon rather than silicon carbide was found to deliver disappointingly low efficiency. Since silicon has a lower thermal conductivity than silicon carbide it was suggested that the problem might be excessive thermally induced knee walkout due to the inevitable higher channel temperature. To test this preposition sets of fan diagrams were taken in both CW mode and 12% duty cycle pulse mode, with class B bias. If true we would expect to see reduced knee walkout under pulsed conditions. The apparatus used was the VTD based Fully Active Harmonic Load Pull system as described in Appendices B and D.

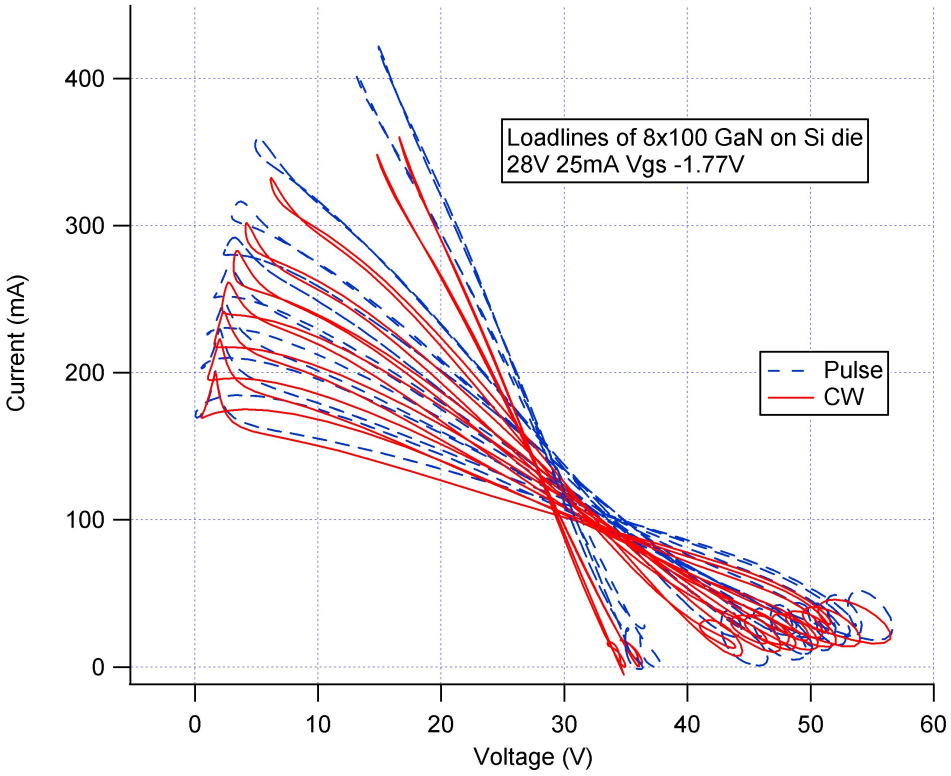

Figure E.2 Dynamic Loadlines for a 8x100 GaN on Si device.

It can be seen that there is significant reduction in current at lower impedances (steeper loadlines), but around the knee region likely to be targeted for RF amplifier applications the reduction is not that great. However, looking at the opposite end of the loadlines reveals that the current is failing to pinch off at higher voltages, and it is this which is causing the poor efficiency.

The finding is very significant for the system engineer, for there are a great many applications involving a high peak to average power ratio where the collapse under CW conditions is not relevant, and the greatly reduced cost of the silicon substrate compared to silicon carbide would make these parts attractive, however the pinch off behaviour might preclude some of these. For systems where the signal is generally at a low level but occasionally peaks the poor pinch off might cause a very slight fall in performance, for radar type applications where the signal is either off or at full power it would give rise to poor efficiency and reduced output power.

A further concern could be the high drain voltages experienced away from band centre when attempting the new continuous mode type of amplifier. The reactive component of the load will cause much higher voltages, if this exacerbates the pinch off problem then the wideband performance will be very disappointing. Without the insight given by Waveform Engineering methods this could be assigned to failure to achieve continuous mode operation correctly, when in fact the energy loss is unavoidable.

As a result of these measurements it proved possible to identify the problem as a parasitic conduction layer forming in the silicon substrate, and to greatly reduce the magnitude of the current flowing in this layer and hence recover the major part of the performance by improvements to the manufacturing process [24].

Appendix F

High Power GaN on Silicon device Analysis.

Following on from the work described in *Appendix E*, a device on the same process but intended for operation at higher drain bias was examined, designated MMXB. The device also had a much greater gate periphery, and was constructed in an unusual parallel format, with links and air bridges connecting the two halves (fig. F.1). Being a relatively high power device it might be thought that it could be difficult to perform active load pull tests at wafer level, however since the optimum operation loads are close to 50Ω it may in fact be measured without excessive reverse power.

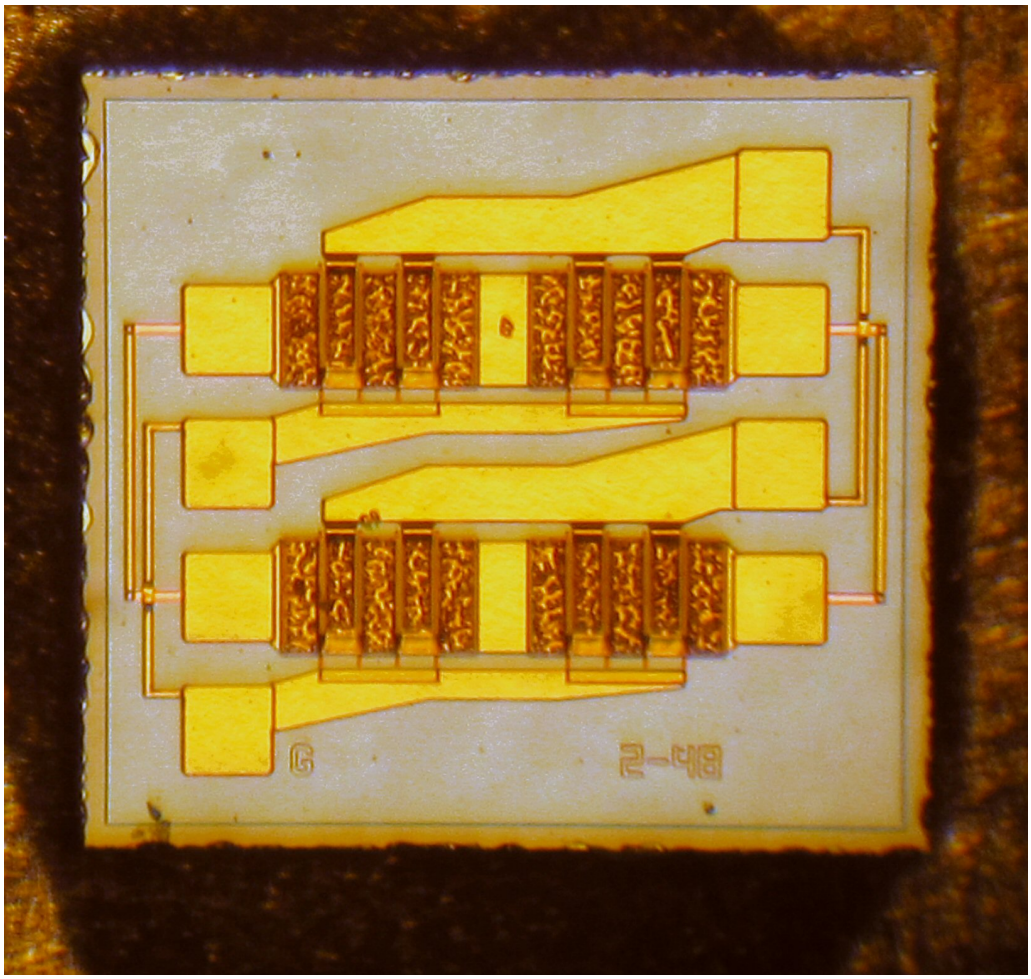

Figure F.1 The large GaN on Si device (MMXB die).

As a first step pulsed and CW DCIV traces were taken, over a range of temperatures. It was anticipated that there would be a substantial difference between the steady and pulsed conditions and this did indeed prove to be the case, as seen in fig. F.2, which shows the curves obtained at Vgs = +0.5V.

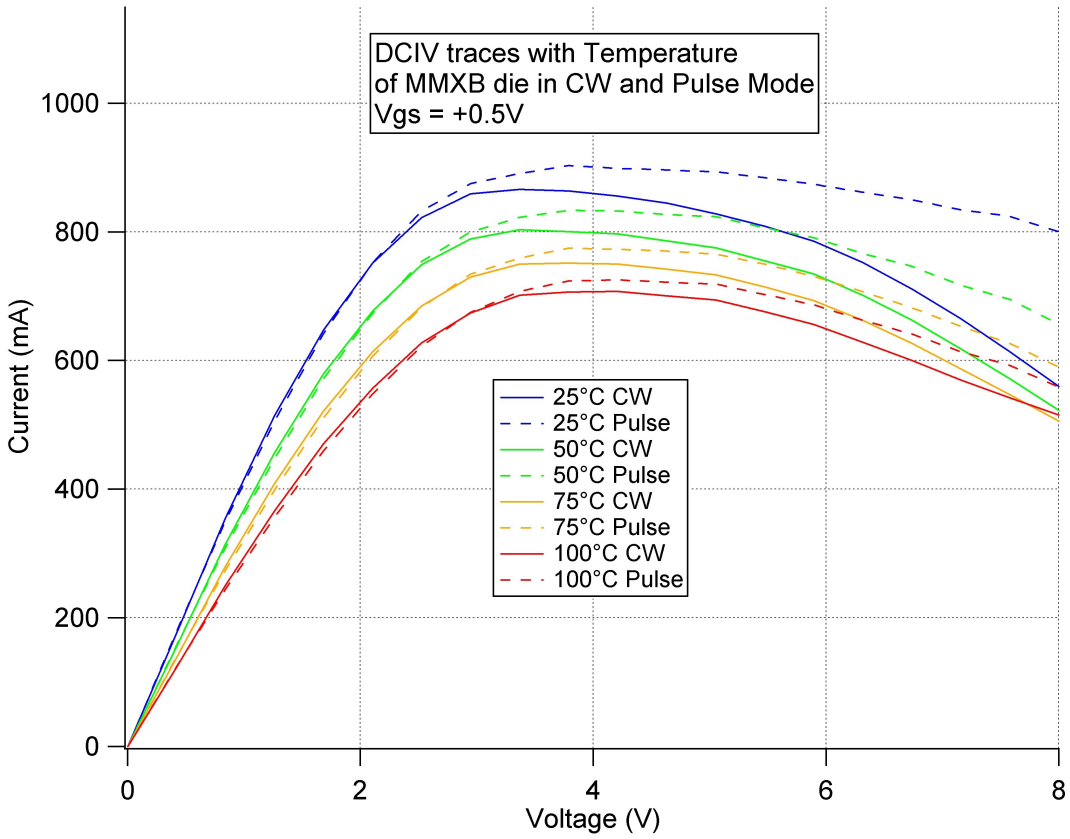

Figure F.2 DCIV traces with temperature for GaN on Si MMXB device under pulse and CW operation. Pulse width 500µs, duty cycle 1%.

Clearly there is a falling off of current with increasing drain bias in the steady state condition which is greatly reduced in the pulsed condition, consistent with a rise in channel temperature, as shown in the graphs.

The pulsed 3eV laser was also brought into use, to highlight any trapping behaviour which might be present.

Sweeping at lower gate voltages but higher drain voltages shows that there is clearly a trapping mechanism at work,

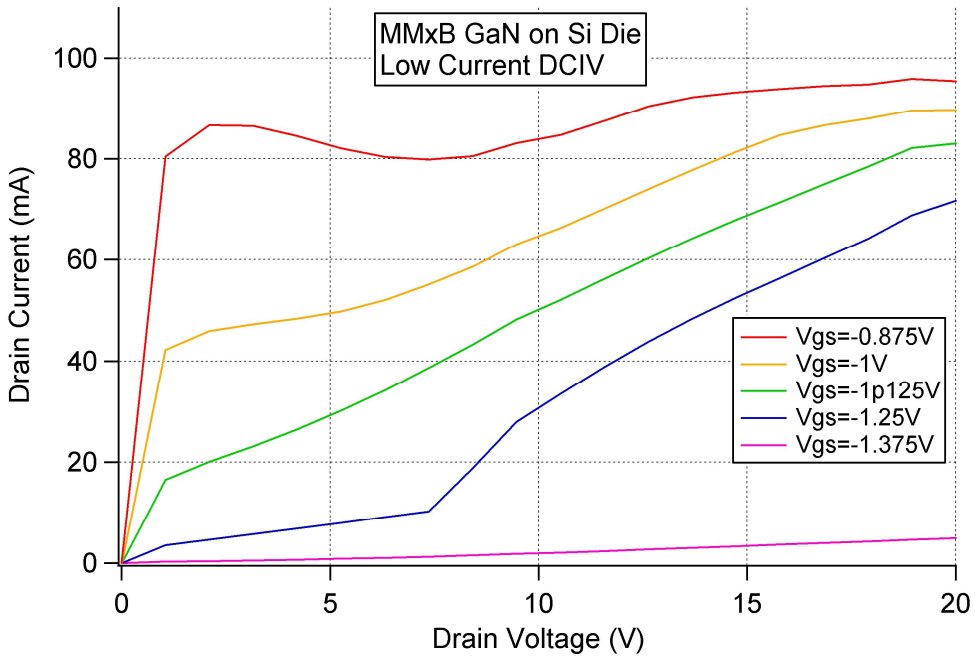

Figure F.3 Higher Drain Voltage DCIV sweeps.

The dip in the Vgs=-0.875V line shows that traps are forming as Vds reaches +3V, but are then swept away as Vds rises above +7V.

Once the DCIV measurements were completed attention was turned to the RF performance, commencing at Vds = 18V, followed by 28V and 38V in turn.

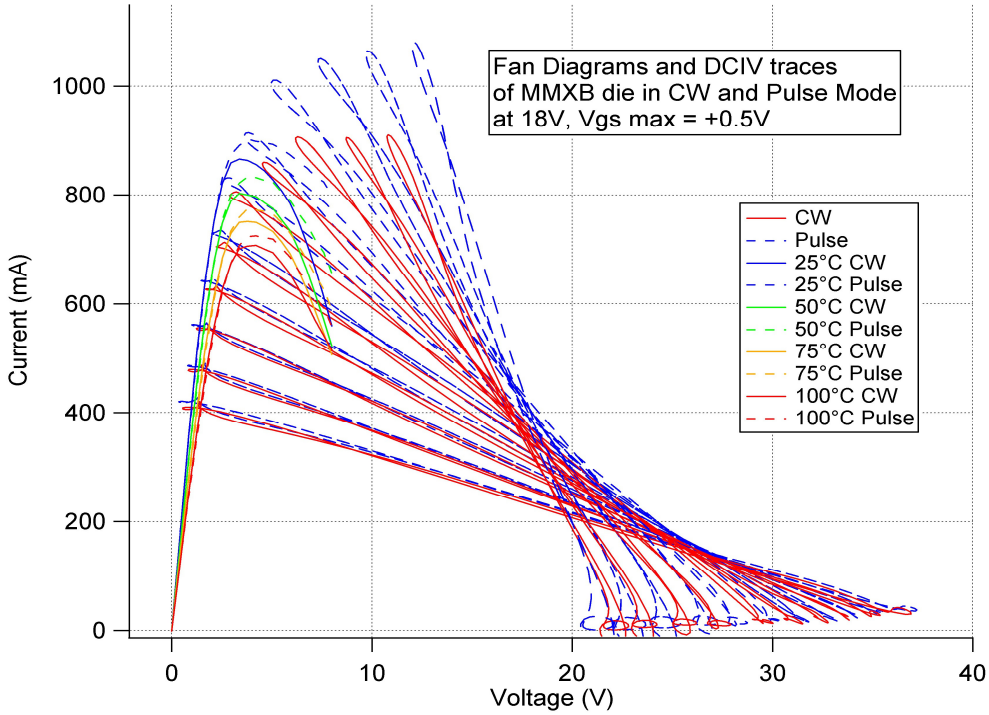

Figure F.4 Loadlines for a GaN on Si MMXB device at 18V drain bias. RF pulse width 10µs, duty cycle 10%. DCIV pulse width 500µs duty cycle 1%.

Considering the 18V curves seen above, we can see that at the shallower, high impedance loadlines there is little difference between the CW and Pulse mode curves, and both reach the DCIV lines. The shallowest line represents Γ=+0.3, the other lines are in 0.1 steps up to Γ=-0.7 and -0.6 pulse and CW respectively. By the forth line, Γ=0 (50Ω) the Pulse and CW curves are beginning to diverge, as the CW performance falls away from the DCIV trace. The process then continues rapidly and by Γ=-0.3 the two are distinctly different, the CW lines are now hitting a limit around 900mA, whereas the pulse lines are carrying up to above 1A.

The pulse performance is very good, exceeding even the pulsed DCIV curves, this is due to the relatively long pulses (500µs) used for the DC measurements, compared to the RF pulses (10µs).

The behaviour seen here is consistent with thermal degradation, as indicated by the drop in the DCIV lines, there is no sign of a trap induced walkout problem, which is as expected at this low drain bias voltage.

An area which is beginning to give cause for concern is at the high voltage end of the high impedance loadlines, significant current is flowing when the device should ideally be pinched off. Clearly this will have an adverse effect on the efficiency, and these lines do represent the correct RF operation area for the device.

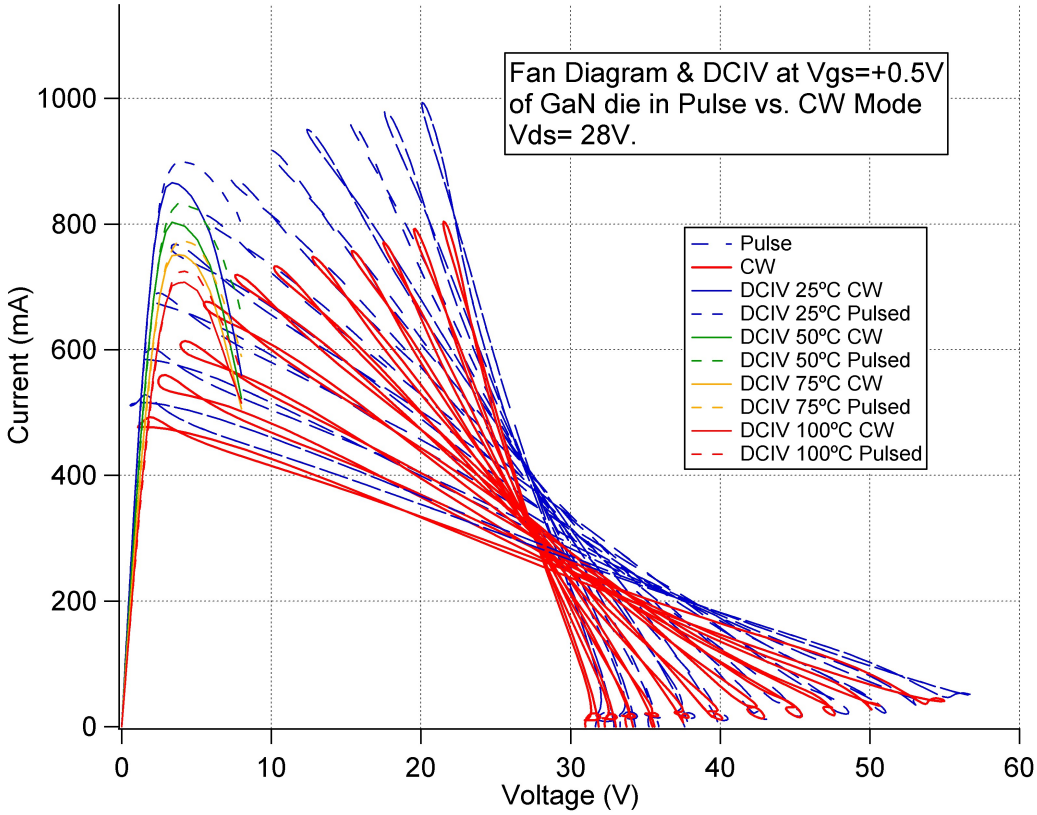

Figure F.5 Loadlines for a GaN on Si MMXB device at 28V drain bias. RF pulse width 10µs, duty cycle 10%. DCIV pulse width 500µs duty cycle 1%.

With the drain bias raised to 28V a different picture emerges, now the CW lines are moved down and away from the pulse and DCIV lines even at Γ=0.4, the shallowest load. The separation increases rapidly as the loadline steepens, and now even the pulsed lines have fallen away from the cold DCIV lines. At loadlines steeper than Γ=0 (50Ω) the peak current is reduced by approximately 20%, however such loads are a substantial departure from the correct RF operating point. Maximum drain efficiency occurs at Γ=+0.3 in CW mode, but at Γ=+0.2 in pulse, while maximum power stays at Γ=+0.1

The poor pinch off performance is worsening, as might be expected.

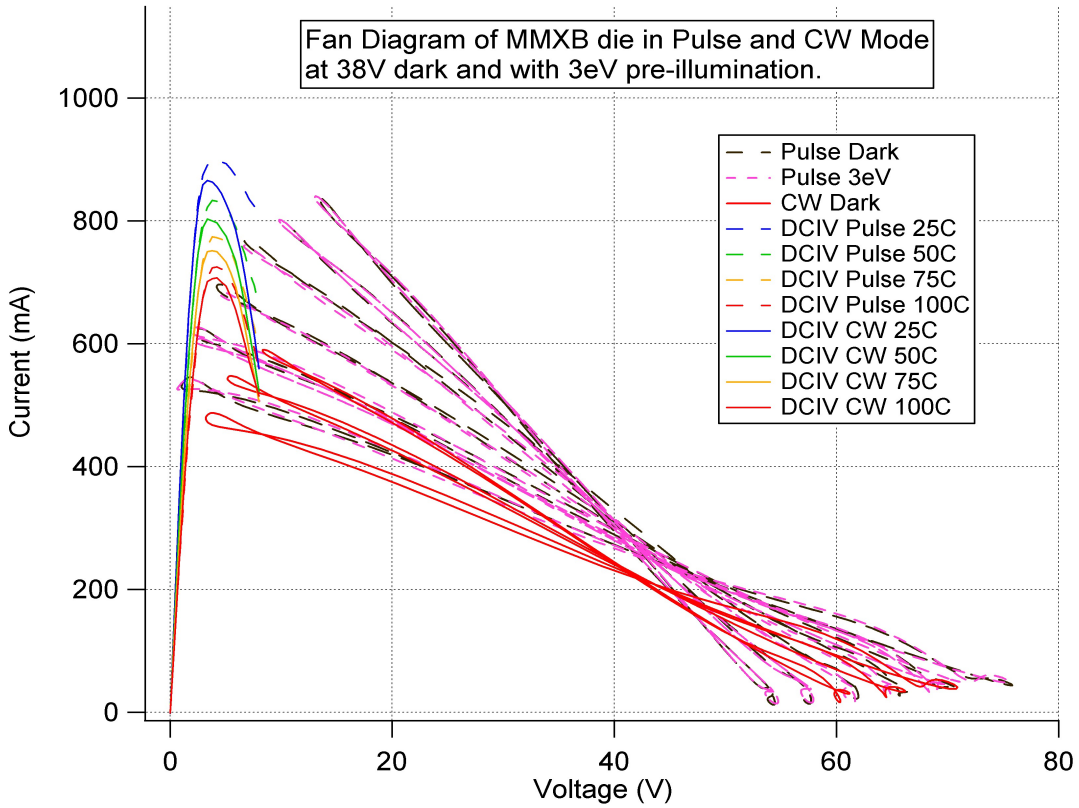

Figure F.6 Loadlines for a GaN on Si MMXB device at 38V drain bias. RF pulse width 10µs, duty cycle 10%. DCIV pulse width 500us duty cycle 1%.

At 38V a very limited range of load impedances were measured, particularly in CW mode. The thermal dissipation is now such that there is considerable risk of destroying the device and damaging the wafer probe (a Cascade high power Z probe). We see that now the CW lines are moved well away from the pulse and DCIV lines, even though these three lines are in the area of best efficiency. The Pulse lines are moving away at all but the shallowest loads.

Also shown on this graph are the lines produced when the synchronised 3eV laser is pulsed alternately to the RF, the intention being to release any trapped charge which might be impairing the performance. The dark and 3eV pulse lines are essentially coincident, so it is reasonable to assume that there is no significant trap related problem with this device, despite the trap related behaviour witnessed during the low voltage DCIV measurements. It may well be that the failure to pinch off fully is linked with this trap free operation, if the supposedly insulating regions of the device are in fact slightly conducting, any potentially trapped charges may be swept away. Certainly the DCIV curves show definite signs of trap formation, fig F.3, so it may be that the loss of efficiency due to the poor pinch off is a price worth paying in some applications.

Footnote: As a result of these measurements the pinch off problem was traced to a parasitic conduction layer forming in the silicon substrate, and the production process was subsequently improved to reduce this to an acceptable level [24], more details are provided in Chapter 2.

Appendix G

The Design and Construction of a Very High Frequency Resistive Load

In order to assist with determining the true cause of memory effects and knee walkout problems in microwave semiconductor devices the apparatus described here was developed. Its application is described in detail in chapter 5, this section is concerned with the principles and practice of its construction.

It is in essence a very simple routine circuit, however the practicalities of achieving good performance into the VHF region means great care must be taken with the design and construction to minimise parasitic elements. Significant amounts of heat can be developed in some modes of operation, so miniaturisation is impractical, and the voltages present must be measured accurately without influencing the circuit unduly. The objective is to replace the tuned narrowband RF load and low impedance DC bias feed with a resistor connecting the drain terminal and the DC supply, in effect presenting the same load impedance to all frequencies including DC.

RESISTIVE DRAIN LOAD TEST EQUIPMENT

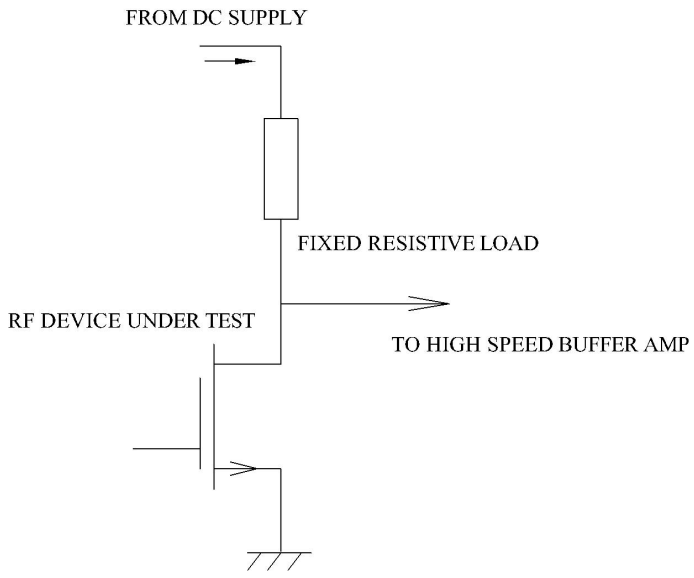

Figure G.1 The basic Resistive Drain Load test schematic.

The device can now be moved to and held at any point on the load line in a nano-second time scale by controlling V_{GS}, which permits a variety of tests to be carried out. The prime goal in developing this was to reveal the extent of I_{DSmax} reduction caused by each

region of the load-line, and so shed light on the cause of residual Knee Walkout seen in GaN devices, however it became apparent that other uses could be found, including incipient breakdown analysis and time constant extraction.

The most critical aspect of the system is the accurate capturing of V_{DS}, the voltage at the drain terminal, then since the supply voltage, $V_{DD,}$ is known the current through the drain resistor can easily be found from Ohm's Law, and from Kirchoff's first law this must equal the device drain current, I_{DS}.

$$I_{DS} = I_R = (V_{DD} - V_{DS})/R$$

It is vital not to significantly influence the voltage by the addition of the measurement circuit so a high impedance probe must be used, and if the analysis of transient effects is to be carried out then a high speed capturing capability is needed. The requirement is further complicated by the dynamic range of the signal, with a maximum value possibly up to 100V, an 8 bit bi-polar oscilloscope will only have +/-128 levels available, making it impossible to measure the small changes in V_{DS} while the device is conducting heavily. A Picoscope 4227 high speed modular oscilloscope was chosen, this combines a maximum sampling rate of 250MS/s with 12 bit resolution and a 3.5ns rise time, but it's input impedance is too low to permit direct connection to the circuit, so a buffer amplifier was added.

A National Semiconductor LMH6732 high speed Op-amp formed the basis of the buffer amplifier, this can realise a 3dB bandwidth of 500MHz, and an output slew rate of 2700 V/μs. The input impedance of 15MΩ and capacitance of 1.7pF means the circuit loading can be negligible. To optimise the performance the buffer amplifier was fabricated on the same board as the main drain resistor, the whole being mounted on pillars inside a metal housing to give minimal capacitance to ground but good electrical screening. A consequence of this method of construction is that a lead must be used to connect the amplifier to the oscilloscope, it is essential at the frequencies being measured to match impedances and terminate such leads carefully to avoid distortion and ringing, in order to achieve this a 47R resistor was connected between the op-amp and a 50R BNC socket, a 50R cable was then used to link to a 50R "through" termination fitted directly to the input port of the oscilloscope. In this way the Op-amp, with its own 3R

impedance, “sees” the correct 100R load, and good impedance matching is maintained throughout.

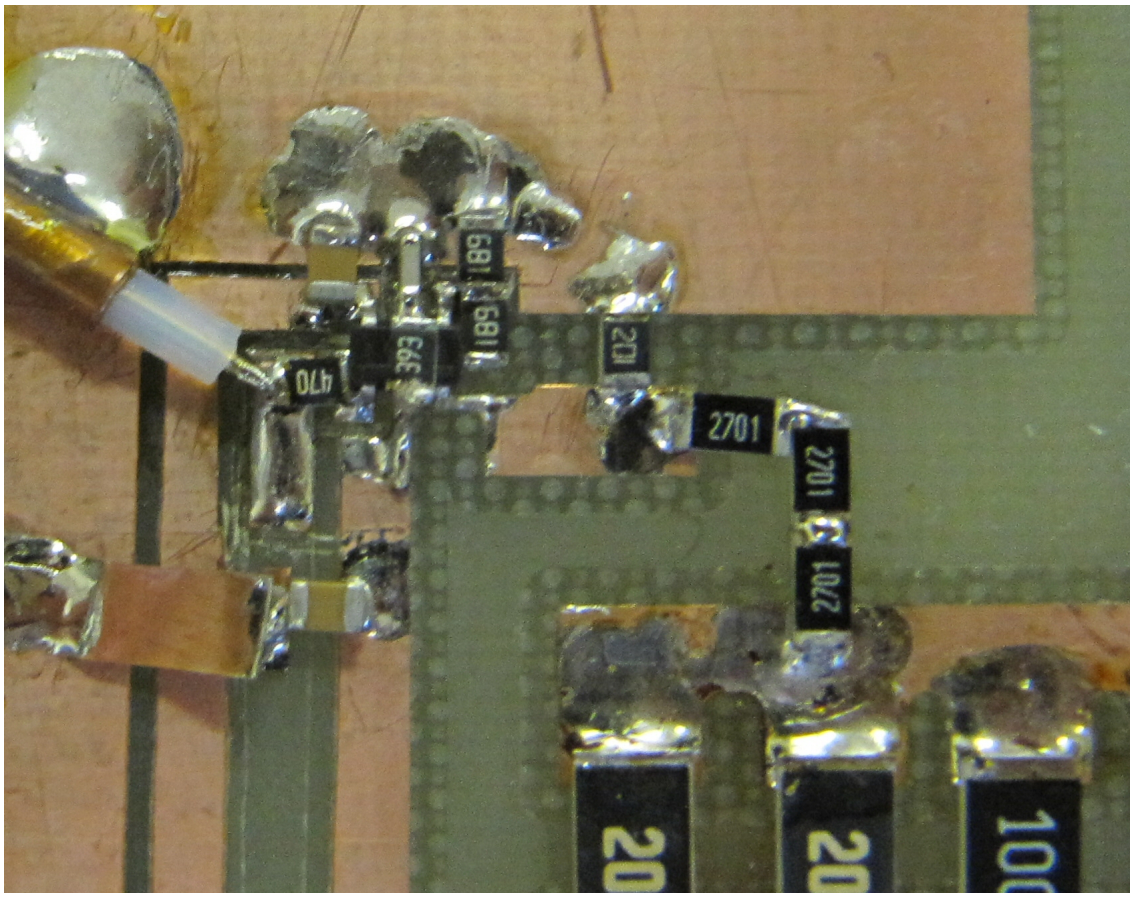

Figure G.2 The high speed buffer amplifier and some of the resistive drain loads.

To make the system more versatile a number of different resistance values must be selectable, this was achieved by using a DIP style eight way switch, with all eight inputs connected to the supply side and the eight outputs fanned out to a selection of high power surface mount resistors. Ideally the system should cover the range from Γ=+0.95 to -0.6 in reasonably fine steps, this would enable a good range of loads to be presented to all likely parts, however this cannot be achieved with only eight values, so in practise the selection was adapted when moving between GaAs and GaN. Table G-1 below lists the equivalent resistance and maximum power dissipation when V_{DD} =100V for various values of Reflection Coefficient.

Reflection Coefficient Γ for Zo = 50R	Resistance (ohms)	Maximum Power (watts) Vdd = 100V
0.95	1950	5.1
0.9	950	10.5
0.85	617	16.2
0.8	450	22.2
0.75	350	28.6
0.7	284	35.2
0.65	236	42.4
0.6	200	50
0.5	150	67
0.4	117	85
0.3	93	108
0.2	75	133
0.1	61	164
0	50	200
-0.1	41	244
-0.2	33	303
-0.3	27	370
-0.4	21	454

Table G-1 Equivalent resistance and power dissipation for various Reflection Coefficient values.

It is obvious that the power levels calculated for the lowest loads are rather impractical, these represent rather extreme circumstances, a large device at the limits of wafer probing, at loads well below the optimum RF load and continuously conducting rather than switching. Since the main objective is to study process performance there is little need to measure large devices in this way, and for most tests the duty cycle will at least

halve the dissipated power, in many cases a 90% reduction can be arranged. Figure G.3 shows the final assembly, the circuit board is single sided FR4, mounted on pillars to minimise the capacitance to ground. The resistors used are SMD 2512 parts rated at 2 Watts each, with up to five in series to give the power handling needed. The line of three 10 ohm resistors at the top of the board is shown with copper foil heatsinks connecting them, this proved necessary to avoid scorching the FR4 board when testing an 8x400 GaAs die. Note also the array of decoupling capacitors at the incoming supply end of the board

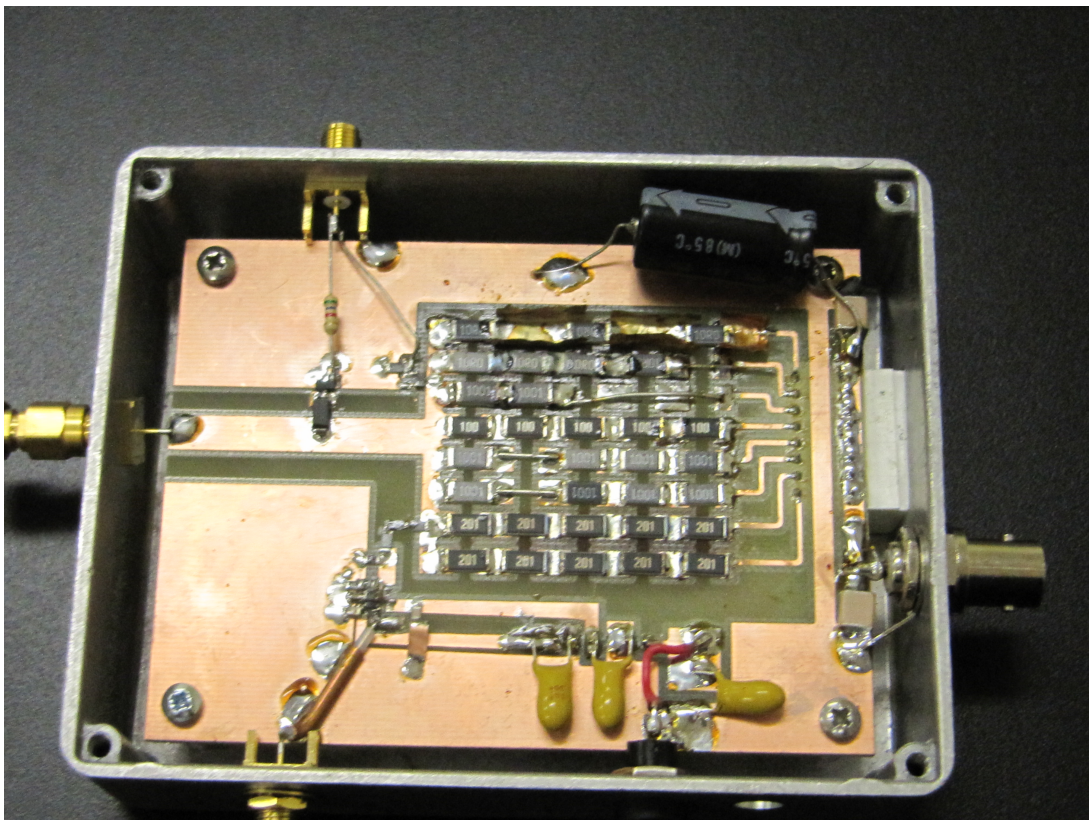

Figure G.3 The switchable resistor array.

The connection between the resistor array and the D.U.T. is critical to the performance, unfortunately it cannot be impedance matched, since the wafer probes have a characteristic impedance of 50 ohms, and we are operating over a range of impedances. Inevitably the resulting mismatch will cause reflective “ringing”, the best that can be done is to minimise the length of the interconnection, and so raise the frequency of the ringing, to reduce the disrupted period as far as possible. To this end the screened box was attached directly to the wafer probe as shown in fig. G.4.

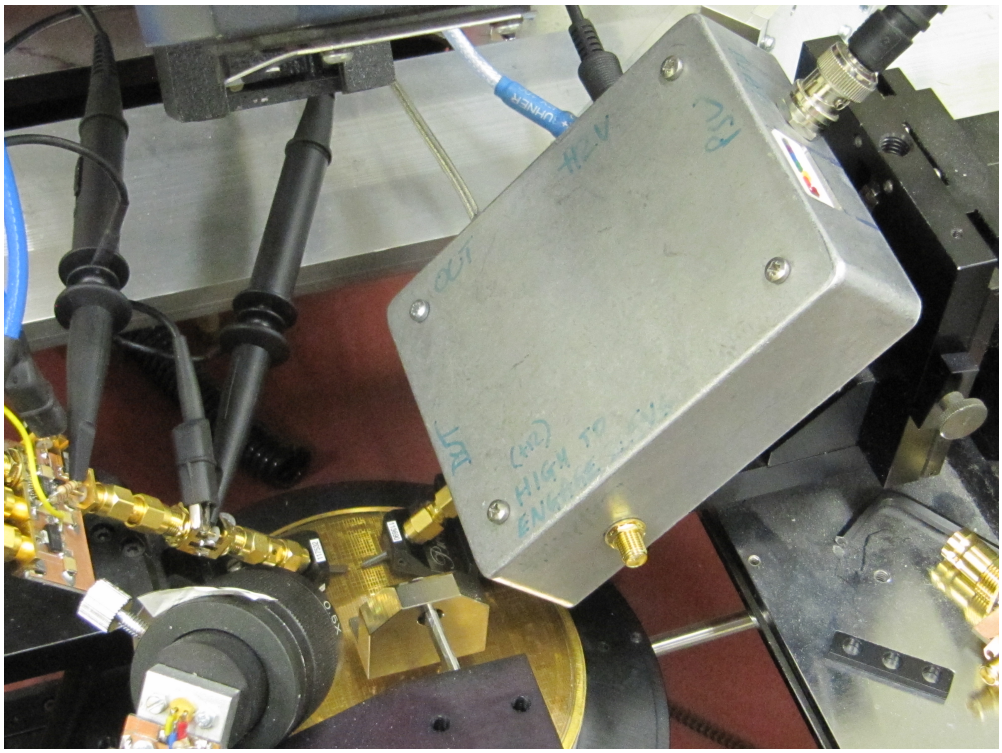

Figure G.4 The Resistive Drain Load in position on the wafer probe station.

The waveform applied to the gate is clearly important, for the principle purpose this apparatus was intended for the ideal would be an instantaneous step change from one voltage to another, the magnitude of each being adjustable. For the first round of measurements this was closely approximated by using a high speed rail to rail comparator to drive the gate. The positive terminal of the comparator's supply was grounded and the magnitude of that supply then governed the negative voltage swing at the gate. Using a MAX998 allowed the negative excursion to be set between -1.5V and -6V, with the high state being around -200mV.

As the investigation progressed a greater negative voltage was required, and a true zero or even positive high state was also desired. To meet these needs a circuit based on the Analog Devices ADG3123 logic voltage level shifter was developed, this uses a TTL input signal to switch its output between two variable supplies, which can be set between +35V and -24V (subject to some detailed constraints, see the manufacturers datasheet). When followed by a buffer this proved capable of cleanly switching the gate from deep pinch off to full conduction in nanoseconds, fig G.5. The circuit, fig G.6, is optimised for fast switch on, as this is the critical area of interest for these tests. Since the intention is to soak the device at varying degrees of pinch off before measuring the subsequent switch on behaviour, the time taken to change from conduction to pinch off is less important.

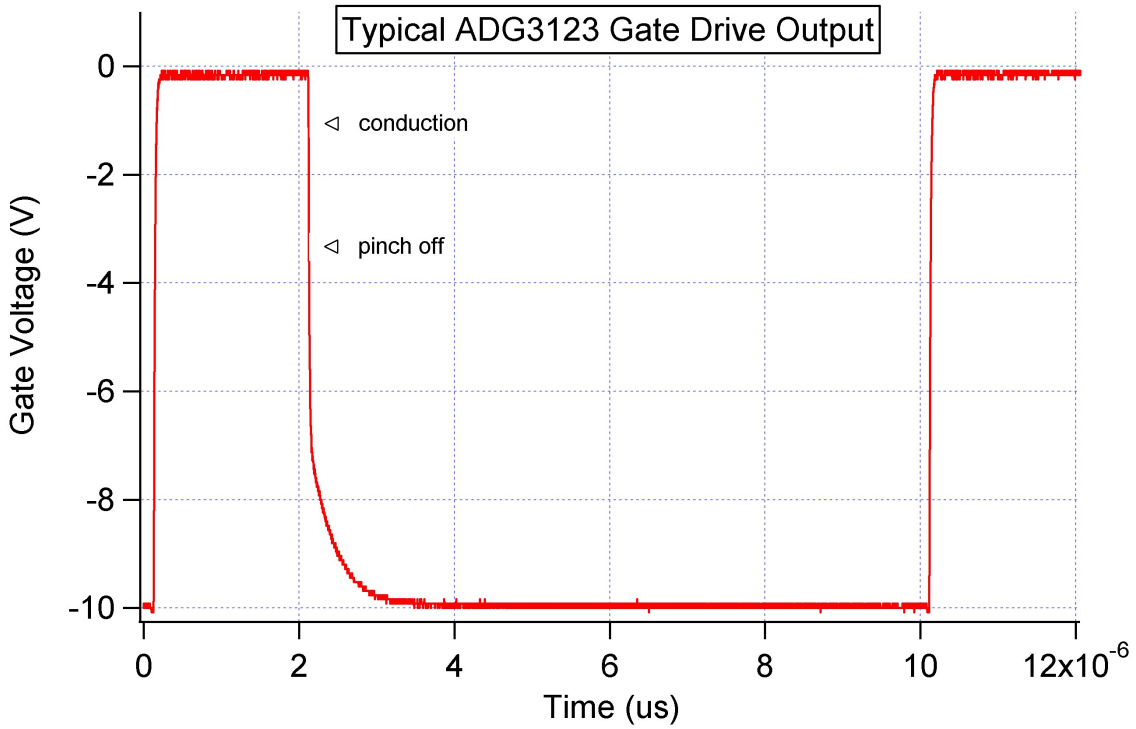

Figure G.5 A typical gate drive waveform generated by the ADG 3123.

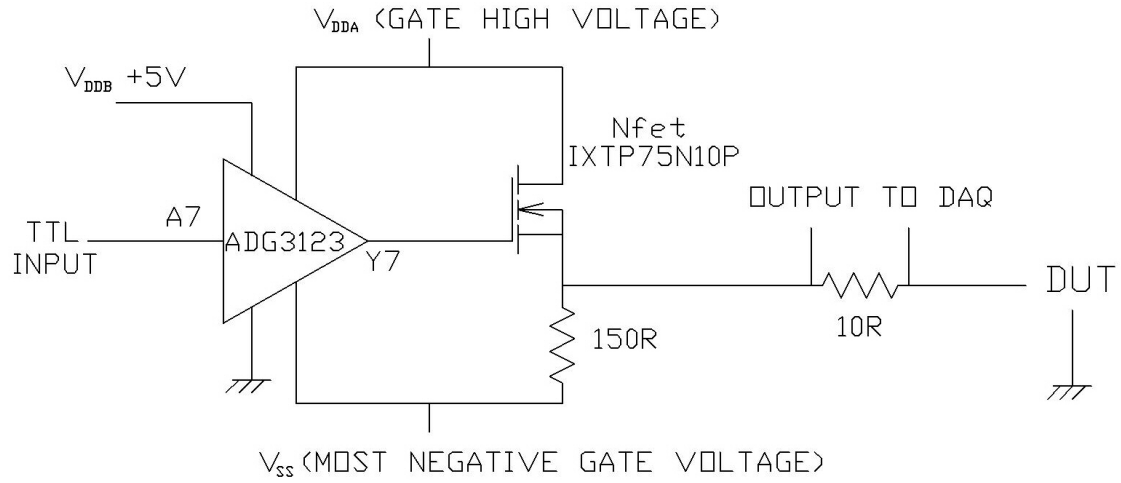

Figure G.6 the ADG 3123 gate switching circuit.

In the circuit shown in fig. G.6, one of the "digital" gates is used, A7-Y7, the output Y7 switches between V_{DDB} (+5V) and V_{SS}, so as long as V_{DDA} is more than the threshold voltage of the N-fet below V_{DDB} the N-fet will be turned fully on. The original intention had been to use some of the six "analogue" gates in the ADG3123 which switch between V_{DDA} and V_{SS}, however the resulting waveform suffered from overshoot and ringing which was unacceptable in this application. It can be seen that in fact the connection to V_{DDA} serves no particular purpose in this modified circuit, and making the

drain supply of the N-fet independent will allow a negative voltage to be used for the "High" level of the gate waveform, potentially useful for normal RF pulse operation, allowing switching between an adjustable "High" bias set point for RF on and a pinched off "Low" condition.

The switch off performance could be improved by reducing the value of the resistor connecting the DUT gate to V_{SS} of course, but this must be balanced against the current and power handling capabilities of the N-fet chosen, and for normal RF applications a very rapid turn off might not be desirable as it could well cause a very large back - EMF at the DUT drain terminal, it would be quite practical to tailor the switch off time to give a clean transition.