CMOS compatible all-silicon TM pass polarizer based on highly doped silicon waveguide

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Abstract: We propose and analyze via simulation a novel approach to implement a complementary metal-oxide-semiconductor compatible and high extinction ratio transverse magnetic pass polarizer on the silicon-on-insulator platform with a 340 nm thick silicon core. The TM-pass polarizer utilizes a highly doped p-silicon waveguide as the transverse hybrid plasmonic waveguide. We observed an extinction ratio of 30.11 dB and an insertion loss of 3.08 dB for a device length of 15 μm. The fabrication process of the proposed TM-pass polarizer is simpler compared to the state-of-the-art since it only uses silicon waveguides and does not require any special material or feature size.

OCIS codes: (230.5440) Polarization-selective devices; (230.3120) Integrated optics devices; (130.2790) Guided waves.

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1. Introduction

Silicon photonics has been recognized as a key technology to fabricate compact optical components and systems [1–4]. The large difference in refractive index between silicon and its native oxide silica enables high-density integration of photonic components. However, this also makes the silicon-on-insulator (SOI) platform highly polarization dependant which greatly limits the large-scale application of the SOI based photonic integrated circuits (PICs) [5]. Hence, polarization management is one of the key requirements in silicon photonics in order to avoid performance degradation [5]. Oftentimes, a polarization diversity scheme [6] is used to avoid this issue. Polarization beam splitters [7, 8] and rotators [9] are required to implement a polarization diversity scheme which increases the complexity and footprint of the overall PIC. Unless a polarization division multiplexing scheme is required, a simple solution will be to use a polarizer which suppresses the undesired mode and passes the desired one.

There are three key features of a polarizer that need to be achieved including achieving a high extinction ratio, a low insertion loss and a compact footprint. In the past, researchers have proposed and demonstrated several transverse electric (TE)-pass and transverse magnetic (TM)-pass polarizers based on complementary metal oxide semiconductor (CMOS) compatible [10–12] and non-CMOS compatible materials [13–15]. Since one of the most attractive features of silicon photonics is the compatibility with the CMOS process which enables low-cost mass volume production, it is desirable to design polarizers using CMOS compatible materials and processes. Dai et al. [16] proposed a TE-pass polarizer with 20 dB extinction ratio using shallowly-etched SOI ridge optical waveguides with a length of 1 mm which is too long from the integration perspective. Sub-wavelength grating (SWG) based TE-pass and TM-pass polarizers have also been demonstrated in [17] and [11] respectively where the grating acts as a Bragg reflector for one mode and as a sub-wavelength waveguide for the other mode. However, SWGs require feature sizes which can not be fabricated using 193 nm deep ultraviolet (DUV) lithography. Polarizers using special materials like graphene and vanadium oxide have been demonstrated in [18, 19] and [20], respectively. However, fabricating these structures are challenging. Furthermore, the design proposed by [19] has a length of 150 μm which is excessively long and the performance of the vanadium oxide based design depends on the insulator-to-metal phase transitions with a critical temperature of 68°C which increases the energy consumption [20] with respect to passive devices. Due to the ability to manipulate light at dimensions beyond the diffraction limit [21], surface plasmon polariton based devices have received increased attention in the recent years [22, 23]. Several hybrid plasmonic waveguide based polarizers have been demonstrated as well in the past [13, 24, 25] in an attempt to increase the integration density of the PICs. Bai et al. [25] demonstrated a TM-pass polarizer based on hybrid plasmonic grating achieving an extinction ratio over 25 dB with a 2.5 μm active length. However, silver was used as the metal which is not CMOS compatible.

Herein, we report a CMOS compatible hybrid plasmonic TM-pass polarizer on the SOI platform with a silicon layer thickness of 340 nm. Although, SOI wafers with 220 nm thick silicon layers are one of the most widely used platforms, it is a suboptimal option for many on-chip components [26]. Peak directionalities of 84% and 71% were obtained for the TE and the TM modes, respectively for grating couplers with silicon layer thicknesses of ~350 nm and ~330 nm, respectively in [26]. Silicon carrier-depletion modulators based on a 340 nm thick silicon

layer have been reported in [27] to achieve better light-carrier overlap by improving the mode confinement. Frequently, a thicker silicon layer is used in hybrid III-V/SOI lasers to achieve better mode coupling [28]. Several polarization beam splitters [29–31], polarizers [25] and multimode interference couplers [32] have been demonstrated as well on 340 nm SOI wafers. Thus, there is a growing interest in developing passive and active devices on the 340 nm thick SOI platform.

In this paper, we demonstrate a TM-pass polarizer using highly doped p-silicon waveguide. The main contribution of our work is the use of highly doped silicon instead of metals to form the hybrid plasmonic waveguide. The real part of the complex relative permittivity of the highly doped p-silicon approaches a negative value and therefore exhibits metal-like properties. Silver and gold are the two most widely used metals in plasmonics [33]. However, these two metals are not CMOS compatible. Utilizing highly doped p-silicon instead of metal enables our proposed polarizer to be fabricated using the CMOS process. Furthermore, the fabrication process gets simpler due to our all-silicon approach since no other material such as graphene, vanadium oxide, indium tin oxide or metals needs to be deposited. According to our analysis, the proposed TM-pass polarizer achieves an extinction ratio of 30.11 dB and an insertion loss of 3.08 dB with a length of 15 μm near 1550 nm wavelength. The reported polarizer is also highly fabrication tolerant and offers peak extinction ratio selection at different wavelengths by choosing different doping concentrations during fabrication.

2. Theoretical modeling of p-silicon and device design

The highly doped p-silicon is assumed to be doped with boron with a resulting carrier concentration in the range of 10^{20} to 10^{21} cm^{-3}. Active carrier concentration of 1.08×10^{21} cm^{-3} had been demonstrated experimentally in the past by Linaschke et al. [34]. The empirical relations on the variation of the refractive index of the doped silicon provided by Soref et al. [35] are applicable in the case of low doping concentrations. Nevertheless, the complex relative permittivity of the highly doped p-silicon at telecom wavelengths can be modeled using the Lorentz-Drude model [36],

$$\varepsilon(\omega) = \varepsilon_\infty - \frac{\omega_p^2}{\omega^2 \left(1 + i\frac{1}{\omega\tau}\right)} = \left(\varepsilon_\infty - \frac{\omega_p^2 \tau^2}{1 + \omega^2\tau^2}\right) + i\frac{\omega_p^2 \tau}{\omega(1 + \omega^2\tau^2)} \tag{1}$$

where, ω_p is the plasma frequency, ε_∞ is the infinite frequency relative permittivity, τ is the electron/hole relaxation time, $\omega = \frac{2\pi c}{\lambda}$ is the angular frequency, c is the speed of light in vacuum and i is the imaginary unit. In the case of the highly doped degenerate intrinsic semiconductors, $\omega_p^2 = \frac{Ne^2}{\varepsilon_0 m_{eff}}$ and $\tau = \frac{\mu m_{eff}}{e}$; where, N is the free carrier concentration, μ is the electron/hole's drift mobility and m_{eff} is the averaged electron/hole effective mass. Usually, the angular frequency $\omega \gg \omega_p$ and $\omega\tau \gg 1$ [37]. Thus, equation 1 can be expressed as following,

$$\varepsilon(\omega) = \left(\varepsilon_\infty - \frac{\sigma}{\omega^2\varepsilon_0\tau}\right) + i\frac{\sigma}{\omega^3\tau^2\varepsilon_0} \tag{2}$$

where, $\sigma \approx eN\mu$ is the conductivity of the doped silicon and e is the charge of an electron and ε_0 is the free space permittivity. The dielectric-like property of highly doped p-silicon is decreased due to high carrier concentration and the infinite frequency relative permittivity, ε_∞ approaches 1. The real and the imaginary parts of the complex relative permittivity of the p-silicon as a function of the carrier concentration at 1550 nm wavelength are shown in Fig. 1(a). Here, $\mu = 50$ $cm^2/(V.s)$ and $m_{eff} \approx m_0$, where, m_0 is the mass of the electron [37]. The real part of the permittivity becomes negative when the carrier concentration goes beyond $4.55 \times 10^{20} cm^{-3}$. Therefore, p-silicon behaves like a metal after this carrier concentration. The real and the imaginary parts of the permittivity as a function of the wavelength for different carrier concentrations are shown as well in Figs. 1(b) and 1(c), respectively. A small linear wavelength dependence can be observed.
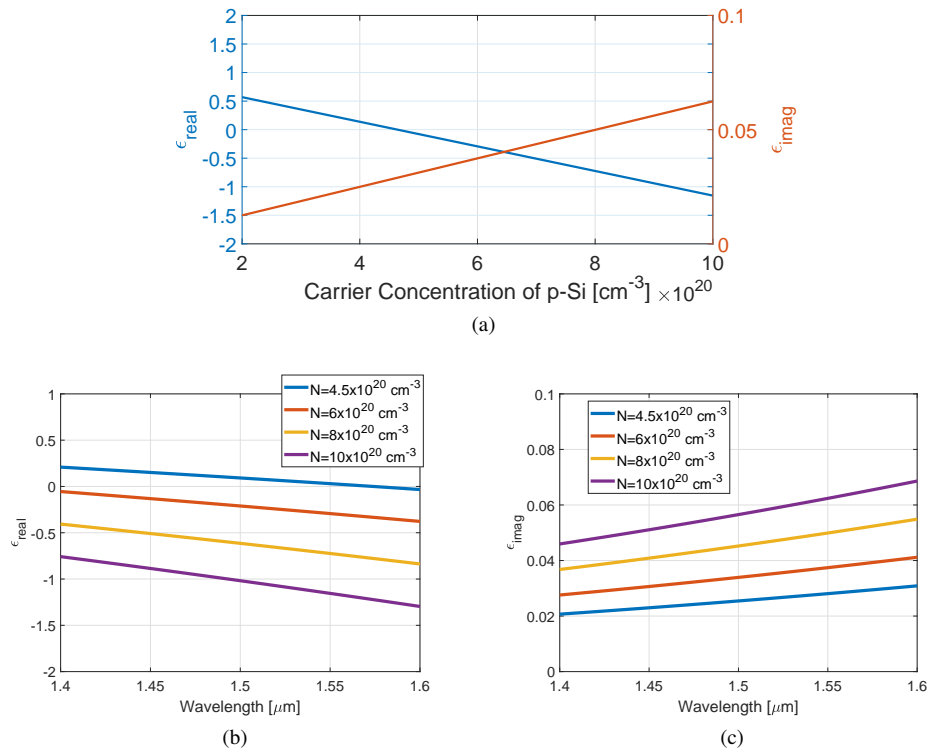
Fig. 1. (a) Real and imaginary parts of the complex permittivity of the highly doped p-silicon as a function of the carrier concentrations at 1.55 μm wavelength, (b) real and (c) imaginary parts of the complex permittivity of the highly doped p-silicon as a function of the wavelength for different carrier concentrations.

In hybrid plasmonic based polarizers (both TE- and TM-pass) the metals are used to support the hybrid plasmonic mode and act as absorbers to attenuate the undesired mode [24]. In principal, the metals can absorb both TE and TM modes depending on which mode is coupled to the metallic waveguide. The geometry of the waveguides determines which mode is coupled to the metallic waveguide and which mode passes through the dielectric waveguide with minimum interference from the metallic waveguide.

The schematic and the cross-section of the proposed TM-pass polarizer are presented in Figs. 2(a) and 2(b), respectively. The polarizer consists of a silicon waveguide and a highly doped silicon waveguide which behaves like a metal. The upper cladding layer is made of silica. The highly doped p-silicon waveguide is the key part of the device which is placed by the side of the silicon waveguide with a certain gap to suppress the TE mode significantly through absorption and let the TM mode pass with minimum attenuation. The silicon waveguide has a width of W_{Si} and the p-silicon waveguide has a width of W_{p-Si} and a length of L_{p-Si}. As mentioned before, the device is designed for the SOI platform with a silicon layer thickness, h = 340 nm. The refractive indices of silicon and silica have been obtained from [38] and for the highly doped p-silicon we utilized the Lorentz-Drude model to obtain the refractive indices as shown in Fig. 1.

3. Results and discussion

The TM-pass polarizer has been analyzed first by varying the different design parameters such as the carrier concentration, the L_{p-Si}, the W_{p-Si}, the W_{Si} and the gap between the two waveguides. All the simulations have been performed using a three-dimensional finite-difference time-domain
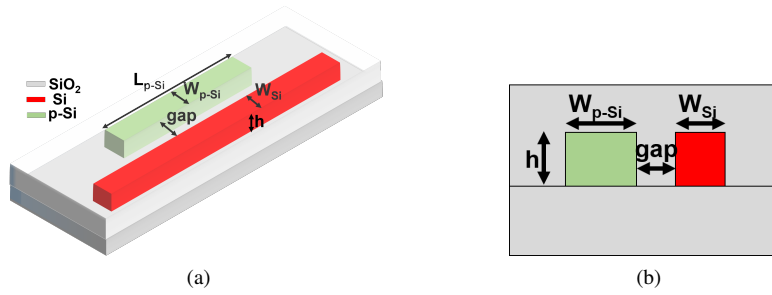
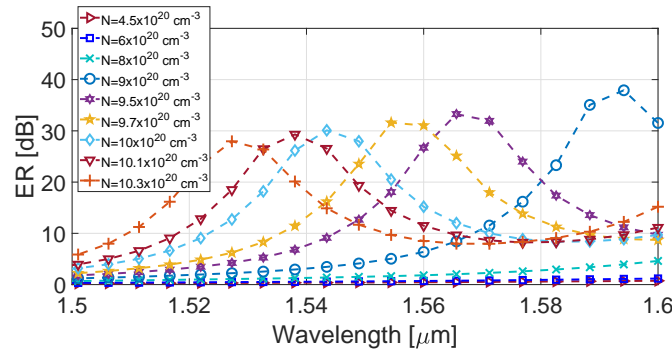Fig. 2. (a) Schematic and (b) cross-section of the proposed TM-pass polarizer.

Fig. 3. Extinction ratio (defined in equation. (3)) as a function of the wavelength for different carrier concentrations with L_{p-Si} =15 μm, W_{p-Si} = 600 nm, W_{Si} = 260 nm and gap = 200 nm.

(FDTD) based solver from Lumerical [39]. The mode source [40] with a Gaussian envelope and a wavelength span of 1.5 μm to 1.6 μm was pumped in the device.

The effect of changing the carrier concentration of the highly-doped p-silicon on the spectral response of the TM-pass polarizer is presented in Fig. 3. It can be observed that the extinction ratio peak exhibits a blue shift as the carrier concentration is increased. As shown earlier in Fig. 1, the real and the imaginary parts of the complex relative permittivity changes with the variation of the carrier concentration. The zero-crossing wavelength for the real part of the complex relative permittivity shifts towards smaller wavelengths with the increase of the carrier concentration. Since the absorption of the p-silicon is wavelength dependent and it depends on both the real and the imaginary parts of the complex relative permittivity, the peak changes as the carrier concentration is varied. This enables the selection of the extinction ratio peak through the variation of the carrier concentration during fabrication. Our target wavelength of operation for the TM-pass polarizer is the C-band (1.530 μm to 1.565 μm). Thus we chose a carrier concentration for which the extinction ratio is maximized in the C-band. For a carrier concentration of 9×10^{20} cm^{-3}, the maximum extinction ratio is 37.91 dB which occurs at 1.595 μm wavelength which is far beyond the C-band. Therefore, we chose a carrier concentration of 10×10^{20} cm^{-3} for which the extinction ratio is maximum in the C-band (near 1.545 μm).

The two most important features that a polarizer should have are high extinction ratio and low insertion loss and their definitions can be expressed as,

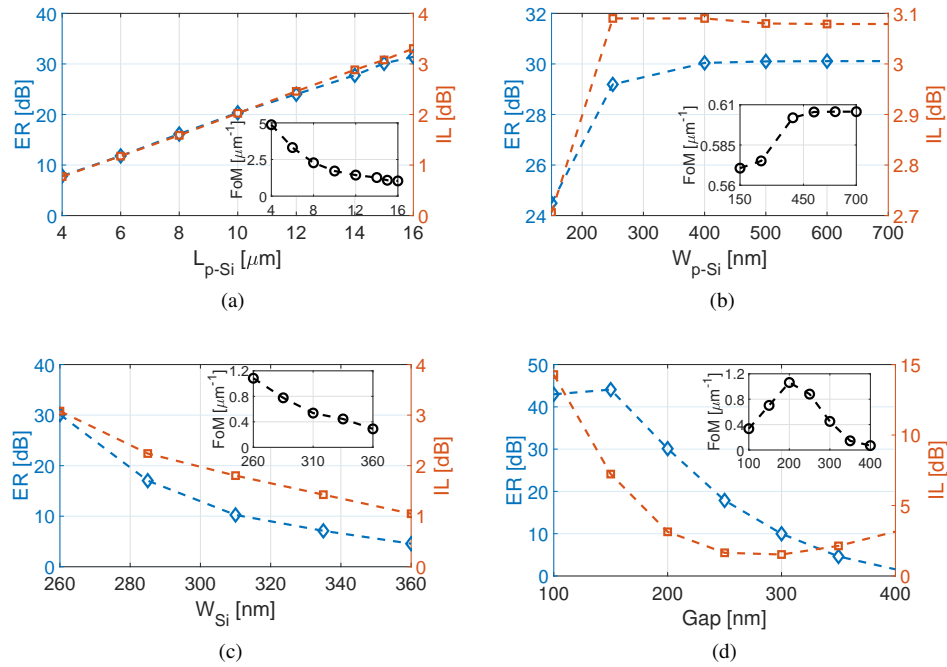$$ER = 10\log_{10}\frac{P_{TM}^{output}}{P_{TE}^{output}} \qquad (3)$$

Fig. 4. Variation of the extinction ratio, insertion loss and figure of merit as a function of (a) the L_{p-Si} for W_{p-Si} = 600 nm, W_{Si} = 260 nm, gap = 200 nm and $N = 10\times10^{20}$ cm^{-3}, (b) the W_{p-Si} for L_{p-Si} = 15 μm, W_{Si} = 260 nm, gap = 200 nm and $N = 10\times10^{20}$ cm^{-3}, (c) the W_{Si} for L_{p-Si} = 15 μm, W_{p-Si} = 600 nm, gap = 200 nm and $N = 10\times10^{20}$ cm^{-3}, and (d) the gap between the waveguides for L_{p-Si} = 15 μm, W_{p-Si} = 600 nm, W_{Si} = 260 nm and $N = 10\times10^{20}$ cm^{-3}. Figure of merits are shown in the inset of each figure.

where, P_{TM}^{output} is the output power of the TM mode at the end of the silicon waveguide and P_{TE}^{output} is the output power of the TE mode at the end of the silicon waveguide.

$$IL = 10\log_{10}\frac{P_{TM}^{output}}{P_{TM}^{input}} \qquad (4)$$

where, P_{TM}^{input} is the power of the TM mode at the input of the silicon waveguide.

The length of the polarizer should be small too to ensure its integrability. We have derived a figure of merit (FoM) based on these three parameters to optimize the design parameters of the proposed TM-pass polarizer.

$$FOM = \frac{ER}{IL \times L} \qquad (5)$$

Figure 4(a) presents the variation of the extinction ratio and the insertion loss as a function of the L_{p-Si}. As we increase the length of the p-silicon waveguide, both the extinction ratio and the insertion loss increase. The figure of merit is also presented in the inset of the figure. The design target is to obtain an extinction ratio greater than 20 dB [41] which is achieved for $L_{p-Si} > 10$ μm. For our device, we choose the L_{p-Si} = 15 μm for which an extinction ratio of 30.11 dB and an insertion loss of 3.08 dB are observed. Although the figure of merit decreases with the increasing L_{p-Si}, it exhibits a saturation tendency at larger values of the L_{p-Si}. Since our target is to maximize the extinction ratio and minimize the device footprint and the insertion loss, we did
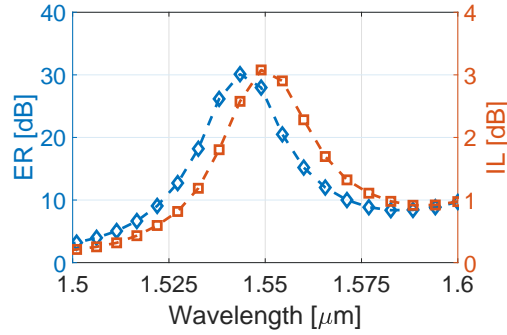
Fig. 5. Extinction ratio and insertion loss as a function of the wavelength of the reported TM-pass polarizer for L_{p-Si} =15 μm, W_{p-Si} = 600 nm, W_{Si} = 260 nm, gap = 200 nm and $N = 10 \times 10^{20}$ cm^{-3}.

not consider L_{p-Si} larger than 15 μm since the insertion loss and footprint go up if we do so. The effects of changing the W_{p-Si} on the extinction ratio and the insertion of the polarizer are shown in Fig. 4(b). The extinction ratio and the insertion loss increase with the increasing W_{p-Si}. Since our goal is to design a CMOS compatible polarizer, the minimum W_{p-Si} is chosen to be 150 nm, which is larger than the minimum feature size of the CMOS foundries [42]. As we increase the W_{p-Si}, the figure of merit increases and saturates around W_{p-Si} = 600 nm. Therefore, we choose the W_{p-Si} to be 600 nm.

In [43], a detail analysis is provided on the modal characteristics of silicon waveguides for different heights and widths in the C-band. It is observed that for a height of 340 nm, the width of the silicon waveguide needs to be between ~260 nm and ~360 nm to maintain the single mode condition for both the TE and the TM modes. Thus, we vary the W_{Si} from 260 nm to 360 nm. Both the extinction ratio and insertion loss are decreased with increasing W_{Si} and the best figure of merit is obtained for a width of 260 nm. For a thinner waveguide, the TE mode is less confined within the waveguide and hence it gets more attenuated (due to absorption) resulting in a higher extinction ratio of the polarizer.

The variation of the extinction ratio and the insertion loss as a function of the gap between the p-silicon and the silicon waveguides is presented in Fig. 4(d). The gap is varied from 100 nm to 400 nm. The extinction ratio and the insertion loss decrease with the increase of the gap; however, the insertion loss start to increase when the gap increases beyond 300 nm. From the inset figure, it can be observed that the highest figure of merit is obtained for a gap of 200 nm.

The wavelength dependence of the extinction ratio and the insertion loss is shown in Fig. 5. With L_{p-Si} = 15 μm, W_{p-Si} = 600 nm, W_{Si} = 260 nm, gap = 200 nm and carrier concentration of 10×10^{20} cm^{-3}, an extinction ratio of 30.11 dB and an insertion loss of 3.08 dB have been obtained. The bandwidths over which the TM-pass polarizer maintains 20 dB and 10 dB extinction ratios are 21.05 nm and 48 nm, respectively.

The evolution of the TE and the TM modes at different points of the polarizer are shown in Fig. 6(a). The amplitudes of the electric field profiles throughout the polarizer are shown as well in Fig. 6(b) for both the TE and the TM modes. It can be observed that the TM mode passes through the polarizer with insignificant attenuation while the TE mode is attenuated significantly.

4. Fabrication techniques and tolerance analysis

The proposed TM-pass polarizer can be fabricated on a SOI wafer with a 340 nm thick silicon core. The devices can be patterned using both electron beam and 193 nm DUV lithography process and the reactive ion etching technique can be used to form the waveguides. Finally, the
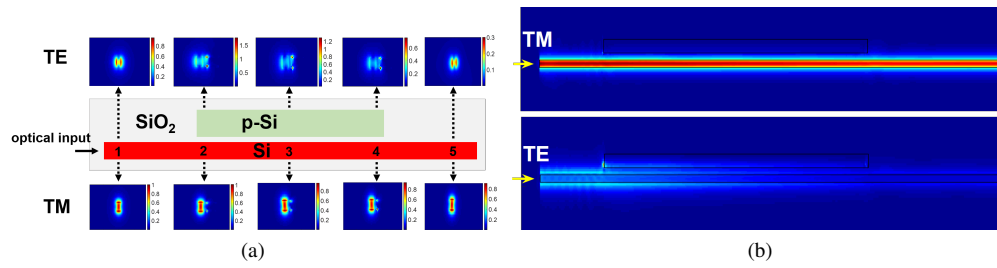
Fig. 6. (a) Schematic showing the mode profiles at different points along the TM-pass polarizer, (b) TM and TE mode propagation through the polarizer. (Electric fields are plotted in both the figures.)

silicon waveguide can be doped with boron using the ion implantation method and a layer of silica can be deposited over the silicon layer as the cladding. The 200 mm SOI wafers used in multi-project wafer (MPW) runs offer a silicon layer thickness non-uniformity with a 3σ of ±6 nm [44]. However, for 300 mm wafers a non-uniformity with a 3σ of ±1 nm [45] has been achieved. In 193 nm DUV lithography process, the linewidth uniformity is controlled with a 3σ of ±8 nm [26, 46], although a size deviation of up to ±10 nm can be found very often [26]. These variations during the fabrication process causes performance variations of the device. Thus, analyzing the tolerance to the key design parameters of the device is necessary. Figure 7 presents the effects of varying the h, the W_{p-Si}, the W_{Si} and the gap between the waveguides on the extinction ratio and the insertion loss of the device. We varied the height by ±6 nm and the other parameters by ±10 nm in order to analyze the fabrication tolerance of the proposed device. It can be observed from Fig. 7 that the extinction ratio and the insertion loss are almost constant with the variation of the h and the W_{p-Si}. When the W_{Si} is increased by 10 nm, the extinction ratio and the insertion loss are almost constant; however, when the W_{p-Si} is decreased by 10 nm, the extinction ratio is increased by 27.8 dB while the insertion loss is increased by 1.62 dB. As mentioned before, for a height of 340 nm, the silicon waveguide will maintain the single mode condition for both the TE and the TM modes for a width between 260 nm and 360 nm. When the width is less than 260 nm, the waveguide maintains single mode condition for the TM mode but enters the cut-off regime for the TE mode. In case of the 250 nm width of the silicon waveguide, the waveguide is almost on the edge of cut-off regime and the TE mode is less confined in the dielectric waveguide. As a result, the TE mode gets easily absorbed by the p-silicon waveguide. Thus, the sudden jump in extinction ratio occurs when we reduce the W_{Si} to 250 nm while insertion loss exhibit insignificant increase in comparison to the extinction ratio. It should be noted that such high extinction ratio cannot be achieved by only reducing the silicon waveguide width to 250 nm and entering the edge of the cut-off regime. It is the combined effect of both the p-silicon waveguide that absorbs the TE mode and the thinner silicon waveguide that enables the easier absorption. The extinction ratios are increased by 7.8 dB and 14 dB when we change the gap by -10 nm and +10 nm, respectively. The insertion losses increase as well for both the cases.

Table 1 compares our reported TM-pass polarizer with the state-of-the-art. Although Yuan et al. [50] and Hu et al. [19] reported TM-pass polarizers with 45 dB and 40 dB extinction ratio, respectively, their designs are not compatible with the CMOS process. Among the CMOS compatible designs shown in table 1, our TM-pass polarizer has the highest extinction ratio. The polarizer demonstrated by Kim et al. [47] has similar extinction ratio as ours, but their design is based on photonic crystals with sub-wavelength structures which is very challenging to fabricate using the 193 nm DUV lithography process. Our design is based on a regular silicon
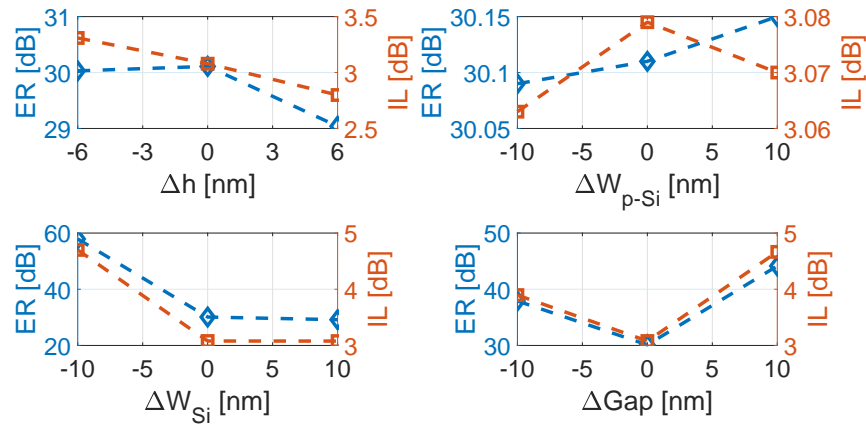
Fig. 7. Fabrication tolerance analysis of the proposed TM-pass polarizer .

Table 1. **Comparison with other TM-pass polarizers. ER = Extinction Ratio and IL = Insertion Loss.**

	ER [dB]	IL [dB]	Length [μm]	CMOS Compatibility
This work	30.11	3.08	15	Yes
Bai et al. [25]	25	0.088	2.5	No
Hu et al. [19]	40	3	150	No
Kim et al. [47]	30	1	4	Yes
Sanchez et al. [20]	15	3	1	No
Azzam et al. [48]	20	0.15	1.31	Yes
Azzam et al. [49]	20	1	2.84	Yes
Yuan et al. [50]	45	1	7.5	No
Ng et al. [12]	11.5	not mentioned	0.1	Yes
Guan et al. [15]	15.2	0.84	3.9	No
Guan et al. [11]	27	0.5	9	Yes

waveguide and a highly-doped p-silicon waveguide, and has feature sizes well above the minimum size required for the 193 nm DUV process. Therefore, the proposed design offers both good performance and relaxed fabrication tolerance.

5. Conclusions

We present a TM-pass polarizer with an extinction ratio of 30.11 dB, an insertion loss of 3.08 and a length of 15 μm. The proposed TM-pass polarizer has the highest extinction ratio among the DUV compatible designs to the best of our knowledge and offer better fabrication tolerances by incorporating feature sizes above the minimum required size for the fabrication process.

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