Electronically Reconfigurable Wideband High-Power Amplifier Architecture for Modern RF Systems (LMBA)

Thesis submitted in partial fulfilment of the requirements for the degree of

Doctor of Philosophy

by

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Electronically Reconfigurable Wideband High-power Amplifiers

Introduction of and surrounding work related to the development of the Load Modulated Balanced Amplifier (LMBA) architecture.

Abstract

As mobile communications and other microwave systems continue to evolve designers and system architects are pushing for ever increasing bandwidth as multiple RF systems are increasingly sharing a common front-end amplifier to save space and reduce routing complexity and losses associated with having separate amplifier systems.

The power amplifier in many RF systems typically accounts for the majority of the power consumption of the device or transmitter platform, it is therefore paramount that to improve the efficiency of these systems RFPA designs must be tailored to achieve the highest possible efficiency.

RFPA modes of operation and architectures to achieve higher efficiency have been developed, but often come with compromises to other system aspects such as linearity, control complexity and most commonly bandwidth.

With the next generation 5G communications specification including frequency bands of up to the Ka frequency spectrum and the high capacity multi-octave spectrum bands allocated at L-C band, traditional RFPA efficiency enhancement techniques struggle to be implementable due to either the high frequency requirements of the control systems needed or due to the bandwidth restrictions of such techniques.

Conventionally narrow bandwidth X-band radar systems that used to be operated at saturated output power conditions are starting to explore multimode operation that require more power back-off (PBO) and control of the RFPA, so are searching for techniques that are applicable at X-band and can achieve the same level of PBO requirements demanded by modern communication modulation standards while working to the power and cooling restraints that come from a limited application platform such as fighter aircraft.

Similarly, such fighter platforms are demanding increased electronic warfare (EW) capability which are restrained to the same platform limitations but often need to cover multi-octave bandwidths where traditional efficiency enhancement techniques cannot be applied.

This research will focus on wideband efficiency enhancement for both saturated and PBO scenarios that present a frequency agnostic technique of overcoming conventional limitations.

The novel work presented is based around the quintessential, but relatively old, bandwidth extension architecture known as the balanced amplifier. The addition of a secondary control signal has been proposed whereby the operating impedance of the amplifier can be dramatically modulated while maintaining the fundamental advantage the balanced amplifier allow, that is multi-octave bandwidth.

The power of this architecture can draw similarities in impedance control afforded by load pull systems, in particular active load-pull. With the correct control signal, any impedance is able to be presented to the transistors to keep them operating at maximum efficiency, where passive matching alone is not able to achieve such efficiency due to fundamental matching theory.

Due to the active element of this novel architecture, named the Load Modulated Balanced Amplifier (LMBA), frequency restrictive and thus band limiting elements present in other efficiency enhancement techniques; such as the quarter wave inverter present in the Doherty Amplifier or the difficulty of realizing the modulator in Envelope Tracking (ET) are not present.

This thesis will present the fundamental theory driving the operation of an LMBA along with multiple implementations, each targeted at differing applications and different frequency bands to demonstrate the versatility and frequency independence of the technique.

Publications

Directly related to this work

Appendix 1 - The original paper published on the LMBA technique first presents the concept and equations that drive LMBA operation. This paper received the Tatsuo Itoh Award at IMS 2018 which recognises the most impactful and novel paper sumbitted to the Microwave and Wireless Components Letters Journel in the year 2016.

D. J. Shepphard, J. Powell and S. C. Cripps, "An Efficient Broadband Reconfigurable Power Amplifier Using Active Load Modulation," *IEEE Microwave and Wireless Components Letters,* vol. 26, no. 6, pp. 443-445, 2016.

Appendix 2 - D. J. Shepphard, J. R. Powell and S. C. Cripps, "A Broadband Reconfigurable Load Modulated Balanced Amplifier," *IEEE MTT-S International Microwave Symposium (IMS),* pp. 947-949, 2017.

Appendix 3 - J. R. Powell, D. J. Shepphard, R. Quaglia and S. C. Cripps, "A Reconfigurable High-Efficiency X-Band Power Amplifier MMIC Using the Load Modulated Balanced Ampifier Technique," *IEEE Microwave and Wireless Components Letters,* vol. 28, no. 6, pp. 527-529, 2018.

Indirectly related work

D. J. Shepphard, S. C. Cripps and J. R. Powell, "High Efficiency GaN 2.5 to 9 GHz Power Amplifiers Realized in Multilayer LCP Hybrid Technology," *EEE Microwave and Wireless Components Letters,* vol. 26, no. 6, pp. 440-442, June 2016.

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To my parents, for the love and support throughout my academic career. Providing encouragement and comfort along with an environment in which to develop a healthy appetite for curiosity and engineering drive.

Last, but by no means least, to my teachers and lecturers for their impeccable knowledge and ability to impart knowledge, with particular thanks to those at Cardiff University's Centre for High Frequency Engineering.

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Abbreviations

BA	Balanced Amplifier
COTS	Commercial Of The Shelf
CS	Control Signal
CSP	Control Signal Power
DC	Direct Current
DPD	Digital Pre-Distortion
DUT	Device Under Test
ET	Envelope Tracking
EW	Electronic Warfare
FET	Field Effect Transistor
FBW	Fractional Bandwidth
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Gbps	Gigabits per second
LMBA	Load Modulated Balanced Amplifier
MEM	Micro Electro-mechanical
MIMO	Multiple Input Multiple Output
MMIC	Monolithic Microwave Integrated Circuit
Octave+	Beyond octave bandwidth
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PBO	Power Back-off
PDK	Process Development Kit
RFPA	Radio Frequency Power Amplifier
SiC	Silicon Carbide
SoC	System on a Chip

Chapter 1 – Research Perspective

1.1 - Introduction

The focus of this thesis will be on the introduction of the Load Modulated Balanced Amplifier (LMBA); presenting simulated and measured results showing the frequency agnostic application of this architecture, exploring what the limiting aspects of an LMBA design are and the modes of operation for which the LMBA architectures can be employed and optimised for.

This thesis will present the problems that this work attempts to overcome along with evaluating the short falls of historic architectures and techniques that are currently used in commercial and state of the art research amplifiers that attempt to cover the same set of problems.

Two well-known amplifier architectures that use active load modulation are the Doherty and Chireix outphasing amplifiers. Both active modulation methods attempt to solve the problem of diminishing efficiency when the RF drive power is reduced to an amplifier, a standard procedure employed in modern telecommunication systems for a variety of modulation schemes. This problem will become worse as telecom systems push for higher data rates which require higher bit count modulation schemes which in turn will call for higher peak-to-average power ratios (PAPR) along with increases in spectral

bandwidth and frequency. Both methods have shown significant increases in power back off (PBO) applications with high PAPR applications but neither have shown that they can maintain the same level of high efficiency operation when bandwidth requirements calling for greater than an octave. Similarly, the application of these architectures become increasingly harder to implement over wide bandwidths when frequencies exceed 6GHz due either to the increased difficulty of achieving the required passive network match in the case of the Doherty amplifier or the increased complexity introduced into the control system required to implement a Chireix outphasing amplifier.

With the LMBA modulation method it is theoretically possible to electronically reconfigure a balanced amplifier's transistors to be presented with any required load so that the load impedance can be optimised to increase their output power and efficiency performance under any level of RF drive signal and DC bias condition. Much like the well-known method of characterising an RF transistor though passive loadpull techniques or more recently active loadpull techniques, the LMBA is able to pull the impedance of the transistor around the smith chart. As the LMBA is an amplifier rather than a characterisation system there will be practical limitations to the load modulation range the LMBA can achieve while considering the impact of overall system PAE.

1.2 – Applications Driving Broader Bandwidths

Small form factor consumer electronics paired with increasing demand for high data rate communication, and functionality from increasingly mobile platforms, are pushing designers to integrate more functionality into devices. Improvements in microelectronic assembly and co-simulation tools for complex RF integrated PCB designs have enabled PCB area reductions while integrating the increased functionality. Although standardised, multiple modulation methods over different carrier frequencies are having to be incorporated leading to the adoption of multiple power amplifiers being present in a single 'system on a chip' (SoC) to handle the different modulation methods as efficiently as possible. This has been an effective solution for accommodating historic modulation methods that are typically narrowband since the data rate requirement for these modulation standards are now considered relatively low in the face of current LTE and the proposed 5G modulation standard.

To accommodate the higher bit rate requirement of modern communication standards Nyquist's theorem relating data rate to bandwidth and data constellation states still applies. Increasing the number of constellation states would demand higher PAPR from the systems' amplifiers, alternatively increasing the spectrum bandwidth would yield a greater data transmission rate but also decrease the efficiency of the amplifier design due to compromises made to the impedance match to accommodate the bandwidth.

1.3 – LTE Spectrum and Beyond: Entering the Ka Spectrum

Future generations of LTE and 5G communication have been allocated and agreed internationally for global harmonisation with three band classification used; sub 1GHz for wide area and deep indoor coverage, 1-6GHz for high capacity and coverage which encompasses the current 4G spectrum and lastly the >6GHz classification for high speed line of sight/surface penetrating high speed data links.

To provide the muti-gigabit per second (Gbps) links that the 5G standard aims to achieve the >6GHz band will be critical. With the frequency spectrum below 6GHz already crowded, mobile carriers are currently limited to providing only 10's of MHz of bandwidth for their data links, which without increasing modulation complexity limits the throughput available on their data links. In Europe the 26GHz band, as it is known, will span from 24.25-27.5GHz offering a comparatively massive bandwidth of 2.25GHz that carriers will be able to use. It is unclear how this bandwidth will be divided right now but this opens up the opportunities for 100's of MHz of bandwidth per channel which will greatly increase the throughput achievable.

Moving communication to Ka band imposes new challenges particularly as RF semiconductor technology at this band is somewhat immature. Conventional GaAs foundries that produce chips for S and C band have improved their process capability to offer 0.1μm gate widths on their processes which allow for reasonable performance to be achieved at Ka band

but there are still many shortfalls in the desired performance that has come to be expected such as high available gain and great PAE.

Atmospheric absorption and reflections from buildings are also a lot greater at Ka frequencies which requires transmitters and receivers to either produce more power or to be equipped with highly directional antennas. System PAE becomes an even greater factor when considering the approaches that have been put forward for 5G network coverage. There has been a lot of research focus on medium power multiple input multiple output (MIMO) phased array transceivers for Ka band distributed wireless communications for micro base stations. With these basestations requiring 5-50W of RF transmit power, the limited range will call for a lot of these stations where efficiency improvements need to be made to make 5G systems economically competitive.

While the focus of this thesis will not be on modulated comms measurements or any considerations towards optimising for a particular modulation scheme, the work presented will cover the fundamentals of an active impedance modulation method that is flexible enough to be adapted and optimised through future research to be more applicable to 5G comms applications. The LMBA load impedance modulation method aims to solve the bandwidth limitations of the conventional Doherty amplifier while retaining the same functionality, if desired, along with providing a platform for system designers to manipulate and optimise.

1.4 – Conventional Amplifier Design

Conventional linear power amplifier design relies on measured load-pull data of a transistor, from which a designer could utilise the data to design passive matching networks that present the transistor with the optimal load impedance match for power, efficiency or noise figure. Historically these measurements were taken with precision mechanical tuners that loaded the transistor with known impedances at which the response of the transistor was measured and recorded. Data would then be compiled to produce contours on a smith chart showing the optimal match for each parameter. Loadpull systems have evolved from the manual slide rules and slotted line tuners of the past, in favour of electronically controlled passive tuners that are capable of producing loadpull data in as little as hours, depending on the detail required, where previously manual measurement could have spanned days or even weeks where multiple frequency points of great resolution are required. A good summary of loadpull system evolution can be found at [1].

Modern systems using open-loop active loadpull, whereby mechanical load tuners have been replaced with a secondary signal source, enable even faster measurement as all mechanical moving parts are replaced with electronically generated signals which can resolve to impedance conversion in a few milliseconds through iterative measurement. Utilising a low-loss coupler and vector network analyser (VNA), the b2 wave generated by the transistor under measurement can be analysed, so that a corresponding a2 wave, with

determined amplitude and phase, can be returned to present the transistor with an apparent reflection co-efficient equivalent to that of a physical load. With the addition of multiplexors and multiple signal sources it is possible to perform multi-harmonic loadpull at arbitrary reflection coefficients beyond what would be achievable through passive matching without the use of filter banks.

High power amplifier designers are typically concerned more about efficiency and power output than noise figure; which is of utmost importance to a low-noise amplifier (LNA) designer, that typically needs to amplify a low power signal from some kind of receive circuity or antenna, introducing as little distortion as possible in order to preserve signal data integrity. Such data can be predicted from loadline principles and was first presented in 1983 [2], with an extension to the work presented recently in 2017 [3] which extends the analysis to include an knee region profile based from of a single parameter.

1.4.1 – Loadline Theory

Simple loadline analysis assumes a strongly nonlinear device model whereby the characteristic turn-on ('knee') region of a transistor is negligible and linear control of the output current generator is achieved from 0 to I_{max}, the I-V curve for such a device can be seen in Figure 1. Analysis using this method is valid only in the region of linear transconductance and is valid up to the onset of gain compression.

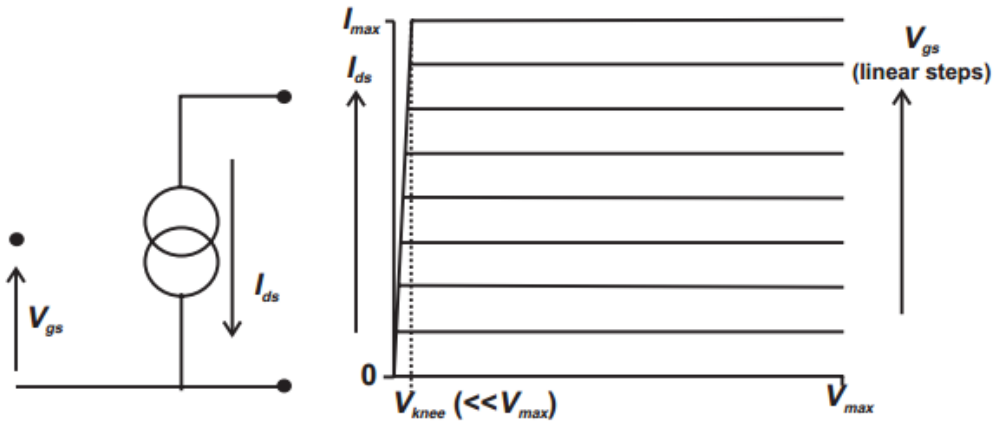


Figure 1 – Ideal, strongly non-linear transistor device I-V model where the 'knee' region is negligible. [4]

Real transistors will exhibit a non-zero turn on voltage which will cause gain compression as the RF input drive voltage swing enters the transistor linear region (where V_{ds}<V_{knee}). The linear region represents a region of non-linear transconductance and linear resistance resulting in reduced output power due to reduced output current as the RF voltage swing drives deeper into the knee region.

The optimal loading condition for a sinusoidally driven transistor producing maximum linear output power can be extracted from the I-V characteristic of Figure 1, whereby current is allowed to swing over the maximum linear range from zero to I_{max} with an amplitude of $I_{max}/2$ and the voltage swings over the maximum range of $V_{max} = 2V_{dc}$ with an amplitude of V_{dc} (figure 2) leading to the optimal power matched loadline being:

$$R_{opt} = V_{dc}/(I_{max}/2) = V_{dc}\ /I_{dc}$$

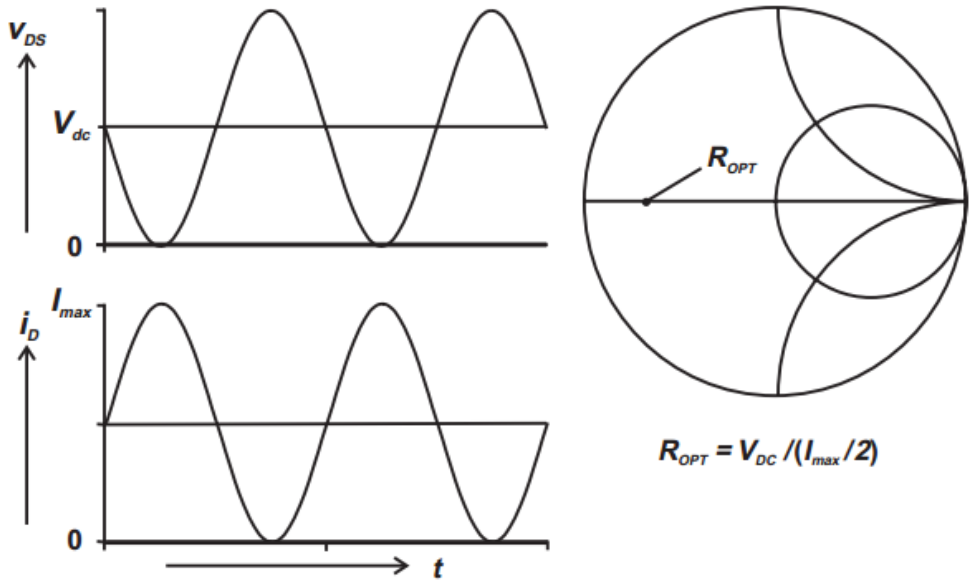


Figure 2 - Class A linear power amplifier optimal loadline waveform conditions. [4]

It is important to note that R_{opt} is calculated from the intrinsic current generator plane of a transistor device, it is assumed that all parasitic capacitances form part of the matching network therefore R_{opt} represents an entirely resistive impedance.

Figure 2 shows that an optimally matched class A amplifier will have an optimal output power of:

$$P_{opt} = \frac{1}{2} V_{dc} I_{dc}$$

As explained in [4], varying the load impedance and analysing the resulting current and voltage waveforms it is possible to draw contours of constant power output for a range of resistive and reactive load values forming contours on a smith chart as pictured in Figure 3

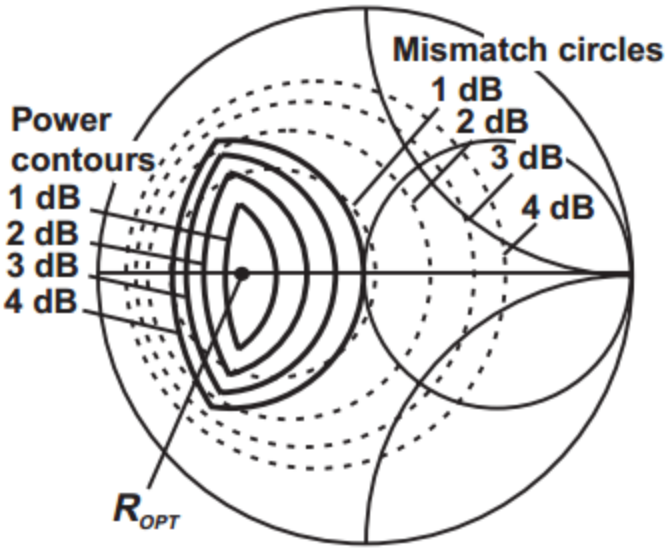


Figure 3 – Load-pull contours of an ideal Class A transistor showing power match contours (solid) expressed in dB relative to Popt at Ropt, Gain mismatch circles are plotted as dotted circles. [4]

Load-pull contours extracted from physical devices do not exhibit the sharp boundary that occurs along the contours of constant resistance and constant conductance, instead they exhibit more rounded behaviour which is not captured by the assumed ideal model used for the analysis.

The rounding of the intersections is the manifestation of knee effect in real transistor devices, therefore, to capture and model the behaviour of a device with a non-zero knee, an extension to the loadline theory has been shown in [3] to include a simplified expression for the knee characteristic which will introduce harmonic components into the current and voltage waveforms as the device enters saturation.

$$k(v_{ds}) = 1 - (1 - v_{ds})^N$$

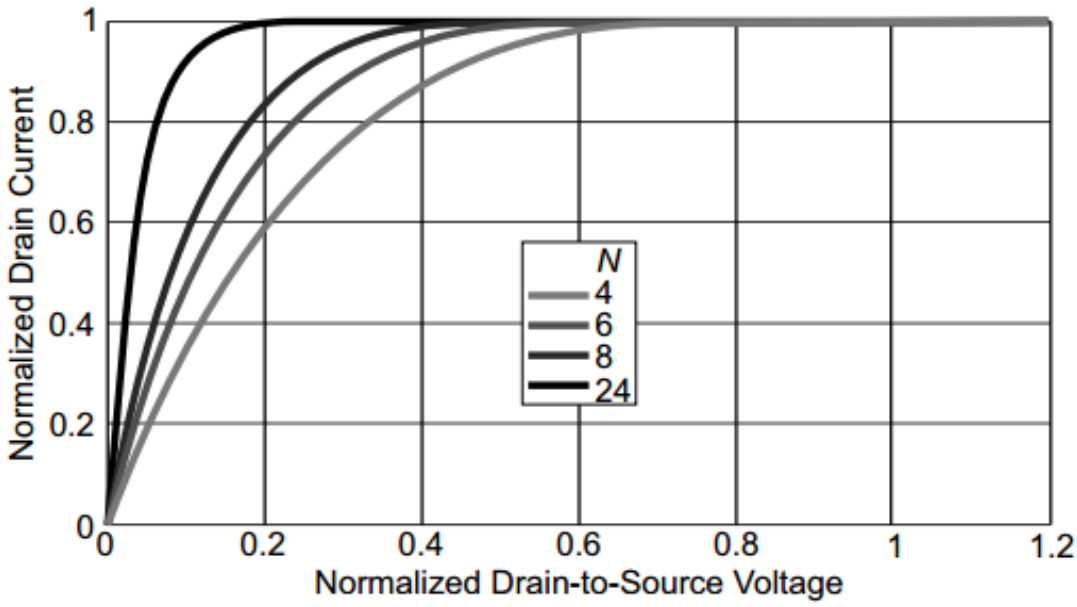


Figure 4 - Knee profile vs. vds for N = 4 (light grey), 6 (grey), 8 (dark grey), and 24 (black) [3]

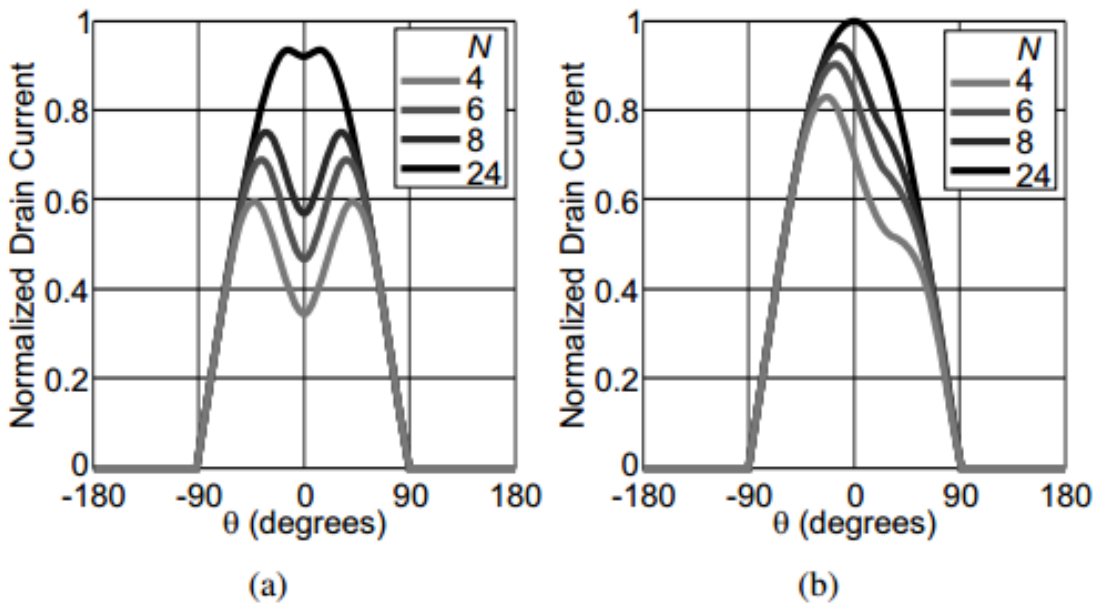


Figure 5 - Intrinsic current waveforms for N = 4 (light grey), 6 (grey), 8 (dark grey), and 24 (black). V = 0:9, φ = 0 (a), and V = 0:8, φ = − π 8 (b) [3]

By choosing an appropriate N value to approximate the knee characteristic of a particular transistor technology/process, it is possible to improve the

prediction of load-pull contours. Figure 6 shows the loadpull contours for 3 devices; 2 GaN devices and 1 GaAs device.

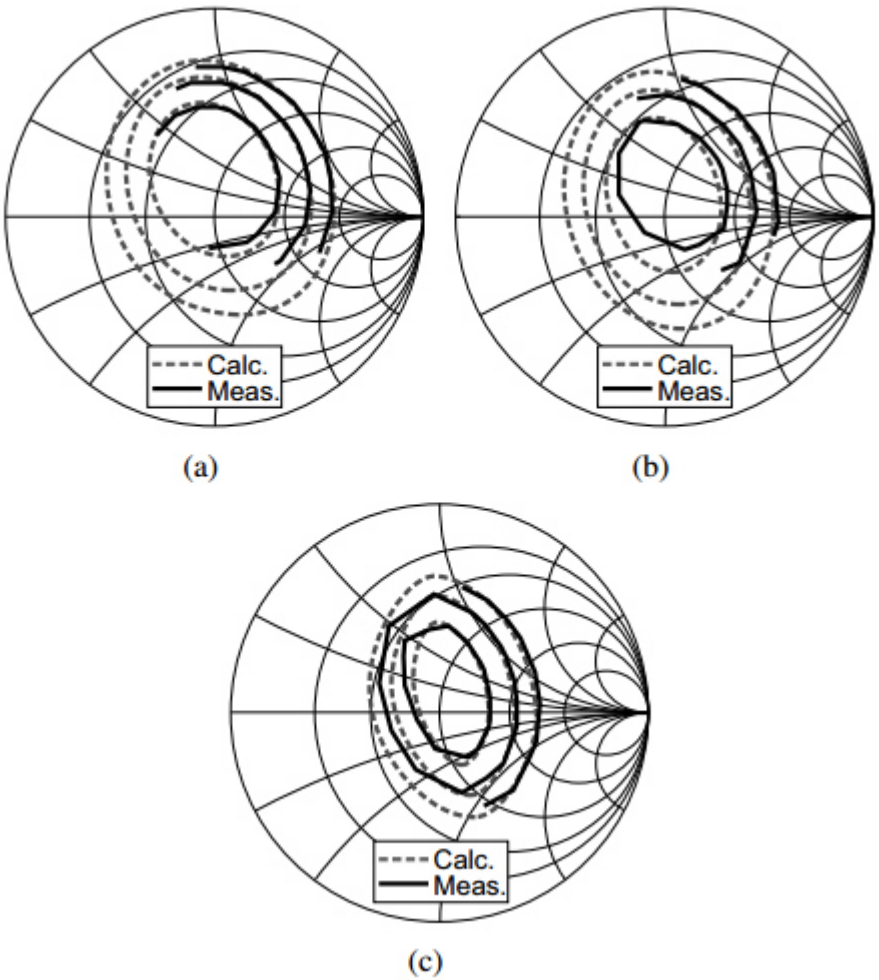


Figure 6 - Output power contours for the 3 measured devices, GaNFET1 (a), GaNFET2 (b) and GaAsFET (c) devices. Comparison between measurements (black solid) and calculated (grey dashed). Contour step: 1dB. [3]

With the load-pull contours for a given device now defined, a designer can use this information to provide a matching network whereby a range of impedances may be specified without variation in performance; given the output impedance match lies within the confines of the contour.

1.4.2 – High Efficiency Reduced Conduction Angle Modes

High efficiency reduced conduction angle modes relate to a set of amplifier modes where the operating quiescent bias point sets the angle of conduction i.e. the amount of time a waveform is conducting current in a given period. These modes are designated as A, AB, B and C whereby AB and C represent a continuum of conduction angles defined in Table 1.

A class A amplifier, as we have seen from Figure 2, conducts current over the entire period of the waveform, as such the maximum efficiency a class A amplifier can achieve is 50%. Setting the quiescent bias point such that the input signal voltage will swing the transistor into pinch-off will result in clipping the current waveform thus reducing the conduction angle (Figure 7).

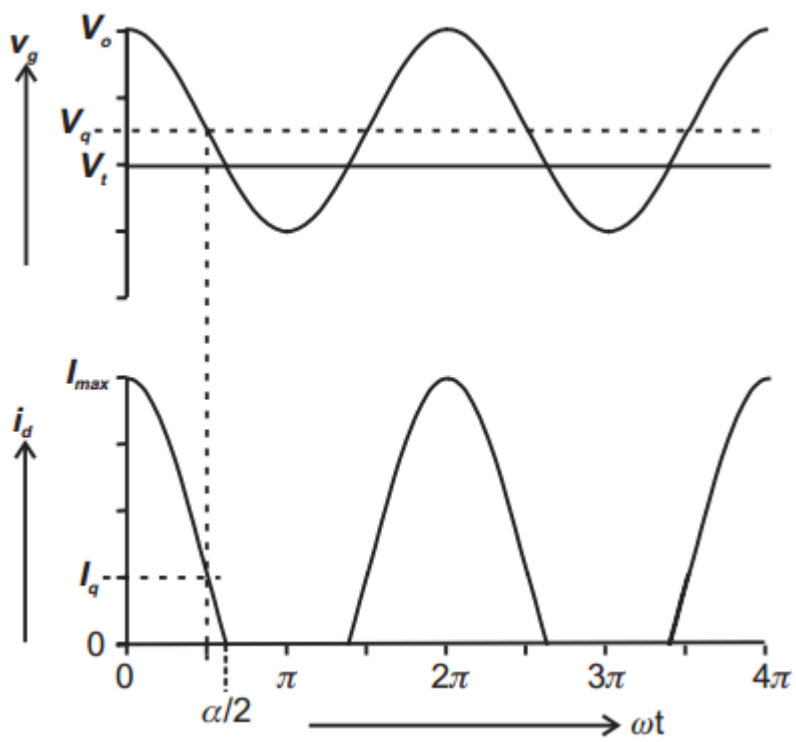


Figure 7 - Reduced conduction angle waveform [4]

The RF current as expressed by Cripps [4] for the waveform in Figure 7 can be written as:

$$i_d(\phi) = I_q + I_{pk} \cdot \cos(\phi), \qquad -\alpha/2 < \phi < \alpha/2\,;$$
$$= 0, \qquad -\pi < \phi < -\alpha/2\,;\ -\alpha/2 < \phi < \pi$$

Where $\cos(\alpha/2) = -(I_q/I_{pk})$, and $I_{pk} = I_{max} - I_q$,

So, $I_d(\phi) = \frac{I_{max}}{1-\cos(\alpha/2)} \cdot (\cos(\phi) - \cos(\alpha/2))$

The mean current is therefore given as:

$$I_{dc} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)} \cdot (\cos(\phi) - \cos(\alpha/2)).\, d\phi$$

And the magnitude of the nth harmonic is:

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1-\cos(\alpha/2)} \cdot (\cos(\phi) - \cos(\alpha/2)) \cdot \cos(n\phi)\,.\, d\phi$$

Table 1 - Classical reduced conduction angle modes.

Class	Bias Point (V_q)	Quiescent Current	Conduction Angle
A	0.5	0.5	2π
AB	0 - 0.5	0 - 0.5	π - 2π
B	0	0	π
C	< 0	0	0 - π

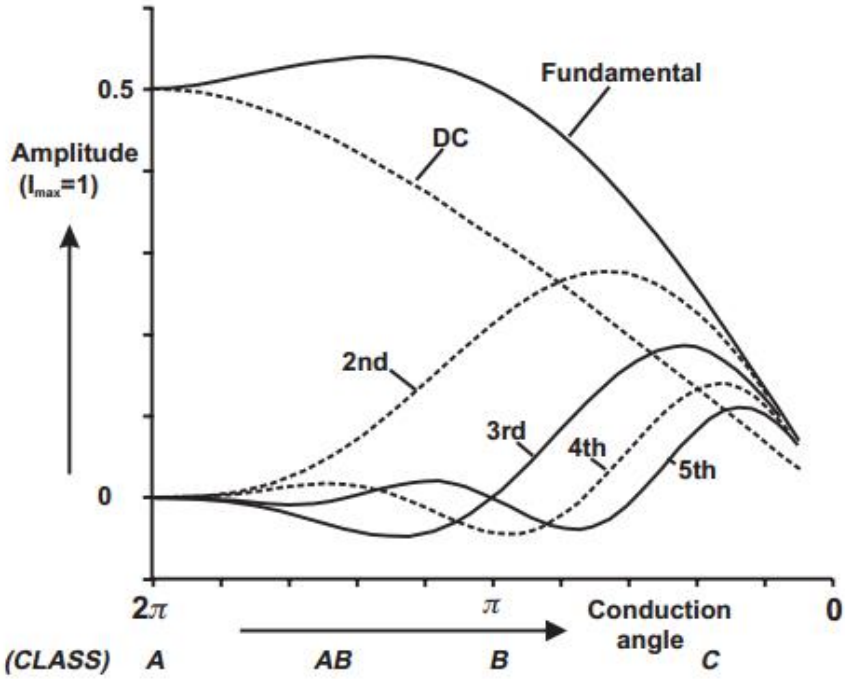


Figure 8 - Fourier analysis of reduced conduction angle waveforms up to the 5th harmonic. [4]

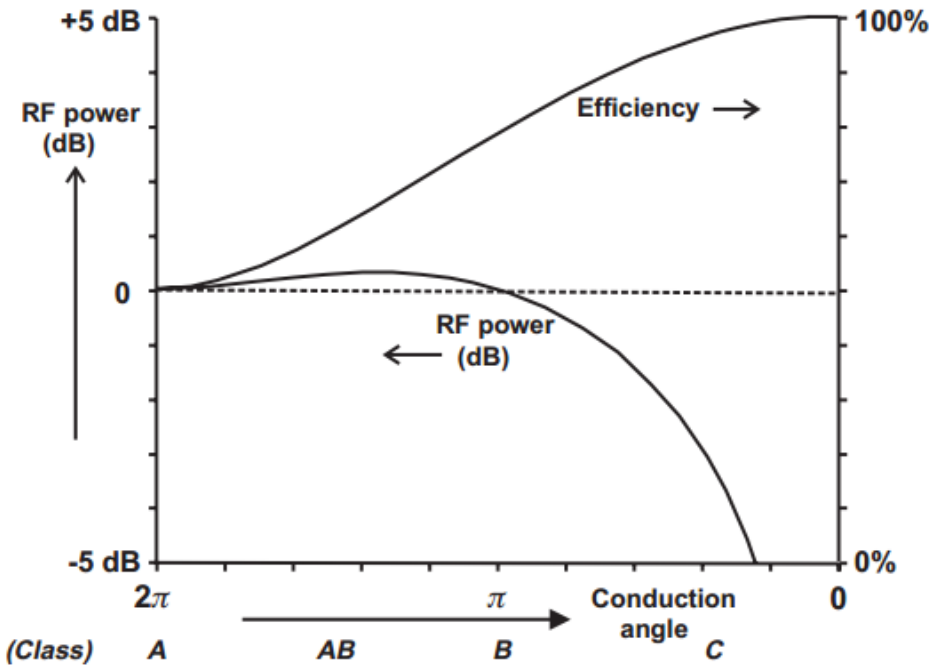


Figure 9 - RF power (relative to Class A) and efficiency as a function of conduction angle; optimum load and harmonic short assumed.

Figure 8 illustrates how the mean (DC) current component drops as conduction angle is reduced through the classes, resulting in increased efficiency. Supporting the clipped current waveforms require higher order harmonic content to be present in the current waveform resulting in increasing RF harmonic content in the output waveform. The classical analysis which Figure 8 and Figure 9 are based on assume that the fundamental is matched to R_{opt} and all harmonic frequencies are presented with a short circuit.

In practice this impedance environment will be hard to achieve with passive matching elements resulting in either a compromise of efficiency, output power and/or bandwidth.

Octave+ bandwidth amplifiers struggle to achieve the correct harmonic terminations due to harmonics being 'in band' at the lower end of the bandwidth. Class B/J theory however presents a continuum of waveform solutions through reactive harmonic tuning to achieve operation efficiency close to that of the class AB/B without the need to short circuit all harmonic components. [4] [5].

Utilising reduced conduction mode theory, adaptive matching networks allow the bandwidth of such an amplifier to be extended through load switching elements that will be addressed in the next section.

1.5 – Passive Load Switching Techniques

1.5.1 - Switched Matching Networks

Adaptive load switching can be summarised into two categories; switched matching networks and switched network elements. Both methods have advantages and drawbacks , which are outlined in Table 2 & Table 3, and both methods require some form of switching element to toggle between the two networks.

Table 2 - Pros and Cons of switching entire matching networks.

Pros	Cons
• Optimal matching networks may be formed for a given frequency or function i.e. back-off power. • Easy to design and analyse. • Simple control method.	• Large area required. • Limited granularity in network control i.e. once designed the network response is fixed.

Switches can either be electrical, mechanical or electromechanically controlled. Adaptive/reconfigurable systems that need to adapt to the signal in-situ eliminates the usability of purely mechanical toggle-based switches.

The most common electrically based switch used in RF designs is the switching Field Effect Transistor (FET) which is highly integrate able into MMIC designs.

Table 3 - Pros and Cons of switching individual matching elements.

Pros	Cons
• Granular control of impedance can be achieved in a relatively small area.	• Each element needs a control signal which may be many if individual element control is required. • Susceptible to loading effects when in off state due to non-ideal switches. Leading to complex design and analysis.

Micro Electro-Mechanical (MEM) switches on the other hand are not directly capable of being integrated into a MMIC but may be used in a hybrid fashion for chip-on-MMIC or more commonly chip-on-carrier designs.

Improvements in Micro Electro-Mechanical (MEM) switches have been made in recent years that now allows them to operate in more rugged conditions and for switching cycles exceeding $>10^{11}$. These switches offer low insertion loss and high isolation between switched paths but can require high voltage to be applied as the control which makes them complicated to integrate into traditional GaAs or even GaN amplifier designs, as it would require an additional DC supply. Switching response rate is typically in the kHz range and longevity is only achieved through cold switching (under no RF drive).

The power handling of MEM switches is also typically limited to a few watts meaning limited usability in high RF output amplifiers.

A switching FET (Field Effect Transistor) uses the gate as a control mechanism to pinch off the channel to switch the circuit in or out. One of the main disadvantages of using FET switches is the inherent loss associated with the parasitic reactance and channel resistance of the transistor. Using FETs that have not been designed as fast switching FETs may also lead to issues with time critical designs, where short pulse lengths are used and surface charge around the gate has not had time to deplete leading to switch lag. Given these disadvantages, the switched FET is still the best option for integration into a MMIC given its compact footprint and lifespan in situations where switching occurs frequently.

1.5.2 - Varactor Based Matching Networks

Varactor based adaptive modulation methods can be used independently or in conjunction with switched network designs for a more complex design. The varactor is a diode device that has a changing capacitance curve with applied voltage. This voltage may be AC or DC in nature and can be used for example to change the capacitance of a matching network under differing output drive levels, given that the RF output voltage will increase with increasing power output. Typically, a combination of both AC and DC voltage is used; the DC voltage provides an offset for the AC voltage to modulate around and by

choosing an appropriate varactor a wide range of capacitance can be achieved just by adjusting the DC offset voltage.

One drawback of varactor devices is that they are inherently non-linear and therefore produce harmonic distortion in the voltage waveform causing higher order products to be generated which can be detrimental to the fundamental output power and efficiency. Varactor diodes also have a temperature dependency that can limit the usefulness in environments with a high degree of temperature fluctuation.

Further information on varactor diodes can be found in an application note published by Skyworks [6].

Given these drawbacks, successful implementations of broadband adaptive amplifiers can be found in literature that utilise varactor based tuning networks. Chen and Peroulis [7] use a combination of drain bias voltage manipulation and stacked varactors to improve the power back-off (PBO) efficiency of an octave bandwidth amplifier showing significant improvements across the band even at -10 dB PBO. Similarly, Hallberg et. al. [8] has achieved PBO performance improvement over a wide bandwidth using a varactor-based output matching network but with limited parameter optimisation such as drain voltage manipulation showing the efficiency trade-off that comes with simplified control mechanisms.

1.6 – Active Load Modulation Techniques

The Doherty and Chireix amplifier architectures both fall under the category of active load modulation that present transistors with apparent impedances based on the superposition of the magnitude and phase of forward and reverse waveforms. An analysis of the conventional concepts for both architectures can be found in [9].

1.6.1 - The Doherty Amplifier

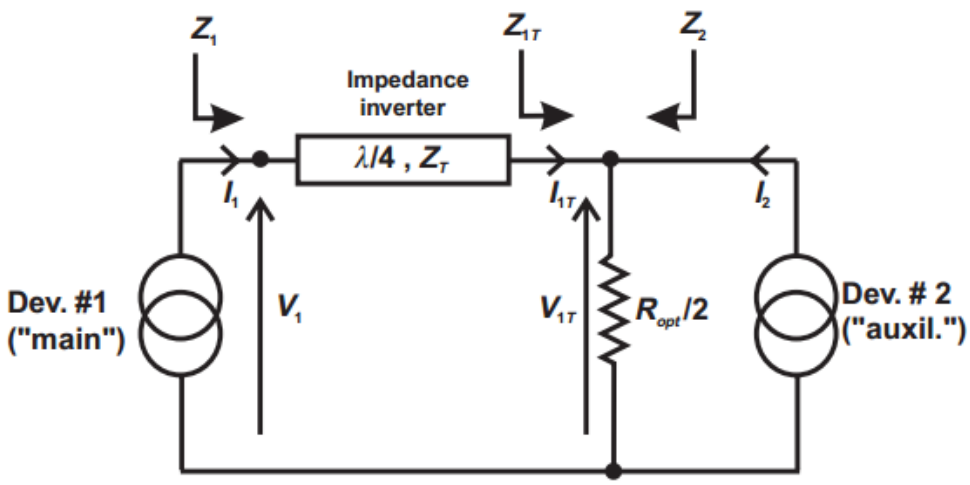


Figure 10 - Schematic representation of a Doherty amplifier. [4]

The Doherty amplifier conventionally relies on an oversized, class-C, auxiliary peaking amplifier driven by the same input signal to the main amplifier and a quarter wave impedance inversion network on the output of the main amplifier to combine the two output waveforms such that the superimposed waveform presents an optimal impedance to the main transistor at saturated output power and, under the classical configuration, the 6dB PBO point resulting in an efficiency profile such as Figure 11.

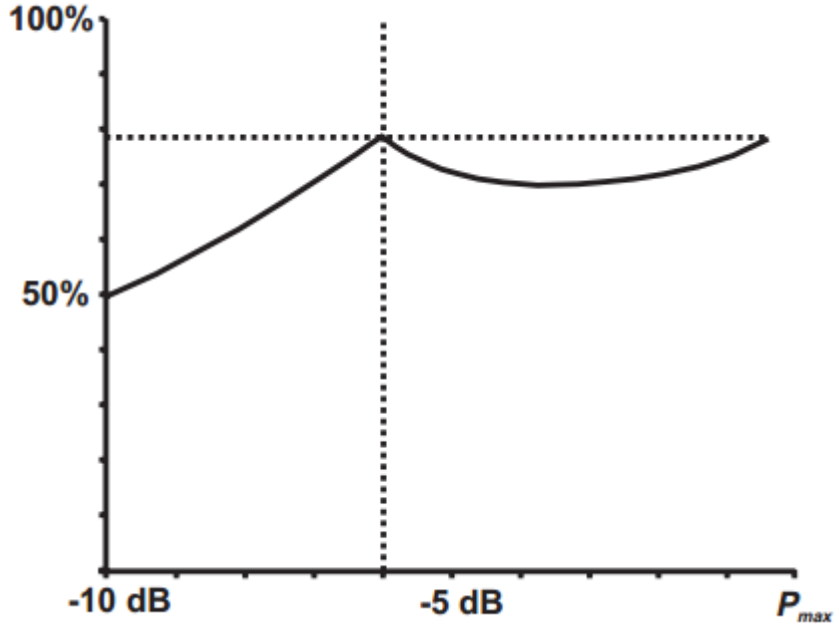


Figure 11 - Power back-off efficiency profile for a Doherty amplifier. [4]

This is a great configuration for narrowband applications where PAPR is only 6dB but as discussed earlier, modern communication modulation methods demand higher PAPR ratios that extend to as much as 12dB. By resizing the peaking device and class of operation it is possible to move the breakpoint of the second peak of maximum efficiency at PBO to tailor the amplifier design for a specific application, sacrificing absolute efficiency in power back-off for higher modulated signal efficiency in operation.

Efforts have been made to maintain efficiency under extended PAPR with the introduction of N-way Doherty PAs where additional peaking amplifiers are configured to give multiple breakpoints in the PBO curve. A sufficiently broadband 3-way Doherty designed for LTE signals can be found in [10] which demonstrated high efficiency over 12dB PBO with minimal efficiency

drop in the mid PBO range due to the additional peaking amplifier. Similar work can be found tailoring to the WCDMA modulation method in [11] using the 3-way Doherty design.

Using a fixed quarter wave impedance inverter at the output of the Doherty amplifier limits the bandwidth achievable significantly. Recent works [12] have shown that performing IQ modulation on the signal driving one of the amplifiers can significantly improve the achievable bandwidth while still maintaining the dynamic range and efficiency improvement that comes with the Doherty architecture. The IQ modulation compensates for the phase requirement at the output of the devices for the correct super positioning of the waveforms as the electrical length of the output transmission lines change with frequency.

1.6.2 - The Chireix Amplifier

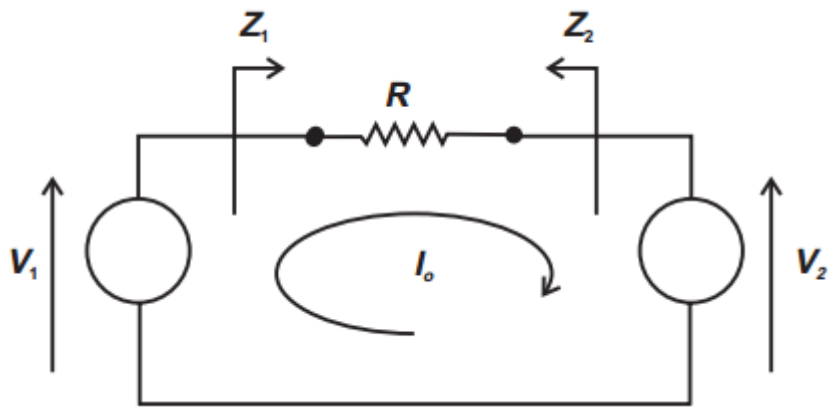


Figure 12 - Schematic of the Chireix outphasing amplifier. [4]

The Chireix outphasing power amplifier architecture relies on two differentially driven identical transistors operating in saturation into a common load. The apparent load presented to each transistor will be a function of the superimposed voltages generated by the transistors at any given relative phase angle.

Power control in a Chireix amplifier is achieved through varying the phase offset between the two amplifiers; phase shifting the two devices such that the output voltage waveforms cancel in principle cause an open circuit to be presented resulting in zero power dissipation to the load, subsequent phase adjustment results in increasing the apparent load resistance yielding greater power dissipations and therefore power output.

Outphasing the two signals not only modulates the apparent resistive element presented to the transistors but also modulates the apparent reactance.

Without compensation, the reactance will reduce the operating efficiency of the transistors.

The band limiting elements of a Chireix amplifier are the output combining network, harmonic termination and reactive compensation networks. Broadband combining networks such as the Balun and Wilkinson combiner have been used by [13] [14] to implement broadband Chireix amplifiers while retaining good PBO PAE performance.

A 4-way outphasing system has been investigated and implemented in [15] to address the sub-optimal reactive loading condition generated when outphasing two signals to obtain flatter PBO efficiency performance. Another solution to the reactive loading issue has recently been presented as a study in [16] borrowing from the active load modulation presented in this thesis by using a circulator to inject power into the Chireix combiner to create the non-Foster load required to cancel the device parasitics and maintain class-F operation over a broad bandwidth.

A class-E implementation has been realised in [17] with 10dB PBO showing good drain efficiency with relatively flat performance over a 2.1-2.45 GHz bandwidth; achieving >35% drain efficiency over the stated bandwidth at 10 dB PBO and >60% at peak power output.

1.7 – Efficiency Enhancement Techniques

PA drain voltage modulation can greatly increase the operating efficiency of an RF PA operating in classical class A, AB or B. By reducing the drain voltage with PBO, utilisation of the rail-to-rail voltage with the now reduced input drive signal is vastly improved, maintaining high efficiency.

Two well known techniques known as Envelope Tracking (ET) and Envelope Elimination and Restoration (EER) utilise the modulation of drain voltage supply to achieve greater efficiency at PBO.

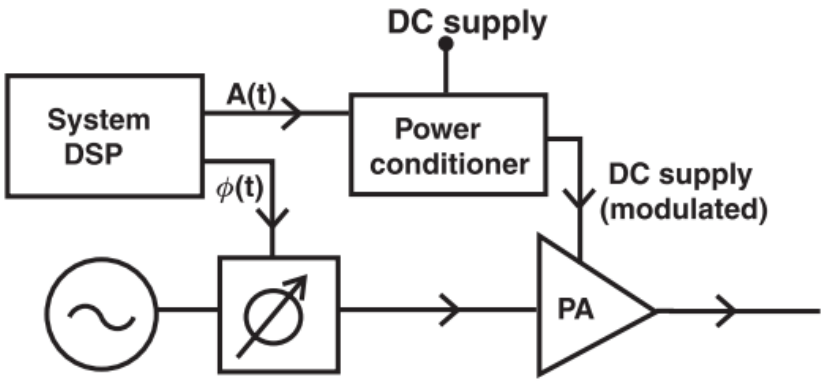


Figure 13 - Envelope tracking control schematic. [4]

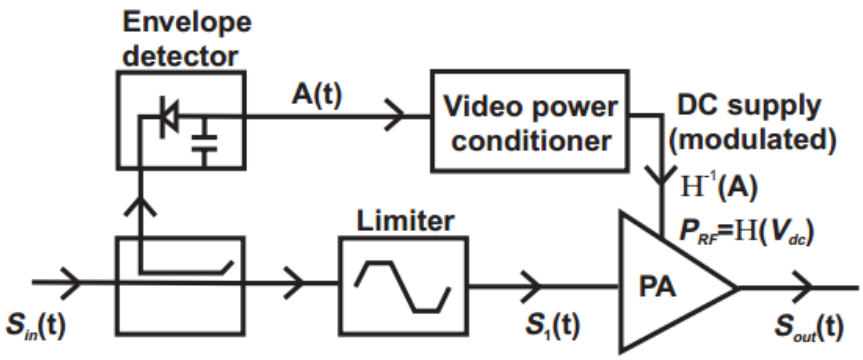


Figure 14 - EER control schematic. [4]

The EER system requires alimiter to preserve the phase information of the signal to limit any AM-PM distortion as a result of non-linear amplification by the PA. The envelope detection and video power amplifier maintain the amplitude information of the signal by means of modulating the drain of the saturated PA to control power output and thus amplitude modulation.

Envelope tracking on the other hand utilises a conventional linear PA, rather than a saturated PA, where the amplitude of the input signal is known and through digital control of the power supply, an appropriate voltage level is set to maintain optimal utilisation of rail-to-rail voltage swing.

Although in theory EER is the more efficient method, the realisation of a video power amplifier capable of producing the voltage and current requirements to modulate the saturated PA will come at an efficiency cost. ET on the other hand doesn't rely on accurate reproduction of AM information through supply control, therefore conventional DC-DC converters can be used which have a very high efficiency, having negligible impact on the overall system efficiency. The downside to DC-DC converters is usually limited bandwidth, however recent developments in CMOS implementations have shown great efficiency even at 80MHz bandwidth [18].

1.8 - The Balanced Amplifier (BA)

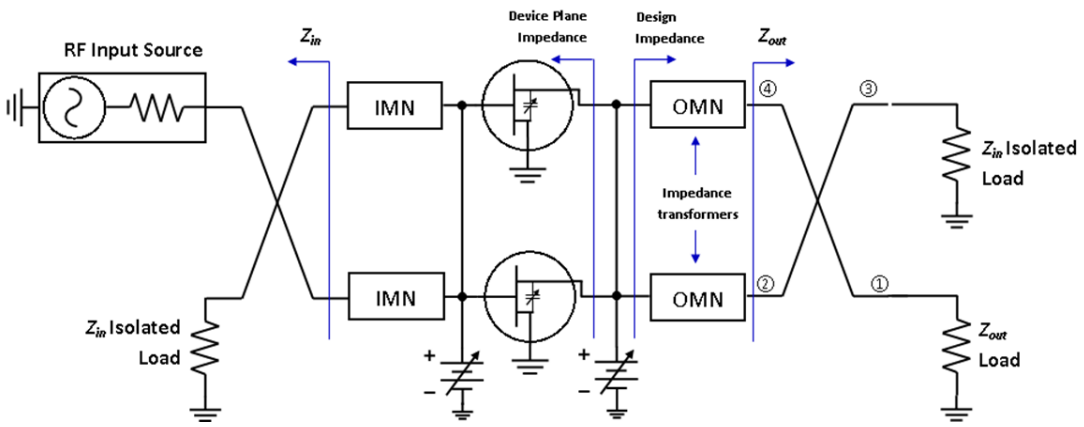


Figure 15 - Schematic representation of a balanced amplifier.

1.8.1 - Overview

The balanced amplifier has long been an architecture that offers great wideband performance with reasonable saturated drive efficiency along with great input and output return loss performance due the quadrature phasing transform of the waveforms as they propagate through the quadrature coupling structures.

The RF input signal to a balanced amplifier is traditionally fed into a 3dB quadrature coupler which splits the signal into two branches where the amplifying transistors and their matching periphery form separate identical amplifying circuits. The quadrature nature of the couplers means that the signals travelling through the two amplifying circuits are 90 degrees out of phase with each other, so a second identical quadrature coupler is required to recombine the signals with the correct phasing to produce a single output signal.

With the two amplifying circuits being fed a quadrature signal, any mismatch of impedance between the coupler characteristic impedance and the input matching network of the amplifying circuits causes the reflected power to be recombined at the input coupler but instead due to the additional quadrature phase shift will direct the reflected power to the isolated input coupler port. The same process occurs at the output coupler with the interaction between coupler impedance and output matching network mismatch.

It is this redirection of reflected power that give the balanced amplifiers its excellent return loss characteristic at the input and output ports.

Theoretically a balanced amplifier has an infinite bandwidth over which the amplifier can operate so long as the quadrature couplers satisfy the two criteria; that the magnitude separation between the coupled signals is 3dB and that the phase offset between the signals are 90 degrees offset.

In practical amplifier design there are many factors that compromise the performance of the quadrature coupler, which ultimately lead to a narrowing of the achievable bandwidth. An octave can be achieved with a single section coupler design or may be stretched to double octave given a multi-section coupler design which will be discussed in the following section.

1.8.2 - Bandwidth limitations

The balanced amplifier has three sources of bandwidth limitation; intrinsic to the manufacturing technology will lead to a maximum operational frequency,

fmax, beyond which the power gain of the transistor drops below unity, the coupling bandwidth of the quadrature couplers used and the cut-off frequency, f_c, of the matching networks used within the design.

This thesis will primarily focus on the use of Gallium Nitride on Silicon Carbide (GaN on SiC) which with modern processes typically achieve an f_{max} >32GHz on a commercial 0.25µm fabrication process. Commercial off the shelf (COTs) GaN bare die and packaged transistors with varying degrees of manufacturer alterations to the GaN fabrication process are also available. The products that are optimised for a particular frequency band will also have a limited operational frequency range for the transistor. Given that the operation frequency range of a given RF transistor such as Quorvo's bare die TGF2023-02 spans multiple octaves, with careful selection of foundry technology the frequency limitation of the transistor technology is generally not a limiting factory in achieving a broadband balanced amplifier.

Quadrature hybrid couplers are a sub-class of coupling structures that are constructed using multiple sections of transmission lines. All quadrature hybrid couplers are defined by their property of producing two output signals that are 3dB lower in power than the input signal with the phase difference between the two output signals being 90 degrees offset from one another. There are four conventional arrangements to creating a quadrature hybrid coupler; Lange, broadside, edge and branchline. All the above-mentioned quadrature coupler designs use quarter wave (λ/4) transmission line sections

which dictates the centre operational frequency of the coupler either side of which the desired coupling factor deviates from the desired 3dB value. The theory of coupled line structures has been well documented and published in books and journals so will not be discussed in detail in this thesis, only the practical implementation and bandwidth extension methods, such as over coupling and phase compensation, will be addressed. Given compromise on absolute performance requirements the above coupling structures can span bandwidths greater than an octave.

Typical matching networks of high frequency RF amplifies consist of n number of sections of low, high or bandpass filter networks that transform the port interface impedance, usually 50 Ohms, to an impedance the transistor device requires such that power is transferred efficiently without reflection due to impedance mismatch. This is relatively trivial for a single frequency point but becomes increasingly difficult to present the required impedances over a broad frequency bandwidth without sacrificing on optimal performance match. For pure, passively matched (i.e. no active devices that change characteristic with applied voltage or current) Fano's theorem dictates the return loss (the measure of incident to reflected power between two impedances) achievable by the matching network for a desired bandwidth, factoring in the parallel resistive and capacitive components of the transistor drain output for a given technology. GaN transistors have a higher output resistance than GaAs transistors making the impedance transformation ratio

of high power transistors easier to match to. For a typical 10W GaN transistor the output resistance will be around ~40 Ohms where as an equivalent GaAs device would present around ~2 Ohms. In the case of GaAs the limiting factor for matching network bandwidth comes from the transformation ratio required of the matching network, whereas in GaN the limiting factor is the one of match return loss.

Of the above frequency limitations mentioned, the matching network imposes the greatest bandwidth performance limitation. Overcoming this limitation will be the focus of this thesis through a novel method of applying active load modulation, to present the transistor device with the optimal impedance, improving the operating power and/or efficiency of the device.

1.9 – Research Objectives

The objective of this work is to provide an amplifier architecture that is capable of load modulation over very wide, octave+ bandwidth, which can be electronically controlled and reconfigured to optimise the PA depending on mode of operation and current drive condition.

Theoretical ideal analysis will be established for the control of the amplifier's impedance environment, supported by fabricated circuit measurement based off of the ideal analysis.

Implementation practicalities will be explored and documented with the implications of any compromise explained.

1.10 – Thesis Organisation

Chapter 2 – introduces the LMBA concept and architecture along with the supporting ideal analysis of how load modulation is achieved.

Chapter 3 - An L-band LMBA demonstration amplifier is presented along with the measurement setup used for all LMBA measurements presented in this thesis. Key performance graphs are presented, explained and related back to the analysis of chapter 1. Control power loss mechanisms are investigated along with alternative power control use case scenarios.

Chapter 4 - C-band and X-band amplifier results are presented in this section to illustrate the LMBA is frequency agnostic. Quadrature coupler implications

are explored two design approaches are shown for achieving flat efficiency during power back-off. Power back-off range limitations are made clear and theoretical LMBA performance with envelope tracking enhancement is presented.

Chapter 5 - Discussions on some of the practical design considerations when designing an LMBA are presented along with some exampled of inspired research coving LMBA amplifiers that use only a single RF source.

Chapter 6 - Conclusions of LMBA capability as an architecture are drawn and avenues for future work are expressed.

Chapter 2 – The Load Modulated Balanced Amplifier (LMBA)

2.1 – Introduction

The basic Load Modulated Balanced Amplifier is presented here as a flexible platform whereby designers can modify the device plane impedance environment of an RF Power Amplifier (RFPA) dynamically through electronic control of the magnitude and phase of the control signal fed into the normally isolated output port of a balanced amplifier as can be seen in Figure 16.

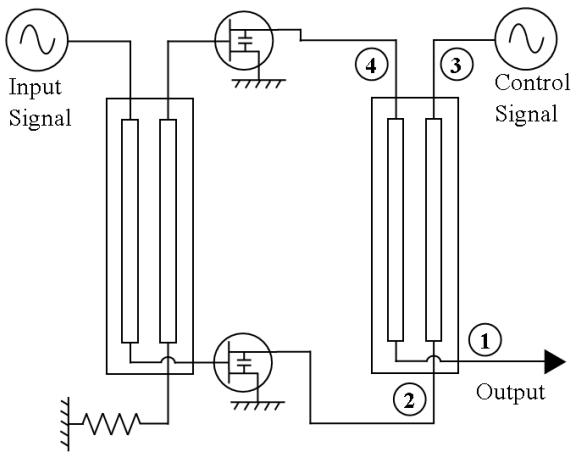


Figure 16 - Schematic representations of the Load Modulated Balanced Amplifier (LMBA)

Conventional RFPAs with fixed, reactively matched, tuning networks that use only passive elements will usually represent a compromise in performance vs bandwidth. Performance will be detuned across the band from the optimal impedance for the transistor so that the performance of the amplifier is close

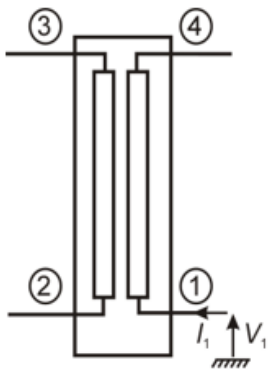
to uniform with bandwidth while presenting a good return loss over the operational bandwidth.

While it is possible to create fairly wideband amplifiers with over an octave bandwidth using structures such as the distributed amplifier architecture or the reactively matched corporate feed amplifier, the efficiency of these amplifiers is usually far below the load-pull prediction for a transistor that is optimally matched.

The control signal in an LMBA architecture can reconfigure the apparent impedance presented to the transistor pair through the superposition of waveforms in the same way active load-pull systems use forward and reverse waveforms to create any apparent impedance to present to the Device Under Test (DUT). The advantage of using a balanced arrangement is that not only are both devices modulated concurrently and identically, the injected control power used will be completely reflected so long as the transistors are modelled as perfect current generators. In practice some injected control power will be lost through metal loss and because the transistors are not perfect current generators, but a substantial amount of the injected power is recovered at the output port due to the use of quadrature hybrid couplers.

2.2 - Output Coupler Port Impedance Analysis

The impedance presented to each port of the output coupler is most easily analysed using the 4-port Z-matrix representation of an ideal 3dB quadrature hybrid coupler, as shown in Figure 17. The Z-matrix representation does not use the cross-over representation of the quadrature hybrid coupler so labelling between Figure 16 and Figure 17 has been kept consistent. This is because confusion can arise due to practical couplers used in balanced amplifiers typically have ports ① and ② crossed over so that both transistors are fed or feed into the same side of the coupler. Another assumption made in the 4-port Z-matrix representation is that the port currents I_n flow into the structure and the port voltages V_n are measured with respect to a common ground connection as depicted on port ① of Figure 17.



$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z_0 \begin{bmatrix} 0 & 0 & -j & -j\sqrt{2} \\ 0 & 0 & -j\sqrt{2} & -j \\ -j & -j\sqrt{2} & 0 & 0 \\ -j\sqrt{2} & -j & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}$$

Figure 17 - The 4-port Z matrix representation of a quadrature hybrid coupler.

In the case of the LMBA, the two balanced devices are represented as current sinks on port ② and ④ having equal magnitude, I_b, and appropriate quadrature phase offset, so that $I_2 = -I_b$, and $I_4 = -jI_b$. The control device output on port ③ can also be represented as a current sink, since in practice

this will most likely be another amplifier, which has a stipulated phase offset, ϕ, so that $I_3 = I_{con} = -jI_c e^{j\phi}$. Current flow for I_1 is defined as out of the structure so that $V_1 = -Z_0 I_1$ leading to the modified matrix of Figure 18.

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z_0 \begin{bmatrix} 0 & 0 & -j & -j\sqrt{2} \\ 0 & 0 & -j\sqrt{2} & -j \\ -j & -j\sqrt{2} & 0 & 0 \\ -j\sqrt{2} & -j & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ -I_b \\ -jI_c e^{j\phi} \\ -jI_b \end{bmatrix}$$

Figure 18 - Modified Z-matrix representing current flow for LMBA analysis.

Expanding the matrix of Figure 18 results in the following relationships:

$$\begin{aligned} V_1 &= Z_0 \cdot \left(-I_c e^{j\phi} - \sqrt{2} I_b\right) \\ V_2 &= Z_0 \cdot \left(-I_b - \sqrt{2} I_c e^{j\phi}\right) \\ V_3 &= Z_0 \cdot \left(-jI_1 + j\sqrt{2} I_b\right) \\ V_4 &= Z_0 \cdot \left(jI_b - j\sqrt{2} I_1\right) \end{aligned} \tag{1}$$

The denotation of Z_A and Z_B represent the impedance plane presented to the two transistors located on port ② and ④ and are defined as:

$$V_2 = -Z_A I_b = Z_0 \cdot \left(-I_b - \sqrt{2} I_c e^{j\phi}\right) \tag{2}$$

$$V_4 = -Z_B j I_b = Z_0 \cdot \left(jI_b - j\sqrt{2} I_1\right) \tag{3}$$

Z_A can be computed directly through rearrangement as follows:

$$\boldsymbol{Z_A = \frac{V_2}{-I_b} = Z_0 \left(1 + \sqrt{2} \frac{I_c e^{j\phi}}{I_b}\right)} \tag{4}$$

To compute Z_B requires the computation of the current I_1. We can use the relationship from the Z-matrix to determine and expression for I_1 as follows:

$$V_1 = -Z_0 I_1 = Z_0 \cdot \left(-I_c e^{j\phi} - \sqrt{2} I_b\right) \tag{5}$$

$$I_1 = I_c e^{j\phi} + \sqrt{2} I_b \tag{6}$$

Substituting (6) into (3) gives an expression for V_4 as

$$\begin{aligned} V_4 &= Z_0 \cdot \left(jI_b - j\sqrt{2}\left(I_c e^{j\phi} + \sqrt{2} I_b\right)\right) \\ V_4 &= Z_0 \cdot \left(jI_b - j\sqrt{2} I_c e^{j\phi} - 2jI_b\right) \\ V_4 &= Z_0 \cdot \left(-jI_b - j\sqrt{2} I_c e^{j\phi}\right) \end{aligned} \tag{7}$$

Therefore

$$\boldsymbol{Z_B = \frac{V_4}{-jI_b} = Z_0 \cdot \left(1 + \sqrt{2}\frac{I_c e^{j\phi}}{I_b}\right)} \tag{8}$$

Equations (4) and (8) expose the result that the impedance presented at the ports connected to each of the balanced device outputs can be modulated by adjusting the magnitude and phase of $I_c e^{j\phi}$ and that the resulting impedance is the same for each balanced device.

2.3 - Control Power Recovery

The power generated by the auxiliary amplifier is fully recovered as part of the output power in port ①. In the following we will demonstrate this.

Power output of port ① is defined as:

$$P_1 = \frac{1}{2} Z_0 I_1 I_1^* \tag{9}$$

As we know from equation (6) that:

$$I_1 = I_c e^{j\phi} + \sqrt{2} I_b$$

Where we can write the control current in terms of real and imaginary components:

$$I_c e^{j\phi} = I_c \cos\phi + j I_c \sin\phi \tag{10}$$

The total output power P_1 is:

$$\begin{aligned} P_1 &= \frac{1}{2} Z_0 \left| \left(\sqrt{2} I_b + I_c \cos\phi\right) + j I_c \sin\phi \right|^2 \\ &= \frac{1}{2} Z_0 \left(2 I_b^2 + 2\sqrt{2} I_b I_c \cos\phi + I_c^2 \cos^2\phi + I_c^2 \sin^2\phi\right) \\ &= Z_0 \left(I_b^2 + \sqrt{2} I_b I_c \cos\phi + \frac{1}{2} I_c^2 \right) \end{aligned} \tag{11}$$

The power generation at each port can now be calculated to show that their sum is equal to P_1. Analysing the power generated by each of the balanced current sources, P_{bal}:

$$2P_{bal} = I_b^2 Re\{Z_A\} = I_b^2 Re\{Z_B\}$$
$$2P_{bal} = I_b^2 Z_0 Re\left\{1 + \sqrt{2}\frac{I_c e^{j\phi}}{I_b}\right\} \quad (12)$$

Expanding out all the terms and simplifying results in:

$$2P_{bal} = Z_0\left(I_b^2 + \sqrt{2} I_b I_c \cos\phi\right) \quad (13)$$

Given that the injected control power, P_{con}, is defined by:

$$P_{con} = \frac{1}{2} Z_o I_c^2 \quad (14)$$

It can be seen that:

$$P_1 = 2P_{bal} + P_{con}$$
$$= Z_0\left(I_b^2 + \sqrt{2} I_b I_c \cos\phi + \frac{1}{2} I_c^2\right) \quad (15)$$

Comparing equation (11) to (15) it is clear that the control power is fully recovered at the output port with only a change in phase component as expected after being transformed through the quadrature coupler.

Given the result of equations (4) and (8) it has been shown that the impedances presented to the balanced devices can be modulated upwards and downwards in phase and magnitude through the control of the power ratio between the control power and balanced device power and phase offset between them.

Recalling equation (12) and (14) we can formulate a power ratio, α, where α is defined as the power ratio between the output power of one balanced device and the injected control power.

$$\frac{P_{con}}{P_{bal}} = \frac{\frac{1}{2} Z_o I_c^2}{\frac{1}{2} I_b^2 Z_0 Re\left\{1 + \sqrt{2}\frac{I_c e^{j\phi}}{I_b}\right\}} \qquad (16)$$

Defining Z_b as the impedance presented to either of the balanced devices;

$$Z_b = Z_0 \cdot \left(1 + \sqrt{2}\frac{I_c e^{j\phi}}{I_b}\right) \qquad (17)$$

Substituting (17) into (16)

$$\frac{P_{con}}{P_{bal}} = \frac{\frac{1}{2} Z_o I_c^2}{\frac{1}{2} I_b^2 Re\{Zb\}} = \frac{(I_c/I_b)^2}{Re\{Z_b/Z_0\}} \qquad (18)$$

Rearranging (17) to give

$$\frac{I_c}{I_b} = \frac{((Z_b/Z_0) - 1)}{\sqrt{2}} \tag{19}$$

$$\left(\frac{I_c}{I_b}\right)^2 = \frac{((Z_b/Z_0) - 1)^{\,2}}{2} \tag{20}$$

Substituting back (20) into (18) gives

$$\frac{P_{con}}{P_{bal}} = \frac{|Z_b/Z_0 - 1|^2}{2Re\{Z_b/Z_0\}} = \alpha \tag{21}$$

2.4 - Modulation Contours

Recalling that α is the power ratio between a single transistor and the control signal power (CSP), α can be used to plot the modulation around the reference plane impedance, Z_0, on a smith chart whereby:

$$\rho_b = \frac{z_b - 1}{z_b + 1}, \qquad (z_b = Z_b/Z_0) \tag{22}$$

Whence substituting (22) into (21) to express α as a reflection coefficient:

$$\alpha = \left|\frac{2\rho_b}{1-\rho_b}\right|^2 / 2Re\left\{\frac{1+\rho_b}{1-\rho_b}\right\} \tag{23}$$

Which can be rearranged to give:

$$|\rho_b|^2 = \alpha/(2+\alpha) \tag{24}$$

The relative control signal power (CSP) factor α thus defines a circular contour, centred at the origin of the Smith chart for a given normalised impedance Z_0. It can then be seen that varying α represents a range of impedances the active modulation is able to virtually present to the LMBA transistor devices. In Figure 19 below, three values of α have been plotted, -3dB, -6dB and -10dB. To modulate the device plane impedance downwards by a factor of 2 (e.g. 50 Ohm to 25 Ohm), the α value is ¼, so the control power required is 6dB lower than that being delivered by a single balanced device, or 9 dB down from the total output from the balanced pair. In the pre-clipped

regime such a change in load would result in a 3dB reduction in power output from the main balanced PA; this gives a qualitative indication of the useful tuning range for a very modest CSP level.

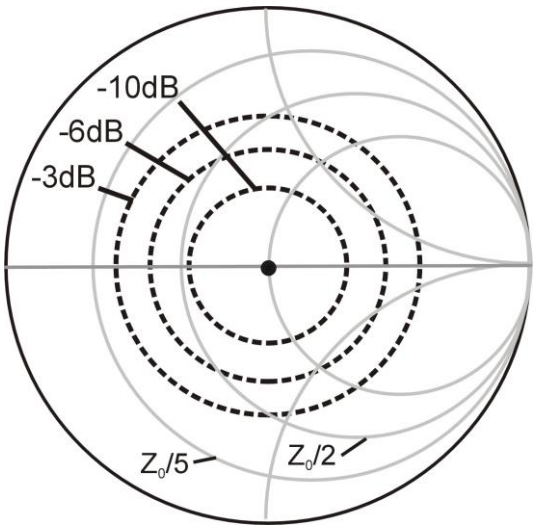


Figure 19 - Load modulation range for (dB) ratios of control to balanced PA power.

2.5 - Efficiency Definition for an LMBA System

With the control signal power being recovered at the output port of an LMBA careful attention must be paid to how this power is treated with regards to its efficiency of generation. LMBA efficiency is calculated with an efficiency factor if the CS amplifier is not integrated into the design, otherwise conventional PAE calculations will yield >100% efficiency with large enough CSP. As such a definition for LMBA efficiency is provided in (25).

$$\eta_{LMBA} = \frac{RF_{out}}{P_{dc} + \left(CSP * \left(\frac{100}{\eta_{CSP}}\right)\right)} \qquad (25)$$

Where η_{LMBA} is the efficiency of the LMBA amplifier, RF_{out} is the RF output power, P_{dc} is the DC power consumption of the balanced transistors, CSP is the power of the control signal and η_{CSP} is the generation efficiency of the CSP power as a percentage.

2.7 – Subtle Implications

2.7.1 - Frequency Dependant Modulation

Given an ideal lossless environment, the one on which the above analysis assumes, and that all elements attached to the coupler ports react in a linear manner i.e. do not produce harmonic frequencies, then it can be seen this modulation method is capable of modulating only the impedance of the fundamental signal to which the control source power is locked.

With control of the CSP frequency, power and phase the LMBA is theoretically capable of providing an impedance not only to the fundamental frequency of the RFPA but also any harmonic frequency with an independent alpha factor and phase offset, presenting the possibility for greater than octave band, harmonically tuned RFPA designs that can achieve high efficiency modes of operation.

2.7.2 - Impact of Coupler Parameters on Performance

There are four parameters that characterise a quadrature hybrid coupler; bandwidth, insertion loss, magnitude balance and phase balance. An ideal coupler has infinite bandwidth, zero insertion loss and perfectly flat phase and amplitude balance response between coupler ports. Real quadrature hybrid couplers however are realised with quarter wave, $\lambda/4$, coupled line segments that are only a quarter wave as at precise frequency; this leads to increasing phase and magnitude imbalance at all other frequencies. Therefore, the usable bandwidth of a coupler is defined by its use scenario and how

much of a phase and amplitude imbalance can the application accept. In the case of the balanced amplifier magnitude imbalances of up to 1.5 dB and a phase imbalance of 5 degrees is generally acceptable within the bandwidth of operation. Wideband couplers are characteristically over coupled at the centre frequency of operation, where the magnitude imbalance will be at its peak, to broaden the usable bandwidth of the coupler. A single section coupler with these imbalance tolerances can be capable of achieving octave bandwidth performance. For wider bandwidths the tolerances either must be loosened or the number of $\lambda/4$ line sections increased leading to a drastic increase in area and insertion loss due to metal and substrate losses.

It stands to reason then that a real coupler will introduce unequal modulation between the two transistor arms when operated as an LMBA with each α factor now differing depending on which balanced device is analysed due to the amplitude imbalance of the coupler causing amplitude imbalance of CSP to both devices. Likewise, a phase imbalance in the coupler will result in a CSP phase imbalance between devices. The impact these imbalances have will depend on the α factor the RFPA is operating under. LMBA designs that use a large α factor are more susceptible to these imbalances due to larger modulation circumference where a phase imbalance of 5 degrees would result in a larger arc segment deviation than that of a lower α factor design.

The formula of (25) allows the efficiency of an LMBA amplifier to be quantified without the need to design a CSP amplifier and given reasonable

efficiency assumptions for the generation efficiency of η_{CSP} , system performance can be evaluated.

Chapter 3 – L-Band LMBA Prototype

3.1 – Introduction

The results of this chapter are partially covered in publication [19].

An L-Band 0.8-2 GHz RFPA was designed to demonstrate the capabilities of the LMBA architecture to modulate the device plane impedance of a pair of 10W Cree CGH40010 GaN transistors. The CGH40010 transistor is a packaged device capable of operating up to 6 GHz but designed primarily for applications up to 3.5 GHz and was chosen due to its comparatively high output impedance to a similar powered GaAs device. GaN devices of this power level typically have a device plane impedance where the real part is around 25 Ohms making the CGH40010 an ideal candidate for direct modulation through the LMBA method. The demonstration RFPA shown in Figure 20 has minimal passive tuning at the input and output providing only gain tuning at the input to cover the 0.8-2 GHz operational bandwidth of the RFPA and only DC feed networks feeding the drains of both transistors.

The gate bias for the RFPA was provided though external bias tees but the drain bias was provided through approximately 30 nH hand wound inductors with a 100 pF 0402 blocking capacitor placed in the RF path. This approach was chosen to have minimal impact on the native device plane impedance this

transistor presents so that the load modulation ability of the LMBA can be shown from a near 50 Ω load impedance.

The couplers used in this design were a pair of IPP-2004 three section stripline quadrature hybrid couplers that provide excellent magnitude and phase balance over a 1.0-4.2 GHz bandwidth, easily covering the design bandwidth of this demonstrator.

Measurement of the L-band LMBA was carried out using a pair of phase locked signal generators driving class A pre-amplifiers which were dynamically power calibrated using a coupler feedback system and control software to ensure that the power injection planes, i.e. the RF input port and Control port in Figure 20 were accurately calibrated against gain imbalance in the pre-amplifiers and gain imbalance due to increasing operation temperature over long measurement runs. The schematic for this measurement system is presented in Figure 21.

The signal generators in this test setup where phase locked using a 10 MHz reference which means that the absolute phase difference between the sources is not know, but it maintained while varying the power level of the sources. On the other hand, when the frequency is changed, the phase coherence is lost. This implies that the same phase setting of the generators will not guarantee the same phase difference at their outputs when changing or moving back to the same frequency. Practically this means that the different measurement data sets are not comparable in terms of phase setting, and that

is it not possible to verify, using this measurement system, the accuracy of the load modulation in terms of phase. With this limitation it was necessary to always sweep the phase offset by 360 degrees to ensure optimum impedances were being presented.

Calibration and measurement took 0.4 seconds per measurement point of interest but given the limitation that the full phase range needed to be swept, with sufficient resolution and given the bandwidth of operation this measurement setup, a better implementation would use a 4 port VNA given sufficient equipment budget to improve the phase coherence between signals and speed up the calibration measurements as the power detectors were interfaced with over USB using the VISA protocol.

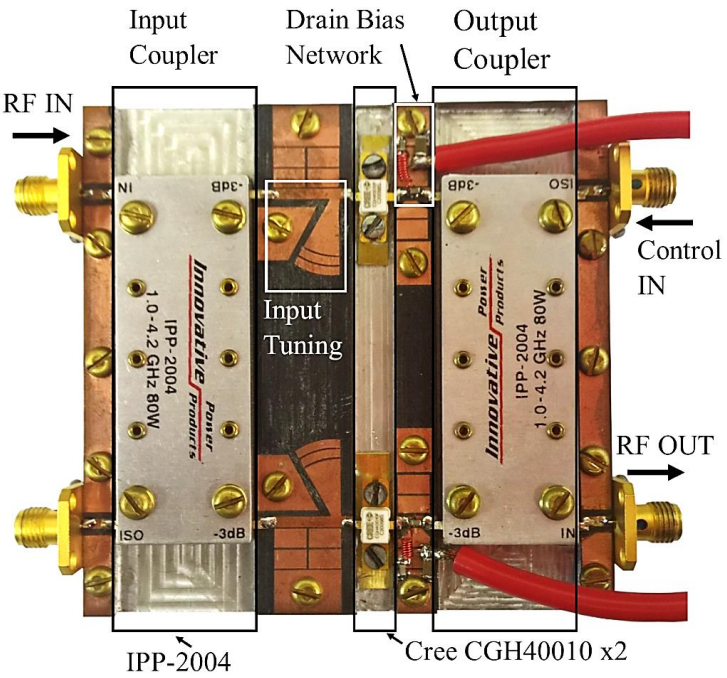


Figure 20 - L-Band LMBA demonstrator with minimal gain tuned input matching and DC feed only output matching network.

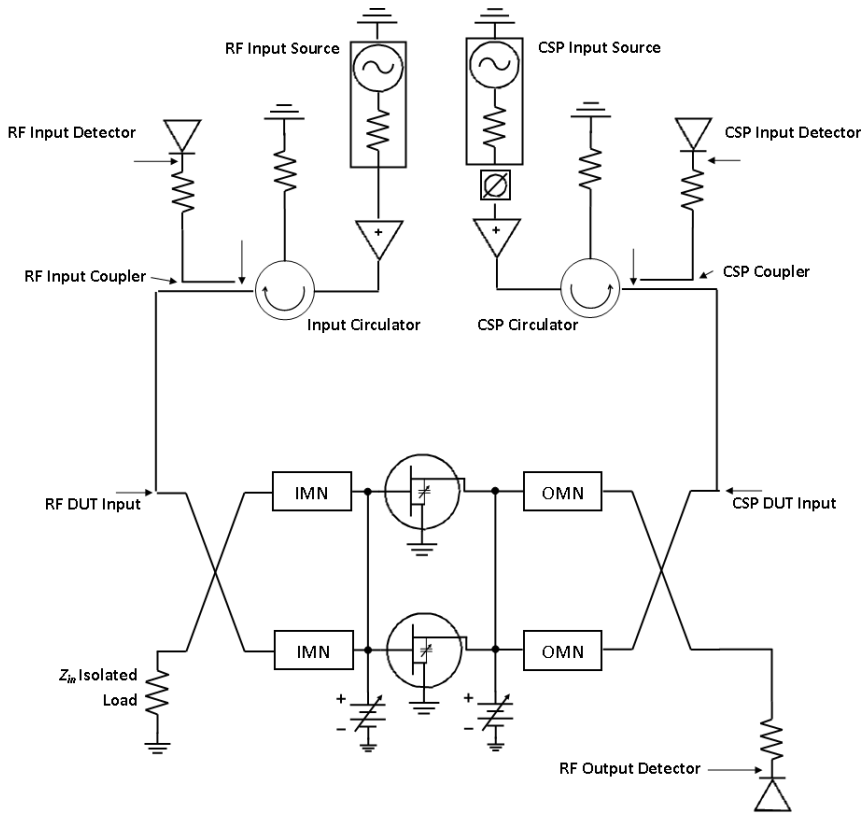


Figure 21 - Schematic of the LMBA automated measurement setup with dynamic power calibration.

3.2 - Measurement Results

Figure 22 shows the overall system efficiency and power output variations under 2 watts of control signal power through 360° phase rotation (20° steps); for graphical simplicity the power level is kept constant. These measurements give a clear indication of the improved performance of how optimum performance can be maintained across a wide frequency band. Relative phase settings between input and control sources are indicated for the maximum efficiency condition.

Figure 23 shows power and efficiency over the 0.8-2 GHz bandwidth where data series are categorised by non-modulated output power levels of 34 dBm, 37 dBm and Psat. Modulated power is plotted at the maximum efficiency condition, together with the level of efficiency achieved. For reference the efficiency with no control power applied is also included in the plot. It should be noted that these measurements were taken with a supply voltage of 18V, rather than the specified maximum 28V supply. This was done to obtain better thermal stability over lengthy measurement runs but results in lower individual device power output (38.5 dBm) than the 10 W specification for this device. As such, it is clear from Figure 22 that at the higher output power levels the 2 W power control signal is being substantially recovered. It can also be seen that at very low output levels, where the CSP starts to exceed the BPA power, the BPA devices absorb power; this is due, in part, to the load modulation moving outside the Smith Chart, as is clearly possible from the

previous ideal analysis. In practical LMBA usage such action would be avoided by reducing CSP in backed-off conditions.

Figure 22 & Figure 23 illustrate only variations in control signal phase and RF input power parameters of the LMBA. Control signal amplitude variation and DC supply voltage will yield the full range of modulation impedances capable from such an architecture.

Figure 24 shows the measured results at 18Vds, 1.5 GHz, while varying control signal power for a fixed input drive power which produces 40.8dBm of output power under no modulation condition.

The growing modulation loop exhibited in Figure 24 illustrates how changing the alpha factor by applying more CSP power can pull the impedance of the transistors closer to optimal power and efficiency or conversely away from maximum power and efficiency where the CSP phasing pulls the impedance to a sub-optimal load impedance.

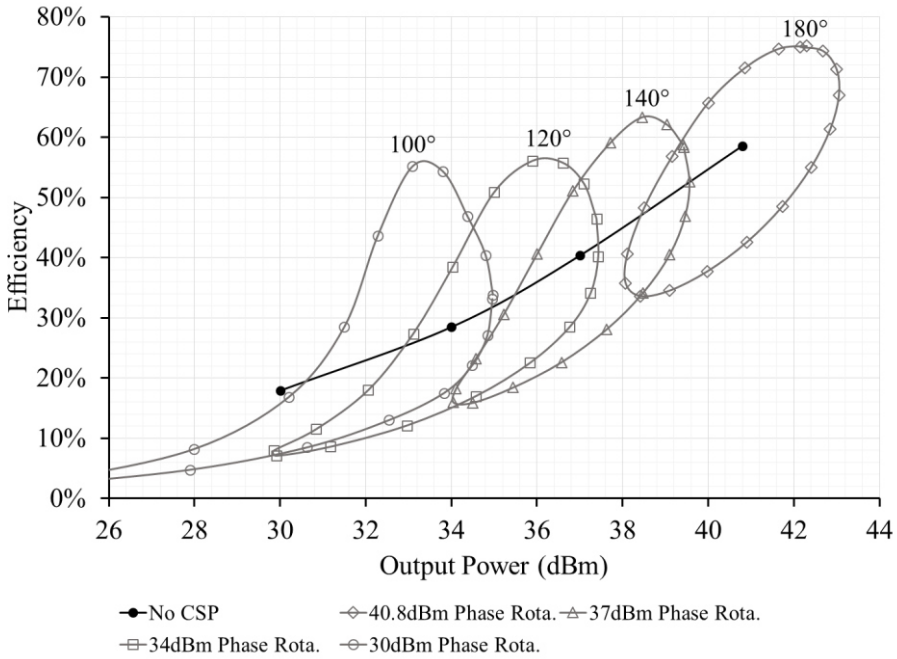


Figure 22 - Measured results at 18Vds, 1.5GHz,showing the modulation effect (loops) from 40.8, 37, 34 and 30 dBm unmodulated power output operating points (line) through 360° phase rotation using 2W control signal power.Phase numbers above loops represent phase offset at max eff. point.

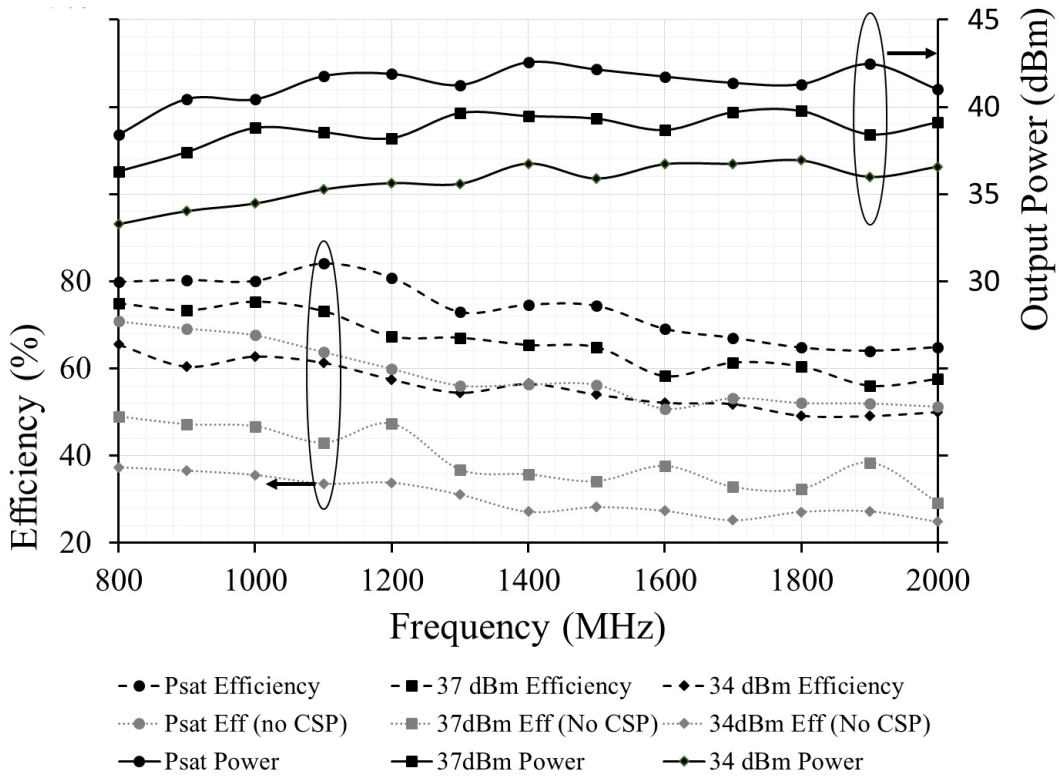


Figure 23 - Measured maximum efficiency and corresponding total output power for the L-band LMBA, over ≥ 6dB backoff power range (2W control signal power @70% applied) categorised using the output power level under no CSP.

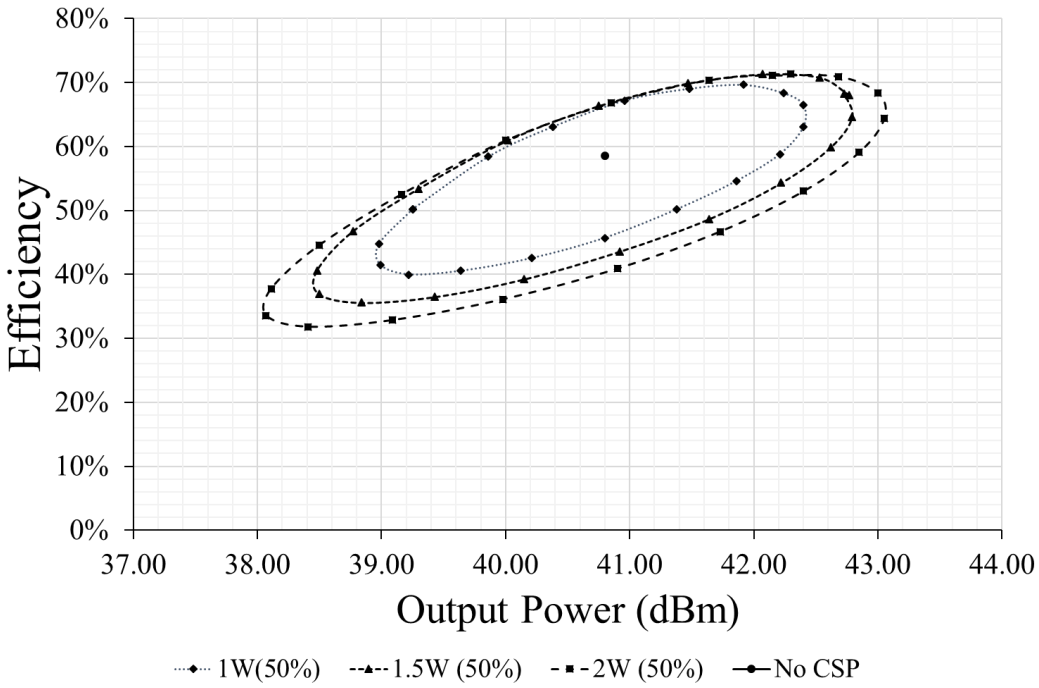


Figure 24 - Measured results at 18Vds, 1.5GHz, showing the modulation effect (loops) while varying control signal power for a fixed input drive power which produces 40.8dBm of output power under no modulation condition. CSP power is assumed to be generated at 50% efficiency.

3.3 - Power Recovery and Coupler Loss

Complete power recovery of the CSP has been theoretically analysed using ideal current source assumptions at the start of this chapter. However, field effect transistors (FETs) are not ideal current sources but rather voltage controlled current sources, whereby the output resistance of the transistor is a function of the applied drain current which in turn is a function of the applied DC gate-source and drain-source voltage. The drain source reactance will also be frequency dependant due to the associated parasitic capacitances of a FET.

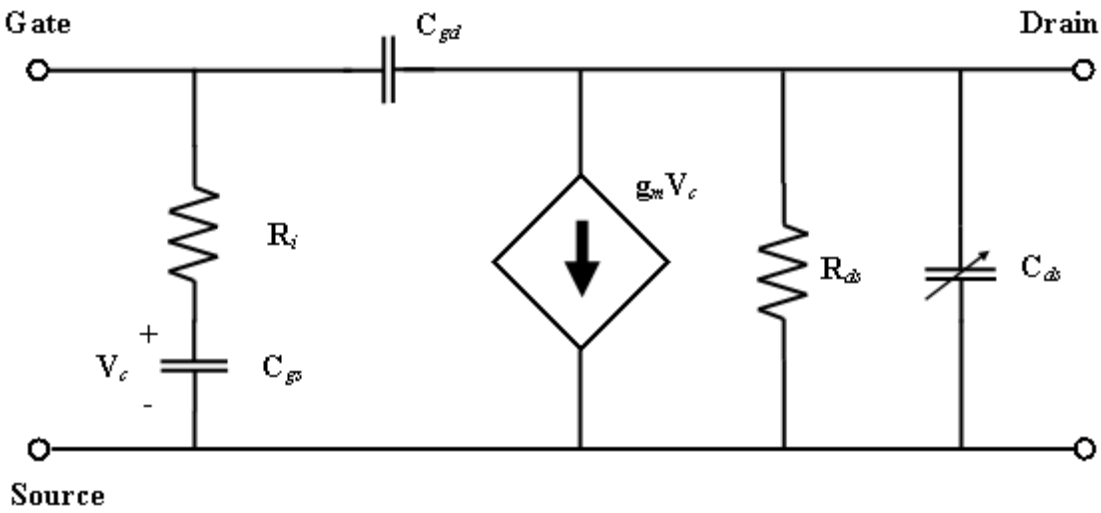
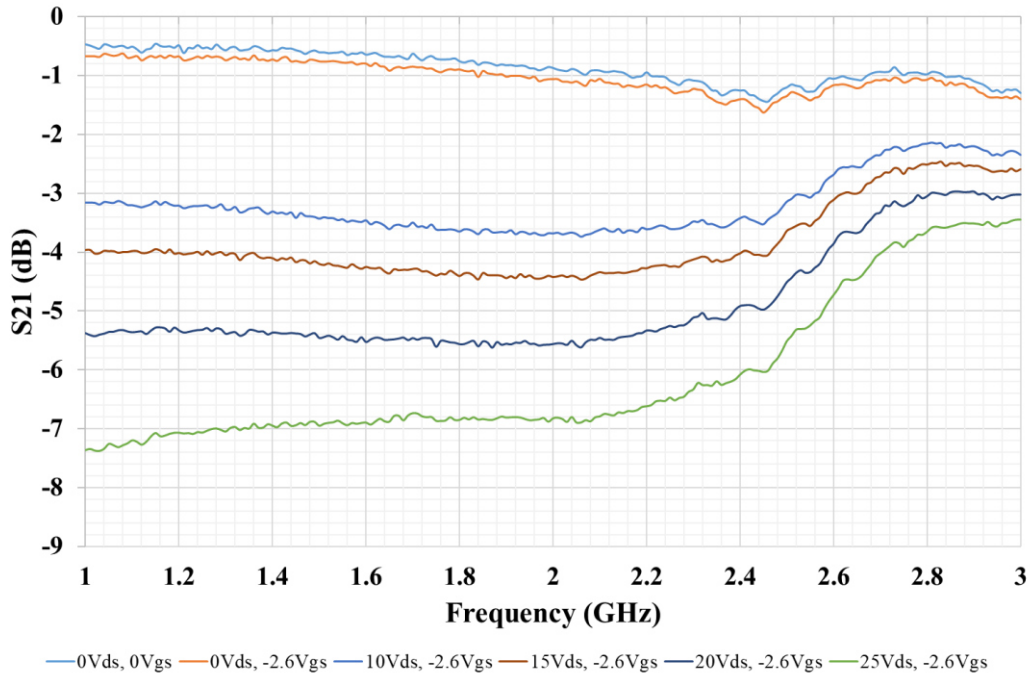


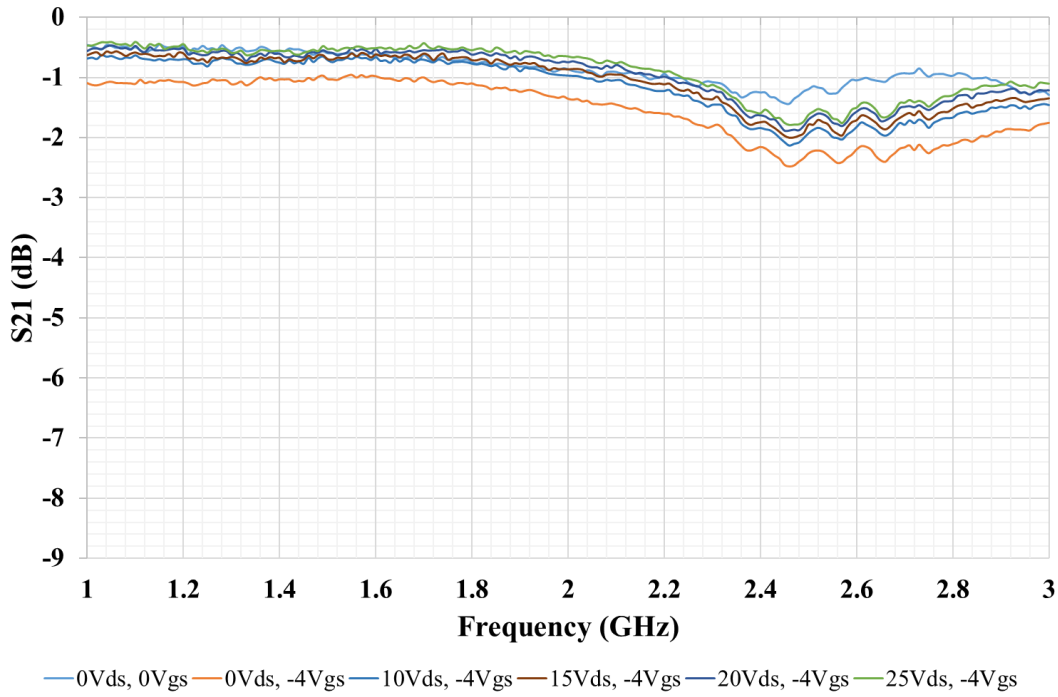
Figure 25 - Small signal model of a JFET

For complete reflection of the CSP signal to occur, the impedance presented by the transistors must be predominantly reactive. R_{ds} will depend on the applied gate and drain voltage, as the transistor channel length increases, R_{ds} will present a lower impedance and thus a lossy RF path to ground, resulting in power absorption by the transistor as can be seen in of Figure 26a.

Applying a pinch-off voltage condition to the gate of the transistor will result in near zero current flow from drain to source through R_{ds} regardless of the applied V_{ds} voltage thus Figure 26b shows almost complete reflection of CSP to the RF output port.



(a)



(b)

Figure 26 - Isolated output port to RF output port S-parameter measurements under various bias conditions showing CSP power absorbtion in the FETs of a balanced amplifier. (a) Maximum transconductance gate-source bias condition. (b) Pinch-off gate bias condition.

3.4 - Power Control

Sub-optimally matching the load by varying CSP phase can be seen as a way of varying the output power without changing the input drive power. This potentially has applications where the input power is generated from a calibrated power source where power back-off of the source is not possible, but the amplifier still needs to produce a dynamic range of output power. Conventionally this is done through a digitally controlled attenuators where the RF signal is attenuated in accordance with which attenuation bits are switch in. For applications that require precise attenuation, multiple attenuation circuits can be used with differing attenuation values arranged in a switchable series will give fine tuning of attenuation at the cost of additional space. Each attenuation bit added results in finer attenuation control at the expense of circuit area.

Attenuators are primarily linear devices that are not capable of compensating for the non-linear power profile exhibited by transistors as they approach saturated output power. One proposed use for the LMBA would be to use the control signal phase to control the LMBA output power as depicted in Figure 27.

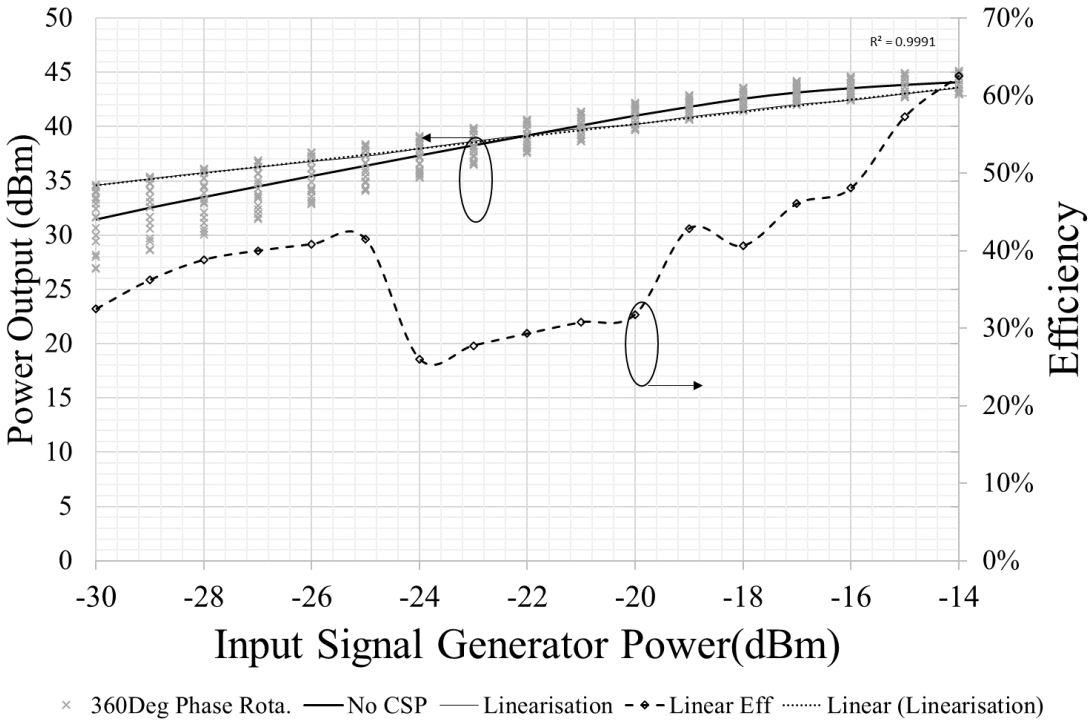


Figure 27 - Linearization of output power at 1.5GHz. Power variation is achieved through phase variation of the control signal power only.

A linear power profile has been selected from differing phase states, while varying the input signal generator power level while keeping the CSP level constant. As it can be seen from the R^2 value of the fit in Figure 27, the back off power profile is now almost completely linear, however, the amplifier is no longer operating in its most efficient state as indicated by the efficiency plot of Figure 27 whereby the efficiency has been plotted for every output power state selected when 'linearised'.

This power control method has only conceptually been explored through data mining and the author realises that such a technique would require the input RF signal to be sampled, whereby its known characteristics used to generate the correct CSP signal.

3.5 - Constant Efficiency Power Back-off

The modulation capabilities of the LMBA architecture have been demonstrated in Figure 22-Figure 27 whereby the drain impedance of a pair of transistors in a balanced RFPA where electronically modified through the use of a CSP. To better explore the exact impedance environment needed to create constant efficiency with output power backoff using only CSP, the load pull system at Cardiff University was employed and operated in such a way as to simulate how an LMBA would operate given a 'fixed impedance' like that which could be created from a passive matching network and then loadpulling in contours around the fixed impedance.

Figure 28 shows the intrinsic plane load pull contours for the Triquint TGF2023-02-01 device whereby the red contours indicate RF output power, blue contours indicate drain efficiency and green numbered squared illustrate a synthetic LMBA contour around a fixed impedance located at the maximum efficiency.

The green 'LMBA' contour position shows that with changing only the phase component of a CSP signal will cause modulation around a contour of constant efficiency while simultaneously cutting through output power contours.

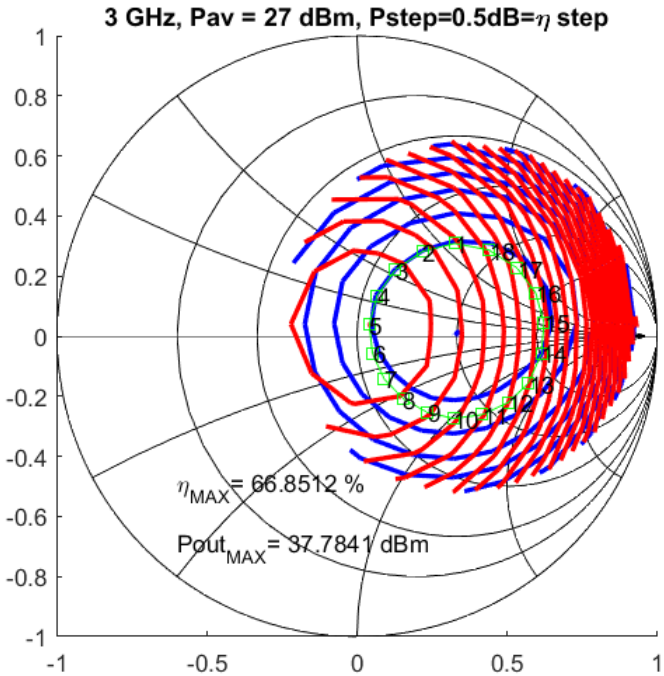


Figure 28 - Intrinsic plane load pull contours for the Triquint TGF2023-02-01 device. Red contours indicate RF output power, Blue contours indicate drain efficiency. Green numbered squared illustrate a synthetic LMBA contour around a fixed impedance located at the maximum efficiency.

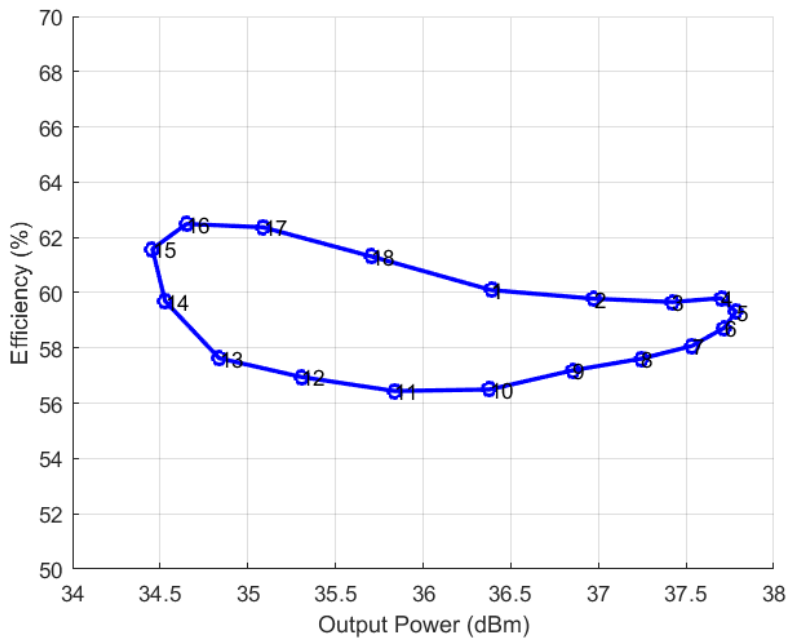


Figure 29 - Modulation loop of power vs. efficiency for the synthetic LMBA modulation contour of Figure 28.

Plotting as a modulation loop (Figure 29) of output power versus drain efficiency it is evident that to achieve flat efficiency with power back-off would require a matching network to present an exact desired impedance, which would prove difficult to achieve over a significantly wide bandwidth.

Chapter 4 – C-band and X-band Load Modulated Balanced Amplifiers

4.1 – Introduction

The work in this chapter is partially covered in publication [20] and [21].

This chapter will cover the fabrication and design of two LMBAs, the first operating at C-band covering a frequency range of 4-8 GHz and the second at X-band covering a narrower band application but targeted at constant efficiency over power back-off states.

A C-band amplifier has been realised using hybrid techniques utilising Liquid Crystal Polymer (LCP) as the passive substrate with a pair of GaN Quorvo TGF2023-02-01, 5 W bare die transistors mounted on a gold-plated copper carrier and wire bonded to the passive substrate. The quadrature couplers were realised as quasi-stripline broadside couplers embedded partially within the LCP layers of the substrate. This amplifier was designed to explore the application of the LMBA architecture over a more challenging octave bandwidth of 4-8 GHz, with the control methodology in conjunction with DC drain bias 'modulation', was explored to extend the PBO range while maintaining high efficiency.

The X-band amplifier was designed using WIN semiconductors GaN NP25 0.25um process whereby both the RF input and CSP pre-drivers were

integrated on a single MMIC including all DC biasing. Noting that driver amplifiers in this frequency band tend to operate well below the previously assumed 70% PAE, a complete system was designed on a single MMIC to evaluate the impact inefficiency drivers have on system PAE. Combined with drain bias manipulation, a discrete 10:1 power back-off profile was explored with the primary objective of maintaining a constant efficiency level at all PBO states.

4.2 – Fabrication Considerations for Quadrature Couplers

4.2.1 - Types of Coupler

Microstrip and strip line couplers fall under two broad categories; edge coupled, or broadside coupled. Single layer microstrip PCB couplers are limited to only edge coupling structures due to the lack of z-dimension while strip line PCB construction offers both edge and broadside structures to the designer. Important to note is the mode of electro-magnetic wave propagation differs in strip line and microstrip structures; the symmetrical grounding that can be seen in Figure 30 for a stripline construction allows the full TEM wave propagation to be established within the construction whereby the odd and even mode impedance of wave propagation is at the same velocity, microstrip construction however approximates to a quasi-TEM propagation mode as long as the substrate thickness is much less than the propagating wavelength, this support for only a quasi-TEM wave results in slight variations of odd and even mode wave velocity which leads to greater phase imbalance and

directionality. A more in-depth analysis of mode propagation in coupled structures for microstrip and strip line constructions is available in Pozar [22].

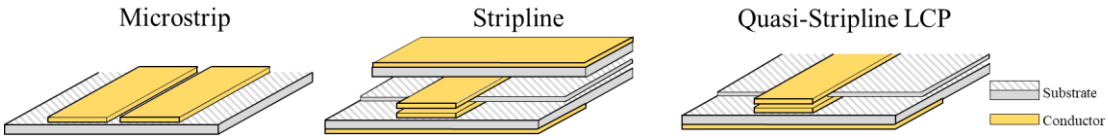


Figure 30 - Three PCB constructions for implementing couplers

4.2.2 - Considerations for Substrate Integrated Couplers

Integration of coupling structures into the amplifier passive substrate can remove the need for addition manufacturing steps which would be required to accommodate a discrete packaged coupler that typically comes in a bulky leaded package. Integrating the coupler allows the designer to optimise the coupler performance for the application bandwidth but comes with some considerations and technical challenges that need to be overcome.

Commercial packaged couplers are typically implemented as strip line couplers, such as the Innovative Power Products IPP-2004 quadrature wideband coupler used for the C-band LMBA design of the previous section. Strip line couplers offer superior phase and amplitude performance than microstrip due to the symmetrical electric field grounding afforded by the construction of bottom and top ground plane. The multiple layers of dielectric substrate with conductors embedded between the layers make stripline constructions significantly more complex than microstrip implementations.

The metal conductor deposition method on microwave thin-film substrate such as Alumina is achieved through photolithographic methods whereby the

process capability limits the minimum gap achievable between conductors, which, will be the primary limiting factor when designing tightly coupled broadband quadrature couplers. Typically thin-film processing facilities can achieve a minimum conductor seperation of 20 μm where, in some designs, may not be adequete to achieve the overcoupling nessessary for multi-octave bandwidth performance from a single section coupler design.

Utilising LCP technology, it is possible to design a quasi-stripline coupler whereby the top ground metal of a conventional stripline structure is removed (Figure 30). The advantage of using LCP is that tight coupling factors can be achived through broadside coupling while requiring minimal assembly after the PCB has been manufactured, since the LCP layers are applied as part of the passive substrate manufacturing process.

The lack of top ground conductor however causes an imbalance in the phase velocity of the odd and even mode propagating waves causing phase and amplitude imbalance between the coupler ports as can be seen in Figure 31.

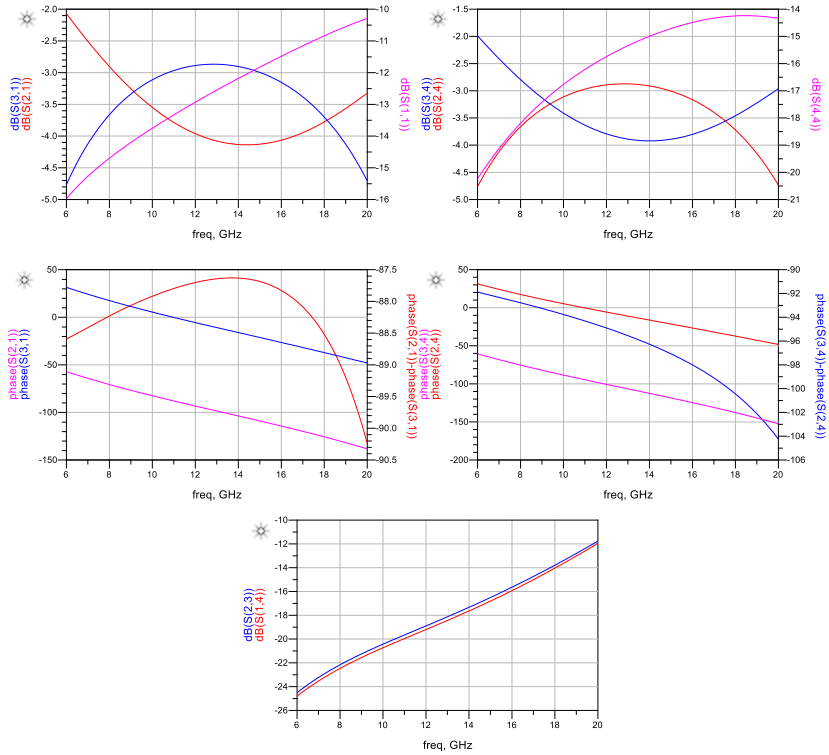


Figure 31 -Simulated S-parameter performance for a Broadside LCP coupler designed for 13GHz using a quasi-stripline structure.

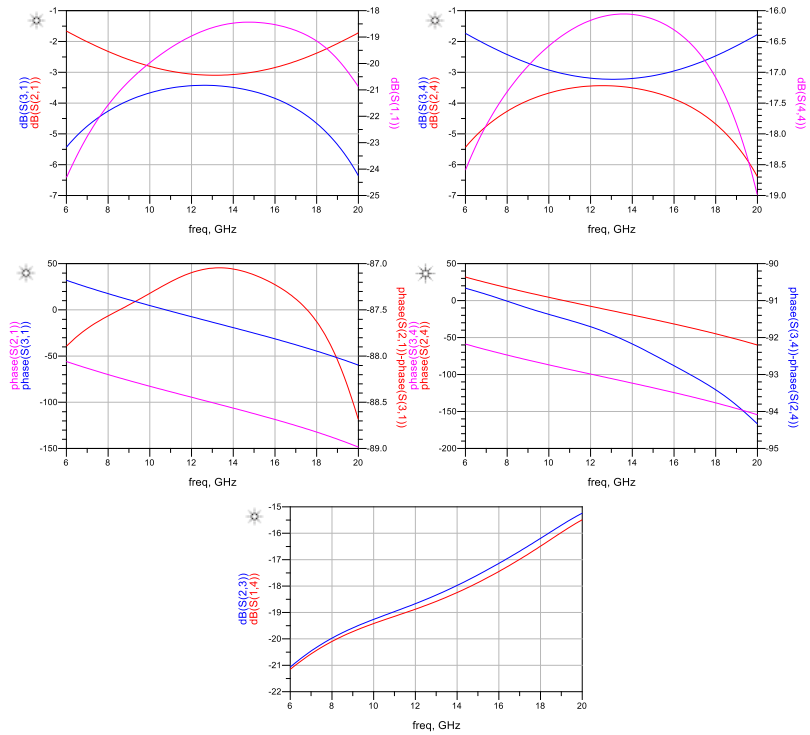


Figure 32 - Simulated S-parameter performance for a Broadside LCP coupler designed for 13GHz with a grounding cover strip.

To compensate for lack of top ground plane it may be possible to include an additional metal layer in the LCP substrate stack. From this the coupled lines can be created using the inner conductors and use the top layer conductor as a grounded cover. Simulation results using a grounded cover strip can be seen in Figure 32 for the same coupler dimensions as that of the results seen in Figure 31 but with the additional LCP substrate layer and grounded cover strip seen in Figure 33. It can be seen that the additional ground strip results in better port match and isolation along with improved phase balance.

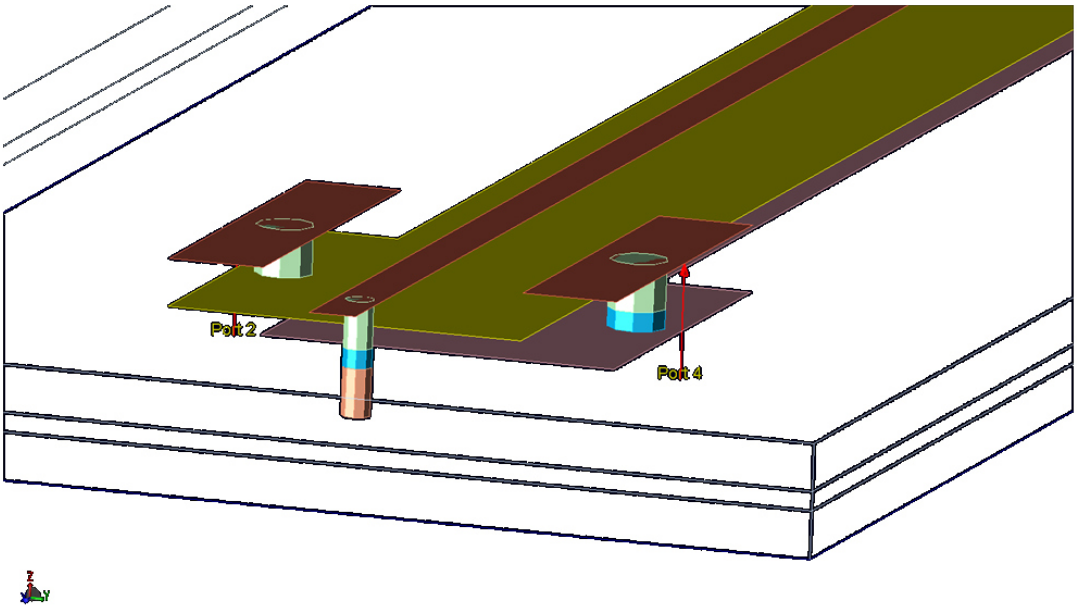


Figure 33 - 3D view of the proposed coupler with grounded cover strip.

4.3 - C-Band LMBA Hybrid on Liquid Crystal Polymer (LCP) with Integrated Couplers

4.3.1 - Introduction

To reduce the number of unknown variables it was decided that the C-band amplifier were to be constructed using a previously known working LCP coupler design as used in [23], where the quadrature coupler featured a slightly offset broadside structure which helps to balance phase velocity.

Design philosophy for the C-band amplifier followed much the same as the S-band prototype of the previous section, directly attached quadrature coupler to the transistors drain with a broadband input matching network; comprising of stepped impedance transmission lines with series di-cap capacitor as a DC block and a high impedance gate DC bias feedline using lumped SMD capacitors for decoupling and an SMD series resistor for stability.

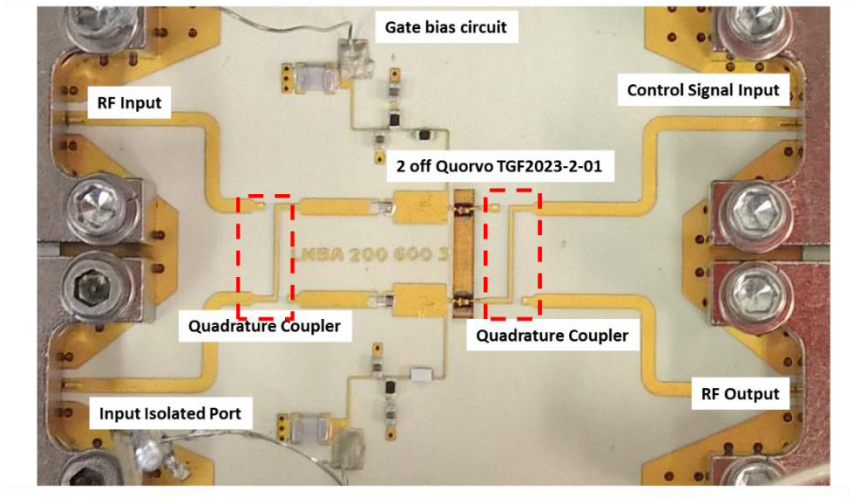


Figure 34 - C-Band LMBA octave amplifier utilising integrated embedded quadrature couplers on LCP substrate.

A loadpull simulation for the TGF2023-02-01 transistor can be seen in Figure 35 where the maximum efficiency and maximum output power drain impedance has been plotted as a function of frequency on a smith chart.

The relatively high output impedance of the GaN device is ideally suited to exploring LMBA operation with direct coupler attachment at low frequencies as it can be seen that the real part of the impedance range of the TGF2023-02-01 device over a 4-8 GHz bandwidth is between 12.5-25 Ohms.

Recalling the modulation expression of (24) and the derived Figure 19, such a modulation range targeted at maximum efficiency for the GaN device should be achievable with a CSP to device output power range of -10 dB at the lower (higher impedance) 4 GHz impedance to -3 dB at the higher (lower impedance) 8 GHz frequency.

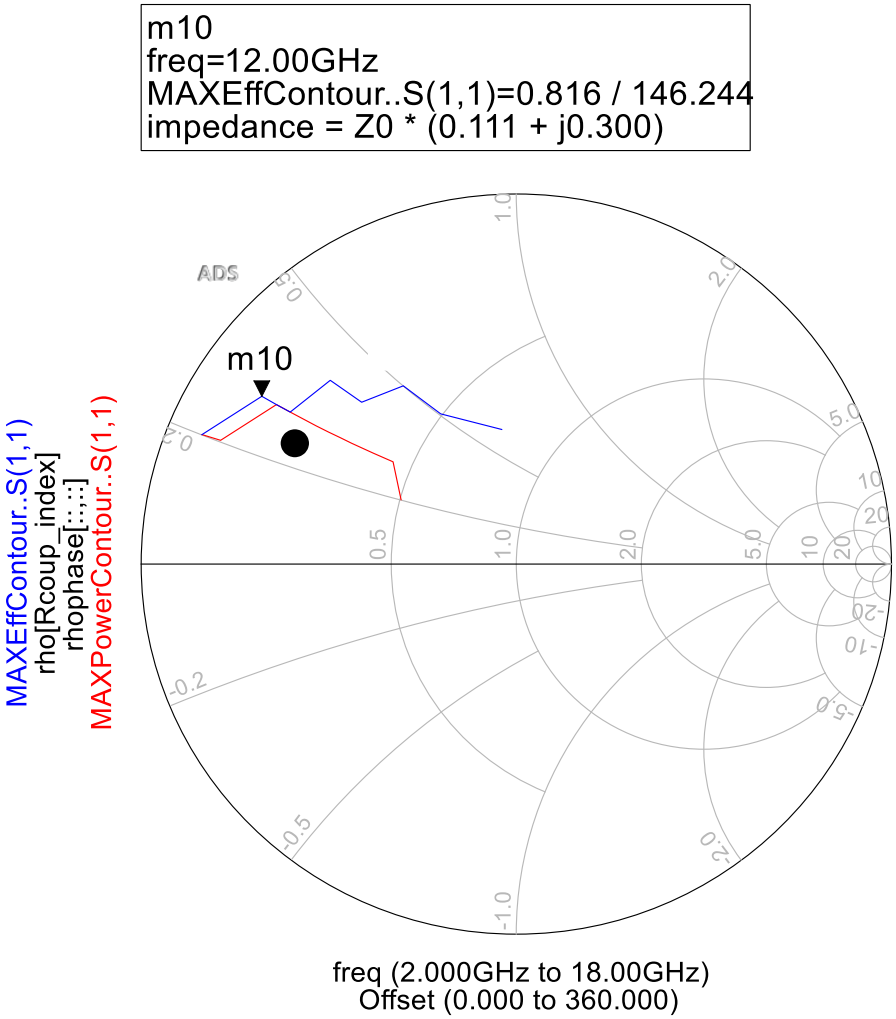


Figure 35 - Load pull maximum efficiency point contour (blue) and maximum output power contour (red) for the TGF2023-02-01 GaN transistor. Frequency range is 2-18GHz with the lower impedance points being lower in frequency, device biased at 28Vds.

4.3.2 - Measurement Results

Small signal analysis on the fabricated circuit is displayed in Figure 36. The none ideal quasi-stripline quadrature coupling structure provided the tight coupling factor required to achieve the 4-12GHz bandwidth it was designed for in [23] but like the ideal simulations shown in Figure 31, the port match suffers greatly causing the poor return loss performance shown in Figure 36.

Gain flatness can also be seen to be an issue with almost a 6 dB variation across the band. This gain variation will be an issue that we will explore when it comes to large signal efficiency performance.

Due to the large α factor requied, the -3 dB CSP to device power for these 5 W devices means that the CSP would need to be at least 2.5 W at 8 GHz and at -10 dB (0.5 W) which would require the CSP driver to have a dynamic power range of 7 dB. This PBO requirement would require the driver amplifier itself to be implemented as an LMBA to achieve the octave bandwidth requirement and high efficieny at PBO. As a compromise, the CSP level of 1 W was identified to achieve the best fixed output power performance over the bandwidth while maintaining the assumption the driver will be operating at its highest efficiency at all times.

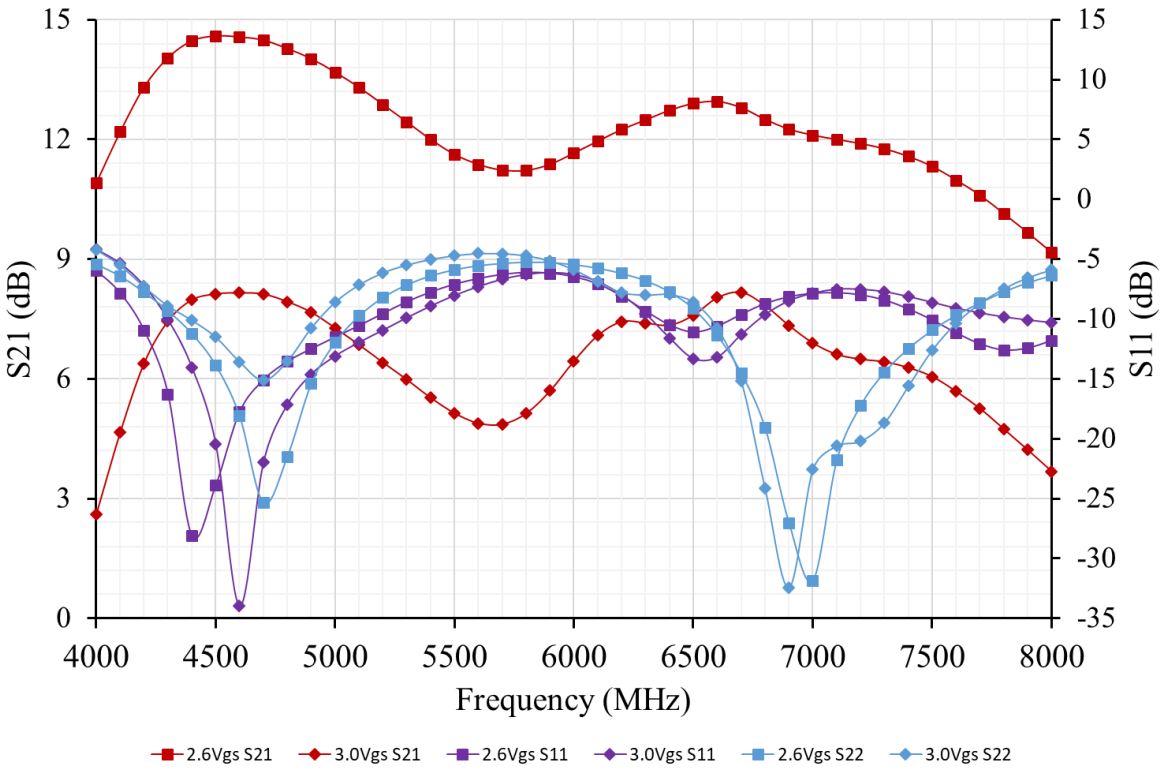


Figure 36 - S-parameter performance of the C-band LMBA amplifier under two differing gate bias conditions at 28Vds.

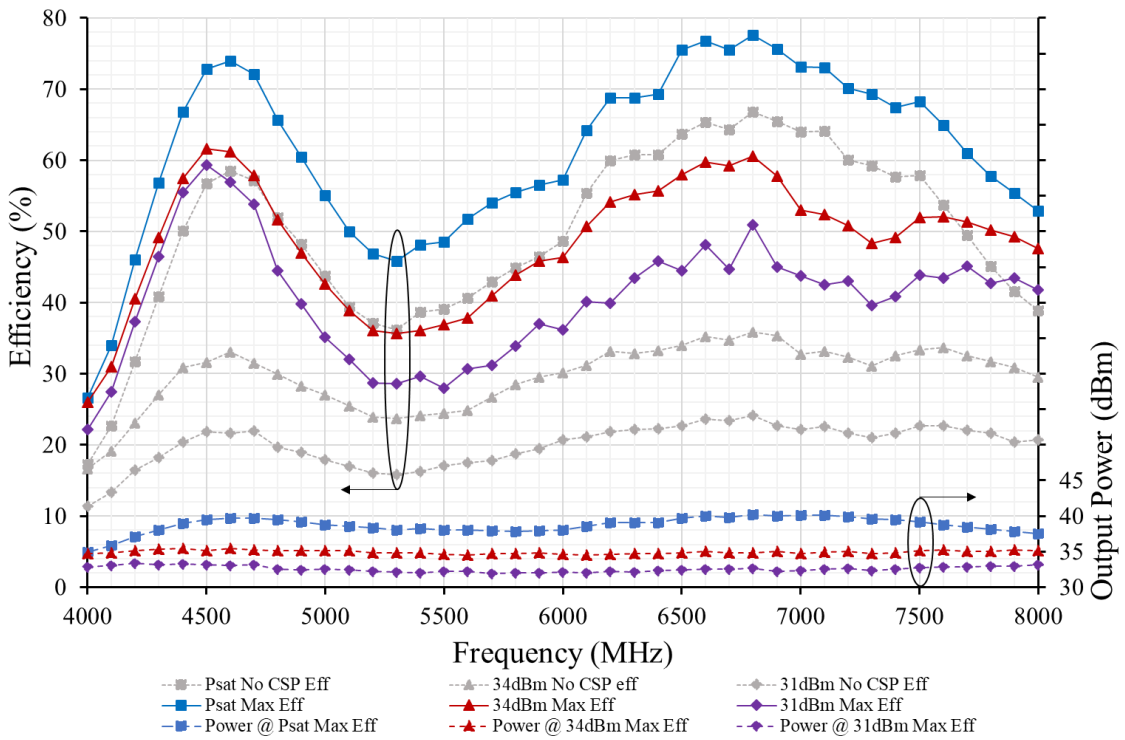


Figure 37 - Large signal bandwidth efficiency response of the C-band LMBA operating at 28V with 1W of CSP. Maximum efficiency points have been plotted from varying phase offset by 360 degrees.

The calculated efficiency of the overall amplifier for all large signal measurements presented thus far assumes a CSP amplifier to have 70% efficiency – in practice CSP signals were injected using a phase locked signal generator in the configuration shown in Figure 21.

Figure 37 shows power and efficiency over a 4 to 8 GHz bandwidth. Data series are categorized by non-modulated output power levels of 31 dBm, 34 dBm and Psat. Modulated power is plotted at the maximum efficiency condition, together with the level of efficiency achieved. For reference the efficiency with no control power applied is also included in the plot. Within each data series the trace indicating CSP is being applied always has a higher efficiency value.

Three processes can be seen in Figure 37 that attribute to the efficiency roll-off at the band edges and mid-band:

The first is that the input matching network for the amplifier has significant gain roll-off at the band edges and at the mid band which is causing loss of efficiency. The variation in gain leads to a variation in non-CSP output power which means that given the CSP was fixed to 1 W, the α will be higher where output power levels are lower leading to a much larger impedance modulation circle.

The second is that because the CSP is maintained at 1 W which translated to the optimum power level for modulation at around 6.5 GHz, naturally this

would cause over modulation at the lower frequency end of the bandwidth and under modulation at the higher end.

The third is that the return loss at the input and output ports of the amplifier indicate it is not very well matched at the mid band due to the quadrature couplers as previously mentioned.

The uneven gain ripple plays in favour of the amplifier at 8 GHz whereby the output power is lower due to gain being lower thus increasing the α factor. This explains why the efficiency is higher at 8 GHz than 4 GHz even though the gain is lower. At 4 GHz however the gain is around the nominal for the amplifier leading to over modulation of the impedance. The gain dip mid-band coupled with the corresponding poor return loss leads to a dip in efficiency that load modulation alone cannot compensate for.

From these results it has been identified that a flat gain profile is preferred for this fixed CSP mode of operation to avoid the corresponding variations seen in efficiency and output power. As the LMBA is a drain modulation method only, the small signal gain profile is predominantly influenced by the passive input match to the amplifier.

4.3.3 - Power Back-off Limitation

The PBO range of an LMBA system under fixed CSP drive power is limited to the power level of the CSP drive signal. For example, looking at the modulation loops for the C-band amplifier in Figure 38, as the LMBA approaches the power output level of the CSP over modulation is prolific. Maximum efficiency in this high PBO region under these drive conditions is dominated by the efficiency of the CSP generation and occurs where the phase offset corresponds to a presented apparent impedance that is inside of the smith chart.

Reduction in efficiency in this region can be attributed to the DC power consumption and thereby reduction in efficiency of the main balanced amplifier and the power loss as the CSP transverses the output coupler twice, leading to up to 1dB of power loss in a lossy coupler. Unfortunately, the exact performance of the embedded coupler used could not be measured due to the lack of a dedicated test cell for the structure but based off previous measurements [23] it can be estimated to be in the region of 0.75-1dB.

PBO range could be extended given control of the CSP amplitude but the efficiency profile would be governed thereafter by the efficiency profile of the CSP amplifier architecture vs input power.

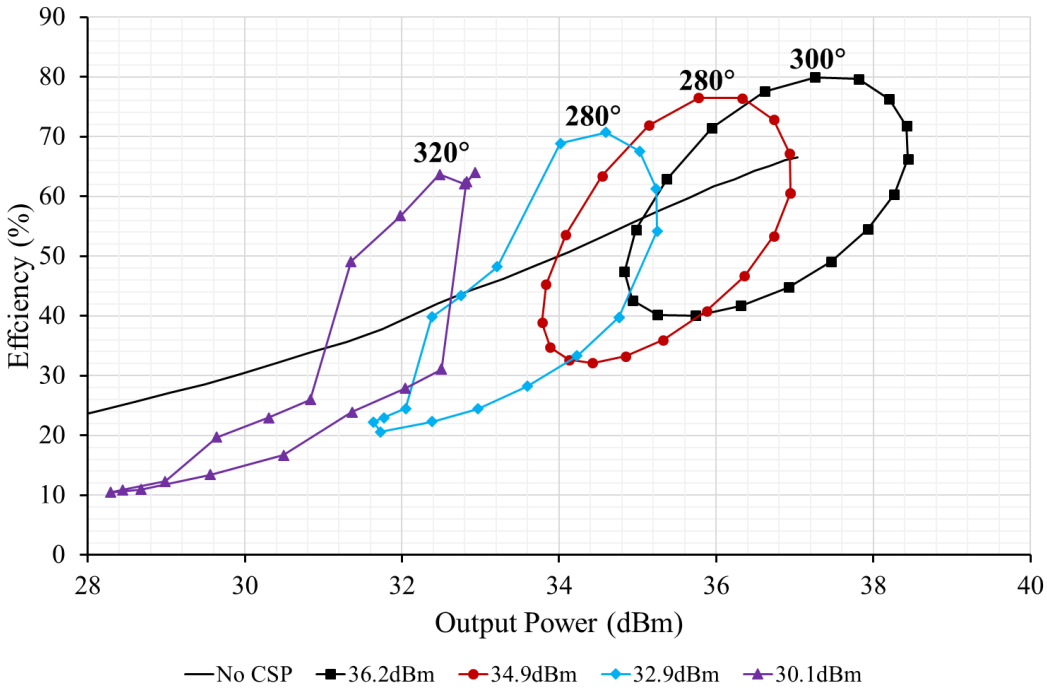


Figure 38 - Measured large signal performance of the LMBA at 6.5 GHz for various CSP phase settings. 18V, 1W CSP.

4.3.4 - PBO Under Drain Voltage Modulation

Reducing the drain voltage to a FET will decrease the DC current component thereby reducing the total current draw from the power supply. This reduction in rail voltage limits the FETs maximum power output but is irrelevant when operating at more than 3 dB PBO for most GaN devices. The reduction in DC component yields higher operating efficiencies at large PBO but also changes the R_{ds} value the output matching network needs to match to. Using the adaptive nature of the LMBA, adjusting the CSP applied will bring the apparent load back to the optimal match.

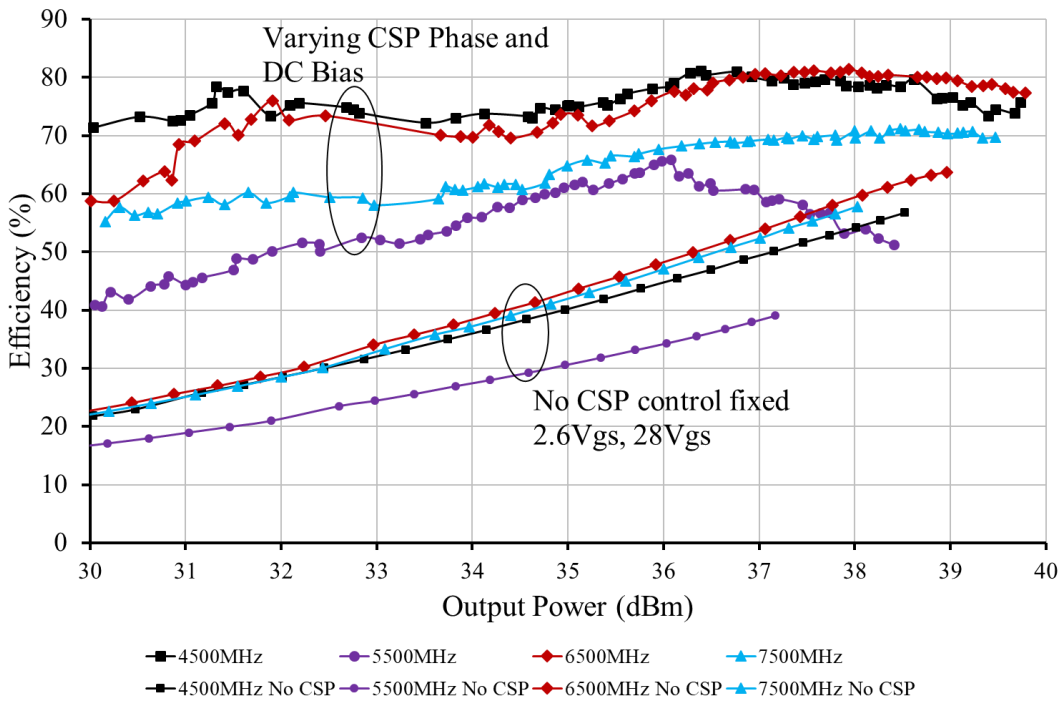


Figure 39 - Measured power back off (PBO) performance for the LMBA. Data points are chosen from measurements with 18- 28V bias, 1W CSP.

Figure 39 shows the C-band amplifier operating at high efficiency over an extended PBO range of 8-9.8 dB. The data shown was extracted through search algorithm to find the maximum efficiency given any drain voltage

between 18-28V, any phase offset between 0->360 degree for a given 1 W of CSP and any RF drive power between 16dBm to 30.5 dBm. If the data were to be shown tabulated with corresponding drain voltage and phase offset it would be seen that output power level tracked traditionally with increasing input power and drain voltage reductions from 28V at maximum output power to 18V at minimum output power yielded the highest efficiency. No conclusion could be drawn from phase offset setting due to the measurement limitation mentioned in the previous chapter.

It is noted that this method of drain modulation would not be simple to implement traditionally in a communications system that would require such a dynamic range, but with DPD becoming widely implemented and wideband envelope tracking modulators becoming available, the control mechanism can be tied to the same controller used for DPD, given that the amplitude and phase of the signal is already predetermined before transmission.

4.4 - X-Band GaN on SiC LMBA MMIC

4.4.1 - Introduction

Matching at X-band frequencies becomes a challenge due to the increasing reactance of the drain-source capacitance associated with FETs. Figure 35 showed the optimum fundamental matching impedances required for a bandwidth of 2-12 GHz whereby the higher in frequency the amplifier was to operate, the lower the real part of the optimum impedance needed to be match to.

Achieving the low impedance required through active modulation alone would require a large amount of CSP if no matching network was used to first transform the 'home' impedance. In an effort to reduce the amount of CSP power that would be required. A 14 W X-band PA was designed with a matching network that would complement the active modulation and be capable of using the reconfigurability of the LMBA technique to output lower power levels at ~5 W and 1.5 W, representing almost a 10:1 dynamic power range and still be capable of achieving high efficiency.

Figure 40 shows the fabricated MMIC using WIN semiconductors NP25 process and Figure 41 shows the schematic and bias arrangement used to achieve the output power states. The amplifier was measured using the same measurement setup as all other amplifiers, pictured in Figure 21.

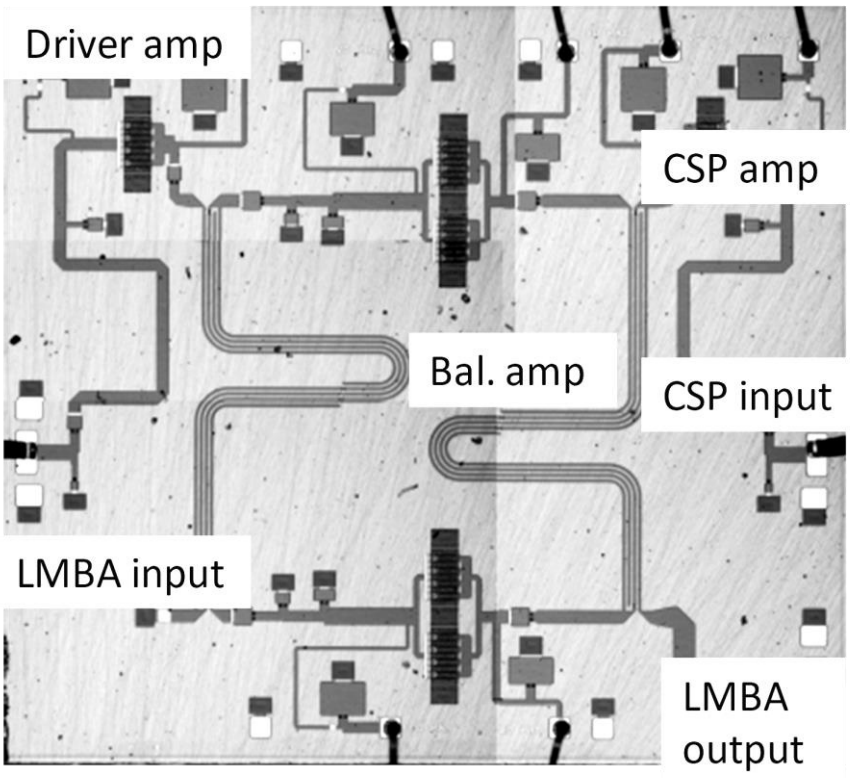


Figure 40 - Micrograph of the fabricated X-band LMBA with built in driver amplifiers.

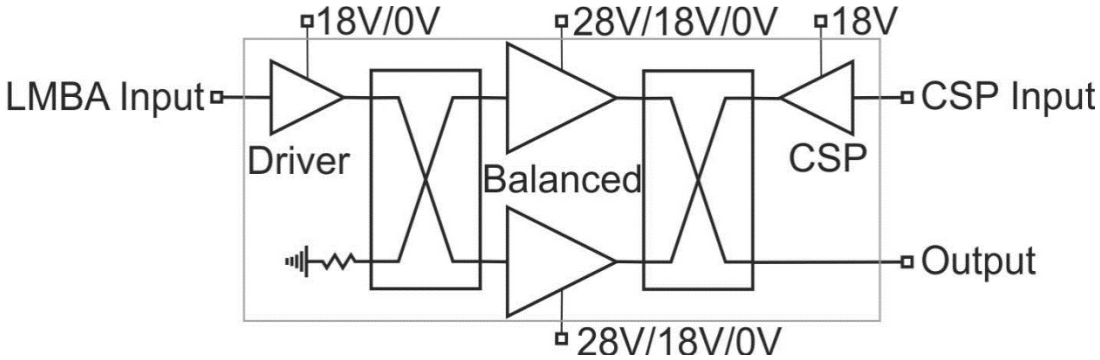


Figure 41 – System architecture and DC bias' used to drive the X-band LMBA at the stated output power states.

This X-band amplifier targeted the 8-9GHz (11.7% FBW) band for peak power performance while maintaining an acceptable efficiency bandwidth of 7.5-9.5 GHz (23.5% FBW) whereby acceptable efficiency was deemed as >35% at peak power.

It can be beneficial in certain system applications that the generated source power remain at a fixed calibrated output level and that power control is achieved through attenuation or other means. The LMBA architecture along with drain bias modulation is capable of doing such without having to resort to using digitally controlled attenuators which by definition add loss and inefficiency into an RF system. As such, this X-band amplifier is proposed to operate at a fixed RF and CSP input power of 22 dBm and sized so that the input driver and CSP driver are identical.

The LMBA MMIC incorporates a balanced amplifier pair, a driver amplifier, and a CSP amplifier in a single chip. The design objective was to demonstrate that load modulation could be employed to enable the amplifier to maintain efficiency at three discrete output power states; 14 W, 5 W, and 1.5 W by using various bias voltage states. The design strategy was to configure the balanced amplifier circuit for peak efficiency at a drain voltage of 18 V and use the LMBA function to reconfigure the balanced amplifier output match when the balanced amplifier drain voltage is varied. In this way, the added power from the CSP will contribute to the overall higher power when the drain is increased to 28 V.

To achieve efficiency at the 1.5 W output power state, the 'degenerative mode' would need to be activated. The LMBA degenerate mode is where the driver and balanced amplifier are biased off so that they draw no current and as we saw in Figure 26, zero bias is the optimal condition to get reflection of the CSP.

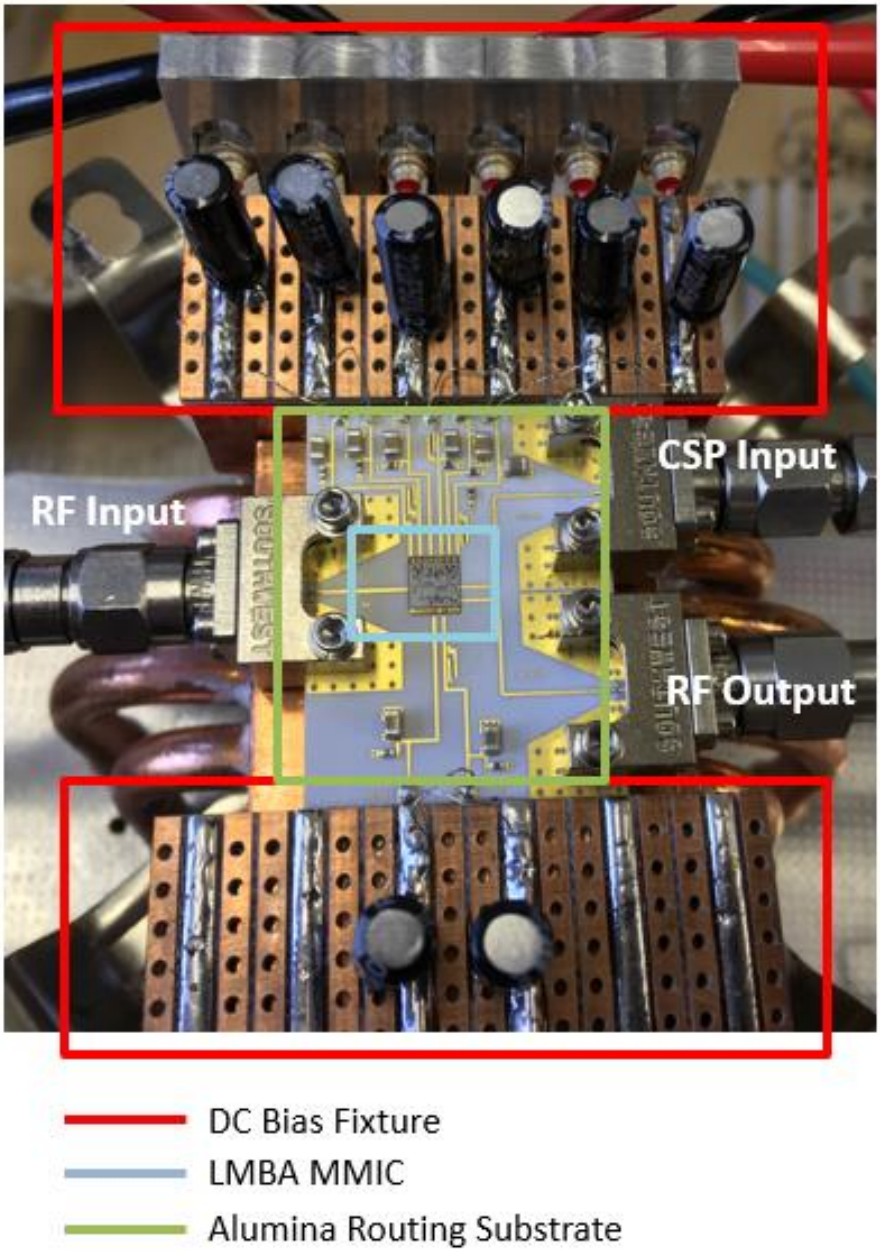


Figure 42 - Assembled MMIC mounted on gold plated copper carrier with surrounding alumina routing substrate mounted within a DC interface jig.

4.4.2 - Measurement Results

In Figure 43 the measured vs simulated S-parameter results can be seen for the MMIC design. The measured vs simulated S21 showed good agreement with S11 and S22 yielding better measured performance than simulated.

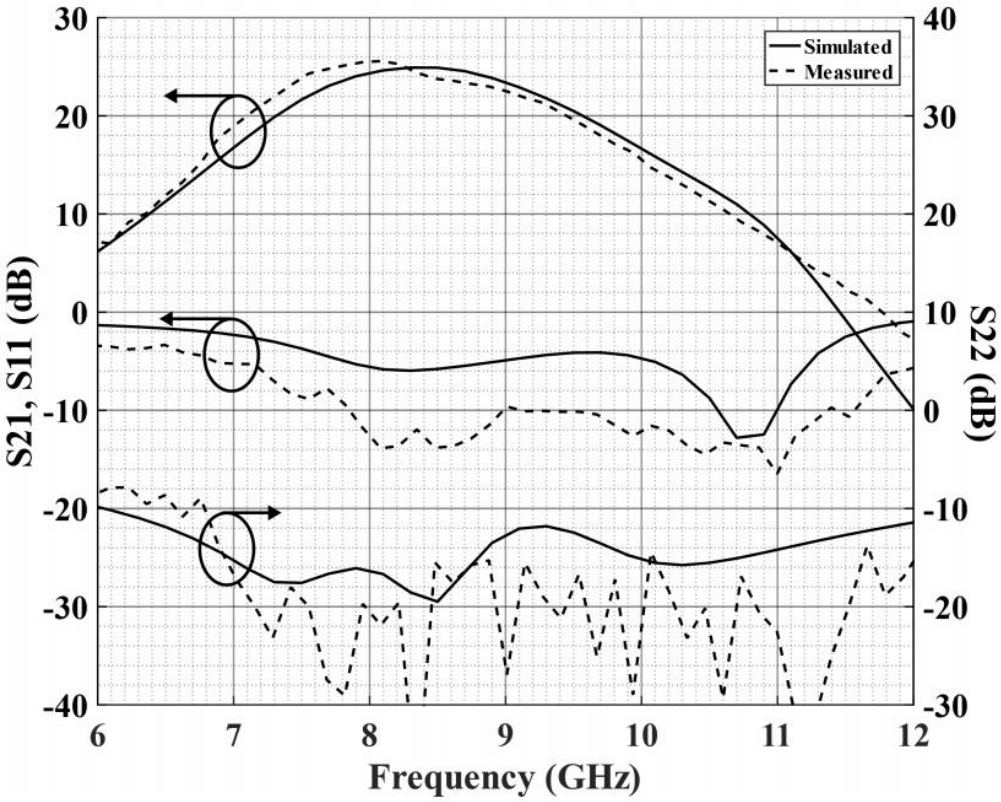


Figure 43 - Measured vs simulated S-parameter results for the X-band LMBA, 18Vds Input Driver, 28Vds Balanced stage, Common -3.7Vgs.

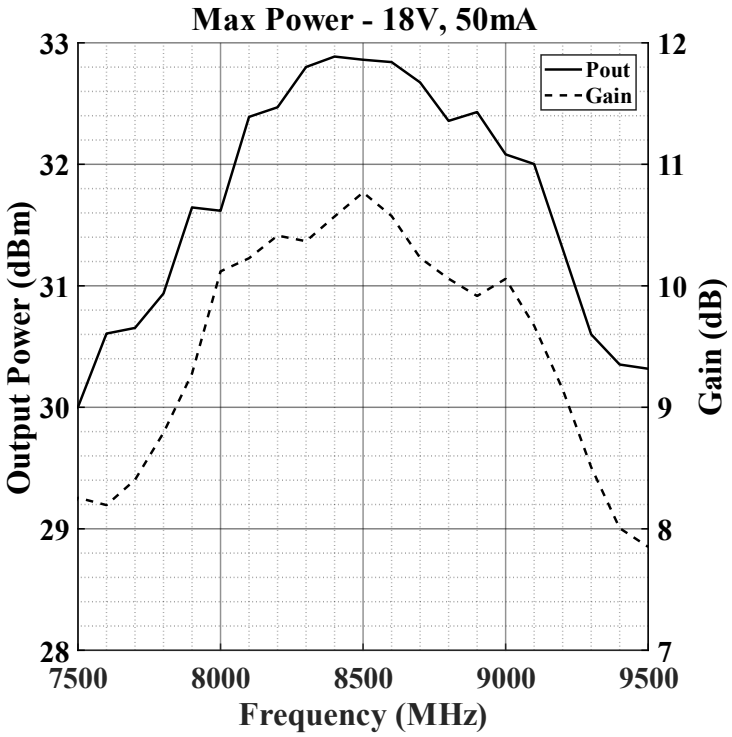
Due to limited space availability on this shared wafer run, no test cells were available to measure the performance of the driver amplifiers or the couplers directly. Using the loss figure of 0.5 dB extracted from EM simulation of the Lange coupler and the assumption that the transistors are entirely reflective, the power delivered to the FETs can be extrapolated by measuring the degenerate mode performance and subtracting the coupler loss. Figure 44

shows the resulting extracted performance for the CSP amplifier measurement which can reasonably be said to also be the performance of the input amplifier due to the drivers being symmetrical.

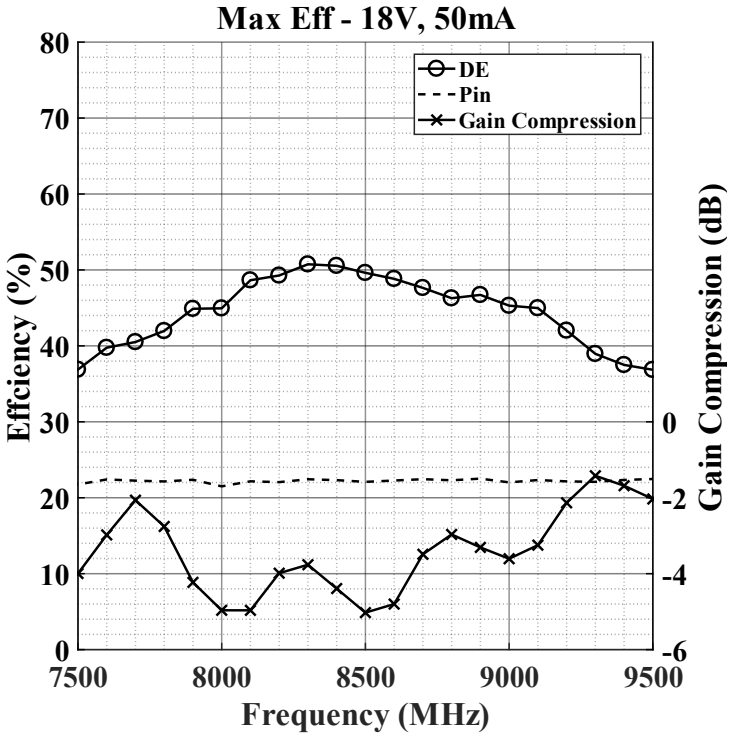
Measurement for the high power LMBA condition (Figure 45 – black trace) was extracted using the same method of running a full 360 degrees phase offset sweep for the CSP and selecting the corresponding output power and efficiency from the phase state that yielded the highest efficiency. Degenerate mode operation was measured by applying 0V bias to the input driver and main balanced amplifier and biasing the CSP amplifier as normal whereby the power reflected to the output was measured.

As the X-band amplifiers matching networks were designed for 18V operation and given the relatively narrow fractional bandwidth of 11.7%, applying CSP in this scenario would result in over modulation due to the artificial constraint that the source drive power of 22 dBm is fixed. It may be possible that performance could be improved by using a reduced CSP, but this would also add to the overall system output power and the reduced driver efficiency may start eating away at PAE gains. More will be said on driver sizing and system PAE consideration in a later chapter.

More large signal measurement results have been presented on this amplifier in [21] but have been omitted from this thesis due to the overlapping conclusions that can be drawn from the previous L-band and C-band amplifiers.



(a)



(b)

Figure 44 – (a) Driver power and (b) Driver efficiency as measured through degenerate mode operation and coupler loss calibration under 22dBm RF source power.

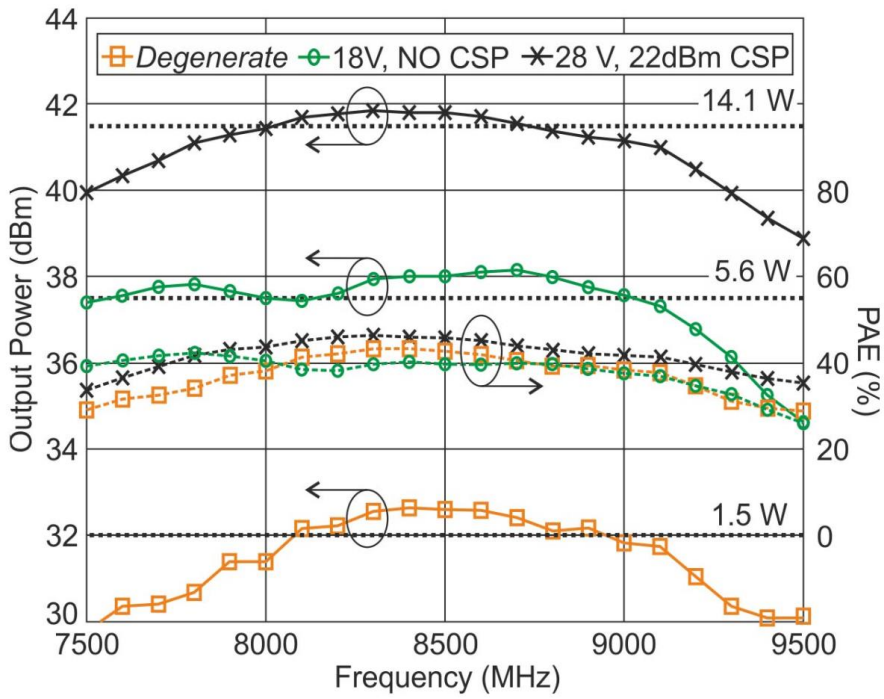


Figure 45 - X-band amplifier performance for the 3 discrete output power states with corresponding PAE. RF drive power for the source and CSP are 22dBm and drain voltage is as stated in the legend.

The X-band results show the practical implementation of another use scenario for the LMBA architecture and has successfully demonstrated that degenerate mode operation is achievable, thereby extending the PBO range to >10:1.

Chapter 5– Design Considerations for Practical LMBA Systems

5.1 – Introduction

This chapter will summarise the achieved and potential use case scenarios in which an LMBA architecture can be deployed. Active to passive matching trade-off will be discussed along with the implications it brings to system PAE.

So far in this thesis we have seen the development of the LMBA from theoretical concept through to specific application designs covering the following scenarios:

- Direct drain impedance modulation for wideband saturated power and efficiency improvement.
- Power linearization through CSP control.
- Constant efficiency PBO using only CSP phase control.
- PBO efficiency improvement using CSP and Drain Bias modulation.
- 10:1 PBO without backing off source signal power.

Each of the items above overcome a problem in a different way, and each will have its own design considerations based off transistor technology, output power, bandwidth and power back-off specifications.

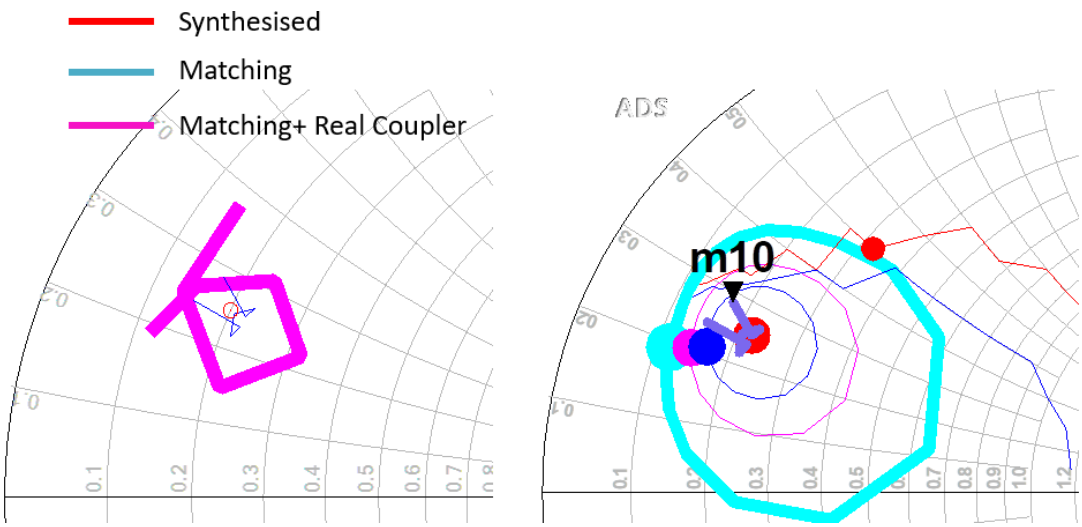
5.2 - Wideband LMBA Design and Fano & Fosters' Limits on Passive Optimal Matching

Foster [24] proposed his theorem of reactance in 1924 stating that reactance can only increase for inductive and capacitive components as electrical signal frequency increases and Fano [25] produced his technical report in 1948 on the limitations of broadband matching using passive components in arbitrary impedance matching.

These two theorems in conjunction with the transistor technology, which determines the real and reactive load presented by a given transistor, will dictate how close of an optimal impedance match is realisable over a given bandwidth.

The addition of active matching however breaks these two theorems in that the phase offset control can effectively produce a non-Foster response in apparent reactance and for a given optimally matched passive network the additional modulation afforded by active power injection is capable of achieving wideband matching better than any passive network.

With high frequency X-band and greater designs, the parasitic capacitance of the transistor dictates that the LMBA home impedance needs to be relocated, i.e. a matching network inserted, keeping the α ratio of CSP/BPA low in order to limit the impact of driver inefficiency on system PAE.



(a) *(b)*

Figure 46 – (a) Device plane drain impedance presented to transistor as a function of frequency for a fixed 'synthesised' impedance, Chebyshev match and Chebyshev match with EM simulated non-ideal coupler. (b) Load modulation contours (Cyan, Magenta and Blue) for three different α factors overlaid on the maximum power (blue) and efficiency (red) impedance trajectories of Figure 35.

Figure 46 illustrates that if a fixed impedance point can be presented to the transistor across all frequencies, then with an appropriate α factor can be established such that the modulation arc coincides with the maximum trajectories. Figure 46a illustrated that a perfect point impedance is not physically achievable over very wide bandwidths, but, a high order ideal Chebyshev or Butterworth matching network can achieve a very good approximation over the 4-14 GHz shown. With the imperfect port match of a wideband Lange coupler also accounted for, it can be seen that such a single point impedance will be very hard to achieve in practice leading to deviation in the home impedance around which the CSP will modulate.

What Figure 46b shows is that optimal impedance match can be achieved with appropriate CSP power and phase offset, and the amount of CSP used directly

affects the bandwidth over which optimum impedance can be maintained; therefore more CSP yields more bandwidth.

Without implementing the CSP driver as another LMBA, the wideband efficiency performance of this driver will be significantly less than that of the LMBA, therefore a disproportionate amount of DC power will be drawn by the driver which will impact the overall system PAE.

For example, a 10 W LMBA operating at 50% efficiency will draw 20 W of DC power, if a 1 W CSP driver is used that can only achieve 20% efficiency then the DC consumption will be 5 W meaning that for a 10:1 RF power ratio the DC consumption split is actual 4:1 which increases to 2:1 if a 2W driver with the same efficiency is used.

A very simplistic representation of this can be seen in Figure 47 whereby the CSP power has been increased from 0.2 W to 4 W at a fixed generation efficiency of 20%. The full CSP power has been added to the 10 W of power from the main balanced PA and recalculated for overall system efficiency from the total DC power consumption.

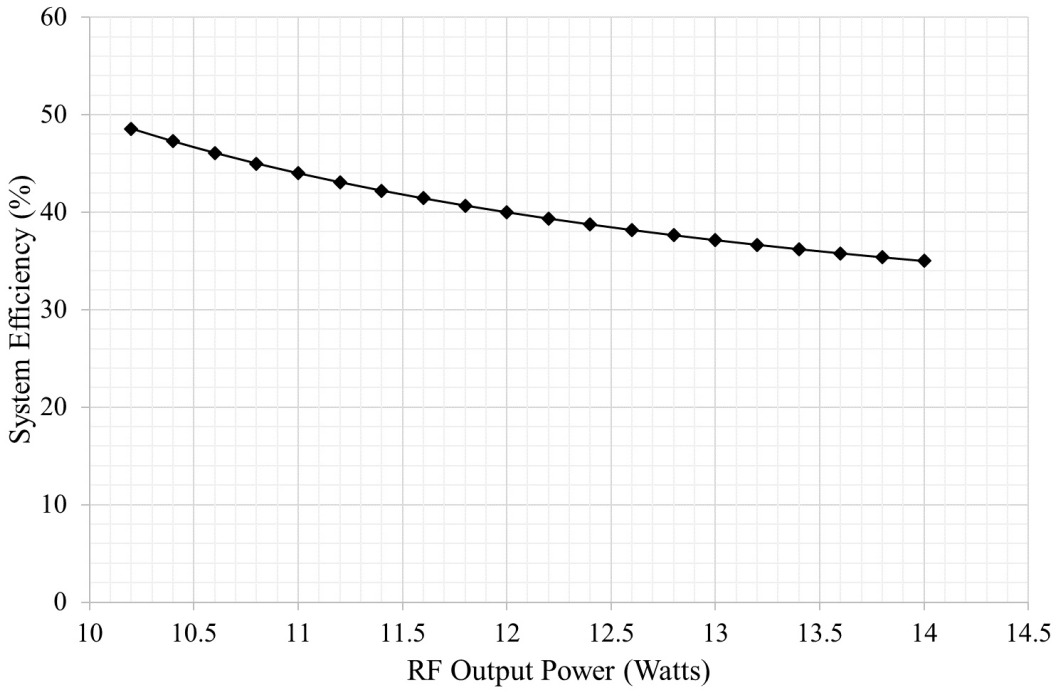


Figure 47 - System efficiency vs increasing CSP power at fixed 20% CSP generation

Figure 47 represents a simplistic view in that it is assumes that every CSP level modulated the balanced PA to the same output power and efficiency state thereby assuming the only thing that is changing is the passive output matching network.

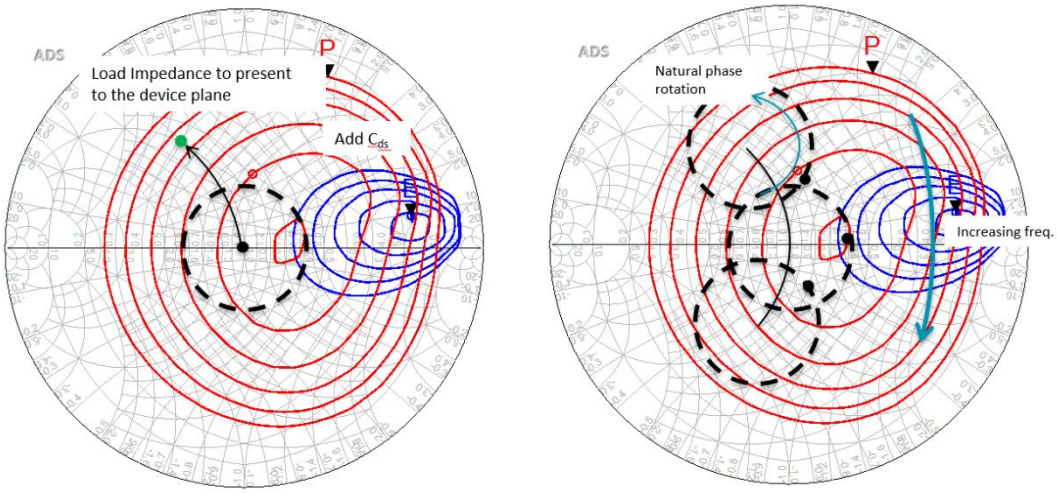
Figure 48 shows an ideal broadband matching example for a GaN transistor over a 2-14 GHz bandwidth. The loadpull contours show the impedance needed at the intrinsic plane of the device to match for optimal power (red) and PAE (blue). Matching for a good broadband return loss is easier if the impedance transformation ratio is not too great, but in the case of Figure 48 the chosen passive impedance to present to the transistor is 50 Ω at the intrinsic plane. Adding the effect of the Cds capacitance, it is clear that everywhere other than mid-band would experience a severe degradation in

output power. By adding active modulation and phase control it is possible to present an apparent impedance to the intrinsic plane that it better optimised for power output across the band while maintaining the ease of passive matching.

With CSP applied it can be seen that, on one of WIN's 8 finger by 125µm gate length (8F125) transistors with outer source vias, over the 2-14 GHz frequency band it is possible to maintain almost a flat output power profile.

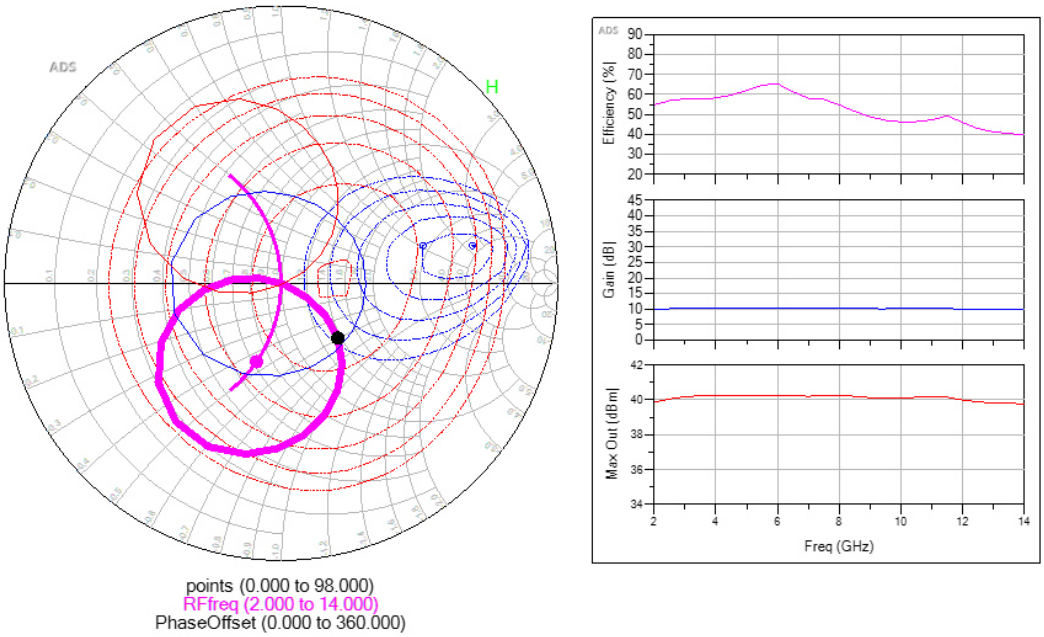
Such a fixed point matching network may give constant output power but the efficiency profile is far from constant. This is due to the intrinsic efficiency that the device is capable of, typically decreasing with increased efficiency, and due to the modulation not placing the impedance within the same efficiency contour across the band.

Having established a fixed 'home' impedance may not necessarily be optimal, it is shown in Figure 51 that an optimal, Fano constrained, passive matching network with the LMBA technique applied can produce an almost flat efficiency and power response over the entire bandwidth, thereby defeating the limiting theory Fano proposed.



(a) *(b)*

*Figure 48 - LMBA impedance modulation contours at a transistor intrinsic plane. (a) Black dot symbolises the centre impedance around which the LMBA will operate at the centre frequency of the bandwidth, green dot indicates the transformed impedance after adding Cds. (b) Black solid arc represents the intrinsic impedance presented with increasing frequency, circles represent the modulation range for a given alpha factor at 3 frequency points, black dots represent a **fixed** phase state.*



(a) *(b)*

Figure 49 - (a) ADS simulation on showing the concept depicted in Figure 48 on a 8F125 OSV transistor from the NP25 process with (b) corresponding large signal performance parameters with the device driven to 3dB compression.

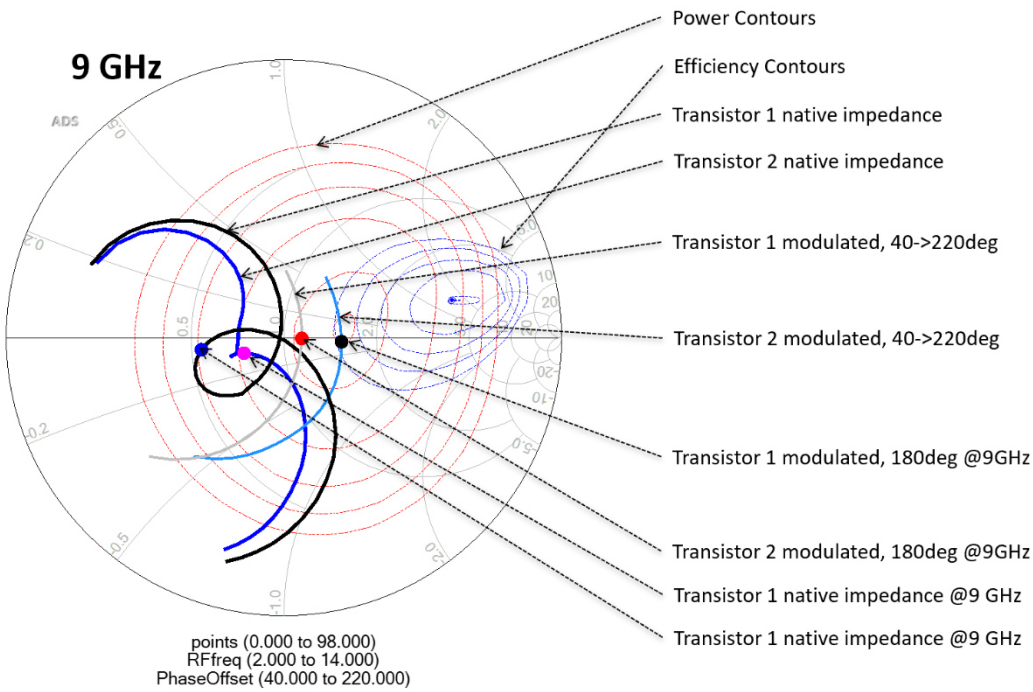


Figure 50 - Intrinsic plane impedance trajectory for both balanced transistors using non-ideal component optimal passive matching and EM simulated Lange coupler for a balanced amplifier utilizing the 8F125 transistor. Various dots represent the native and modulated impedance at 9GHz.

Through the use of a Chebyshev optimal matching network, realised using PDK elements that include metal loss and other parasitic modelling of the passive components for the NP25 process, an LMBA has been constructed. The circuit impedance environment can be seen in Figure 50 whereby the looped nature of a Chebychev match can be seen to sub-optimally match the transistors at 9 GHz. After the application of CSP, the modulated impedance is brought back to the optimal power matched condition. Since the matching network provides a looped response, the modulated impedance remains at optimal power and within the same efficiency contour, resulting in the response show in Figure 51.

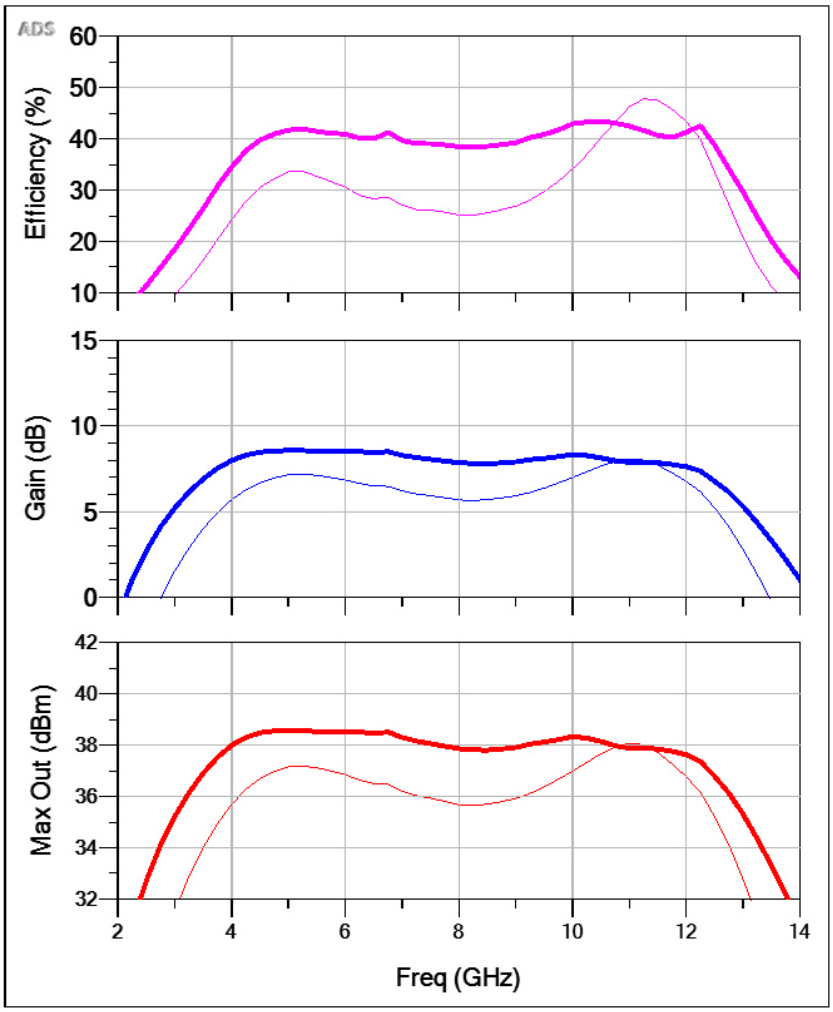


Figure 51 - Large signal response of the amplifier designed using non-ideal components and coupler. Bold trace – Performance under CSP. Faint trace – native balanced amplifier response.

The skew of the matching network impedance trajectories seen in Figure 50 show a bias towards the higher end of the band which is evident when looking at the large signal response in Figure 51. Since the CSP power was fixed for this simulation, over modulation occurs at the 10.5-11 GHz resulting in no power output improvement and a dip in efficiency as the impedance is modulated to within the same power contour but a lower efficiency contour.

Substantial gains of over 10% efficiency and 2dB output power are experienced across the bandwidth of 4-12 GHz from the already optimal passive matched balanced amplifier.

The reduction in performance between Figure 49 and Figure 51 is attributed to the losses associated with an imperfect gate match (reducing gain and in turn output power for the same source drive power), drain match and metal loss of the Lange couplers at the input and output. The bandwidth reduction is due to the now limited bandwidth of the matching network and the coupling bandwidth of the Lange coupler over the ideal infinite bandwidth coupler assumed in Figure 49.

5.3 - Fixed Phase Offset LMBA (single input)

As it can be seen in Figure 48, it is possible to use the natural phase rotation of an output matching network to optimise impedance over wide bandwidths given the correct placement of the output matching network.

Designing wideband amplifiers using this approach will yield all the benefits in section 4.2 with the additional benefit that the CSP and RF input can be fed from the same pre-amplifier, alleviating some of the system efficiency penalty related to separate amplification and reducing control complexity. The downside of this method is that the loss of phase control will remove the ability to cause non-Foster modulation which could hurt the LMBAs ability to optimise impedance under PBO conditions.

Since the publication of [19] , single input LMBAs have been presented by Cardiff University and University of Colorado utilising class-C control amplifiers to improve the PBO performance of the LMBA [26] [27] [28] [29] [30].

In [29], drain supply modulation in the form of ET has been implemented as suggested 4.3.4 and 'simulated' through manual drain voltage control (Figure 39). The same flat output power profile was observed over >6dB PBO.

Chapter 6 – Conclusions and Future Work

6.1 – Conclusions

This work has introduced the LMBA as a broadband amplifier architecture that is capable of drastic efficiency improvement over octave bandwidth. The active control nature of the architecture is capable of surpassing any matching impedance environment that is implemented using passive elements alone; used in conjunction with passive matching, drastic reductions in matching network size can be achieved along with the added benefit of reduced loss inherent with multi-section broadband matching networks.

It has been shown in this work, and surrounding publications, that the control scheme of an LMBA can be implemented and manipulated to suit the design application parameters.

The LMBA is capable of achieving broadband PBO ranges and efficiency profiles similar to conventional active load modulation structures such as Doherty and Chireix and has demonstrated that it can be practically implemented for next generation telecom applications [30].

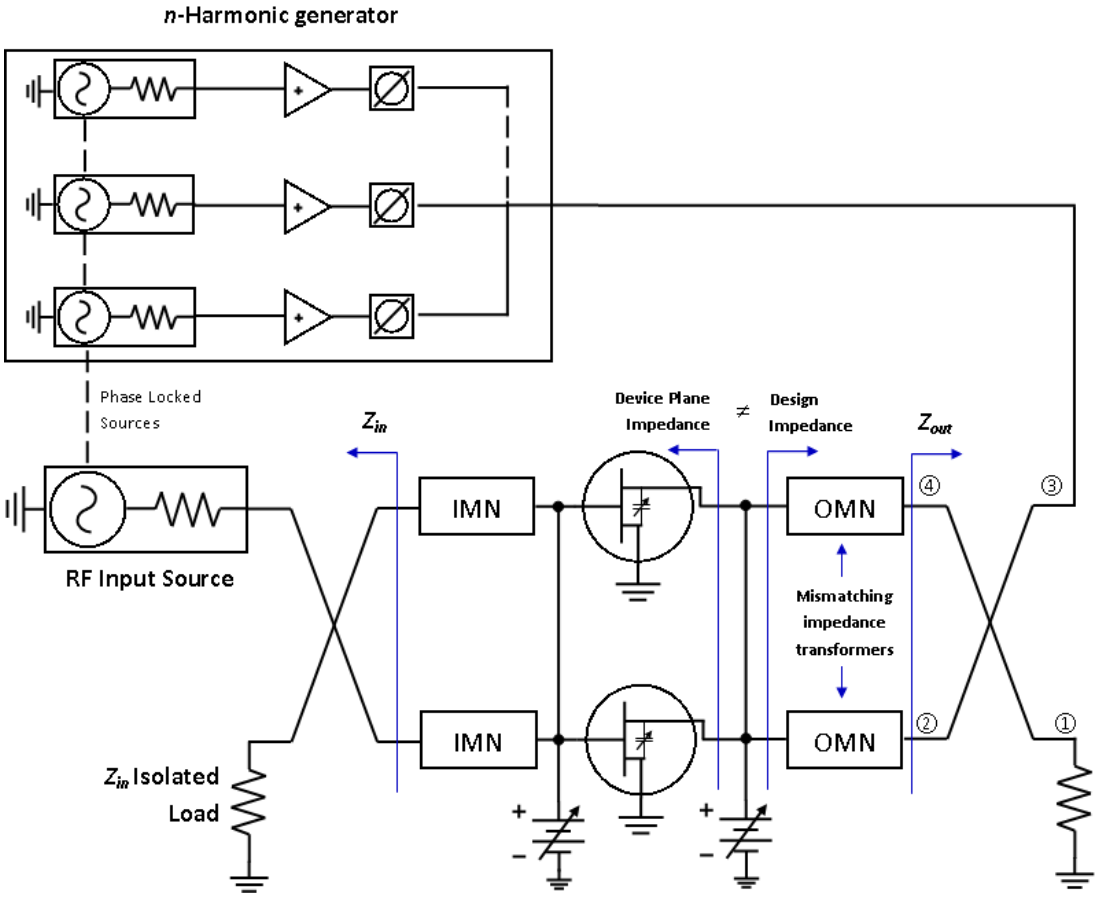
Further efficiency enhancement has been shown to be possible through the use of envelope tracking in this work and [29] showing that the LMBA

platform is capable of accommodating established concepts while providing significantly wider bandwidth than any other active modulation method.

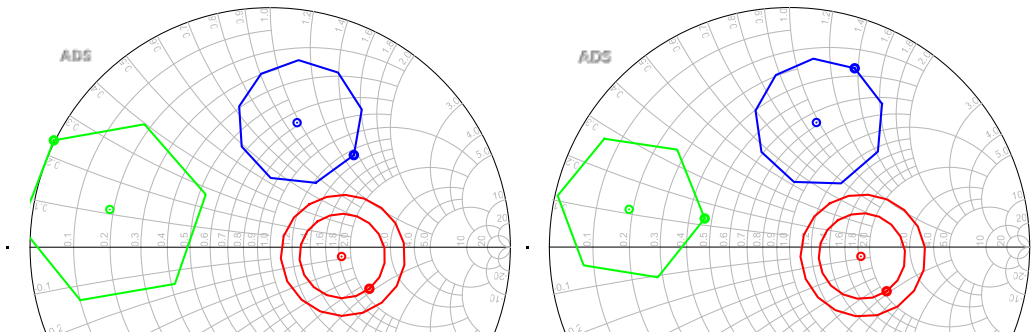
6.2 – Future Work

Although harmonic terminations have been overlooked for the most part in this work due to the broadband nature of the designs, it is suggested that future work looks at whether the LMBA can be used to improve the harmonic impedance environment to utilize high efficiency modes over octave+ bandwidth where multiple harmonics may be encapsulated within the operational bandwidth.

The theoretical isolation of impedance modulation between harmonics may be utilized in future work by providing passive matching networks that optimize for harmonic frequencies rather than the fundamental, whereby the load modulation capability of the LMBA is utilized to optimize the impedance of at the fundamental frequency. Inversely the fundamental match can be implemented using passive matching and the LMBA used to modulate the harmonic termination. As harmonic power is usually drastically lower than fundamental power, a smaller CSP device would be required which may alleviate some of the issue of system PAE when driver efficiency (or lack thereof) is taken into consideration.



(a)



(b)

Figure 52 – (a) Schematic representation of an LMBA system with 3 control signal sourced representing f_0, f_2 and f_3. (b)Large signal simulation showing the effect of independent modulation of fundamental (red), second harmonic (blue) and third harmonic (green). Two smith charts are provided showing the impedance intrinsic impedance seen by both devices in the balanced amplifier with an ideal infinite bandwidth quadrature coupler.

Figure 52b shows that the LMBA technique can be applied to harmonic frequencies with appropriate scaling of the α factor control signal. With an infinite bandwidth quadrature coupler, independent control of all harmonics can be achieved through relative phase and power offset of the CSP. One caveat to harmonic control however is that the phasing of the 2nd harmonic is 90° offset when comparing the impedance seen by each of the transistors in the balanced amplifier, extending to 3rd harmonic this offset becomes 180°.

Another caveat that can be seen in Figure 53 is that for a real coupler, with limited coupling bandwidth, if the harmonic lies out of the coupling bandwidth, modulation will only occur for the transistor this is connected to the through path as no energy is coupled to the coupled path.

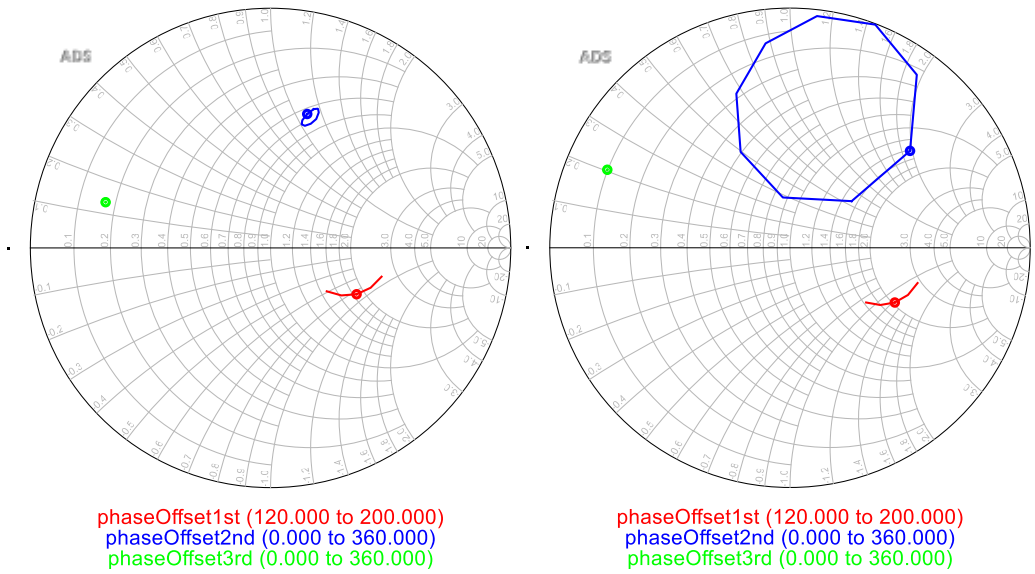


Figure 53 - 2nd harmonic modulation for a narrow band quadrature coupler where the 2nd harmonic is out of the coupling bandwidth.

Providing the classical shorted harmonic terminations for class AB, B may be impractical due to the modulation, α, factor required and the aforementioned

caveats. A closer look at class B/J terminations may yield the answer for harmonically tunable octave+ bandwidth designs.

Providing three separate control amplifiers may be impractical along with the required multiplexor, in practice the control amplifier will be a real amplifier which most likely will be operating in some other mode other than class A. The impact of harmonic generation from the control amplifier has largely been ignored to date but it may provide further insight into the control amplifier being used for optimization of fundament and harmonic impedances.

Lastly, the ideal current source assumption made in Chapter 2 could be expanded to evaluate the performance implications of transistor not being a perfect current generator that also has parasitics. The implications have been empirically shown in 3.3 without a solid grasp of the process that drives control power absorption.

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