Letters

Double-Thyristor-Based Protection for Valve-Side Single-Phase-to-Ground Faults in HB-MMC-Based Bipolar HVDC Systems

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***Abstract*—The valve-side single-phase-to-ground (SPG) faults in the half-bridge modular multilevel converter (HB-MMC)-based bipolar high-voltage direct-current (HVdc) systems induce some special fault consequences: overvoltage on the submodule (SM) capacitors in converter upper arms and nonzero-crossing currents in the grid-side ac circuit breaker (ACCB). In this letter, a protection strategy based on converter-embedded double-thyristors is proposed to address these issues. The double-thyristors are installed in parallel with each SM in the lower arms of the converter. By triggering the double-thyristors, the SPG fault is converted into a three-phase short-circuit that ensures current zero-crossings in the grid-side ACCB. Moreover, as the voltages of converter ac buses are clamped by the ground through the triggered double-thyristors, the upper arm overvoltage is mitigated. The effectiveness of the proposed protection strategy has been verified in a bipolar HB-MMC HVdc link built in PSCAD/EMTDC.**

***Index Terms*—Bipolar high-voltage direct-current (HVdc), double-thyristors, modular multilevel converter (MMC) protection, single-phase fault, valve-side fault.**

I. Introduction

THANKS to the extensive research and field applications in the past years, modular multilevel converter based high-voltage direct-current (MMC-HVdc) technology is getting mature and has been deployed in many projects including multiterminal HVdc networks [1], [2]. Currently, most of the commissioned MMC-HVdc projects are symmetrical monopoles [3]. With the increasing demand of bulk-power transmission and high reliability of power supply, there will be more applications using bipoles. However, bipolar MMC-HVdc exhibits some special technical issues. For instance, dc voltage offsets at the valve-side of the converter transformer and the severe consequences caused by the valve-side single-phase-to-ground (SPG) faults in half-bridge (HB) MMC-based systems [4], [5].

According to the studies in [6]–[8], the valve-side SPG faults in bipolar HB-MMCs will lead to grid-side nonzero-crossing currents and overvoltage of the submodule (SM) capacitors in converter upper arms. The grid-side ac circuit breaker (ACCB) may have difficulty in interrupting such nonzero-crossing fault currents [4], [5], [9]. The upper arm overvoltage may damage the SM capacitors and threaten the insulation of the converter.

To address the above problems, some solutions have been proposed in the literature. In [4] and [5], an auxiliary grounding ACCB is installed on the grid-side of the converter to create zero-crossings in the total currents in the grid-side ACCB. However, the three-phase-to-ground fault created by the auxiliary ACCB may aggravate the fault impact on the AC grid. Li *et al*. [8] employ an *LR* circuit as the dc-side grounding of the HB-MMC to create grid-side zero-crossing currents. However, a large reactance is needed to guarantee continuous current zero-crossings. Moreover, the application of the *LR* circuit will worsen the upper arm capacitor overvoltage and produce large disturbances on the healthy pole.

One mixed-SM MMC proposed in [6] uses full-bridge (FB) SMs in the upper arms and HB-SMs in the lower arms. Although this topology can mitigate the upper arm overvoltage, the grid-side nonzero-crossing currents still exist. Both FB-MMCs and the mixed-SM MMC (which uses HB-SMs in the upper arms and FB-SMs in the lower arms) proposed in [7] can eliminate the issue of grid-side nonzero-crossing currents [10]–[12]. However, the SM capacitors in the upper arms of them will still suffer severe overvoltage. Moreover, the capital cost and power losses of the above mixed-SM MMCs and FB-MMCs are much higher than HB-MMCs due to the additional application of insulated-gate bipolar transistors (IGBTs).

In this letter, SM embedded double-thyristors are employed to address the problems caused by valve-side SPG faults in bipolar

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HB-MMC HVdc systems. The double-thyristors are placed in parallel with each SM in converter lower arms. Current zero-crossings will quickly appear in grid-side ACCB due to the symmetrical short-circuit created by the triggered double-thyristors. Given that the ac bus voltages are clamped by the ground through the triggered double-thyristors, the upper arm capacitor overvoltage will be mitigated as well.

As single-bypass-thyristors have been widely employed in real industrial applications to protect the system upon dc faults [13], [14], adding one more thyristor to form double-thyristors may not be a technical problem and may not lead to a high increase of cost [15], [16]. In addition, the double-thyristors will not cause power losses during normal operation. Therefore, the proposed protection scheme is compact and cost-effective compared with other solutions.

II. Double-Thyristor-Based Protection Strategy

Fig. 1(a) shows a typical positive terminal in a bipolar HB-MMC station. Single-bypass-thyristors are installed in each SM. As a valve-side SPG fault is usually caused by the insulation failure of the wall bushing of converter ac buses, it is normally a permanent fault [7], [11]. Therefore, the converter should be blocked immediately once a valve-side SPG fault is detected. Fig. 1(b) illustrates the equivalent circuit and fault behavior of the blocked HB-MMC due to a valve-side SPG fault at phase A. u'_a, u'_b, and u'_c are valve-side post-fault voltages. i'_{ga}, i'_{gb}, and i'_{gc} are gird-side post-fault currents. The fault characteristics can be summarized as the following [8].

1) The voltages of all SM capacitors in the lower arms will remain constant when the converter is blocked.
2) The SM capacitors in the upper arm of the faulted phase will only be charged by the dc terminal transient overvoltage caused by the SPG fault.
3) The SM capacitors in the upper arms of the two nonfaulted phases will be charged during every negative half-cycle of the valve-side post-fault ac voltages. The maximum voltages that the SM capacitors can be charged are mainly determined by the parameters of the arm reactor and the leakage inductor of the converter transformer.
4) Due to the free-wheeling effect of diodes and the small resistance in the current paths, the currents flow through the lower arms in the two nonfaulted phases are always positive and have no zero-crossing. After the transformation of the transformer, the grid-side currents contain high dc components and exhibit no zero-crossing as well. There is a high risk that the grid-side ACCB cannot clear such fault currents and in fact might be damaged [4], [5], [9].

The above analysis is made based on the case that the converter station uses a dc side solid grounding. The fault behavior will exhibit some differences if the converter's dc side is grounded through a high impedance, for instance, in a rigid bipolar system. If the grounding resistor is very large (in mega-ohm or higher), nearly no fault current will flow through the lower arms. Therefore, the problem of grid-side nonzero-crossing currents will not exist. If the grounding resistor is not large enough

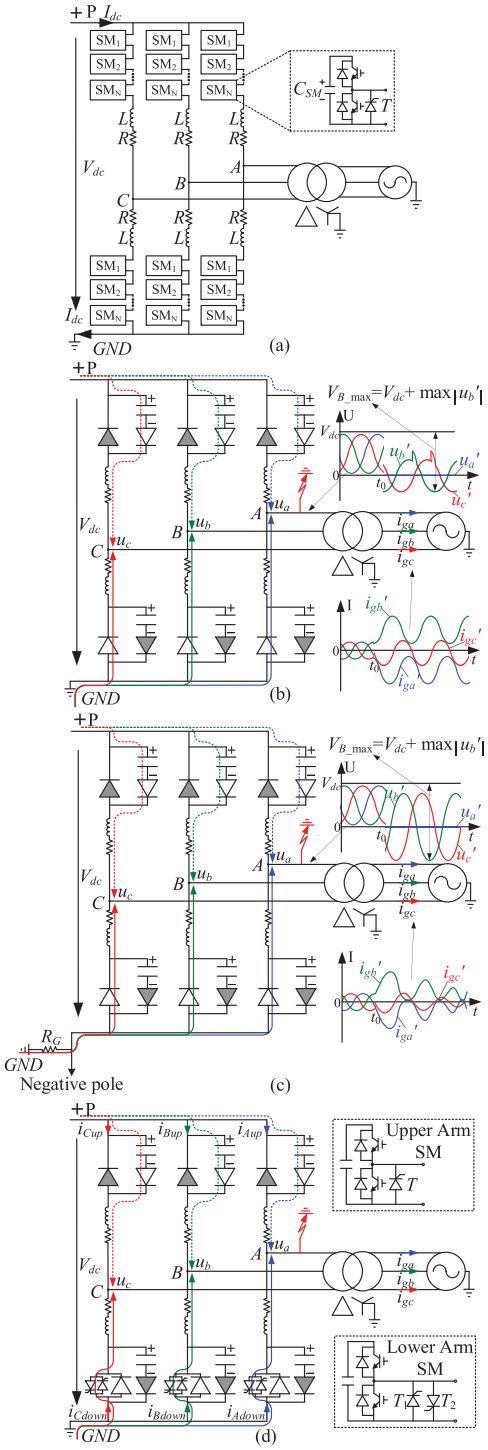

Fig. 1. Positive terminal of a bipolar HB-MMC. (a) Topology of the conventional HB-MMC. (b) Equivalent circuit of a blocked conventional HB-MMC. (c) Converter with a dc side high-impedance grounding. (d) Equivalent circuit of a blocked proposed converter.

(in kilo–ohm or lower), currents will flow through the grounding resistor and the lower arms. According to the analysis in [8], the dc components in the currents may be damped by the grounding resistor and grid-side current zero-crossings may appear, as shown in Fig. 1(c).

It can be concluded that the converter can be protected by the grid-side ACCB in bipolar systems with high-impedance dc groundings. However, due to the impedance of the dc grounding, the valve-side voltages are not directly clamped by the ground. Therefore, the postfault valve-side ac voltages in the two nonfaulted phases, as shown in Fig. 1(c), will be much higher than the system shown in Fig. 1(a). In this case, the upper arm overvoltage will be much more severe. Although the current nonzero-crossing problem may not occur in bipolar systems with dc-side high impedance groundings, this problem is still one of the most critical faults in bipolar systems with dc-side solid groundings. This letter focuses on addressing the current nonzero-crossing problem caused by valve-side SPG faults in bipolar HB-MMC systems with dc-side solid groundings.

Based on the aforementioned fault characteristics, a double-thyristor-based protection strategy is proposed in this letter. An additional thyristor T_2 is installed in the antiparallel position with the existing thyristor to form the double-thyristor SM in the three lower arms, as shown in Fig. 1(d). The three upper arms still use the conventional single-thyristor SM. It should be mentioned that the thyristor T_1 in the lower arms is under the same control as the upper arm thyristor T. Thyristors T and T_1 will be triggered together following the blocking of the IGBTs due to a dc fault. In other words, the application of the thyristor T_2 will not affect the conventional protection systems. The thyristor T_2 will only be triggered once a valve-side SPG fault has been detected.

All the thyristors T_2 in the three phases will be triggered to bypass all the three lower arms after the fault discrimination. Then the SPG fault is converted to a three-phase-to-ground short-circuit which eliminates the diode free-wheeling effect and, therefore, creates symmetrical components in grid-side ac currents and ensures current zero-crossings in the grid-side ACCB. It can be seen from Fig. 1(d) that the impedance of the SPG fault is bypassed by the created three-phase-to-ground short-circuit. The grid-side current zero-crossings will appear once the three-phase short-circuit is created. Therefore, the value of the fault impedance will not affect the effectiveness of the proposed solution to generate grid-side current zero-crossings. Although the created three-phase short-circuit may result in large fault currents in the double-thyristors, the inductor of the converter transformer and arm inductors will limit the fault currents which can also be handled by deploying thyristors with a high I^2t capacity. For instance, the press-pack thyristor can be utilized due to their excellent capability to withstand large surge currents [13].

As the valve-side SPG faults are normally permanent, the remote converter should be shut down immediately after the fault. The remote converter will be blocked based on either its local dc protection or a blocking signal received from the faulted converter through communications [17]. Then, the remote converter can switch to a static synchronous compensator mode when the SPG fault is fully isolated. The proposed protection strategy is summarized in Fig. 2.

A bipolar configuration consists of two independently controlled asymmetrical monopoles that features the monopolar operation mode in case of a failure in one pole. The proposed

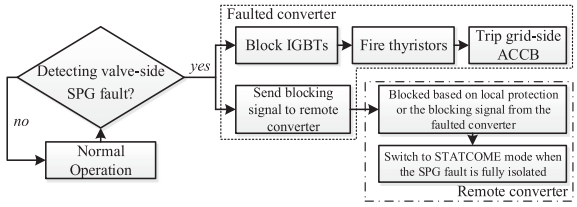

Fig. 2. Block diagram of the proposed protection strategy.

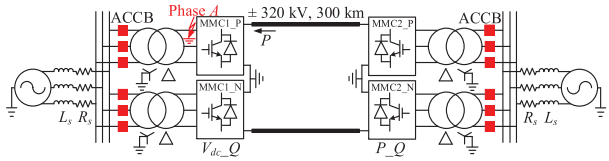

Fig. 3. Typical HB-MMC based bipolar HVdc link.

TABLE I
PARAMETERS OF THE HVDC LINK

Parameters	Values	Parameters	Values
Capacity of each pole	500 MW	DC terminal inductor	0.1 H
Rated dc voltage	320 kV	SM capacitance	2.5 mF
Rated ac voltage	230 kV	Arm inductance L	0.02 H
Transformer ratio	200/230	Arm resistance R	0.1 Ω
Transformer leakage reactance	0.10 p.u.	AC system equivalent resistance R_S	0.52637 Ω
Number of SMs in each arm	10	AC system equivalent reactor L_S	0.01675 H

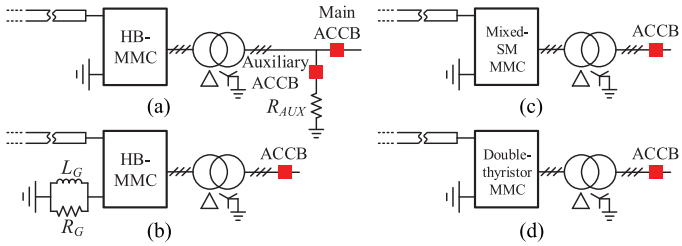

Fig. 4. Arrangements of the four studied protection methods. (a) Auxiliary ACCB-based method. (b) *LR* circuit based method. (c) Mixed-SM MMC based method. (d) Double-thyristor based method.

double-thyristors are installed in all lower arms of the MMCs in both poles. Therefore, after the clearance of the valve-side SPG fault in the faulted pole, the remaining asymmetrical monopole will be able to keep operating and the proposed protection method will be able to protect another valve-side SPG fault in the remaining pole. Moreover, differing from the protection methods in [5] and [8], the proposed solution in this letter will almost not affect the operation on the healthy pole during the fault clearing process. This is another advantage of the proposed solution and will be further discussed in the next session.

III. Case Study

A. System Modeling

The double-thyristor-based protection strategy has been applied in a bipolar HB-MMC link built in PSCAD/EMTDC, as

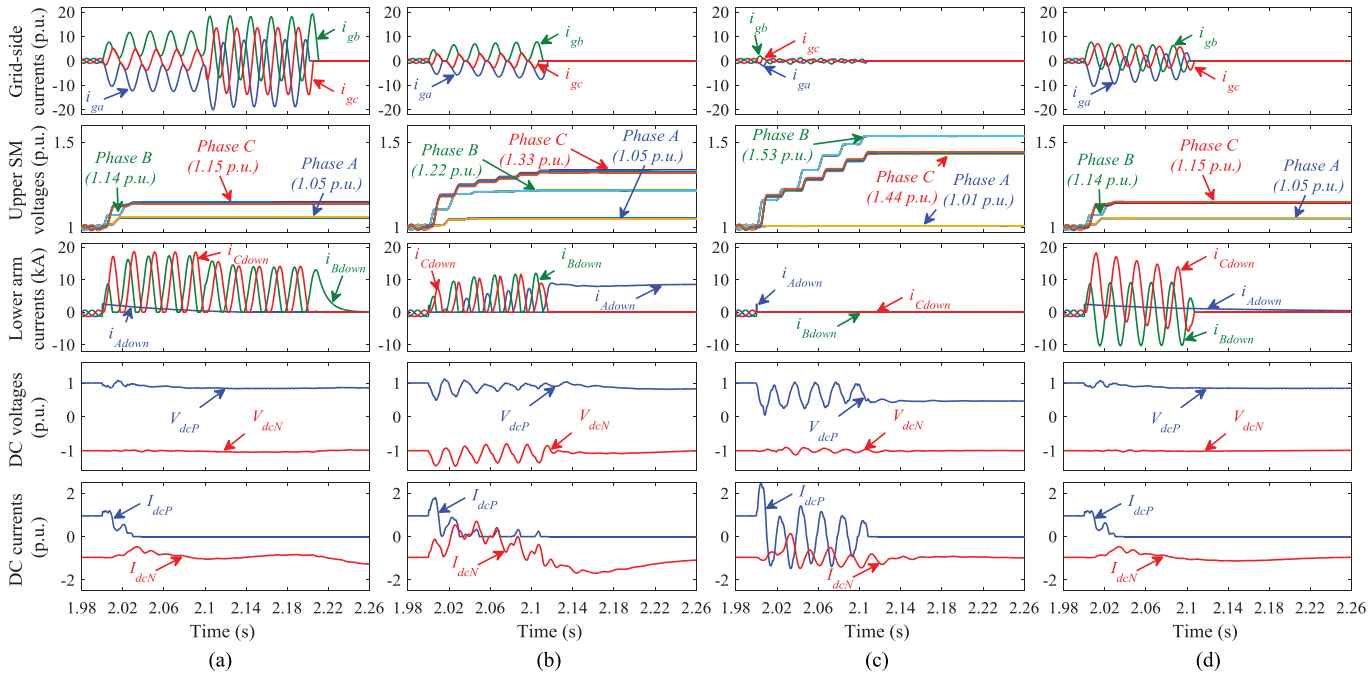

Fig. 5. Results of employing the four studied protection methods. (a) Auxiliary ACCB based method. (b) *LR* circuit based method. (c) Mixed-SM MMC based method. (d) Double-thyristor based method.

shown in Fig. 3. System parameters are given in Table I. The HVdc cable model is taken from [18].

To verify the effectiveness of the proposed strategy in creating grid-side current zero-crossings, the results are compared with the methods presented in Section I: the auxiliary ACCB based method [4], the *LR* circuit based method [8], and the mixed-SM MMC-based method [7]. The arrangements of the four studied protection methods are shown in Fig. 4. To ensure the occurrence of grid-side current zero-crossings, the auxiliary resistor R_{AUX} in Fig. 4(a) has been set as 5 Ω. The L_G and R_G in Fig. 4(b) have been increased to 0.55 H and 20 Ω to ensure the grid-side current zero-crossings can last longer than 100 ms. The mixed-SM MMC in Fig. 4(c) uses HB-SMs in the upper arms and FB-SMs in the lower arms.

A valve-side SPG fault is set at phase *A* of the positive terminal (MMC1_P) of the station controlling V_{dc} and Q. The converter receives 1 p.u. power from the remote terminal in the prefault condition. In order to verify the effectiveness of the proposed strategy under the worst case, a small fault resistor with a resistance of 0.01 Ω is applied. The fault occurs at $t = 2$ s. The faulted converter is blocked if any arm current exceeds 2.5 kA. At the same time, a tripping signal is sent to the remote converter. The double-thyristors are triggered by 0.5 ms after blocking the converter. The delay is to emulate the time to discriminate the SPG fault. The three-phase short-circuit will be created immediately as long as the double-thyristors are triggered. Moreover, as the fault discrimination time (within a millisecond) is much shorter than the opening time (in tens milliseconds) of the grid-side ACCB. Therefore, the time delay will not affect the effectiveness of generating the grid-side current zero-crossing and the opening of the grid-side ACCB. A 100 ms delay is used to emulate the operating time of ACCBs. The remote converter is blocked based on either the blocking signal sent from the faulted converter (a 5 ms delay is used to emulate the communication delay) or its local protection (either any arm current exceeds 2.5 kA or the DCa terminal voltage is less than 0.8 p.u. or higher than 1.2 p.u.).

B. Simulations and Analysis

It can be seen from the simulation results shown in Fig. 5 that all of the methods can ensure the occurrence of grid-side current zero-crossings. However, the auxiliary ACCB based method takes a longer time as the main ACCB needs to be opened after the close of the auxiliary ACCB to ensure it can be opened under current zero-crossings. The grid-side overcurrents of the proposed method are lower than the auxiliary ACCB based method and the *LR* circuit based method. Although the mixed-SM MMC-based method does not lead to overcurrent because the current path is blocked by the lower arm FB-SMs, the severe upper arm overvoltage and high cost are the main limitations of this method. It is illustrated that the upper arm SM capacitor overvoltage in the proposed method has been limited to less than 1.15 p.u. [as shown in Fig. 5(d)] which is much lower than the *LR* circuit based method [1.33 p.u. as shown in Fig. 5(b)] and the mixed-SM MMC-based method [1.53 p.u. as shown in Fig. 5(c)].

Although the lower arm currents in the proposed method are larger than the other methods, it can be handled by selecting thyristors with suitable I^2t capacity. In addition, in the *LR* circuit based method, the large (over 8 kA) residual current i_{Adwon} in the lower arm of the faulted phase takes a long time to naturally decay to zero, which may lead to severe overtemperature of the single-bypass-thyristors used to protect diodes. Such a large

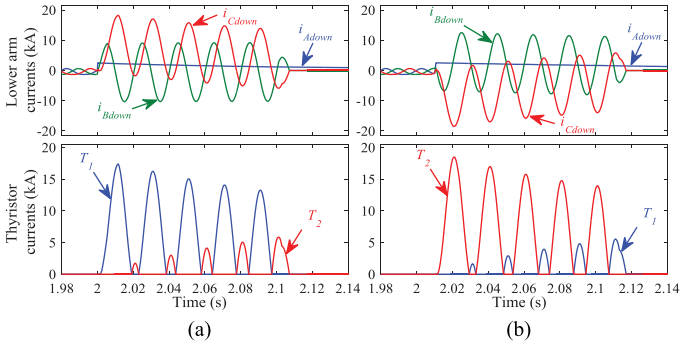

Fig. 6. Currents in the lower arms and in the double-thyristors in phase *C*. (a) Fault occurs at $t = 2.00$ s. (b) Fault occurs at $t = 2.01$ s.

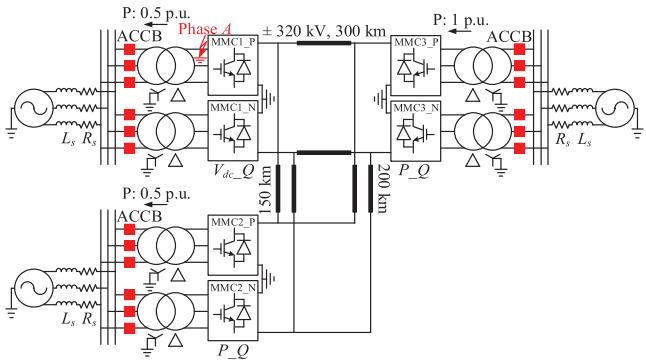

Fig. 7. Three-terminal HB-MMC-based bipolar HVdc grid.

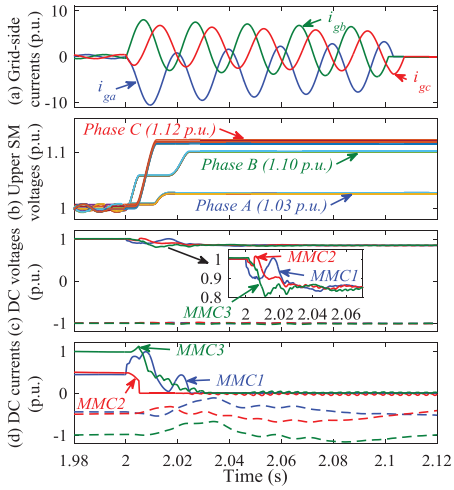

Fig. 8. System responses of the three-terminal dc grid. (a) Grid-side ac currents of the faulted MMC. (b) Upper arm SM voltages of the faulted MMC. (c) DC terminal voltages of each converter (solid lines for the positive pole and dash lines for the negative pole). (d) DC terminal current of each converter (solid lines for the positive pole and dash lines for the negative pole).

residual current is caused by the large L in the LR circuit. In contrast, the residual current i_{Adown} is much lower (2.52 kA) in the proposed method and can decay to zero quickly.

Moreover, it can be seen from the dc voltages and currents shown in Fig. 5 that the healthy pole in the LR circuit based method and the mixed-SM MMC-based method experience large disturbances before the fault clearance. The healthy pole in the auxiliary ACCB based method is also disturbed due to the grid-side three-phase short-circuit created by the auxiliary ACCB and it takes longer time than the proposed method to recover to the steady-state. In a word, the proposed method results in the least impact on the healthy pole compared to the other methods.

It should be mentioned that the time when the fault occurs may affect the behavior of fault currents, for instance, the initial sign (positive or negative) of the fault currents. Fig. 6 depicts the currents in the three lower arms and the two thyristors (T_1 and T_2) in phase C when the SPG fault occurs at two different times ($t = 2.00$ s and $t = 2.01$ s). It can be seen that the initial fault currents can be either positive or negative after the fault. Both T_1 and T_2 may experience the maximum fault current. Therefore, the parameters of the two thyristors in each SM should be the same and consider the maximum fault currents. Moreover, as the three phases are symmetrical and a fault can randomly occur in any phase, the maximum fault current can appear in any phase. Therefore, the parameters of the used thyristors in the three phases should be the same as well.

To verify the effectiveness of the proposed method in MTDC grids, a three-terminal meshed dc grid is built in PSCAD, as shown in Fig. 7. The system parameters are the same as the system shown in Fig. 3. MMC1 regulates the dc voltage and MMC2 and MMC3 controls the power. The proposed protection method is deployed at MMC1. The strategies and criteria of the local protection for MMC2 and MMC3 are the same as the last case. The valve-side SPG fault occurs at $t = 2$ s at the positive pole of MMC1. Before the fault, MMC3 sends 1 p.u. active power and MMC1 and MMC2 receive 0.5 p.u. each.

It can be seen from the simulation results shown in Fig. 8(a) and (b) that the faulted MMC is effectively protected by the proposed method. Fig. 8(c) and (d) illustrate the dc terminal voltages and dc current of each converter. It can be seen that the dc voltages and currents of the two remote MMCs do not reach the thresholds of their local protections. Therefore, they are blocked based on the blocking signal sent from the faulted converter. The converters in the negative pole experience disturbances during the fault clearing process, however, they recover quickly after clearing the fault.

IV. Conclusion

In this letter, a converter embedded double-thyristor-based protection strategy was proposed to address the problems caused by valve-side SPG faults in bipolar HB-MMC HVdc systems. The proposed protection strategy, which was verified through simulations conducted in PSCAD/EMTDC, could effectively mitigate the upper arm overvoltage and create grid-side current zero-crossings. Moreover, the proposed method presented great advantages compared with other methods: no further aggravation of upper arm overvoltage, no more occupation of converter station footprint, no impact on the healthy pole, and no risk of overtemperature of thyristors due to the lower arm residual current.

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