Reduction of DC-link Ripples for SiC-based Three-phase Four-wire Inverters with Unbalanced Loads

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***Abstract*—Three-phase inverters are widely used in the smart grid to integrate renewable energy resources. When the inverters are used to feed the unbalanced three-phase loads, the three-phase four-wire inverters are usually required to provide the current path for neutral currents. However, unbalanced loads will cause undesirable second-order ripples on DC bus. Conventional three-phase four-wire inverters with neutral legs can not address this challenge. Bulky capacitors or extra active circuits are still required to reduce the ripples. This inevitably leads to increased size and cost of the system. Although SiC-based converters have the advantage of achieving high power density, the DC-bus capacitance can not be reduced by simply replacing Si IGBTs with SiC MOSFETs. In this paper, a new topology of SiC-based three-phase four-wire inverters is proposed to reduce the DC-bus ripples without adding any additional hardware components. With the reduction of DC-bus ripples, the DC-bus capacitance can be reduced to achieve high power density. The equivalent circuit is analyzed and the control strategy for the proposed topology is designed. The proposed topology is built in Matlab/Simulink and simulation results are presented to verify the proposed topology.**

I. Introduction

In mordern smart grids, three-phase inverters play an important role in the integration of renewable energy resources such as solar PVs and wind turbines, etc. In electricity distribution networks, when the inverters are used to feed the unbalanced three-phase loads, three-phase four-wire inverters are usually required to provide the current path for zero-sequence currents, i.e., the neutral current.

There are two main challenges in the three-phase four-wire inverters supplying unbalanced loads: a) providing neutral currents required by unbalanced loads [1][2]; b) reducing the second-order ripples on the DC bus [3].

There are various topologies of three-phase four-wire inverters proposed in the literature focusing on providing the neutral current [4]. A popular solution is adopting an independently-controlled neutral leg [5] as shown in Fig. 1. In this topology, the neutral leg can provide the neutral current to the loads and also balance the voltages of the DC-bus capacitors. Besides, this topology can achieve independent control of the three-phase legs and attenuate the electromagnetic interference (EMI) problems [6].

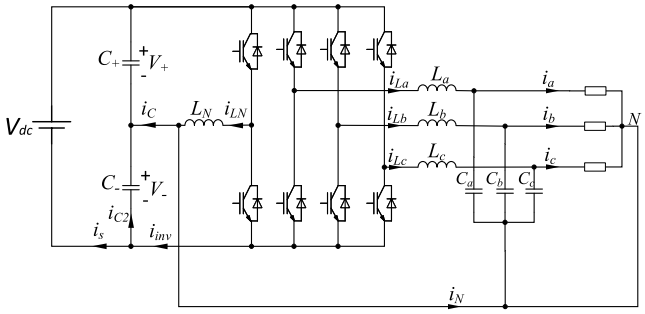

Figure 1. A conventional topology of three-phase four-wire inverters

However, another challenge, i.e. the second-order ripples on the DC bus, can not be addressed by this neutral leg. Bulky and vulnerable DC electrolytic capacitors must then be used to reduce the ripples, which is undesirable for a converter to achieve high power density [7].

To reduce the second-order ripples and capacitance in the DC bus, many active power decoupling solutions have been proposed [8]. Although some solutions are proposed for single-phase converters, they can also be applied to three-phase converters. These solutions need extra active circuits to store the ripple energy so that the ripple energy flowing through the DC bus can be reduced or even completely eliminated [9]. However, the extra active switches and other components will increase the cost of the system.

SiC MOSFETs have the advantages of higher efficiency and higher switching frequency comparing to the Si counterparts. Therefore, the size of filter components and the heat sink can be significantly reduced for the SiC-based converters to achieve high power density [10]. However, the bulky DC-bus capacitors can not be reduced by simply using SiC MOSFETs.

In this paper, a topology of three-phase four-wire inverters is proposed to solve both challenges without adding additional hardware components. By constructing an additional conduction path between the DC bus and the filter capacitors, the DC-bus ripples are reduced without adding any components. The neutral leg is used in the topology not only to provide neutral currents but also to compensate the harmonics in the load

currents. The equivalent circuit is analyzed and the control strategy for the proposed topology is designed. The proposed topology is built in Matlab/Simulink and simulation results are presented to verify the proposed topology.

II. Analysis of DC Voltage Ripples under Unbalanced Conditions

For a three-phase four-wire inverter with unbalanced loads as shown in Fig. 1, the three-phase output voltages are balanced, but the currents are unbalanced due to unbalanced loads. Hence, the three-phase voltages and currents can be written as:

$$\begin{cases} v_a = V\sin(\omega t) \\ v_b = V\sin(\omega t - 120^\circ) \\ v_c = V\sin(\omega t + 120^\circ) \end{cases} \tag{1}$$

$$\begin{cases} i_a = I_a\sin(\omega t + \varphi_{ia}) \\ i_b = I_b\sin(\omega t + \varphi_{ib}) \\ i_c = I_c\sin(\omega t + \varphi_{ic}) \end{cases} \tag{2}$$

The instantaneous power of each single phase can be calculated as:

$$p_a = v_{ga}i_{ga} = \frac{1}{2}VI_a\left[\cos(\varphi_{ia}) - \cos(2\omega t + \varphi_{ia})\right] \tag{3}$$

$$p_b = \frac{1}{2}VI_b\left[\cos(120^\circ + \varphi_{ib}) - \cos(2\omega t - 120^\circ + \varphi_{ib})\right] \tag{4}$$

$$p_c = \frac{1}{2}VI_c\left[\cos(120^\circ - \varphi_{ic}) - \cos(2\omega t + 120^\circ + \varphi_{ic})\right] \tag{5}$$

Based on the principle of power balance, the instantaneous power of the DC bus can be calculated as:

$$p_{dc} = p_{ac} = p_a + p_b + p_c = P_0 + P_{2\omega}\cos(2\omega t + \phi) \tag{6}$$

where

$$\begin{aligned} P_0 = {} & \frac{1}{2}VI_a\cos(\varphi_{ia}) + \frac{1}{2}VI_b\cos(120^\circ + \varphi_{ib}) \\ & + \frac{1}{2}VI_c\cos(120^\circ - \varphi_{ic}) \end{aligned} \tag{7}$$

$$\begin{aligned} P_{2\omega}\cos(2\omega t + \phi) = -\frac{1}{2}\big[& VI_a\cos(2\omega t + \varphi_{ia}) \\ & + VI_b\cos(2\omega t - 120^\circ + \varphi_{ib}) \\ & + VI_c\cos(2\omega t + 120^\circ + \varphi_{ic})\big] \end{aligned} \tag{8}$$

It can be seen from (6) that the instantaneous power of the DC bus contains the second-order power ripple due to the unbalanced load currents.

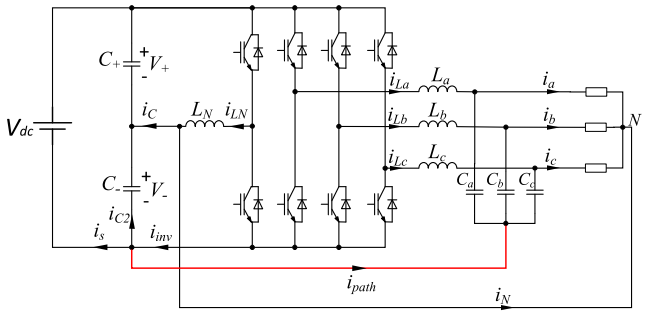

Figure 2. Proposed control diagram

III. Proposed Solution to Reduce DC-bus Ripples

A. Proposed Topology

Fig. 2 shows the proposed topology to reduce DC-bus ripples for three-phase four-wire inverters under unbalanced load condition. In the proposed topology, the common point of filter capacitors is connected to the negative pole of the DC bus instead of the midpoint of DC bus in the conventional topology. Besides, a neutral leg is adopted in the proposed topology. The neutral leg is commonly used in the conventional three-phase four-wire converter to provide neutral currents and balance the voltages on the split capacitors of DC bus. However, in the proposed topology, the neutral leg is also used to inject second-order harmonics to the DC bus capacitors so that the second-order ripples caused by unbalance load currents can be absorbed by the filters capacitors without affecting the output power quality. In this way, the ripples on the DC bus are reduced without adding any hardware components.

Due to the unbalanced load currents, there is second-order power ripple flowing through the inverter. Therefore, the inverter current i_{inv} contains second-order harmonics. In the conventional three-phase four-wire converter in Fig. 1, the harmonics can only flow into the DC source and DC capacitors, causing second-order voltage and current ripples on the DC bus. However, in the proposed topology, by connecting the common point of filter capacitors to the negative pole of DC bus, another current path is created as shown in Fig. 2 . According to Kirchhoff's law,

$$i_{inv} = i_s + i_{C2} + i_{path} \tag{9}$$

According to (9), with proper control strategy, the harmonics current can flow through the added conduction path between the negative pole of DC bus and the common point of filter capacitors. In this way, the second-order power ripple can be stored into the filter capacitors and there will be no ripples on the DC bus.

B. Equivalent Circuit Analysis

Fig. 3 shows the equivalent circuit of the proposed topology under unbalanced load condition. The voltage drop on the filter inductors is neglected during the anaylsis for simplification. In order to absorb the second-order ripples by filter capacitors,

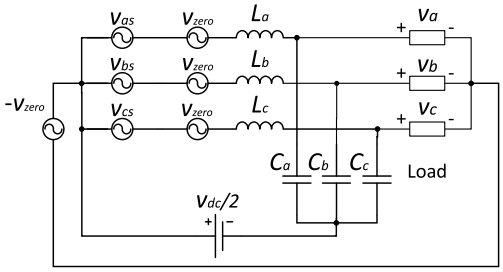

Figure 3. Equivalent circuit of the proposed topology

a second-order zero-sequence compensation voltage should be applied to the filter capacitors. The voltages on the filter capacitors can be written as

$$\begin{cases} v_{Ca} = v_a + \frac{1}{2}V_{dc} + v_{zero} \\ v_{Cb} = v_b + \frac{1}{2}V_{dc} + v_{zero} \\ v_{Cc} = v_c + \frac{1}{2}V_{dc} + v_{zero} \end{cases} \tag{10}$$

$$v_{zero} = V_{2\omega}\sin\left(2\omega t + \delta_{2\omega}\right) \tag{11}$$

where v_a, v_b and v_c are balanced load voltages as shown in (1); $\frac{1}{2}V_{dc}$ is added to the voltages of filter capacitors because the common point of the filter capacitors is connected to the negative pole of DC bus. v_{zero} is the second-order zero-sequence compensation voltage generated by the inverter to divert the second-order ripples to filter capacitors. However, in order to get sinusoidal output voltages and currents on the loads, the negative compensation voltage $-v_{zero}$ should be added to the midpoint of DC bus by the neutral leg to cancel the zero-sequence voltage compensated by the inverter. In this way, the zero-sequence voltage v_{zero} will only be added to the filter capacitors without affecting the power quality on the load.

According to (10), the currents of filter capacitors can be calculated as

$$\begin{cases} i_{Ca} = \omega C_a V\cos\left(\omega t\right) + i_{zero} \\ i_{Cb} = \omega C_b V\cos\left(\omega t - 120^\circ\right) + i_{zero} \\ i_{Cc} = \omega C_c V\cos\left(\omega t + 120^\circ\right) + i_{zero} \end{cases} \tag{12}$$

$$i_{zero} = 2\omega C_f V_{2\omega}\cos\left(2\omega t + \delta_{2\omega}\right) \tag{13}$$

where

$$C_a = C_b = C_c = C_f \tag{14}$$

According to (10) and (12), the instantaneous power of the filter capacitors can be summed up as

$$\begin{aligned} p_{Cf} &= v_{Ca}i_{Ca} + v_{Cb}i_{Cb} + v_{Cc}i_{Cc} \\ &= p_{Cf\_2\omega} + p_{Cf\_4\omega} \end{aligned} \tag{15}$$

where

$$p_{Cf\_2\omega} = 3\omega C_f V_{2\omega} V_{dc}\cos\left(2\omega t + \delta_{2\omega}\right) \tag{16}$$

$$p_{Cf\_4\omega} = 3\omega C_f V_{2\omega}^2\sin\left(4\omega t + 2\delta_{2\omega}\right) \tag{17}$$

Therefore, by adding a proper value of v_{zero} to filter capacitors, the $p_{Cf\_2\omega}$ in (16) can be equal to the second-order ripple component in (8). Accordingly, the magnitude and phase angle uof v_{zero} can be calculated as:

$$\begin{cases} V_{2\omega} = \frac{P_{2\omega}}{3\omega C_f V_{dc}} \\ \delta_{2\omega} = \phi + \pi \end{cases} \tag{18}$$

In this way, the second-order ripples caused by unbalanced loads can be absorbed by filter capacitors. In other words, there is no second-order ripples flowing into DC bus. However, as can be seen in (15), another 4^{th}-order ripple component is introduced by the zero-sequence voltage, which will be transferred to DC bus and cause 4^{th}-order ripples on DC bus. It can be seen that the ratio between the 4^{th}-order ripple and second-order ripple is

$$\frac{p_{Cf\_4\omega}}{p_{Cf\_2\omega}} = \frac{V_{2\omega}}{V_{dc}} < 0.1 \tag{19}$$

The ratio between $V_{2\omega}$ and V_{dc} is determined by the unbalanced ratio of load currents. Generally, $V_{2\omega}$ is no more than 1/10 of V_{dc}. Therefore, although the 4^{th}-order ripples are induced by the proposed method, the total ripples on DC bus are still reduced. On the other hand, in order to further reduce the 4^{th}-order ripples on DC bus, a 4^{th}-order compensation voltage can be further added. The compensated zero-sequence voltage can be rewritten as

$$v_{zero} = V_{2\omega}\sin(2\omega t + \delta_{2\omega}) + V_{4\omega}\sin\left(4\omega t + \delta_{4\omega}\right) \tag{20}$$

where the 4^{th}-order component is used to eliminate the 4^{th}-order ripples in (15).

The instantaneous power in the filter capacitors can be calculated as

$$\begin{aligned} p_{Cf} &= v_{Ca}i_{Ca} + v_{Cb}i_{Cb} + v_{Cc}i_{Cc} \\ &= p_{Cf\_2\omega} + p_{Cf\_4\omega} + p_{Cf\_6\omega} + p_{Cf\_8\omega} \end{aligned} \tag{21}$$

where

$$\begin{aligned} p_{Cf\_2\omega} &= 3\omega C_f V_{2\omega} V_{dc}\cos\left(2\omega t + \delta_{2\omega}\right) \\ &\quad + 3\omega C_f V_{2\omega} V_{4\omega}\sin\left(2\omega t - \delta_{2\omega} + \delta_{4\omega}\right) \end{aligned} \tag{22}$$

$$\begin{aligned} p_{Cf\_4\omega} &= 3\omega C_f V_{2\omega}^2\sin\left(4\omega t + 2\delta_{2\omega}\right) \\ &\quad + 6\omega C_f V_{4\omega} V_{dc}\cos\left(4\omega t + \delta_{4\omega}\right) \end{aligned} \tag{23}$$

$$p_{Cf\_6\omega} = 3\omega C_f V_{2\omega} V_{4\omega}\sin\left(6\omega t + \delta_{2\omega} + \delta_{4\omega}\right) \tag{24}$$

$$p_{Cf\_8\omega} = 6\omega C_f V_{4\omega}^2\sin\left(8\omega t + 2\delta_{4\omega}\right) \tag{25}$$

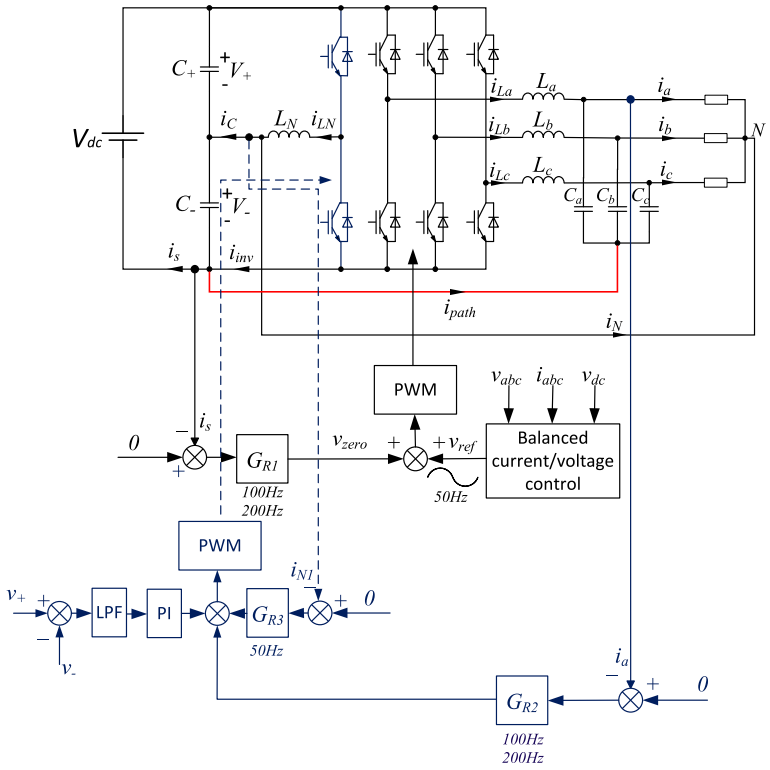

Figure 4. Proposed control diagram

According to (23), to eliminate the 4^{th}-order ripples, the added 4^{th}-order zero-sequence voltage should satisfy:

$$\begin{cases} V_{4\omega} = \frac{V_{2\omega}^2}{2V_{dc}} \\ \delta_{4\omega} = 2\delta_{2\omega} + \frac{\pi}{2} \end{cases} \tag{26}$$

At the same time, the $p_{Cf\_2\omega}$ in (22) should be equal to the ripple component in (8) by choosing the magnitude and phase angle of the second-order zero-sequence voltage properly. By substituting (8) and (26) into (22), the following equation can be obtained:

$$3\omega C_f V_{2\omega} V_{dc} \left[1 + \frac{V_{2\omega}^2}{2V_{dc}^2}\right] \cos(2\omega t + \delta_{2\omega}) + P_{2\omega} \cos(2\omega t + \phi) = 0 \tag{27}$$

where $\frac{V_{2\omega}^2}{2V_{dc}^2} \ll 1$, so the magnitude of the 2^{nd}-order component of v_{zero} can be approximately calculated as:

$$\begin{cases} V_{2\omega} \approx \frac{P_{2\omega}}{3\omega C_f V_{dc}} \\ \delta_{2\omega} = \phi + \pi \end{cases} \tag{28}$$

It can be seen from (21) that in order to eliminate the 4^{th}-order power ripple, the 6^{th}-order and 8^{th}-order ripples are induced by the proposed method. However, the magnitude of ripples is futher reduced. According to (19) and (26), the magnitudes of the 6^{th}-order and 8^{th}-order ripples are generally around 1% and $1‰$ of the original second-order ripples respectively.

According to the above analysis of the equivalent circuit, by adding zero-sequence voltage on the inverter output, the second-order ripples can be absorbed by the filter capacitors so that the ripples on DC bus are reduced. Proper control strategy should be proposed to realize this function. It should be highlighted that no matter what kind of zero-sequence voltage is added on the inverter output, a negative compensation voltage should be added on the midpoint of DC capacitors accordingly so that the sinusoidal voltages on the load are not affected. This negative compensation voltage is realized by the proposed control strategy of the neutral leg.

C. Proposed Control Strategy

The proposed control strategy is shown in Fig. 4, which consists of two parts. The first part is the closed-loop control of the inverter. The second part is the control of the neutral leg. It is worth mentioning that the two parts of the control work independently, which is beneficial to the system stability.

In the closed-loop control of the inverter, the DC source current i_s is measured as the feedback. A resonant controller is applied. The input of the resonant controller is the deviation between 0 and i_s. The output of the resonant controller is the zero-sequence compensation voltage. The zero-sequence voltage is added on the sinusoidal voltage and generated by the PWM operation of the inverter. The closed-loop control of three-phase voltages and currents of the inverter is not the main focus of this paper and is not discussed in detail. As is discussed in Section III-B, in order to eliminiate both 2^{nd}-order and 4^{th}-order harmonics in the DC bus, the compensated

zero-sequence voltage need to contain 2^{nd}-order and 4^{th}-order components. Therefore, the resonant controller has two resonant frequency at 100 Hz and 200 Hz respectively, assuming that the fundamental frequency is 50 Hz:

$$G_{R1} = \sum_{h=2,4} \frac{2\xi_h h\omega s}{s^2 + 2\xi_n h\omega s + (h\omega)^2} \times K_h \tag{29}$$

where ω is the fundamental frequence; K_h is the gain of resonant controller, which need to be tuned in practice. In this way, the 2^{nd}-order and 4^{th}-order harmonics in i_s are controlled to be zero. The second-order ripples caused by unbalanced loads will flow into the filter capacitors.

In order to get sinusoidal voltages on the load, the zero-sequence voltage compensated by the inverter should not appear on the load. Therefore, a negative compensation voltage is generated by the neutral leg to cancel the zero-sequence voltage as shown in the equivalent circuit in Fig. 3. The control of the neutral leg also consists of two parts.

The first part is to control the neutral leg to balance the voltages of two capacitors on DC bus and provide neutral currents at 50 Hz to the unbalanced loads. A PI controller is applied to balance the voltages of two capacitors and a resonant controller at 50 Hz is applied to provide neutral currents to unbalanced loads.

The second part of the controller is to generate a negative compensation voltage to cancel the zero-sequence voltage. The phase current on Phase a is detected as feedback to a resonant controller. By controlling the 2^{nd}-order and 4^{th}-order harmonics in the current of phase a to zero, the negative compensation voltage is generated by the neutral leg to cancel the zero-sequence voltage. Either the phase current or the phase voltage of any phase can be used as the feedback. Also, this resonant controller has two resonant frequency at 100 Hz and 200 Hz to fully eliminate the zero-sequence 2^{nd}-order and 4^{th}-order voltages.

It can be seen that the proposed controllers for the inverter and the neutral leg are independent to each other. This will allow to tune the two controllers independently and easily.

IV. Selection of Filter Capacitors

As shown in (28), the magnitude of second-order zero-sequence voltage is proportional to $P_{2\omega}$ and inversely proportional to C_f. Therefore, for a set amount of second-order ripples, if the smaller filter capacitors are selected, a larger zero-sequence conpensation voltage should be provided by the inverter. Futhermore, this zero-sequence voltage will increase the minimum requirement of DC voltage, which increases the voltage stress of semiconductors and brings to low DC-bus voltage utilization. On the other hand, larger filter capacitors may cause large undesirable reactive power, which will increase the converter losses.

For three-phase four-wire converters under balanced condition, the minimum requirement of DC voltage can be calculated as:

$$V_{dc\_min} = 2\sqrt{2}V_{rms\_phase} \tag{30}$$

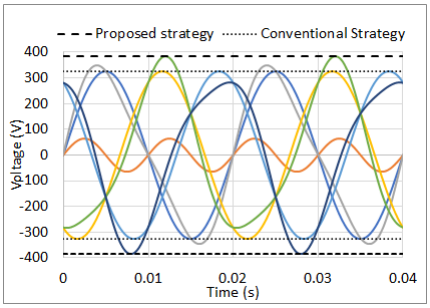

Figure 5. Capacitor voltages and minimum DC voltage required in proposed topology and conventional topology

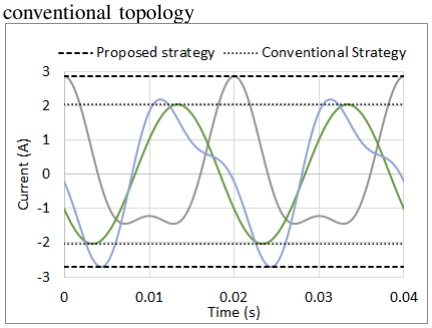

Figure 6. Current stress of converter in proposed topology and conventional topology

where V_{rms_phase} is the RMS value of phase voltage. In 400V distribution network in UK, $V_{rms\_phase} = 230V$, so $V_{dc\_min} = 650V$.

For three-phase four-wire converters under unbalanced condition, if the proposed strategy is used, the inverter should output not only the three-phase load voltages, but also the zero-sequence voltage. Considering the worst scenario, The minimum requirement of DC voltage should be

$$V_{dc\_min} = 2\sqrt{2}V_{rms\_phase} + 2V_{2\omega} \tag{31}$$

where the 4^{th}-order zero-sequence voltage is neglected because is the far smaller than $V_{2\omega}$.

In (31), the minimum DC bus voltage is determined by the compensated zero-sequence voltage $V_{2\omega}$. According to (28), $V_{2\omega}$ is determined by unbalanced power ripples $P_{2\omega}$ and the capacitance of filter capacitors C_f. Therefore, in practice, the maximum allowable unbalanced power ripples in the system should be firstly attained. Then the capacitance of filter capacitors can be selected to determine the minimum DC bus voltage.

For example, if the magnitude of unbalanced power ripples $P_{2\omega} = 1\,\text{kW}$ and the capacitance of filter capacitors $C_f = 20\,\mu\text{F}$. Accroding to (28), the compensated 2^{nd}-order zero-sequence voltage can be calculated as:

$$V_{2\omega} \approx \frac{P_{2\omega}}{3\omega C_f V_{dc}} \approx 65\,\text{V} \tag{32}$$

The minimum DC bus voltage can be calculated as 780 V according to (31), as shown in Fig. 5. Also, as shown in Fig. 6, the peak value of the current of the filter inductors in

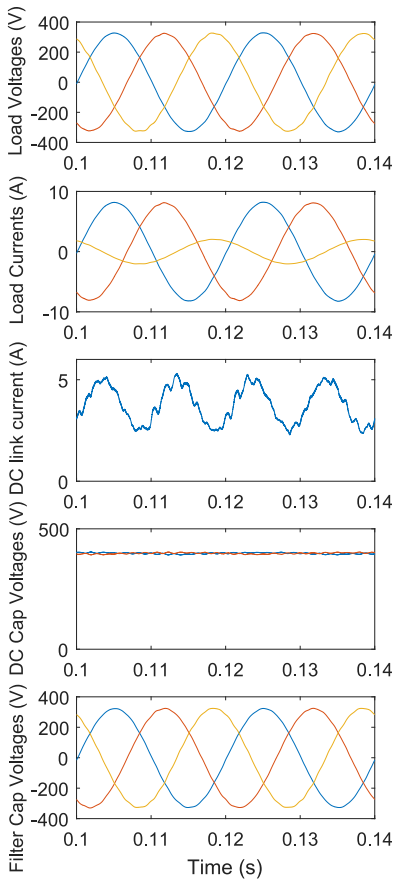

Figure 7. Simulation results of conventional three-phase four-wire inverter.

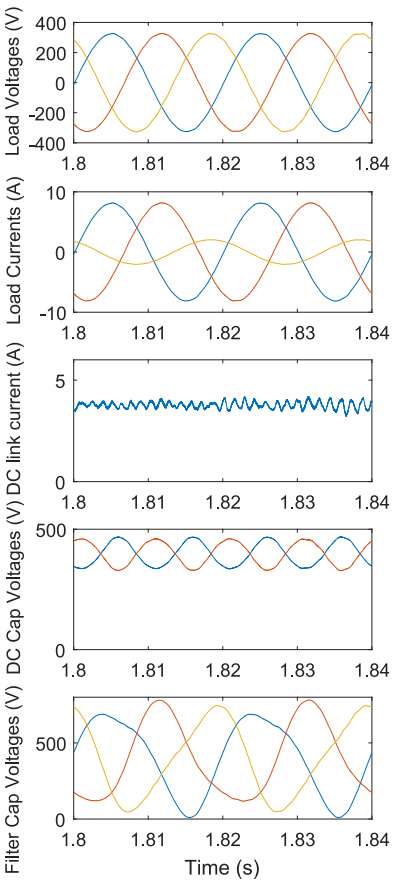

Figure 8. Simulation results of the proposed three-phase four-wire inverter.

the proposed converter is higher than that in the conventional converter, which causes higher current stress to the semiconductor swithes and the filter inductors. This is because that the second-order current will flow through the filter inductors caused by the compensated zero-sequence voltage.

V. Simulation Verification

A simulation model is built in MATLAB/Simulink to verify the proposed topology and control strategy. The parameters used in the simulation is summarised in Table. I. Fig. 7 shows the simulation results of the conventional three-phase four-wire inverter. The DC-bus current contains second-order ripples due to the unbalanced load currents. Fig. 8 shows the simulation results of the proposed three-phase four-wire inverter. Comparing to the conventional inverter, the proposed one removes second-order ripples from DC link current. The second-order ripples are absorbed by the AC filter capacitors. With the reduction of DC-bus ripples, the DC-bus capacitance can be significantly reduced. The proposed topology can be applied to the three-phase four-wire SiC-based inverter to increase the power density by reducing the DC-bus capacitance.

Table I
Simulation Parameters.

V_{dc}	800V	V_{ac_rms}	230V
Split DC capacitors	20 μF	Filter capacitors	20 μF
Neutral inductor	2.5 mH	Filter inductors	2.5mH
Switching frequency		20 kHz	
Load resistors	$R_a = R_b = 40\,\Omega$, $R_c = 160\,\Omega$		

As discussed in Section III, a negative compensated voltage is applied by the neutral leg on the DC-bus split capacitors to remove the second-order harmonics on the loads. Comparing the voltages of filter capacitors in Fig. 7 and Fig. 8, it can be seen that there is the DC offset voltage and second-order harmonics in the capacitor voltages in Fig. 8 according to (10). Therefore, the voltage stress of the filter capacitors is higher in the proposed topology due to the DC offset voltage, which need to be considered when selecting the capacitors.

VI. Conclusion

In this paper, a SiC-based three-phase four-wire inverter has been proposed to reduce the second-order ripples on the DC bus to achieve high power density. An additional conduction

path is constructed between the negative DC bus and the AC filter capacitors. With the proposed control strategy, the second-order ripples are absorbed by the filter capacitors and the DC-bus ripples and capacitance are reduced. The above function has been achieved without adding any additional hardware components. It is also discussed that the proposed topology requires higher DC-bus voltage and causes higher current and voltage stress. The future work is to build the experimental testbench based on SiC MOSFETs to validate the proposed topology and analyze the efficiency of the converters.

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