Optimization of ohmic contact for AlGaN/ GaN HEMT on low resistivity silicon

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***Abstract*— In this study, we report the optimisation of ohmic contact formation on AlGaN/GaN on low resistivity silicon. To achieve this, a strategy of uneven AlGaN / GaN was introduced through patterned etching of the substrate under the contact. Various pattern designs (holes, horizontal lines, vertical lines, grid) and varied etch depth (above and below the 2-dimensional electron gas) were investigated. Further, a study of planar and non-planar ohmic metallisation was investigated. Compared to a traditional fabrication strategy, we observed a reduced contact resistance from 0.35 Ω.mm to 0.27 Ω.mm by employing a grid etching approach with a "below channel" etch depth and non-planar ohmic metallisation. In general, measurements of "below channel" test structures exhibited improved contact resistance compared to "above channel" in both planar and non-planar ohmic metallisation.**

***Index Terms*— AlGaN/GaN High Electron Mobility Transistors (HEMTs), annealing temperatures, above and below 2DEG channel etching, contacts, contact resistance, contact roughness, GaN HEMTs, GaN on Low Resistivity Silicon, metal morphology, ohmic contacts, patterned etching, planar and non-planar ohmic surfaces, recessed ohmic contacts.**

I. Introduction

Wide band gap materials such as gallium nitride (GaN) are well suited for high-power, and high-frequency electronic devices over their silicon counterparts. This is due to a large bandgap (E_g ~3.42 eV), high critical electric field (E_e ~3.3 MV/cm), high electron saturation velocity (v_{sat} ~2.7×10^7 cm/s) and high carrier mobility (μ_n ~2000 cm^2/s) of the two-dimensional electron gas (2DEG) channel formed by an AlGaN/ GaN interface. The ability to grow defect-free GaN on large silicon wafers also makes this technology more economic, while maintaining high performance [1]. However, one the many factors that limits the performance of GaN HEMTs is the requirement of low ohmic resistance, smooth surface morphology, and thermal stability for high-temperature performance [2]. This paper reports on the optimisation of ohmic contact formation on GaN-on-low resistivity (LR) Si substrate.

Several approaches have been adopted to try reduce access resistance to an AlGaN/ GaN interface. Ti/Al based metal schemes like Ti/Al/Ni/Au, Ti/Al/Mo/Au, Ta/Ti/Al/Ni/Au, Ti/Al/Ta/Au and Ti/Al/Ti/TiN annealed at elevated temperatures have been successfully demonstrated to reduce contact resistance [3] [4] [5] [6] [7]. Recess of the barrier layer at the drain and source has also proven to be successful [8] [9]. Regrowth of N-type GaN is so far the most effective way to reduce ohmic contact resistance, however the procedure is currently cost prohibitive and adds significant complexity to the fabrication process. N-type doping in the source and drain is also effective but requires extremely high anneal temperatures of the ohmic contacts compared to conventional schemes and can be similarly expensive.

In this paper, characteristics of contact resistance are studied by creating an uneven AlGaN/ GaN interface (barrier recess) through etching different patterns into the substrate. Two different etch depths were considered in this experiment; above and below the 2DEG channel, and different etch patterns, holes,

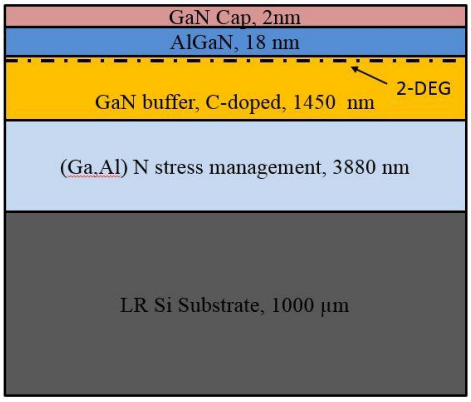

Fig. 1. Schematic of the AlGaN/GaN HEMT on the LR Si (111) silicon

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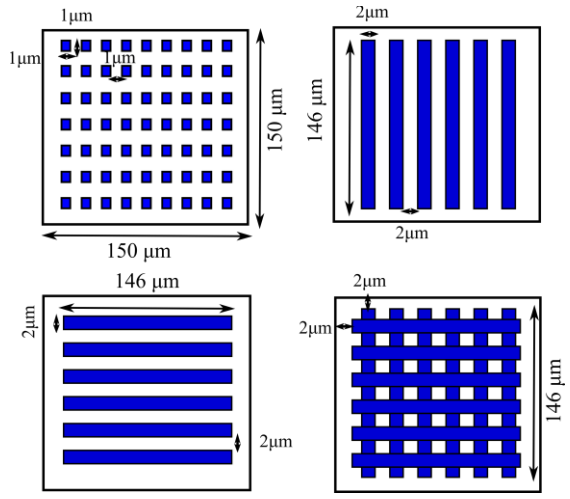


Fig. 2. Etching patterns of uneven AlGaN/GaN structures used in this experiment

vertical lines, horizontal lines and a grid. Further, differences in resistance for planar and non-planar ohmic contact for above channel etch formation was measured. This is the first time such an experiment has been reported for GaN-on-LR Si.

II. Experimental

The Epitaxial layer structure used in this paper is as shown in the Fig. 1. Growth of AlGaN/GaN was done on a 1 mm thick silicon substrate by metal organic chemical vapour deposition (MOCVD). This process starts with the growth of a GaN stress management layer of 3880 nm followed by a carbon doped buffer layer of 1450 nm and the formation of an 18 nm $Al_xGa_{1-x}N$ (X=0.26) and 2 nm GaN cap layer. A sheet resistance of 475.4 Ω/□, carrier density of 7.41×10^{12} cm^{-2} and mobility of 1770 cm^2/V-s was obtained through Hall measurement of van der Pauw (VDP) structures.

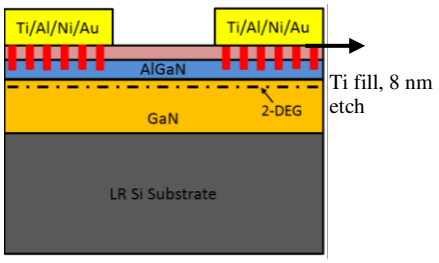
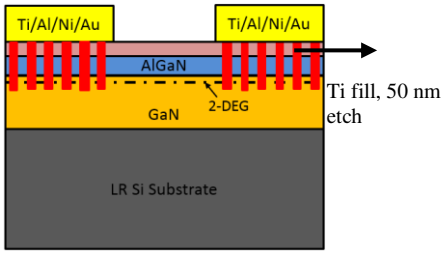
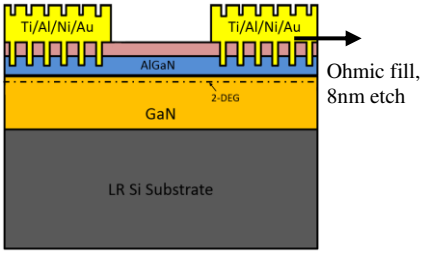
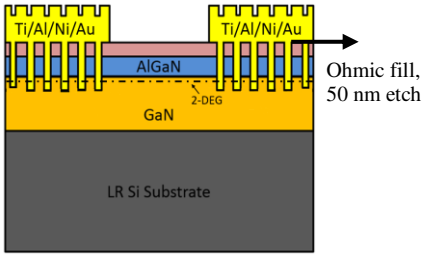
Sample set	Etch depth	Etch pattern	Metal filled	AFM Roughness by annealed temperatures (RMS nm)				Cross-section schematic
				790°C	810°C	830°C	850°C	
Set I	N/A	No etch (control structure)	N/A	75.4	88.9	92	101	
	8 nm	Holes	Ti	64.2	91.8	68.7	65.5	
		Horizontal		73.7	92.5	91	103	
		Vertical		69.3	85.4	100	98.6	
		Grid		70.7	86.2	93	95.8	
Set II	N/A	No etch (control structure)	N/A	N/A				
	50 nm	Holes	Ti	88.7	97.2	97	106	
		Horizontal		87.6	84.9	95.2	103	
		Vertical		93.9	94.6	101	101	
		Grid		94.8	101	104	115	
Set III	N/A	No etch (control structure)	N/A	81	97.5	103	112	
	8 nm	Holes	Ti/Al/Ni/Au	61.3	72.4	82.9	73.4	
		Horizontal		87	105	80.6	100	
		Vertical		91.2	108	102	105	
		Grid		69.4	88.1	79.3	71.1	
Set IV	N/A	No etch (control structure)	N/A	N/A				
	50 nm	Holes	Ti/Al/Ni/Au	56.7	61.9	87.6	110	
		Horizontal		82.3	99.1	105	105	
		Vertical		102	106	70.4	103	
		Grid		92.5	92.2	88.7	108	

Table. 1. Summary of samples used in this study. Each set has varied etch depth, metallization and contact roughness. An illustrative cross section of the ohmic contact is provided for each set.

Fig. 2 shows the different etching patterns investigated. First is a hole pattern consisting of 1 × 1 µm holes with 1 µm separation. Second is a horizontal line pattern of size 2 × 146 µm lines separated by 2 µm. Next is a vertical line etch pattern of the same geometry perpendicular to the direction of current flow and lastly a combination of horizontal and vertical etching to form a grid pattern. Additionally, a control contact with no etching was included for comparison purposes. Contact resistance of each approach was determined using the Transmission Line Measurement (TLM) method. Table 1 shows the sample sets prepared for this experiment, each set has four samples for different annealing temperatures (790, 810, 830, 850 ^{0}C) and in total 16 samples were fabricated. Each sample had the four etch patterns, as mentioned above, with a control of no etch pattern and two VDP structures for Hall measurements. All the samples were processed together and taken from the same wafer to mitigate parameter dispersion. Set I and set III were tested for above 2DEG channel etching and set II and IV for below 2DEG channel etching. Also, experiments were designed to compare between a planar and non-planar ohmic surface. Planar ohmic pads (Set I and II) were fabricated by filling the etched trenches under the ohmic contact with Ti metal with the thickness depending on the etch depth. Whereas, for the non-planar contacts (Set III and IV) there was no additional deposition of Ti metal to fill the trenches, resulting in an uneven metal surface on top of the contact. An ohmic metal stack of Ti/Al/Ni/Au (20/120/40/50 nm) was used. This is illustrated by cross-section schematic of each contact formation type in Table 1.

III. Fabrication

All fabrication was done using e-beam lithography and samples were prepared in parallel with each other. Samples in set I and III were etched using $SiCl_4$ in an Oxford Instruments PlasmaLab system 100 RIE with RF power of 200 W for above channel etching and samples in set II and IV for below channel etching. Etch depths of 8 nm and 50 nm were achieved respectively and was verified using Atomic Force Microscopy (AFM). For deposition of Ti into the trenches of set I and II, a lithography step was designed for Ti metal lift-off process using electron-beam evaporation. The thickness of the Ti filled in the etched area was matched to the depth measured by AFM to produce a planar surface. AFM and optical analysis during the fabrication process verified the resist profile matched that of the etch and no gaps were observed. For samples without additional Ti deposition (set III and IV), both etching and ohmic metallization were carried out in a single lithography step, producing a non-planar surface. Ohmic metals were deposited using electron-beam evaporation and all sets of samples were metallised at the same time. Isolation of the TLM's was achieved via a mesa etch around the test structures, using inductively coupled plasma (ICP) and Cl_2/Ar chemistry. Lastly, the ohmic contacts were annealed under vacuum using Rapid Thermal Annealing (RTA) at four different temperatures of 790, 810, 830, 850^{0}C for 30 secs.

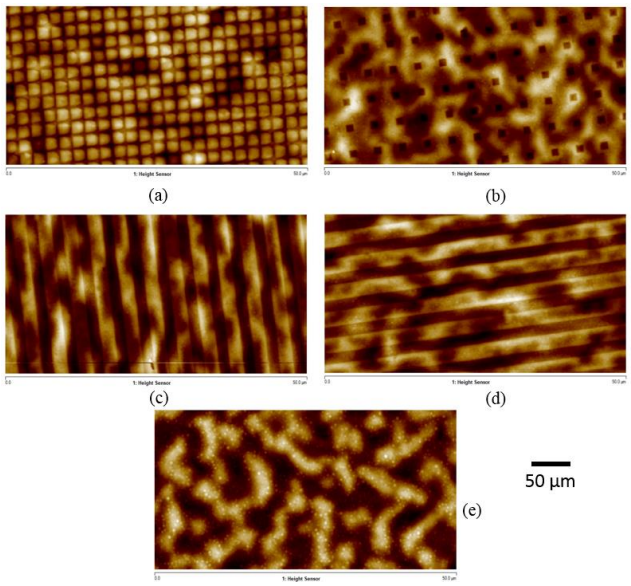


Fig. 3. 50 µm AFM scans of non-planar ohmic surface (a) holes (b) grid (c) vertical (d) horizontal (e) no etch

Fig. 3 shows AFM scans for each etch pattern after metallisation for non-planar contacts. The roughness values of all four temperatures annealed for each pattern and etch depth along with control sample are presented in the 6th column of Table 1. Samples annealed were rougher (50 nm-110 nm) than the other pattern etching studies (19 nm - 43 nm) [10]. This might be due to the etching of the AlGaN interface or use of Ti/Al/Ni/Au ohmic metal stack. Further, there was no clear difference in roughness between planar and non-planar ohmic surfaces, most likely due to the metal re-flow in non-planar structures. Roughness increased with annealing temperature for all samples, as could be expected. The roughness of annealed Ti/Al/Ni/Au ohmic metal stack is often reported to be much higher than a Ti/Al/Mo/Au or Ti/Al/Ti/Au due to the Ni-Al alloy aggregation in some areas [11].

IV. Results and Discussion

Fig. 4 shows the measurement of contact resistance with annealing temperature for different etch depths, etch patterns, planar contacts and the control design. Above channel etching is represented by a black solid line, and below channel etching is represented by black dashed line. Above channel etching showed greater contact resistance (0.424 - 0.616 Ω.mm) in general compared to below channel etching (0.348 - 1.157 Ω.mm), except in the grid and vertical etch pattern designs. Below channel etching for both vertical and grid patterns showed some unusual behaviour. For vertical etching there was a sudden dip in the contact resistance at 810^0 C and for grid etching there was a sudden rise in contact resistance at 810^0 C. These anomalies might be due to ohmic roughness or impurities in GaN which contribute towards contact resistance. Comparing all above channel etching, the hole pattern exhibited a lower contact resistance in general (0.424 - 0.477 Ω.mm) compared to horizontal (0.535 - 0.555 Ω.mm), vertical (0.572 - 0.607 Ω.mm) and grid etching patterns (0.512 - 0.616 Ω.mm). For below channel etching patterns, hole etching exhibited

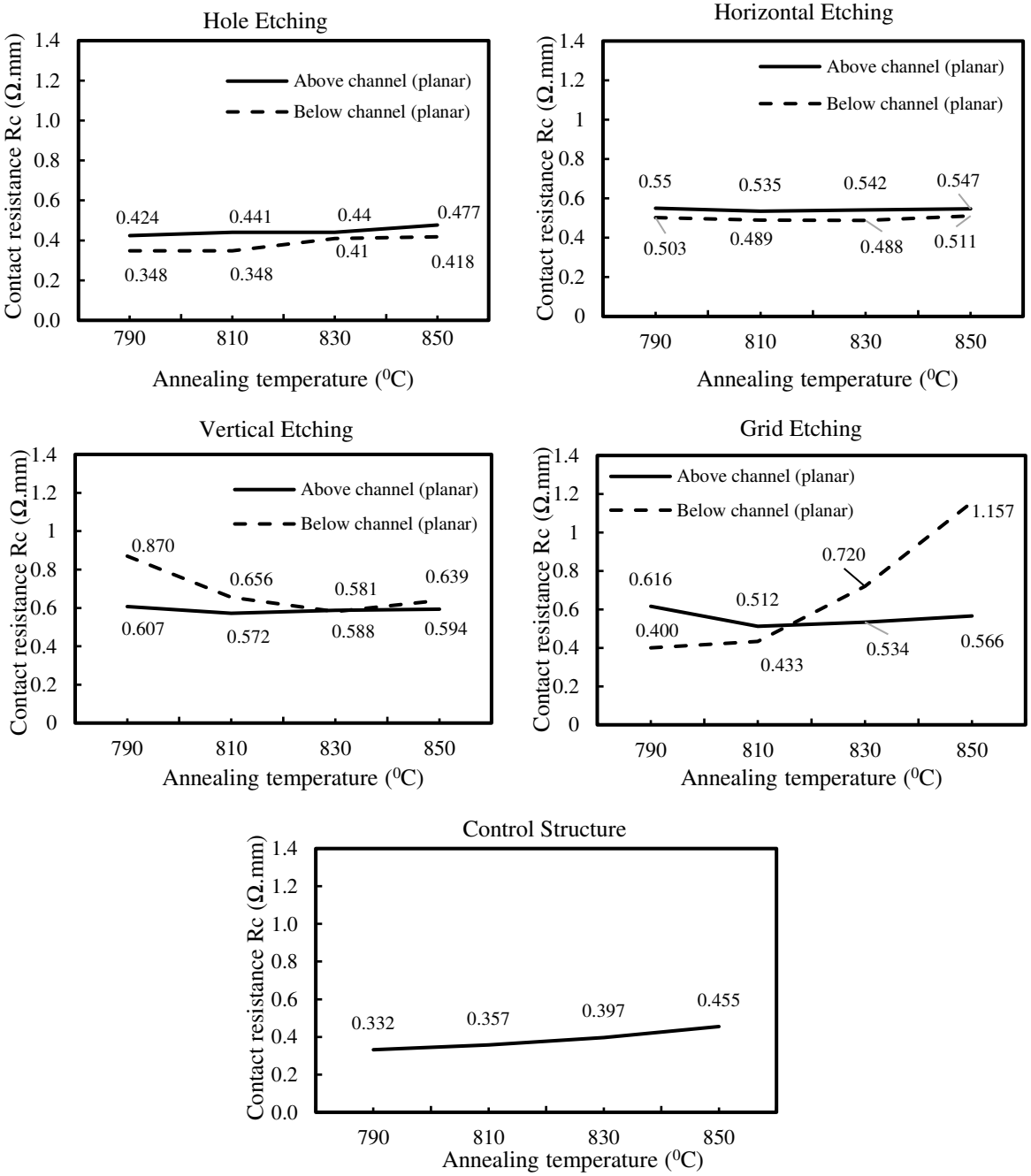


Fig. 4. Plots of planar ohmic contact resistance vs annealing temperatures

lower contact resistance (0.348-0.418 Ω.mm) in general compared to horizontal (0.488-0.511 Ω.mm), vertical (0.581-0.870 Ω.mm), and grid (0.4 - 1.157 Ω.mm). Comparing this to the control sample, a contact resistance of 0.332 - 0.455 Ω.mm was achieved, which showed better performance than above or below etching with planar ohmic surfaces.

Fig. 5 shows the measurement of contact resistance with annealing for the non-planar samples. Above channel etching is represented by a red solid line and data of below etching is represented by a red dashed line. Above channel etching showed higher ohmic contact resistance (0.475 - 1.136 Ω.mm) compared to below channel for non-planar ohmic surfaces (0.278 - 0.755 Ω.mm). Comparing to other above channel etching, hole etching (0.475 - 0.804 Ω.mm) performed better in general than horizontal etching (0.93 - 1.136 Ω.mm), vertical (1.077 - 1.094 Ω.mm) and grid etching (0.603 - 0.865 Ω.mm), despite the unusual spike at 810^0C. Below channel etching with a grid design (0.278-0.455 Ω.mm) performed better than hole (0.502 - 0.716 Ω.mm), horizontal (0.482 - 0.68 Ω.mm) and vertical etching (0.509 - 0.755 Ω.mm). Relating these results to the control sample, an average contact resistance of 0.35 to 0.41 Ω.mm was achieved. A contact resistance of 0.27 Ω.mm was observed for a grid patterned ohmic contact employing below channel etching and an anneal temperature of 830^0C. By comparison, the lowest contact resistance measured for TLM's without etching was 0.32 Ω.mm, annealed at 790^0 C. Since the

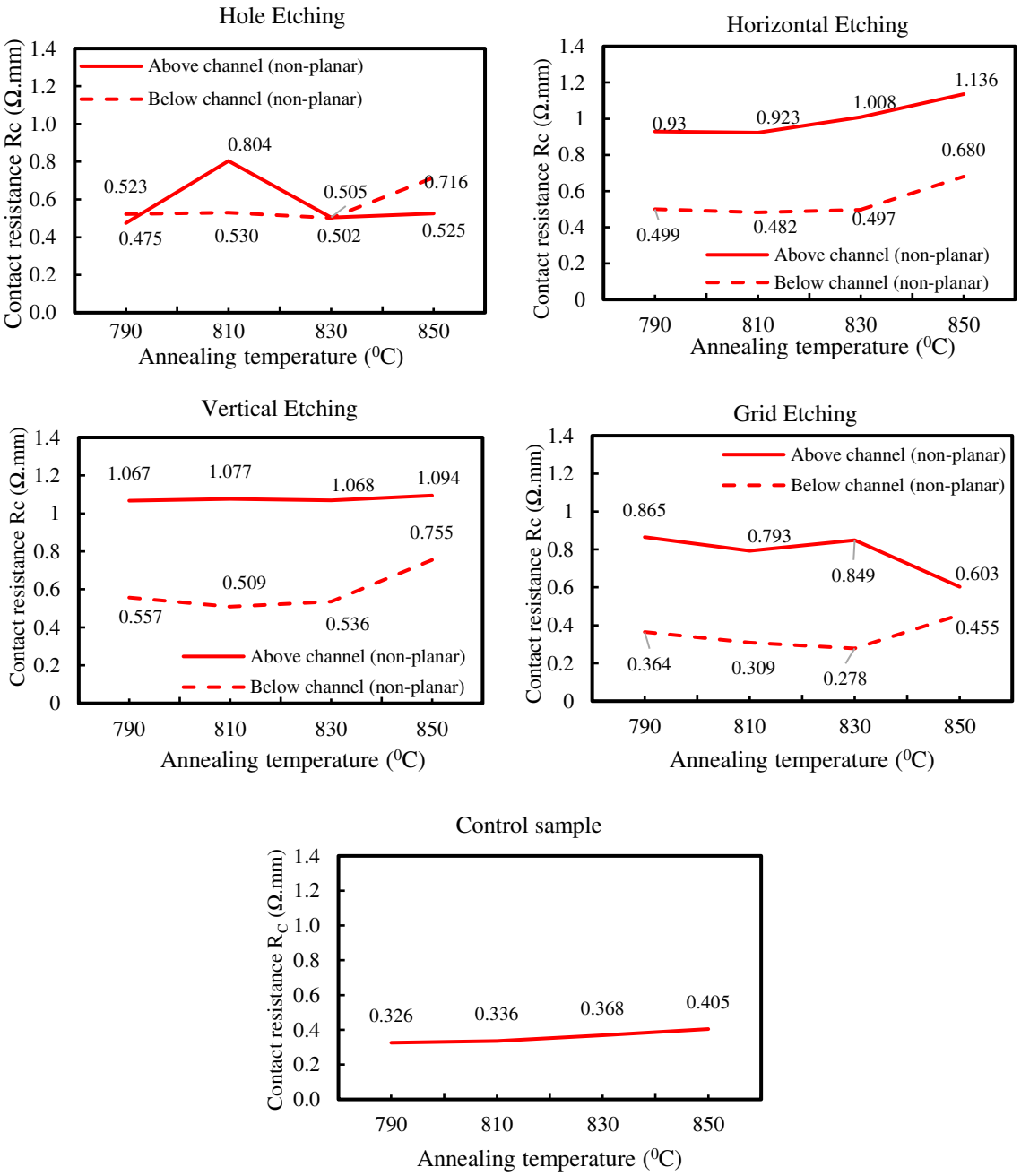


Fig. 5. Plots of non-planar ohmic contact resistance vs annealing temperatures

annealing temperature only differed by 20^0C, it is possible that a contact resistance of less than 0.27 Ω.mm was achieved between the annealing temperatures of 810 and 850^0 C.

The concept of an irregular AlGaN layer underneath the ohmic metal was proposed to reduce contact resistance lower than the limit found in control structures. First, patterned etching removes the irregular surface oxide layers and the pollutants by etching process which attributes to the lowering the contact resistance [12]. Second, patterned AlGaN increases 2DEG concentration by creating fringes near the edges of the etched AlGaN and high-density 2DEG located just outside these regions [13] [14]. Third, due to more side wall area the Ti will react with AlGaN to form TiN (which has lower work function than Ti), facilitating direct carrier transport between metal and 2DEG [15]. The improved tunneling effect through N vacancies can be explained by the following equations:

$$R_c = \left(\frac{\partial J}{\partial V}\right)^{-1}\Bigg|_{V=0} \ \Omega.cm^2 \quad (1)$$

, where

$$J_t \propto \exp\left(\frac{-e\phi_{Bn}}{E_{00}}\right) \quad (2)$$

$$E_{00} = \frac{e\hbar}{2}\sqrt{\frac{N_d}{\varepsilon_s m_n^*}} \quad (3)$$

Through plasma etching, N vacancies are created at the surface of AlGaN [10] [14], which increases the donor doping concentration N_d and electric field E_{00}, Equation 3. Thus, increasing the tunnel current J_t and reducing the contact resistance R_C, Equation 1 & 2. In the above channel etch, the electron tunneling between the ohmic metal and channel is low due to the thick barrier underneath, contributing to higher contact resistance. Non-planar surface ohmics demonstrate this behavior whereas in planar surface ohmics this is improved, which may be due to the extra filling of Ti in the trenches which could have reduced the barrier height. This shows the importance of Ti thickness with respect to the AlGaN thickness. In below channel etching, we find that non-planar ohmic surface performed much better than the planar surface, extra filling of Ti metal in the etched area did not show any significant improvement in the contact resistance. Previous some research [9] [14] has shown etching below the 2DEG channel, in the case of a single recess ohmic contact, to exhibit high contact resistance. Even though the barrier height is low, the absence of 2DEG channel underneath the contact limits carrier tunneling to a smaller region around the sidewall of the recessed barrier. Other work [16] [15] has shown, etching below the channel enhances ohmic performance. This difference is reportedly due to the sidewall angle, metal coverage and metallization. In our case, several small areas are etched under the contacts and thus tunneling is likely to occur around the sidewall of each etched region, achieving lower contact resistance. Overall, the below channel etch pattern with increased sidewall area exhibited lower contact resistance. When comparing the grid pattern to others tested, it is also possible the improvement in contact resistance observed is due to increased sidewall area in the transfer length region of the contact alone. This method of pre-etching the substrate prior to metallization is simple and non-invasive.

V. Conclusion

In this paper, we have investigated the optimization of ohmic contact formation on GaN on low resistivity silicon through patterned etching of the AlGaN/ GaN substrate at two different etch depths and four annealing temperatures. A grid pattern etched below the 2DEG channel produced the lowest ohmic contact resistance observed (0.27 Ω.mm). Using a grid pattern produces increased exposed sidewall area and is most likely the cause of reduced contact resistance. Below channel etching also exhibited lower contact resistance compared to above channel etching. Further, use of extra Ti metal in the etched trenches to produce a planar surface showed reduction in contact resistance for above channel etching, but not for below channel etching. These results indicate etching beneath contacts can be a relatively simple method to reduce contact resistance, which will benefit RF and power devices based on GaN on low resistivity silicon. While devices in this study were produced using e-beam lithography, such etching can be easily achieved with photolithography also. Further optimization of etch pattern design could yield even greater improvements, such as a tapered profile to maximize sidewall area.

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