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Citation for final published version:

Wang, Sheng , Ming, Wenlong , Liu, Wei, Li, Chuanyue , Ugalde Loo, Carlos and Liang, Jun 2021. A multi-function integrated circuit breaker for DC grid applications. IEEE Transactions on Power Delivery 36 (2) , pp. 566-577. 10.1109/TPWRD.2020.2984673

Publishers page: http://dx.doi.org/10.1109/TPWRD.2020.2984673

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A Multi-Function Integrated Circuit Breaker for DC Grid Applications

Sheng Wang, *Member, IEEE*, Wenlong Ming, *Member IEEE*, Wei Liu, *Member IEEE*, Chuanyue Li, Carlos E. Ugalde-Loo, *Senior Member*, *IEEE* and Jun Liang, *Senior Member*, *IEEE*

***Abstract*-- The protection and current flow regulation of high-voltage direct-current (HVDC) grids requires the deployment of additional semiconductor-based equipment including dc circuit breakers (DCCBs) and current flow controllers (CFCs). However, the inclusion of multiple devices could significantly increase the total cost of an HVDC system. To potentially reduce costs, this paper presents an innovative multi-function integrated DCCB (MF-ICB). The proposed device exhibits a reduced number of semiconductor switches and can fully block dc faults at different locations while regulating dc currents. The configuration of the integrated solution and its operating principle are assessed, with its performance being examined in PSCAD/EMTDC using a three-terminal HVDC grid. Simulation results demonstrate the capability and effectiveness of the MF-ICB to regulate grid current and isolate dc faults.**

***Index Terms*--HVDC, protection, current flow regulation.**

I. Introduction

MESHED high-voltage direct-current (HVDC) grids are becoming increasingly important for bulk power transmission due to their higher transmission capability and reliability compared to radial configurations. However, the presence of multiple dc lines may require selective protection and current flow regulation to prevent line overloading.

Current flow controllers (CFCs) are semiconductor-based devices enabling dc current regulation in meshed HVDC grids. Numerous implementations are possible. For instance, a CFC based on a controllable variable resistor regulates currents by inserting a resistor in series [1]. However, such an approach incurs extra power losses and, hence, a large cooling system may be needed. Moreover, the direction of current flow cannot be changed. To relieve these shortcomings, a CFC based on a controllable voltage source (CVS-CFC) regulates dc currents by inserting an active (positive or negative) voltage to a dc line, enabling the magnitude and direction of the current to be modified [2]. By avoiding the use of a resistor, power losses are reduced. An ac-coupled CVS-CFC connects one dc line to an external ac source using an ac/dc converter linked to an isolation transformer [3]. Conversely, a dc-coupled CVS-CFC links two dc lines via dc/dc converters connected in series [4], [5] or in a series-parallel topology [6]. DC-coupled CFCs based on H-bridge modules are arguably the ideal solution for current regulation as they do not need an isolation transformer and, in addition, require fewer semiconductors [7], [8].

A number of dc circuit breaker (DCCB) technologies are available for dc protection. Resonant DCCBs have a low cost as they employ mechanical switches. However, their speed of operation is slow (~60 ms), making them less competitive [9]. Solid-state DCCBs can block a fault current within 1 ms; however, they exhibit high power losses [10]. This may be circumvented by using unidirectional solid-state topologies, although losses are much higher than with other types of DCCBs [11]. A favorable choice is the use of hybrid DCCBs (HCBs), which combine low power losses (~0.1%) and a fast speed of operation (2-3 ms) [12]. In an HCB, current is conducted through a low-loss bypass branch during normal operation. Once a fault occurs, current is commutated to an IGBT-based main breaker, which immediately blocks the fault current. Different HCBs have been proposed by manufacturers [10], [12], [13], but their key features remain the same.

Although the simultaneous use of DCCBs and CFCs may improve the control and protection of an HVDC grid, the practical deployment of multiple devices could be prohibitive due to the large number of controllable components. For instance, a single HCB may use hundreds of IGBTs in its main breaker only. It is essential to decrease overall costs to facilitate implementation, which may be possible if the number of IGBTs used is reduced. Research has been done in this direction. For instance, [14] presents a series interline CFC for unidirectional current flow control, whereas [15], [16] incorporate a current regulation function into an HCB to avoid including extra CFCs. In [17], unidirectional HCBs with half the number of IGBTs are considered to block faults in a single direction, while a commutation-based HCB with an additional diode bridge has been proposed [13]. An alternative is the implementation of an H-bridge-based HCB with additional bypass branches but fewer IGBTs [18]. The number of IGBTs within an HCB can be also reduced by coordinating the protection strategy between converters and HCBs to suppress fault currents [19].

Another option to reduce costs is the use of integrated circuit breakers (ICBs), where IGBTs are shared between components to protect multiple dc nodes. ICBs can reduce the IGBT count by 25 to 50% by sharing several reduced-size main breakers [20], [21]. In [22], an ICB topology termed dc switchyard is designed to provide both primary and backup protection with a reduced number of main breakers. The number of IGBTs can be further decreased by either sharing a unidirectional main breaker [23] or by using bridged current commutation circuits [24]. Alternatively, strings of thyristors can be used within an ICB to replace several IGBT-based main breakers [25], [26].

Although the previously discussed alternatives add insight to the design of cost-saving DCCBs, a multi-objective integrated device for dc grid protection and current flow regulation with a reduced number of semiconductor switches is yet to be developed. To bridge such gap, this paper presents a multi-

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function ICB (MF-ICB) offering the following features and benefits: full protection from dc faults at different dc lines, converter terminals and dc buses; current control capability; and significant reduction of the IGBT count. It is shown that the installation of a single MF-ICB to connect several dc nodes is a cost-effective option preventing the use of multiple devices. For completeness, the concept and structure of the MF-ICB, its operating principle, a mathematical analysis, a comparison with other solutions, and simulation studies are provided in the paper.

II. Conceptual Description of an MF-ICB

A. Conventional DC Protection and Current Regulation

A typical solution for dc grid protection and current regulation relies on separate DCCBs and CFCs placed at different dc nodes. Fig. 1 shows the schematic of an HCB. It consists of a bidirectional main breaker (BMB), a bypass branch, and associated elements including a current limiting reactor (CLR) and a residual circuit breaker (RCB) [27]. Under normal conditions, the current will flow through the bypass branch only. This branch has an IGBT-based load commutation switch (LCS) and a mechanical ultrafast disconnector (UFD). The LCS may include 9 IGBTs connected as a 3×3 matrix [28]; hence, power losses will be very low. Once a fault occurs, the LCS immediately opens to commutate the current to the BMB. The UFD will then open after a delay of ≈2-2.5 ms [27]. The BMB is based on a significant number of IGBTs (>100) and, thus, can turn off immediately following the opening of the UFD. Finally, the RCB is opened to physically isolate the fault.

Fig. 2 shows a schematic of a dc-coupled CFC. It has two H-bridge converters and a dc capacitor. One converter regulates the dc line current (i_1) by injecting an adjustable voltage (u_{01}), while the other regulates the voltage across the capacitor [7].

Fig. 3 shows the deployment of multiple HCBs and CFCs to concurrently protect a dc grid and regulate current flow. For a dc bus with n nodes, n HCBs will be needed (one at each node). If the current through k nodes needs to be controlled, k CFCs will be need. Since both devices are based on IGBTs, such an approach considerably increases the overall cost of the solution.

B. MF-ICB Solution

The MF-ICB topology shown in Fig. 4 may be adopted to reduce the IGBT count and to provide an integrated solution for dc protection and current flow regulation. It consists of a single bridge-type BMB and several bypass branches based on UFDs and two different types of LCSs. Compared to the solution shown in Fig. 3, an MF-ICB offers three main advantages:

1. The BMB is shared to protect different nodes. This will significantly reduce the cost of the protection system.
2. Within the BMB and LCS units at the lower bypass branches, the bridge-based one-IGBT-four-diode units (see bottom of Fig. 4) requires half the number of IGBTs compared to the anti-series connected two-IGBT-two-diode units used in HCBs (see Fig. 1). Since the cost of a diode is around 10 times less than the cost of an IGBT [13], the adoption of one-IGBT-four-diode units will not greatly affect the overall cost.
3. The CFC units are integrated to the upper bypass branches of the MF-ICB (CFC-LCS modules) for current flow regulation. This further reduces costs as no separate CFC is needed.

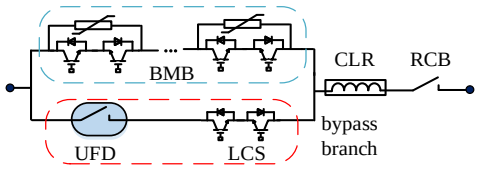

Fig. 1. Conventional HCB.

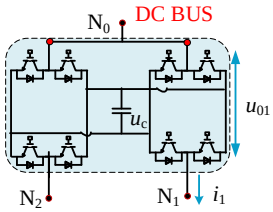

Fig.2. Conventional dc-coupled CFC.

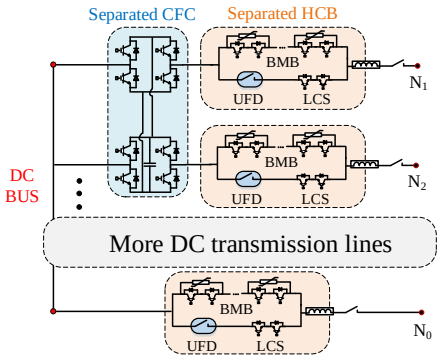

Fig. 3. Conventional solution using multiple HCBs and CFCs.

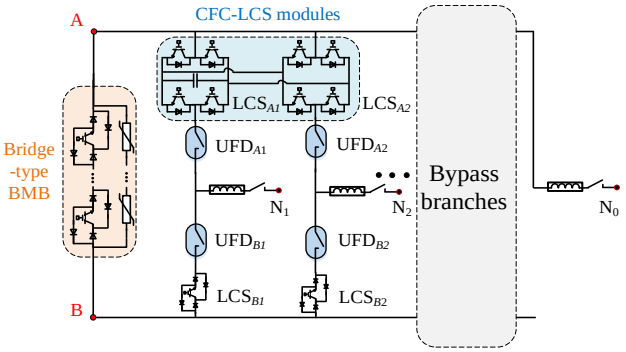

Fig. 4. Structure of an MF-ICB.

Table I compares the total component count for an MF-ICB and a conventional solution based on separate HCBs and CFCs. The number of devices for the conventional solution depends on the number of connected dc nodes n and dc lines with current regulation k, which increases as n and k, in turn, increase. However, since an MF-ICB does not require external CFCs, a single BMB is needed. The main shortcoming is that an MF-ICB requires additional bypass branches. However, the UFDs in these branches are mechanical components and their cost is lower compared to that of the main breakers. Also, the LCSs in the bypass branches have a low voltage rating and, thus, will not considerably increase the cost. A more detailed comparison on the cost of the different solutions is given in Section IV.

TABLE I
COMPARISON BETWEEN CONVENTIONAL SOLUTION AND MF-ICB

Components	Conventional solution	MF-ICB
CFC	k	0
DCCB	n	1
Main breakers	n	1
Bypass branches	n	$2n$-2

III. Operating Principle of an MF-ICB

A. Operation of CFC-LCS Modules for Current Regulation

To facilitate the description of the operating principle of an MF-ICB, a three-node device is used for simplicity (see Fig. 5). It is assumed that nodes N_1 and N_2 are connected to dc lines and node N_0 is connected to a converter. The operating principle for an *n*-node MF-ICB can be extended from this topology.

Under a no-fault condition, the MF-ICB regulates dc line current using the CFC-LCS modules in its upper bypass branches LCS_{A1} and LCS_{A2}. At the lower bypass branches, LCS_{B1} and LCS_{B2} must be open to prevent the CFC-LCS modules from being bypassed. The bridge-type BMB can stay closed and no leakage current will flow through it as LCS_{B1} and LCS_{B2} are open. This is different to a conventional HCB, whose main breaker should remain open during no-fault conditions to prevent leakage current. All UFDs (see Fig. 5) can stay closed.

Fig. 6 shows the operating modes of the CFC-LCS modules: buck and boost. The IGBTs highlighted in red switch for pulse-width modulation (PWM), whereas those in black remain closed and those in grey are open. If the modules operate in buck mode, a PWM signal will be sent to Q_{11}, Q_{12}, Q_{21} and Q_{22} (see Fig. 6(a)). If Q_{11} and Q_{21} are 'on', Q_{12} and Q_{22} must be 'off' and vice versa. IGBTs Q_{13} and Q_{24} are always closed. When Q_{11} and Q_{21} are 'on', the current flowing through the capacitor ($\boldsymbol{i_c}$) is:

$$i_c(t) = i_0(t) - i_1(t) \tag{1}$$

where i_0 and i_1 are the currents at nodes N_0 and N_1, respectively. Similarly, when Q_{12} and Q_{22} are 'on', $i_c = -i_1$.

The capacitor voltage u_c is maintained constant in steady-state and the energy stored in the capacitor is balanced. Thus, the average current through the capacitor ($I_{c,avr}$) is zero within one PWM cycle. The following relations can be established:

$$I_{c,avr} = \frac{1}{T}\int_0^T i_c(t)\,dt = \frac{[i_0(t)-i_1(t)]\times DT - i_1(t)(1-D)\times T}{T} = 0 \tag{2}$$

$$i_1(t) = i_0(t) \times D \tag{3}$$

$$i_2(t) = i_0(t) \times (1-D) \tag{4}$$

where T is the duration of one PWM cycle, D is the duty ratio and i_2 is the current at N_2. By adjusting D, $i_1(t)$ and $i_2(t)$ can be regulated, as shown in (4). However, D has a value between 0 and 1 and, thus, $i_1(t)$ and $i_2(t)$ will have a lower magnitude than the converter current $i_0(t)$ for buck mode operation.

A dc line current higher than $i_0(t)$ is achieved when the CFC-LCS modules operate in boost mode. This is shown in Fig. 6(b). The PWM signal is sent to Q_{13} and Q_{14}. When Q_{13} is 'on', $i_c(t)$, $i_0(t)$ and $i_1(t)$ have the same relationship given in (1). When Q_{14} is 'on', $i_c(t) = i_1(t)$. The currents are given as:

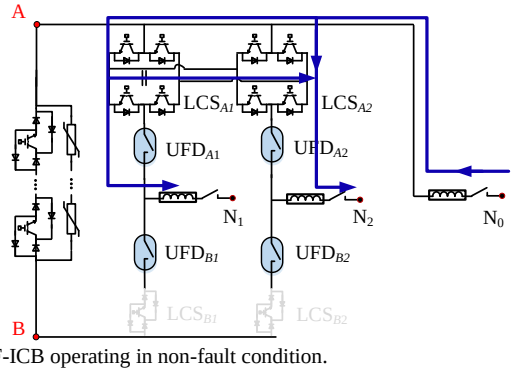

Fig 5. MF-ICB operating in non-fault condition.

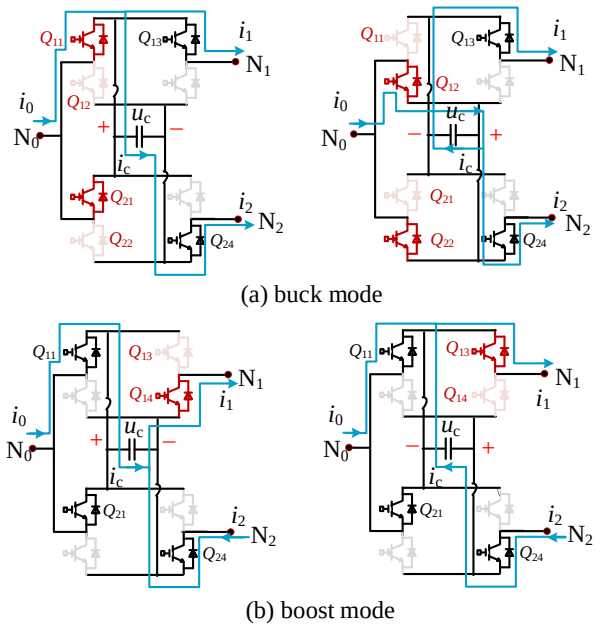

Fig. 6. Operating modes of the CFC.

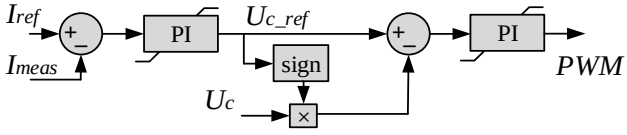

Fig. 7. Control of CFC modules.

$$I_{c,avr} = \frac{[i_0(t)-i_1(t)](1-D)T - i_0(t)DT}{T} = 0 \tag{5}$$

$$i_1(t) = \frac{i_0(t)}{1-D} \tag{6}$$

$$i_2(t) = \frac{-D\times i_0(t)}{1-D} \tag{7}$$

where the magnitudes of $i_1(t)$ and $i_2(t)$ can be higher than that of $i_0(t)$. Therefore, by shifting between boost and buck modes, the CFC-LCS modules can flexibly regulate a dc line current.

Fig. 7 shows the control diagram of the CFC-LCS modules. The targeted current (I_{meas}) is regulated to its reference value (I_{ref}) with a PI controller. This generates a reference capacitor voltage (U_{c_ref}). The capacitor voltage (U_c) is regulated using another PI structure. The generated PWM signals are then sent to the IGBTs within the CFC-LCS modules.

It is worth mentioning that for current flow regulation in general, it is not possible to control all nodes' currents in a dc grid as at least the current at one node must remain uncontrolled to balance the current changes in other current-controlled nodes. For the 3-node MF-ICB presented in this paper, the current at one dc line can be controlled at a specific time only, while other currents remain uncontrolled to balance any current changes.

For a practical application, the number of current-controlled dc lines should be selected based on the demands for current regulation within a dc system. For example, if a single dc line is likely to be overloaded during operation, ensuring such a dc line is current-controllable only would be adequate. Additional current-controlled dc lines could be incorporated if extra flexibility for current flow regulation is required or if other lines could become overloaded following changes in the dc system. However, a well-designed dc system should arguably have a small number of dc lines exposed to overloading only and,

hence, few current-controlled dc lines should be sufficient to guarantee the safe operation of the system. Adding more than the required current-controlled dc lines would make power flow management of a dc system unnecessarily complex. In addition, more CFC-LCS modules would be needed rather than the bridge-based one-IGBT-four-diode LCS units. This would inevitably increase the cost of an MF-ICB.

B. MF-ICB Operation for Protection

The priority of the MF-ICB following a dc fault is protection and it should act to isolate the fault. Consider a fault occurring at the line end connected to N_2. The currents will feed into N_2 via the other dc nodes, N_0 and N_1, as shown in Fig. 8. The MF-ICB will immediately open its LCS at the upper bypass branch (LCS_{A2}) connected to the faulty line (N_2), while it will close the corresponding LCS at the lower bypass branch (LCS_{B2}, see Fig. 8(a)). The right-hand side IGBTs within LCS_{A1} at the upper bypass branch connected to the healthy node N_1 will remain closed to provide a path for the fault currents, while the left-hand side IGBTs are opened. This prevents the capacitor within the CFC-LCS modules from discharging and further contributing to the fault current. At the same time, LCS_{B1} will remain open. This way, the fault current can be fully commutated to the BMB. The operating time of all LCSs is within 250 μs due to the fast opening and closing of IGBTs.

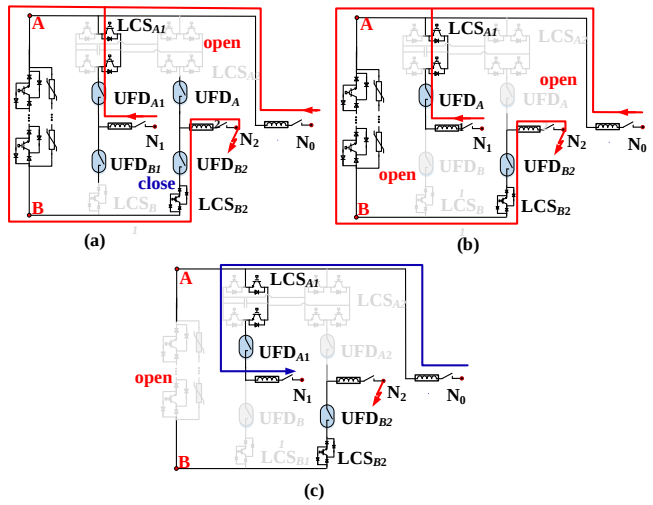

Fig. 8. Operating sequence for isolating a dc line fault.

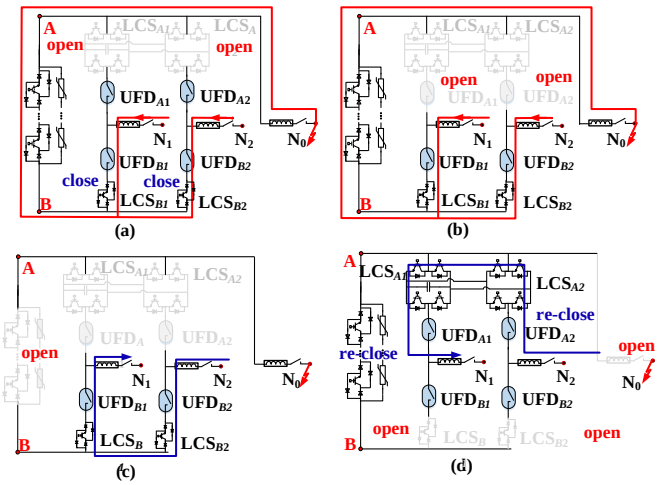

Fig. 9. Operating sequence for isolating a converter fault.

The next step is to open the UFDs associated with the opened LCSs (in this case, UFD_{A2} and UFD_{B1}), as shown in Fig. 8(b). As in an HCB, the opening time of UFDs is relatively long (≈2 ms). Once the UFDs open, the bridge-type BMB can also open to block the fault current and the fault energy will be absorbed by the surge arresters, as shown in Fig. 8(c). The current flowing through the healthy circuits can be then restored. In addition, the mechanical circuit breaker next to N_2 can be closed to physically disconnect the faulty circuit in the same way as RCBs operate in HCBs.

Note: The opening of the mechanical circuit breaker at the faulty circuit allows the recovery of the BMB and its corresponding UFDs and LCSs to the pre-fault status shown in Fig. 5. For an MF-ICB connected to more than three lines, this would enable the device to continue to protect healthy circuits after isolating a fault at a given dc line. The BMB, LCSs and UFDs connected to the healthy circuits would follow the same procedure as described in this section to isolate a second fault if this were to occur. However, if the second fault were to happen immediately after the mechanical circuit breaker opens, the surge arrester of the BMB would exhibit a very high temperature when absorbing the fault energy as it would not have enough time to cool down following the first fault event.

If a second fault were to happen prior to the opening of the mechanical switch at the first faulty node, it would not be successfully blocked as the BMB, UFDs and LCSs within the MF-ICB would not have been recovered to a pre-fault status. Although this issue deserves additional investigation, it falls out of the scope of this paper.

When a fault happens at the dc converter side (N_0), the operating sequence is slightly different. This is shown in Fig 9. To be able to commutate the fault current to the bridge-type BMB, the CFC-LCS modules at the upper bypass branches should be fully opened, while the conventional LCSs at lower bypass branches should be simultaneously closed (Fig. 9(a)). The UFDs at the upper bypass branches will also be opened (see Fig. 9(b)). The bridge-type BMB can then block the fault current, as shown in Fig. 9(c), and the current will flow between healthy nodes. The mechanical switch at the faulty converter connected node (N_0) should be open (see Fig. 9(d)). To restore the CFC function and to recover the MF-ICB for the protection of the remaining healthy circuits, the CFC-LCSs at the upper bypass branches should re-close, while the LCSs at the lower bypass branches should open. The BMB should be re-closed.

It should be noticed that the restoration of the CFC function is not necessary for the three-node example in Fig. 5. Given that one node is isolated, the current flowing through the remaining two nodes is identical. However, for more than three nodes, the last step should be adopted to enable current regulation in multiple healthy circuits. It is also worth to note that the CFC capability of an MF-ICB can be recovered for a dc line fault if it does not happen at the line connected to the CFC-LCS modules.

TABLE II
OPERATING SEQUENCES FOR PROTECTION AND RATIONALE BEHIND EACH STEP

Steps	Components acting (different locations)				Reason
	Line	Converter	Internal A	Internal B	
1.LCS action	Open LCS_{A1} (left-hand side IGBTs) Open LCS_{A2} Close LCS_{B2}	Open LCS_{A1} Open LCS_{A2} Close LCS_{B1} Close LCS_{B2}	Open LCS_{A1} Open LCS_{A2} Close LCS_{B1} Close LCS_{B2}	Open LCS_{A1} (left-hand side IGBTs) Open LCS_{A2} (left-hand side IGBTs)	To ensure all currents to flow through the main breaker (*i.e.* no current bypassing the main breaker).
2. UFD action	Open UFD_{A2} Open UFD_{B1}	Open UFD_{A2} Open UFD_{A1}	Open UFD_{A2} Open UFD_{A1}	Open UFD_{A2} Open UFD_{B1}	To withstand the high voltage transient when the main breaker opens to block a fault current.
3. BMB action	Open main breaker				To fully block the fault current.
4. Recovery	Mechanical switch at N_1 open; other components recovered to pre-fault status	Mechanical switch at N_0 open; other components recovered to pre-fault status	Main breaker and opened UFDs stays open; other components recovered to pre-fault status	Main breaker and opened UFDs stays open; other components recovered to pre-fault status	To restore the currents at healthy nodes.

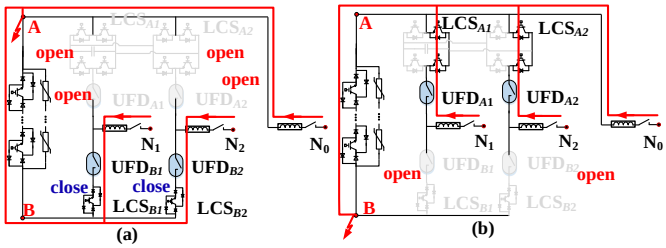

Fig. 10. Isolating an internal fault.

An internal bus fault within the MF-ICB is unlikely as the components can be air or gas-insulated in an HVDC substation [29]. However, it is still desirable to consider such faults when designing a DCCB. An MF-ICB can provide protection for an internal bus, as shown in Fig. 10. If a bus fault occurs at point A, both the LCSs and UFDs at the upper bypass branches need to be opened while the LCSs at the lower bypass branches need to be closed to commutate the fault current to the BMB (see Fig. 10(a)). The BMB can then open to block the fault current contributed from N_1 and N_2. To interrupt the current fed from N_0, the VSC connected to N_0 should also be blocked and the circuit breakers at the VSC's ac side can be opened. After fault isolation, the currents at N_1 and N_2 are restored.

For a fault at point B, currents will flow through the upper bypass branches and the BMB only; thus, no commutation is needed. However, UFDs at the lower bypass branches must be opened prior to turning off the BMB. This is to let the UFDs withstand the high voltage across the MF-ICB after opening the BMB. Currents between nodes will be restored after the BMB opens. The current flow function will be also recovered.

The operating speed of an MF-ICB is similar to that of a conventional HCB as its LCSs or UFDs act simultaneously and, hence, no extra delays are incurred. In the event of a bus fault at point B, the operating speed of the MF-ICB is even slightly faster as no current commutation is needed. Another advantage exhibited by the MF-ICB is that the current flowing through different nodes following a bus fault can be partially or fully recovered after fault isolation. This is not possible for HCBs as they must be blocked to prevent current flow through all dc nodes connected to the bus to feed the faulty point.

The operating sequences of an MF-ICB for fault isolation at different locations are summarized in Table II. It should be noted that these sequences change depending on the type and location of the fault. For instance, for Step 1, different LCSs need to act to ensure that all node currents flow through the main breaker—failure to do so would lead to the currents bypassing the main breaker, which, in turn, would not be able to successfully block fault currents in Step 3.

Consequently, in Step 2, different UFDs will need to be opened to withstand the high voltage transient during the blocking of fault current and, hence, to protect the fully opened LCSs. The main breaker can then open to block a fault current in Step 3. This applies for all types of fault. The last step, Step 4, is to restore the currents at the remaining healthy circuits while keeping the fault blocked by means of the mechanical switch at a faulty node (for dc line and converter faults) or by the opened main breaker and UFDs (for internal bus faults).

IV. ANALYSIS AND COMPARISON

A. Rating of Components

The rating of components within an MF-ICB is determined by the protection requirements rather than those for current flow regulation. An MF-ICB should withstand a maximum current and voltage during different fault events. The most severe condition is a solid internal bus fault at point B. This causes a maximum fault current flowing through the bridge-type BMB. Taking the bus fault in Fig. 10(b) as an example, the currents at all nodes will flow through the BMB, while for dc line or converter faults, current is fed by two nodes only. Therefore, if an MF-ICB can block a fault at bus B, it should be capable to block other types of faults.

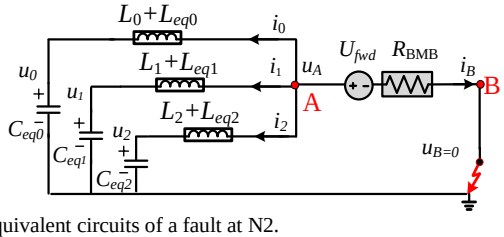

Fig. 11. Equivalent circuits of a fault at N2.

Let us assume that the MF-ICB starts its protection sequence when the total fault current exceeds 1.5 times the rated current (I_{rated}). The left-hand side IGBTs within LCS_{A1} and LCS_{A2} will immediately open, as shown in Fig. 10(b), while the UFDs at the lower bypass branches (UFD_{B1} and UFD_{B2}) will take several milliseconds to open. During this period, the magnitude of the fault current through the BMB, UFD_{A1}, UFD_{A2}, and the closed IGBTs within LCS_{A1} and LCS_{A2} will keep increasing. The equivalent circuits of the MF-ICB during this period are shown in Fig. 11, where L_0, L_1 and L_2 are the inductances of the current limiting reactors at the different nodes; L_{eq0}, L_{eq1}, L_{eq2} and C_{eq0}, C_{eq1}, C_{eq2} the inductances and capacitances of a connected dc network; and U_{fwd} and R_{BMB} the total forward voltage drop and resistances of IGBTs and diodes of the BMB. Since the LCSs have significantly fewer semiconductor switches compared to the BMB, their forward voltage drop and resistance are negligible. Since the capacitor of the CFC-LCS modules is blocked, it is not shown in Fig. 11.

The voltage at point A can be calculated as:

$$u_A(t) = R_{\mathrm{BMB}} i_B(t) + U_{fwd} \tag{8}$$

$$u_A(t) = (L_2 + L_{eq2}) \frac{di_2(t)}{dt} + u_2(t) \tag{9}$$

$$u_A(t) = (L_1 + L_{eq1}) \frac{di_1(t)}{dt} + u_1(t) \tag{10}$$

$$u_A(t) = (L_0 + L_{eq0}) \frac{di_0(t)}{dt} + u_0(t) \tag{11}$$

The MF-ICB must be able to withstand a maximum fault current, which will be reached only if all voltages of the healthy circuits are around the dc rated voltage (U_{rated}) before the UFDs start to act:

$$u_1(t) = u_2(t) = u_0(t) = U_{rated} \tag{12}$$

The currents at point A have the following relationship:

$$\frac{di_0(t)}{dt} + \frac{di_1(t)}{dt} + \frac{di_2(t)}{dt} + \frac{di_B(t)}{dt} = 0 \tag{13}$$

The current at point B (I_B) is given by combining (8)-(13):

$$I_B = 1.5 I_{rated} + \frac{U_{rated} - U_{fwd}}{R_{\mathrm{BMB}}} \left[1 - e^{\frac{-R_{\mathrm{BMB}}}{L_{\mathrm{hlthy}}} \times (t_1 - t_0)} \right] \tag{14}$$

where t_o is the time when the UFDs start to act and t_1 is the time when the UFDs are fully opened. The initial magnitude of the current is $1.5 I_{rated}$ as the MF-ICB starts to operate when the fault current exceeds 1.5 times the rated current. The total susceptance of the healthy circuits $1/\mathrm{L_{hlthy}}$ is given by

$$\frac{1}{L_{hlthy}} = \frac{1}{(L_0 + L_{eq0})} + \frac{1}{(L_1 + L_{eq1})} + \frac{1}{(L_2 + L_{eq2})} \tag{15}$$

The forward voltage drop U_{fwd} is negligible compared to the system voltage U_{rated}. Since L_{hlthy} is considerably larger than R_{BMB}, (14) can be further simplified to

$$I_B = 1.5 I_{rated} + \frac{U_{rated}}{L_{hlthy}} \times (t_1 - t_0) \tag{16}$$

This implies that the current rating of the bridge-type BMB of an MF-ICB should be no less than I_B to block a dc bus fault.

Although (16) was derived for a three-node MF-ICB, it can be modified for a generic MF-ICB with *n* nodes. In this case,

$$\frac{1}{L_{hlthy\_n\_node}} = \sum_{j=0}^{n-1} \frac{1}{(L_j + L_{eqj})} \tag{17}$$

Equation (16) would be modified to

$$I_B = 1.5 I_{rated} + \frac{U_{rated}}{L_{hlthy\_n\_node}} \times (t_1 - t_0) \tag{18}$$

The current rating of the LCS and UFD at an arbitrary node *j* should be no less than $I_{bypass,j}$. Thus,

$$I_{bypass,j} = 1.5 I_{rated} + \frac{1}{(L_j + L_{eqj})} \times \frac{U_{rated}}{L_{\mathrm{hlthy\_n\_node}}} (t_1 - t_0) \tag{19}$$

The previous expression is obtained by considering the worst scenario when the initial current ($1.5 I_{rated}$) is entirely contributed by node *j*. The total inductance at all nodes would be the same (*i.e.* $L_0 + L_{eq0} = L_1 + L_{eq1} = \cdots = L_n + L_{eqn}$). Given that the current rising at all nodes connected to the bus will be the same, (19) can be then further simplified to

$$I_{bypass,j} = 1.5 I_{rated} + \frac{U_{rated}}{(L_j + L_{eqj})} \times (t_1 - t_0) \tag{20}$$

If the total inductance at the nodes is not identical (*i.e.* different $L_j + L_{eqj}$), the maximum current exhibited by LCSs and UFDs at different bypass branches would be different. According to (19), the larger $(L_j + L_{eqj})$ is, the smaller $I_{bypass,j}$ would be and, hence, an LCS and an UFD with a smaller current rating could be selected. Conversely, for a smaller value of $(L_j + L_{eqj})$, both the LCS and the UFD would require a higher current rating.

The voltage ratings of the BMB (U_{BMB}) and UFDs (U_{UFD}) are determined by the peak voltage during the fault blocking. The peak voltage is, in turn, determined from the rating of associated surge arresters, which is typically selected as 1.5 times the dc system rating ($1.5 U_{rated}$) [27]. Hence,

$$U_B = U_{UFD} = 1.5 U_{rated} \tag{21}$$

The voltage rating of LCSs (U_{LCS}) is much smaller than $1.5 U_{rated}$. It only needs to exceed the voltage drop across the bridge-type BMB for current commutation:

$$U_{\mathrm{LCS}} = I_B \times R_{BMB} + U_{fwd} \tag{22}$$

B. Reduction of IGBTs

The MF-ICB device is compared with a conventional solution employing separate HCBs and CFCs by calculating the total number of IGBTs for each approach. For an MF-ICB with *n* nodes and *k* current-controlled dc lines, the total number of IGBTs (M_{MF}) is:

$$M_{MF} = M_{BMB} + M_{LCS\alpha} + M_{LCS\beta} \tag{23}$$

where M_{BMB}, $M_{LCS\alpha}$ and $M_{LCS\beta}$ are the IGBTs in the bridge-type BMB, CFC-LCS modules, and other LCSs, respectively. Equation (23) can be expanded as:

$$M_{MF} = ceil\left(\frac{I_B}{I_{igbt}}\right) \times ceil\left(\frac{1.5 U_{rated}}{U_{igbt}}\right) + \left(\frac{2n + 6k - 2}{n}\right) \times ceil\left(\frac{I_{bypass}}{I_{igbt}}\right) \times ceil\left(\frac{U_{LCS}}{U_{igbt}}\right) \tag{24}$$

where $n \geq 3$ and $n \geq (2k + 1)$, I_{igbt} and U_{igbt} are the current and voltage ratings of a single IGBT, and function $'ceil'$ rounds the elements up to the nearest integer.

Similarly, the total number of IGBTs for the conventional solution (M_{CS}) is calculated as:

$$M_{CS} = 2 \times \sum_{j=1}^{n} \left[ceil\left(\frac{I_{HCBMB,j}}{I_{igbt}}\right) \times ceil\left(\frac{1.5 U_{rated}}{U_{igbt}}\right) + ceil\left(\frac{1.5 I_{rated}}{I_{igbt}}\right) \times ceil\left(\frac{U_{LCS,HCBj}}{U_{igbt}}\right) \right] + 8 \times \sum_{h=1}^{k} \left[ceil\left(\frac{I_{HCBMB,h}}{I_{igbt}}\right) \times ceil\left(\frac{0.05 U_{rated}}{U_{igbt}}\right) \right] \tag{25}$$

where $I_{HCBMB,h}$ is the current rating of the main breakers of the HCBs. The term $0.05U_{rated}$ is the voltage rating of the CFC-LCS modules, which is 5% of the dc system's voltage [2].

TABLE II
COMPARISON OF THE NUMBER OF IGBTS FOR DIFFERENT N AND K

Number of nodes (n) and controlled dc lines (k)	IGBT number for MF-ICB	IGBT number for conventional solution	IGBT reduction in MF-ICB
n = 3; k = 1	1032	3156	2124
n = 4; k = 1	1372	4160	2788
n = 5; k = 1	1712	5164	3452
n = 5; k = 2	1730	5308	3578
n = 7; k = 2	2243	7316	5073
n = 7; k = 3	2261	7460	5199
n = 10; k = 2	3096	10328	7232
n = 10; k = 3	3114	10472	7358

A case study is undertaken considering DCCB ratings of 500 kV and 3 kA. IGBT 5SNA 3000K452300s is used. It can withstand a voltage of 4.5 kV and a current of 6 kA in transient conditions [30]. The total inductance at each node is assumed to be 0.1 H ($L_0 + L_{eq0}$). Results are summarized in Table II.

As it can be observed in Table II, for n = 3 and k = 1, an MF-ICB needs 1032 IGBTs only, while the conventional solution requires 3156 IGBTs instead—2124 additional IGBTs (67.3%). The increase in the number of IGBTs for a conventional arrangement will be more significant as n increases (*i.e.* 600+ more IGBTs per n), as more dc lines will share a single bridge-type BMB instead of using an individual HCB at each node. Moreover, the increase in the number of devices will also be apparent if k is larger (*i.e.* 100+ IGBTs more per k), as only CFC-LCS modules are included in an MF-ICB instead of incorporating separate CFCs. For instance, the MF-ICB reduces the IGBT count by 70.3% (7358) for a 10-node bus with 3 current-controlled dc lines.

C. Cost Considerations

For this exercise, the following costs per component are assumed: C_{igbt} for an IGBT, C_d for a diode, and C_{ufd} for a UFD. The total cost of an MF-ICB is thus given as:

$$C_{MF} = M_{MF} \times C_{igbt} + (2n-2) \times C_{ufd} + \left[4 \times (M_{BMB} + M_{LCS\alpha}) + M_{LCS\beta}\right] \times C_d \quad (26)$$

Notice that (26) considers 4 diodes per IGBT in a bridge-type BMB and LCSs, while those in CFC-LCS modules have one diode each. The total number of UFDs is $(2n-2)$. The total cost for the conventional solution is given by:

$$C_{CS} = M_{CS} \times (C_{igbt} + C_d) + n \times C_{ufd} \quad (27)$$

where one diode is associated to each IGBT.

A sensitivity analysis is performed to compare the cost of both solutions by modifying the cost of a UFD. The cost of a diode is set to $0.1C_{igbt}$ [13]. Given that UFDs are mechanical components, their cost should be low. Thus, C_{ufd} is assumed to be in the range of $5C_{igbt}$ to $100C_{igbt}$. Fig. 12 shows the ratio between the cost of an MF-ICB and that of the conventional approach (C_{MF}/C_{CS}) against the value of C_{ufd}. This ratio is used to effectively show the cost saving of the MF-ICB. As it can be observed, the ratio changes from 0.42 to around 0.5 for different C_{ufd}, n and k. This indicates that the cost of an MF-ICB is around 42-50% of the cost of conventional solution. In addition, for lower values of C_{ufd}, the ratio is also smaller and, thus, the cost reduction afforded by the MF-ICB is greater. This occurs as an MF-ICB reduces the number of IGBTs at the expense of using additional bypass branches (UFDs and LCSs); however, these branches do not significantly contribute to the total cost as the price of a UFD is significantly less than that of an IGBT, as discussed.

A similar sensitivity study is done when the value of C_d changes from $0.05C_{igbt}$ to $0.8C_{igbt}$. The value of C_{ufd} is kept as 50 times that of C_{igbt} (*i.e.* $C_{ufd} = 50C_{igbt}$). Results are given in Fig. 13. As it can be observed, the ratio C_{MF}/C_{CS} increases with an increase of C_d,which implies that the MF-ICB will have a reduced cost compared to the conventional solution. This occurs as one-IGBT-four-diode units are mainly adopted in an MF-ICB while two-IGBT-two-diode units are used in the conventional approach. Notably, even if C_d increases to a value $0.8C_{igbt}$, the cost of an MF-ICB is still about 76% of the cost of a conventional solution for different values of n and k—although C_d will be typically low ($0.1C_{igbt}$), translating to a ratio C_{MF}/C_{CS} of around 0.43.

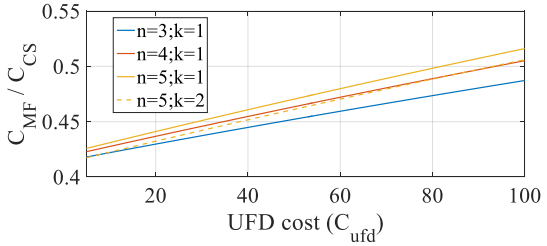

Fig.12. Impact of changing C_{ufd} on the cost ratio C_{MF}/C_{CS}.

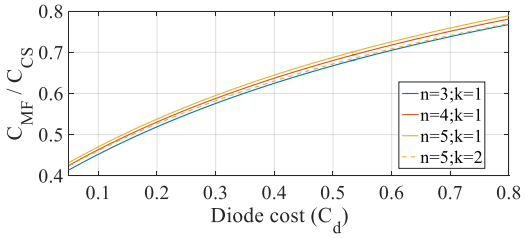

Fig. 13. Impact of changing C_d on the cost ratio C_{MF}/C_{CS}.

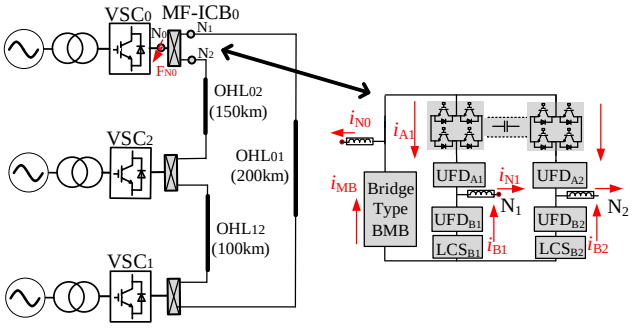

Fig. 14. Test system and current convention of the MF-ICB at VSC_0.

TABLE III
SYSTEM PARAMETER

Component	Parameter/control setting
DC line (per 50 km)	R = 0.57 Ω; C = 0.615 μF; L = 0.04678 H
VSC_0	Droop gain: –0.05 kV/kA; current reference: 2 kA; voltage reference:500 kV
VSC_1	Droop gain: –0.05 kV/kA; current reference: 1 kA; voltage reference:500 kV
VSC_2	Droop gain: –0.05 kV/kA; current reference: –2 kA; voltage reference:500 kV

V. Simulation Studies

Simulations are performed to verify the effectiveness of an MF-ICB to provide dc protection and current regulation. A three-terminal HVDC grid with an MF-ICB located at each terminal is adopted as a test system, as shown in Fig. 14. The dc system is rated at 500 kV. Overhead lines are considered and modeled as lumped π sections. All VSCs operate under voltage droop control [31], with relevant parameters given in Table III. To clearly show the performance of the MF-ICB, the focus is on the unit located at the dc terminal of VSC_0 ($MF\text{-}ICB_0$).

A. Current Regulation at OHL_{01}

The performance of $MF\text{-}ICB_0$ is assessed when regulating current I_{01} flowing through overhead line OHL_{01}. Simulation results are given in Fig. 15. Prior to current flow regulation being enabled, currents at OHL_{01}, OHL_{02} (I_{02}) OHL_{12} (I_{12}) are determined by the dc line resistances and the VSCs' controllers. At 3 s, $MF\text{-}ICB_0$ starts regulating I_{01} to 1.5 kA and this value is reached after 1 s. I_{02} almost reduces to zero due to the increase in I_{01}. I_{12} barely changes as OHL_{12} is not directly connected to $MF\text{-}ICB_0$ and, hence, the control of $MF\text{-}ICB_0$ will have less impact on I_{12}. At 7 s, I_{01} is required to change from 1.5 to –1 kA to assess current flow reversal. When I_{01} reaches 0 kA at 8 s, the operation of the CFC modules changes from buck to boost mode and, subsequently, the current is reversed. At ≈9 s, I_{01} is successfully regulated to –1 kA.

Fig. 15 also shows the voltage across the dc capacitor. As it can be observed, the voltage varies accordingly to regulate I_{01} to different values. However, the magnitude of the change in voltage is considerably small compared to the dc system rating (500 kV)—up to 20 kV only in the transient regime.

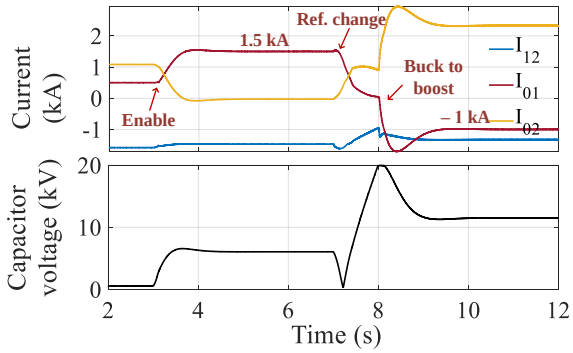

Fig. 15. Current flow regulation for OHL_{01}.

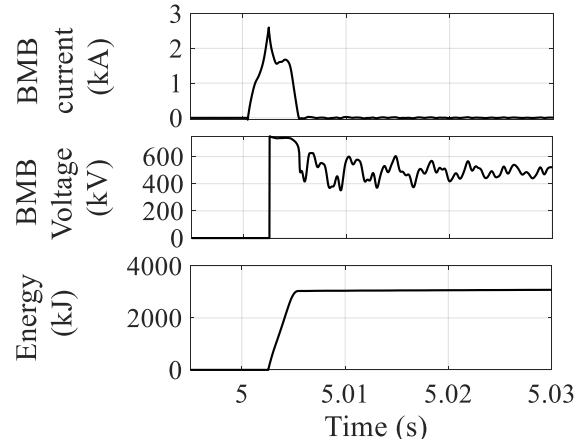

Fig. 16. Current, voltage and energy of the bridge-type BMB.

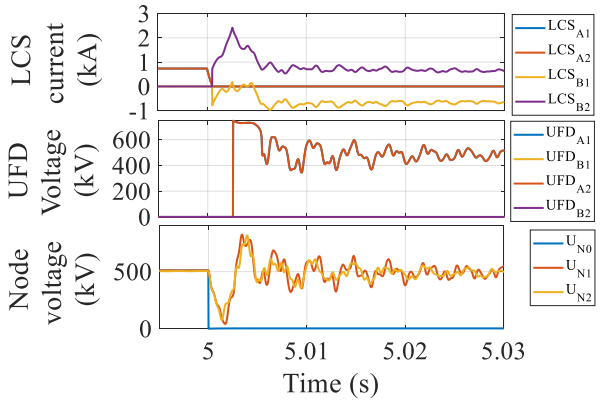

Fig. 17. LCS current, UFD and node voltage.

B. Isolating a Fault at N_0

A second test is undertaken to evaluate the use of $MF\text{-}ICB_0$ to block a solid fault at node N_0. The fault is applied at 5 s and it is detected in 0.5 ms; $MF\text{-}ICB_0$ then starts blocking the fault following the sequence illustrated in Fig. 9. Simulation results are given in Figs. 16 and 17.

Fig. 16 shows the current, voltage and absorbed energy of the bridge-type BMB. It can be observed that the fault current is blocked within 3 ms and that the maximum fault current is ≈2.6 kA only. The voltage across the BMB reaches 750 kV after the fault is blocked. This value is determined by the rating of the surge arrester (selected to 1.5 times the system rating, i.e. 750 kV). The absorbed energy is ≈3000 kJ.

Fig. 17 shows the currents of the LCSs and voltages of different UFDs and dc nodes. Before the fault, current flows through LSC_{A1} and LCS_{A2} only, while LSC_{B1} and LSC_{B2} are open. After fault detection, LSC_{A1} and LCS_{A2} immediately open for current commutation and, hence, their currents drop to zero. LSC_{B1} and LSC_{B2} close simultaneously and, as a result, fault current flows through them. At 5.003 s, the fault current is blocked by the BMB, but LSC_{B1} and LSC_{B2} remain closed to allow current flow between healthy circuits. The opened UFDs (UFD_{A1} and UFD_{A2}) withstand almost the same voltage across the BMB as they are in parallel, while the voltage across opened LCSs is negligible. The closed UFDs (UFD_{B1} and UFD_{B2}) have zero voltage across them. Since the fault occurs at N_0, its voltage (U_{N0}) drops to zero directly. The voltages at N_1 (U_{N1}) and N_2 (U_{N2}) will also drop due to the discharging of the capacitive component within dc overhead lines. However, once the fault is blocked, U_{N1} and U_{N2} will start to recover and the remainder healthy circuits can operate normally.

As it can be seen from the simulation results presented in this section, the system is well-protected by using MF-ICBs.

C. Isolating a DC Line Fault at N_1 and N_2

To further assess the performance of the MF-ICB, solid faults at nodes N_1 and N_2 where dc lines are connected are simulated in this section. The fault is applied at 5 s into the simulation for each test.

Figs. 18 and 19 show that the MF-ICB can successfully block a fault at N_1. The BMB within the MF-ICB opens at around 2.5 ms to reduce the magnitude of fault current from –6 kA to zero. An energy of 6000 kJ is absorbed by the surge

arrester during this period. The magnitude of the voltage across the BMB is 750 kV—determined by the rating of the surge arrester.

LCS_{A1} is fully open after fault detection (5.0005 s) and LCS_{B2} remains in an open state. This way, their currents are zero while the fault current is fully commutated to the BMB. Following current commutation, the current at LSC_{B1} is the same as the current at the BMB. After the BMB blocks the fault current, the current of LSC_{B1} also drops to zero. A current still flows between nodes N_1 and N_2 through LSC_{A2} during this fault event. The voltage magnitude across the opened UFDs (UFD_{A1} and UFD_{B2}) is around 750 kV, which is similar to the voltage across the BMB.

Fig. 19 also shows the voltages at different nodes within the network. After the fault happens, the voltage at the faulty node N_1 remains at zero. The voltages at N_2 and N_0 drop during the fault, but they return to pre-fault values after the fault is blocked. The voltage oscillation at N_0 is mitigated by the converter as it is in voltage droop control; however, the oscillation exhibited at N_2 is larger.

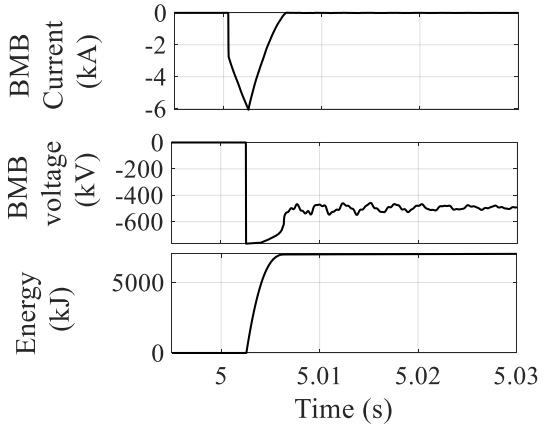

Fig. 18. Current, voltage and energy for the bridge-type BMB (fault at N_1).

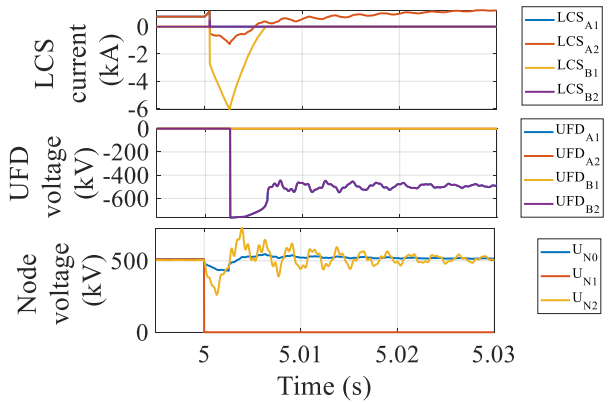

Fig. 19. LCS current, UFD and node voltage (fault at N_1).

An additional test is conducted but with a dc line fault applied at N_2 instead. Simulation results are given in Figs. 20 and 21. As it can be observed, the MF-ICB can also block the fault within 3 ms. The magnitude of the peak fault current is 4 kA, with an absorbed energy of around 4000 kJ.

During the fault blocking procedure, LCS_{A2} and LCS_{B1} are in a fully open state, followed by the opening of their UFDs. Hence, currents at LCS_{A2} and LCS_{B1} are zero. The fault current is then commutated to the BMB and LCS_{B2} (BMB and LCS_{B2} are in series after current commutation). After the BMB blocks the fault, the fault current drops to zero. Current keeps flowing between heathy nodes (N_0 and N_1) through LCS_{A1}.

After the fault is blocked by the BMB, the magnitude of the voltages across both the BMB and the opened UFDs are both 750 kV. The remaining healthy circuits start to recover and voltages at N_0 and N_1 return back to around 500 kV.

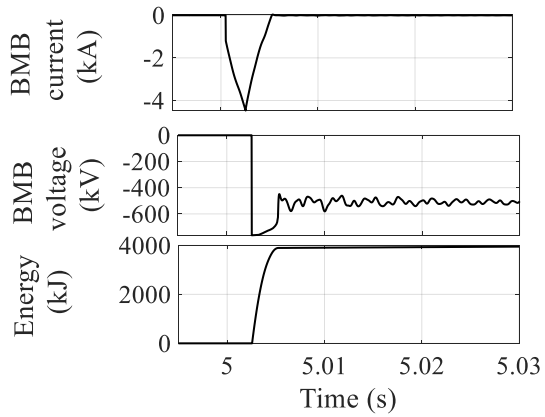

Fig. 20. Current, voltage and energy for the bridge-type BMB (fault at N_2).

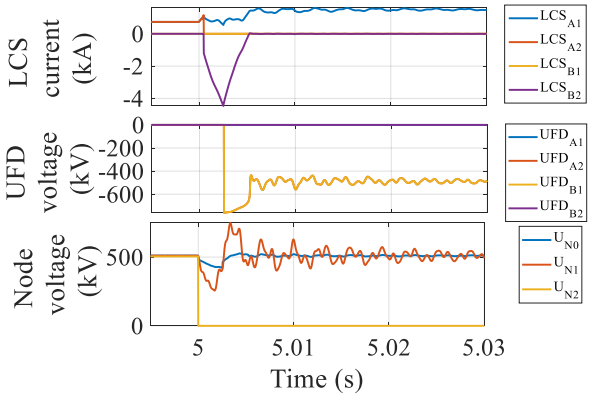

Fig. 21. LCS current, UFD and node voltage (fault at N_2).

D. Considerations Towards Prototype Development

Although the feasibility of the MF-ICB concept has been verified through simulation studies, significant efforts are still required towards the practical deployment of the presented solution. A way to facilitate this process is by assessing the performance of a real MF-ICB prototype. Tests embedding the device in a real dc grid, even at scaled-down ratings, would provide more detailed practical insight into the voltage and current dynamics of each component of the MF-ICB during breaking operations and current flow regulation.

Extra considerations related to the components' reliability, electromagnetic compatibility and mechanical enclosure would be required during the development of a real prototype. The design process would also give additional insight into associated components, such as driving circuits for IGBTs and control units. Although building an MF-ICB prototype would be highly desirable, this is a very challenging task which falls out of the scope of this paper; however, laboratory-scale MF-ICB devices should be built in the future to experimentally validate the work here presented.

VI. Conclusion

An innovative DCCB that provides dc protection and current regulation while reducing the semiconductor switch component count has been presented in this paper. For completeness, their control structure and a mathematical analysis is presented. Under regular operating conditions, the MF-ICB regulates dc currents using its CFC-LCS modules. Effective current regulation is achieved by alternating between buck and boost modes of operation of the CFC-LCS modules.

Following a dc fault event, the MF-ICB will temporarily stop current flow regulation and act to block a dc fault. The fault will be blocked within milliseconds and the currents in healthy circuits will not be interrupted even at the occurrence of a bus fault. The CFC function can be then recovered after fault isolation. The operating sequences for isolating a dc fault at different locations have been established. The design of an MF-ICB in terms of rating is informed with a mathematical analysis.

The use of MF-ICBs could be beneficial to a dc grid as it significantly reduces the amount of IGBTs when compared to a conventional solution based on separate HCBs and CFCs. Hence, the total cost for dc grid protection would be also decreased as a result. It is shown that the reduction in cost dramatically increases as the number of nodes and controlled dc lines increases. A cost sensitivity analysis has been carried out considering different prices for UFDs and diodes. This exercise further demonstrates the potential of the MF-ICB device.

The presented MF-ICB has been further studied through time-domain simulations where a three-terminal meshed dc grid is employed as a test system. Simulation results show that an MF-ICB can effectively regulate dc line current to different values in non-fault conditions. Current flow can be also reversed. Following a dc fault, the MF-ICB can isolate it to protect the reminder healthy circuits.

VII. References

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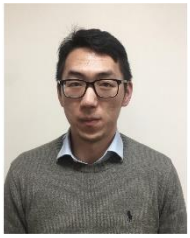

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