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Orientation-controlled Selective-area Epitaxy of III-V Nanowires on (001) Silicon for Silicon Photonics

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Abstract

Monolithic integration of III-V nanowires on silicon platforms has been regarded as a promising building block for many on-chip optoelectronic, nanophotonic, and electronic applications. Although great advances have been made from fundamental material engineering to realizing functional devices, one of the remaining challenges for on-chip applications is that the growth direction of nanowires on Si(001) substrates is difficult to control. Here, we propose and demonstrate catalyst-free selective-area epitaxy of nanowires on (001)-oriented silicon-on-insulator (SOI) substrates with the nanowires aligned to desired directions. This is enabled by exposing {111} planes on (001) substrates using wet chemical etching, followed by growing nanowires on the exposed planes. We demonstrate the formation of nanowire array-based bottom-up photonic crystal cavities on SOI(001) and their coupling to silicon waveguides and grating couplers, which support the feasibility for on-chip photonic applications. The proposed method of integrating position- and orientation-controllable nanowires on Si(001) provides a new degree of freedom in combining functional and ultracompact III-V devices with mature silicon platforms.

1. Introduction

In recent decades, integrating III-V semiconductors on silicon has been of great interest in electronics and photonics communities. In electronic applications, employing III-V semiconductors can improve the device speed by virtue of their high carrier mobility[1–3] while still being able to utilize the mature CMOS fabrication processes and low-cost silicon substrates. In photonic and optoelectronic applications, their direct bandgap brings an immediate benefit for realizing highly efficient light emitters on silicon,[4–7] and furthermore, their nonlinear optical properties and the capability to form quantized heterostructures provide a promising platform for nonlinear optics[8,9] and quantum optics.[10,11] Especially, silicon-on-insulator (SOI) based silicon photonic platforms, which employ thin SOI layers to confine and guide the light, have shown promises for chip-scale optical communications with a potential to outperform conventional electrical interconnects in terms of both bandwidth and energy consumption.

Despite a significant recent progress, however, integrating III-V materials onto silicon or SOI still remains a challenge. This is primarily owing to the mismatch of lattice constants and thermal expansion coefficients between III-Vs and silicon, which make it difficult to directly grow III-V materials on silicon without introducing crystal defects that can seriously deteriorate the device performance.[12,13] Therefore, heterogeneous integration methods such as wafer bonding and flip-chip bonding are typically employed to integrate III-V devices on silicon, although these methods require costly III-V substrates.[14] As an alternative approach, several epitaxy techniques have been proposed to directly grow high-quality III-V materials on silicon, such as growing graded buffers,[15] introducing dislocation filter layers,[16] which are based on planar thin film structures directly formed on bare silicon substrates. More advanced epitaxial techniques employ pre-treated silicon substrates. For example, aspect ratio trapping (ART) technique utilizes V-

grooves of silicon formed by wet etching to nucleate III-V from (111) sidewalls and confine the dislocations near the interface by its unique geometry.[17] This process is shown to be an effective approach to form III-V lasers on silicon with wafer scale processing,[18] while electrical injection could be challenging due to the geometry. Another non-planar approach is using pre-formed oxide template on silicon and growing III-V by filling in the template, which is termed as template-assisted selective epitaxy (TASE).[19,20] Lasing is also demonstrated by this approach, while the growth depends on diffusion of adatoms into the oxide template, and thus growth of ternary or quaternary III-V materials with precisely engineered material composition may be challenging due to different diffusion lengths of adatoms. Also, the material quality near the III-V/silicon interface is still defective in these techniques, and this could limit the efficiency and functionality of III-V/silicon hybrid devices.

To overcome these issues, epitaxy of III-V *nanowires* on silicon has recently gained attention to monolithically integrate high-quality III-V on silicon. Lattice-matching requirement is alleviated in nanowire approaches due to the extremely small interface area between nanowires and silicon, enabling threading dislocation-free growth of highly lattice-mismatched material systems, for example InAs nanowires on silicon that exhibits 11.6% of lattice mismatch.[21] In a similar manner, lattice-mismatched heterostructures can be formed inside of nanowires, such as axial or core/shell heterostructures, providing additional degree of freedom in bandgap engineering. It should also be noted that nanowire's small footprints make it one of the promising candidates for next-generation ultracompact optoelectronic devices[22,23], along with other emerging low-dimensional material platforms.[24,25] However, III-V nanowires typically grow along <111> directions regardless of the substrate orientation,[26,27] and it impairs the compatibility with Si(001) or SOI(001) substrates which are standard platforms in electronics and silicon photonics. There

have been reports on forming nanowires with their longitudinal axis aligned to <001> direction by controlling the growth conditions,[28,29] but it can be applied only for a limited material set and the growth on silicon has not been demonstrated so far. Template-based approaches, wherein III-V materials are grown inside pre-defined oxide tubes with <001> direction, have been also proposed to form vertical nanowires on Si(001),[30,31] while these processes exhibit sophisticated and complicated fabrication processes to pre-form the oxide tubes.

Here, we demonstrate bottom-up integration of III-V nanowires on SOI(001), which could be a novel approach of directly growing high-quality III-V on silicon platforms. The key enabling idea is to expose (111) planes of (001)-oriented substrates, from which nanowires can grow vertically with respect to the exposed crystal planes. In other words, nanowires grow along <111> direction of (001) substrates, and the position of nanowires and the direction of the nanowires among the four available <111> directions (*i.e.* $[\bar{1}11]$, $[1\bar{1}1]$, $[\bar{1}\bar{1}1]$, and $[111]$) can be controlled by combining selective-area epitaxy and anisotropic silicon wet etching. Based on this approach, as a proof-of-concept demonstration, one-dimensional (1D) nanowire arrays are grown on SOI(001) to form 1D photonic crystal cavities, wherein the nanowire cavity is optically coupled with a SOI waveguide and an output grating coupler. These results support that the proposed approach could be a path toward monolithically integrated ultracompact light sources on silicon photonic platforms. Although we have employed here 220 nm-thick SOI(001) substrates here to show promise for and compatibility with silicon photonics, the proposed method can be universally applied to Si(001) as well as other elemental and compound semiconductor materials.

2. Results and Discussion

2.1. Nanowire growth on (001)- and (111)-oriented substrates.

In typical III-V nanowire epitaxy, for both vapor-liquid-solid (VLS) and vapor-solid (VS) phase growths, the growth direction of nanowires is generally limited to <111> direction due to asymmetric surface energies depending on crystal planes. For (111)-oriented substrates, there is only one <111> direction exposed, which is surface normal direction by definition, as schematically shown in **Figure 1(a)**. On the other hand, for (001)-oriented substrates, there are four sets of <111> directions exposed, which are inclined by 54.7° from the surface normal direction (Figure 1(c)). To show these substrate orientation effects, we have grown GaAs nanowires on Si(111) and Si(001) substrates using metal-organic chemical vapor deposition (MOCVD). Here we have adopted selective-area epitaxy technique, wherein a dielectric mask with selectively exposed nanoholes is employed as a growth template. The nucleation occurs only from where silicon is exposed, and hence the position of nanowires can be lithographically controlled by this technique (see Methods for detailed growth template preparation and nanowire growth processes). Therefore, this approach ensures co-integration of nanowires with pre-patterned silicon structures with precise alignment, which is demonstrated in the later section. The nanowires grown on Si(111) are vertically aligned as seen in the angled and top-view scanning-electron microscope (SEM) images in Figure 1(c) and 1(e), which agrees with previous reports on various III-V nanowires.[32,33] On the contrary, the nanowires grown on Si(001) are randomly oriented along one of the four <111> directions, as in Figure 1(d) and 1(f). The portion of nanowires aligned to each <111> direction is in the range of 25 ± 2% (see Supporting Figure S1), indicating that there is no preferable choice of nanowire growth direction among the four exposed <111> family. The geometry of angled nanowires grown on Si(001) (Figure 1(d)) exhibits an average height of 716 nm, with a maximum and minimum height of 883 nm and 542 nm, and standard deviation of 68 nm. This is less uniform than vertical nanowires on Si(111) (Figure 1(c)) having an average height

of 874 nm, maximum and minimum height of 918 nm and 823 nm, and standard deviation of 21 nm. We speculate that the non-uniformity is stemming from two factors. First, as the growth takes place along angled direction, the position of nuclei formed inside of each nanohole will affect the nanowire height, unlike the case of vertical growths. Second, if more than one nucleus are seeded in a nanohole, and if they grow along different <111> directions, they will form phase boundary when merged, affecting the growth of nanowires.

These results indicate that although the position of nanowires can be controlled lithographically when (001)-oriented substrates is used, the growth direction of these nanowires cannot be controlled to a specific direction. The lack of controllability of the growth direction can be detrimental in nanowire-based optoelectronic devices, since the variation of nanowire directions results in unpredictable scattering of optical field and non-uniform current-injection from metal contact. Furthermore, when densely packed nanowires are grown, these randomly inclined nanowires inevitably merge with each other, which could form grain boundaries at the interface that can degrade electrical properties of nanowires. Therefore, controlling the growth direction of nanowires on Si(001) is crucial for many silicon photonic applications.

2.2. Controlling the growth direction of nanowires on SOI(001).

Here, we demonstrate that the challenges in controlling the growth direction of nanowires on (001)-oriented silicon can be overcome by exposing specific {111} facets of interest using wet chemical etching, followed by selective-area epitaxy from the exposed facets. As it is already well known and widely adopted in silicon microfabrication processes, {111} planes of silicon act as an etch-stop when anisotropic wet chemical etchants such as potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH) is used, due to the huge anisotropy between the etch rate of {111} planes and other planes.[34] A 220 nm-thick SOI(001) wafer is employed for the study

here, instead of Si(001), for two reasons; first, the buried oxide (BOx) layer is not etched by TMAH and thus works as a perfect etch-stop layer, making it easy to control the etched depth of silicon layer, and second, more importantly, the 220 nm-thick SOI(001) is a standard in silicon photonic platforms,[35] and thus the compatibility with silicon photonics can be demonstrated using SOI. While, it should be noted that exactly the same approach can be used for Si(001) platforms, not only SOI(001).

For the growth of nanowires on {111} sidewalls of SOI(001), four {111} sidewalls are first defined on SOI(001) by lithography and wet etching, and then silicon nitride (SiN_x) is conformally deposited as a growth mask by low-pressure chemical vapor deposition (LPCVD) followed by exposing nanoholes, as schematically shown in Figure 2(a) (see Methods for detailed fabrication processes). The SEM image in Figure 2(c) confirms the formation of four smooth {111} side planes with nanoholes patterned on two of the sidewalls. As only one <111> direction, *i.e.* surface normal direction, exists on these {111} sidewalls, the nanowires grow vertically with respect to the sidewall where nanoholes are patterned, as demonstrated in Figure 2(d). In other words, the growth direction can be perfectly controlled by exposing {111} sidewalls of interest. Using this approach, nanowires can be formed as well-ordered arrays by patterning arrays of nanoholes on a sidewall. As an example, interdigitated nanowire arrays are fabricated bottom-up, as shown in Figure 2(f), by patterning nanohole arrays on two {111} sidewalls facing each other (Figure 2(e)). We note that a similar nanowire structure is recently demonstrated on III-V substrates using gold-catalyzed nanowire epitaxy, as a versatile platform for various quantum devices,[36] implying that our proposed approach could be a stepping stone for realizing such advanced applications on silicon platforms.

However, the diameter and height of nanowires in Figure 2(f) are not identical, with the nanowires on the right-hand side fatter than the nanowires on the other side. As GaAs nanowires tend to grow fatter and shorter by increasing the diameter of exposed nanoholes on silicon,[33] the non-uniformity of nanowire geometry could be stemming from the non-uniform opening size of nanohole patterns for nanowire growth. Nanoholes on the right {111} plane in Figure 2(e) is adjacent to the top (001) surface of the SOI layer, while nanoholes on the left plane is patterned on the middle of the {111} plane (see Supporting Figure S2 for details). This is due to a slight misalignment between the wet-etched patterns and nanohole patterns during the electron-beam writing process. Nanoholes are exposed by dry-etching the silicon nitride layer using e-beam resist as an etch-mask, and the thickness of the e-beam resist gets thicker on the slanted {111} sidewalls compared with {001} surface due to the viscosity of e-beam resist. When e-beam resist is thicker, etch rate of small features decreases, meaning that the etch rate of nanoholes on the right sidewall will be faster than that on the left sidewall, resulting in larger nanohole diameter, and thus fatter nanowires.

To verify this speculation, the effect of nanohole position on the nanowire growth is further studied by gradually modulating the position of nanoholes with respect to the {111} sidewall, as shown in Figure 3(a) (See also Supporting Figure S3). The nanohole position spans from (001) surface to {111} sidewall with 20-nm-offset. In other words, some of the nanoholes are exposed on (001) surface, some on the corner of (001) and {111} surface, and some on the {111} sidewall. The morphology of nanowires grown from these intentionally tuned nanoholes is shown in the SEM image in Figure 3(b). The growth direction of nanowires from the holes on (001) surface is random, as already shown from nanowire arrays grown on Si(001) surface in Figure 1(f), while the nanowires grown from nanoholes on the corner and on {111} surface grows vertically with

respect to the {111} surface. Also, the nanowires grown at the corner are fatter than the nanowires on the center of {111} sidewall, which agrees with the tendency observed in Figure 2(f). To study the interface of nanowires and substrate, cross-sectional scanning transmission electron microscope (STEM) images of a nanowire on a {111} sidewall are measured by slicing the sample using focus ion beam (FIB) milling. As shown in the bright-field STEM image in Figure 3(c), a smooth Si{111} surface is formed on SOI(001) by wet etching, and 20 nm-thick silicon nitride mask is conformally deposited on the top and slanted Si planes. GaAs nanowire is grown vertically from the exposed nanohole on {111} surface. The close-up STEM image in Figure 3(d) and 3(e) shows the nanowire/substrate interface with the exposed hole diameter of around 41 nm. It is worth mentioning that the exposed diameter of 41 nm is smaller than the opening size of the topside of silicon nitride layer, which is around 60 nm based on SEM. The STEM images in Figure 3(d) and 3(e) clearly show that the silicon nitride is not vertically nor symmetrically etched, since the physical etching in dry etcher mostly occurs along perpendicular direction from (001) surface. We attribute this to one of the reasons for non-uniformity of nanowire geometry. In the STEM image, it can be clearly observed that the nanowire integrated on SOI(001) are grown along <111> direction perpendicular to the exposed {111} surface, and the nanowire is free of threading dislocations despite the lattice mismatch of 4.1% between GaAs and silicon due to the ultrasmall interface area (See Supporting Figure S4 for details). However, high density of stacking faults is observed along the zinc-blende GaAs nanowires, which is commonly observed from GaAs nanowires grown on Si in vapor-solid phase growths.[37] These stacking faults in nanowires could be reduced or eliminated by tuning the growth conditions of nanowires, such as growth temperature and V/III ratio.[38]

2.3. Integration of nanowire arrays with SOI(001) photonic components.

Based on the selective-area nanowire growth on {111} sidewalls of (001) substrates shown above, the feasibility and usefulness of integrating nanowires with silicon photonic platforms are justified by forming ordered nanowires on pre-patterned SOI(001) platforms with passive photonic elements. As a proof-of-concept demonstration, we form nanowire array-based photonic crystal cavities coupled with conventional SOI ridge waveguides and output grating couplers by employing our approach of growing nanowires on {111} sidewalls, combined with dry etching of silicon. As shown in the schematic illustration in Figure 4(a), 220 nm-thick SOI(001) wafer is first wet-etched to expose {111} crystal planes, followed by dry etching of silicon to form ridge waveguides, output grating couplers, and trapezoidal silicon stripes for nanowire growth. The following processes are identical to the processes shown above, *i.e.* silicon nitride mask deposition, nanohole patterning, and nanowire growth (see detailed processes in Methods and Supporting Figure S5).

Here, we adopt a one-dimensional (1D) photonic crystal laser cavity design composed of a nanowire array aligned on a {111} sidewall of SOI(001). This structure can exhibit high Q factor with extremely small footprint, which is promising for compact light sources such as nanolasers and photonic crystal LEDs, as we have theoretically proposed elsewhere recently.[39] The proposed nanowire laser cavity design is composed of 19 nanowires on a silicon stripe made by combination of wet etching and dry etching (Supporting Figure S5(e)). To demonstrate the potential for on-chip photonic applications, the nanowire cavity is butt-coupled to a ridge waveguide having a width of 440 nm and height of 220 nm. The distance of adjacent nanowires is set to 400 nm for the nanowires at the periphery of the 1D array, while the distance is gradually tuned to become 350 nm for nanowire in the center for optical confinement. The position and number of nanowires are carefully determined to simultaneously realize high Q factor, high coupling efficiency, and

ultracompact device size.[39] In the proposed design, the footprint of the nanowire cavity is only $6.7 \times 1.0\ \mu m^2$.

The top-view SEM images in Figure 4(b) and 4(c) show the SOI platform prepared for nanowire epitaxy. A 1D nanohole array is patterned on the {111} sidewall of a trapezoidal silicon stripe. The silicon nitride mask is removed around the nanowire array (noted as 'exposed Si' in Figure 4(b)), so that the exposed Si area can work as a diffusion barrier of adatoms during nanowire epitaxy and thus promote uniform growth of nanowires by limiting the diffusion area of adatoms on the surface.[40,41] A 1D GaAs nanowire array is grown on this platform, and as shown in Figure 4(d) and 4(f), the nanowires grown are aligned vertically on the {111} sidewall of the silicon stripe. Although the as-grown nanowires form a 1D array with perfect alignment, however, the diameter and height of nanowires are not uniform, which could be due to the fluctuation of the geometry of patterned nanoholes as these nanoholes are defined on slanted planes. The 19 nanowires exhibit average height of 808 nm, with the maximum and minimum height of 898 nm and 713 nm, and the standard deviation of 62 nm. The average diameter is 190 nm, with the maximum and minimum diameter of 226 nm and 147 nm, and the standard deviation of 18 nm (SEM of other arrays also shown in Supporting Figure S6). The non-uniformity of the nanowire size will not only affect the cavity mode wavelength, but will degrade the cavity Q factor,[6] and thus needs to be improved for high-Q cavities. For improved uniformity, we anticipate that either wet etching approach or modified dry etching approach could be implemented. Because wet etching of the silicon nitride layer is isotropic when HF or BOE solutions is used, this will ensure simultaneous exposure of nanohole patterns on the wafer surface and slanted sidewalls. Alternatively, dry etching method can be still utilized by loading the sample roughly 54.7°-tilted, so that the nanoholes on the slanted sidewall of interest face upwards and vertical etching can occur on these sidewalls.

To verify the cavity properties and waveguide-coupling characteristics, the nanowire array is optically pumped by a pulsed laser with a 660 nm wavelength, and the emission spectra are resolved using a commercial 2D InGaAs focal plane array detector (see Methods for measurement setup). The emission pattern in Figure 5(a), wherein the pump laser is blocked by a filter and represents only the emission from nanowires, shows light emission on top of the nanowire array as well as from the output grating coupler, indicating that the emitted light from nanowires is coupled to the SOI waveguide, transmitted, and out-coupled by the grating coupler. Next, direct emission from nanowires to the free space and the emission from the grating coupler are separately resolved to investigate the cavity and coupling characteristics, as shown in Figure 5(b), under the average pump power of 8.6 μW. Multiple cavity peaks are observed by pumping the 1D nanowire array, with two sharp peaks (λ_1 and λ_2) and several other broad peaks. These sharp peaks and some of the broader peaks are also measured from the output coupler, while the broad spontaneous emission is not observed, indicating that the coupling of these confined modes to the waveguide is stronger than spontaneous emission from the nanowires. On the other hand, when the PL of GaAs nanowires grown on Si(001) area (Figure 1(d)) is measured with the same pump power of 8.6 μW, only a broad spontaneous emission is observed, as shown in Figure 5(c), substantiating that the sharp peaks are originating from photonic crystal cavity modes (See Supporting Figure S7 and S8 for additional PL data).

The origin of these peaks is studied by three-dimensional (3D) finite-difference time-domain (FDTD) simulations (Lumerical FDTD), by employing actual dimensions of as-grown nanowires in the simulation model. Two cavity modes are found from the FDTD simulation, with the cavity mode wavelengths at 1430 nm and 1475 nm and cavity Q factors larger than 100 (Supporting Figure S9). These wavelengths almost perfectly match with the two sharp peaks (λ_1 and λ_2)

observed from photoluminescence (PL) measurement in Figure 5(b), and thus we conclude that the calculated field profiles (shown in Supporting Figure S9) correspond to the measured cavity modes at the mode wavelengths of λ_1 and λ_2. Other cavity peaks at shorter wavelengths, such as two peaks around 1200 nm observed from the PL in Figure 5(b), were not identified by FDTD simulations. This could be because the Q factor of other cavity modes are too small, as suggested by broader cavity linewidths shown in Figure 5(b), and cannot be resolved from FDTD simulations due to a quick decay of optical field. For example, the measured linewidth (full-width at half-maximum) of two distinctive peaks around 1200 nm are both around 13-15 nm, indicating that the Q factor is below 100. It should be noted that the Q factor and coupling efficiency of two cavity modes (λ_1 and λ_2) calculated by FDTD simulations are far from ideal due to the non-uniformity of nanowire dimensions. If all 19 nanowires exhibit identical diameter of 220 nm and height of 1000 nm, then this nanowire cavity will show high cavity Q factor of ~ 38,800 and coupling efficiency of 23.8 % at a cavity peak wavelength of 1515 nm (See Supporting Figure S10 for details).

The nanowires grown here for the demonstration of waveguide-coupled nanowire cavities are un-passivated GaAs nanowires. This implies that the emission observed in Figure 5(b) is not from band-edge emission, but from surface states and impurity states,[42,43] while the band-edge emission from the nanowires at the GaAs bandgap around 800-900 nm is not observed due to the detector cutoff. Therefore, although the sharp emission peaks from cavity modes and their waveguide-coupling observed here support the feasibility of proposed approach for monolithic and ultracompact photonic crystal elements on SOI(001) photonic platforms, there is no optical gain overlapping with the cavity modes. If the proposed architecture is to be employed as photonic crystal lasers on silicon photonic platforms, nanowires need to be made of materials with optical gain at these wavelengths, such as InGaAs or InGaAsP with surface passivation, and also need to

have uniform dimension for high Q factor. As it has been recently shown that uniform InGaAs nanowires with proper passivation can be formed on patterned silicon platforms[4,44] and room-temperature lasing at telecom wavelengths can be realized by this approach,[5] the proof-of-concept demonstration here suggests that telecom lasers on SOI(001) platforms can be realized by combining InGaAs nanowires with proposed approach.

3. Conclusion

In summary, we have shown a method to deterministically control the growth direction of III-V nanowires on SOI(001) platforms by catalyst-free selective area epitaxy. The enabling technique is defining {111} planes on (001) substrates by wet chemical etching, where nanowires grow vertically with respect to the exposed planes. The GaAs nanowires grown on SOI(001) were free of threading dislocations due to the small interface area, and the effect of nanohole patterning on the nanowire geometry is investigated to understand the mechanism of growths on the slanted sidewalls. Using this approach, one-dimensional nanowire arrays are grown on SOI(001) platforms with optical waveguides and output grating couplers, from which waveguide-coupled photonic crystal cavity modes are observed by optically pumping the nanowire arrays. These results indicate that the proposed method could be utilized as monolithic lasers on silicon photonic platforms. We believe that the proposed nanowire integration technique could be a building block for various nanophotonic and electronic components on (001) silicon-based platforms, such as on-chip light sources, quantum emitters, filters/resonators, bio-/chemical sensors and vertical nanowire field effect transistors (FETs).

4. Experimental Section

4.1. Fabrication.

An undoped 6-inch SOI(001) wafer with an SOI layer thickness of 220 nm and a buried oxide (BOx) layer thickness of 2 μm was first cleaned by Piranha solution followed by 6:1 BOE solution to remove surface contaminants and native oxide. Next, a 20-nm-thick silicon dioxide was thermally grown in furnace at 900 ˚C as a mask for wet etching. Then, e-beam lithography and dry etching were conducted to define wet-etch patterns on the oxide mask. The wafer was etched in TMAH (20 wt.% in DI water) at 70 ˚C for 18 min, followed by rinsing with DI water. Then, the oxide mask was stripped by 6:1 BOE solution. Next, electron-beam lithography and dry etching were conducted using e-beam resist as an etch-mask to make vertical silicon patterns, including silicon stripes, ridge waveguides and output grating couplers. After the dry etching, a 20-nm-thick silicon nitride (SiN_x) mask was deposited by low-pressure chemical vapor deposition as an epitaxial growth mask, which is resistant to BOE solution. Next, electron-beam lithography and dry etching were carried out to pattern nanoholes on wet-etched {111} crystal planes. Lastly, the SOI(001) wafer was diced into pieces and cleaned for nanowire epitaxy.

4.2. Nanowire growth.

Nanowire epitaxy was carried out by catalyst-free selective-area epitaxy using a low-pressure (60 torr) Emcore D-75 MOCVD reactor. Following the substrate preparation, the sample was cleaned in a 6:1 BOE solution to remove native oxide and was immediately loaded into the MOCVD reactor. The reactor temperature was ramped up to 875 ˚C and was kept for 15 min to remove the native oxide possibly formed during the sample loading. The temperature was then ramped down and stabilized at 680 ˚C for nanowire growth. Triethylgallium (TEGa) and tertiarybutylarsine (TBAs) precursors were switched on simultaneously and brought into the MOCVD reactor using purified hydrogen as carrier gas, where the V/III ratio was kept at ~100 for 30 min with the molar flow rate of [TEGa] = 5.41×10^{-7} mol/min and [TBAs] = 5.45×10^{-5} mol/min.

After the nanowire epitaxy, the reactor temperature was cooled down in a TBAs overpressure ambient to prevent desorption.

4.3. Optical characterization.

The nanowire arrays were optically pumped at room temperature (293K) by a pulsed supercontinuum laser (SuperK EXTREME EXW-12, NKT Photonics) with 660 nm laser wavelength, 30 ps pulse duration and 78 MHz repetition rate. Normal incidence was employed in the micro-photoluminescence (μ-PL) setup, in which the pumping source and the sample emission were focused and collected through a 50× objective lens (NA=0.42). The laser beam focused on the substrate has an estimated spot size of 2 μm. The emission from nanowire array and grating was directed to and resolved by an Acton SP-2500i spectrometer (Princeton instruments) equipped with a liquid nitrogen-cooled commercial 2D InGaAs focal planar array detector (2D-OMA, Princeton instruments). A 695 nm long pass optical filter was placed before the front entrance of the spectrometer to block the pump laser. The emission patterns from the nanowire arrays and output couplers were spatially captured by the live imaging mode of the 2D InGaAs detector with the pump beam located near the center of the nanowire array.

Supporting Information
Supporting Information is available from the Wiley Online Library or from the author.

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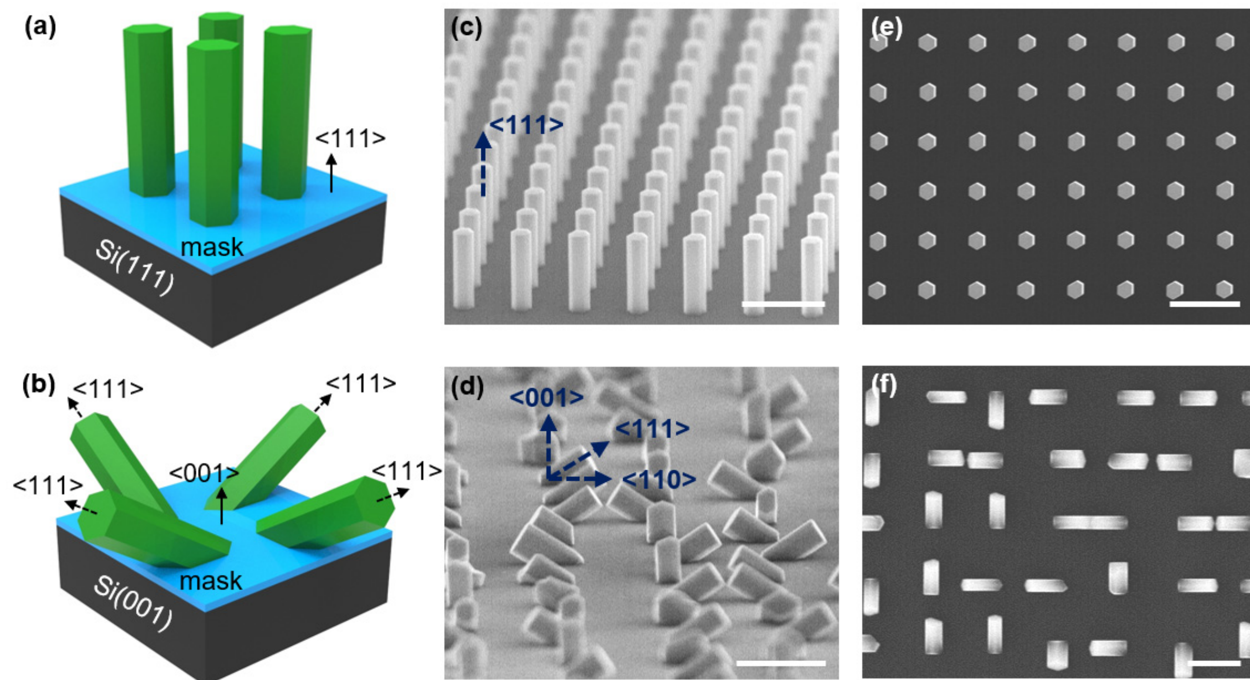

Figure 1. GaAs nanowires grown on (111) and (001) surfaces of silicon by selective-area epitaxy. Schematics of nanowire array on (a) Si(111) and (b) Si(001). 75º-tilted SEM images of nanowire array on (c) Si(111) and (d) Si(001), and corresponding top-view SEM images of (e) Si(111) and (f) Si(001). All scale bars are 1 μm.

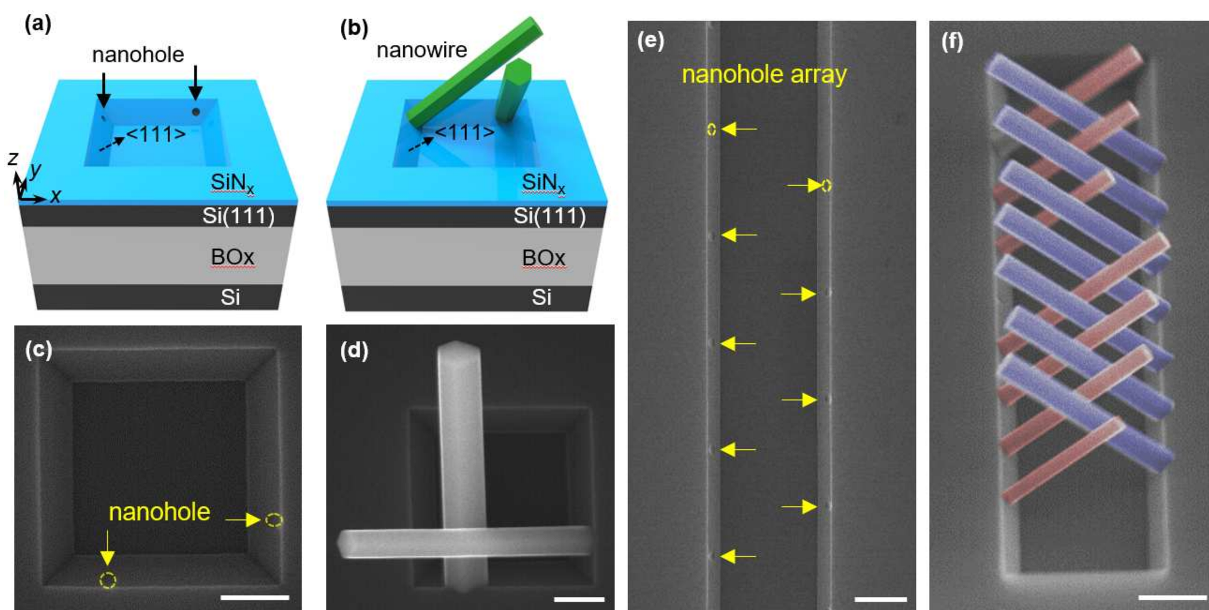

Figure 2. Proposed approach of controlling nanowire growth on (001) platforms. Schematics of (a) nanohole pattern on wet-etched {111} sidewalls of SOI(001) and (b) nanowires grown from nanoholes. Top-view SEM images of (c) nanohole patterns on two (111) sidewalls and (d) GaAs nanowires grown from the nanoholes. (e) Top-view SEM image of nanohole pattern on two {111} sidewalls and (f) 75^0-tilted false-color SEM image of interdigitated nanowires grown from the pattern. Scale bars, (c,d) 250 nm, and (e,f) 500 nm.

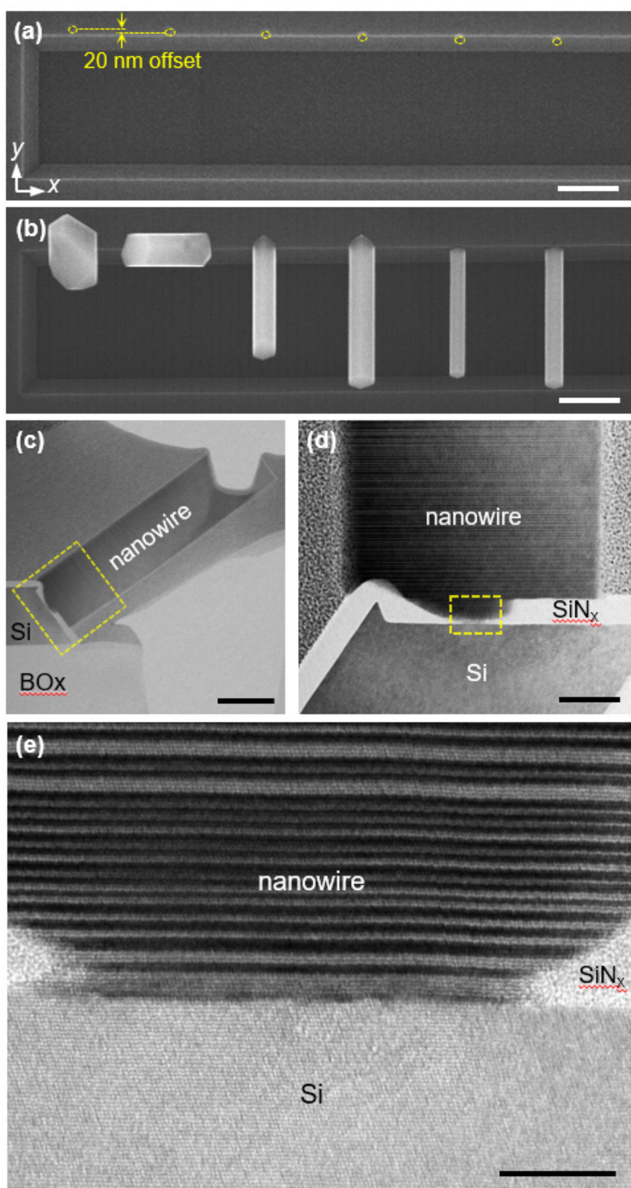

Figure 3. SEM images of (a) nanoholes patterned with 20 nm offset along *y*-direction and (b) nanowire growth results. (c,d,e) Cross-sectional bright-field STEM images of a nanowire on SOI(001) platform. (d) is a close-up image of dashed region in (c), and (e) is a close-up image of nanowire/silicon interface area in (d). Scale bars, (a) 500 nm, (b) 1 µm, (c) 200 nm, (d) 50 nm, and (e) 10 nm

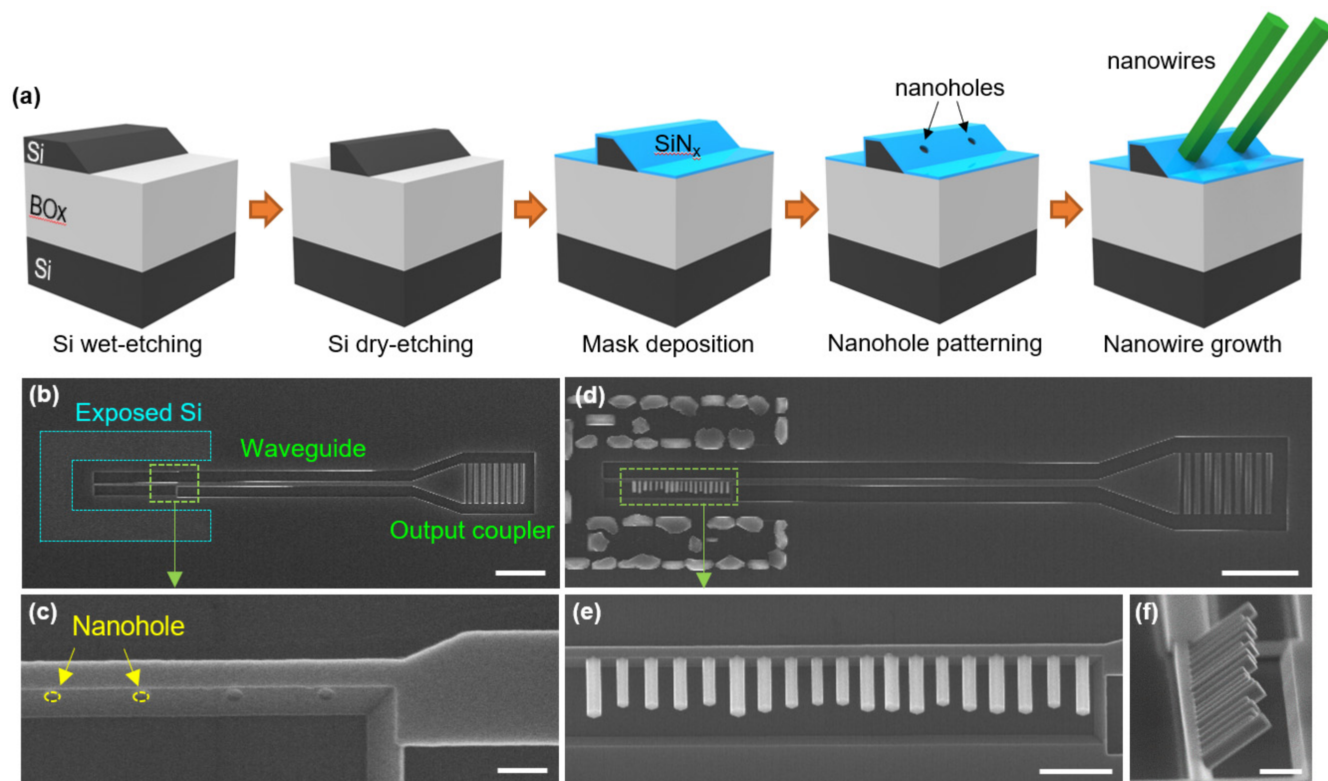

Figure 4. (a) Schematic of fabrication processes for nanowire array photonic crystals on patterned SOI platforms. (b,c) Top-view SEM images of fabricated nanohole patterns with SOI waveguide and output grating coupler, and (d,e) top-view SEM images after nanowire growth. (f) 75º-tilted SEM image of the nanowire array in (e). Scale bars, (b) 5 µm, (c) 200 nm, (d) 5 µm, (e) 1 µm, and (f) 500 nm.

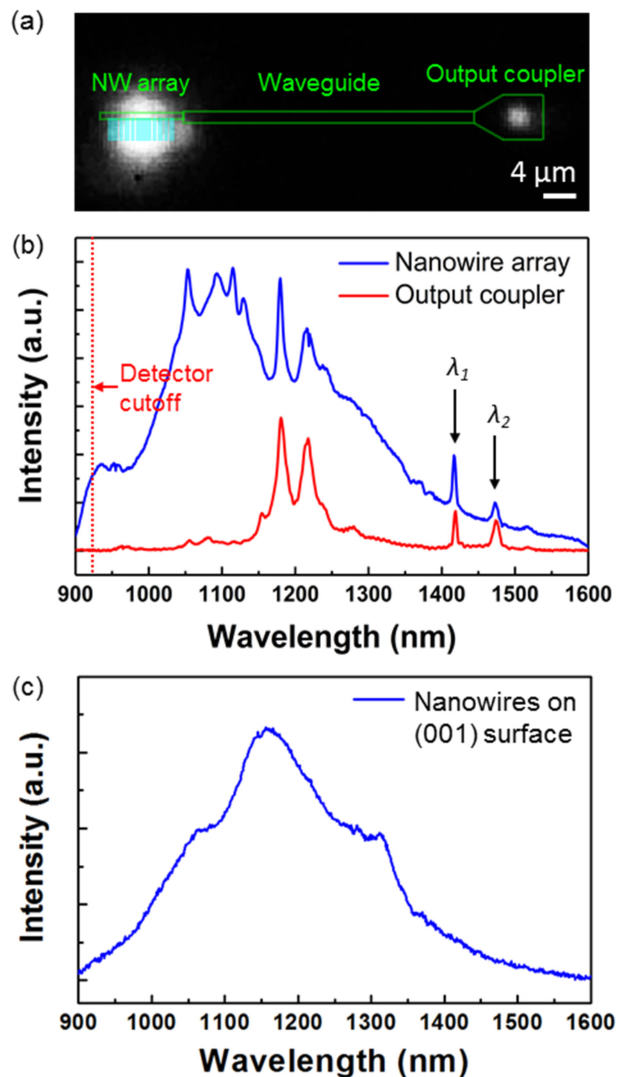

Figure 5. (a) Emission from an optically pumped nanowire array connected to a SOI waveguide and an output coupler. (b) Emission spectra from nanowire array and from output coupler, indicating waveguide coupling of cavity modes. (c) Emission spectra from 2D nanowire array grown on planar area of Si(001) surface.

Integration of III-V nanowires on silicon (001) platforms is demonstrated, with the capability to control the position and orientation of nanowires. Nanowire array-based photonic crystal cavities are formed on silicon-on-insulator photonic platforms by this approach, substantiating that the proposed method could be utilized for combining functional and ultracompact III-V devices with mature silicon platforms.

Keyword: nanowires, III-V on Si, monolithic integration, silicon photonics, photonic crystals

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Orientation-controlled Selective-area Epitaxy of III-V Nanowires on (001) Silicon for Silicon Photonics

ToC figure