# A Step-by-step Modelling Approach for SiC Half-bridge Modules Considering Temperature Characteristics

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***Abstract*—In this paper, a detailed step-by-step modelling approach is proposed for Silicon Carbide (SiC) MOSFET half-bridge power modules. The drain-to-source current, anti-parallel diode and parasitic capacitors are accurately modelled considering temperature dependency. A step-by-step parameter extraction method based on datasheet is introduced. A SPICE model is built based on the proposed modelling approach for a commercial power module. The model is verified by comparing experiment and PSpice simulation results of the same double pulse tester (DPT), which proves the effectiveness of the modelling approach for analysing switching losses and converter design. The proposed modelling approach can help the converter designers quickly and accurately develop their own models for SiC MOSFET power modules.**

## I. Introduction

Silicon Carbide (SiC) MOSFETs have been becoming very attractive for high efficiency and high power density applications due to their superior properties. Comparing to Si IGBTs, SiC MOSFETs have the advantages such as low on-resistance, fast switching speed, low switching losses and high junction temperature capability [1]. However, high switching speed of SiC devices brings to more serious electromagnetic interface (EMI) issues due to the higher $dv/dt$ and $di/dt$ during the switching transients [2]. Moreover, the efficiency and power density of the converters highly depend on the switching losses during the switching transients. Experimental approaches can be used to mitigate EMI issues and optimize the efficiency and power density by multiple rounds of prototype testing, which are both time and money consuming. An alternative approach is the simulation-based design of power electronic converters. To accurately simulate the EMI and switching losses, an accurate transient model of SiC MOSFETs is required to predict the waveforms of the switching transients [3].

Although many manufacturers have provided simulation models for their discrete SiC MOSFETs, there are very few commercial models for SiC MOSFET power modules. The converter designers often need to build the model for the power modules by themselves. However, most converter designers are not expert in semiconductors. A simple and detailed modelling approach that can be used for various SiC MOSFET power modules is required to help these designers.

There have been various models presented in the literature [4]. An accurate SiC MOSFET model is built in [2] by measuring the $I_{DS}$-$V_{DS}$ characteristics of the high-voltage and high-current region and the on-state capacitance characteristics. However, additional measurement equipment and test circuits are required for this model, which might not be available for converter designers. From this perspective, a datasheet-based modelling approach without additional experimental measurements is preferred because it can be adopted by all designers. A datasheet-based SiC MOSFET model is proposed in [5] with wide temperature range. Another accurate subcircuit model of SiC half-bridge modules is proposed in [3] for switching-loss optimization based on datasheet. However, both models used segmented capacitance models which might bring convergence problem [6]. To solve the convergence problem, a non-segmented model is proposed in [7].

SiC MOSFET models usually contain complicated nonlinear equations and multiple parameters to accurately model the current and capacitance characteristics. Although the same model can be used for different power modules, the parameters in the model are distinct. Therefore, the model parameters should be extracted based on the datasheet of specific power modules. Although there are various models in the literature, the parameter extraction procedure of these models are either too complicated or not well-established, which hinders the application of the models for converter designers. Therefore, a step-by-step parameter extraction procedure is required.

In this paper, a step-by-step modelling approach for SiC MOSFET half-bridge power modules is proposed considering temperature characteristics. The drain-to-source current, anti-parallel diode and parasitic capacitors are accurately modelled based on datasheet. The temperature dependency is considered. A step-by-step parameter extraction approach of each component is clearly introduced. A SPICE model for a commercial power module is built based on the proposed modelling approach. The established model is verified by comparing experiment and PSpice simulation results of the same double pulse tester (DPT). This modelling approach can be easily applied to model other SiC MOSFET power modules so that it can help converter designers develop their own model quickly and accurately.

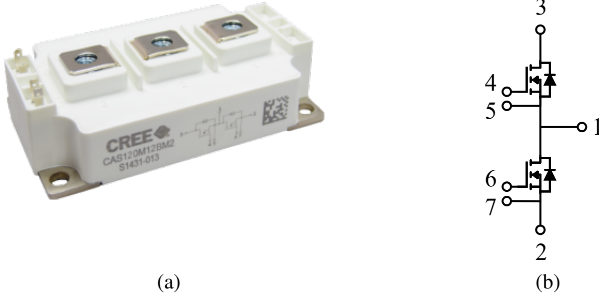



Figure 1. A 1200-V 120-A SiC MOSFET Half-Bridge Power Module CAS120M12BM2: (a) Package, (b) Schematic,

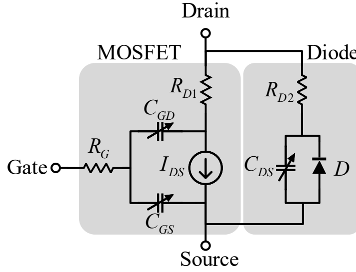



Figure 2. Subcircuit model of a pair of SiC MOSFET and anti-parallel diode in the power module.

## II. Model Description

A 1200V 120A SiC half-bridge module CAS120M12BM2 [8] from Wolfspeed is used to explain the proposed modelling approach. The same approach can be used for other SiC MOSFETs. The power module is shown in Fig 1a. As shown in Fig. 1b, the half-bridge module is packaged with two pairs of SiC MOSFETs and anti-parallel SiC Schottky diodes. Fig. 2 shows the subcircuit model of a pair of SiC MOSFET and anti-parallel diode in the module. The model consists of three major parts: drain-to-source current $I_{DS}$ model, diode model and capacitance models. These three parts are modelled respectively.

### A. $I_{DS}$ model

In Fig. 2, a voltage-controlled current source $I_{DS}$ and a series resistor $R_{D1}$ are used to model the drain-to-source current of the SiC MOSFET. The model is based on the standard MOSFET level 1 SPICE model [9]:

if $V_{DS} < 0$ or $V_{GS} < V_{GS(th)}$,

$$I_{DS} = 0 \tag{1}$$

if $0 < V_{DS} < V_{GS} - V_{GS(th)}$,

$$I_{DS} = K_p \left( V_{GS} - V_{GS(th)} - \frac{V_{ch}}{2} \right) V_{ch} \left(1 + \lambda V_{ch}\right) \tag{2}$$

if $V_{DS} > V_{GS} - V_{GS(th)}$,

$$I_{DS} = K_p \frac{\left(V_{GS} - V_{GS(th)}\right)^2}{2} \left(1 + \lambda V_{ch}\right) \tag{3}$$

$$K_p = K_{p1} + K_{p2} \left(V_{GS} - 10\right) \tag{4}$$

$$V_{ch} = V_{DS} - R_{D1} I_{DS} \tag{5}$$

where $V_{GS}$ and $V_{DS}$ are the gate-to-source and the drain-to-source voltages respectively; $V_{ch}$ is the channel voltage applied to the voltage-controlled current source $I_{DS}$; $V_{GS(th)}$ is the gate threshold voltage; $\lambda$ is the coefficient of short-channel effect; $K_p$ is the transconductance coefficient, which is modelled as a linear function of $V_{GS}$ with two parameters $K_{p1}$ and $K_{p2}$ in (4). In the $I_{DS}$ model, $K_{p1}$, $K_{p2}$, $V_{GS(th)}$, $R_{D1}$ and $\lambda$ are the parameters that need to be extracted according to datasheet. Furthermore, to consider the temperature characteristics, $K_{p1}$, $K_{p2}$, $V_{GS(th)}$ and $R_{D1}$ are modelled as linear or quadratic functions of temperature: $K_{p1}(T)$, $K_{p2}(T)$, $V_{GS(th)}(T)$ and $R_{D1}$(T), based on the curve fitting results. The detailed modelling approach will be described in Section III.

### B. Diode model

In Fig. 2, a voltage-controlled current source $I_D$ and a series resistor $R_{D2}$ are used to model the current behavior of the anti-parallel diode. The model can be described in the following equations:

$$I_D = I_S \left( \exp\left( \frac{qV_D}{kT} \right) - 1 \right) \tag{6}$$

$$V_D = V_{SD} - R_{D2} I_D \tag{7}$$

where $V_{SD}$ is the source-to-drain voltage; $V_D$ is the diode voltage applied to the voltage-controlled current source $I_D$; $I_S$ is the reverse saturation current; $q = 1.602 \times 10^{-19}$ C is the electronic charge; $k = 1.3806488 \times 10^{-23}$ J/K is the Boltzmann's constant; T is the Kelvin temperature.

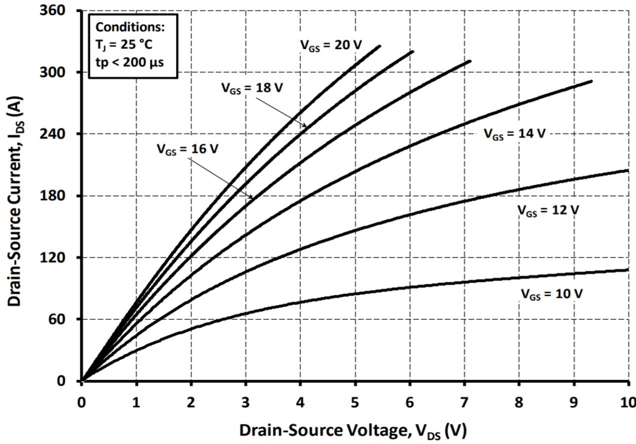
### C. Capacitance models

In Fig. 2, three capacitors, $C_{GS}$, $C_{GD}$ and $C_{DS}$, are used to model the parasitic capacitors of the SiC MOSFET. $C_{GS}$ is modelled as a constant capacitor. $C_{DS}$ and $C_{GD}$ are modelled as nonlinear capacitors as shown in (8) [3] and (9) [10].

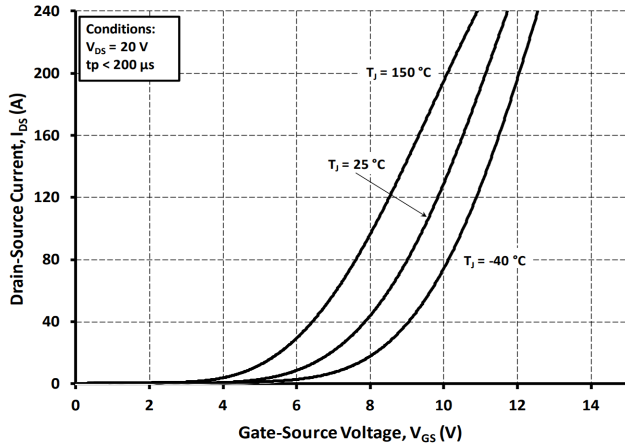
$$C_{DS} = C_{DS0} \left( \frac{V_{bi}}{V_{DS} + V_{bi}} \right)^{M_{CDS}} \tag{8}$$

$$C_{GD} = \frac{C_{GD0}}{\left(1 + V_{DG}\left(1 + k_1 \frac{1 + \tanh(k_2(V_{DG} - V_T))}{2}\right)\right)^{M_{CGD}}} \tag{9}$$

where $V_{DG}$ is the drain-to-gate voltage; $C_{DS0}$, $V_{bi}$, $M_{CDS}$ are the parameters for $C_{DS}$; $C_{GD0}$,$M_{CGD}$, $k_1$, $k_2$ and $V_T$ are the parameters for $C_{GD}$.




(a) $I_{DS}$–$V_{DS}$ output characteristics at 25 °C.




(b) $I_{DS}$–$V_{GS}$ transfer characteristics.

Figure 3. $I_{DS}$ characteristics of CAS120M12BM2 in the datasheet.

## III. Step-by-step modelling approach

### A. Modelling approach of $I_{DS}$ at 25 °C

Firstly, the modelling approach of $I_{DS}$ at 25 °C is described. The same modelling approach can be used for $I_{DS}$ model at different temperatures. The parameters $K_{p1}$, $K_{p2}$, $V_{GS(th)}$, $R_{D1}$ and $\lambda$ need to be extracted based on the $I_{DS}$–$V_{GS}$ transfer characteristics and $I_{DS}$–$V_{DS}$ output characteristics at 25 °C from the datasheet as shown in Fig. 3. The software GetData Graph Digitizer is used to convert the graphs of $I_{DS}$ characteristics in the datasheet into digital data. MATLAB curve fitting toolbox is used to do the curve fitting to extract parameters.

*1) Coefficient of short-channel effect $\lambda$:* Due to the short-channel effect, the channel length modulation occurs in SiC MOSFETs, which makes the positive current slope in the saturation region [11]. The short channel effect can be observed in Fig. 3a in the saturation region when $V_{GS} = 10\,\text{V}$. In the saturation region, $V_{ch}$ is the dominant factor of $V_{DS}$ due to the high channel resistance when the channel is pinched off. The voltage drop on $R_{D1}$ can be ignored. It can be assumed that $V_{ch} \approx V_{DS}$. Therefore, $V_{ch}$ in (3) can be replaced with $V_{DS}$. (3) can be simplified as:

$$I_{DS} = A(1 + \lambda V_{DS}) \tag{10}$$

where $A = K_p \frac{\left(V_{GS}-V_{GS(th)}\right)^2}{2}$ is a constant value when $V_{GS} = 10\,\text{V}$. $\lambda$ can be extracted by curve fitting to fit (10) to the saturation region of $I_{DS}$–$V_{DS}$ curve when $V_{GS} = 10\,\text{V}$ in Fig. 3a.

*2) Gate threshold voltage $V_{GS(th)}$:* The gate threshold voltage is defined as the gate-to-source voltage when the MOSFET starts to conduct a certain small amount of current. However, different MOSFETs and manufacturers might have different criteria of this current magnitude from $1\,\text{mA}$ up to $50\,\text{mA}$. Therefore, it is better to extract the $V_{GS(th)}$ for the model although it is already provided in the datasheet [3]. In the datasheet, the transfer characteristics, i.e. the $I_{DS}$–$V_{GS}$ curve, are usually measured with a high drain-to-source voltage bias so that $I_{DS}$ is saturated. For example, in the datasheet of CAS120M12BM2, $V_{DS} = 20\,\text{V}$ is used to measure the transfer characteristics as shown in Fig. 3b. In the saturation region, $V_{ch} \approx V_{DS}$ can be assumed since $V_{ch}$ is the dominant factor of $V_{DS}$ . Therefore, $V_{ch}$ in (3) can be replaced with $V_{DS} = 20\,\text{V}$. (3) can be simplified as:

$$I_{DS} = B \frac{\left(V_{GS} - V_{GS(th)}\right)^2}{2} \tag{11}$$

where $B = K_p(1 + \lambda V_{DS})$ is a constant value when $V_{DS} = 20\,\text{V}$. $V_{GS(th)}$ can be extracted by curve fitting to fit (3) to the $I_{DS}$–$V_{GS}$ curve in Fig. 3b.

*3) Transconductance coefficient $K_p$:* Two sets of $I_{DS}$–$V_{DS}$ curves are required since the transconductance coefficient is modelled with two parameters $K_{p1}$ and $K_{p2}$ in (4). The $I_{DS}$–$V_{DS}$ curves when $V_{GS} = 10\,\text{V}$ and $12\,\text{V}$ are chosen due to the high channel resistance at low gate-to-source voltage. Therefore, the voltage drop on $R_{D1}$ can be ignored and $V_{ch} \approx V_{DS}$ can be assumed. In this case, $V_{ch}$ in (2) can be replaced with $V_{DS}$. (2) can be rewritten as:

$$I_{DS} = K_p \left(V_{GS} - V_{GS(th)} - \frac{V_{DS}}{2}\right) V_{DS} \left(1 + \lambda V_{DS}\right) \tag{12}$$

$K_p$ can be extracted by curve fitting to fit (12) to the linear region of $I_{DS}$–$V_{DS}$ curves when $V_{GS} = 10\,\text{V}$ and $12\,\text{V}$ in Fig. 3a respectively. Two different values of $K_p$ can be extracted with $V_{GS} = 10\,\text{V}$ and $12\,\text{V}$ respectively as shown in Table I. Afterwards, (4) can be used to fit Table I to extract $K_{p1}$ and $K_{p2}$.

Table I
Extracted $K_p$ with different $V_{GS}$.

| $V_{GS}$ | 10 V | 12 V |
|---|---|---|
| $K_p$ | 4.886 | 5.450 |

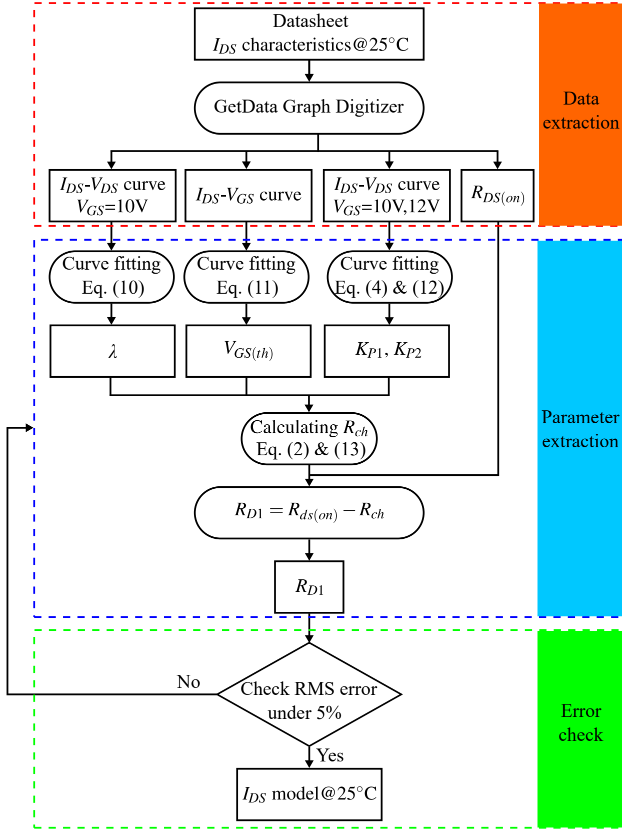



Figure 4. Modelling approach of $I_{DS}$ at 25 °C.

Table II
PARAMETERS OF $I_{DS}$ AT 25 °C.

| $K_{P1}$ | $K_{P2}$ | $V_{GS(th)}$ (V) | $R_{D1}$(mΩ) | $\lambda$ |
|---|---|---|---|---|
| 4.886 | 0.2818 | 3.992 | 6.001 | 0.043 |

*4) Series resistance $R_{D1}$:* In the model shown in Fig. 2, the on-state resistance $R_{DS(on)}$ consists of the channel resistance $R_{ch}$ of the current source $I_{DS}$ and the series resistance $R_{D1}$. $R_{DS(on)}$ is provided in the datasheet at specific conditions. For example, in the datasheet of CAS120M12BM2, $R_{DS(on)} = 13\,\text{m}\Omega$ when $V_{GS} = 20\,\text{V}$ and $I_{DS} = 120\,\text{A}$. The channel voltage $V_{ch}$ can be calculated under the same $V_{GS}$ and $I_{DS}$ condition according to (2). $R_{ch}$ and $R_{D1}$ can be then calculated as:

$$R_{ch} = \frac{V_{ch}}{I_{DS}} \tag{13}$$

$$R_{D1} = R_{DS(on)} - R_{ch} \tag{14}$$

*5) RMS error check:* After all the parameters are extracted, the accuracy of the model is checked by comparing the simulated $I_{DS} - V_{DS}$ characteristics with the characteristics in the datasheet. The root mean square (RMS) error is calculated using the following equation [2]:

$$RMS = \sqrt{\frac{\sum_{i=1}^{N} \mid m_i - s_i \mid^2}{N}} \times 100\% \tag{15}$$

where N, $m_i$ and $s_i$ denote the number of data, measured and simulated values of $I_{DS}$. If the calculated RMS error exceeds 5%, the parameter extraction procedure will be done again until the RMS error is lower than 5%.

The step-by-step modelling approach of $I_{DS}$ is summarized in Fig. 4. The extracted parameters are shown in Table II.

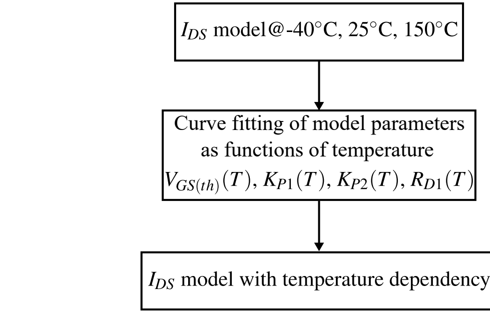



Figure 5. Modelling approach of $I_{DS}$ with temperature dependency.

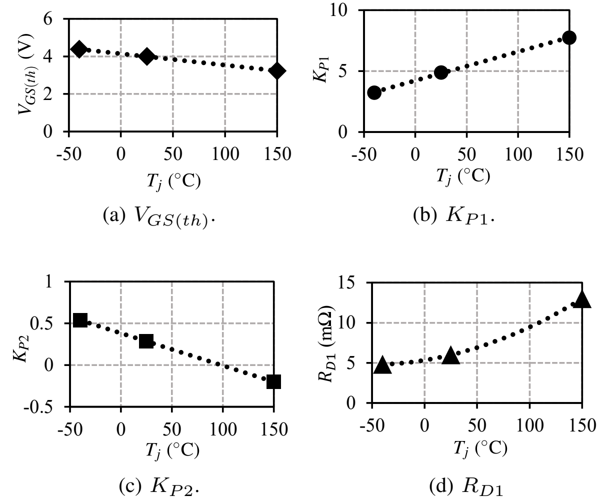
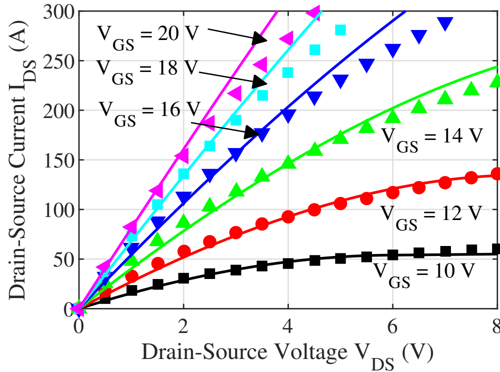


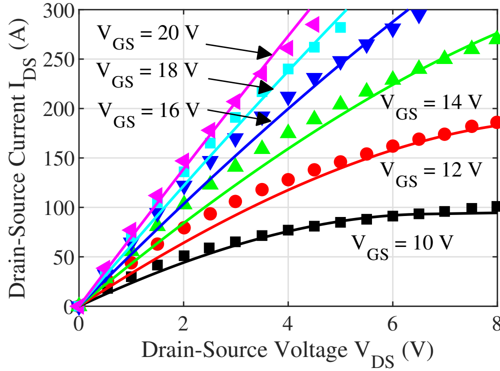

Figure 6. Temperature dependency of model parameters.

### *B. Modelling approach of $I_{DS}$ with temperature dependency*

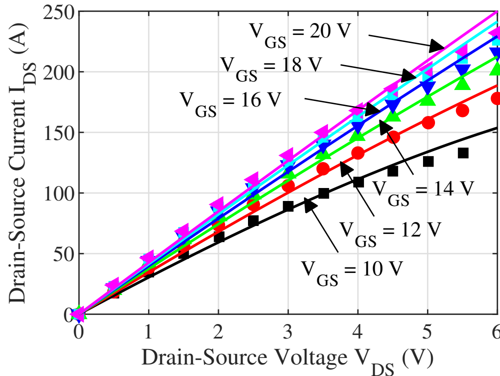
In the datasheet of CAS120M12BM2, the $I_{DS}$ characteristics at $-40\,°\text{C}$, $25\,°\text{C}$ and $150\,°\text{C}$ are provided, which can be used to model the temperature dependency. The parameters $K_{p1}$, $K_{p2}$, $V_{GS(th)}$ and $R_{D1}$ are modelled as linear or quadratic functions of temperature: $K_{p1}(T)$, $K_{p2}(T)$, $V_{GS(th)}(T)$ and $R_{D1}(T)$. Firstly, the parameters are extracted following the same approach in Fig. 4 at different temperatures. Secondly, the linear or quadratic functions are used to fit the values of each parameter at different temperatures. The modelling approach is summarized in Fig. 5. The temperature




(a) -40 °C.




(b) 25 °C.




(c) 150 °C.

Figure 7. $I_{DS}$–$V_{DS}$ characteristics at different temperatures comparing to datasheet.

dependency of the parameters are shown in Fig. 6. The equations to describe the temperature dependency are:

$$\begin{cases} V_{GS(th)} = -0.006T + 4.1416 \\ K_{P1} = 0.0237T + 4.2227 \\ K_{P2} = -0.0039T + 0.3816 \\ R_{D1} = 0.0002T^2 + 0.0214T + 5.3409 \end{cases} \tag{16}$$

The comparison between the $I_{DS}$ model with the datasheet is shown in Fig. 7. It can be seen that the simulated $I_{DS}$ characteristics match the datasheet very well, which can verify the effectiveness of the proposed modelling approach.

Table III
PARAMETERS OF DIODE MODEL.

| $I_S$ (A) | $R_{D2}(m\Omega)$ |
|---|---|
| 1.925e-14 | 4.66 |

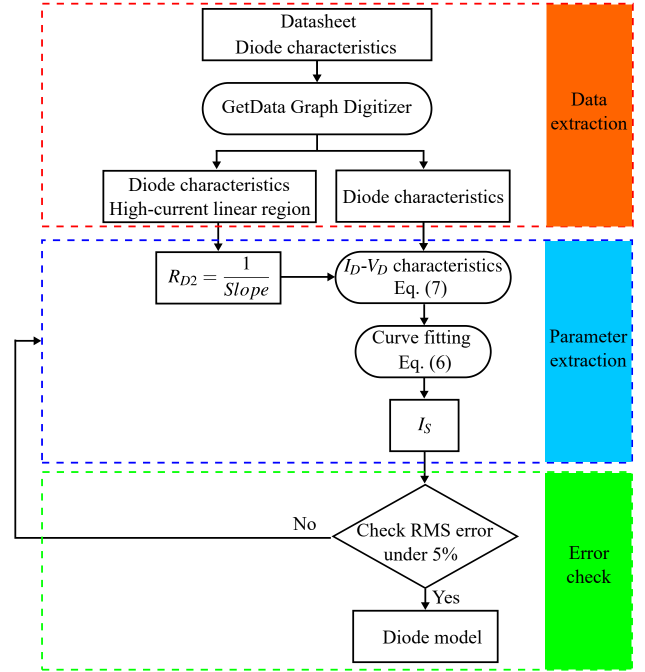



Figure 8. Modelling approach of diode.

### C. Modelling approach of diode

The diode model described in (6) and (7) contains two parameters that need to be extracted: $R_{D2}$ and $I_S$. The parameters are extracted according to diode characteristics in the datasheet.

*1) Series resistance $R_{D2}$:* According to (6), the differential resistance of the voltage-dependent current source $I_D$ can be calculated as:

$$R_D = \frac{\mathrm{d}V_D}{\mathrm{d}I_D} = \frac{kT}{q} \cdot \frac{1}{I_D + I_S} \tag{17}$$

According to (17), $R_D << R_{D2}$ can be assumed when $I_{DS}$ is larger than 100 A. Therefore, the slope of the diode characteristics in the high current linear region can be used to extract the series resistance $R_{D2}$.

*2) Reverse saturation current $I_S$:* After $R_{D2}$ is extracted, the $I_D$–$V_D$ characteristics can be obtained from the $I_D$–$V_{SD}$ diode characteristics according to (7). $I_S$ can be then extracted by fitting (6) to the $I_D$–$V_D$ characteristics.

The extracted parameters of the diode are listed in Table III. The step-by-step modelling approach is summarized in Fig. 8. In Fig. 9, the diode model matches the diode characteristics in the datasheet very well, which can verify the effectiveness of the proposed modelling approach.

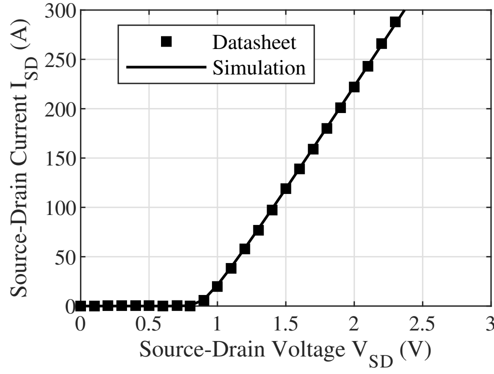



Figure 9. Diode characteristics comparing to datasheet.

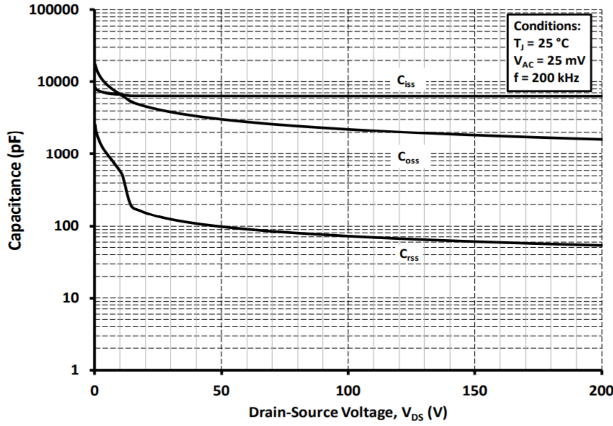



Figure 10. Capacitance characteristics of CAS120M12BM2 in the datasheet.

### D. Modelling approach of parasitic capacitors

In the datasheet, the input capacitance $C_{iss}$, output capacitance $C_{oss}$ and reverse transfer capacitance $C_{rss}$ are given as the capacitance characteristics as shown in Fig. 10. $C_{GS}$, $C_{GD}$ and $C_{DS}$ can be calculated by $C_{iss}$, $C_{oss}$ and $C_{rss}$ according to (18):

$$\begin{cases} C_{GS} = C_{iss} - C_{rss} \\ C_{DS} = C_{oss} - C_{rss} \\ C_{GD} = C_{rss} \end{cases} \tag{18}$$

*1) $C_{GS}$:* A constant value is used to model $C_{GS}$. It can be easily extracted by subtracting $C_{rss}$ from $C_{iss}$ according to (18). $C_{GS}$ = 6319 pF can be obtained for CAS120M12BM2.

*2) $C_{DS}$:* $C_{DS}$ is a nonlinear capacitor varying with drain-to-source voltage $V_{DS}$. The $C_{DS}$–$V_{DS}$ curve can be derived from the datasheet using (18). $C_{DS0}$, $V_{bi}$, $M_{CDS}$ can be easily extracted by curve fitting using (8) and the $C_{DS}$–$V_{DS}$ curve.

*3) $C_{GD}$:* $C_{DS}$ is a more complicated nonlinear capacitor varying with drain-to-gate voltage $V_{DG}$. The $C_{rss}$–$V_{DS}$ curve in the datasheet can be used to extract the parameters of $C_{GD}$. In Fig. 10, two significantly different slopes can be observed in the $C_{rss}$–$V_{DS}$ curve. $V_T$ can be firstly extracted as the transition voltage of these two slopes. In (9), a hyperbolic tangent function is used to model the transition of slopes in

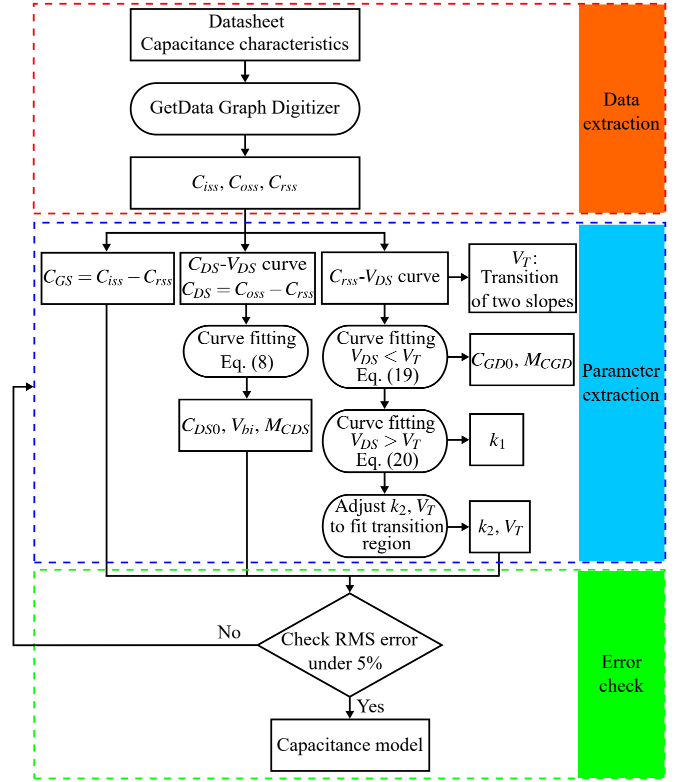



Figure 11. Modelling approach of parasitic capacitors.

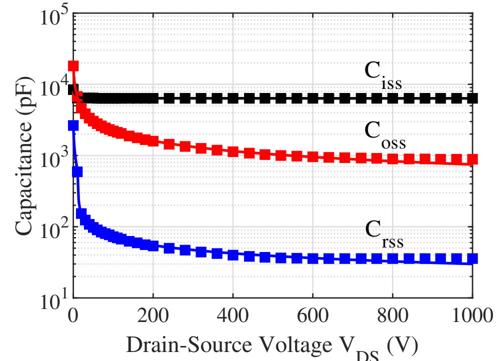



Figure 12. Capacitance characteristics comparing to datasheet.

$C_{rss}$–$V_{DS}$ curve . When $V_{DG} < V_T$, (9) can be approximated as:

$$C_{GD} = \frac{C_{GD0}}{(1 + V_{DG})^{M_{CGD}}} \tag{19}$$

$C_{GD0}$ and $M_{CGD}$ can be extracted by curve fitting to fit (19) to $C_{rss}$–$V_{DS}$ curve when $V_{DS} < V_T$.

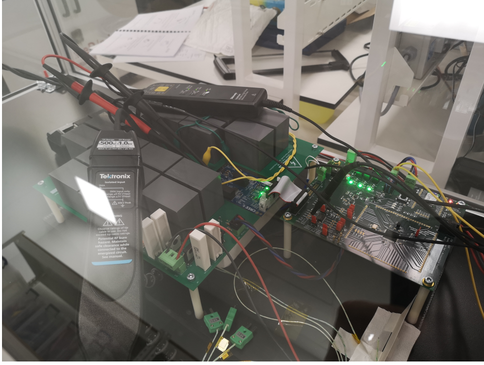
When $V_{DG} > V_T$, (9) can be approximated as

$$C_{GD} = \frac{C_{GD0}}{(1 + V_{DG}(1 + k_1))^{M_{CGD}}} \tag{20}$$

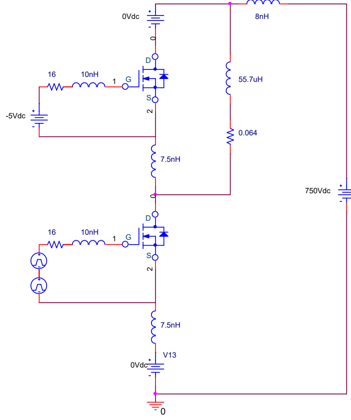
$k_1$ can be extracted by curve fitting to fit (20) to $C_{rss}$–$V_{DS}$ curve when $V_{DS} > V_T$.

Table IV
PARAMETERS OF CAPACITANCE MODEL.

| $C_{GS}$(pF) | $C_{DS0}$(pF) | $V_{bi}$ (V) | $M_{CDS}$ | $C_{GD0}$(pF) | $V_T$(V) | $k_1$ | $k_2$ | $M_{CGD}$ |
|---|---|---|---|---|---|---|---|---|
| 6319 | 15500 | 1.622 | 0.478 | 2646 | 13.52 | 40.51 | 0.3815 | 0.4295 |

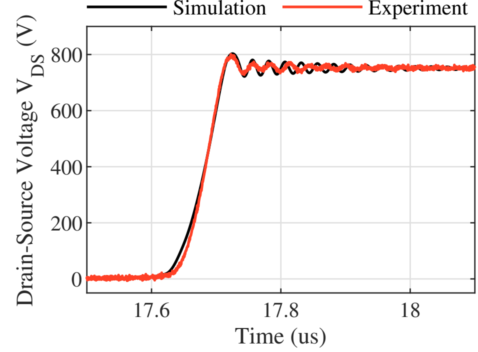


(a) Experimental platform.

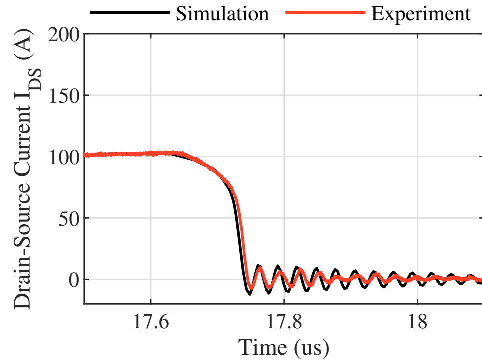



(b) Simulation circuit.

Figure 13. Experimental platform and simulation circuit of DPT.




(a) Turn-off voltage $V_{DS}$.




(b) Turn-off voltage $I_{DS}$.

Figure 14. Comparison of turn-off waveforms by simulation and experiment at 25 °C.

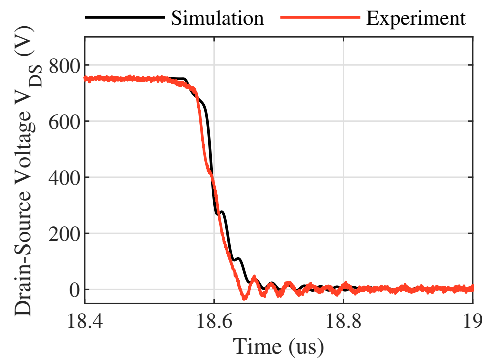
Finally, $k_2$ and $V_T$ are adjusted to accurately fit the transition region of two different slopes of the $C_{rss}$–$V_{DS}$ curve.

The step-by-step modelling approach of parasitic capacitors is summarized in Fig. 11. The extracted parameters are listed in Table IV. The comparison between the capacitance model and the datasheet is shown in Fig. 12, which shows a good agreement.

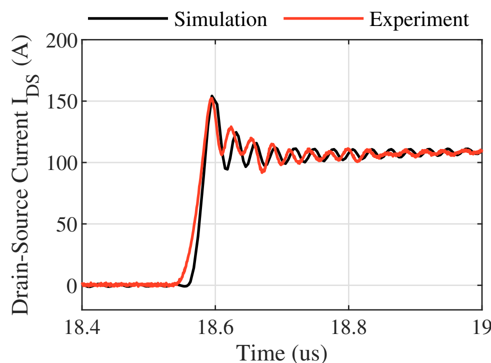
## IV. MODEL VERIFICATION

A SPICE model is built for CAS120M12BM2B using the subcircuit model and extracted parameters. Both experimental platform and simulation platform of double pulse tester (DPT) are built to verify the proposed SPICE model. The experimental platform of DPT is shown in Fig. 13a. A PCB board with low parasitic inductance is designed as the main circuit. A commercial gate driver CGD15HB62P1 for half-bridge module from Wolfspeed is used [12]. The upper switch is always off and the lower switch is controlled by the DPT signal generated by the DSP control board. A $55.7\,\mu$H with low equivalent parallel capacitance is designed as the load inductor. The equivalent series resistance of the load inductor is measured as $0.064\,\Omega$. The voltage and current of the lower switch is measured by high-bandwidth differential voltage probes and high-bandwidth current probes.

The same simulation circuit of DPT is built in PSpice as shown in Fig. 13b. The 5 nH DC-bus stray inductance is obtained by simulating the S-parameter of the PCB board including all the stray inductance of the DC capacitors in Keysight Advanced Design System (ADS) [13]. The stray inductance in the power module is 15 nH according to the datasheet. Two 7.5 nH inductors are added to the drain terminals of upper and lower SiC MOSFETs in the half-bridge module respectively to represent this stray inductance. The gate loop resistance is obtained by calculating the time constant of the measured gate-to-source voltage. The DPT results in both simulation and experiment are shown in Fig. 14 and Fig. 15. The simulation of the turn-on and turn-off transients shows good agreement with the experiment.




(a) Turn-on voltage $V_{DS}$




(b) Turn-on voltage $I_{DS}$

Figure 15. Comparison of turn-on waveforms by simulation and experiment at 25 °C.

## V. Conclusions

In this paper, a step-by-step modelling approach for SiC MOSFET half-bridge power modules has been presented. The proposed modelling approach significantly reduces time and efforts of converter designers to develop their own models for switching-loss analysis and converter design. Subcircuits and equations of SiC modules were firstly introduced to model the drain-to-source current, antiparallel diode, parasitic capacitance and temperature dependency accurately. Then, a step-by-step parameter extraction approach based on datasheet was proposed, which can be easily used to model other SiC MOSFET half-bridge power modules. As an example, a SPICE model was built based on the proposed modelling approach for a commercial power module. A good agreement on switching on/off waveforms is achieved between simulation and experiment results, which verifies the accuracy of the proposed modelling approach.

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