ADVANCED CHARACTERISATION TECHNIQUES FOR ENVELOPE TRACKING POWER AMPLIFIERS

A thesis submitted to Cardiff University

in candidature for the degree of

Doctor of Philosophy by

Sattam Fahd Alsahali, M.Sc.

Centre for High Frequency Engineering

School of Engineering

Cardiff University

United Kingdom

February 2020

…. To my father Fahd,
May Allah forgive him
& have mercy on him ……

ABSTRACT

Envelope tracking (ET) is a strong contender architecture for enhancing the power efficiency performance of power amplifiers (PAs) in emerging communication systems. However, the design and characterisation of envelope tracking power amplifiers (ET-PAs) introduces a number of significant technical challenges related to the optimisation and interaction of the numerous subsystems involved, namely the PA itself, envelope detection/generation, the supply modulator and linearisation elements. This Ph.D. research extends the current state of the art in ET-PA measurement and characterisation and considers new measurement and characterisation capabilities that provide for the rapid development of ET-PA architectures.

The research starts by fully implementing a new ET-PA measurement system and includes the characterisation and validation of the requirements for such a system. Following this, the realised system is used to investigate the important area of interaction between an PA and a supply modulator in the presence of voltage ripple representative of an actual switching modulator. By varying the ripple magnitude as a proportion of the modulated drain voltage, the effects on the linearity of the PA are observed and analysed, providing the system designer with insight into the amount of ripple that is tolerable, and at what cost in terms of other key parameters. Additionally, potential countermeasures including digital pre-distortion (DPD) and shaping function optimisation are explored and the influence of the ripple magnitude on an ET-PA is quantified.

The second part of the thesis presents an integration of a modulated active load-pull system, allowing simultaneous broadband impedance environment emulation and DPD linearisation, in one integrated measurement system. This novel combination allows investigation of for example, how well a microwave power transistor, operating in an optimal RF impedance environment, responds to linearisation with DPD techniques. Following this demonstration, a fully emulated ET-PA environment is realised by adding a dynamic supply voltage capability, and excited using industry-standard modulated.

As a result, a measurement setup has been demonstrated that enables the PA designer to characterise device operation within fully emulated PA modes of operation, under realistic modulated signal conditions, as well as allowing, in real time, the rapid investigation into how well these modes respond simultaneously to ET and DPD techniques.

ACKNOWLEDGMENTS

In the name of Allah, the most merciful and most beneficent

First of all, I wish to express my sincere appreciation to my supervisor, Dr. Jonathan Lees for his dedicated supervision on my Ph.D. research work. I am truly grateful for his encouragement. I should also acknowledge my second supervisor, Prof. Paul Tasker, for his support. In addition, I would like to thank friends; Dr. Peng Chen and Alexander Alt.

I am thankful for the Engineering and Physical Science Research Council in the context of the research project EP/N016408/1 and Mesuro Limited to support this research. I would also like to thank the Royal Saudi Land Forces for financial support. This work would not have been possible without their support.

My time in Cardiff School of Engineering was more enjoyable with great friends that made the tougher times much more bearable, and the easier times thoroughly enjoyable. I would like to express my special thanks to Prof Adrian Porch and Dr. Roberto Quaglia. I wish to thank the Mesuro team including Dr. Dragan Gecan, Dr. Aamir Sheikh, and Dr. Simon Woodington. Also, I would like to thank the electrical workshop team and especially Denley Slade and Richard Rogers who were always there when I needed to fabricate a circuit.

Finally, I would like to express the biggest thank to my family. I am grateful to my parents Fahd Hazza, who passed away last year may Allah mercy him, and Norah Faraj for their endless love and encouragement since my childhood. My sincere pleasure to my wife Norah for her unlimited love and support during my Ph.D. journey. Moreover, I would like to express thankfulness for my lovely children; Fahd, Sultan, Munirah, and Nawaf for their smiles and laughter that always make my day.

List of Publications

First author:

1. **Alsahali, S**., Gecan, D., Alt, A., Chen, P., Woodington, S., Sheikh, A., Tasker, P. J. & Lees, J., "Modulated rapid load pull system for the emulation of envelope tracking power amplifiers," Electronics Letters, 2020. ***Note that this letter was chosen for the featured article in IET, Issue 7, March 2020.***

2. **Alsahali, S.**, Alt, A., Chen, P., Tasker, P. J. & Lees, J. (2019, October). Supply Modulator Ripple in Envelope Tracking Systems - Effects and Countermeasures. In 2019 49th European Microwave Conference (EuMC) (pp. 773-776). IEEE.

3. **Alsahali, S.**, Gecan, D., Alt, A., Wang,G., Anera ,S .,Chen, P.,Woodington,S., Sheikh, A., Tasker, P. J. & Lees, J. (2019, June). A Novel Modulated Rapid Load Pull System with Digital Pre-Distortion Capabilities. In 2019 93rd ARFTG Microwave Measurement Conference (ARFTG) (pp. 773-776). IEEE.

4. **Alsahali, S.**, Alt, A, Chen, P., & Lees, J. (2018, April). Effect of supply modulator voltage ripple on efficiency and linearity in Envelope Tracking Power Amplifiers. In 2018 Automated RF & Microwave Measurement Society (ARMMS).

Co-authored:

1. Chen, P., **Alsahali, S**., Alt, A., Wang, G., Casbon, M. A., Lees, J.,& Tasker, P. J., " A Flexible Bandwidth Reduction Technique for Envelope Tracking Using Low-Pass Finite Impulse Response Filters," Electronics Letters, 2020.

2. Chen, P., **Alsahali, S**., Alt, A., Lees, J., & Tasker, P. J. (2018, July). Behavioral Modeling of GaN Power Amplifiers Using Long Short-Term Memory Networks. In 2018 International Workshop on Integrated

Nonlinear Microwave and Millimeter-wave Circuits (INMMIC) (pp. 1-3). IEEE.

3. Alt, A., Chen, P., **Alsahali, S**., Quaglia, R., Tasker, P. J., & Lees, J. (2018, July). Comparing FET Technologies in Terms of Their Suitability for Broadband Envelope Tracking Power Amplifiers. In 2018 International Workshop on Integrated Nonlinear Microwave and Millimeter-wave Circuits (INMMIC) (pp. 1-3). IEEE.

4. Alt, A., Quaglia, R., Chen, P**., Alsahali, S**., Tasker, P. J., & Lees, J. (2018, June). Class B*-A New High-Efficiency RF DC/DC Converter Concept Using Second Harmonic Generation/Injection. In 2018 IEEE Wireless Power Transfer Conference (WPTC) (pp. 1-4). IEEE.

5. Alt, A., Quaglia, R., Chen, P., **Alsahali, S**., Tasker, P. J., & Lees, J. (2018, September). Analysis of Highly Efficient Self-Synchronous Class-F Microwave Rectifiers Using Waveform Engineering. In 2018 48th European Microwave Conference (EuMC) (pp. 773-776). IEEE.

6. Alt, A., Chen, P., **Alsahali, S.**, Wang, G., Quaglia, R., Tasker, P. J., & Lees, J. (2019, October). Impact of the Input Impedance on the Linearity of Supply Modulated GaN HEMT Power Amplifiers. In 2019 49th European Microwave Conference (EuMC) (pp. 706-709). IEEE.

7. Anera, S. M. S., Husseini, T., **Alsahali, S.**, Bell, J. J., Quaglia, R., Kermalli, M., Tasker, P.J. and Benedikt, J. (2019, September). High-Efficiency Broadband PA Design Based on Continuous Class-F Mode with Compression. 2019 IEEE MTT-S International Microwave Symposium (IMS). IEEE.

LIST OF ACRONYMS

IPTV	- Internet Protocol television
IOT	- Internet of Things
WCDMA	- Wideband Code Division Multiple Access
HSPA	- High-Speed Packet Access
LTE	- Long-Term Evolution
4G	- Fourth generation mobile communications system
5G	- Fifth generation mobile communications system
PAPR	- Peak-to-Average Power Ratio
PA	- Power Amplifier
UE	- User Equipment
BTS	- Base Station
OPEX	- Operation Expenditure
ET-PA	- Envelope Tracking Power Amplifier
EPSRC	- Engineering and Physical Sciences Research Council
MMIC	- Monolithic Microwave Integrated Circuit
RF	-Radio Frequency
GaN	- Gallium Nitride
EER	- Envelope Elimination and Restoration
DPD	- Digital Pre-Distortion
ET	- Envelope Tracking
CW	- Continuous Wave
NI	- National Instruments
HT	- Harmonically Tuned
GaAs	- Gallium Arsenide
DC	- Direct Current
SMPA	- Switch-Mode PA
OBO	- Output Power Back Off
DPS	- Dynamic Power Supply

MOS	- Metal–Oxide–Silicon
DLM	- Dynamic Load Modulation
LMBA	- Load Modulated Balanced Amplifier
DPA	- Doherty PA
PAE	- Power Added Efficiency
LINC	- Linear Amplification with Nonlinear Components
ML-LNIC	- Multilevel LINC
AMO	- Asymmetric Multilevel Outphasing
MMMB	- Multimode Multiband
AET	- Auxiliary Envelope Tracking
AC	- Alternating Current
NVNA	- Nonlinear Vector Network Analyser
DUT	- Device Under Test
RLP	- Rapid Load-pull
FPGA	- Field-Programmable Gate Array
LO	- Local Oscillator
AWG	- Arbitrary Waveform Generator
LUT	- Look Up Table
EVM	- Error Vector Magnitude
ACPR	- Adjacent Channel Power Ratio
IMD	- Intermodulation Distortion
DE	- Drain Efficiency
Q	- Quadrature
VST	- Vector Signal Transfer
VSA	- Vector Signal Analyser
VSG	- Vector Signal Generator
Op-Amp	- Operational Amplifier
FET	- Field-Effect Transistor
OMN	- Output Matching Network
IMN	- Input Matching Network

SMU	- Source Measure Unit
RMS	- Root Mean Square
GMP	- Generalised Memory Polynomial
MP	- Memory Polynomial
PEP	- Peak Envelope Power
ADC	- Analog-to-Digital Converter
DAC	- Digital to Analogue Converter
ADS	- Advanced Design System

Table of Contents

List of Figures

List of Tables

CHAPTER 1

Introduction

1.1 Research Motivation

Recent years have witnessed a dramatic growth in the number of mobile subscriptions, which is expected to reach 8.9 billion by 2025, with 2.6 billion of those being for 5G, as shown in Figure 1.1[1]. A massive amount of data is driven via mobile communication networks and includes mobile internet and multimedia services, such as web browsing, music downloads, movie streaming, videos, social networking, video games, cloud services and internet of things (IoT), which together, will require enormous data rates to be supported by communications systems.

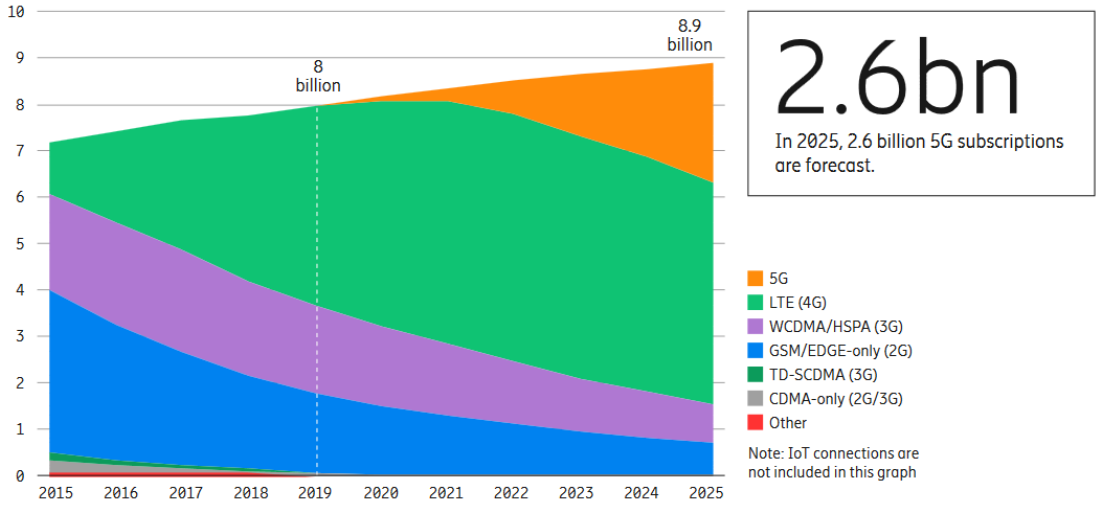

Figure 1.1 Universal mobile subscriptions by communication technology (in billions) [1]

Consequently, more complex modulated signals, such as wideband code division multiple access (WCDMA), high-speed packet access (HSPA) , long-term evolution (LTE) and LTE advanced have all been employed in the current, and likely the forthcoming, generations of mobile systems, such as 5G and beyond, to satisfy this massive growth and enhance spectral efficiency. While these modulation schemes offer high data throughput and high spectral efficiency, the time-domain envelope of their output signals is not constant, with high (typically up to 10 dB) associated peak-to-average power ratio (PAPR). Traditionally, the PA needs to operate in an output back-off (OBO) condition, as the PAPR increases, in order to meet linearity requirements, which leads to a severe degradation in the efficiency of the PA. This efficiency degradation, in turn, leads to an increase in the amount of dissipated power in user equipment (UE) since the PA dominates the power consumption. Moreover, the base transceiver station (BTS) will suffer from a similar issue of power dissipation, and these concerns have a vital impact on the mobile communication industry. Generally, when the efficiency of the PA decreases, and in a handset, this means the battery life will drop dramatically. The temperature of the device will also rise, which will, in turn cause issues with reliability. In addition, using efficient PAs across a network will result in a reduction in CO_2 emissions and will save on the raw materials used to produce this energy [2]. Furthermore, the operation expenditure (OPEX), which is the cost of the consumption power to operate both the UEs and BTSs, plus the cost of the cooling system and heat sinks inside the BTSs, will largely depend on how efficient the PA is.

The main challenge of PA design is to achieve high efficiency and maintain linearity over the entire range of operational power levels and bandwidth. Consequently, significant research into PA design continues within academia and industry, which has resulted in several enhanced approaches for maintaining efficiency over OBO; for instance envelope elimination and restoration (EER)[3], the Doherty PA [4], and envelope tracking (ET) [5], [6].

ET is one of the most promising solutions to achieve high efficiency and maintain linearity over a wide range of power levels and high bandwidth. It works by rapidly changing the supply voltage of the PA in response to the input signal, providing a low supply voltage for low output powers and a high supply voltage for high powers, ideally maintaining the PA in an efficient state at all times. As transition between transmitted power levels happens rapidly in modern communication systems, realising ET introduces substantial technical challenges, not only in terms of design but also in terms of measurement and characterisation. One difficulty is that an ET system comprises several subsystems; the ET-PA itself, envelope detection and baseband generation, the supply modulator and linearisation system elements. These interfaces introduce new challenges however, for example, it is difficult to characterise a transistor's performance within an emulated PA environment, i.e. without having to build a full ET-PA system, as would typically be done in a conventional PA design. As understanding the different subsystems requires different expertise, the work described in this thesis has contributed to In GaNET, an

Engineering and Physical Science Research Council (EPSRC) research project which tackles ET system design from different angles; aiming to integrate GaN RF circuits with high-speed GaN switching architectures on common silicon substrates. The project consortium brings together expertise of five UK Universities; Cambridge, Sheffield, Glasgow, Manchester and Cardiff. The focus of each group is shown in Table 1-1, and this thesis will deal with ET-PA characterisation part. Therefore, this thesis aims to develop measurement capabilities to characterise the integration and interaction between PA and an efficient DC/DC converter, in a monolithic microwave integrated circuit (MMIC) structure.

Table 1-1 EPSRC project groups' tasks

Group	Task
Cambridge	GaN on Si Epitaxy
Sheffield	GaN Device Fabrication
Glasgow	GaN MMIC Fabrication Passives – inductors, waveguides
Manchester	Dynamic Power Convertor Design
Cardiff	Device Characterization RF PA & Design System Integration & Characterization

1.2 Research Objectives

The research focuses on four main areas around ET measurement and characterisation. The first is to build an ET characterisation system to fully demonstrate and prove the ability of the Cardiff University group to conduct ET-PA measurements, for this thesis and in support of the EPSRC project.

The second research challenge was to investigate the interaction between PA and the supply modulator, to provide research findings to the other partners in the EPSRC project, enabling them to optimise their designs.

The third research challenge was to combine a modulated load pull system with digital pre-distortion (DPD) in one integrated measurement system. Such a measurement setup should enable the PA designer to characterise devices within emulated PA modes and architectures, under realistic modulated signal conditions, and investigate how well they respond to linearisation with DPD techniques.

Finally, a further potential objective of the Ph.D. work was to develop a high-speed modulated measurement system to fully emulate power amplifier envelope tracking (ET-PA) in conjunction with the DPD linearisation technique. Such a system will help to fully characterise PAs and investigate how well they respond to ET and DPD techniques.

1.3 Thesis Organisation

This thesis is divided into seven chapters which are summarised as follows:

Chapter 2: This chapter reviews different power amplifier architectures and various characterisation techniques documented in the current literature. It starts by reviewing different PA classes, which provide high efficiency close to saturation or at peak envelope power, and then moves on to consider PA architectures that can achieve high efficiency at OBO. Then, the chapter reviews different measurement

techniques which are used to measure and characterise PAs under either *c*ontinuous wave (CW) or modulated excitation, with associated advantages, disadvantages, and limitations. The chapter concludes by presenting an ET measurement system which includes a comparison of two commercial ET measurement systems.

Chapter 3: The work in this chapter discusses the essential requirements for an ET measurement system. Then, it describes the (National Instruments) NI PXI system which is used to carry out ET measurements and illustrates the design of the hardware that is used to test and demonstrate the capabilities of the ET measurement system. After this, an experimental validation for the ET characterisation system using 10 MHz LTE is demonstrated for the first time in the Centre for High Frequency Engineering (CHFE) at Cardiff University.

Chapter 4: This chapter presents an experimental investigation into the interaction between a PA and a supply modulator in the presence of voltage ripple. The effects on the linearity of the PA can be observed and analysed by adding a varying ripple magnitude to the modulated drain voltage. This allows the ET-PA designer to gain insight into the amount of ripple that is tolerable. Additionally, the ripple sensitivity of two different ET-PA linearisation techniques are investigated; firstly, applying a generalised memory polynomial digital pre-distortion (DPD), and secondly, optimising the shape of the tracking signal, which will improve linearity.

Chapter 5: This chapter investigates the concurrent operation of a commercially available, modulated impedance synthesis and measurement system with digital

pre-distortion (DPD). The measurement setup enables the PA designer to characterise devices within emulated PA modes and architectures, under realistic modulated signal conditions and to investigate how well they respond to linearisation using the DPD technique.

Chapter 6: The work described in this chapter presents a novel characterisation system that can fully emulate a complete ET environment, with modulated impedance synthesis and dynamic supply voltage generation while using industry-standard modulated signals and DPD. The characterisation system is utilised to characterise a 10 W GaN HEMT device and provide impedance control over the signal and distortion bandwidths. Such a system can be considered a useful tool in ET-PA design space, to completely investigate the performance of the device in a realistic ET environment.

Chapter 7: This chapter concludes the thesis by outlining research contributions to the advancement of the ET-PA measurement system. This chapter also discusses potential areas of improvement to the ET-PA measurement system that can be investigated in the future.

1.4 References

[1] "Ericsson Mobility Report June 2019." https://www.ericsson.com/en/mobility-report/reports/june-2019/mobile-subscriptions-outlook (accessed 2019).

[2] M. Liu, L. Liu, X. Wu, L. Teng, J. Cao and S. Qin, "A Research on the Telecommunication Base Station Power Consumption Investment Analysis and Optimized Configuration Method for Hybrid Energy Power," Intelec 2013; 35th International Telecommunications Energy Conference, SMART POWER AND EFFICIENCY, Hamburg, Germany, 2013, pp. 1-6.

[3] F. Wang et al., "An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 12, pp. 4086-4099, Dec. 2006.

[4] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho and B. Kim, "The Doherty Power Amplifier: Review of Recent Solutions and Trends," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 2, pp. 559-571, Feb. 2015.

[5] P. Asbeck and Z. Popovic, "ET Comes of Age: Envelope Tracking for Higher-Efficiency Power Amplifiers," in IEEE Microwave Magazine, vol. 17, no. 3, pp. 16-25, March 2016.

[6] Z. Wang, "Demystifying Envelope Tracking: Use for High-Efficiency Power Amplifiers for 4G and Beyond," in IEEE Microwave Magazine, vol. 16, no. 3, pp. 106-129, April 2015.

Chapter 2

Literature Review

2.1 Introduction & Motivation

This chapter delivers a brief overview of different power amplifier (PA) architectures and characterisation techniques, from current research literature. The chapter starts by reviewing different classes of PA, that can provide high efficiency close to saturation or at peak envelope power, and then moves to consider architectures that achieve high efficiency over wide dynamic range, i.e. at OBO. A state-of-the-art example of such an architecture, envelope tracking (ET) is reviewed extensively. The second part of this chapter reviews the measurement techniques that are used to measure and characterise PAs under either CW or modulated excitation, with associated advantages, disadvantages, and limitations. The ET measurement system that forms the focus of this thesis is presented, and two commercial ET measurement systems are compared. Finally, the chapter concludes with a robust case illustrating the need to develop a measurement system that can fully emulate envelope tracking power amplifier (ET-PA).

2.2 Power Amplifiers Classes

Fundamentally, the main objective of a PA is to increase the amplitude or power of an input signal suitable for transmission or onward travel. There are several forms

of PA that can be used in different applications, and these are classified, based on their circuit topology and their operation, into three major groups; fundamental mode, switching mode and harmonically tuned (HT).

2.2.1 Fundamental PA Modes

The transistor in this grouping of amplifiers acts as either a voltage controlled current source or a current controlled current source. The PAs of this group, which are classed as A, B, AB and C modes, have similar basic construction but are different in terms of their conduction angle (α), where the conduction angle describes the portion of the output waveform causing conduction.

The Class-A mode requires the simplest circuit topology in this group of amplifiers. In an ideal device, the quiescent point of this mode is chosen to be half of the maximum current I_{max} (saturation current). Therefore, for a conduction angle of 360° , the whole current waveform is conducted (α = 1), whilst a maximum voltage swing between the knee voltage the safe maximum voltage is typically established, which means that the transistor will be active all the time. This translates to relatively high average DC current and results in poor efficiency (ideally 50 %) but with good linearity [1].

In the class-B mode, theoretically, the quiescent point is set at the device pinch-off, which, when excited by a sinewave, causes a half-rectified output current waveform with a conduction angle of $180^{\circ}(\alpha = 0.5)$, and a reduced average DC

current, with less overlap between the voltage and current waveforms. This leads to improved ideal efficiency when compared to class A of $\pi/4$ or 78.5 % on a tuned load with 6 dB of gain reduction [1].

Class-AB achieves a good balance between the efficiency of class-B and linearity of class-A, as well as having the attractive property of delivering more fundamental output current and hence power, than both class-A and class-B. Hence, the biasing point in class-AB is set between the half maximum current and pinch-off. The conduction angle in class-AB is less than 360° and greater than 180° ($0 < \alpha < 0.5$). This mode is suitable for applications requiring either high efficiency (50 % and 78.5 %) or good linearity, determined by the choice of bias point [1].

In Class-C, less than half period is conducted ($0.5 < \alpha < 0$) because the bias point is located below the pinch-off voltage. Reducing the conduction angle in this way theoretically increases the efficiency of this mode to 100 % [2], [3]. However, as the conduction angle decreases beyond that of class-B, so too does the fundamental output current, power and hence gain. The practical trade off between efficiency, linearity and gain of this PA mode means that a conduction angle of 150° is typical, which will yield an efficiency of 85 % with a moderate reduction in gain and output power [3].

2.2.2 Switch-Mode PAs

In the switch-mode PA (SMPA), the transistor acts as a switch, where the

output current is continually switched between two states ; either ON or OFF. These PAs can theoretically produce 100 % efficiency but with significant nonlinear features [1]. This group includes class-D and class-E mode.

The conventional circuit of class-D mode comprises two transistors, which act to continually switch ON and OFF via the input drive input signal. Thus, theoretically, there is no overlap between the current and square voltage waveforms, which results in zero power dissipation. Theoretically, the efficiency of class-D could be 100 % if the switch were sufficiently fast. However, the efficiency of this class is degraded through the loss of switching speed and parasitic capacitance associated with real devices [3].

The efficiency degradation in class-D mode is resolved by using a transistor with a shunt capacitor, as used in class-E mode and proposed in 1975 by Sokal [4]. The basic schematic of the class-E mode consists of one switch, which conducts for 180° of the waveform, and a shunt capacitor which discharges for the other half of the waveform to provide the required output.

2.2.3 Harmonic Tuned PAs

The third group of PAs is known as harmonically tuned (HT) PAs. The PAs in this group are operated as current sources. The efficiency in this category increases but usually at the cost of linearity [5]. The output waveform of the current and voltage are reshaped via harmonic terminations to obtain higher efficiencies. These classes are described below, focussing on class-F and class-J modes.

The Class-F amplifier employs drain voltage and current waveform shaping to achieve high efficiency. The output matching network is designed to present low (short) impedances to even-order harmonics and high (open) impedances to odd-order harmonics to assemble the required odd-order dominated square-wave drain voltage waveform, while the even harmonics dominate the half-wave rectified drain current waveform [6], [7]. The efficiency can theoretically reach 100 % by presenting an infinite number of harmonic components, which produces a perfect square voltage waveform and no overlap with the ideal half-rectified current waveform. However, the perfect square voltage waveform cannot be reached due to the frequency limitations of the device and the matching network. It is interesting to note however that limiting to a fifth harmonic component results in a theoretical efficiency to

94.8 % [1].

The Class-J and class-BJ PA modes proposed by S. C. Cripps [8] provide the same efficiency and linearity as Class-B, but offers the potential to do so over a wide range of frequencies. This is achieved by presenting an inductive/capacitive impedance termination to the fundamental and second harmonic current components respectively, producing a half wave rectified current waveform with a 'peaky' sinusoidal voltage waveform containing a significant second harmonic component and a 90° phase shift between the two waveforms. The possibility of presenting different pairs of fundamental and harmonics impedances while the output power and efficiency are maintained constant makes this class of PA

appropriate for broadband applications [8] and led directly to the general concept of continuous mode PAs that are now widely explored by many research groups worldwide [9],[10]. The various PA classes based on their conduction angle and efficiency are summarized in Table 2-1.

Table 2-1 Summary of PAs Mode Performance

Mode	Class	Conduction Angle α	Maximum Theoretical Efficiency
Linear -Mode PAs	A	2π	50 %
	B	π	78.5 %
	AB	$\pi - 2\pi$	50~78.5 %
	C	$0 - \pi$	78.5~100 %
Switch-Mode PAs	D	π	100 %
	E	π	100 %
Harmonic Tuned PAs	F	π	100 %
	J	Π	78.5 %

As discussed previously, conventional PAs produce poor efficiency when they amplify signals with high PAPR, so generally, are practically limited to signals with constant envelope, such as GMSK modulation signals [3]. However, their efficiency performance degrades as the PAPR rises with complex modulation schemes. This is because of the usual proportional relationship between the efficiency and the drive level. Linear or switched mode PAs, however, can be adapted to increase their efficiency when operating over dynamic range OBO, by using other techniques, such as load modulation and dynamic power supply (DPS). These are discussed briefly in the following section.

2.3 Architectures of Power amplifier

Several enhancement techniques have been proposed to optimise the output and the efficiency at OBO by means of dynamically changing either the load impedance or the supply voltage [11].

2.3.1 Dynamic Load Modulation

Load modulation is one of the promising techniques that has attracted the attention of RF designers and researchers to enhance PA efficiency in OBO. The output power level in this approach changes by varying the load impedance presented to the output of the PA in order to achieve high efficiency [12]. With the load modulation approach, the complexity of modulating the supply is not needed, which gives this approach an advantage of simplicity over the envelope elimination and restoration (EER) or envelope tracking (ET) techniques. In so called supply modulation techniques, the supply modulator can be realised using a linear amplifier, which has power dissipation and efficiency issues, or using much more efficient DC-DC converters, which have two significant weaknesses; difficulty in achieving the required baseband bandwidth and inherent switching noise or ripple voltage [13].

In the literature, various approaches for the load modulation topology have been proposed over the years, such as the passive load modulation technique, which was introduced as a cost-effective solution using MEMS devices, and as a solution for the varactor-based dynamic load modulation (DLM), which suffers from linearity

issues[14] . Another load modulation approach that has recently appeared is the load modulated balanced amplifier (LMBA) where the impedance seen by two 'large' PAs is modulated by changing the amplitude and phase of a 'control' signal, generated by a smaller PA, which leads to better control of the dynamic characteristics of the PA over a wide range of amplitudes and frequencies [15] . The outphasing [14], Doherty PA (DPA) [17] and varactor-based dynamic load modulation [18], [19] are all different approaches that exploit the load modulation technique. However, the most popular architecture for achieving PA efficiency enhancement over a wide dynamic range is by far the DPA.

2.3.1.1 The Doherty PA

The relatively simple and elegant concept of achieving efficiency enhancement over a wide dynamic range, using two interacting devices was initially introduced by William H. Doherty in 1936 to improve the efficiency of vacuum tube transmitters initially for very high power broadcasting applications [17]. The PA efficiency is increased in the OBO region via two or more amplifiers using load modulation. The classical structure of a DPA comprises two amplifiers that work as a current source, as depicted in Figure 2.1. The carrier amplifier is typically biased in Class AB, while the peaking amplifier typically biased in Class C. The carrier amplifier is connected to the output load via an impedance inverter (usually a quarter-wave transmission line), while the peaking amplifier is directly coupled to the load. The main amplifier is active at all powers of operation and realises high-efficiency performance at a reduced drive

power through the choice of a relatively high load impedance $(2Z_{Opt})$, while the peaking amplifier remains off because of its bias point of class C. When the output power level increases and the main amplifier starts to compress, the peaking amplifier, by virtue of its bias point, begins to turn on. Classically, this is set to be at one half of the maximum input voltage $({}^{v_{in,max}}/_{2})$. The correct phasing and combination of these signals via the impedance inverter leads to a realisation of high efficiency over a range of 6 dB OBO from the maximum input power by combining the output of the two amplifiers [20].

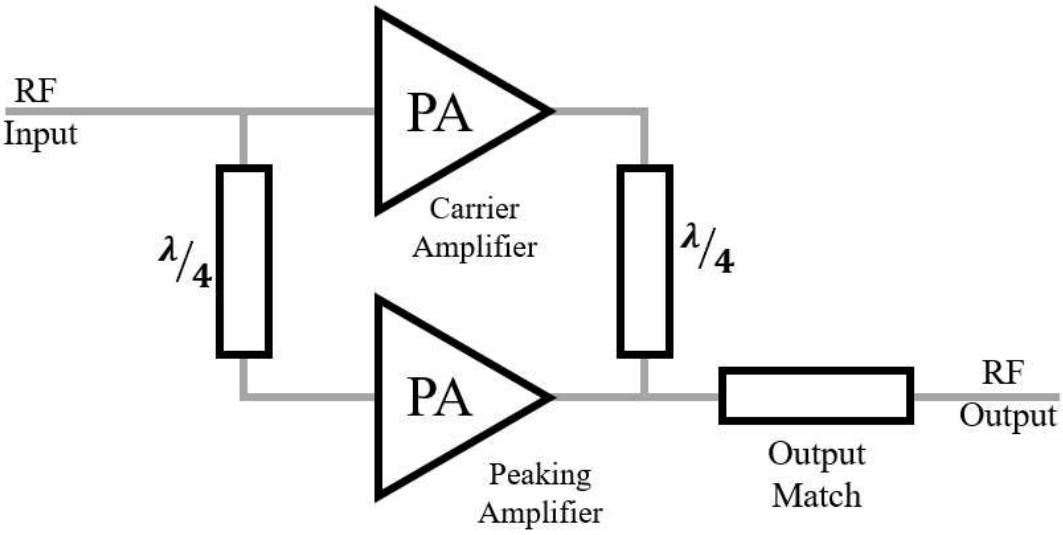

Figure 2.1 Simple diagram of DPA with impedance transformer

Although the main drawback of the DPA is its bandwidth limitation due to the quarter-wave transmission lines used, its performance can be enhanced by adopting several circuit techniques to extend the bandwidth of DPAs for broadband application [21], [22]. Moreover, there have also been significant efforts to improve the efficiency range up to 12 dB OBO using 3-way DPAs [21], [23] or 4-way DPAs to achieve an

efficiency output range of 18 dB OBO [17], [24]. In asymmetrical DPAs, peaking amplifiers that are much larger than the carrier amplifier are employed to achieve high efficiency over extend dynamic ranges up to 12 dB [25] as shown in Figure 2.2. The enhancement of efficiency in this technique is carried out completely using RF signals without the need to perform any special processing of the baseband signals. Such simple RF in – RF out structures are attractive in commercial base station applications [26] due to their simplicity of implementation. In terms of typical performance in a practical application, an average power added efficiency (PAE) of 39.5 % over 10 dB OBO has been achieved with symmetrical DPA in [27].

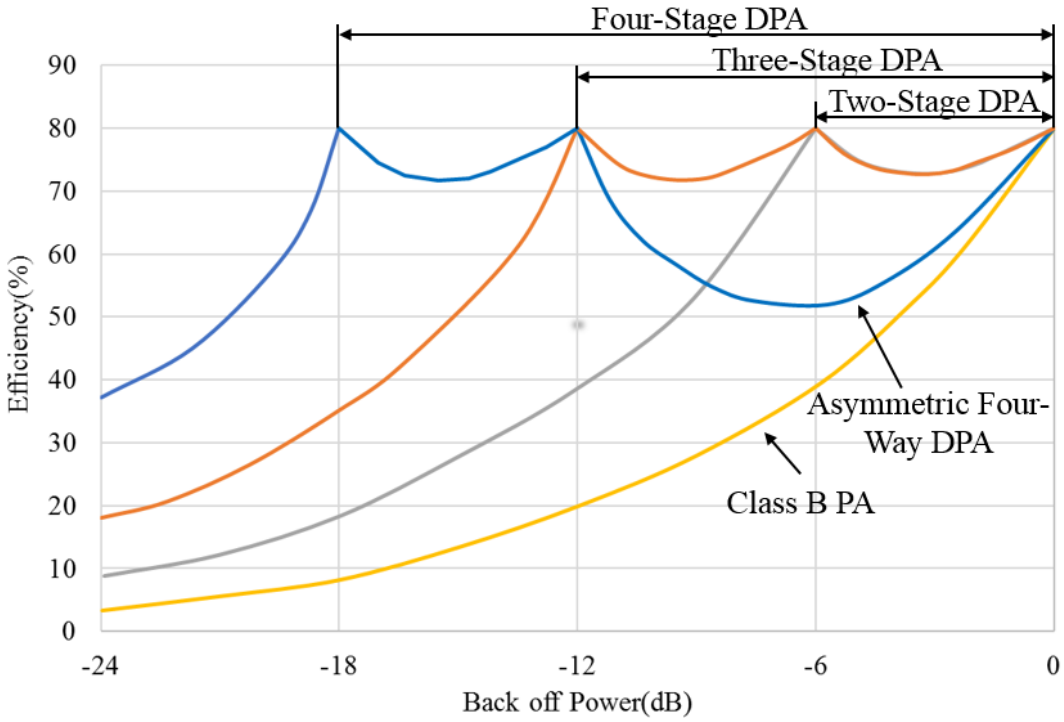

Figure 2.2 The efficiency of DPA for various configurations

2.3.1.2 The Outphasing PA

Outphasing was first presented by Chireix in 1935 as an enhancement technique for both efficiency and linearity for high power AM-broadcast transmitters [28]. Later on (in 1947) D.C. Cox [29] used the outphasing technique to produce linear modulation by combining the outputs of nonlinear amplifiers and called it Linear Amplification with Nonlinear Components (LINC). The basic mechanism of LINC approach, as depicted in Figure 2.3, is based on splitting the differential input signals into two paths with constant envelope phase-modulated signals.

$$S_1(t) = A_O(t)\cos\big(\omega t + \emptyset(t) + \varphi(t)\big)$$
$$S_2(t) = A_O(t)\cos\left(\omega t + \emptyset(t) - \varphi(t)\right) \quad (2.1)$$

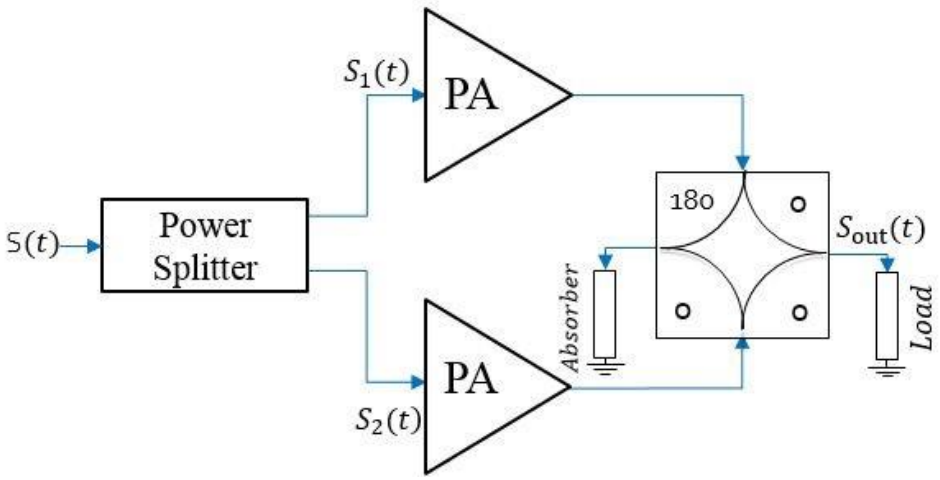

Figure 2.3 Traditional architecture of outphasing PA

Then, these two signals are amplified with two nonlinear PAs driven into compression. At the output stage, the two signals are combined via a passive power combiner where the in-phase signal components add together, and the out-of-phase

signal components cancel each other out. The resultant signal is the desired amplified replica of the original source signal $S(t)$. The maximum envelope will be achieved with the two signals in phase, while if the signals are antiphase, the envelope will be minimum [30]. Although both DPA and outphasing PAs require two PAs, the outphasing PA can use nonlinear PAs, while the DPA requires the two PAs to be relatively linear. However, the outphasing PA requires well-balanced paths with matching conditions between the two PAs to completely cancel the out-of-phase signals. In the literature, there are many variations of the outphasing technique including multilevel LINC (ML-LNIC) where different levels of supply voltage are supplied to the PAs to support the dynamic range [31]. However, this approach has a drawback of phase accuracy, which limits its performance. This issue is addressed using asymmetric multilevel outphasing (AMO), where the two PAs are supplied with two different voltage levels. Therefore, the requirement of the phase accuracy between the two signals will decrease according to the phase input signals [30]. The work presented in [32] shows how to extend the bandwidth of using outphasing with a broadband balun as a power combiner.

2.3.2 Dynamic Power Supply PAs

Several dynamic power supply (DPS) designs have been proposed to improve the efficiency of the power amplifier in the OBO region, such as envelope elimination and restoration (EER)[33], [34] , auxiliary envelope tracking (AET) [35] and envelope tracking (ET) [33], [36].

2.3.2.1 Envelope Elimination and Restoration

Envelope Elimination and Restoration (EER), or Khan Transmitter, is the first category of dynamic power supply in which the power amplifier is utilised to enhance the efficiency of the PAs under OBO and was first introduced in 1952 [37]. As illustrated in Figure 2.4, the input signal is divided into two paths, where the envelope extracted by the envelope detector to produce the amplitude modulation signal and the phase modulation signal which will be generated by the limiter by eliminating the envelope from the input signal. The former will be amplified efficiently by the envelope amplifier and a switched PA will amplify the latter. After that, the envelope of the phase modulation will be restored by the amplitude modulation signal, which will create an amplified copy of the original input signal [37], [38].

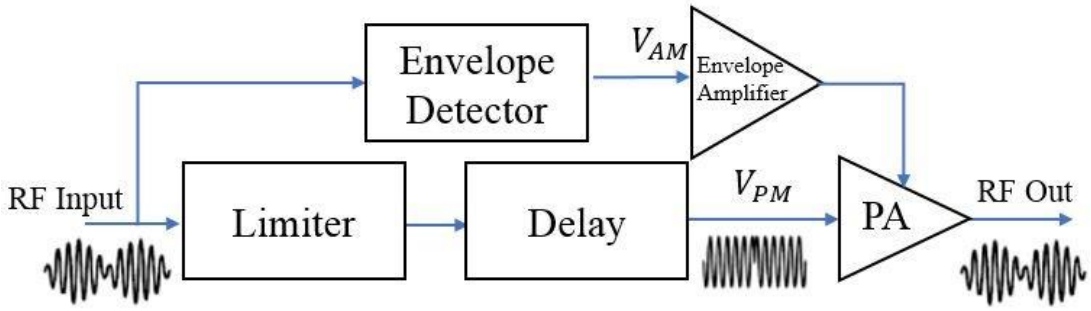

Figure 2.4 General block diagrams of the EER technique

Unfortunately, the bandwidth of the PA is limited by the low-frequency envelope modulator, which makes this technique appropriate for narrowband applications only [34], [39]. Nonetheless, the bandwidth of the EER might be improved

using special techniques, such as hybrid EER architecture where the PA will cover only the bandwidth of the modulation signal instead of the bandwidth of the phase-modulated signal. This can be achieved by using the modulated signal as the input signal instead of the phase-modulated signal [40]. For example, in [41] an efficiency of 44% was achieved using a multilevel converter with a linear regulator in series instead of using a linear regulator only. In a split band modulator, a class-S modulator and class-B linear amplifier are combined to extend the bandwidth to 5MHz with a 10% reduction in the average efficiency [42].

Another drawback of EER is its linearity, which is modest due to various sources involved, including the supply modulator and the misalignment between the envelope and the phase-modulated signals. However, many methodologies have been presented in the literature to enhance it, including envelope feedback and phase lock (polar loop), pre-distortion and Cartesian (I & Q) feedback [38].

2.3.2.2 Envelope Tracking

Envelope Tracking (ET) has been recognized for many years as potentially a key solution in PA design to amplify signals with high PARP efficiently. In addition, ET has also been considered to be an effective solution in the structure of the BTS and UE PAs due to its flexibility for multimode multiband (MMMB) operations [43]. Fundamentally, the main idea of envelope tracking, which is a variant that has emerged from EER, is that the voltage supply is adjusted dynamically in conjunction with the envelope of the input signal, as shown in Figure 2.5. As a result of tracking

the envelope of the input signal, the efficiency of the PA will increase dramatically, as this technique maintains the PA near compression most of the time. As such, the impedance inverter is not required in ET, unlike the Doherty PA and as such, the ET has the potential to be inherently broadband. However, the power consumption in ET has the potential to be higher due to the additional requirement of the supply modulator, so careful design is necessary. In theory, the accuracy of the alignment between the envelope signal and the RF signal is less sensitive than is the case in EER, as in ET, both amplitude and phase information is retained in the RF path [44]. Another key feature of ET is that efficiency and linearity can be optimised through shaping the tracking signal via shaping functions. As the PA is driven further toward compression to yield maximum efficiency, the linearity of the PA degrades. Therefore, adding digital pre-distortion (DPD) is generally considered as compulsory to linearise the ET-PA performance to acceptable levels [45]. An efficient broadband ET-PA with octave bandwidth (2–4 GHz) with 45 % – 60 % drain efficiency is presented in [46]. In [47], an envelope driver with a power efficiency greater than 70 % for a modulation bandwidth of 40 MHz is shown.

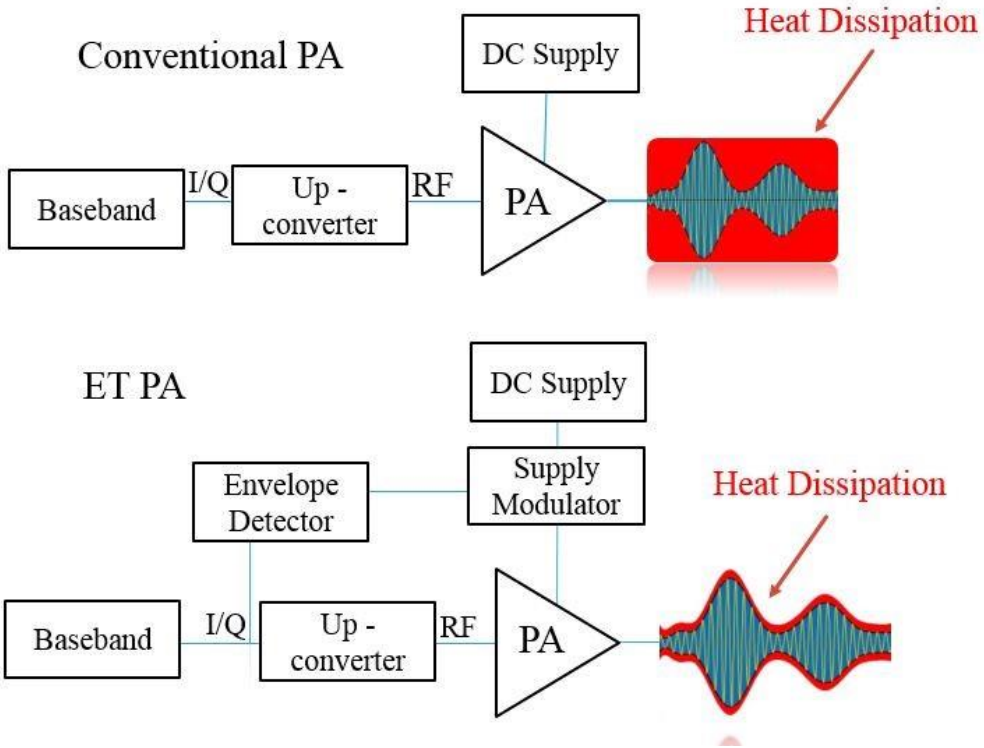

Figure 2.5 Comparison between conventional PA and ET-PA [43]

2.3.2.2.1 Envelope Tracking (ET) Mechanism

As earlier mentioned, modern communication systems use more complex modulation schemes, which have higher PAPRs to improve spectrum efficiency, leading to a substantial variation in the envelope of the modulated signal. This dynamic variation in signal power causes the PA to operate in the OBO instead of in saturation mode. The basic principle of ET is to track the input envelope by means of a controlled supply voltage for the PA. Thus, the supply voltage is reduced based on the envelope of the input signal without affecting the RF signal and keeping the PA compressed for most of the time. Typically, the general architecture of ET consists of a PA, envelope detector and supply modulator. Firstly, the envelope of the modulated

signal magnitude (*A*) is calculated from the in-phase (I) and quadrature (Q) components, which is expressed in the following equation (2.2):

$$A = \sqrt{I^2 + Q^2} \tag{2.2}$$

The equation in (2.2) suggests a linear relationship is needed between the dynamic supply signal and the envelope of the RF input signal, which in reality is not practical because the supply voltage cannot be allowed to drop to a zero to avoid gain collapse [48]. As a result, the envelope should be reshaped by a 'shaping function' that modifies the linear relationship to optimise the PA's performance in terms of efficiency, gain and linearity [49], [50]. Then, a highly efficient supply modulator is driven with the shaped envelope to produce a variable drain supply voltage for the PA. At the same time, the baseband I &Q signals are used in the up-conversion process to generate the required signal to drive the PA [51].

2.3.2.2.2 Supply Modulator

The correlation between the output power and efficiency that exists in the traditional fixed bias approach no longer exists in the ET-PA, which leads to an efficiency enhancement when the PA is operated in the OBO mode. With the fixed bias approach, the efficiency of the PA degrades as the output power backs off in order to maintain the linearity requirements. However, as the biasing voltage is varied dynamically, high efficiency over a wide range of output levels can be preserved, as seen in the envelope trajectory in Figure 2.6.

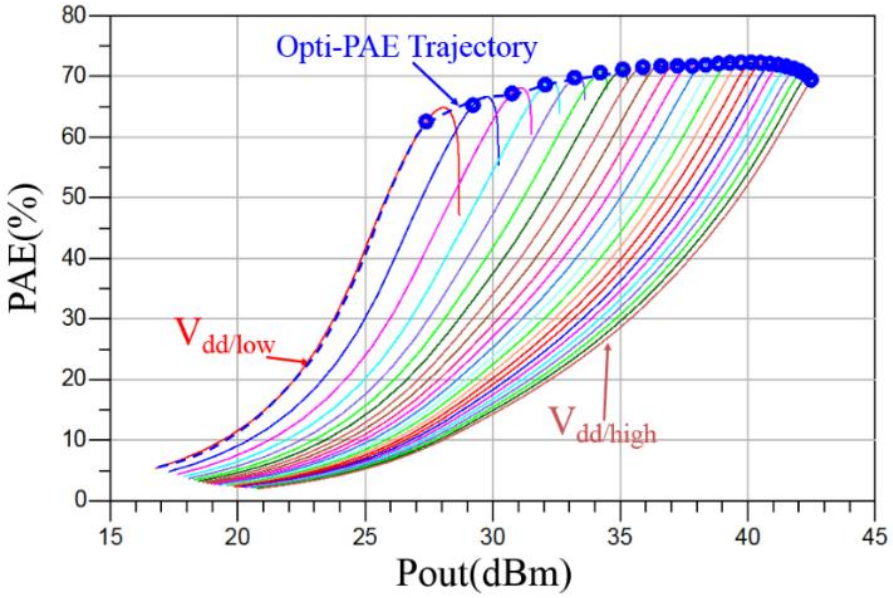

Figure 2.6 Efficiency improvement of PA when the bias is adjusted dynamically along with the envelope of the input signal (ADS simulation) Vdd/low is the minimum tracking voltage, the maximum tracking voltage is Vdd/high and the blue dots the desired trajectory

High efficiency in the ET approach can be achieved as long as the PA and the supply modulator is sufficiently efficient [52]. This is due to the fact that the instantaneous efficiency of the ET system (η_{ET}) is simply the product of the efficiency of the PA (η_{PA}) and the efficiency of supply modulator (η_{supply})[53], [54]:

$$\eta_{ET} = \eta_{PA} \cdot \eta_{supply} \tag{2.3}$$

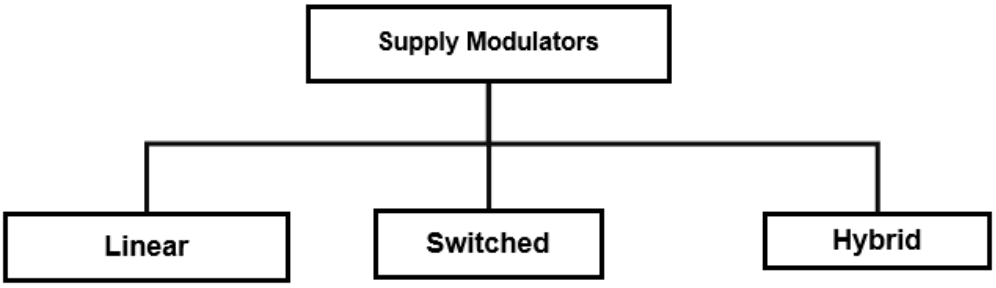

Figure 2.7 Supply modulator categories

In literature, the supply modulator is generally classified as being either a switching or linear type of modulator, or a combination of the two [55]. In comparison, the linear modulator has low output ripple (lower noise) and higher bandwidth but suffers from low efficiency. However, the switching modulator offers high efficiency with high output ripple but is typically only suitable for relatively narrow low bandwidth operation. The advantages of both linear and switching modulators can be combined with a hybrid modulator, which consists of a high efficient switching amplifier and a wideband linear modulator. The former deals with low-frequency components and high-frequency components are processed with the latter. Additionally, the linear modulator helps to reduce the switching noise (ripple) which is usually generated by the switching modulator [43], [56]. The performance of these supply modulators plays a vital role in determining the overall performance of the ET-PA in terms of modulation bandwidth, linearity, and overall efficiency. Despite extensive and ongoing research focussing on supply modulator design [57]–[59], there are still significant challenges in achieving the required performance in terms of modulation bandwidth, efficiency, and output voltage ripple, which limit the application of ET in commercial systems, as outlined in Table 2-2. The switched modulators are among the most efficient types of supply modulators, but they inherently produce a significant ripple voltage. Filtering this ripple not only causes significant losses, especially using high order filters [60] but also reduces the achievable modulation bandwidth at a given switching frequency. However, using digital pre-distortion (DPD) or reshaping the envelope might be a good option to

diminish the effect of the output ripple.

Table 2-2 Comparison of different supply modulator structure performance [2]

	Linear Modulator	**Switched Modulator**	**Hybrid Modulator**
Efficiency	Low	High	Medium
Linearity	Good	Medium	Good
Bandwidth	Wide	Narrow	Wide
Complexity	Simple	Medium	High
Output Ripple	Low	High	Medium

2.3.2.3 Auxiliary Envelope Tracking

The third enhancement technique for power amplifier efficiency is the Auxiliary Envelope Tracking (AET) technique. The AET technique is a variation of the classical ET system, which improves both the linearity and efficiency of the PA. The ET and AET techniques have a similar basic configuration. AET, however, uses a different mechanism to produce the drain modulated signal, where DC and AC components of the AET tracking signal generated separately, and then added in a specific manner using a special bifilar wound transformer-based combiner. The combined AET signal is then applied to the PA, as illustrated in Figure 2.8. In ET, however, the supply modulator must deal with both AC and DC components simultaneously [59].

Unlike the other techniques, the architecture of the AET system does not comprise additional building blocks dedicated to improving the linearity of the PA, such as digital pre-distortion (DPD). In addition, the structure of AET, which includes a simple source-follower, diplexer and RF transformer, is easy to realise and implement [60] and really focus on applications that can benefit from a simple and cost-effective solution.

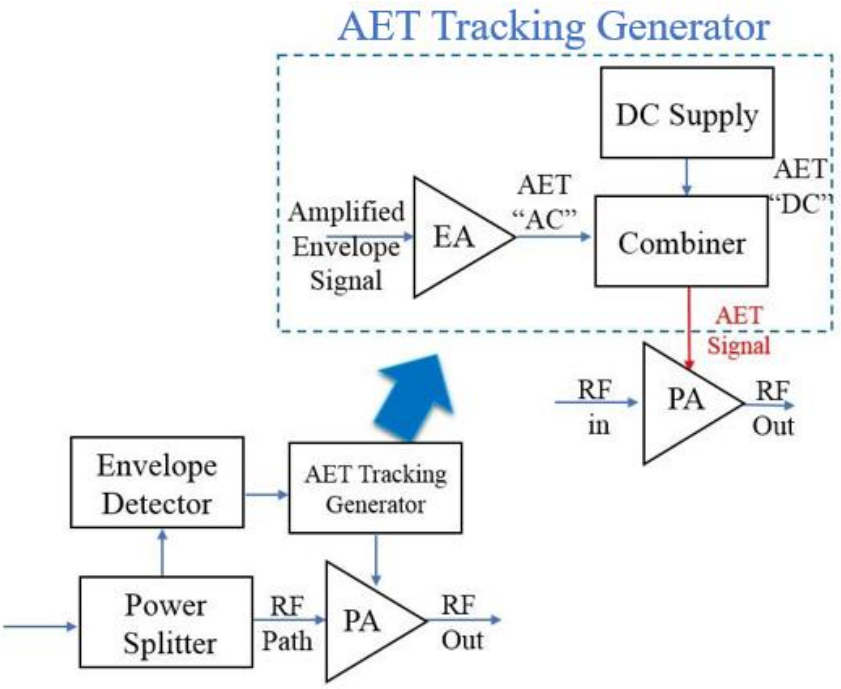

Figure 2.8 Basic architecture of the AET

2.4 Measurement techniques

Over the years, numerous microwave techniques have been introduced to measure and characterise RF devices. Starting from simple instruments such as the power meter, network analyser and spectrum analyser which are generally used to

perform nonlinear measurements and extending to more complex instruments e.g. the Large Signal Vector Network Analyser (LSNA) that allows the full nonlinear behaviour of a device or circuit to be characterised. Since these microwave measurement techniques have been introduced, they have had a significant influence on the PA design process and testing of RF devices. The design procedure of PAs typically begins with the complete and accurate measurement and characterisation of a device. The design and measurement contribution of these advanced network analysers have been enhanced over the years. For example, the functionality of NVNAs has been extended to characterise the performance of an PA under different loading conditions instead of a fixed load, which is a technique called load pull [63]. Moreover, the excitation signal which plays a vital role to determine the nonlinear response of PA has been developed from the CW signal to multi-tone or modulated signals. The following section provides and overview of the measurement techniques that are used to measure and characterise PAs under either CW or modulated excitation, with associated advantages, disadvantages, and limitations.

2.4.1 Power meter

A power meter is one of the most useful pieces of equipment in the microwave laboratory which can be used to characterise circuit power transfer characteristics, such as amplifiers, mixers, limiters, etc. They can also be utilised to measure output power, efficiency, insertion loss (or gain) and return loss, similar to using a spectrum analyser, but at a fraction of the equipment cost [64].

2.4.2 Spectrum Analyser

A spectrum analyser, which is a frequency domain instrument, is used to measure and display electrical signals according to their amplitude and frequencies. The frequency range where a spectrum analyser is considered a powerful tool to measure these signals ranges from around 2 Hz to about 110 GHz [65]. The main use of a spectrum analyser is the measurement of unknown signals, modulation, distortion, and noise. As the nonlinearity of active devices introduces distortions to systems, the spectrum analyser can be used to measure these distortions which mainly include harmonics products and intermodulation distortion components (IMDs). Moreover, the spectrum analyser can be utilised to measure the noise figure and signal-to-noise ratio (SNR) [66]. Nevertheless, the main drawback of the spectrum analyser is the ability to measure only the magnitude and not the phase information, which limits its usefulness in making measurements that are needed to model the full behaviour of active devices. Even with this limitation, real-time broadband behaviour of the spectrum analyser delivers the ability to detect and measure spurious signals resulting from the instabilities of the devices.

2.4.3 Vector Network Analyser

A traditional vector network analyser can provide the measurement for both magnitude and phase of an electrical signal. The s-parameter measurements of RF devices are the basic capability of the vector network analyser where the amplitude and phase ratio information can be measured and converted to impedance or

admittance over a wide range of frequencies from DC to 120 GHz [67]. Even though s-parameter measurements provide valuable information, this measurement approach is only valid if the superposition principle holds (superposition principle prevents the transformation of energy from the stimulus frequency to other harmonic frequencies). Therefore, the vector network analyser, in its traditional form, although extremely useful in RF, microwave and mm-wave design, is not able to measure and characterise the full nonlinear features of active devices because the nonlinearity will produce harmonics and intermodulation distortion components (IMD) [68].

2.4.4 Large Signal Network Analyser

The large signal network analyser (LSNA) is similar to the vector network analyser. The LSNA, however, has the ability to measure the absolute values of the incident and the reflected traveling waves and not just their ratios. Importantly, the LSNA is also able to measure the relative phase between frequency components that comprise these signals. Examples are Agilent's Large-Signal Network Analyser which operates from 10 MHz to 67 GHz [69] and Maury Microwave's MT4463B Large-Signal Network Analyser operating from 600 MHz to 50 GHz [70]. These absolute measurements of traveling waves can be easily transformed into voltages and current waveforms at a defined reference plane established through calibration, in the time-domain by means of an inverse Fourier transform.

2.4.5 Load Pull

Load pull is a recognized technique frequently utilised initially in the PA design procedure to characterise the performance of a device under test (DUT), mainly transistors. The main concept of the load pull approach is to evaluate the response of a device as a function of either source-pull or load impedances in terms of input power, bias, temperature, and other related parameters. In other words, with a load pull system, a set of controlled impedances are presented to DUT and simultaneously the performance parameters of the PA at each impedance are assessed.

The load pull system can be classified into two categories namely passive and active. The load pull approach is not limited to only fundamental frequency, but the load pull technique can be extended to harmonic frequencies, where the loads presented to the DUT at multiple frequencies could be considered at the same time. Then, all parameters of the PA performance are measured at various combinations of load impedance for fundamental and harmonic frequencies.

2.4.5.1 Passive Load Pull System

In the passive load pull system, the load impedance is varied using a mechanical stub tuner impedance transformer between the DUT and (50 Ω) termination. The length of stub is used to control the magnitude of the output reflection coefficient (Γ_L) while the phase of the output reflection coefficient (Γ_L) is changed by the position of the stub. While single tuning stub is used to control the fundamental

frequency impedance, the harmonics impedances can be controlled via a combination of two, three or more stub tuners as shown in Figure 2.9 [71]. This passive load pull technique has many disadvantages such as the loss in the tuner and couplers which limits achievable reflection coefficient (Γ_L) below 1.0 while the harmonic tuning often requires an ideal reflection coefficient of(Γ_L) =1.0.

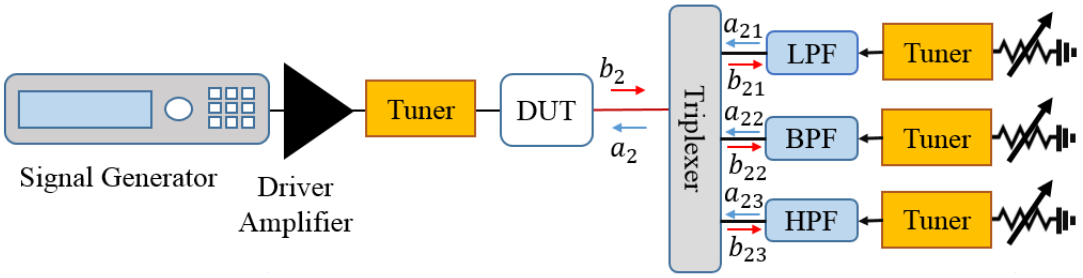

Figure 2.9 Generic system configuration for passive harmonic load-pull

2.4.5.2 Active Load Pull System

The loss disadvantage, which is the main limitation of the passive load system, can be addressed by using an active load pull system. The main idea of the active load technique is the ability to introduce any value of impedance to the DUT at both the input and output, which can be achieved by the synthesized signal. This injected signal presents the required harmonic impedances to produce a reflection coefficient of (Γ_L) =1.0 for fundamental frequency and other harmonic frequencies [72]. The active load pull systems can be classified into two categories:

- Closed-Loop Systems and Envelope Systems.
- Open Loop Systems.

2.4.5.3 Closed Loop Systems

The active closed-loop system which is shown in Figure 2.10 was first realised by Bava et al. [73]. The mechanism of this technology is based on appropriate adjustment of the phase and amplitude of the traveling wave, b_2. Then, it is injected back to the DUT output port, a_2, to realise the desired load reflection coefficient. This system is fast because the injected wave, a_2, will be a modified version of the traveling wave b_2. Therefore, any change in the DUT characteristics will have an immediate effect on the emulated impedance. Furthermore, the drive-level will be independent of emulated load impedances. However, the system is prone to instability and oscillations, especially if the injection amplifier is broadband and there are excessive leakages in the various passive components. Even though the oscillations can be reduced by implement filtering, the bandwidth of this method will be reduced to be narrowband, and the cost will increase [74].

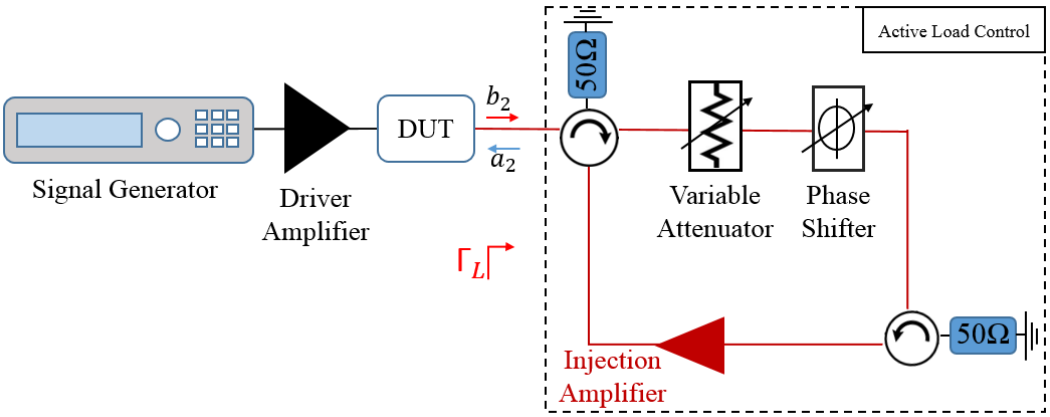

Figure 2.10 Active closed-loop configuration

2.4.5.4 Active Envelope Load-pull Systems (AELP)

The Active Envelope Load-pull system (AELP) is an enhanced version of the closed-loop technique. This technique was introduced by Williams et al. in [75] for the first time where the traveling wave b_2 is down converted to a baseband signal $(I \ \& \ Q)$ using a quadrature demodulator. This allows load pull at baseband frequencies which are realised using external control signals, X and Y as shown in Figure 2.11.

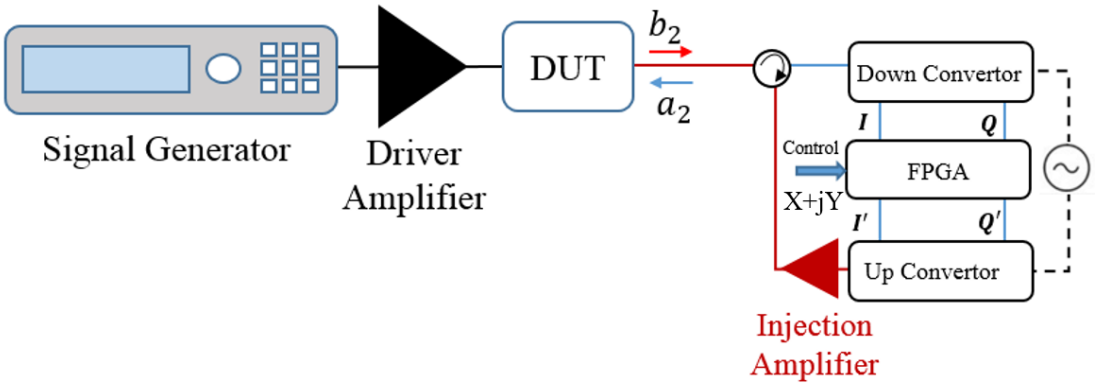

Figure 2.11 Basic diagram for Active Envelope Load-pull Systems (AELP)

Then, the modified versions of the baseband signals $(I' \ \& \ Q')$ are upconverted and injected into the output of the DUT after linear amplification in order to emulate the desired reflection coefficient. Thus, the risk of oscillation at RF frequencies is low since the feedback in the load pull system is at baseband frequencies and not at RF. More work was done by Hashmi et al [74]to enhance this approach to include robust and realisable calibration routines and delay compensation in the injection loop.

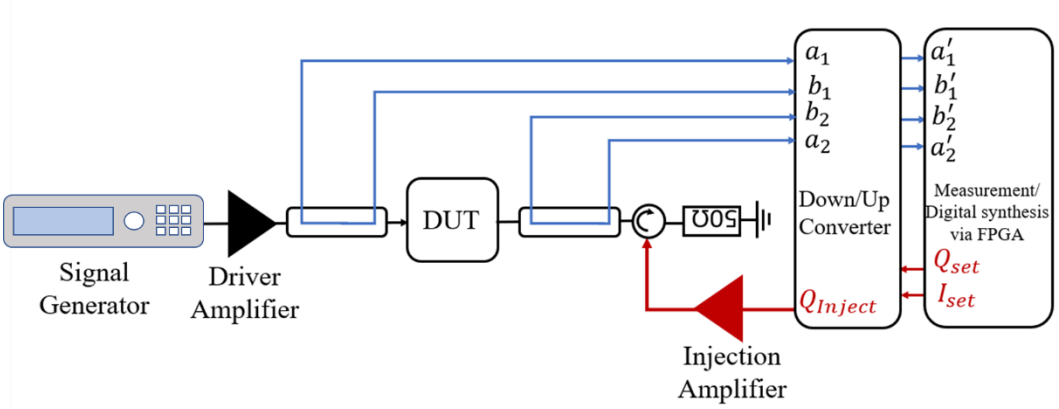

Figure 2.12 Mesuro rapid Load-pull (RLP) system configuration

Figure 2.12 shows a schematic of the Mesuro Rapid Load pull (RLP) system [76] which is an active closed load pull system based on a digital PXI tuner with high throughput. The output of the DUT is fed, after being attenuated and down converted, to a PXI chassis which comprises an FPGA module. The traveling waves (a_1, b_1,a_2 and b_2) incident and reflected from the DUT are down-converted to (a'_1 ,b'_1, a'_2 and b'_2) signals which are then manipulated within the FPGA card to produce a new reflection coefficient (I_{set} & Q_{set})which,agrees with that set by the user. Then, the modified signals (I_{set} & Q_{set}) are upconverted and amplified and injected back into the output of the DUT. Sharing a common local oscillator (LO) between the down and up-converter modules relaxes the requirement for the drive signal of the DUT and active loop to be phase-locked, which eliminates any drift in phase over time. The RLP has the capability to maintain constant impedance over the instantaneous bandwidth of up to 40 MHz. The frequency range of the RLP is typically limited by the FPGA module from 200 MHz to 4.4 GHz but could be extended to 40 GHz by adding a further up/down convertors in the loop.

2.4.5.5 Open Loop Active Load-pull

Takayama et al. [77] initially introduced the open-loop architecture which is shown in Figure 2.13. The input signal is split into two paths where the first part is used to drive the DUT while the other is used as a source to emulate the desired impedance at the fundamental frequency. The emulated impedance is varied manually using a mechanical phase shifter and a variable attenuator. Later, Ghannouchi et al [78] extended the system to control the measurement of second and third harmonics.

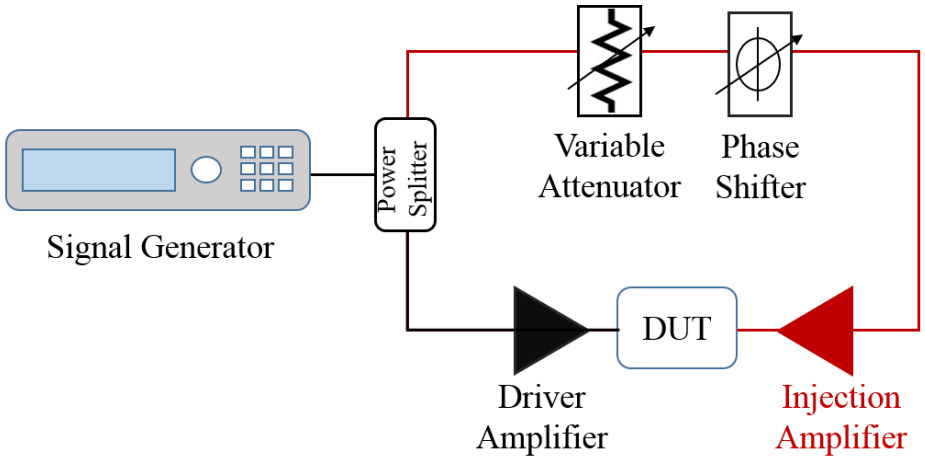

Figure 2.13 Open active load-pull configuration

After that, an active harmonic load-pull system with waveform measurement capabilities, a maximum power level of 30 W and frequency range between 0.5 - 12.5 GHz was introduced by Benedikt et al. [79]. However, the requirement to manually tune the load impedances for fundamental and harmonic components, as the input power level was changed during a power sweep, was the main restriction in the architecture of this system. As a result, the architecture requires numerous

iterations, particularly for multiple harmonics which slows the process. Therefore, a number of fast, multi-harmonic active load-pull approaches have been introduced in to accelerate the load pull process.

The *Anteverta* active load pull system is a wideband open-loop active harmonic load-pull system based on wideband data acquisition and wideband injection as shown in Figure 2.14 [80]. The injected signal that forms the required reflection coefficients are produced by a PXI-based baseband arbitrary waveform generator (AWG) which has a bandwidth of 80 MHz, then, up-converted using PXI-based in-phase/quadrature (I & Q) modulators. All AWGs and A/D converter modules are synchronized via an internally generated 10 MHz clock with an independent buffer on the backplane of the chassis. The local oscillator (LO) signal, which drives the I & Q mixers to up-convert the baseband signals, is independent of the PXIe chassis. Higher harmonics are generated using the I & Q mixers which are driven by LO signals using frequency multipliers. Furthermore, an external shared LO, which is also independent of the PXIe chassis, is used in the down-conversion of the signal, and power splitters and high-pass filters are then used to split signal harmonic components. As the I & Q mixing system allows a constant load impedance to be maintained over bandwidth, the system is able to load-pull a modulated signal over 1GHz bandwidth.

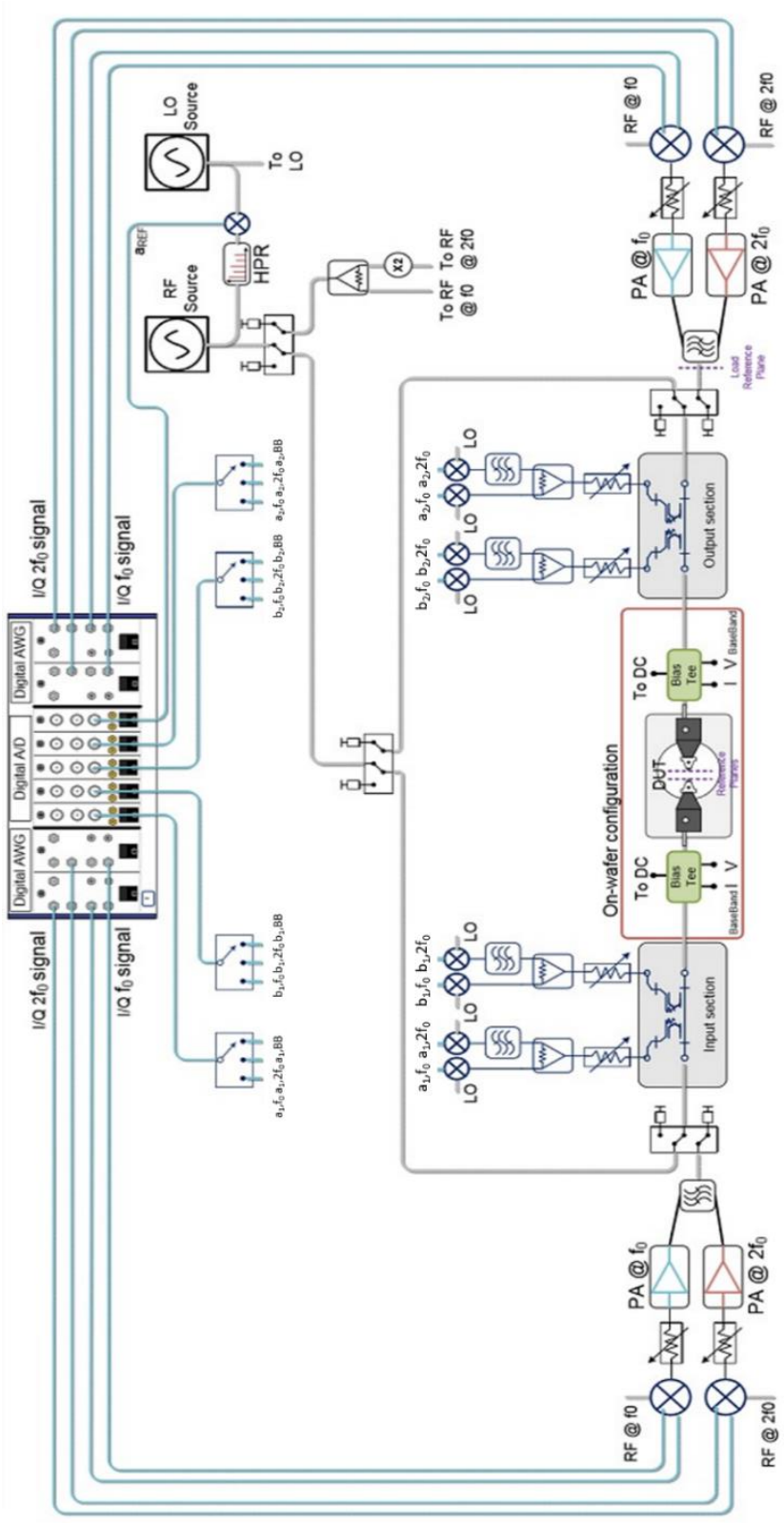

Figure 2.14 Antiverta open-loop active load-pull system configuration [78]

2.4.6 Envelope Tracking Measurement System

Traditional PA measurements requires a number of key instruments that can simply include a signal generator and some form of signal analyser. However, a complex measurement set up is required to fully characterise ET-PAs for modern communications systems. The difficulty in the ET measurement is a consequence of the fact that an ET system comprises several subsystems; as well as the ET-PA itself, there is envelope generation, the supply modulator, and the linearization system. In an ET system, the PA can be considered as a three-port device, with a dynamically controlled drain bias voltage. Practically, the ET measurement system consists of an Envelope Tracking Control Host, which is the digital domain of the system, an RF signal generator, an Arbitrary Waveform Generator, and a Vector Signal Analyser as shown in Figure 2.15.

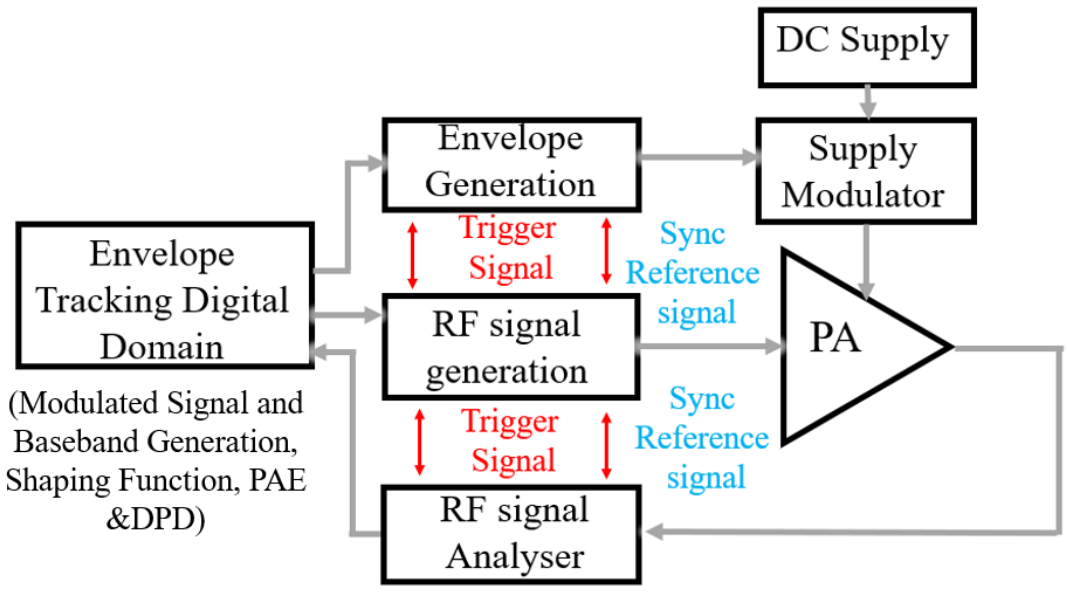

Figure 2.15 Block diagram of an envelope tracking characterisation system

Also, synchronization between theses different instruments is required which is a major challenge from a test and a characterisation perspective. Essentially, the synchronization between the RF signal generator and the baseband arbitrary waveform generator (AWG) in an envelope tracking system. Therefore, a measurement system for the envelope requires more complex measurement than fixed bias PAs.

Recently, several commercial ET measurement systems were introduced by companies such as National Instruments (NI) [81] and Rohde & Schwarz [82]. The NI ET measurement system is based on PXIe chassis equipped with Vector Signal Transfer (VST), Arbitrary Wave Generator (AWG) and high-speed oscilloscope where all these modules are interconnected via the backplane of chassis as shown in Figure 2.16. The software which is mainly used to control the measurement system is a National Instruments software package called RFIC. However, LabView software could be used to do further measurements which give this system a good degree of flexibility.

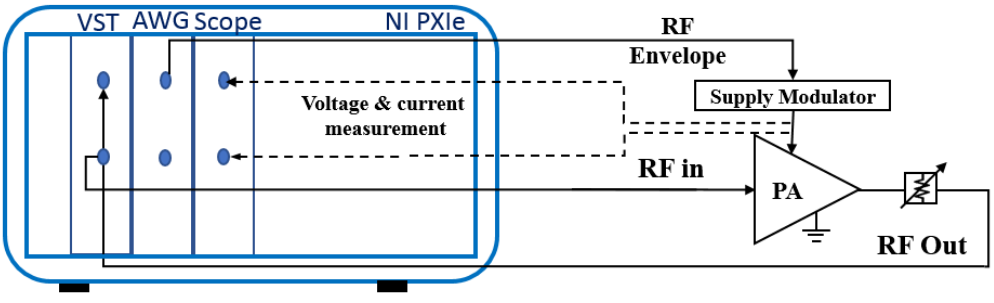

Figure 2.16 Block diagram for NI ET measurement system

However, Rohde & Schwarz ET measurement system consists of a vector signal generator (SMW) signal analyser (FSW) as presented in Figure 2.17. Both the RF signal and the corresponding envelope are generated by the SMW. The FSW has two additional baseband input ports to the RF port used to measure the drain current and voltage and enhance the synchronization between the RF and baseband for efficiency measurement. The system is controlled with a standard software which importantly, cannot be customized.

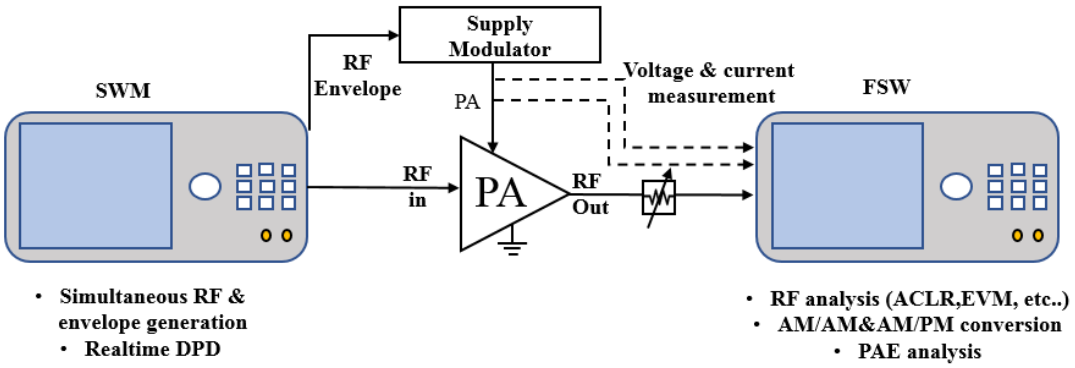

Figure 2.17 Simple diagram for Rohde & Schwarz ET measurement system

Both systems have all ET functions including synchronization, time alignment between the RF signal and the envelope, shaping function, DPD, and efficiency measurement. However, R&S has the capability to measure instantaneous efficiency.

2.5 Conclusion

This chapter has shown significant research into high efficiency PA design, and that this is taking place within academia and industry, and which has resulted in a number of enhancements and approaches for efficiency over dynamic range, by

dynamically changing either the load impedance or the supply voltage. The ET approach is one of the most promising potential solutions to tackle these issues, among numerous other improvement techniques that have been developed. The ET mechanism is introduced, and several architectures of supply modulator are identified and compared in terms of their advantages and disadvantages. The chapter also discusses several microwave measurement techniques that are used to characterise RF devices, starting from simple instruments such as the power meter, network analyser and spectrum analyser which are generally used to perform nonlinear measurements and extending to more complex instruments e.g. the Large Signal Network Analyser (LSNA) that allows the full nonlinear behaviour of a device to be characterised.

The chapter also introduces different types of load pull system which is a well-established technique to characterise the performance of a device at the early stage of the PA design procedure, with advantages and disadvantages of various load pull architectures are outlined. In active envelope load-pull, the emulated impedance environment is generally insensitive to drive level and bias condition, a property that can significantly speed-up device measurements. Also, the emulated impedance environment can be held constant over a modulation bandwidth, which enables the system to load pull devices under realistic modulated signal conditions.

Finally, as the NI ET measurement system has flexibility in terms of its control software and its PXIe standard interface, which can be upgraded or integrated easily

with any PXIe system, the NI ET system is selected to be used in this research work. However, the full ET measurement system still needed to be assembled, realised, tested and validated. Only then was it possible to integrate the system with the Mesuro Rapid Load pull system which is discussed previously to load pull RF devices and apply DPD. Following these steps, it is possible for a fully emulated system for ET characterisation in conjunction with DPD can be addressed and is discussed in later chapters.

2.6 Reference

[1] S. Cripps, RF power amplifiers for wireless communications. Artech House, 2006.

[2] F. H. Raab et al., "RF and microwave power amplifier and transmitter technologies-Part 1," High Frequency Electronics, vol. 2, no. 3, pp. 22-36, 2003.

[3] P. B. Kenington, High linearity RF amplifier design. Artech House, Inc., 2000.

[4] N. Kumar, C. Prakash, A. Grebennikov, and A. Mediano, "High-efficiency broadband parallel-circuit class E RF power amplifier with reactance-compensation technique," IEEE Transactions on Microwave Theory and Techniques, vol. 56, no. 3, pp. 604-612, 2008.

[5] K. Chen and D. Peroulis, "Design of Broadband Highly Efficient Harmonic-Tuned Power Amplifier Using In-Band Continuous Class- ${\hbox{F}}^{-1}/{\hbox{F}}$ Mode Transferring," in IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 12, pp. 4107-4116, Dec. 2012.

[6] A. Sheikh et al., "Systematic waveform engineering enabling high efficiency modes of operation in Si LDMOS at both L-band and S-band frequencies," 2008 IEEE MTT-S International Microwave Symposium Digest, Atlanta, GA, USA, 2008, pp. 1143-1146.

[7] S. Gao et al., "Microwave Class-F and Inverse Class-F Power Amplifiers Designs using GaN Technology and GaAs pHEMT," 2006 European Microwave Integrated Circuits Conference, Manchester, 2006, pp. 493-496.

[8] P. Wright, J. Lees, J. Benedikt, P. J. Tasker and S. C. Cripps, "A Methodology for Realizing High Efficiency Class-J in a Linear and Broadband PA," in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 12, pp. 3196-3204, Dec. 2009.

[9] S. C. Cripps, P. J. Tasker, A. L. Clarke, J. Lees and J. Benedikt, "On the Continuity of High Efficiency Modes in Linear RF Power Amplifiers," in IEEE Microwave and Wireless Components Letters, vol. 19, no. 10, pp. 665-667, Oct. 2009.

[10] T. Canning, P. J. Tasker and S. C. Cripps, "Continuous Mode Power Amplifier Design Using Harmonic Clipping Contours: Theory and Practice," in IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 1, pp. 100-110, Jan. 2014.

[11] S. Liao and Y. E. Wang, "A high efficiency WCDMA power amplifier with Pulsed Load Modulation (PLM)," 2010 IEEE Radio and Wireless Symposium (RWS), New Orleans, LA, 2010, pp. 49-52.

[12] H. Cao, H. Mashad Nemati, A. Soltani Tehrani, T. Eriksson, J. Grahn and C. Fager, "Linearization of Efficiency-Optimized Dynamic Load Modulation Transmitter

Architectures," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 4, pp. 873-881, April 2010.

[13] F. Lepine, R. Jos and H. Zirath, "A Load Modulated High Efficiency Power Amplifier," 2006 European Microwave Conference, Manchester, 2006, pp. 411-414.

[14] G. Tant, A. Giry, P. Vincent, J. Arnould and J. Fournier, "A 2.14GHz watt-level power amplifier with passive load modulation in a SOI CMOS technology," 2013 Proceedings of the ESSCIRC (ESSCIRC), Bucharest, 2013, pp. 189-192.

[15] D. J. Shepphard, J. Powell and S. C. Cripps, "An Efficient Broadband Reconfigurable Power Amplifier Using Active Load Modulation," in IEEE Microwave and Wireless Components Letters, vol. 26, no. 6, pp. 443-445, June 2016.

[16] F. Raab, "Efficiency of Outphasing RF Power-Amplifier Systems," in IEEE Transactions on Communications, vol. 33, no. 10, pp. 1094-1099, October 1985.

[17] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho and B. Kim, "The Doherty Power Amplifier: Review of Recent Solutions and Trends," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 2, pp. 559-571, Feb. 2015.

[18] H. M. Nemati, C. Fager, U. Gustavsson, R. Jos and H. Zirath, "Design of Varactor-Based Tunable Matching Networks for Dynamic Load Modulation of High Power Amplifiers," in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 5, pp. 1110-1118, May 2009.

[19] K. Buisman et al., "Low-distortion, low-loss varactor-based adaptive matching networks, implemented in a silicon-on-glass technology," 2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers, Long Beach, CA, USA, 2005, pp. 389-392.

[20] F. H. Raab, "Efficiency of Doherty RF Power-Amplifier Systems," in IEEE Transactions on Broadcasting, vol. BC-33, no. 3, pp. 77-83, Sept. 1987.

[21] D. Gustafsson, C. M. Andersson, and C. Fager, "A modified Doherty power amplifier with extended bandwidth and reconfigurable efficiency," IEEE transactions on microwave theory and techniques, vol. 61, no. 1, pp. 533-542, 2013.

[22] V. Camarchia et al., "Bandwidth extension of GaN Doherty power amplifier: Effect on power, efficiency and linearity," 2013 IEEE International Wireless Symposium (IWS), Beijing, 2013, pp. 1-4.

[23] X. A. Nghiem, J. Guan and R. Negra, "Design of a broadband three-way sequential Doherty power amplifier for modern wireless communications," 2014 IEEE MTT-S International Microwave Symposium (IMS2014), Tampa, FL, 2014, pp. 1-4.

[24] B. Kim, I. Kim and J. Moon, "Advanced Doherty Architecture," in IEEE Microwave Magazine, vol. 11, no. 5, pp. 72-86, Aug. 2010.

[25] R. Pengelly, C. Fager and M. Ozen, "Doherty's Legacy: A History of the Doherty Power Amplifier from 1936 to the Present Day," in IEEE Microwave Magazine, vol. 17, no. 2, pp. 41-58, Feb. 2016.

[26] S. C. Cripps, Advanced techniques in RF power amplifier design. Artech House, 2002.

[27] R. Paulo, T. Drechsel, R. Wolf, C. Carta and F. Ellinger, "High efficient Doherty power amplifier for wireless communication: An RF power amplifier for upcoming radio standards like LTE and LTE-Advanced in microstrip technology," International Multi-Conference on Systems, Signals & Devices, Chemnitz, 2012, pp. 1-6.

[28] H. Chireix, "High Power Outphasing Modulation," in Proceedings of the Institute of Radio Engineers, vol. 23, no. 11, pp. 1370-1392, Nov. 1935.

[29] D. Cox, "Linear Amplification w

ith Nonlinear Components," in IEEE Transactions on Communications, vol. 22, no. 12, pp. 1942-1945, December 1974.

[30] P. A. Godoy, S. Chung, T. W. Barton, D. J. Perreault and J. L. Dawson, "A 2.4-GHz, 27-dBm Asymmetric Multilevel Outphasing Power Amplifier in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 47, no. 10, pp. 2372-2384, Oct. 2012.

[31] Y. Chen, K. Jheng, A. Wu, H. Tsao and B. Tzeng, "Multilevel LINC System Design for Wireless Transmitters," 2007 International Symposium on VLSI Design, Automation and Test (VLSI-DAT), Hsinchu, 2007, pp. 1-4.

[32] A. Bogusz, J. Lees, R. Quaglia, G. Watkins and S. C. Cripps, "A Waveform-Engineered Outphasing RFPA Using a Broadband Balun Combiner," 2018 IEEE/MTT-S International Microwave Symposium - IMS, Philadelphia, PA, 2018, pp. 301-303.

[33] K. Bumman, M. Junghwan and K. Ildu, "Efficiently Amplified," in IEEE Microwave Magazine, vol. 11, no. 5, pp. 87-100, Aug. 2010.

[34] A. K. Mustafa, V. Bassoo and M. Faulkner, "Reducing the drive signal bandwidths of EER microwave power amplifiers," 2009 IEEE MTT-S International Microwave Symposium Digest, Boston, MA, 2009, pp. 1525-1528.

[35] Z. Yusoff, J. Lees, J. Benedikt, P. J. Tasker and S. C. Cripps, "Linearity improvement in RF power amplifier system using integrated Auxiliary Envelope Tracking system," 2011 IEEE MTT-S International Microwave Symposium, Baltimore, MD, 2011, pp. 1-4.

[36] I I. A. Rumyancev, "Efficient amplification techniques for signals with high PAPR," 2015 IEEE NW Russia Young Researchers in Electrical and Electronic Engineering Conference (EIConRusNW), St. Petersburg, 2015, pp. 139-142.

[37] L. R. Kahn, "Single-Sideband Transmission by Envelope Elimination and Restoration," in Proceedings of the IRE, vol. 40, no. 7, pp. 803-806, July 1952.

[38] F. H. Raab and D. J. Rupp, "High-efficiency single-sideband HF/VHF transmitter based upon envelope elimination and restoration," 1994 Sixth International Conference on HF Radio Systems and Techniques, York, UK, 1994, pp. 21-25.

[39] A. W. Hietala, "A quad-band 8PSK/GMSK polar transceiver," 2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers, Long Beach, CA, USA, 2005, pp. 9-12.

[40] F. Wang et al., "An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 12, pp. 4086-4099, Dec. 2006.

[41] M. Vasić et al., "Efficient and Linear Power Amplifier Based on Envelope Elimination and Restoration," in IEEE Transactions on Power Electronics, vol. 27, no. 1, pp. 5-9, Jan. 2012.

[42] F. H. Raab, "Split-band modulator for Kahn-technique transmitters," 2004 IEEE MTT-S International Microwave Symposium Digest (IEEE Cat. No.04CH37535), Fort Worth, TX, USA, 2004, pp. 887-890 Vol.2.

[43] J. Choi, D. Kim, D. Kang and B. Kim, "A Polar Transmitter With CMOS Programmable Hysteretic-Controlled Hybrid Switching Supply Modulator for Multistandard Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 7, pp. 1675-1686, July 2009.

[44] J. Hendy, "Envelope tracking for RF power amplifiers in mobile handsets." [Online]. Available: https://www.techdesignforums.com/practice/technique/envelope-tracking-for-rf-power-amplifiers-in-mobile-handsets/

[45] P. M. Lavrador, T. R. Cunha, P. M. Cabral and J. Pedro, "The Linearity-Efficiency Compromise," in IEEE Microwave Magazine, vol. 11, no. 5, pp. 44-58, Aug. 2010.

[46] M. R. Duffy, G. Lasser, M. Olavsbråten, E. Berry and Z. Popović, "Efficient Multisignal 2–4-GHz Power Amplifier With Power Tracking," in IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 12, pp. 5652-5663, Dec. 2018.

[47] H. Gheidi, P. Theilmann, J. J. Yan, T. Nakatani and D. Kimball, "A broadband envelope-tracking push-pull GaN power amplifier using grounded-coplanar ring Marchand balun," 2018 IEEE 19th Wireless and Microwave Technology Conference (WAMICON), Sand Key, FL, 2018, pp. 1-4.

[48] A. Bräckle, L. Rathgeber, F. Siegert, S. Heck and M. Berroth, "Power supply modulation for RF applications," 2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC), Novi Sad, 2012, pp. LS8d.3-1-LS8d.3-5.

[49] M. O. H. Khalifa, A. Abdelhafiz, A. Kwan, F. M. Ghannouchi and O. Hammi, "Behavioral modeling of envelope tracking power amplifier using Volterra series model and compressed sampling," 2015 IEEE International Wireless Symposium (IWS 2015), Shenzhen, 2015, pp. 1-4.

[50] D. Kim, D. Kang, J. Choi, J. Kim, Y. Cho and B. Kim, "Optimization for Envelope Shaped Operation of Envelope Tracking Power Amplifier," in IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 7, pp. 1787-1795, July 2011.

[51] D. F. Kimball et al., "High-efficiency envelope-tracking W-CDMA base-station amplifier using GaN HFETs," IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 11, pp. 3848-3856, 2006.

[52] J. Kim, D. Kim, Y. Cho, D. Kang, B. Park and B. Kim, "Envelope-Tracking Two-Stage Power Amplifier With Dual-Mode Supply Modulator for LTE Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 1, pp. 543-552, Jan. 2013.

[53] J. Y. Jonmei, D. Kimball, C. Hsia, H. Pan, S. Ricketts and H. Ghajari, "High-efficiency, high-linearity envelope tracking power amplifier for mobile UHF applications," 2010 - MILCOM 2010 MILITARY COMMUNICATIONS CONFERENCE, San Jose, CA, 2010, pp. 1572-1576.

[54] J. Jeong, D. F. Kimball, M. Kwak, C. Hsia, P. Draxler and P. M. Asbeck, "Modeling and Design of RF Amplifiers for Envelope Tracking WCDMA Base-Station Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 9, pp. 2148-2159, Sept. 2009.

[55] X. Ruan, Y. Wang and Q. Jin, "A review of envelope tracking power supply for mobile communication systems," in CPSS Transactions on Power Electronics and Applications, vol. 2, no. 4, pp. 277-291, December 2017.

[56] F. Wang, D. F. Kimball, D. Y. Lie, P. M. Asbeck and L. E. Larson, "A Monolithic High-Efficiency 2.4-GHz 20-dBm SiGe BiCMOS Envelope-Tracking OFDM Power Amplifier," in IEEE Journal of Solid-State Circuits, vol. 42, no. 6, pp. 1271-1281, June 2007.

[57] P. T. Theilmann, J. J. Yan, C. Vu, J. Moon, H. P. Moyer and D. F. Kimball, "A 60MHz Bandwidth High Efficiency X-Band Envelope Tracking Power Amplifier," 2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Monterey, CA, 2013, pp. 1-4.

[58] A. Disserand, A. Martin, P. Bouysse and R. Quéré, "High efficiency GaN HEMT switching device with integrated driver for envelope tracking modulators," 2018 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMIC), Brive La Gaillarde, 2018, pp. 1-3.

[59] N. Wolff, W. Heinrich and O. Bengtsson, "100-MHz GaN-HEMT Class-G Supply Modulator for High-Power Envelope-Tracking Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 3, pp. 872-880, March 2017.

[60] S. Paul, N. Wolff, C. Delepaut, V. Valenta, W. Heinrich and O. Bengtsson, "Analysis of Dissipated Power in Envelope Amplifier Output Filters," 2018 48th European Microwave Conference (EuMC), Madrid, 2018, pp. 515-518.

[61] Z. Yusoff, J. Lees, J. Benedikt, P. J. Tasker and S. C. Cripps, "Linearity improvement in RF power amplifier system using integrated Auxiliary Envelope

Tracking system," 2011 IEEE MTT-S International Microwave Symposium, Baltimore, MD, 2011, pp. 1-4.

[62] Z. Yusoff et al., "Simple and low-cost tracking generator design in envelope tracking radio frequency power amplifier system for WCDMA applications," in IET Microwaves, Antennas & Propagation, vol. 7, no. 10, pp. 802-808, 16 July 2013.

[63] V. Camarchia, V. Teppati, S. Corbellini and M. Pirola, "Microwave Measurements Part II Non-linear Measurements," in IEEE Instrumentation & Measurement Magazine, vol. 10, no. 3, pp. 34-39, June 2007.

[64] Keysight Technologies. "Power Meters and Power Sensors." https://literature.cdn.keysight.com/litweb/pdf/5989-7837EN.pdf?id=1633170 (accessed 2019).

[65] Keysight Technologies. "Keysight Technologies X-Series Signal Analysers." https://literature.cdn.keysight.com/litweb/pdf/5992-1316EN.pdf?id=2699588 (accessed 2019).

[66] Keysight Technologies. "Spectrum Analysers (Signal Analysers)." https://www.keysight.com/en/pcx-x2015002/spectrum-analyser s-signal-analysers?cc=US&lc=eng (accessed 2019).

[67] Keysight Technologies. "Microwave Network Analyser s PNA-X Series." https://literature.cdn.keysight.com/litweb/pdf/5990-4592EN.pdf?id=1900906-1-eng (accessed 2018).

[68] Tektronix. "Introduction to Vector Network Analysers Basics." https://www.tek.com/document/primer/introduction-vector-network-analyser s-basics (accessed 2019).

[69] Keysight Technologies. "Nonlinear Vector Network Analyser (NVNA)." http://literature.cdn.keysight.com/litweb/pdf/5989-8575EN.pdf (accessed 2019).

[70] Maury Microwave. "MT4463 Large - Signal Network Analyser." http://www.nmdg.be/files/MT4463DataSheet.pdf (accessed 2019).

[71] F. M. Ghannouchi and M. S. Hashmi, "Load-pull techniques and their applications in power amplifiers design (invited)," 2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Atlanta, GA, 2011, pp. 133-137.

[72] A. Ferrero and M. Pirola, "Harmonic Load-Pull Techniques: An Overview of Modern Systems," in IEEE Microwave Magazine, vol. 14, no. 4, pp. 116-123, June 2013.

[73] G. P. Bava, U. Pisani and V. Pozzolo, "Active load technique for load-pull characterisation at microwave frequencies," in Electronics Letters, vol. 18, no. 4, pp. 178-180, 18 February 1982.

[74] M. S. Hashmi and F. M. Ghannouchi, "Introduction to load-pull systems and

their applications," in IEEE Instrumentation & Measurement Magazine, vol. 16, no. 1, pp. 30-36, February 2013.

[75] T. Williams, B. Wee, R. Saini, S. Mathias and M. V. Bossche, "A digital, PXI-based active load-pull tuner to maximize throughput of a load-pull test bench," 83rd ARFTG Microwave Measurement Conference, Tampa, FL, 2014, pp. 1-4.

[76] M. S. Hashmi, A. L. Clarke, S. P. Woodington, J. Lees, J. Benedikt and P. J. Tasker, "Electronic multi-harmonic load-pull system for experimentally driven power amplifier design optimization," 2009 IEEE MTT-S International Microwave Symposium Digest, Boston, MA, 2009, pp. 1549-1552.

[77] Y. Takayama, "A New Load-Pull Characterization Method for Microwave Power Transistors," 1976 IEEE-MTT-S International Microwave Symposium, Cherry Hill, NJ, USA, 1976, pp. 218-220.

[78] F. M. Ghannouchi, F. Beauregard and A. B. Kouki, "Large-signal stability and spectrum characterization of a medium power HBT using active load-pull techniques," in IEEE Microwave and Guided Wave Letters, vol. 4, no. 6, pp. 191-193, June 1994.

[79] J. Benedikt, R. Gaddi, P. J. Tasker, M. Goss and M. Zadeh, "High power time domain measurement system with active harmonic load-pull for high efficiency base station amplifier design," 2000 IEEE MTT-S International Microwave Symposium Digest (Cat. No.00CH37017), Boston, MA, USA, 2000, pp. 1459-1462 vol.3.

[80] M. Marchetti, "Mixed-signal instrumentation for large-signal device characterisation and modelling," Ph.D. dissertation, 2013. Microelectronics & Computer Engineering, Delft University of Technology,

[81] S. Ferguson and H. Nelson, "Envelope Tracking Fundamentals and Test Solutions," MICROWAVE JOURNAL, vol. 56, no. 6, pp. 66-+, 2013.

[82] Rohde & Schwarz. " Envelope Tracking and Digital Pre-Distortion Test Solution for RF Amplifiers." https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_application/application_notes/1gp104/1GP104_2E_ET_DPD_testing_for_amplifiers.pdf (accessed 2019).

Chapter 3

Realising an Envelope Tracking Measurement System

3.1 Introduction & Motivation

The objective of this chapter is to fully demonstrate and prove the concept of an ET characterisation system for three main reasons.

- To fully test the capabilities of the NI ET measurement system and ensure the system meets the requirements.
- Provide the ability of the CHFE to conduct ET-PA measurements for the ET-focussed EPSRC project partners.
- Allow investigations into the interaction between the PA and supply modulator, and to provide feedback to the other panthers that enables them to optimise switching modulator design, such as output ripple effects which will be discussed later.

This chapter starts by discussing the essential requirements for an ET-PA measurement system. Then, it will demonstrate the NI ET system which will be used to realise the ET measurements. After this, the chapter will describe the design of the necessary hardware which is used to implement the tests and then demonstrate the

capabilities of the ET measurement system. This includes designing a demonstration linear amplifier, which was used as an ET modulator, to supply the PA with the necessary dynamic drain biasing voltage. After that, the performance of the modulator is evaluated to identify its limitations. Then, a low-power demonstrator PA was designed and built based on the capabilities of the supply modulator. In addition to this, an integrated sensor circuit is designed to measure the instantaneous drain current and voltage. The remainder of the chapter demonstrates an experimental validation of the ET characterisation system using 10 MHz LTE modulation for the first time, at Cardiff University.

3.2 Envelope Tracking Measurement System Requirements

It has been discussed in the literature review chapter that deploying a full ET system faces several challenges, not only in ET-PA design itself, but also the requirement for more complex stimulus, bias and measurement techniques. This is a consequence of the fact that an ET system comprises several subsystems; as well as the ET-PA itself, there is envelope generation, the supply modulator and the linearization system. In an ET system, the ET-PA can be considered as a three-port device, with a dynamically controlled drain bias voltage. Therefore, a measurement system for ET requires more complex measurement than fixed bias PAs. Thus, a measurement system is needed to satisfy certain criteria, which will be discussed in detail in the following subsections.

3.2.1 Modulated Signal and Baseband Generation

The ET measurement system is needed to generate a modulated RF signal based on current and future communication and wireless waveform standards, together with associated baseband ET (dynamic bias) signals. The modulated RF waveforms can be generated using commercial software tools such as MATLAB, in the form of I & Q data. The necessary baseband signals can be obtained from I & Q data directly or by detecting the envelope of the RF signal using a simple RF envelope detectors[1].

3.2.2 Shaping Functions

The inherent tradeoff between efficiency and linearity in traditional fixed bias PAs is no longer present in the ET [2]. In addition, there is flexibility in achieving the desired performance of an ET-PA, as efficiency and linearity can be optimised using different shaping functions. The mapping between the instantaneous input power and dynamic supply voltage plays a vital role in the ET approach due to the impact on PA design specifications, which include output power, efficiency, and linearity, particularly AM-AM and AM-PM distortion. Unlike the fixed supply PAs, a lower-level of AM-AM distortion can be obtained in ET despite the nonlinear behavior of the device when operated in compression, if the tracking signal is shaped in a specific manner [3]. Furthermore, the bandwidth requirements of the tracking signal, and hence the requirements of an eventual ET modulator, can also be reduced when using the appropriate envelope shaping function. This results in a modest requirement of bandwidth with only a small degradation in efficiency and linearity [4] – very

important design information. Hence, the ability to precisely adjust the shaping of the baseband tracking signals is needed to optimise the efficiency and linearity of the ET-PA and to explore the design space that results. Thus, the measurement system should support different types of shaping function with a high degree of flexibility. For example, a lookup table (LUT) to enable a shaping function to achieve constant gain (ISOgain) as introduced by the Nujira company in [5] or a detroughing function to keep the tracking signal above the knee voltage, avoiding gain collapse and significant phase distortion.

3.2.3 Synchronization and Time Alignment

Synchronization between different instruments is a major challenge from a test and a characterisation perspective. Essentially, the synchronization between the RF signal generator and the baseband arbitrary waveform generator (AWG) in an envelope tracking system should be achieved with maximum timing accuracy and minimal jitter. Additionally, due to the frequencies of interest, the delay of the RF modulated waveform and the tracking signal must be adjustable with sub-nanosecond accuracy. This is because the modulated RF signal and the tracking signal travel in two different paths, and will both be affected by the delay, which needs to be compensated. However, the required alignment in ET is not as stringent as it is in EER due to the fact that in ET, the amplitude information is always maintained in the RF signal path. Misalignment could be a source of nonlinearity however, as the time deviation between these signals can lead to a significant increase in the EVM and

ACPR [6]. The misalignment between the RF signal and the tracking signal leads to other unintended interactions, resulting in for example asymmetry in ACPR which is symptomatic of an electrical memory effect, as shown in [8]. Generally, the maximum value of efficiency can be expected when an optimum supply voltage amplitude is applied to the PA, which aligns with the RF modulated signal. Otherwise, the tracking voltage will be either higher or lower than this desired value. So in summary, the system must provide for the precise alignment between the modulated RF signal and the tracking signal to an accuracy in order to minimise any degradation in the efficiency or distortion introduced to the PA [1].

3.2.4 Efficiency Measurement

The efficiency measurement is a vital parameter to evaluate the performance of the ET-PA. The efficiency can be defined in several ways, drain efficiency (DE) and power added efficiency (PAE). The drain efficiency is defined as the ratio between the output power of the PA (dissipated at the fundamental load) and the DC power from the DC power supply.

$$DE = \frac{P_{out}}{P_{DC}} \times 100\% \tag{3.2}$$

$$P_{DC} = I_{dd} * V_{dd} \tag{3.3}$$

Where P_{out} is the RF output power and $\boldsymbol{P_{DC}}$ is the dissipated DC power, while I_{dd} & $\boldsymbol{V_{dd}}$ are the drain supply current and voltage respectively. The power added efficiency

(PAE) is a more comprehensive definition of PA efficiency than DE because it takes gain into account. However, realising a dynamic efficiency measurement is one of the challenges in realising the ET measurement system. This is because the measurement of the instantaneous current and voltage supplied to the PA should be taken between the supply modulator and the ET-PA, which can potentially affect the combined performance of the ET-PA. Nevertheless, the practical measurement of the instantaneous current and voltage in an ET-PA can be achieved, as shown in Figure 3.1 , where dedicated probes are used to measure the instantaneous current and voltage supplied and displayed and captured directly using the oscilloscope.

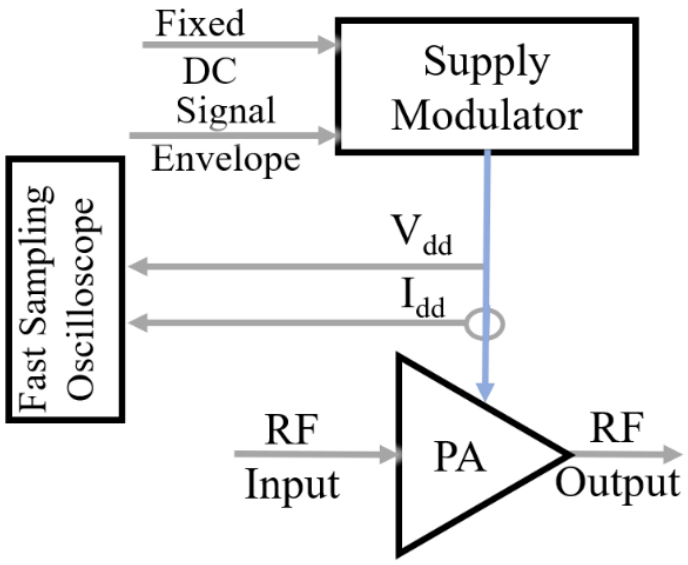

Figure 3.1 The required set-up to measure the instantaneous current and voltage showing voltage a current probe located between the Supply Modulator and the PA

The instantaneous voltage could be probed by a wideband high precision voltage probe. The line impedance of the probe should be high enough to minimise any associated loading [1]. The instantaneous current could be measured using shunt

resistor and probing the voltage drop across this shunt resistor. However, this method is not accurate enough because the shunt resistor, which will be used, should have low resistance value to minimise its effect on the tracking signal to avoid efficiency degradation. Therefore, a current sensor method is proposed to measure the instantaneous drain current. Both voltage and current measurements should be captured with a fast sampling oscilloscope and correlated with the output power to calculate the instantaneous efficiency. The time delay between the measured voltage and current must be calibrated to enhance the accuracy of the measurement.

3.2.5 Digital Pre-Distortion

As an ET-PA is maintained for most of the time near its compression point, the non-linearity that results, generally, must be corrected and usually through using digital pre-distortion (DPD) linearization. Essentially, the DPD linearization technique shares similarities with the mathematical concept to eliminate distortion with a feedforward linearization method [9]. In the pre-distortion method, conversely, the cancellation of distortion is introduced in the input rather than in the output stage by distorting the input signal in a specific manner which is inverse to the PA distortion produced, in order to cancel it [10]. As shown in Figure 3.2, the input signal is passed through a virtual digital pre-distorter circuit, which adds the necessary pre-distortion before amplification. Then, the introduced nonlinear behaviour is corrected through the non-linearity of the output stage. Thus, the measurement system should include customisable DPD, as mentioned previously, in order to linearise the ET using

a memoryless lookup table (LUT) [11] and different memory pre-distortion models [12].

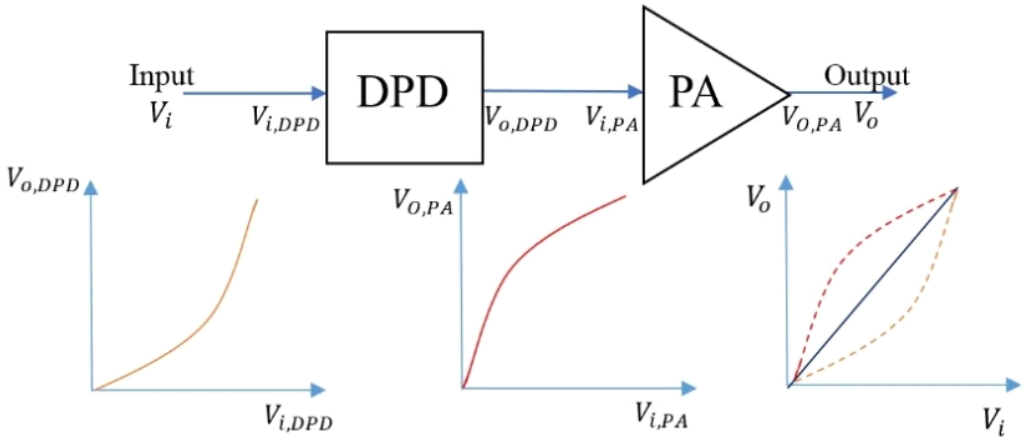

Figure 3.2 Pre-distortion block diagram

3.3 Envelope Tracking Measurement System Arrangement

3.3.1 Hardware Setup

A modulated microwave measurement system from National Instrument (NI) is used as the basis for the advanced ET measurement system, as shown in Figure 3.3. This measurement system is implemented within a NI PXIe chassis equipped with a Vector Signal Transceiver (VST) which is able to support up to 1 GHz signal bandwidth and up to a maximum operating frequency of 6 GHz, itself comprising a vector signal generator (VSG) and a vector signal analyser (VSA). In addition, a dual-channel Arbitrary Wave Generator (AWG) with a bandwidth of 400 MHz, is used to generate the envelope of the RF signal. A two-channel fast oscilloscope with 400 MHz bandwidth is used to monitor the drain current and voltage signals to measure the

efficiency. All these modules are interconnected via the backplane of chassis that is capable of carrying numerous clock and trigger distribution lines.

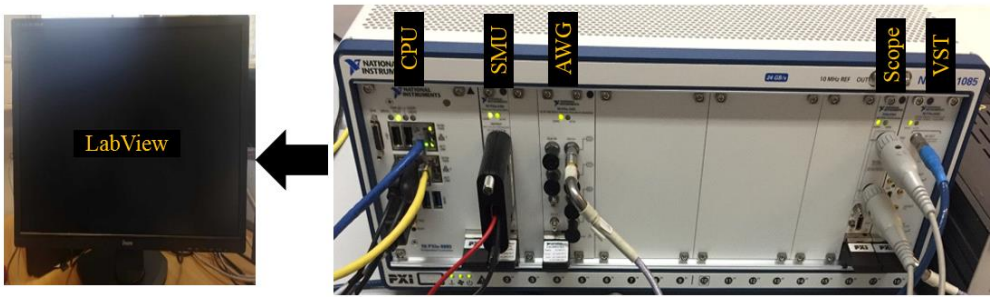

Figure 3.3 ET NI PXIe chassis measurement system

Also, a tight synchronization is achieving using NI's 'T-Clock' capability, which accurately aligns sample clocks and trigger events to allow all devices to start generating simultaneously. As a result, the VST and AWG have a synchronization jitter less than 50 ps which meets the ET measurement requirements for synchronization [13].

3.3.2 Envelope Tracking Software controller

The software which is mainly used to control the measurement system is a National Instruments (NI) software package called RFIC [14]. This software application, which runs on the PC controller in the NI chassis, uses a graphical interface to configure all key hardware. It is also used to fully exploit the hardware capabilities and perform the essential digital signal processing and other tasks needed for ET measurements, including downloading commercial waveforms to the VST, shaping the RF envelope and digital pre-distortion (DPD). Furthermore, the software

is utilised to measure and display the average efficiency, ACPR, AM-AM, AM-PM, with/without DPD measurements. Importantly, the software has the ability to align the RF signal and the tracking signal by applying a digital delay to the RF signal. However, this software application has some limitations and cannot for example be easily customized to do other required measurements. Hence, LabView applications needed to be developed to enable additional measurement capabilities, including instantaneous efficiency, implementing new shaping functions, customising waveforms and time-alignment characterisation.

3.3.3 The Supply Modulator design

Since supply modulator design is out for the scope of this Ph.D. research, a demonstrator linear modulator was designed to characterise the capability of the ET system only. The methodology that was used to design the linear modulator consists of two stages namely gain stage and output stage as displayed in Figure 3.4. The gain stage comprises an inverted voltage Op-Amp which is THS4001 [15] from Texas Instruments to amplify the voltage. While the output stage is used to amplify the current because the maximum current for the gain stage is limited to only 100 mA. The LT1210 Op-Amp [16] which is selected from Linear Technologies is used to amplify the current in the output stage. The values of the resistors were selected to provide the desired voltage gain of 5 V/V.

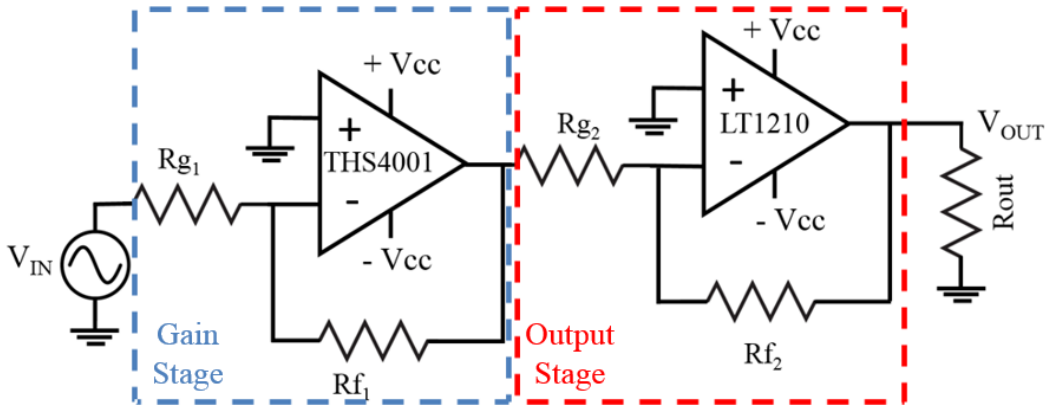

Figure 3.4 Schematic Diagram for the Supply Modulator

The linear modulator was designed and fabricated using FR4 substrate [17]. It was then tested using an envelope generated from a 10 MHz LTE signal, which was produced by the NI Arbitrary Waveform generator. The load of the supply modulator was set to be 50 Ω.

Table 3-1 Measurement of the supply modulator using 50 Ω fixed load

Parameter	Performance
Bandwidth	18 MHz
Maximum Voltage	8.5 V
Maximum Current	170 mA

The input and output voltage signal of the modulator were detected and plotted using 400 MHz oscilloscopes as depicted in Figure 3.5 which shows how close the modulator tracks the envelope of the 10 MHz signal. The output current, output voltage, and 3 dB bandwidth were measured as shown in Table 3-1. Importantly, as has been mentioned above, an optimised supply modulator design is outside the

Ph.D. scope, so this modulator with modest specs was built for demonstration purposes for the ET measurement system.

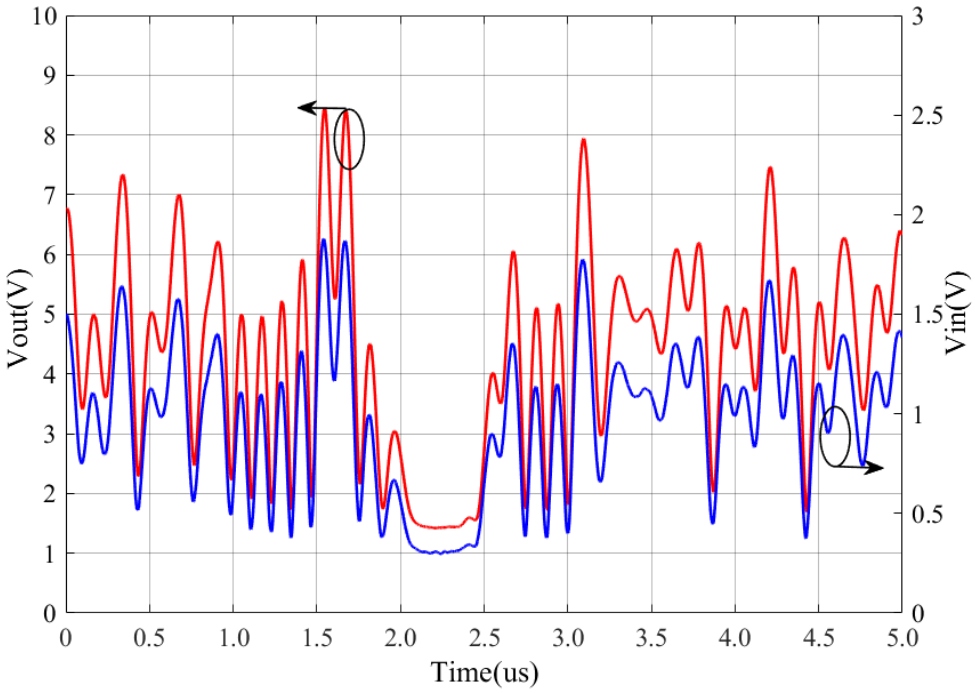

Figure 3.5 The input signal (blue) and the output of the supply modulator (red) using the envelope of a 10MHz LTE signal

3.3.4 Demonstrator PA Design

A 0.35 W GaAs FET(ATF-53189) [18] from Broadcom was chosen to design the test PA, which was then integrated with the supply modulator to characterise the ET system. This device is selected for the following reasons:

- The device offers low drain voltage around 4.5V which is in range of the voltage of the supply modulator used.
- Dealing with a low power device was initially safer for the system being characterised, a good strategy to avoid any damage occurring.

- The cost of the device is low.
- The measurement set up is less complex when compared for example to that needed for a 10 W GaN Device, where a driver amplifier would be required.

In PA design, impedance matching networks are essential in order to maximize the power transfer into and out of a device, to maximise output power and gain. Put another way, the input and output impedances of a device should be matched to 50 Ω to minimise losses due to input and output reflections. Thus, the input matching networks (IMN) and output matching networks (OMN) were designed based on an active load-pull measurement, where the required source impedance was measured to be 27.5+j22 Ω and load impedance is 10.2-j32.5 Ω, at 1.8 GHz. The matching networks were firstly designed using ideal transmission lines and the quarter-wave DC feed. Then, these ideal transmission lines were replaced with lines designed on RT/Duroid® 5880 microstrip, which has a dielectric thickness of 20 mil (508 µm) with a relative permittivity of 2.2 and loss tangent of 0.0004 [19]. The input and output matching over 100 MHz bandwidth from 1.75 GHz to 1.85 GHz is shown on the Smith chart in Figure 3.6.Also, as the device was prone to be unstable at lower frequencies, a 10 Ω resistor was added in series at the gate bias supply point, along with a 10 pF decoupling capacitor. This resistor improves stability by removing the negative resistance that causes the oscillation at lower MHz frequencies. An additional 7 Ω series resistor was added at the input of the device. This resistor is utilised to stabilize the device for all frequencies including those outsides of the operating frequency of

interest. However, the gain of the device is degraded by this resistor. Consequently, a 2 pF capacitor was connected in parallel to this resistor to constrain its contribution to low frequencies. The capacitor effectively by-passes the resistor at higher frequencies, where gain is restored.

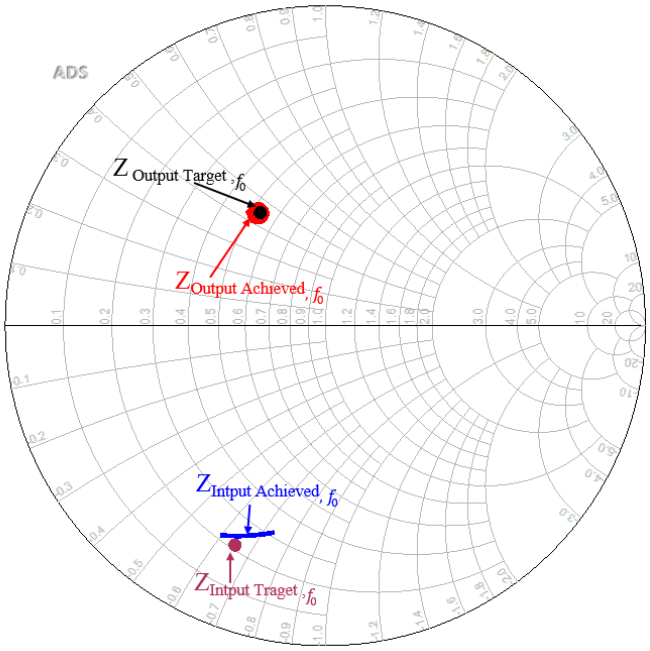

Figure 3.6 The target and achieved input and output matching networks on the Smith chart normalized to 50Ω

The PCB board was fabricated using RT/Duroid® 5880 using microstrip. Then, the GaAs device and all passive components were soldered to the board that contained proper through-plated pin grounding. Finally, the PA was realised as presented in Figure 3.7. To enable drain supply modulation, all bypass capacitors on the drain bias line were removed except the 10 pF RF bypass capacitor [3]. Initially, a small shunt resistor was added allow the drain current to be probed, but it was observed that the accuracy of this method was not sufficient. Thus, the shunt resistor

was replaced with zero-ohm resistance and the drain current measured using an alternative approach with dedicated current sensor, which is discussed in the coming section.

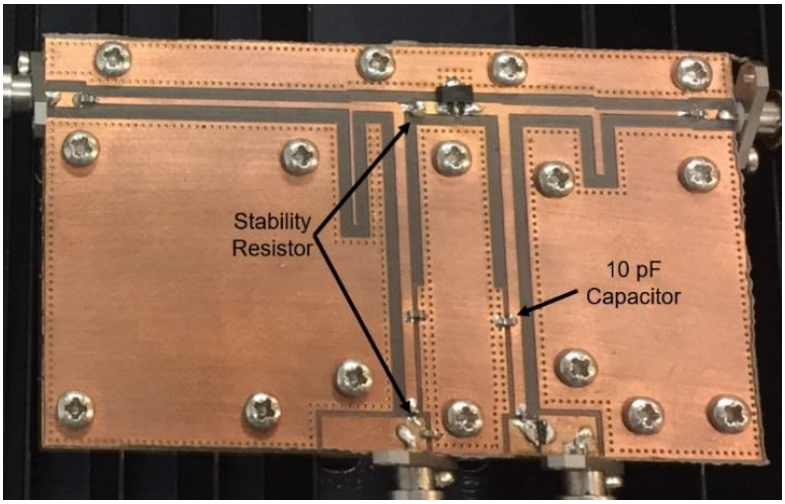

Figure 3.7 The complete and realised 0.35 W E-pHEMT FET (ATF-53189) PA, where all bypass capacitors on the drain bias line were removed except a 10 pF to enable supply modulation

3.3.4.1 Fixed Bias Measurement

As an initial step to predict the performance of the PA, the output power, efficiency and gain performance were measured using a simple CW signal at 1.8 GHz with a fixed drain bias voltage of 4.5 V. The quiescent drain current was chosen to be around 100 mA. The input power was swept from -5 dBm to 15 dBm while the output power, drain efficiency (DE) and gain were measured as depicted in Figure 3.8. The PA delivered a maximum DE of 58 % at an output power of 25.2 dBm for 1 dB compression with a gain of 13.2 dB.

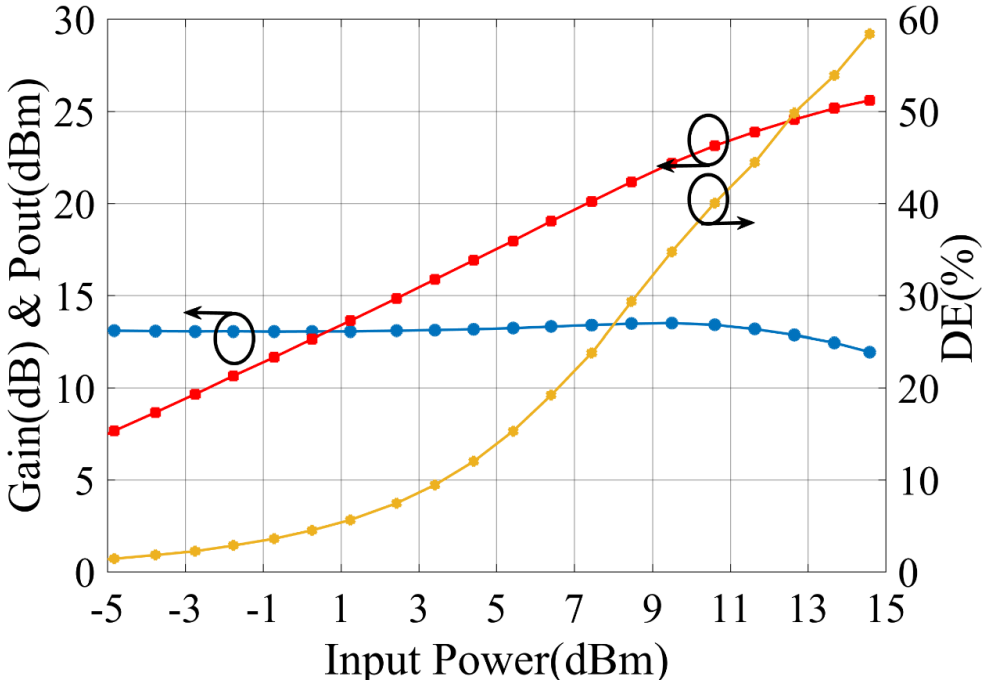

Figure 3.8 The drain efficiency, gain, and output power performance of the PA with fixed 4.5V drain voltage

Since this PA was designed especially for the ET system, where the PA is biased dynamic, the static drain bias voltage was varied from 1.5 V to 4.5 V with 0.5 V step while the drain efficiency and gain of the PA were measured. Figure 3.9 illustrates the DE and gain performance of this PA where the PA maintains high efficiency above 53 % plateau as the drain bias voltage changes from 1.5 V to 4.5 V over a wide range of output power from 25.2 dBm to 18.2 dBm (7 dB OBO). While there is 1 dB variation in the gain from 12.3 dB to 13.02 dB as the gain increase with the increase of the drain bias voltage. Therefore, the PA is good enough to be used for characterisation and demonstration purposes in the ET system.

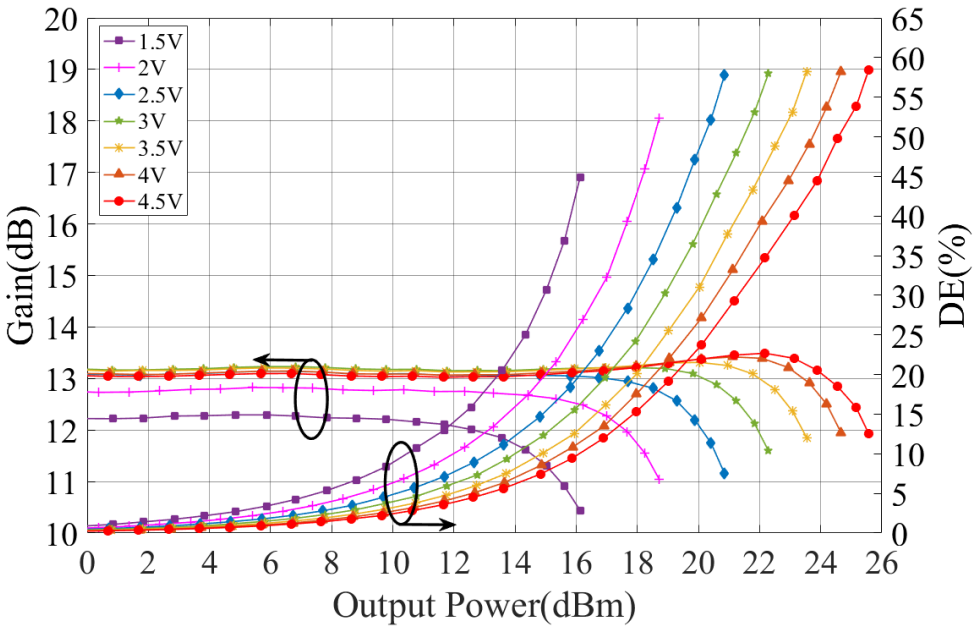

Figure 3.9 PA drain efficiency (DE)and gain performance as the drain voltage changed from 1.5V to 4.5V with 0.5 V step

3.3.5 Current and Voltage Sensor Design

As mentioned above, a current sensor is proposed to measure the instantaneous drain current. The current sensor was built using a MAX9643 [19] differential Op-amp from Maxim with a wide common-mode voltage range and 15 MHz bandwidth. Figure 3.10 illustrates the schematic for the sensor where a 0.1 Ω shunt resistor is placed in the bias feed and delivers a potential difference to the input of the differential Op-amp, which amplifies the voltage suitable for measurement. The output voltage of the differential Op-amp is connected to a fast oscilloscope. LabVIEW was used to calculate the current based on the gain of the differential Op-amp and shunt resistor as follow:

$$\mathrm{V}_{out} = V_A \times V_{(sense)} \tag{3.4}$$

$$I_{sense} = {}^{V_{sense}}/_{R_{sense}} \tag{3.5}$$

V_A is the differential op-amp gain, V_{out} the output voltage of the differential Op-amp, V_{sense} is a voltage drop across the shunt resistor R_{sense}, and I_{sense} is the instantaneous drain current. Also, the instantaneous drain voltage is detected using voltage divider comprising an external resistor of 1k Ω and the internal 50 Ω resistance of the oscilloscope which produces a ratio of ${}^{1}/_{21}$ as presented in [20].

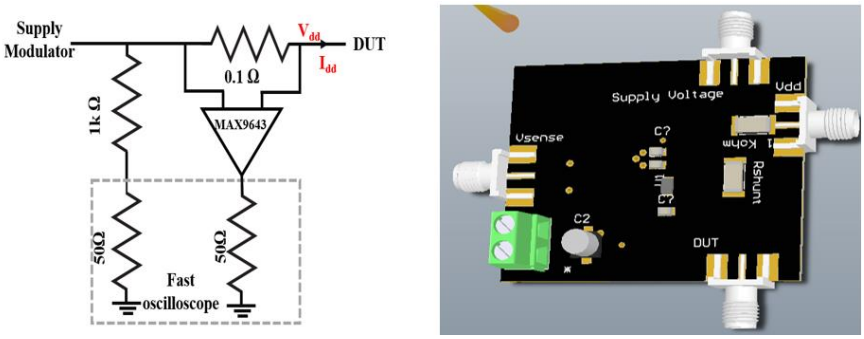

Figure 3.10 Current &voltage sensor circuit schematic and layout

After fabricating the sensor, it was tested with the 0.35 W GaAs PA used as a load. The drain current was measured statically at different supply voltage from 1.5-5 V, using a bench power supply (SMU) and the current sensor as shown in Figure 3.11. The figure demonstrates a good agreement between the SMU measurement and the current sensor measurement which indicates good accuracy.

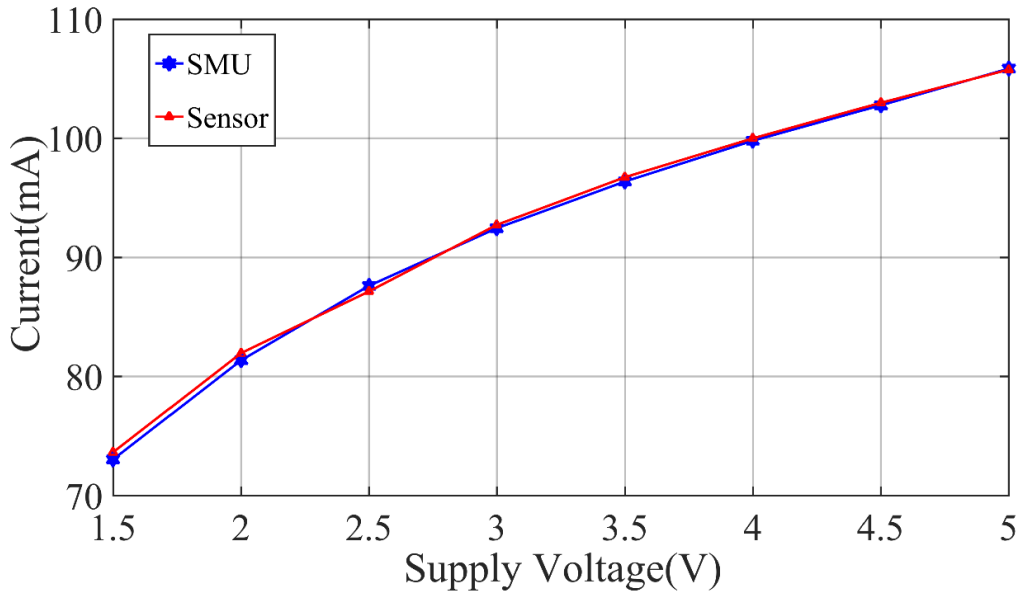

Figure 3.11 The measurement of current using the current sensor and current measured by the supply voltage (SMU)

3.4 Measurement Verification

The PA and supply modulator which are used to verify the ET measurement system are the 0.35 W GaAs FET and the linear amplifier, which were designed and measured previously. The supply modulator was placed as close as possible to the drain of the PA to minimise parasitics, which might impact the tracking signal and degrade performance and the efficiency measurement. The current sensor board was placed between the supply modulator and the PA. The output signal of the board was connected directly to the fast sampling dual channel oscilloscope as shown in Figure 3.12 and Figure 3.13 . As the VSG generated sufficient amplitude, no driver was required, which makes the measurement set-up simpler, and the VSG output could be connected directly to the PA. A circulator, however, was added before the RFPA to

absorb any reflections from the PA which could potentially damage the VSG.

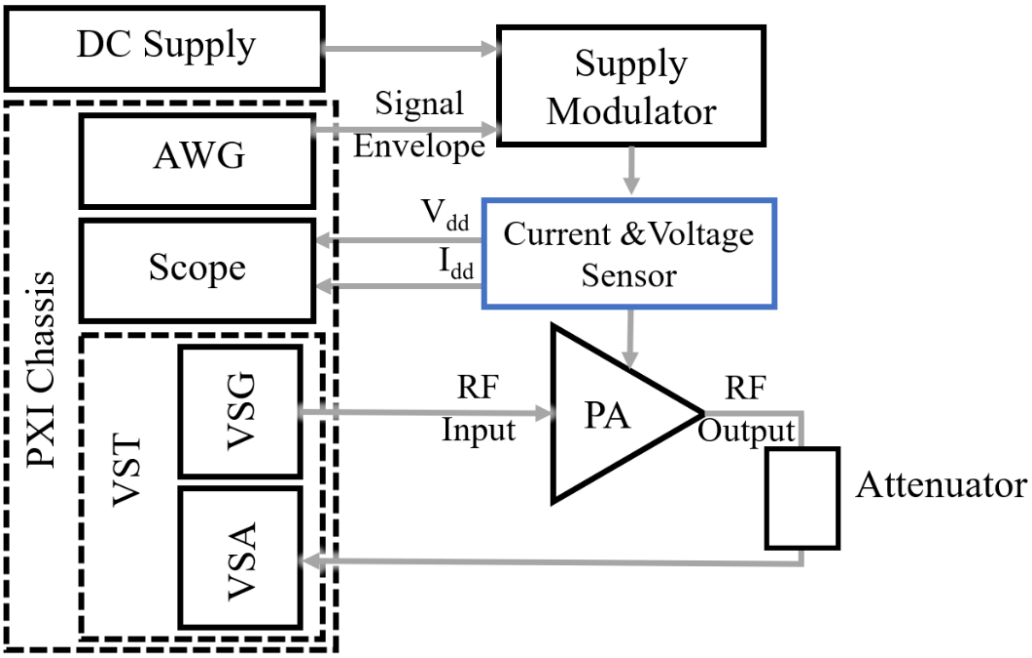

Figure 3.12 Simple representation for typical ET measurement system

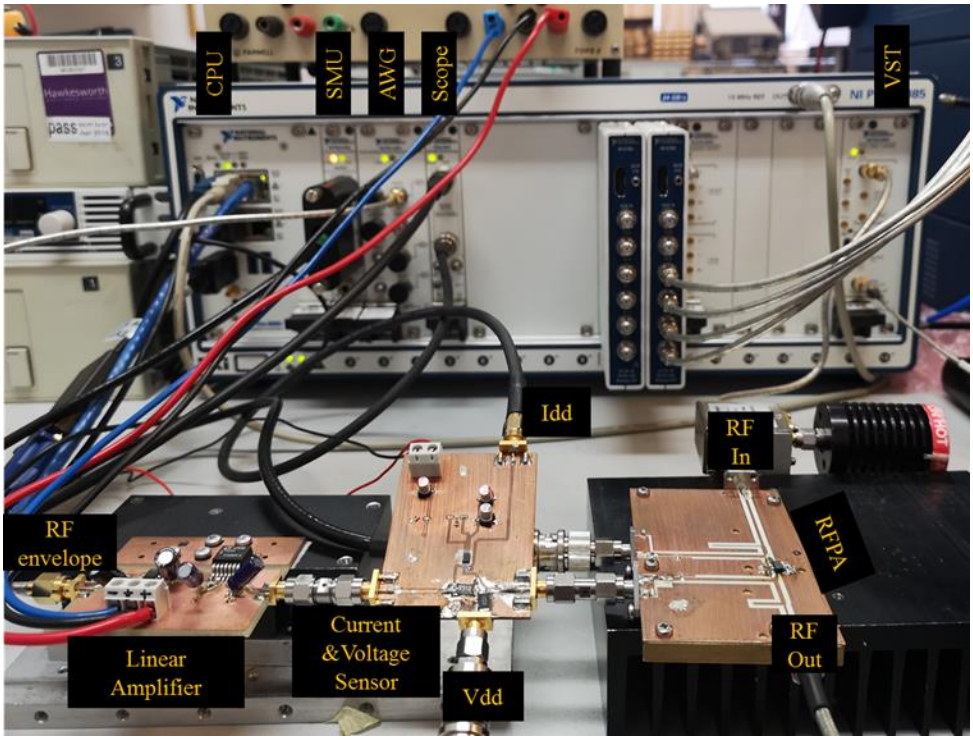

Figure 3.13 Picture of the complete ET measurement test bench

The I & Q components of the input signal were downloaded to the AWG, which was then used to drive the supply modulator. The output signal of the PA was captured by the VSA after attenuating the signal with a 20 dB attenuator, to avoid any possibility of damage to the VSA. The attenuation which was introduced by the circulator, cables and the attenuator at the output was measured, and included in the calibration. Figure 3.13 illustrates the actual ET measurement set-up which is used for all measurements in this chapter.

3.4.1 Input Signal and Baseband

The input signal used to excite the PA is a 10 MHz LTE signal with 6.8 dB PAPR, as illustrated in Figure 3.14, and was downloaded as a TDMS file. The I & Q data was uploaded to the AWG which was then used to drive the supply modulator.

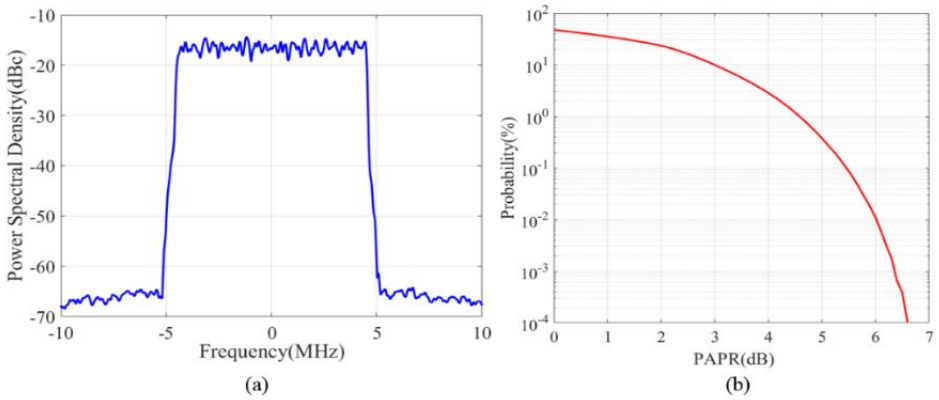

Figure 3.14 (a) Power Spectral Density for 10MHz LTE signal, (b) CCDF for 10 MHz the LTE signal, with PAPR of 6.8 dB measured with the VSA

3.4.2 Shaping Functions

Envelope shaping is an essential function in the ET system, used to modify the linear relationship between the generated tracking signal and RF signal envelope, and to optimise the performance of the PA, for either efficiency or linearity. The system

offers two configurable functions to reshape the envelope including a look-up table (LUT) approach and a de-troughing function. The LUT is defined by the input signal and the desired supply voltage which is specified by the user. The de-troughing function has three different functions which can be selected and configured based on the desired performance. These three different de-troughing functions available are shown in the equations below.

$$f(V) = V + d \cdot e^{(-V/d)} \tag{3.6}$$

$$f(V) = 1 - (1 - d)\cos\left(V \cdot \pi/2\right) \tag{3.7}$$

$$f(V) = d + (1 - d) \cdot V^{a} \tag{3.8}$$

$$d = V_{min}/V_{max} \tag{3.9}$$

Where $f(V)$ is the tracking signal , V is the magnitude of the envelope of the input signal, V_{min} and V_{max} are the minimum and the maximum values for the tracking signal respectively and a is the order of the power de-troughing function. Figure 3.15 demonstrates the normalized drain voltage vs tracking drain voltage for the three de-troughing functions.

Also, different shaping functions can be implemented using LabVIEW MathScript Module [22] which enable users deploy their own code to reshape the envelope. The flow diagram in Figure 3.16 shows the process used to reshape the envelope.

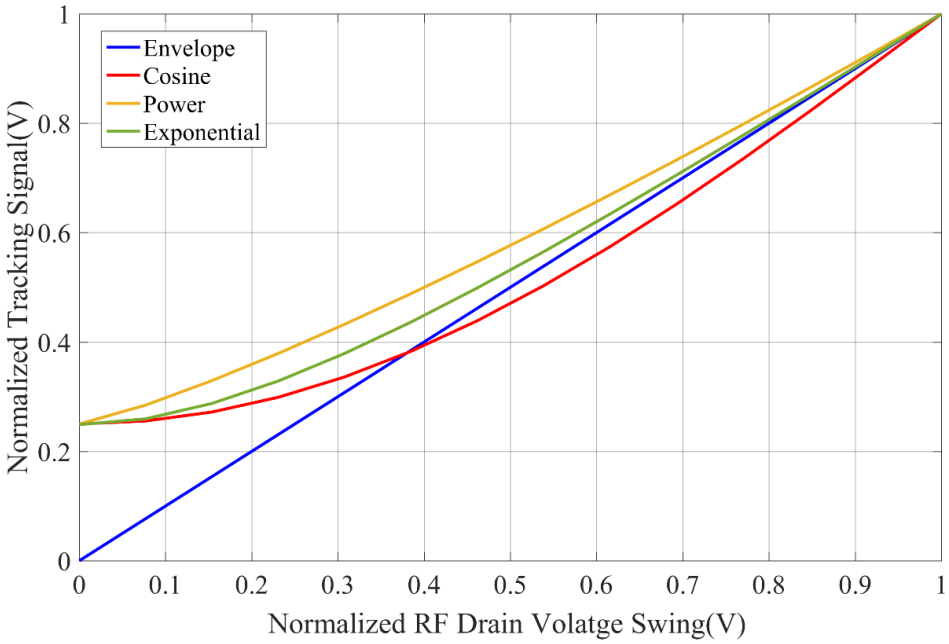

Figure 3.15 Different drain tracking shaping functions

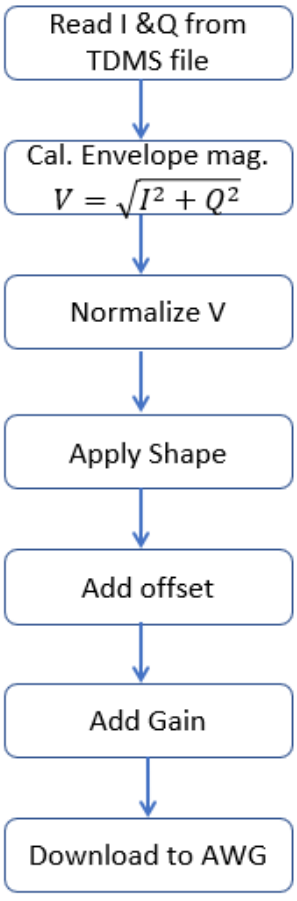

Figure 3.16 The flow diagram to reshape the envelope

For this measurement, the envelope of the 10 MHz LTE signal was extracted and shaped with the de-troughing function which is mentioned above in [3.7]. Figure 3.17 shows the normalized drain voltage and the tracking signal before reshaping the envelope, where the minimum voltage drops to zero. However, the tracking signal was elevated after reshaping the envelope to reach the desired minimum supply voltage. After that, the tracking signal was multiplied by the appropriate gain to reach the maximum desired voltage which, for this PA, was 4.5 V and the minimum voltage was 1.5 V in this case as displayed in Figure 3.18. The sensor board was calibrated by eliminating the time delay differences between the instantaneous current and voltage waveforms which enhances the accuracy of the efficiency measurement.

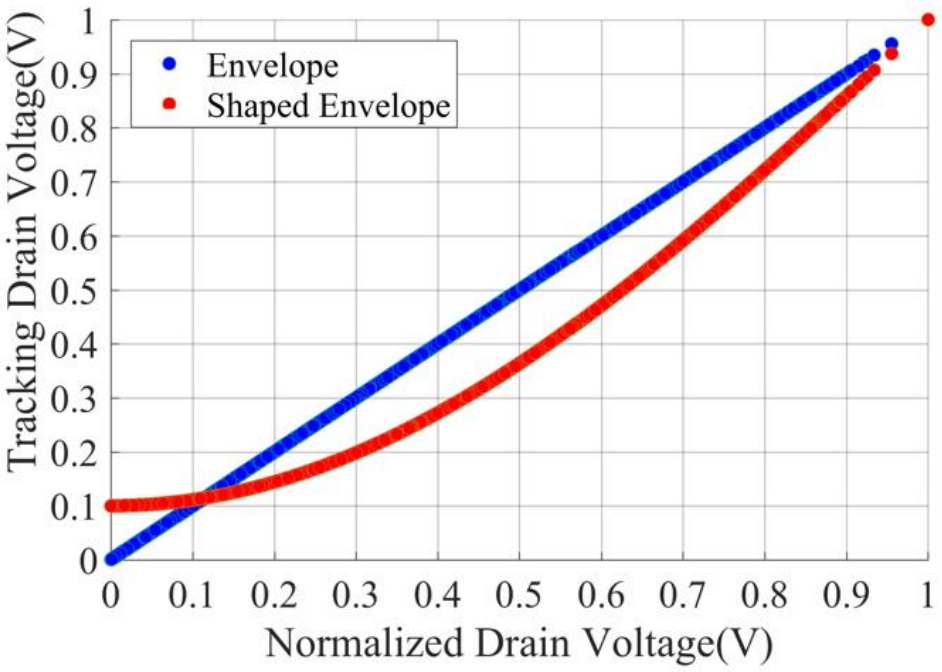

Figure 3.17 De-troughing shaping functions plotted as a function of the envelope of the 10MHz LTE signal (LabVIEW results)

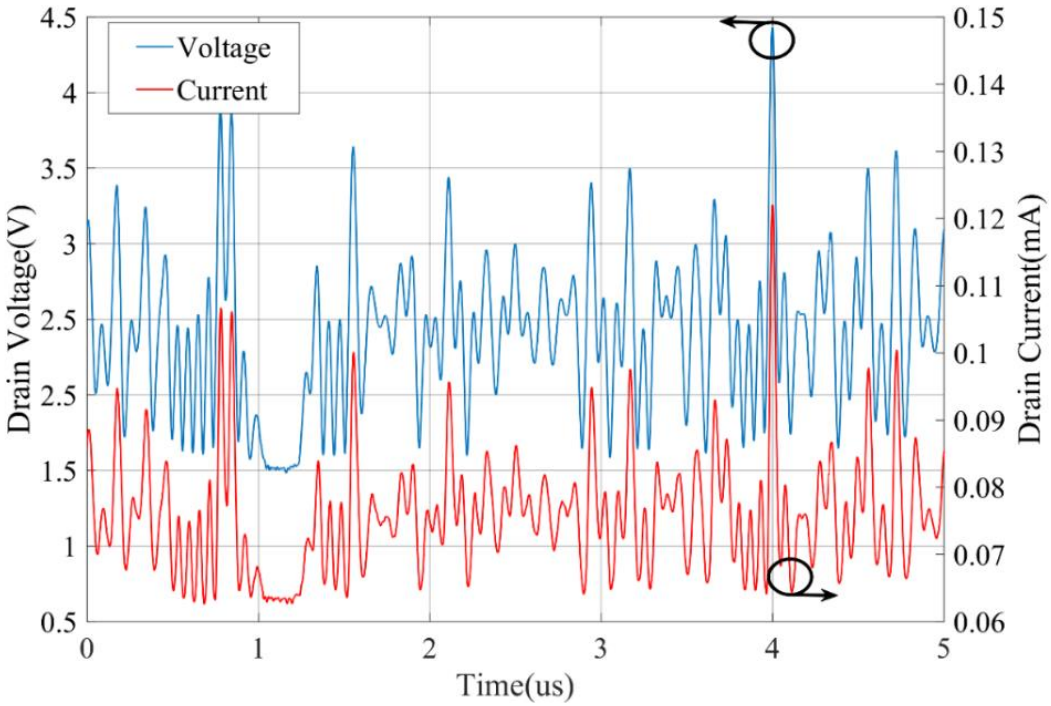

Figure 3.18 High-speed oscilloscope capture of the current waveform (red curve) and drain voltage waveform (blue curve) detected with sensor board

3.4.3 Time Alignment Characterisation

It has been discussed previously that the RF signal and the tracking signal travel in two different paths and they will suffer different time delays, which needs to be compensated. To characterise the alignment between the RF and tracking signals, the centre frequency was temporarily reduced to 400 MHz which is the maximum bandwidth of the oscilloscope. Then, the RF signal and tracking signal (Vdd) were probed with two high-speed voltage probes as shown in Figure 3.19.

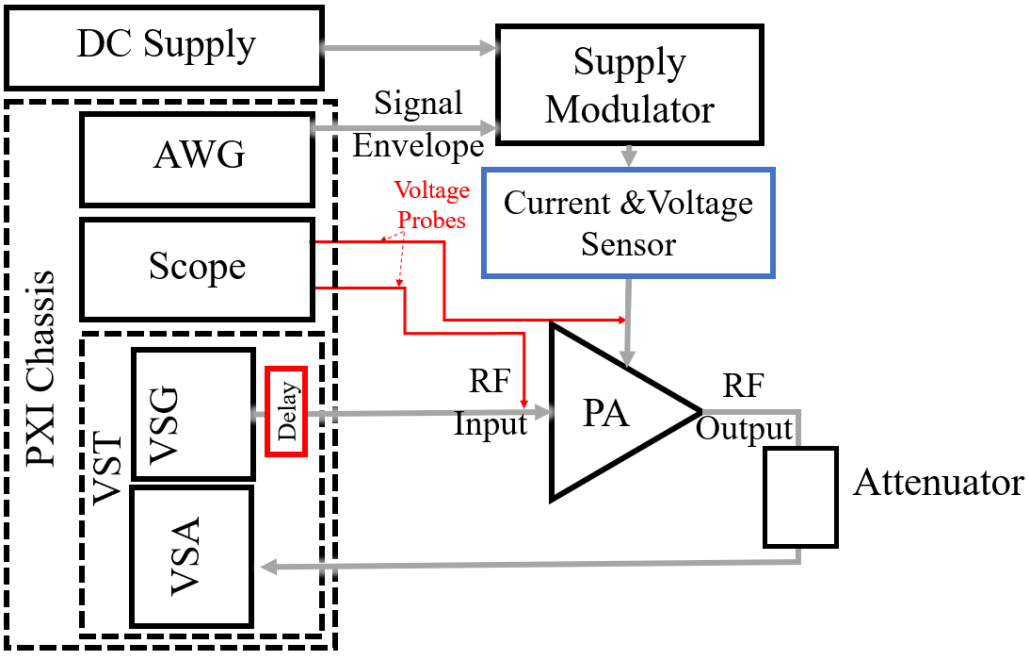

Figure 3.19 Measurement setup to characterise skew between the RF signal and the tracking signal with two voltage probes (red wires)

As illustrated in Figure 3.20, the output signal (RF1) did not align with the tracking signal (Vdd) before applying the delay. Therefore, the delay, which was performed in the digital domain, to the RF signal was swept until both RF signal (RF2) and tracking signal (Vdd) align. Moreover, the measurement of AM-PM distortion, ACLR or EVM as a function of skew between the RF signal and the tracking signal can be used to find the optimum delay [23], [24]. Therefore, a fine alignment was obtained by measuring the AM-PM distortion as an indication of misalignment. After sweeping the delay from 0 to 24 ns with 1 ns steps, the minimum AM-PM distortion occurred when a delay of 12 ns was applied, as shown in Figure 3.21.

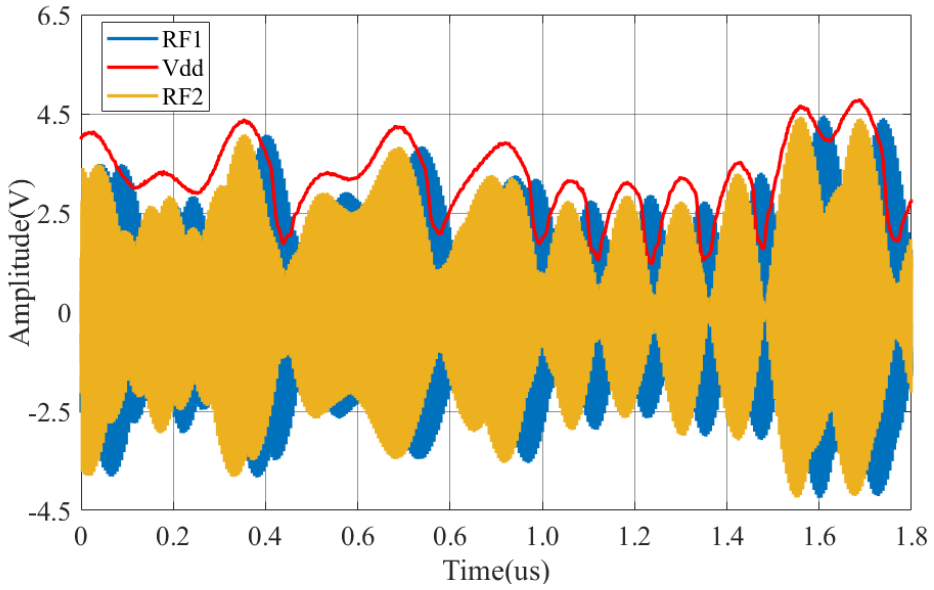

Figure 3.20 The RF signal voltage and the tracking drain voltage (Vdd) for two cases; one without delay adjustment, and the other with delay applied

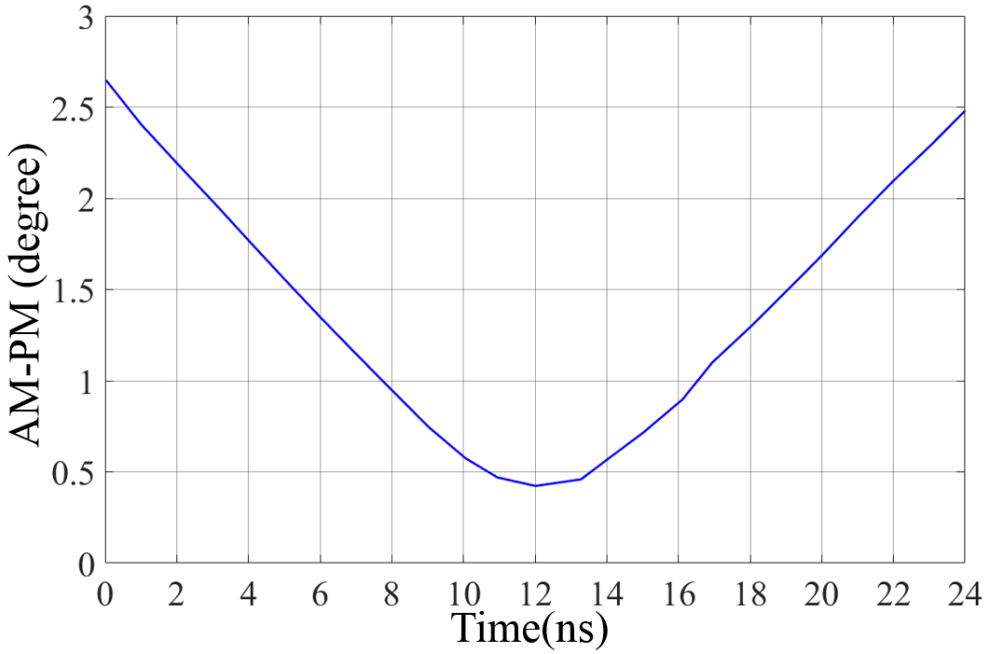

Figure 3.21 The AM-PM distortion as the delay between the RF and envelope is swept over 24ns, where the optimum delay is 12ns

3.4.4 Fixed bias and ET Comparison

After the alignment was achieved, the RFPA was driven up to its 1 dB compression point, with 10 MHz LTE signal at a centre frequency of 1.8 GHz using both 4.5 V fixed and dynamic bias with a minimum voltage of 1.5 V and a maximum voltage of 4.5 V, using the linear modulator which was designed and measured previously. Table 3-2 compares PA performance under fixed bias and ET operation, where the ET increases average drain efficiency from 22.6 % to 43.9 % which is what would be expected from a CW excited, fixed static supply measurement, as shown in Figure 3.9.

Table 3-2 Measured performance for ET and fixed biased with LTE 10 MHz and 6.8 dB PAPR

Input Signal			**Drain Supply**	**Measurement results**				
Freq.	**Mod.BW**	**PAPR**		**Pout**	**Gain**	**DE**	**ACPR**	**EVM**
(GHz)	**(MHz)**	**(dB)**		**(dBm)**	**(dB)**	**(%)**	**(dBc)**	**(%)**
1.8	10	6.8	Fixed	25.1	13.0	22.6	-40.3	2.1
1.8	10	6.8	ET	25.2	12.70	43.9	-38.4	3.6

*The efficiency of the linear modulator is not included in the DE

The linearity performance was also measured. The in-band distortion (EVM) was measured to be 3.6 % for the ET-PA, while for fixed bias, it was measured to be 2.1 %. The out-band distortion (ACPR) was measured to be -38.4 dBc and -40.3 dBc

for ET and fixed bias PA configurations respectively. The ET-PA has 2 dB lower ACPR than fixed bias and has 1.5 % worse EVM, which was expected as the ET-PA has lower linearity performance due to the fact the ET-PA is compressed for most of the time. However, the linearity of the ET-PA might be improved using other shaping functions to optimise linearity such as the Iso-gain shaping function.

3.4.5 The Instantaneous Drain Efficiency Measurement

Generally, the measurement of the average efficiency is useful to evaluate the performance of the ET-PA and to compare it to other techniques. However, the instantaneous efficiency is vital to show the fundamental principle of ET to maintain efficiency over a wide range of OBO. This instantaneous efficiency allows a deeper understand to be developed in terms of how efficiency changes at the rate of the envelope for example, when different shaping functions are applied. Thus, more work needed to be done to be able to robustly measure the instantaneous efficiency because the NI RFIC software measures only the average efficiency. The output power and DC power waveforms are needed to plot the instantaneous DE. The vector signal analyser (VSA) part of the VST measures the output power in the frequency domain, which is then converted into time domain [25]. Meanwhile, an oscilloscope is used to measure the DC components, i.e. current and voltage waveforms directly. However, these RF and DC power measurements lead to misalignment. Also, the two waveforms have a different sample rate. Thus, the output power waveform should be re-sampled in order to align it with the measured DC power.

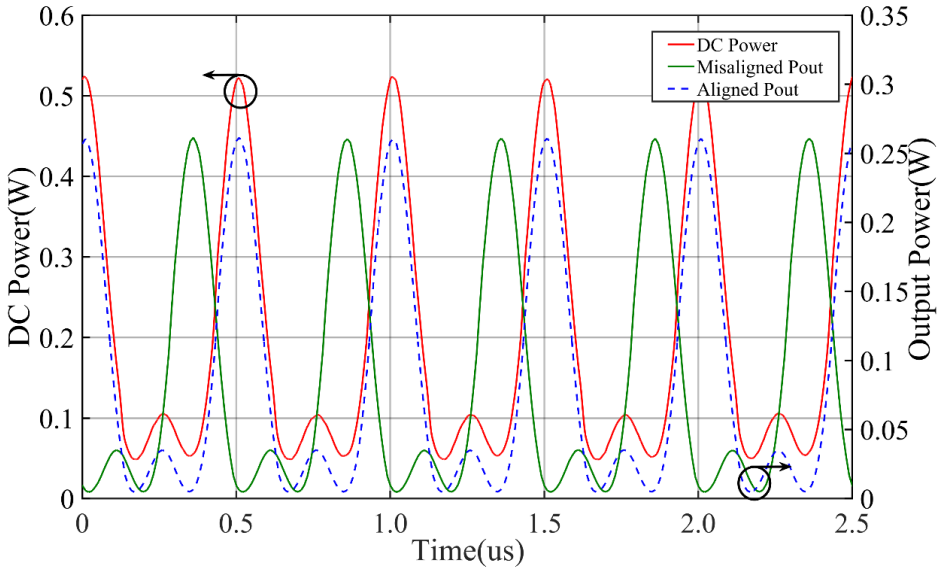

Figure 3.22 The output RF waveform and the DC power waveform before and after aligning them to calculate instantaneous efficiency using a three-tone input

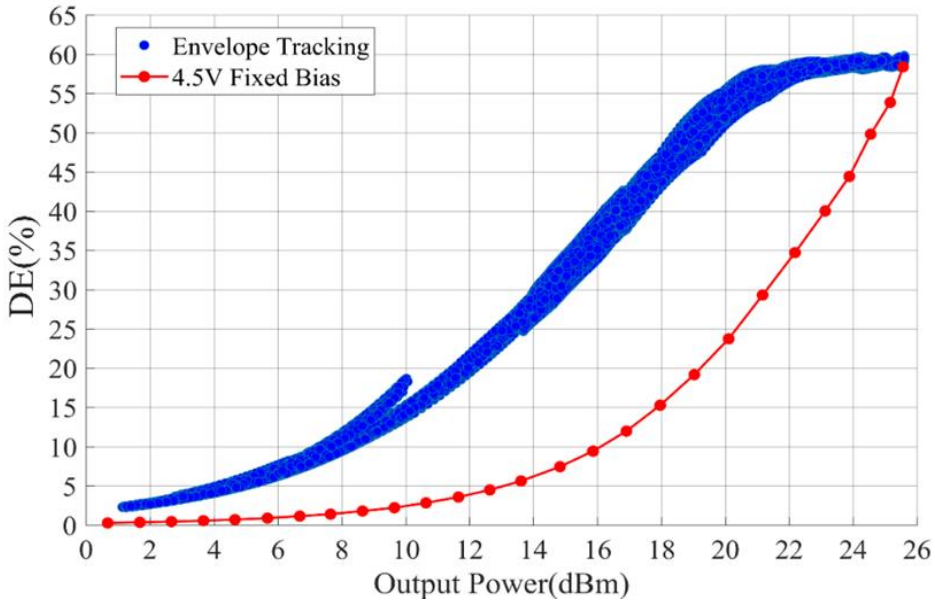

Figure 3.23 Comparing the instantaneous DE for ET and 4.5 V fixed bias for three-tone signal

Figure 3.22 shows output waveform and DC power waveform before and after alignment for a three-tone input signal. Specifically, the measured instantaneous DE under ET and then for a fixed 4.5 V bias can be plotted against output power, as shown

in Figure 3.23. The DE of the PA maintained in a high plateau region, which is above 58 % over 5 dB OBO from 20.2 dBm to 25.2 dBm for a three-tone input signal with 3 MHz bandwidth.

Then, the input signal was changed to a 10 MHz LTE signal with 6.8 PAPR and similar procedures were followed to calculate instantaneous DE, including obtaining waveforms, re-sample and align them. The instantaneous DE with 10 MHz LTE input signal is shown in Figure 3.24. The ET-PA still shows good DE over OBO with more than 50 % over a wide range of output power (4.9 dB) from 20.2 dBm to 25.1 dBm The back off DE with 10 MHz is lower than the three-tone case, which is expected due to the complexity of the 10 MHz waveform and the bandwidth of 10 MHz LTE being greater than the three-tone input signal bandwidth. However, both measurements show nicely how ET-PA can maintain good efficiency over OBO.

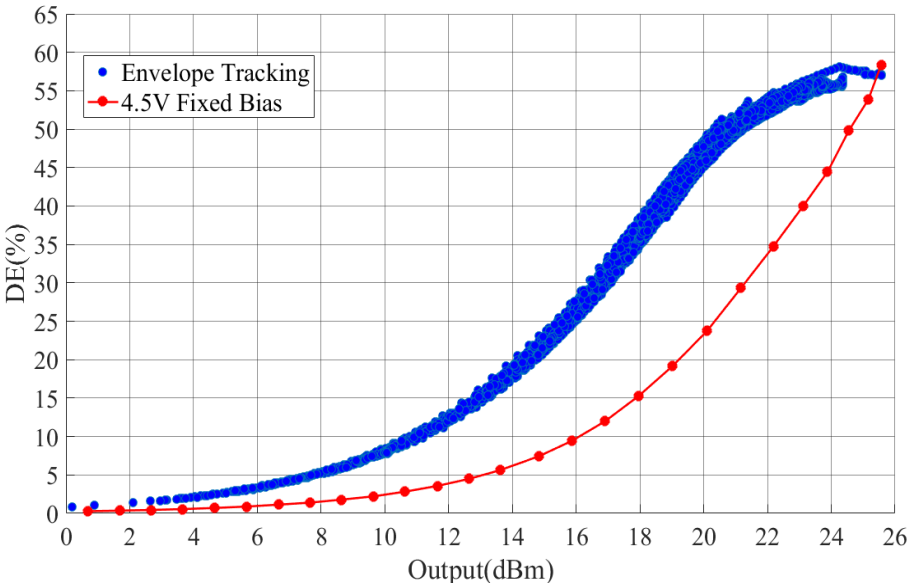

Figure 3.24 Comparing the instantaneous DE for ET and 4.5 V fixed bias using 10MHz LTE signal

3.4.6 Digital Pre-Distortion Measurements

The DPD functionality was used to linearise the output signal by applying a generalised memory polynomial (GMP) [26] with (order=3, memory depth=5). Figure 3.25 illustrates the reduction in the spectral regrowth of the 10 MHz LTE signal after the GMP is applied. The ACPR is improved by around 25 dB from -38 dBc to -63 dBc when the GMP was used, which is predictable from memory DPD model. This is because the GMP can correct for higher degrees of memory effect for both signal and envelope.

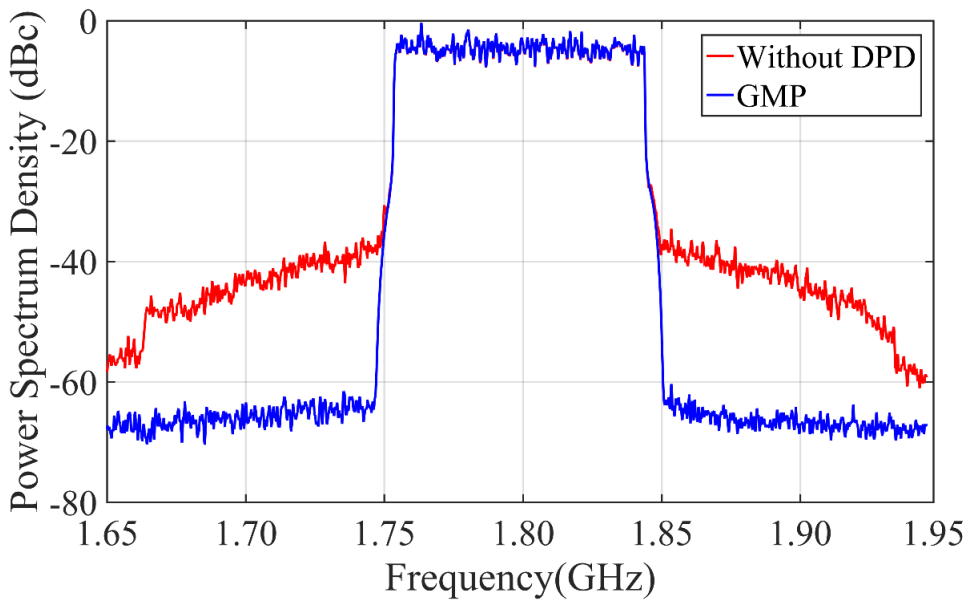

Figure 3.25 Power spectrum density of a 10 MHz LTE signal 6.8-dB PAPR at the output of the PA when GMP algorithms is used

The AM-AM distortion characterisation is used to characterise the gain compression or expansion by describing the relationship between the gain and the input signal at fundamental frequency [27]. Figure 3.26, shows the measurement of AM-AM distortion using the gain as function the input, where there is gain variation

and gain expansion which agrees with Figure 3.9. However, GMP DPD flattens the gain which enhances the linearity performance of the PA. However, when the PA is deeply compressed, the DPD struggled to fix the nonlinearity.

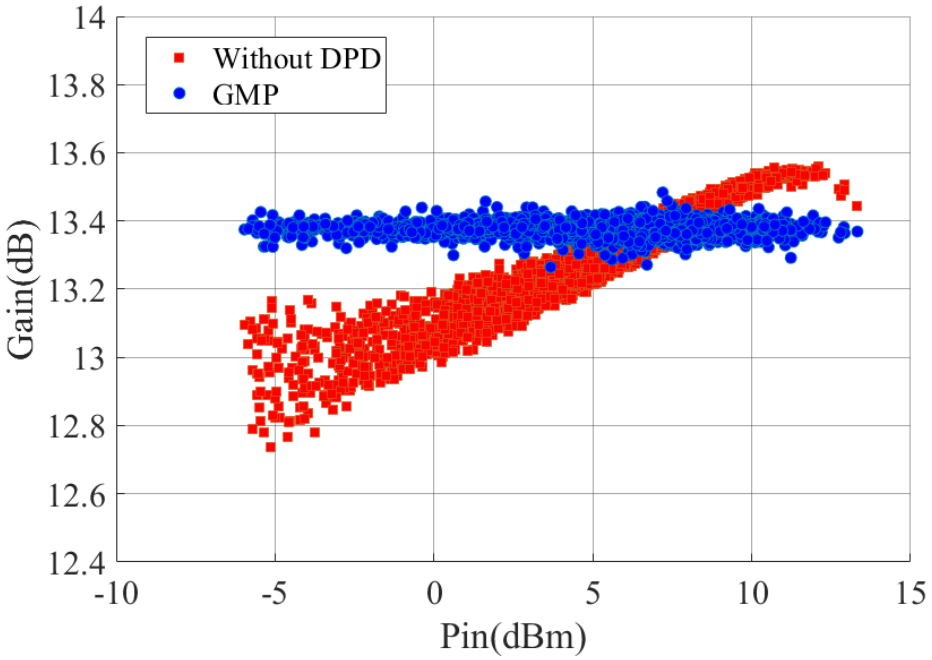

Figure 3.26 AM-AM distortion before DPD where there was variation and expansion in the gain while the DPD flattens the gain

As the amplitude measurement alone isn't sufficient to characterise the nonlinearity of the PA, the AM-PM distortion is used to show the phase variation of the output signal, as the input signal at the fundamental frequency is swept [28]. Figure 3.27 illustrates the AM-PM measurements before and after applying the GMP DPD, where phase variations up to 8° were observed, while after applying DPD, variations dropped to within 1°. The spreading at lower input powers is almost completely down to the envelope delay between input and output modulation envelopes . These AM-AM and AM-PM measurements could potentially be used to

define the shaping function for the tracking signal, which could linearise the PA without the need to apply DPD.

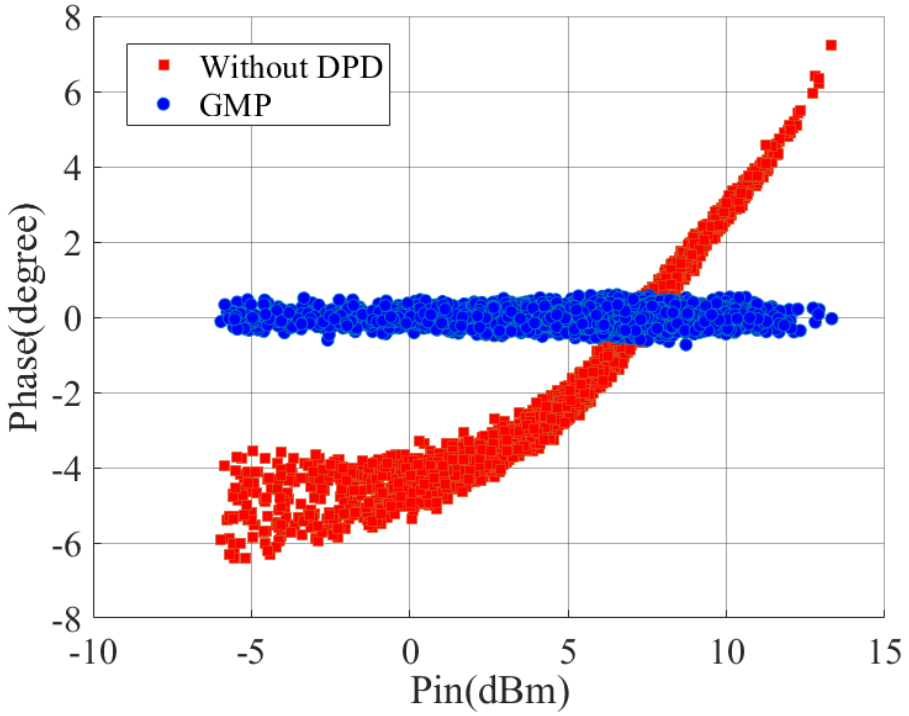

Figure 3.27 AM-PM measurement where memory effects are illustrated by the "spread" of samples at low power level before DPD while DPD fixes it

3.5 Chapter Summary

In this chapter, a full ET measurement system is realised and validated. This involves firstly outlining the important requirements for ET measurement system. Then, a commercial NI PXI system is used as the core for the ET measurement system and is described in detail. This is followed by designing, fabricating and testing the necessary high-frequency and low-frequency circuits i.e. PA, linear amplifier and current and voltage sense board which were integrated around the NI PXI measurement system to realise the ET measurement system. The ET measurement

system was characterised and all the essential requirements for this type of system were validated using 10 MHz LTE signal. The time alignment between the RF signal and the tracking signal is characterised using different methods, including monitoring both RF signal and tracking signal with a high speed oscilloscope and measuring the degradation of the linearity. The average DE of the PA with fixed bias increase from 22.6 % to 43.9 % with 48.5 % improvement. The measurement for the instantaneous efficiency agrees nicely with the measurement for drain efficiency with static measurement when the drain voltage is varied from 0.5 V to 4.5 V. The DE is maintained around 50 % over a 4.9 dB OBO which shows the essential criteria of ET. The digital pre-distortion (DPD) is used to compensate the degradation in the linearity by improving the ACPR by around 25 dB and reduces both AM-AM and AM-PM distortion.

3.6 Reference

[1] Z. Wang, Envelope Tracking Power Amplifiers for Wireless Communications. Artech House, 2014.

[2] D. Kim, D. Kang, J. Choi, J. Kim, Y. Cho and B. Kim, "Optimization for Envelope Shaped Operation of Envelope Tracking Power Amplifier," in IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 7, pp. 1787-1795, July 2011.

[3] M. R. Duffy, G. Lasser, M. Olavsbråten, E. Berry and Z. Popović, "Efficient Multisignal 2–4-GHz Power Amplifier With Power Tracking," in IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 12, pp. 5652-5663, Dec. 2018.

[4] M. Olavsbråten and D. Gecan, "Bandwidth Reduction for Supply Modulated RF PAs Using Power Envelope Tracking," in IEEE Microwave and Wireless Components Letters, vol. 27, no. 4, pp. 374-376, April 2017.

[5] G. Wimpenny, "Understand and characterise envelope-tracking power amplifiers," EDN-Electronic Design News, vol. 57, no. 9, p. 41, 2012.

[6] F. Wang, A. H. Yang, D. F. Kimball, L. E. Larson and P. M. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 4, pp. 1244-1255, April 2005.

[7] D. K. Su and W. J. McFarland, "An IC for linearizing RF power amplifiers using envelope elimination and restoration," in IEEE Journal of Solid-State Circuits, vol. 33, no. 12, pp. 2252-2258, Dec. 1998.

[8] J. Lees et al., "Waveform engineering applied to linear-efficient PA design," 2010 IEEE 11th Annual Wireless and Microwave Technology Conference (WAMICON), Melbourne, FL, 2010, pp. 1-5.

[9] F. Tabatabai and H. S. Al-Raweshidy, "Feedforward Linearization Technique for Reducing Nonlinearity in Semiconductor Optical Amplifier," in Journal of Lightwave Technology, vol. 25, no. 9, pp. 2667-2674, Sept. 2007.

[10] J. Kim and K. Konstantinou, "Digital predistortion of wideband signals based on power amplifier model with memory," in Electronics Letters, vol. 37, no. 23, pp. 1417-1418, 8 Nov. 2001.

[11] J. K. Cavers, "Amplifier linearization using a digital predistorter with fast adaptation and low memory requirements," in IEEE Transactions on Vehicular Technology, vol. 39, no. 4, pp. 374-382, Nov. 1990.

[12] M. O. H. Khalifa, A. Abdelhafiz, A. Kwan, F. M. Ghannouchi and O. Hammi, "Behavioral modeling of envelope tracking power amplifier using Volterra series model and compressed sampling," 2015 IEEE International Wireless Symposium (IWS 2015), Shenzhen, 2015, pp. 1-4.

[13] National Instruments. "National Instruments NI-TClk Technology for Timing and Synchronization of Modular Instruments." http://www.ni.com/tutorial/3675/en/ (accessed 2019).

[14] National Instruments. "NI RFIC 2.5 Test Software." http://www.ni.com/download/rfic-test-software-2.5/7752/en/ (accessed 2017).

[15] Texas Instruments. "THS4001, 270-MHz Voltage-Feedback Amplifier." https://www.ti.com/lit/ds/symlink/ths4001.pdf (accessed 2017).

[16] Analog Devices. "LT1210, 1.1A, 35MHz CurrentFeedback Amplifier." https://www.analog.com/media/en/technical-documentation/data-sheets/lt1210.pdf (accessed 2017).

[17] Farnell. "FR4 Data Sheet." https://www.farnell.com/datasheets/1644697.pdf (accessed 2018).

[18] Farnell. "ATF-53189 Enhancement Mode [1] Pseudomorphic HEMT in SOT 89 Package." http://www.farnell.com/datasheets/1227369.pdf (accessed 2017).

[19] Rogers Corporation. "RT/duroid 5870 /5880High Frequency Laminates." https://rogerscorp.com/-/media/project/rogerscorp/documents/advanced-connectivity-solutions/english/data-sheets/rt-duroid-5870---5880-data-sheet.pdf (accessed 2017).

[20] Maxim Integrated. "MAX9643, 60V High-Speed Precision Current-Sense Amplifier." https://datasheets.maximintegrated.com/en/ds/MAX9643.pdf (accessed 2017).

[21] J. Couvidat, G. P. Gibiino, G. Paillonc y, M. Vanden Bossche, A. Ghiotto and D. Schreurs, "A compact measurement set-up for envelope-tracking RF PAs with calibrated sensing of baseband V/I at the supply terminal," 2015 86th ARFTG Microwave Measurement Conference, Atlanta, GA, 2015, pp. 1-4.

[22] National Instruments. "LabVIEW MathScript Module." http://www.ni.com/en-gb/shop/select/labview-mathscript-module (accessed 2019).

[23] F. Du and H. Yu, "High efficiency test system for envelope tracking Power amplifier," 2017 China Semiconductor Technology International Conference (CSTIC), Shanghai, 2017, pp. 1-3.

[24] E. McCune, Dynamic Power Supply Transmitters: Envelope Tracking, Direct Polar, and Hybrid Combinations. Cambridge University Press, 2015.

[25] National Instruments. "The NI Vector Signal Transceiver Hardware Architecture." http://www.ni.com/product-documentation/14028/en/ (accessed 2018).

[26] D. R. Morgan, Z. Ma, J. Kim, M. G. Zierdt and J. Pastalan, "A Generalized Memory Polynomial Model for Digital Predistortion of RF Power Amplifiers,"

in IEEE Transactions on Signal Processing, vol. 54, no. 10, pp. 3852-3860, Oct. 2006.

[27] J. C. Pedro and N. B. Carvalho, Intermodulation distortion in microwave and wireless circuits. Artech House, 2003.

[28] Keysight Technologies. "Network Analyser Measurements: Filter and Amplifier Examples." http://literature.cdn.keysight.com/litweb/pdf/5965-7710E.pdf (accessed 2019).

Chapter 4

Supply Modulator Ripple Effects and Countermeasures

4.1 Introduction & Motivation

In the previous chapter, a measurement system for the characterisation of envelope tracking (ET) power amplifiers has been realised. The critical characterisation requirements for ET measurements have been identified, discussed and then validated, demonstrating how ET measurement can be carried out precisely.

Even though ET is a strong contender for both base transceiver station (BTS) and user equipment (UE) applications due to its potential to support multimode and multiband operation [1], [2], realising ET in practice presents a number of technical challenges. The difficulty in ET system design and measurement is a consequence of the fact that an ET system comprises several interacting subsystems: the PA, envelope generation, a supply modulator and a linearisation system. The supply modulator plays a vital role as it is a significant contributor to the overall performance of the ET-PA in terms of modulation bandwidth, linearity, and overall efficiency. Despite wide-ranging research focusing on supply modulator design [3]– [5], there are still significant challenges in achieving required performance in terms of modulation bandwidth, efficiency, and output voltage ripple, which limit the application of ET in

commercial systems. Buck-converters are among the most efficient types of supply modulators as discussed in the literature review, but they inherently produce a significant ripple voltage. Filtering this ripple not only causes significant losses, especially through the use of high order filters [6] but also reduces the achievable modulation bandwidth at a given switching frequency.

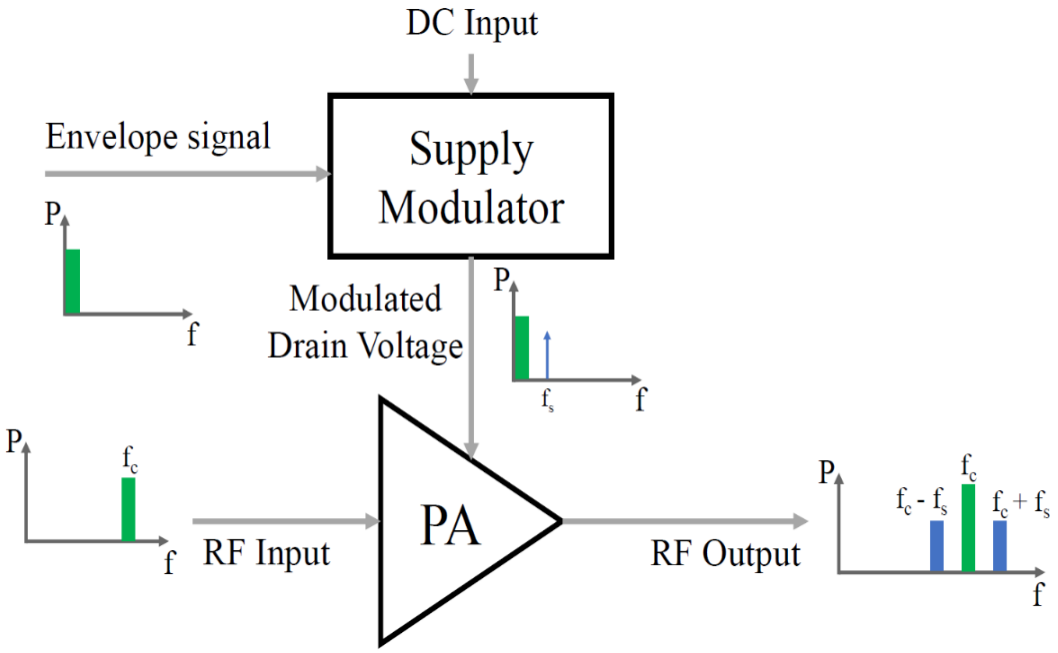

Figure 4.1 Frequency components at different points in an ET system

This chapter presents an experimental investigation into the interaction between a PA and a supply modulator in the presence of voltage ripple introduced by switching noise in the modulator. By varying the ripple magnitude added to the modulated drain voltage of a 10W GaN PA with a 10 MHz LTE signal, the effects of voltage ripple [7]– [9] together with possible countermeasures [10] are explored and the impact of the ripple magnitude on an ET-PA is quantified. The theory behind the

effect of ripple on a PA is introduced and then, the characterisation system used for the study is outlined. This includes the design of a 10 W GaN PA and a wideband high power modulator to accommodate the larger PA. After this, the impact of different magnitudes of ripple on the PA linearity is investigated. The last part of this chapter looks at different ways to linearise ET system, for example, using optimised shaping functions and Digital Per-Distortion (DPD), and their ability to minimise the impact of the ripple are discussed.

4.2 Effect of Voltage Ripple on ET-PAS - Theory

PAs achieve their highest efficiency when the applied drain voltage extends or swings to the lowest practical drain voltage, i.e. 0 V in the case of an ideal transistor, and the knee region in a real device. Using modulated signals with high PAPR, the PA is usually operated under output back off (OBO) conditions, i.e. operating at reduced output power for most of the time in order to maintain good linearity. If the load impedance is fixed, a 6-dB reduction in output power will result in half the usual voltage swing and a significant efficiency reduction. In ET, the PA is maintained in an efficient mode of operation by dynamically changing the supply voltage in response to the modulation, and in the same example of 6 dB OBO, the supply voltage is halved in comparison, thus restoring a maximum voltage swing and maintaining high efficiency. In the case of a real transistor, the function that generates the ET tracking voltage must be carefully designed in order to prevent the device's dynamic load-line from intruding into the knee region, maintaining acceptable linearity [11]. As the

ripple frequencies will be much lower than the RF frequency, the RF load-line can be assumed to be static during one RF period.

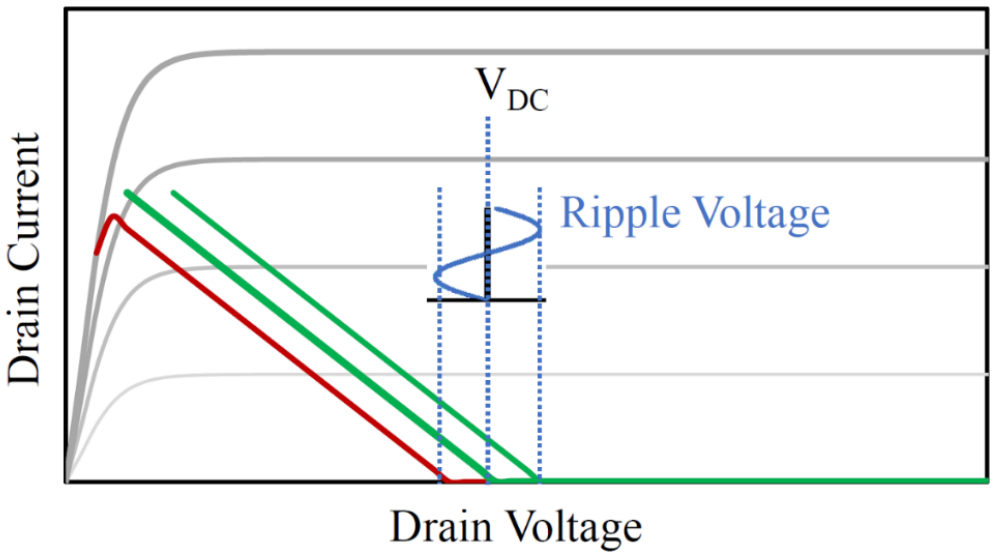

Figure 4.2 Load line of an ideal class B PA effected by ripple voltage

The presence of ripple voltage superimposed onto the modulated supply voltage, however, will have the effect of moving the entire load-line along the drain voltage axis, relative to the static knee voltage, alternating between moving the load line towards the knee region, causing significant distortion and non-linearity, and away from the knee region, improving linearity but reducing the efficiency, as illustrated in Figure 4.2. The increased interaction with the knee region leads to increase non-linear behaviour of the PA, i.e. degradation in the error vector magnitude (EVM) and adjacent channel power ratio (ACPR). In addition to this linearity degradation, there is also a mixing effect that takes place [7], up-converting the ripple to the side-bands around the carrier, with a separation entirely dependent on the ripple and it's the switching frequency. A series analysis, assuming a

memoryless system, delivers a first approximation of this mixing effect, as given in (4.1) [7].

$$V_{out}(V_{in}, V_{ripple}) = a_{10}V_{in} + a_{20}{V_{in}}^2 + a_{30}{V_{in}}^3 + \cdot\cdot$$
$$+a_{11}V_{in}V_{ripple} + a_{21}{V_{in}}^2V_{ripple} + \quad (4.1)$$
$$a_{12}V_{in}{V_{ripple}}^2 + \cdots + a_{01}V_{ripple} + a_{02}{V_{ripple}}^2 +$$
$$a_{03}{V_{ripple}}^3 + \cdots$$

where a_{ij} are the gain terms as a function of the ith order of the input voltage and the jth order of the output ripple, V_{out} is the output voltage, V_{in} and V_{ripple} are the input voltage and output voltage ripple respectively. The first order intermodulation produces is a_{11}.

If the input voltage is given by

$$V_{in} = V_i \cos(\omega_0 t) \quad (4.2)$$

and the output ripple is given by

$$V_{ripple} = V_R \cos(\omega_r t) \quad (4.3)$$

The output ripple generated signal can then be represented as shown in equation (4.4)

$$V_{out}(t) = \frac{1}{2}a_{11}V_iV_R cos\ ((\omega_0 \pm \omega_r)t) \quad (4.4)$$

4.3 Ripple Investigation Measurement Approach

The ET system that was used for the measurements in this chapter is illustrated in Figure 4.3 and Figure 4.4, consisting of a NI ET characterisation system, which was presented in the previous chapter, supplemented with an arbitrary waveform generator (AWG) that generates the synthesized ripple voltage. The ripple and the modulated supply voltage are then combined using a bespoke frequency diplexer consisting of a lumped element low-pass and high-pass filters. A wideband and high-power linear modulator design was used to dynamically bias a 10 W PA.

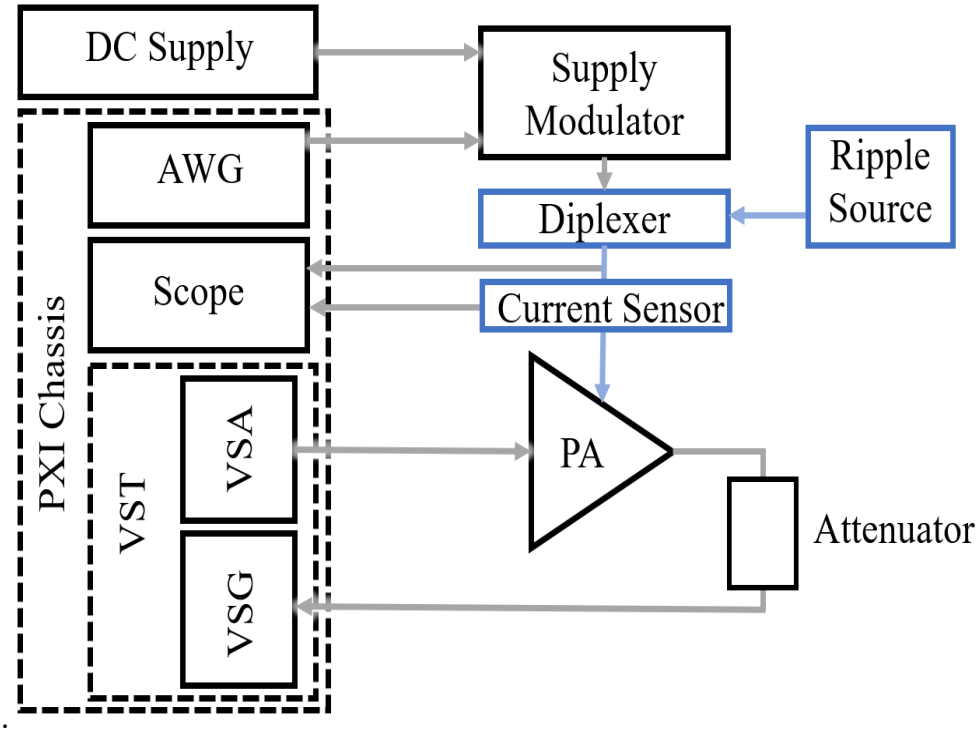

Figure 4.3 Typical ET measurement system with ripple extension

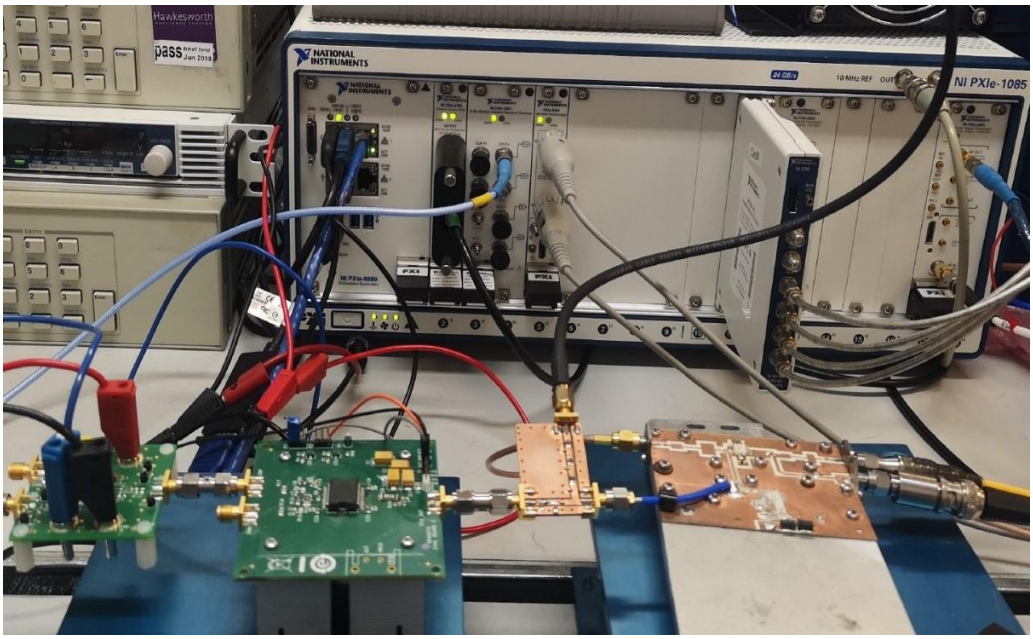

Figure 4.4 Envelope tracking set-up for ripple measurements

4.3.2 Implementing a Wideband Supply Modulator

A two-stage supply modulator was realised using commercially available operational amplifiers as shown in Figure 4.5. The first stage includes THS3001 Op-Amp from Texas Instruments [12] used as voltage amplifier, while the ADA 4870 from Analog Devices [13] was used to amplify the current in the second stage, up to a maximum 1 A. This stage was needed because the maximum current the THS3001 could deliver was limited to 120 mA. The values of feedback and other resistors were chosen to provide the desired voltage gain of 25 dB.

The designed supply modulator was tested using the envelope of a 10 MHz LTE signal, produced by the NI-AWG. A 10 W PA was used as a load. The output current signal was detected using a high-speed current probe [Tektronix TCP312A] while the output voltage signal was detected using a high impedance voltage probe, with

resulting measurements depicted in Figure 4.6.

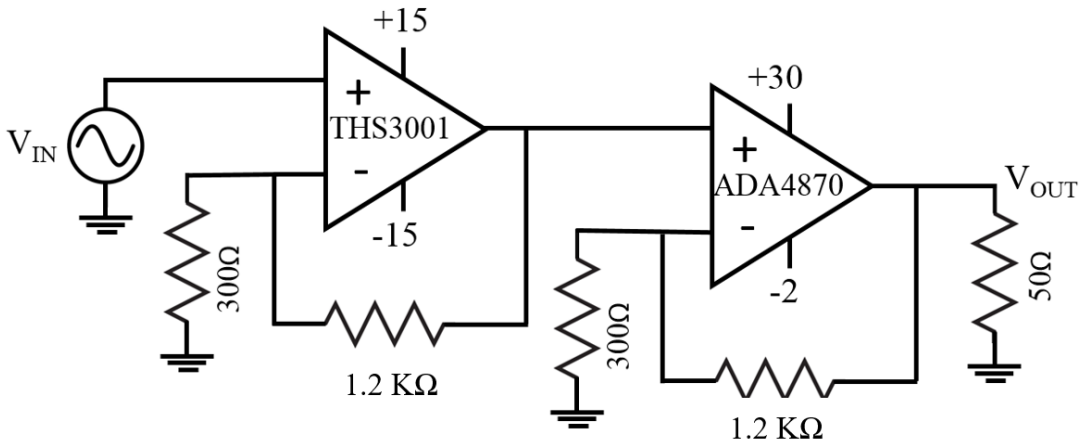

Figure 4.5 Schematic diagram for the 45MHz supply modulator

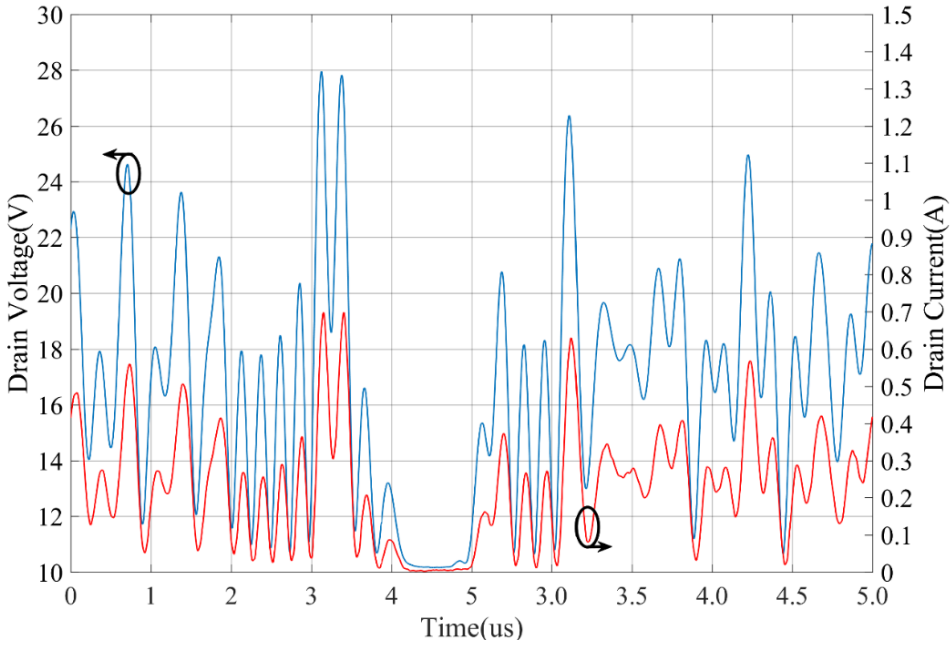

Figure 4.6 The output current and voltage waveforms of the supply modulator with 10MHz LTE envelope input signal

The bandwidth of the supply modulator was characterised by measuring the gain while the frequency of CW input signal was swept from 100 kHz to 100 MHz and is shown in Figure 4.7. The 3 dB bandwidth, maximum output current, and maximum output voltage are listed in Table 4-1.

Table 4-1 The measurement of supply modulator using 10W PA as a load

Parameter	Performance
Bandwidth	45 MHz
Maximum Voltage	28 V
Maximum Current	1 A

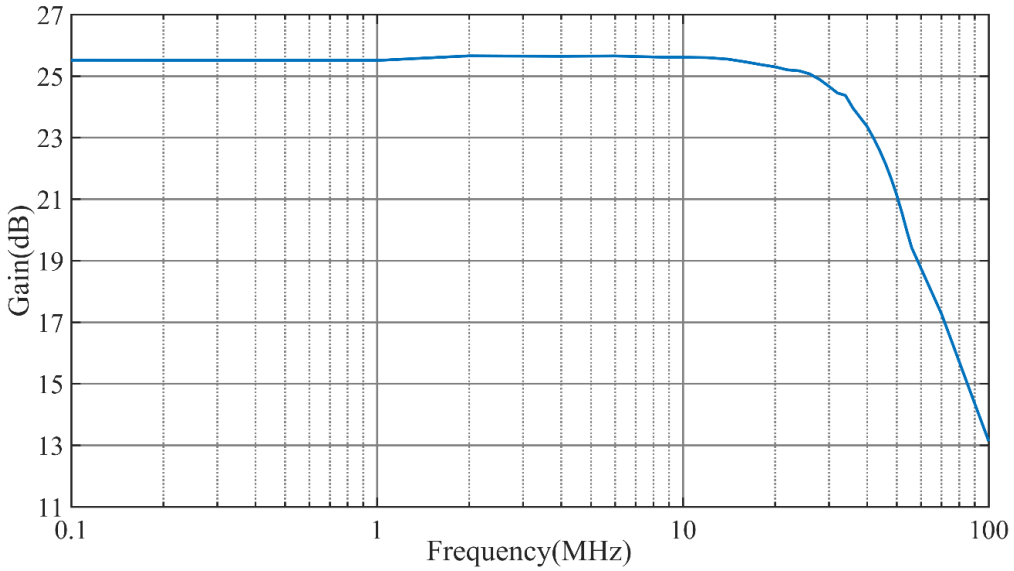

Figure 4.7 Measured frequency response for the supply modulator where the 3dB bandwidth is around 45MHz

4.3.1 RF Power Amplifier Design

A CGH40010F Wolfspeed 10 W GaN HEMT device [14] was used to design a representative PA to test a Manchester University supplied DC-DC converter, capable of supplying a maximum supply voltage of 22 V. Thus, the drain voltage for this PA was limited to 22 V. Since this PA was designed specifically for the ET system where PA is biased dynamically, the PA was initially measured using a simple CW

signal around 2.14 GHz with a quiescent drain current around 100 mA. The drain bias voltage was varied from 8 V to 22 V in 2 V steps while the PAE and gain of the PA was measured. Figure 4.8 demonstrates the PAE and gain performance of this PA, which maintains a high efficiency plateau above 50% as the drain bias voltage changes from 8 to 22 V, over a wide range of OBO from 32 dBm to 38 dBm (6dB OBO). There is a 5 dB variation in the gain observed from 13 dB to 8 dB where gain increases as drain bias voltage increases. This gain variation is a property of the GaN device used and is problematic because it introduces AM-AM distortion and will degrade power added efficiency (PAE) when at lower supply voltages. However, it is clear from Figure 4.8 that the PA offers sufficiently good performance to be used as a demonstrator for the system and operated in an ET mode.

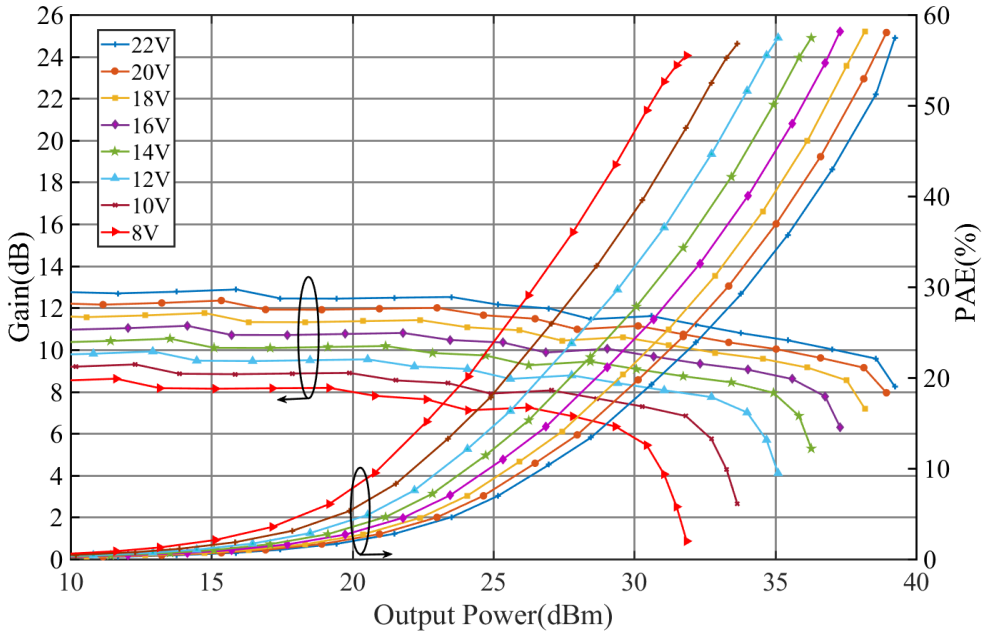

Figure 4.8 PA Power Added Efficiency and Gain performance as the drain voltage changed from 8V to 22V with 2V step using CW signal

4.4 Ripple Investigations - Measurement

In this measurement arrangement, a 10 MHz LTE signal with a PAPR of 6.8 dB was used as the RF modulation for all measurements. The envelope of the modulated signal was extracted from the I & Q data in the NI system and shaped with the de-troughing shaping function (4.5) [15] to yield the desired tracking signal:

$$f(V) = 1 - (1 - d)\cos\left(V \cdot {}^{\pi}/_{2}\right) \tag{4.5}$$

Where $f(V)$ is the tracking signal, V is the magnitude of the envelope of the input signal and V_{min} and V_{max} are the minimum and the maximum values for the tracking signal respectively. The modulated drain voltage was time-aligned with the RF signal using the built-in delay optimiser and verified using the two-channel oscilloscope as displayed in the previous chapter. For this PA, the minimum drain bias voltage was kept above the knee, at a voltage of approximately 8 V. As the PA was designed as a test vehicle for a Manchester modulator, maximum supply voltage was set to 22 V, as previously stated. The PA was driven to its 1 dB compression point at peak envelope power (PEP). The ripple frequency of 41 MHz was chosen such that the ripple-induced sidebands remain within the system measurable frequency range around the carrier, but not too close to the PA's third and fifth-order intermodulation side-bands. Although the switching frequency used in a real ET system would be significantly higher for a 10 MHz modulation signal, the non-linear behaviour induced by the 41 MHz ripple is considered sufficiently representative. The external ripple was

then combined with the drain bias voltage with a voltage amplitude increasing from 0.44 V to 2.2 V. The ripple voltage amplitude is normalized to the maximum voltage which was 22 V. This results in a normalized ripple magnitude, $\hat{v}_r$, ranging between 0.02 and 0.1 as shown in Figure 4.9.

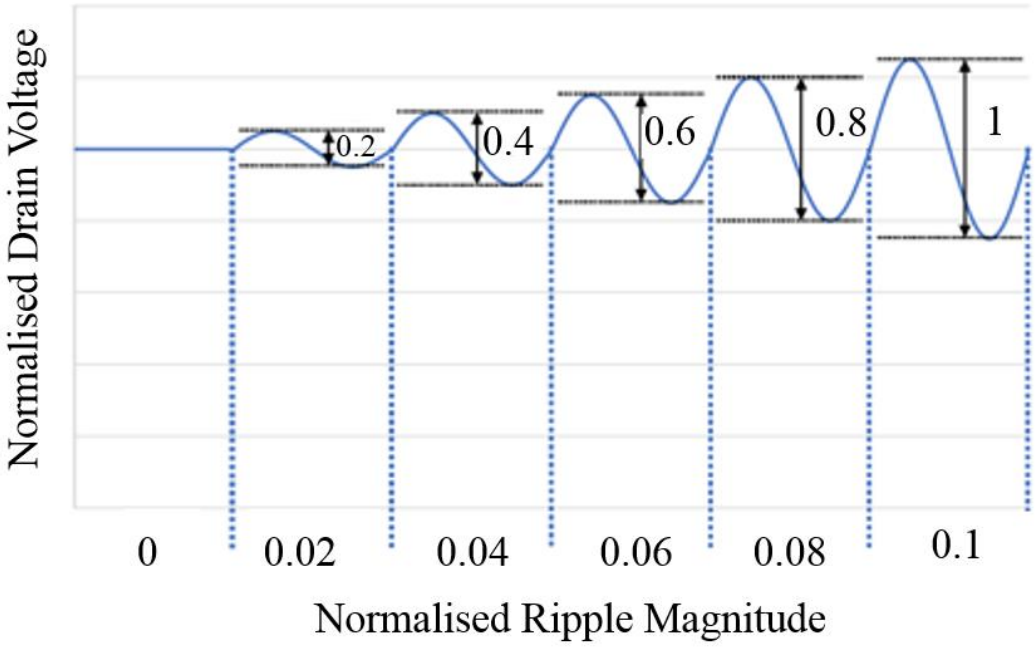

Figure 4.9 Definition of the voltage normalization where the ripple voltage amplitude is normalized 22 V

The linearity performance of the PA is determined by measuring the in-band and the out-of-band distortion in terms of EVM and ACPR, respectively. Figure 4.10 shows that the measured EVM without ripple is 5.7 % which increased to 9.6 % for a normalized ripple voltage $\hat{v}_r$ = 0.1. The ACPR also suffers from increased ripple, increasing from -33.1 dBc with no injected ripple to -26.5 dBc when the normalized ripple amplitude reaches 0.1.

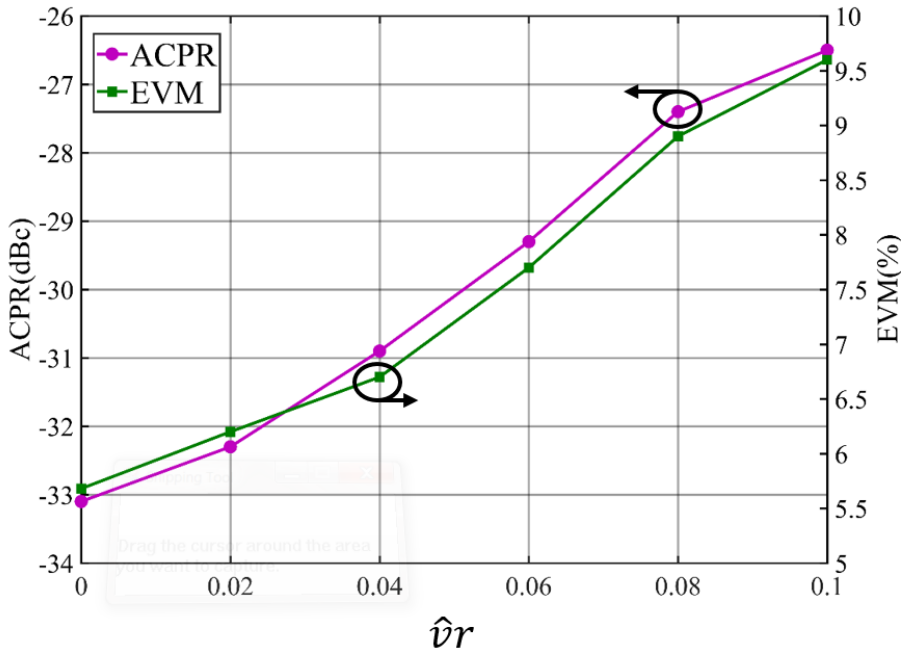

Figure 4.10 Measured EVM and ACPR versus normalized ripple magnitude at a constant PEP and with no DPD

Figure 4.11 shows the measurements of the output spectra of the PA with and without added ripple and illustrates the degraded linearity through ACPR measurements. The main observation in this plot is the ripple induced sidebands. As expected, there are two additional side-lobes separated from the carrier by the ripple frequency of 41 MHz, which is consistent with (4.4) .This leads to two bands with a bandwidth of three times the modulation bandwidth each, separated from the carrier by the ripple frequency. In this experiment, the injected ripple was sinusoidal and thus contained only one frequency component. Depending on the modulator topology and filter employed, the ripple voltage may well have other shapes, e.g. triangular [10], which contain higher harmonic frequencies of the switching frequency, so additional side lobes at those higher harmonics should be expected to appear.

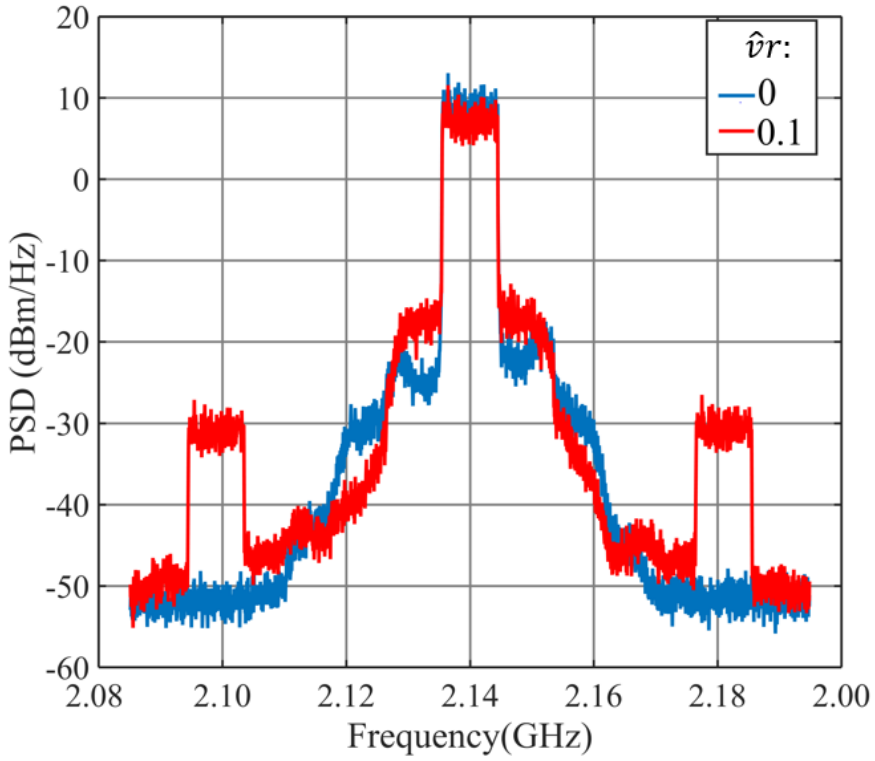

Figure 4.11 Measured power spectral density at the PA output with (normalised ripple magnitude of $\hat{v}_r$=0.1) and without added ripple

4.5 Reducing the Impact of Switching Ripple

The two most common ways of linearizing ET-PAs are DPD and the use of optimised shaping functions [1], [2]. In this section, the usefulness of those two approaches to reduce the ripple-induced non-linear behaviour is discussed.

4.5.1 Applying Digital Pre-distortion Linearisation

As digital pre-distortion (DPD) is already a present in most modern transmission systems, it could be argued that dealing with this new distortion along with the existing distortions generated through the 'normal' non-linearities of a PA, is not a problem as most of the non-linearity can be reduced at the same time. In fact,

measurements show that applying a generalised memory polynomial (GMP) type of DPD, the in-band linearity can be recovered, albeit not to the non-ripple levels as shown in Figure 4.12.

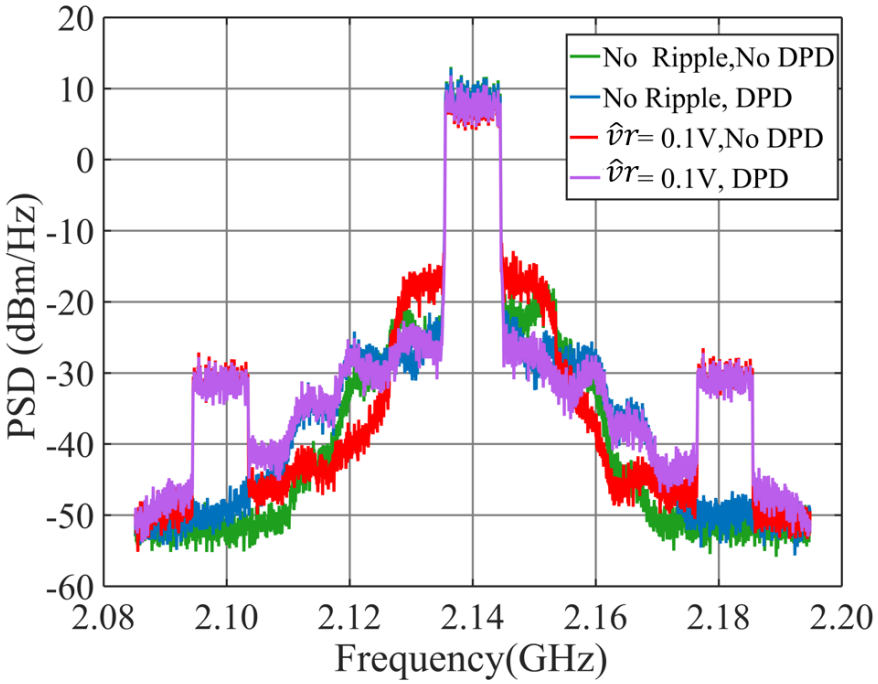

Figure 4.12 Measured PSD at the PA output for cases with and without a ripple and with and without DPD

For a normalized ripple voltage $\hat{v}r$ = 0.1, the EVM is measured to drop from 9.6 % to 3.7 % and the ACPR improves by 7.5 dB from -26.5 dBc to -34.1 dBc when DPD was applied, as shown in Table 4-2. The real limitation of this type of DPD, however, is its inability to correct the out-of-band distortion, with the ripple-induced side lobes remaining unchanged after DPD. In fact, applying DPD introduces additional spurious signals as it tries to correct this non-linearity. As in this case, and typically in practice, the ripple signal is not correlated with the envelope of the RF signal, the relative behaviour constantly changes and as a result, the impact this has

on the PA's AM-AM and AM-PM characteristics cannot be easily predicted by the DPD. This non-coherence of signals also means that any attempt to pre-distort the 'memory-type' effects that result will be unsuccessful, an observation extending from previous work [10].

Table 4-2 Measured linearity at the PA output for cases with and without a ripple and with and without DPD

$\hat{v}_r$	DPD	EVM	$ACPR_{high}$	$ACPR_{low}$
0	No	5.7 %	-33.1 dBc	-30.8 dBc
0	GMP	2.3 %	-39.0 dBc	-38.5 dBc
0.1	No	9.6 %	-26.5 dBc	-25.8 dBc
0.1	GMP	3.7 %	-34.1 dBc	-35.5dBc

4.5.2 Modifying Shaping Function for optimum performance

An alternative approach to recovering or at least improving PA linearity is by modifying the shaping functions used to generate the ET dynamic supply signal. As illustrated in Figure 4.2, the dynamic load line at Peak envelope power (PEP) is 'dropped' into the knee region by the excursions of the ripple voltage. Theoretically, this knee region interaction can be prevented by simply adjusting the supply voltage to shift the area of interaction away from the knee voltage, shown as a black dotted line in Figure 4.13 , and moving the ripple voltage with it, as represented by the dark green trace, again in Figure 4.13. By doing so, in this case, the drain voltage will never reduce to the point where significant knee-interaction takes place. This shift in supply

voltage comes at the cost of average efficiency however, as the mean drain voltage is now increased.

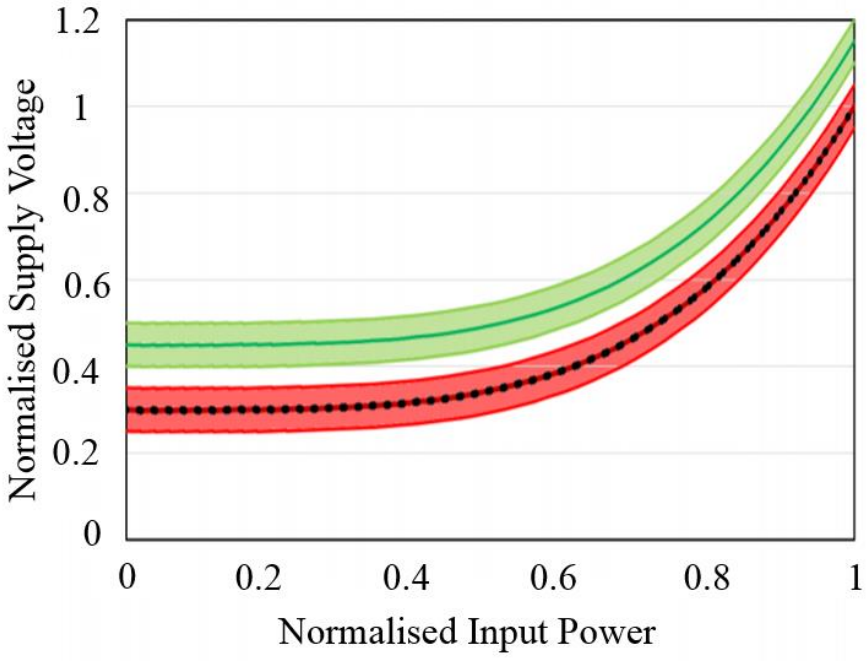

Figure 4.13 Diagram showing the minimum voltage required to maintain the PA load-line out of the knee region (black, dotted), the unmodified shaping function (dark red, the red area highlights the voltage range covered by the ripple) and a shifted shaping function (dark green, the green area highlights the voltage range covered by the ripple)

From measurements, the shift in supply voltage can be seen to significantly improve the raw in-band linearity and reducing the PAE, as expected. The EVM at $\hat{v}r$=0.1 is 9.6 % before shifting the DC and reduces to 5.5 % when the envelope shifted by 3 V and the ACPR improves by 7.5 dB from -26.4 dBc to -33.9 dBc as listed in Table 4-3. For the same DC shift, the PAE drops from 35.3 % to 31.7 %. Even small levels of DC voltage shift lead to significant improvements in EVM and ACPR of 2.2 % and 3 dB respectively, when envelope shifted by only 1 V, revealing an opportunity of trading-off linearity and PAE. The magnitude of the ripple-induced sidebands,

however, is not reduced significantly, as displayed in Figure 4.14 . Even a combination of voltage shift and DPD is not sufficient to recover the out-of-band non-linearities that are introduced by the mixing process.

Table 4-3 Comparison of PA linearity for different levels of voltage shift

$\hat{v}r$	Voltage Shift	EVM	$ACPR_{high}$	$ACPR_{low}$	PAE
0.1	0 V	9.6 %	-26.4 dBc	-25.8 dBc	35.3 %
0.1	1 V	7.4 %	-29.5 dBc	-28.5 dBc	34.1 %
0.1	2 V	6.2 %	-32.3 dBc	-30.8 dBc	32.1 %
0.1	3 V	5.5 %	-33.9 dBc	-32.6 dBc	31.7 %

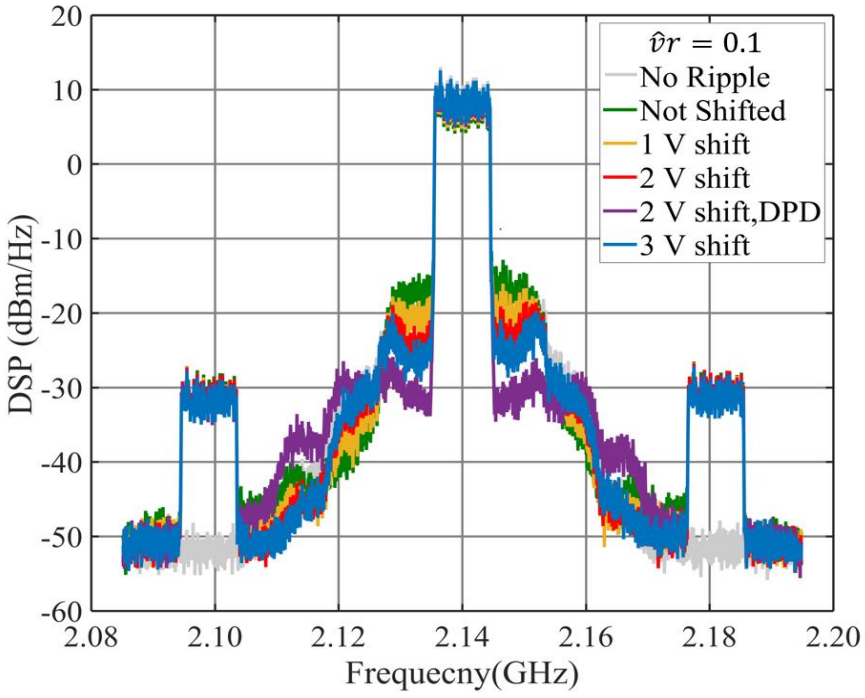

Figure 4.14 Measured PSD at the PA output for different levels of envelope voltage shift

4.6 Conclusions

In this chapter, a measurement-based investigation of the effect of supply voltage ripple on the ET-PA is presented. Firstly, the theoretical effect of the ripple on the linearity of the ET-PA is discussed, and then measurement results were presented that confirm the theory and show that generally linearity degrades as the ripple amplitude increases. This measurement approach allows, for the first time, a realistic measurement-based evaluation of acceptable levels of switching noise / ripple voltage, from the perspective of a GaN power transistor based PA. Reshaping the drain bias voltage, by adapting the shaping function to reduce the interaction between dynamic load-line and the knee region, can be used to enhance the linearity performance, albeit at the cost of lower average efficiency. Importantly, it is shown that the usefulness of digital pre-distortion (DPD) linearization is limited to improving in-band distortion when significant non-coherent output ripple is present, due to the unpredictable and 'memory-like' nature of the interaction between the load line and knee region. These investigations can assist in ET system-level design, giving designers of supply modulators and ET-PAs guidance in terms of the amount of ripple that can be considered acceptable.

4.7 Reference

[1] Z. Popovic, "GaN power amplifiers with supply modulation," 2015 IEEE MTT-S International Microwave Symposium, Phoenix, AZ, 2015, pp. 1-4.

[2] B B. Kim et al., "Push the Envelope: Design Concepts for Envelope-Tracking Power Amplifiers," in IEEE Microwave Magazine, vol. 14, no. 3, pp. 68-81, May 2013.

[3] N. Wolff, W. Heinrich and O. Bengtsson, "100-MHz GaN-HEMT Class-G Supply Modulator for High-Power Envelope-Tracking Applications," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 3, pp. 872-880, March 2017.

[4] P. T. Theilmann, J. J. Yan, C. Vu, J. Moon, H. P. Moyer and D. F. Kimball, "A 60MHz Bandwidth High Efficiency X-Band Envelope Tracking Power Amplifier," 2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), Monterey, CA, 2013, pp. 1-4.

[5] A. Disserand, A. Martin, P. Bouysse and R. Quéré, "High efficiency GaN HEMT switching device with integrated driver for envelope tracking modulators," 2018 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMIC), Brive La Gaillarde, 2018, pp. 1-3.

[6] S. Paul, N. Wolff, C. Delepaut, V. Valenta, W. Heinrich and O. Bengtsson, "Analysis of Dissipated Power in Envelope Amplifier Output Filters," 2018 48th European Microwave Conference (EuMC), Madrid, 2018, pp. 515-518.

[7] J. T. Stauth and S. R. Sanders, "Power supply rejection for common-source linear RF amplifiers: theory and measurements," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2006, San Francisco, CA, 2006, pp. 4 pp.-320.

[8] M. Hassan, L. E. Larson, V. W. Leung and P. M. Asbeck, "Effect of envelope amplifier nonlinearities on the output spectrum of Envelope Tracking Power Amplifiers," 2012 IEEE 12th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Santa Clara, CA, 2012, pp. 187-190.

[9] B. Sahu and G. A. Rincon-Mora, "System-level requirements of DC-DC converters for dynamic power supplies of power amplifiers," Proceedings. IEEE Asia-Pacific Conference on ASIC,, Taipei, Taiwan, 2002, pp. 149-152.

[10] H. Kobayashi and P. M. Asbeck, "Active cancellation of switching noise for DC-DC converter-driven RF power amplifiers," 2002 IEEE MTT-S

International Microwave Symposium Digest (Cat. No.02CH37278), Seattle, WA, USA, 2002, pp. 1647-1650 vol.3.

[11] S. Cripps, RF Power Amplifiers for Wireless Communications. Artech House, 2006.

[12] Texas Instruments. "420-MHz High-Speed Current-Feedback Amplifier." http://www.ti.com/lit/ds/symlink/ths3001.pdf (accessed 2018).

[13] Analog Devices. "ADA4870 High Speed, High Output Current Amplifier." https://www.analog.com/media/en/technical-documentation/user-guides/ADA4870ARR-EBZ-UG-685.pdf (accessed 2018).

[14] Cree. "CGH40010, 10W RF Power HEMT Datasheet." https://www.wolfspeed.com/media/downloads/317/CGH40010-Rev4_0.pdf (accessed 2018).

[15] Rohde & Schwarz. " Envelope Tracking and Digital Pre-Distortion Test Solution for RF Amplifiers." https://scdn.rohde-schwarz.com/ur/pws/dl_downloads/dl_application/application_notes/1gp104/1GP104_2E_ET_DPD_testing_for_amplifiers.pdf (accessed 2019).

Chapter 5

A Novel Modulated Rapid Load Pull System with Digital Pre-Distortion Capabilities

5.1 Introduction & Motivation

As discussed in the introduction to this thesis, current and future wireless communication systems, for instance, 5G, need to support increasingly high data rates. To facilitate this and improve spectral efficiency, complex modulation schemes must be used with associated high peak-to-average power ratios (PAPR). The amplification of these complex signals leads to significant challenges in terms of the linearity and efficiency requirements for emerging PAs. It is therefore highly desirable to be able to characterise and optimise performance of the PA as quickly and as early as possible in the design process. Load pull, as presented in the literature review chapter, is a well-established technique regularly used early in the PA design process to characterise the performance of a device at fundamental and higher harmonic frequencies, usually in terms of output power, efficiency, gain and, when using modulated signals, linearity. In the active load pull approach, the emulated impedance environment is generally insensitive to drive level and bias conditions, a property that can significantly speed up device measurements [1], [2].

Digital pre-distortion (DPD) is currently the most common industrial

approach to linearity correction for PAs. As well as correcting for nonlinearities, DPD allows the PA to operate further into compression, maximizing output power and in turn improving PA efficiency. As the performance of digital signal processing hardware increases, it has become possible to apply increasingly complex correction algorithms to further improve both static and dynamic nonlinearity. Over recent years, many DPD algorithms have been proposed, the most common of which include the Volterra series model [3], memory polynomial (MP) and generalised memory polynomials (GMP) [4]. Although there have been several publications that have documented the use of load pull with DPD using modulated excitation signals [5], [6] these two measurements were not performed simultaneously.

This chapter presents, for the first time, a combination of an active, modulated, impedance emulation system, the Mesuro RAPID system, and DPD, in one integrated measurement system. Such a measurement setup enables the PA designer to characterise devices within emulated PA modes and architectures, under realistic modulated signal conditions and investigate how well they respond to linearisation with standard DPD techniques. This chapter starts by describing the modulated RAPID load-pull (RLP) system along with the DPD techniques used in this chapter, and then demonstrates the accuracy of the calibrated system. After this, the dynamic range of the system is investigated and shifted to high power to enable the measurement for high power device. The system functionality is then demonstrated through the characterisation of a Wolfspeed 10W GaN HEMT device

in terms of its output power and ACPR contours, before and after DPD. Finally, conclusions are given.

5.2 Integrated System Configuration

The measurement system demonstrated in this chapter can be split into two distinct parts; firstly, the RLP and secondly the simultaneous application of DPD. With reference to Figure 5.1, the RLP system consists of an RF test set for coupling the incident and reflected traveling waves present at a device under test (DUT), a 'Digital Tuner' to provide the necessary up- and down-conversion functionality and a digital front-end comprising high-speed ADCs and DACs, and FPGA and a transceiver element.

5.2.1 RF Test Set

The RF test set comprises three 20 dB directional couplers and switch. Two of the 20 dB directional couplers are used to access the travelling waves (a_1, b_1, b_2 and a_2) and one is used to provide the system with a reference signal. The switch is used to control direction of signal flow through the test set between P1 and P2 for calibration purposes.

5.2.2 Digital Tuner

The Digital Tuner houses the I & Q demodulators, which are used for down-conversion of travelling waves (a_1, b_1, b_2 and a_2) ready for the FPGA, as well as

a high-speed modulator to take the FPGA synthesised I & Q data and generate the required modulated load-pull signal. As the FPGA within the measurement and digital synthesis block is designed to deal with only low frequency and low power signals, the signal b_2, that will usually describe the high-power forward travelling power wave generated by a PA, needs to be attenuated before being down-converted using an I & Q demodulator block.

The FPGA then takes the demodulated I & Q data representing b_2, which fully represents the modulated RF signal at the output of the DUT, and modifies these to generate the required broad-band reflection coefficient by producing new modified I & Q data ready for up-conversion. The 'active load-pull loop' is then completed by amplifying the upconverted signal using an linear injection amplifier, before presentation to the DUT. Importantly, the up- and down-conversion process shares a common local oscillator (LO), which relaxes the requirement for the drive signal of the device and the active loop to be phase locked. This also means that there is no drift in phase over time between the two signals – a problem inherent in open-loop architectures. The bandwidths associated with the components within the Digital Tuner provides an ability to present constant and specific load impedances over a potentially very wide bandwidth.

The FPGA both enhances speed and applies further signal conditioning to apply the principles of envelope load-pull, as outlined in [7]. The high-speed ADC/DAC and FPGA are both commercially available PXI chassis-based

components available from National Instruments (NI). Additional external hardware components are added in the form of an injection loop amplifier to provide highly linear amplification of the injected signal needed to load-pull the active device. A circulator is added at the output and used as an injection point for the load pull signal, whilst safely terminating the amplifier's output as shown in Figure 5.1.

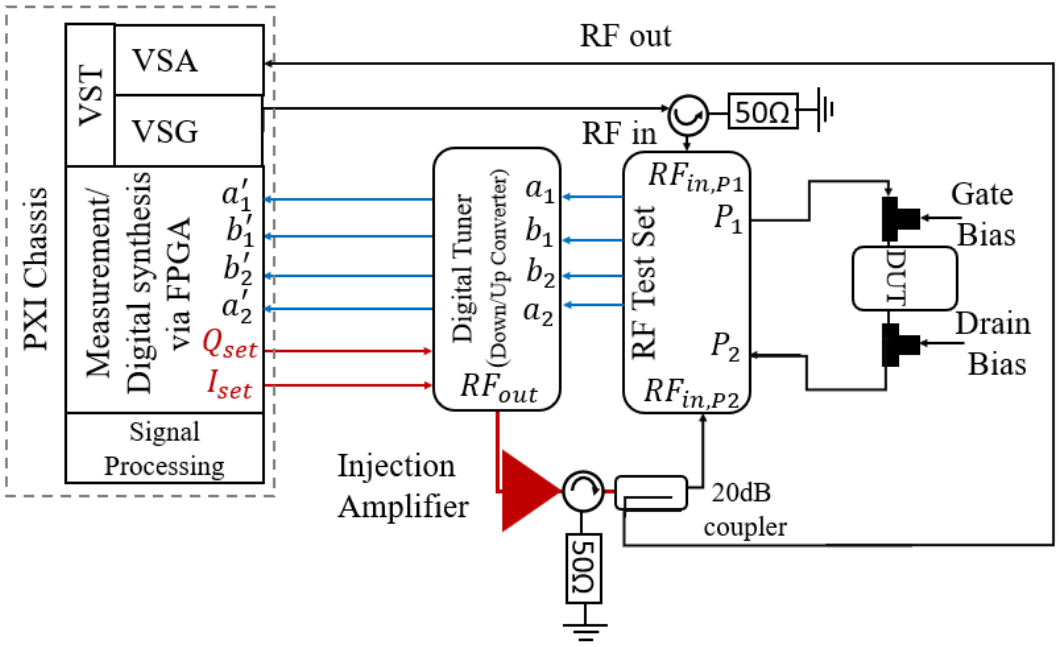

Figure 5.1 Simple representation of the integrated measurement system with RLP with DPD

The system hardware is implemented within an NI PXI Vector Signal Transceiver (VST). This VST is able to support up to 1GHz signal bandwidth and up to a maximum operating frequency of 6GHz. The proprietary DPD algorithm is implemented in a NI provided software package called RFIC [8]. To provide the required feedback signal for the DPD, an additional 20 dB coupler is inserted prior to the circulator. As both

systems utilise PXI chassis-based components, it is very convenient to package all of the NI based hardware within a single chassis leading to a compact, easily synchronized, yet very powerful and flexible measurement setup. The integrated system is outlined in Figure 5.2. All of the RLP and DPD software is controlled using the in-chassis controller. The fast PCI based backplane provides the ability to stream and process data to and from both the RLP and DPD systems, providing real-time analysis. An example is the real-time display of useful analytical data in the form of AM-AM, AM-PM and useful DPD signal metrics such as peak expansion.

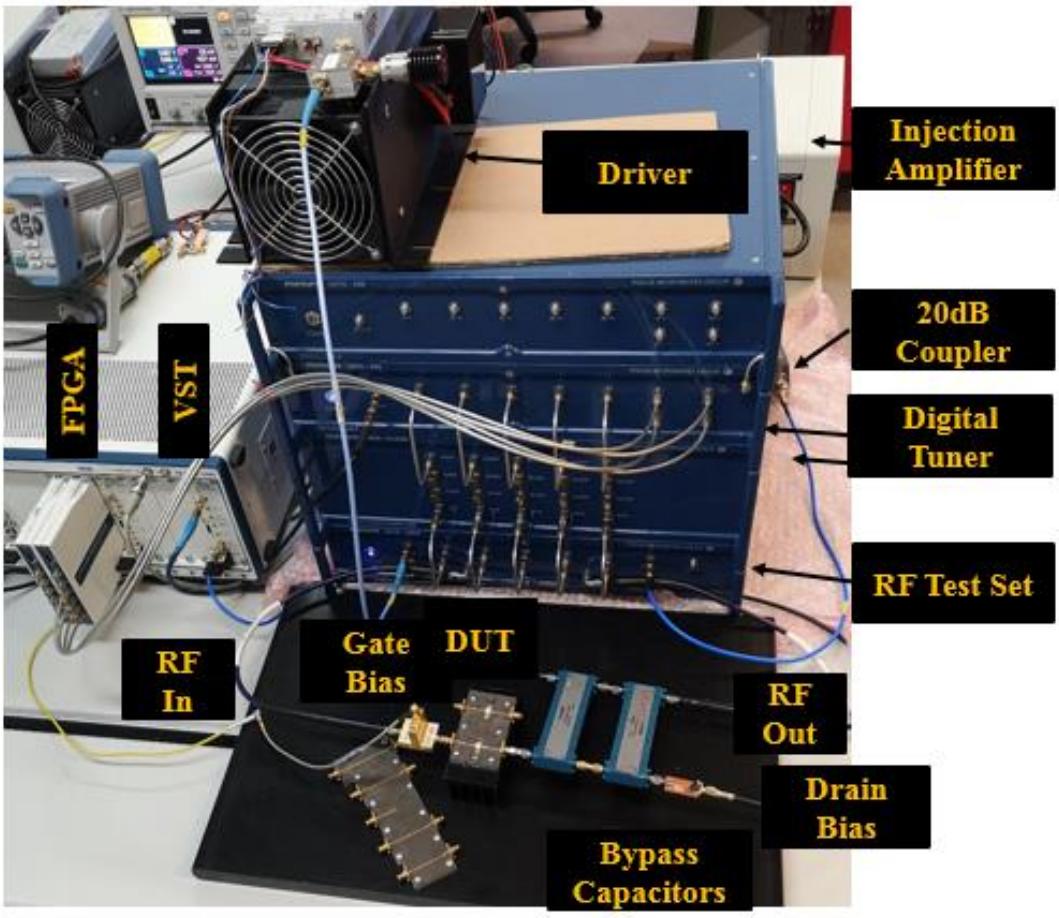

Figure 5.2 Measurement system configuration for RLP and DPD

5.3 System Calibration and Validation

Generally, the objective of load pull characterisation of active devices is to obtain a range of measurements that describe the device performance under specific realistic or imposed impedance conditions. However, errors due to imperfect system components, such as inherent directivity, mismatch, and cross-coupling, cause uncertainty in the measurement, which, in this case, can lead to incorrectly measured optimum impedances and RF power at the calibrated reference planes. It is, therefore, essential to correctly calibrate the load pull system to be able to both accurately set and measure the synthesized reflection coefficient and hence accurately measure key parameters, such as output power and ACPR. As stated earlier, the system is separated into two parts, RLP, and DPD, which will now be discussed in more detail in terms of how they are calibrated. For the RLP, the system is calibrated in four stages; firstly, vector calibration of the complete system, secondly absolute power calibration, followed by the third step, in which the imperfections associated with the load pull injection hardware have to be corrected for quadrature error by nulling the local oscillator (LO) and its image. The final step involves a load pull loop calibration that is conducted with a signal that covers the full load pull bandwidth.

5.3.1 Vector Calibration

A standard two-port TRL calibration is performed at the DUT reference planes to measure the device reflection coefficients using a TRL calibration kit that consists of distinct thru-reflect- and line-standards milling on Rogers laminate. To cover the entire 1-12 GHz frequency range, two-line elements were employed. After that, an absolute power calibration is conducted by connecting a power meter to port1 of the DUT.

5.3.2 Loop Gain Calibration

The loop calibration is determined using a linear error flow model to represent the load pull part of the system, which is shown in Figure 5.3 Here, the system impedance, Γ_0, is defined at zero gain, Γ_F is the feedback term and represents the limited isolation of the loop, the transfer function of the down-converter and up-converter are T_{Down} and T_{UP}, respectively. The required load reflection coefficient is Γ_{Set}, and based on this simple error model as defined in detail in [9] and shown in (5.1).

$$\frac{a_2}{b_2} = \frac{\Gamma_{Set}.T_{Down} \cdot T_{Up}}{1 - \Gamma_F\left(\Gamma_{Set}.T_{Down} \cdot T_{Up}\right)} + \Gamma_0 \qquad (5.1)$$

Due to the imperfections of the system, the measured load Γ_{Meas} is related to Γ_{Set} through equation (5.2).

$$\Gamma_{\text{Meas}} = \left(\frac{\Gamma_{Corr}.G}{1-\Gamma_F(\Gamma_{Corr}.\text{G})}\right) + \Gamma_0 \tag{5.2}$$

Where

$$G = T_{Down} \cdot T_{Up} \tag{5.3}$$

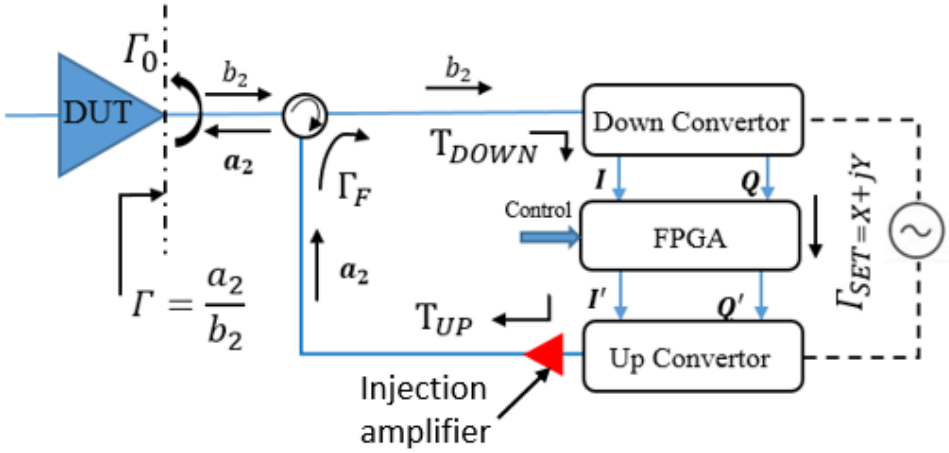

Figure 5.3 Block diagram of ELP displaying the identified sources of errors in the loop components

Rearrange equation (5.2) will yield the following equation

$$\begin{aligned}\Gamma_{\text{Meas}} = \Gamma_0 + \Gamma_{\text{Meas}}\Gamma_{\text{Corr}}(\Gamma_{\text{F}}G) \\ + \Gamma_{\text{Corr}}\big(G(1-\Gamma_0\Gamma_{\text{F}})\big)\end{aligned} \tag{5.4}$$

$$\Gamma_{\text{Meas}} = A + \text{B}(\Gamma_{\text{Meas}}\Gamma_{\text{Corr}}) + C(\Gamma_{\text{Corr}}) \tag{5.5}$$

Where

$$A = \Gamma_0 \tag{5.6}$$

$$B = \Gamma_F G \tag{5.7}$$

$$C = G(1 - \Gamma_0 \Gamma_F). \tag{5.8}$$

From equations (5.5) three independent measurement variables are required to fully characterise the loop.

To validate the loop calibration, an extensive verification across the Smith Chart is conducted on a thru, with the example results shown in Figure 5.4. These results show excellent accuracy to better than -40 dB (1%).

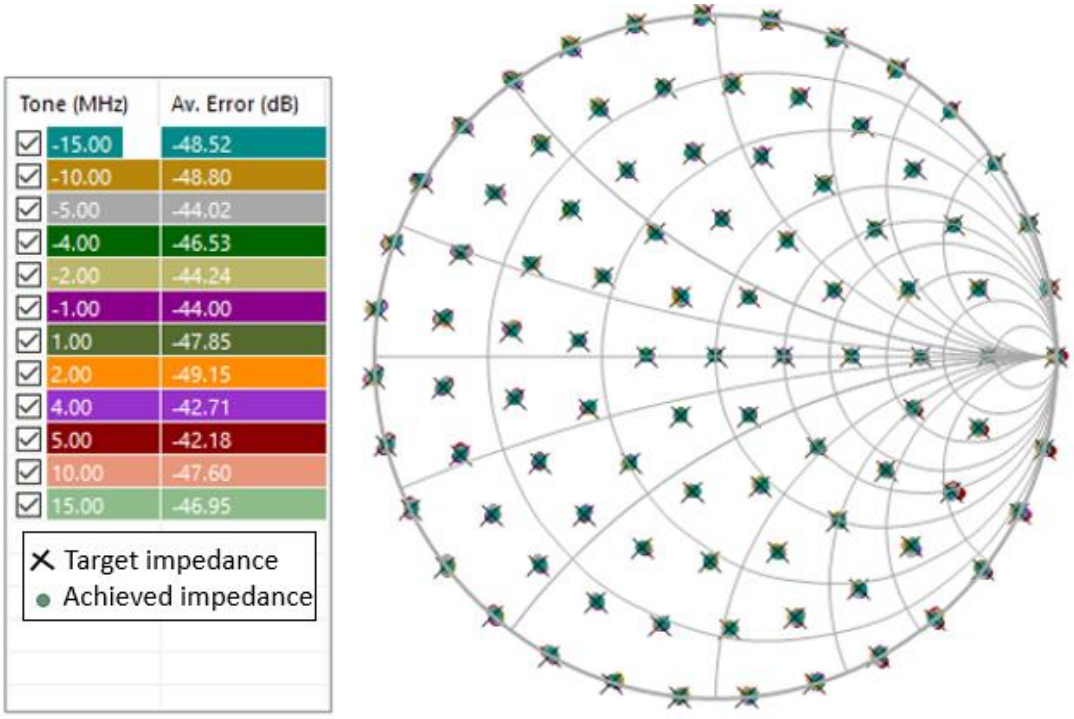

Figure 5.4 Accuracy of the loop calibration

5.4 Investigating & Extending Dynamic Range:

Investigating the capabilities of any system is an important step in order to ensure its efficient use. Thus, the dynamic range of the RLP system needed to be characterised. However, before starting, the power handling capabilities of the system needed to be considered and fully understood. Based on the system specification and with reference to Figure 5.6, there are two power handling considerations for the RF Test Set to consider; firstly during vector calibrations at the calibration input (*Cal In*) port with the system configured such that the loop link cables connect RF Out to RF in P1, and Cal Out P2 to RF In P2. In this configuration, a calibration signal is routed through the test set, and the maximum power is limited to 1W by the central calibration switch. Once these links are removed following calibration however, the power handling of the test set increases to 50 W CW. Also, importantly, the maximum linear input power that can be delivered to the Digital Tuner is -10 dBm, so the input powers present at this part of the system need to be considered carefully, with suitable attenuation used.

The dynamic range of the system was characterised by sweeping the input power after calibrating the system, from -40 dBm to 15 dBm using a THRU, at the expected optimum impedance of Γ_L=0.43∠162. The system successfully presents a near constant emulated load across a 40 dB dynamic range, from -25 dBm to 15 dBm as depicted in Figure 5.5.

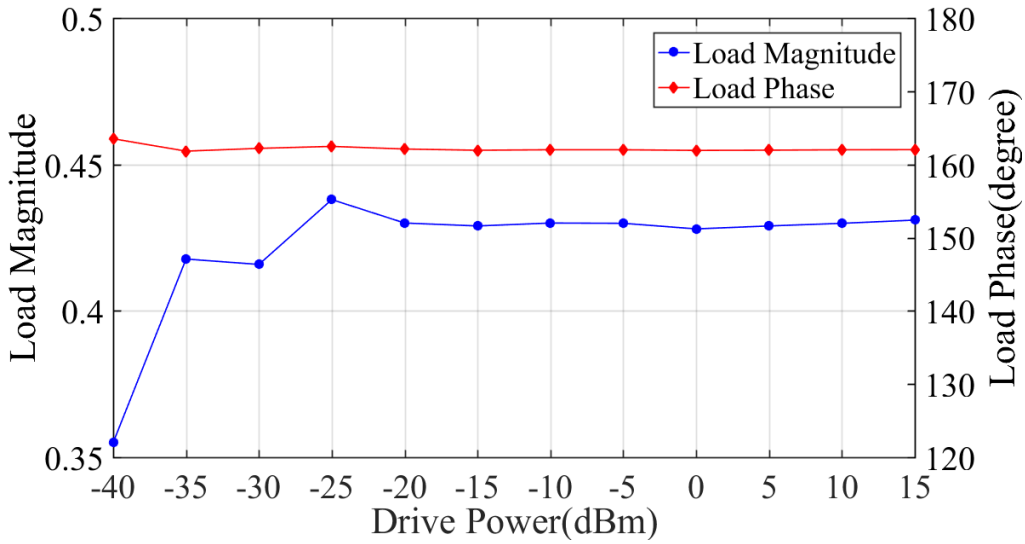

Figure 5.5 Power sweep over a dynamic range of 40 dBm, while the optimum impedance of (Γ_L=0.43∠162°) is kept constant

Now that the dynamic range of the system had been established, for higher power measurements, it needed to be shifted to enable the measurement of, for example a 10 W GaN HEMT device. Based on the maximum input power for the Digital Tuner, which is -10 dBm and RF test set loss which is -20 dBm (coupling factor and associated loss), a 30dB attenuation is required to shift the dynamic range of the system to accommodate a maximum port-2 power of 40 dBm. Thus, the normalised travelling wave amplitudes (a_1, b_1, b_2 and a_2) were attenuated by 30 dB as shown in Figure 5.6.

Importantly, in the new configuration, the injection amplifier used needed to be driven backed off by at least at 10 dB, in order to operate in a sufficiently linear domain. This requires an injection amplifier with 50 dB of gain and 50 dBm output power. Then, the dynamic range of this attenuated configuration of the system was remeasured with a 60 dB power sweep (from-20dBm to 40 dBm) which again, was

conducted at the expected optimum impedance of Γ_L=0.43∠162. As shown in Figure 5.7 the magnitude and phase of the load impedance were close to constant over the entire 50 dB power range.

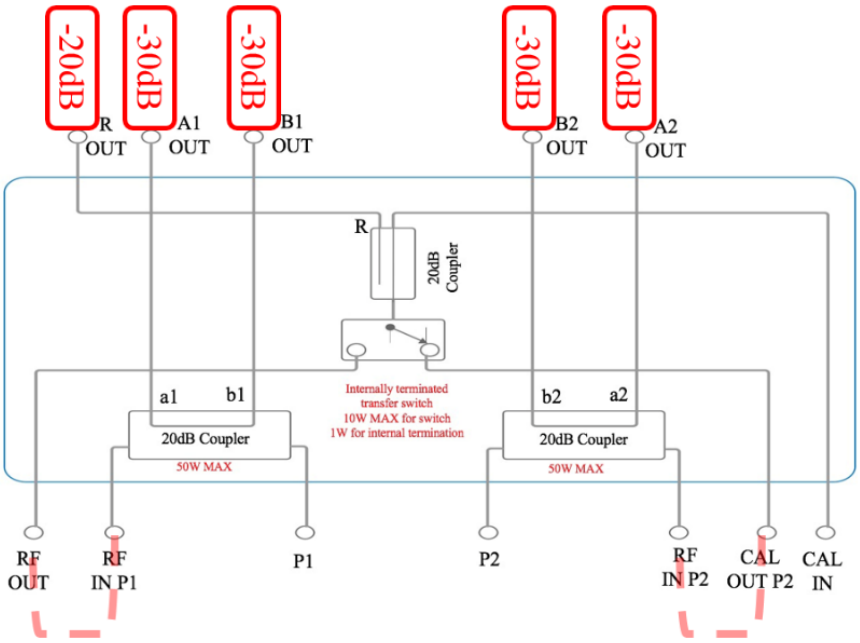

Figure 5.6 The attenuation configuration for RF Test Set to shift the dynamic range of the system to accommodate a 40dBm device.

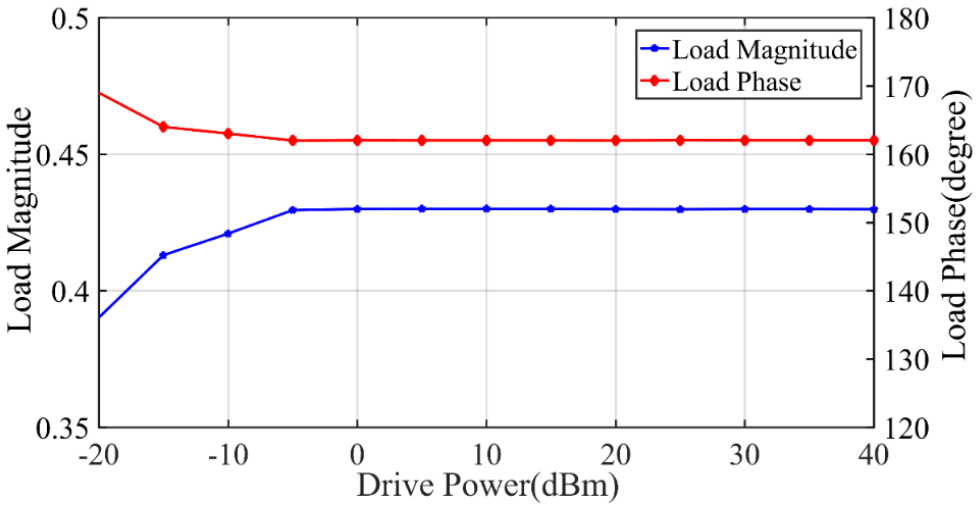

Figure 5.7 Power sweep over a dynamic range of 50dBm, while the optimum impedance of (Γ_L=0.43∠162°) is kept constant

5.5 Load Pull Measurement

5.5.1 Measured Device in Fixture

The device which was used in this measurement is a 10 W GaN HEMT device from Wolfspeed/CREE [10] mounted within a simple microstrip test fixture. The device was stabilized using a parallel RC arrangement at the gate as shown in the lower part of the fixture, in Figure 5.8. Firstly, the stabilization circuit was designed using 10 W GaN HEMT full nonlinear model in the Keysight Advanced Design System (ADS) tool, biased with the quiescent drain current of I_{DQ}=100 mA (class AB) and the quiescent drain voltage V_{DQ}=28 V. The values of the stabilization capacitor and the resistors are R=100 Ω and C=2 pF.

Figure 5.8 A 10W GaN HEMT device on test fixture with series in-line stability circuit in place

5.5.2 Baseband impedance control

In order to properly characterise the linearity of an active device, it is not enough to simply perform source and load pull at the fundamental and harmonic frequencies. In fact, the linearity performance of a transistor depends strongly on the impedance that the transistor sees at the baseband frequencies. For this reason, any transistor-level linearity characterisation must be carried out with either the bias circuit that will be used in the final application or otherwise baseband impedance control is required [11], [12]. The baseband impedance can be terminated to a short circuit either with a passive method [11] or using an active approach [13], [14]. Therefore, additional hardware was added to allow both biasing of the gate and drain of the device, as well as to providing a means for baseband (< 30 MHz) impedance control using a variety of capacitors as shown in Figure 5.9.

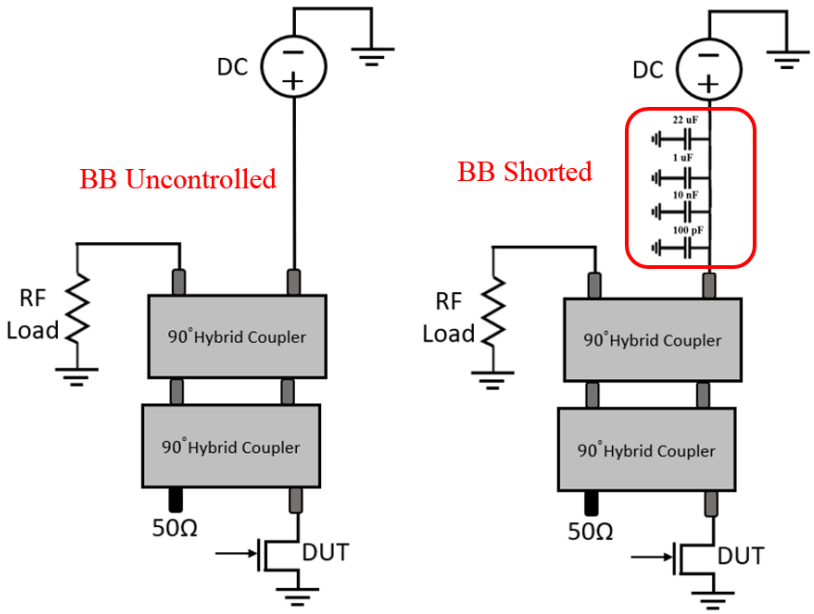

Figure 5.9 Baseband impedance control circuit

After adding the baseband termination, the baseband impedance presented to the device was measured using a calibrated VNA over a 30 MHz bandwidth as shown in Figure 5.10. It is clear that the baseband impedance trajectory was far away from the edge of the Smith chart before inserting the baseband short-circuit. However, the baseband impedance moves to the edge of the Smith chart, much closer to a short circuit when the bypass capacitors circuit was inserted. This reduced baseband impedance is important as it will reduce electrical memory effect related non-linearity.

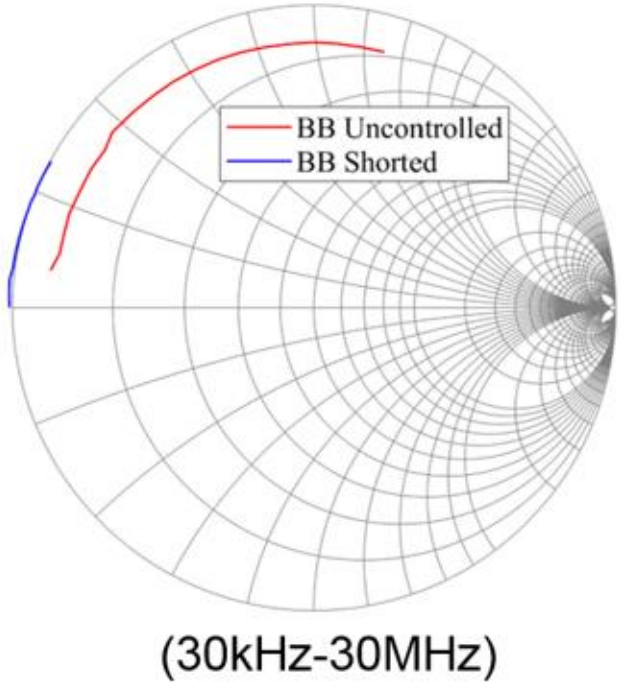

Figure 5.10 The baseband impedance before and after applying shorting capacitors, over 30 MHz

Afterward, the 10 W GaN HEMT device was excited with a 10 MHz LTE input signal such that the output peak envelope power (PEP) achieved P_{1dB} compression. while the out-band distortion (ACPR) and the in-band distortion (EVM) were

measured using the system, before and after adding the baseband impedance termination. Figure 5.11 clearly shows the significant improvement in both ACPR and EVM of the device when baseband impedance is terminated into a short circuit. An enhancement of 10 dB in the ACPR and 7 % in the EVM can be noticed at a peak output power of 40 dBm. Also, Figure 5.12 shows big improvement in output spectral when baseband impedance is shorted.

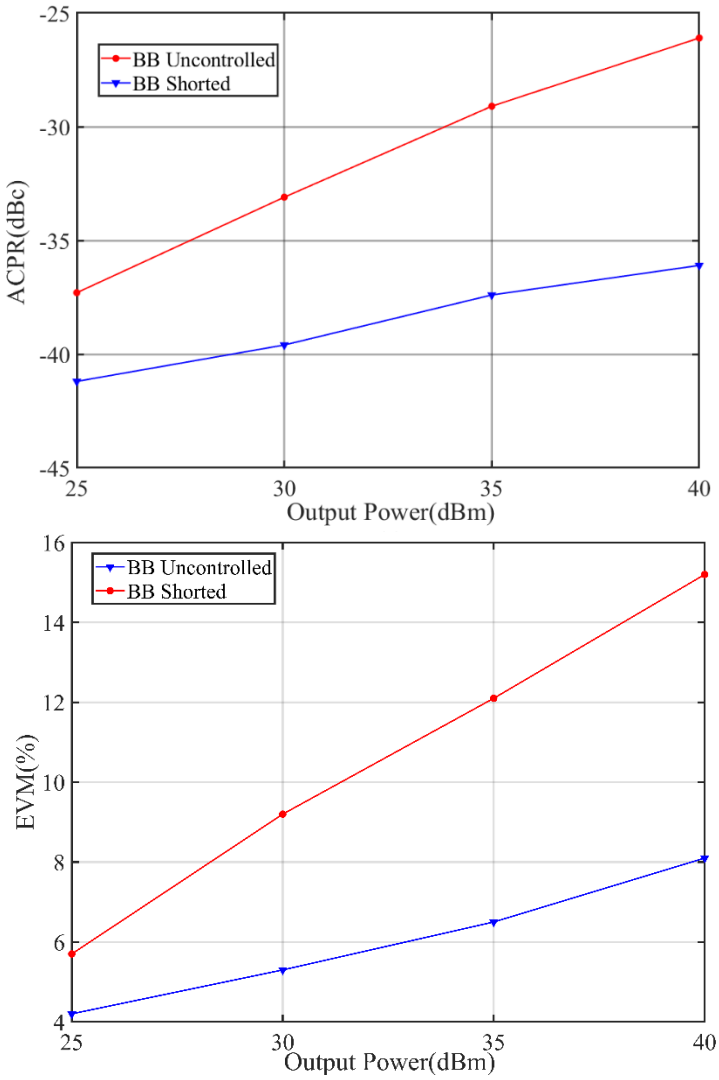

Figure 5.11 The EVM and the ACPR performance before and after baseband shorted for 10MHz LTE signal

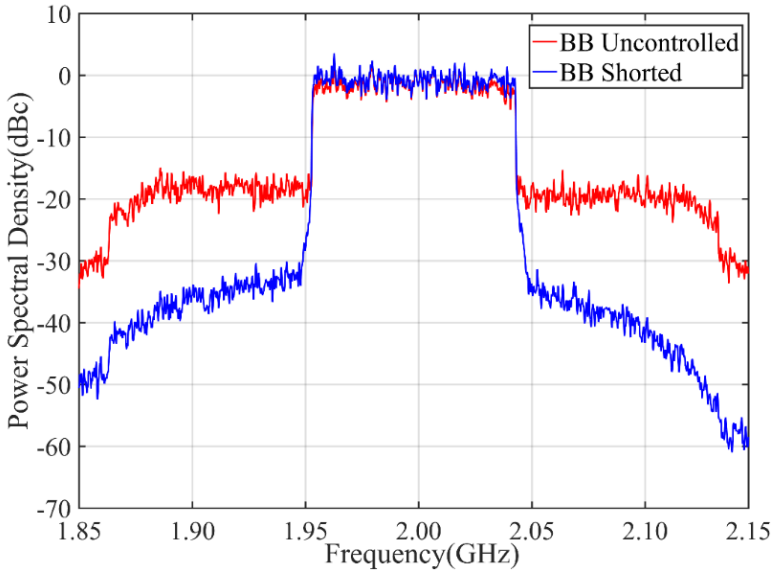

Figure 5.12 A 10 MHz LTE signal power spectral density before and after baseband impedance shorted

5.5.4 CW Load Pull Verification Measurement

To verify the system, a CW load pull measurement was carried out on a 10 W GaN HEMT device mounted in the test fixture shown in Figure 5.8. The device was biased in deep class AB where the quiescent drain current is I_{DQ}=100 mA and the quiescent drain voltage is V_{DQ}=28 V, and excited at a centre frequency of $f_o = 2$ GHz.The fundamental impedance was swept on a circular grid defined by 38 impedance points around the expected optimum impedance for output power, while the device was driven to 1 dB compression. The output power and PAE contours are shown in Figure 5.13. The optimum impedance for the output power of 40.22 dBm is identified at 16.35+j8.63 Ω, and the optimum impedance for maximum PAE of 63% is at 13.65+12.49 Ω.

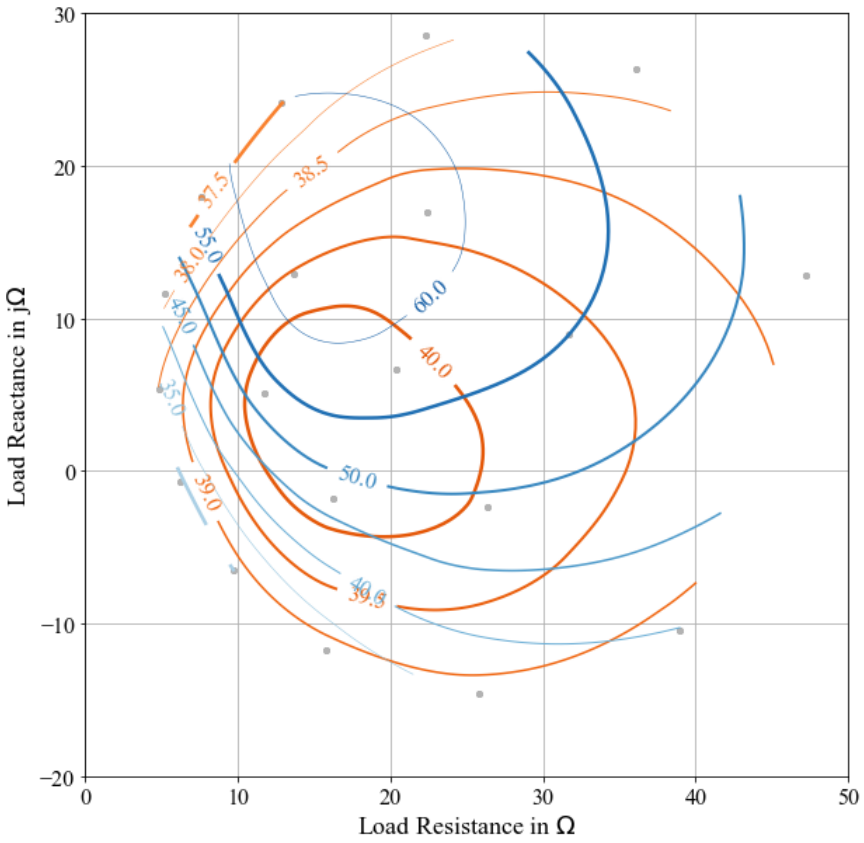

Figure 5.13 Output power (orange contours), PAE (blue contours) load pull contours for 10 W GaN HEMT device with CW signal

5.5.5 Modulated Signal Load Pull Verification

A 10 MHz LTE signal with a PAPR of 6.8dB at a centre frequency of $f_o = 2$ GHz was used to perform modulated load pull measurements on a circle grid of 38 impedance points around the expected fundamental optimal impedance for output power. As for previous cases measurement case, the device was driven until the peak envelope power (PEP) equalled P_{1dB}. The output power and ACPR results of the modulated load pull measurements are shown in Figure 5.14. The output power contours appear in the expected location for the device used, and are in good agreement with the CW measurement, in the upper part of the Smith chart, while the

optimum impedance for ACPR is in the lower half of the Smith chart in this case without DPD. The ACPR at the output optimum impedance (16.35+j8.63 Ω) is -37 dBc and the average output power is 34 dBm.

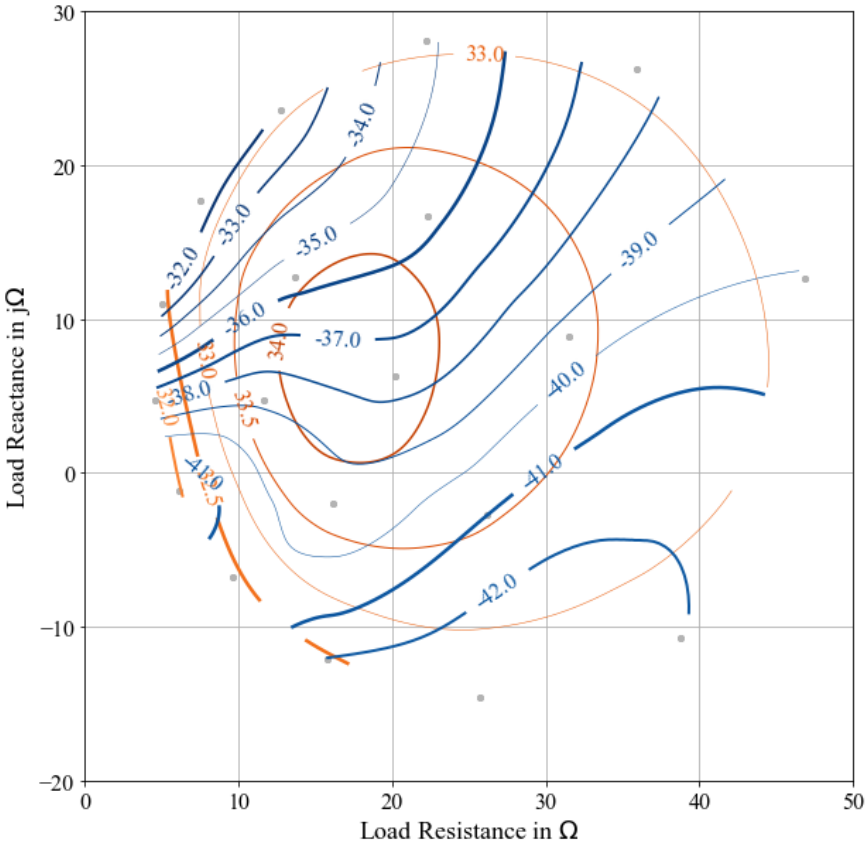

Figure 5.14 ACPR (blue contours) and output power (Orange contours) load pull contours for 10 W GaN HEMT device with a 10 MHz LTE (PAPR = 6.8 dB) source without DPD

5.5.6 Modulated Signal Load Pull with DPD

A generalised memory polynomial (GMP) digital pre-distortion model with an order of 3 and memory depth of 5 was used to Linearise the output signal, alongside modulated load pull with A 10 MHz LTE signal used as excitation, as described in the previous section. The output power and ACPR contours are measured as illustrated in

Figure 5.15.

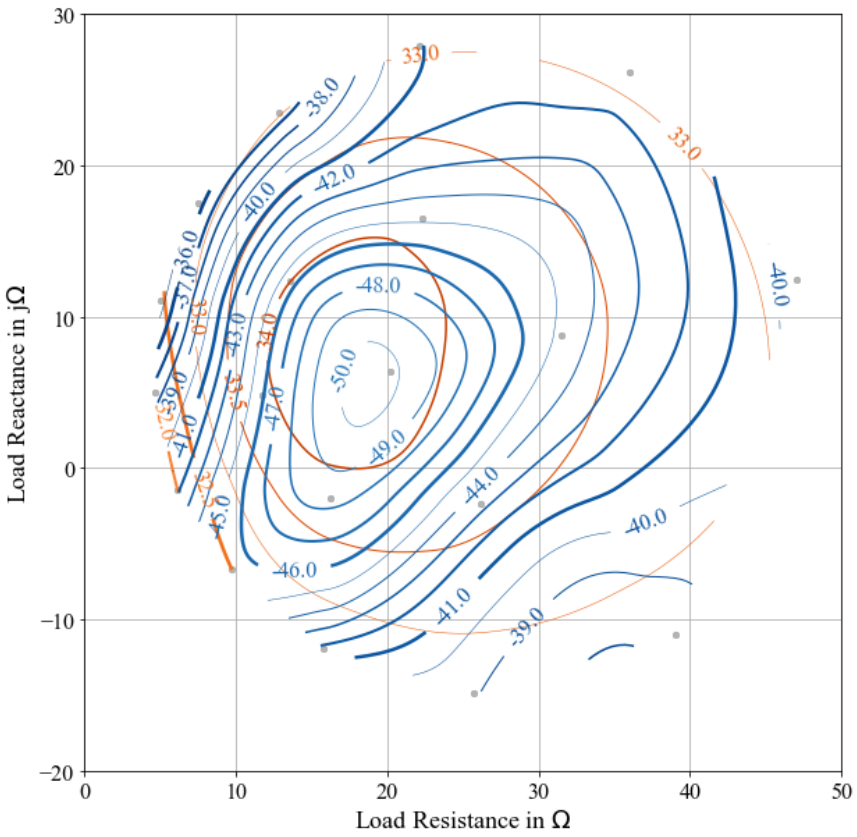

Figure 5.15 ACPR (blue contours) and average output power (Orange contours) load pull contours for 10 W GaN HEMT device with a 10 MHz LTE (PAPR = 6.8 dB) source with GMP DPD

The ACPR improves from -37 dBc to -50 dBc when GMP is applied at the optimum impedance. Interestingly, the optimum impedance for ACPR moved to the upper part of Smith Chart and aligns exactly with optimum output power impedance. From a measurement perspective, this result implies that RFPA designer can design for optimum output power impedance without worrying about the existance of a separate linearity optimum. This because the DPD will compensate for the degradation of the ACPR.

5.7 Chapter Summary

This chapter presents a novel combination of a modulated active load-pull system with a separate measurement system providing DPD. Experimental results verify the ability of the system to accurately maintain a load over both wide dynamic range and modulation bandwidth and show that both load-pull and DPD can be applied simultaneously. The measurements of a 10 W GaN HEMT device have highlighted a large difference in ACPR contours with and without DPD and show that while non-pre-distorted ACPR and output power contours have very different optimum impedances, the contours closely align once DPD is applied. This suggests that the impedance for maximum output power is a more interesting impedance to target when designing power amplifiers which will be operated with DPD. The result also presents the interesting idea of using such a system to rapidly identify, for example, the maximum linearisable output power for other emulated amplifier modes. The measurements demonstrate that this system combination can be used as a valuable tool in PA design to fully characterise the device under realistic modulated and impedance conditions, as a way of exploring design space when simultaneously linearising the device with DPD techniques.

5.8 Reference

[1] M. Hashmi, A. Clarke, J. Lees, M. Helaoui, P. Tasker, and F. Ghannouchi, "Agile harmonic envelope load-pull system enabling reliable and rapid device characterisation," Measurement Science and Technology, vol. 21, no. 5, p. 055109, 2010.

[2] F. M. Ghannouchi and M. S. Hashmi, "Load-pull techniques and their applications in power amplifiers design (invited)," 2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Atlanta, GA, 2011, pp. 133-137.

[3] R. J. P. de Figueiredo, "The Volterra and Wiener theories of nonlinear systems," in Proceedings of the IEEE, vol. 70, no. 3, pp. 316-317, March 1982.

[4] D. R. Morgan, Z. Ma, J. Kim, M. G. Zierdt and J. Pastalan, "A Generalized Memory Polynomial Model for Digital Predistortion of RF Power Amplifiers," in IEEE Transactions on Signal Processing, vol. 54, no. 10, pp. 3852-3860, Oct. 2006.

[5] G. I. Abib, S. Bensmida, E. Bergeault and B. Huyart, "A source-pull/load-pull measurement system including power amplifier linearization using simple instantaneous memoryless polynomial base-band predistortion," 2006 European Microwave Conference, Manchester, 2006, pp. 252-254.

[6] M. Ubostad and M. Olavsbråten, "Linearity performance of an RF power amplifier under different bias-and load conditions with and without DPD," 2010 IEEE Radio and Wireless Symposium (RWS), New Orleans, LA, 2010, pp. 232-235.

[7] P. J. Tasker, "Practical waveform engineering," in IEEE Microwave Magazine, vol. 10, no. 7, pp. 65-76, Dec. 2009.

[8] National Instruments. "NI RFIC 2.5 Test Software." http://www.ni.com/download/rfic-test-software-2.5/7752/en/ (accessed 2017).

[9] M. S. Hashmi, A. L. Clarke, S. P. Woodington, J. Lees, J. Benedikt and P. J. Tasker, "An Accurate Calibrate-Able Multiharmonic Active Load–Pull System Based on the Envelope Load–Pull Concept," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 3, pp. 656-664, March 2010.

[10] Cree. "CGH40010, 10W RF Power HEMT Datasheet." https://www.wolfspeed.com/media/downloads/317/CGH40010-Rev4_0.pdf (accessed 2018).

[11] M. J. Pelk, L. C. N. de Vreede, M. Spirito and J. H. Jos, "Base-band impedance control and calibration for on-wafer linearity measurements," ARFTG 63rd Conference, Spring 2004, Fort Worth, TX, USA, 2004, pp. 35-40.

[12] A. K. Manjanna, M. Marchetti, K. Buisman, M. Spirito, M. J. Pelk and L. C. N. de Vreede, "Device characterization for LTE applications with wideband baseband, fundamental and harmonic impedance control," 2013 European Microwave Conference, Nuremberg, 2013, pp. 255-258.

[13] M. Akmal et al., "Characterization of electrical memory effects for complex multi-tone excitations using broadband active baseband load-pull," 2012 7th European Microwave Integrated Circuit Conference, Amsterdam, 2012, pp. 885-888.

[14] F. L. Ogboi et al., "A LSNA configured to perform baseband engineering for device linearity investigations under modulated excitations," 2013 European Microwave Conference, Nuremberg, 2013, pp. 684-687.

Chapter 6

A Novel Modulated Rapid Load Pull System for the Full Emulation of Envelope Tracking Power Amplifiers

6.1 Introduction and Motivation

The previous chapter stated the need to characterise and optimise the performance of the PA as early as possible in the design cycle. To support this, load-pull is a robust approach commonly utilised at the beginning of the PA design phase to characterise device performance under different load conditions, at fundamental and harmonic frequencies, typically in terms of output power, efficiency, gain and linearity. Unlike active open-loop systems, the active modulated load pull technique used in this work is insensitive to drive level and bias condition, and the device characterisation process can be substantially accelerated as a result. The last chapter concluded by presenting a novel system that combines a modulated active load pull system with a separate measurement system providing digital pre distortion (DPD) which was the first step to realise a measurement that can fully emulate envelope tracking power amplifier (ET-PA) in conjunction with DPD.

This chapter realises, for the first time, the integration of a full ET characterisation bench and Mesuro RAPID modulated load pull system, within a single

combined measurement system. This enhanced characterisation system allows PA designers to quickly characterise for example devices within emulated RFPA modes and architectures, with realistic modulated signal conditions, while investigating their response to ET in conjunction with DPD linearisation techniques. The outline of this chapter is as follows: Firstly, the modulated RAPID load pull (RLP) system coupled to the ET characterisation system is described, followed by measurements to show power-added efficiency (PAE) contours at both fixed and modulated supply voltages, for a CGH40010F Wolfspeed 10 W GaN HEMT device. The functionality of system is then shown using the measurement of the same device in an ET environment using three different look-up table (LUT) -based shaping functions, in terms of efficiency, linearity and output power. Finally, DPD is applied to investigate how well nonlinearity can be corrected, especially for shaping functions used to target high efficiency.

6.2 Measurement System Configuration

The characterisation system presented in this chapter is partitioned into two separate parts, including the RLP and the NI ET measurement system. The RLP system as described in previous chapter comprises an RF test set to couple the incident and reflected traveling signals, a digital tuner which is used to up- and down-convert signals and a digital front-end comprising high speed ADCs and DACs. An FPGA module is used to control all components, to provide speed and flexibility and to implement the concept of 'envelope' load pull, as presented in

[6]. Externally, a highly linear injection loop amplifier is added to deliver the synthesised signal required to actively load pull the device to the required reflection coefficients. At the output of the loop amplifier, a circulator is inserted and used as an injection point for the load pull signal, while safely terminating the amplifier's output into a dissipative load.

For signal generation and measurement, the National Instrument PXIe chassis, which was describe in detail in chapter 3, is equipped with a Vector Signal Transceiver (VST) that can operate up to 6 GHz with 1 GHz instantaneous bandwidth. This instrument comprises a vector signal generator (VSG) and a vector signal analyser (VSA). In addition, a dual-channel arbitrary wave generator (AWG) with a bandwidth of 400 MHz, is used to synthesise the envelope tracking signal. A two-channel PXIe-based oscilloscope is used to monitor the drain voltage and current (via a current probe) and measures the instantaneous efficiency. All modules are synchronized via an internally generated 10 MHz reference clock. Additionally, an external 20 dB coupler was inserted before the circulator to provide the required feedback signal for the ET system.

As both ET characterisation and load-pull systems use PXI chassis-based modules, it is possible to combine all the PXI-based hardware in one PXI chassis, resulting in a compact, yet very robust and flexible measurement system [7]. The chassis controller hosts both the ET and RLP software, as shown in Figure 6.1 and

Figure 6.2. The fast PCI based backplane gives the capability for streaming and processing data to and from the ET and RLP systems to support real-time analysis.

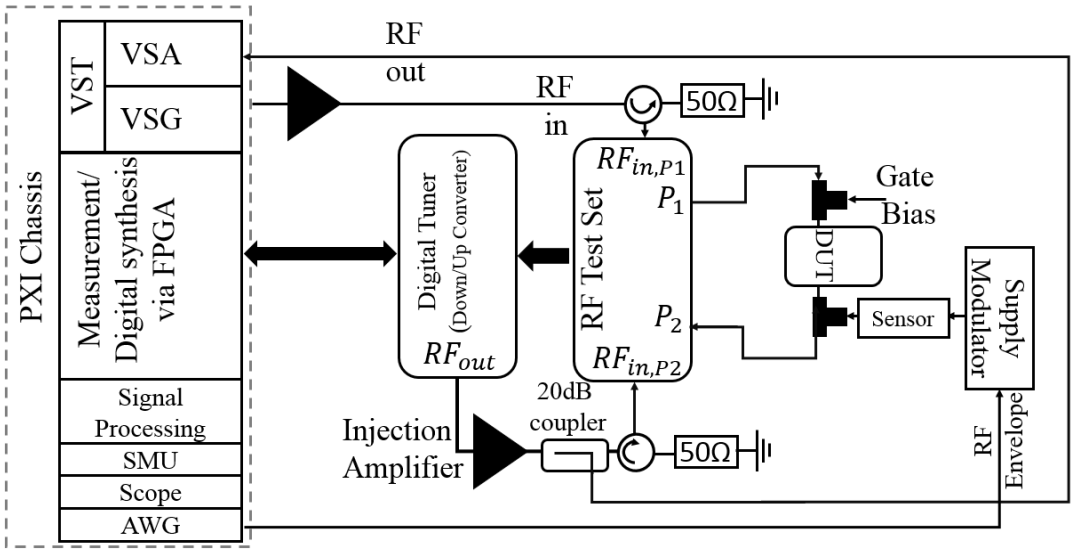

Figure 6.1 Schematic of the measurement system

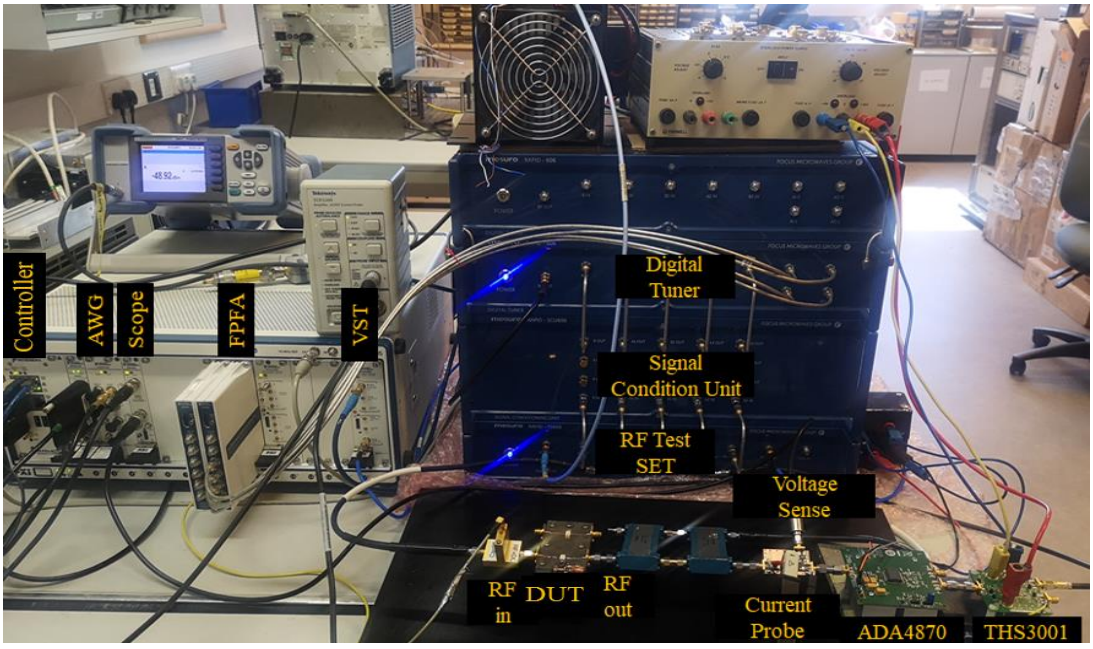

Figure 6.2 Measurement system configuration

6.2 System Calibration

As mentioned in the previous chapter, the purpose of load pull characterisation is to acquire measurement data for an active device that defines the performance of the device in a realistic or imposed impedance environment. Conversely, errors caused by imperfect system elements, for instance, mismatch, cross-coupling and inherent directivity cause measurement uncertainty and incorrect measurement for optimum impedances and RF power at the calibrated reference planes. It is important therefore to precisely calibrate the system, to allow both the accurate setting of the synthesized reflection coefficient, as well as the robust measurement of key parameters, such as output power, efficiency, and linearity. Thus, four calibration steps were followed to calibrate the system sequentially: firstly, vector calibration of the whole system, secondly, absolute power calibration. Afterwards, the quadrature error which is caused by imperfections in the load pull injection hardware should be fixed through nulling the local oscillator (LO) and its image. Finally, a load pull-loop calibration step is performed with a modulated signal which covers the full load-pull modulated bandwidth, as discussed in [6] and [7].

6.3 Emulation Measurement

To demonstrate the capability of the system under ET and modulated load pull conditions, the measurements were carried out on the CGH40010F GaN

device mounted within a simple microstrip test fixture, which demonstrate the capability of the system under ET and modulated load pull conditions. A parallel RC arrangement was used to stabilize the device at its input. The device was biased in class-AB at a quiescent drain current of I_{DQ} = 100 mA.

Firstly, a modulated load pull measurement was conducted at a drain voltage of V_{dd} = 28 V using a 10 MHz LTE signal with a PAPR of 6.8 dB at a centre frequency of 2 GHz and at 1 dB of compression, with the aim of finding the output power's optimum impedance (Z = 16+j11 Ω). Then the device was biased dynamically with the linear supply modulator using two commercial operational amplifiers i.e. THS3001 and ADA 4870 as presented in chapter 4. The envelope of the input signal, i.e. the 10 MHz LTE modulated signal, was extracted from the I & Q data in the NI system and shaped with the de-troughing shaping function (6.1) [8] to produce the desired envelope tracking drain supply voltage:

$$f(V) = 1 - (1 - d)\cos\left(V \cdot {}^{\pi}/_{2}\right) \tag{6.1}$$

$$d = {}^{V_{dd(min)}}\Big/_{V_{dd(max)}} \tag{6.2}$$

Where *f(V)* is the modulated drain supply voltage, *V* is the normalized magnitude of the envelope of the input signal, $V_{dd(\min)}$ and $V_{dd(\max)}$ are the minimum and the maximum values for the drain supply voltage, respectively. The minimum voltage for the envelope was set to 10 V, the maximum voltage to 28 V. The modulated drain voltage was time-aligned with the RF signal using the built-in delay optimiser and

verified using the two-channel oscilloscope. The drain current was detected using a high-speed current probe [Tektronix TCP312A] while the drain voltage was detected using a high impedance voltage divider which composed of external resistance of 1k Ω and internal 50 Ω resistance of the oscilloscope which produces a ratio of $^{1}/_{21}$, as shown in Figure 6.3.

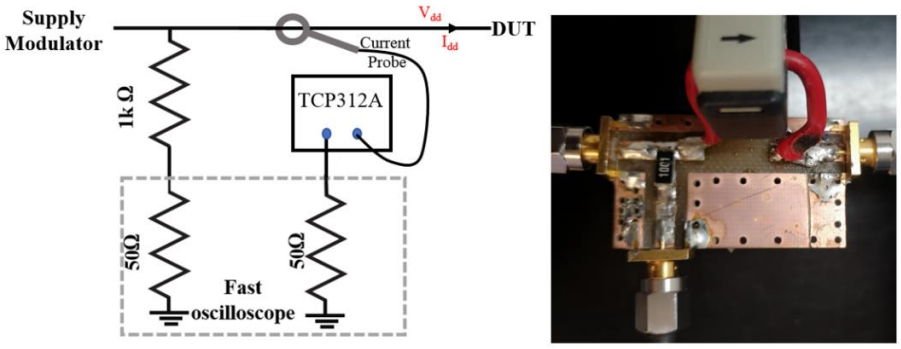

Figure 6.3 Drain current and voltage measurement set up

The PAE contours, as shown in Figure 6.4, are plotted for two cases; 28 V fixed supply and then for applied ET. The contours show the potential enhancement in average PAE when ET is used instead of traditional fixed bias for a 10 MHz LTE signal. At Z_{opt} = 16+j11 Ω, the optimum impedance for P_{out} at 28 V, ET improves the average PAE by around 12 percentage points from 29 % under fixed bias to 41 % with ET. In the highly efficient region of the Smith chart, the average PAE was enhanced by 24 percentage points from 26 % with fixed bias to 50 % under ET at Z = 8+j12 Ω. The efficiency of the linear modulator is not included in the average PAE as the modulator is, in this case, part of the measurement system itself, and is not designed or intended

to offer high efficiency operation.

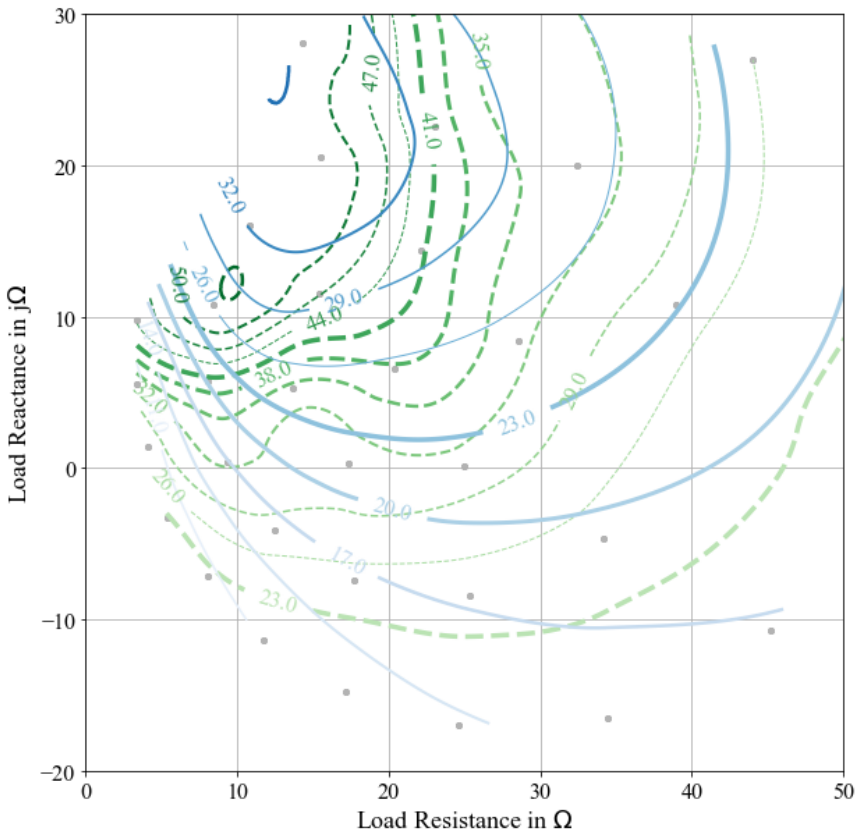

Figure 6.4 Average PAE for 28 V Fixed Bias (blue solid contours) and for ET (green dotted contours)

6.4 Shaping Function Trajectories

The device was characterised statically with power sweeps for different drain voltages from 10 V to 28 V in 0.5 V steps at an optimum impedance for Pout, while the gain was measured and shown in Figure 6.5. This measurement clearly shows a gain variation with applied drain supply voltage, a behaviour prevalent in many GaN HEMTs as shown in [10]. Three different tracking trajectories or shaping functions were designed that demonstrate the usefulness of the integrated system as

demonstrated in [11]. These trajectories are i) ***Iso-Gain*** to achieve flat gain, and thus good AM-AM linearity [12], ii) ***Opti-PAE*** which tracks the highest efficiency and iii) a trajectory termed ***Trade-off***, that aims to achieve a good compromise between linearity as shown in Figure 6.5 and efficiency as shown in Figure 6.6.This ***Trade-off*** function could be modified based on the design requirements.

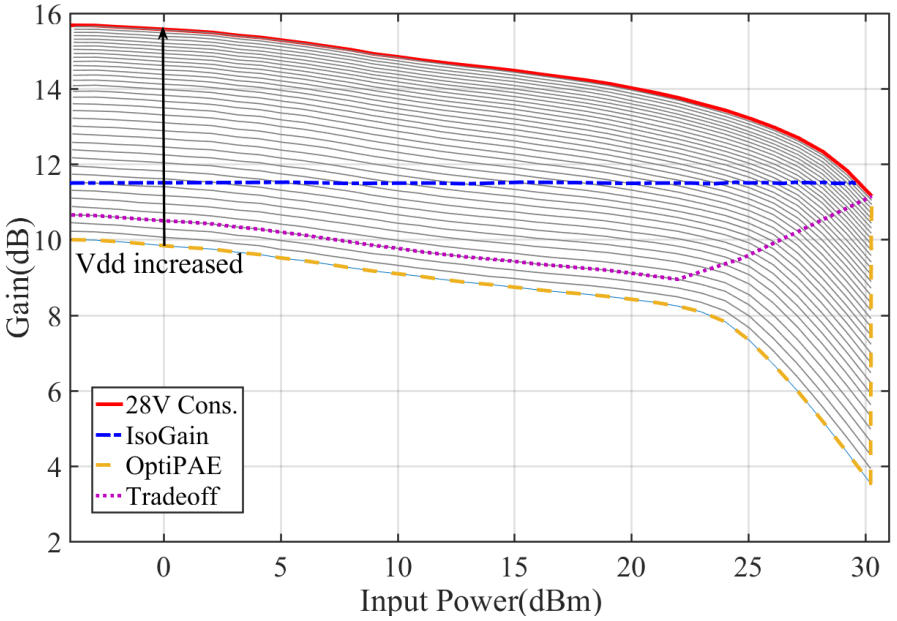

Figure 6.5 CW gain measurement at Zopt for static drain voltage from 10 V to 28V in 0.5 V steps shown as grey lines, with the three different trajectories and the static DC

The gain achieved for the three LUT shaping functions under ET emulation at optimum output impedance for the 10 W GaN device using 10 MHz LTE signal is shown in Figure 6.7. The efficiency and linearity of the three shaping functions was evaluated using 10 MHz LTE, 6.8 dB PAPR at fc = 2 GHz. The peak output power was maintained the same for the three cases. The spreading at lower input powers is almost completely down to the envelope delay between input and output modulation envelopes [13].Importantly, there is a good agreement between the extracted CW

trajectories shown in Figure 6.5 and the gain behaviour presented in Figure 6.7.

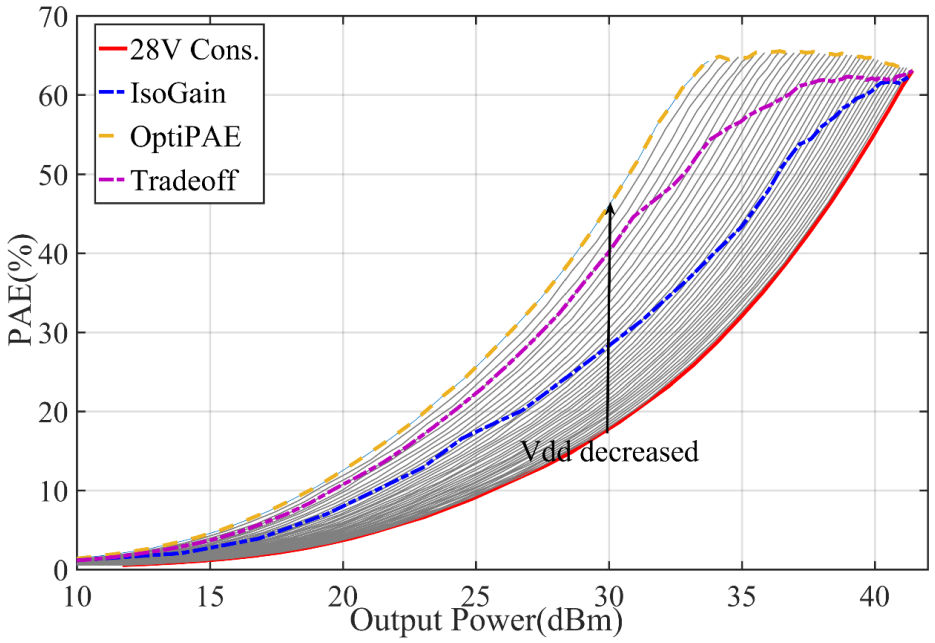

Figure 6.6 CW PAE measurement at Zopt for static drain voltage from 10 V to 28V in 0.5 V steps shown as grey lines, with the three different trajectories and the static DC

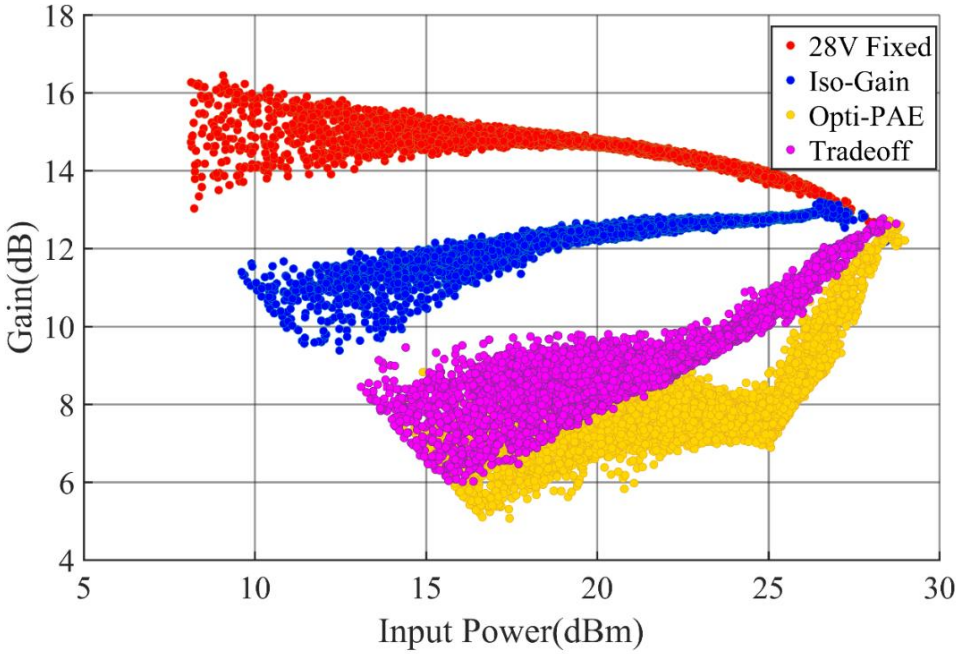

Figure 6.7 Measured dynamic signal gain for the three trajectories investigated, as well as the static DC case

Table 6–1 shows a comparison between the three trajectories in terms of average PAE and linearity including in-band distortion (EVM) and out-band distortion (ACPR), where it is clear that there is an enhancement in PAE for all three trajectories compared to the 28 V fixed bias case. However, the Iso-Gain shaping function achieves only an average PAE of 40.9% which is 7 percentage points lower than the Trade-off shaping function and 10 percentage points lower than that of the Opti-PAE function. In terms of linearity, Iso-Gain achieves good performance with a measured EVM of 2.9% and an ACPR of -36.6 dBc. Trade-off and Opti-PAE cases are worse, with an EVM of 11.3% and 14.0% and measured ACPR of -27.0 dBc and -24.1dBc respectively.

Table 6-1 Comparison of ET measurement at Zopt using different trajectories with a fixed drain supply of 28 V.

Biasing Method	**$P_{out,peak}$ (dBm)**	**PAEaveg* (%)**	**EVM (%)**	**EVM+DPD (%)**	**ACPR (dBc)**	**ACPR+DPD (dBc)**
28 V Fixed	41.1	29.0	2.3	0.65	-35.5	-52.6
Iso-Gain	41.1	40.9	2.9	0.75	-36.6	-54.2
Tradeoff	41.1	47.9	11.3	2.2	-26.9	-41.1
Opti-PAE	41.2	50.1	14.0	5.9	-24.2	-30.87

*The efficiency of the linear modulator is not included in the PAE_{aveg}

6.5 Applying Digital Predistortion

To demonstrate the novel capabilities of the system, fundamental load pull, dynamic tracking and a generalised memory polynomial (GMP) DPD with order of 3 and memory depth of 5 were simultaneously used to explore trade-offs and optimise the efficiency, power, and linearity of the emulated power amplifier under test. The power spectral density for the three trajectories before and after applying DPD is displayed in Figure 6.8. Without DPD, the Iso-Gain trajectory clearly achieves the best linearity with ACPR of -36.6 dBc.

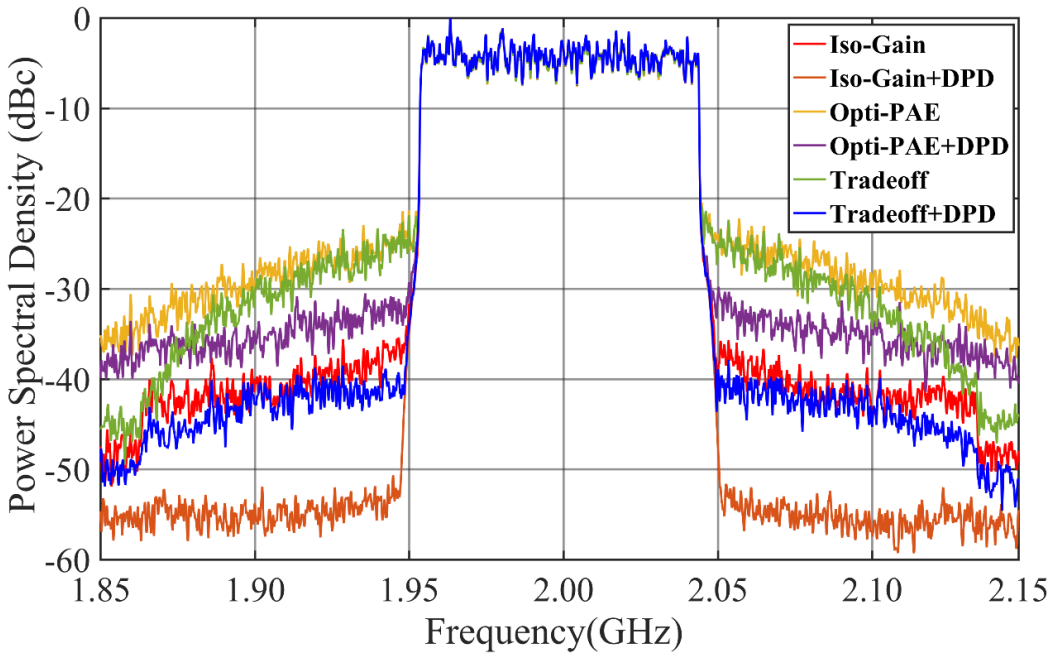

Figure 6.8 Measured power spectral density of the output signal before and after applying DPD for the three different shaping functions

The linearity for both Opti-PAE and Trade-off is degraded however to -24.2 dBc and -26.9 dBc respectively. After applying DPD, the ACPR for both Iso-Gain and Trade-off trajectories reduce to -54.2 dBc and -41.1 dBc respectively. However, the DPD

algorithm used struggles to Linearise the nonlinearity introduced by the Opti-PAE with only -30.8 dBc ACPR achievable.

6.6 Chapter Summary

This chapter presents the novel integration of broadband modulated rapid load pull, ET characterisation and DPD into a single, combined system where all elements operate simultaneously. Experimental results show a good agreement between predictive CW static measurements, and that that achieved when using ET, and confirm the capability of the system to precisely apply both load pull and ET simultaneously. The measurements of a 10 W GaN HEMT device further demonstrate the advantages of the system, showing that with DPD, it is possible to use a less linear shaping function and still get good efficiency and good linearity. Even though the Iso-Gain trajectory provides lower efficiency, it achieves good linearity performance without DPD, so a good option if DPD is not available. The result also presents the interesting idea of using such a system to rapidly optimise an ET-PA, for example, using different shaping functions for other emulated PA types. The measurements show that this emulation system can be utilised in ET-PA design to completely characterise the device in realistic modulated and impedance conditions, as a way of investigating design space for ET.

6.7 Reference

[1] V. Camarchia, M. Pirola, R. Quaglia, S. Jee, Y. Cho and B. Kim, "The Doherty Power Amplifier: Review of Recent Solutions and Trends," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 2, pp. 559-571, Feb. 2015.

[2] Z. Popovic, "GaN power amplifiers with supply modulation," 2015 IEEE MTT-S International Microwave Symposium, Phoenix, AZ, 2015, pp. 1-4.

[3] B. Kim et al., "Push the Envelope: Design Concepts for Envelope-Tracking Power Amplifiers," in IEEE Microwave Magazine, vol. 14, no. 3, pp. 68-81, May 2013..

[4] M. Hashmi, A. Clarke, J. Lees, M. Helaoui, P. Tasker, and F. Ghannouchi, "Agile harmonic envelope load-pull system enabling reliable and rapid device characterisation," Measurement Science and Technology, vol. 21, no. 5, pp. 055109, 2010.

[5] F. M. Ghannouchi and M. S. Hashmi, "Load-pull techniques and their applications in power amplifiers design (invited)," 2011 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Atlanta, GA, 2011, pp. 133-137.

[6] T. Williams, B. Wee, R. Saini, S. Mathias and M. V. Bossche, "A digital, PXI-based active load-pull tuner to maximize throughput of a load-pull test bench," 83rd ARFTG Microwave Measurement Conference, Tampa, FL, 2014, pp. 1-4.

[7] S. Alsahali et al., "A Novel Modulated Rapid Load Pull System with Digital Pre-Distortion Capabilities," 2019 93rd ARFTG Microwave Measurement Conference (ARFTG), Boston, MA, USA, 2019, pp. 1-4.

[8] Rohde & Schwarz, "Envelope Tracking and Digital Pre-Distortion Test Solution for RF Amplifiers," Tech. Rep., 2017.

[9] J. Couvidat, G. P. Gibiino, G. Pailloncy, M. Vanden Bossche, A. Ghiotto and D. Schreurs, "A compact measurement set-up for envelope-tracking RF PAs with calibrated sensing of baseband V/I at the supply terminal," 2015 86th ARFTG Microwave Measurement Conference, Atlanta, GA, 2015, pp. 1-4.

[10] A. Alt et al., "Analysis of Gain Variation With Changing Supply Voltages in GaN HEMTs for Envelope Tracking Power Amplifiers," in IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 7, pp. 2495-2504, July 2019.

[11] M. R. Duffy, G. Lasser, M. Olavsbråten, E. Berry and Z. Popović, "Efficient Multisignal 2–4-GHz Power Amplifier With Power Tracking," in IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 12, pp. 5652-5663, Dec. 2018.

[12] G. Wimpenny, "Understand and characterise envelope-tracking power amplifiers," EDN-Electronic Design News, vol. 57, no. 9, pp. 41, 2012.

[13] J. Lees et al., "Demystifying Device related Memory Effects using Waveform Engineering and Envelope Domain Analysis," 2008 38th European Microwave Conference, Amsterdam, 2008, pp. 753-756.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

The four objectives of this Ph.D. thesis have been successfully achieved. In particular, several measurement and characterisation techniques for ET-PA have been presented, including the realisation of a measurement system for ET-PA characterisation and the introduction of a novel system that integrates modulated active load pull and ET measurement with digital pre-distortion (DPD) capabilities into a single system. This research has also used this realised ET measurement system to study the effect of voltage ripple produced by the supply modulator on the linearity of ET-PA. The key contribution of each chapter is summarised below:

The first contribution of this thesis is the realisation of a measurement system for ET-PA, as presented in Chapter 3. The essential requirements for the ET measurement system were reviewed at the beginning of this chapter. Then, the measurement set-up, including the NI PXI chassis which is used for signal generation and measurement, the linear amplifier, the RFPA and a sensor circuit to measure the instantaneous drain current and voltage, was outlined. A 10 MHz LTE signal was used to characterise the ET measurement system while all the crucial requirements for the ET system were validated. The time alignment between the RF signal and the tracking signal was characterised, which shows the system has the ability to align the two signals. The instantaneous drain efficiency (DE) measurement showed that the

essential features of ET were realised and agree with the predictive static measurements. In addition, it was shown that the DE was maintained at around 50% over a 4.9 dB OBO – a clear indication that ET was working as expected. The degradation in the AM-AM and AM-PM distortions of the RFPA were compensated for by applying DPD, which proves that the capabilities of the available DPD algorithms are acceptable for the work planned.

In Chapter 4, the interaction between RFPA and supply modulator in the presence of output ripple was studied, which is the second major novel contribution. The theoretical effect of the output ripple on the linearity of the ET-PA was presented and verified with measurements that show degradation in the linearity as the ripple amplitude increases. The knee region interaction can be reduced by reshaping the drain bias voltage tracking signal, which recovers the linearity performance, although at a predictable cost to the efficiency. The DPD linearisation performance is limited when a significant non-coherent output ripple is present, which is because of the unpredictable nature of the interaction between the load line and knee region. These types of investigations can allow ET-PA and supply modulator designers to gain an insight into the amount of ripple that is tolerable, while still being able to realise linearity, linearisability and efficiency targets.

In Chapter 5, the third contribution of this thesis has successfully been achieved by presenting a novel system that is able to load-pull the device and apply DPD simultaneously. The measurements validate the ability of the system to precisely maintain load impedance over both a wide dynamic range and modulation bandwidth. The raw measured ACPR and output power contours of a 10 W GaN HEMT

device have indicated very different optimum impedances without DPD. However, after applying DPD, the contours of ACPR move to align with the output power contours. Thus, targeting the impedance for maximum output power is better when designing RFPAs if DPD is available. Such a system allows RFPA designers to fully characterise the device under realistic modulated and impedance conditions.

The fourth novel contribution of this thesis has been successfully realised in Chapter 6 by realising a novel measurement system that can fully emulate ET. The good agreement between predictive CW static measurements and ET measurements validates the ability of the system to accurately apply both load-pull and ET at the same time. The capabilities of the system were shown by investigating the linearity and efficiency performance of three distinct shaping functions, with and without DPD. The measurement setup enables ET-PA designers to rapidly optimise an ET-PA, for instance, by utilising different shaping functions for other emulated PA types.

7.2 Future Work

Even though the research presented in this thesis has demonstrated various new measurement techniques for ET characterisation, there are numerous prospective research areas that can be further explored.

100 MHz Supply Modulator with Integrated Current Sensor:

A wideband supply modulator is needed for ET characterisation, as a reference supply modulator to support 5G systems and beyond bandwidth requirements. Thus, the bandwidth of the current supply modulator should be extended to at least 100 MHz. Also, designing a wide bandwidth current sensor to measure the instantaneous

drain current should be considered and integrated with the supply modulator to reduce any parasitic effects, which might impact the generation of the tracking signal and degrade the efficiency measurement.

Baseband Impedance termination:

In Chapter 5, it was mentioned that the linearity performance of a transistor strongly depends on the impedance that the transistor sees at the baseband frequencies. Therefore, the baseband impedance was terminated to a short using a variety of capacitors. However, the baseband terminated could be completely synthesised by implementing specific shaping functions that act to completely terminate the baseband impedance.

Second & Third Harmonics Load Pull:

In Chapter 5 and Chapter 6, the measurement systems presented cover only the fundamental load pull frequencies. However, in order to fully investigate the potential of the new measurement architecture, the other harmonics including the 2nd and 3rd harmonic, which are significant to characterising a highly efficient PA mode, should be added. Thus, it would be possible to extend the load pull measurement to cover the 2nd and 3rd harmonics' load pull, and as a result explore for example, how continuous mode PA architectures within an ET environment respond to simultaneous ET linearising shaping functions and DPD.

Advanced DPD Implementation:

As the ET measurement system uses only standard DPD algorithms, advanced and more sophisticated DPD algorithms could be implemented to fix the high degree of nonlinearity of the RFPA. The new DPD algorithms could, for example, be used to recover the voltage ripple effect which was presented in Chapter 4.

On-wafer Measurement:

The measurement system presented in Chapter 5 and Chapter 6 could be modified easily to perform the measurement on-wafer instead of test fixture. On-wafer measurements could be used within a volume semiconductor processing environment for example to verify that fabrication was completed acceptably and yield was good. Even though it is possible to use de-embedding techniques, these can introduce additional uncertainties. Also, the bare die characterisation supports investigating the effect of packaging, which help to reduce packaging costs. Moreover, automated wafer testing could increase the measurement speed and reduce development costs.

Extend the Bandwidth of the Rapid Load Pull System:

In Chapter 5 and Chapter 6, the bandwidth of the rapid load pull system was shown to be limited to 40 MHz. However, a 5G system will require a substantial improvement in the bandwidth up to at least 100 MHz to fully characterise the nonlinearity of RFPA, which requires at least five times the modulation bandwidth. Thus, the bandwidth extension the work which has been started should be continued.