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Inversion Boundary Annihilation in GaAs Monolithically Grown on On-Axis Silicon (001)

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Monolithic integration of III–V materials and devices on CMOS compatible on-axis Si (001) substrates enables a route of low-cost and high-density Si-based photonic integrated circuits. Inversion boundaries (IBs) are defects that arise from the interface between III–V materials and Si, which makes it almost impossible to produce high-quality III–V devices on Si. In this paper, a novel technique to achieve IB-free GaAs monolithically grown on on-axis Si (001) substrates by realizing the alternating straight and meandering single atomic steps on Si surface has been demonstrated without the use of double Si atomic steps, which was previously believed to be the key for IB-free III–V growth on Si. The periodic straight and meandering single atomic steps on Si surface are results of high-temperature annealing of Si buffer layer. Furthermore, an electronically pumped quantum-dot laser has been demonstrated on this IB-free GaAs/Si platform with a maximum operating temperature of 120 °C. These results can be a major step towards monolithic integration of III–V materials and devices with the mature CMOS technology.

1. Introduction

Driven by the rapid development of smartphones, cloud computing and the Internet of Things, the unprecedented growth of worldwide data traffic significantly increases the demand of ever-higher data transmission speeds in data centers. A CMOS-process compatible Si-based photonic integrated circuits (PICs), would attract extensive scientific and industrial interest as it offers a low-cost solution for high-speed interconnects for data transmission. The integration of high-quality direct-bandgap III–V lasers on Si platform is a core technology for achieving high-performance Si-based III–V optoelectronic devices,[1–3] due to the inefficient light-emitting properties of Group-IV materials.[4,5] Currently, the realization of III–V lasers on Si mainly relies on either wafer bonding or monolithic growth techniques, with the latter method being more favorable for low cost, high yield and large-scale production.[6,7] Nevertheless, the large lattice mismatch, different polarities and incompatible thermal expansion coefficients between III–V materials and Si induce various crystal defects during the epitaxial growth such as threading dislocations (TDs), inversion boundaries (IBs, often called anti-phase boundaries, APBs), and micro-cracks.[8–13] These defects act as non-radiative recombination centers and significantly hinder the performance of optoelectronic devices in terms of lifetime, threshold operating power and temperature performance.[2,7,14] Approaches including strained-layer superlattice (SLS) acting as a defect filter layer (DFL) and a longer cool-down period after growth were implemented to sufficiently suppress TDs and micro-cracks, respectively.[12,13,15] By contrast, IBs are electrically charged planar

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defects arising from the epitaxial growth of polar III–V compound semiconductor materials on non-polar Si substrates. The IBs are nucleated at the edge of single-atomic-height (*S*) Si steps while their nucleation is prevented on the double-atomic-height (*D*) Si steps.[9,13] To avoid the formation of IBs, the conventional strategy employs Si (001) substrates with 4–6° offcut towards [110] or [111], which promotes stable *D* steps after high-temperature annealing.[16,17] However, this strategy is incompatible with CMOS technology, which strictly requires nominal on-axis Si (001) substrates.[18]

Until now, great efforts have been made to develop epitaxial growth techniques for IB-free III–V materials on on-axis Si (001) substrates including the implementation of V-groove patterned Si substrate,[19–21] template-assisted selective epitaxy (TASE),[22,23] III–V nano-ridge engineering[24,25] and high temperature annealing of Si substrate under hydrogen ambient environment by using metal organic chemical vapor deposition (MOCVD) systems.[26–28] With the aid of high temperature and high-pressure hydrogen, the epitaxial growth of IB-free GaP and GaAs on *D*-dominated Si has achieved great success. However, these methods require hydrogen gas and Si substrates with intentionally selected offcut angles (0.15° and 0.12° for the growth of GaAs/Si and GaP/Si respectively) to promote the formation of dominated *D* steps while few *S* islands remain at the step edge.[26,28–30] IBs that only arise from these few *S* islands remain low density and intersect pairwise during the subsequent high temperature layer growth, leading to sufficient IBs self-annihilation. Those methods are incompatible with solid-source molecular beam epitaxy (MBE) growth, due to lack of hydrogen source. On the other hand, the MBE system is superior in developing high-quality InAs/GaAs quantum dot (QD) lasers, which have been proved as an important laser source for Si photonics due to its robustness and high-quality performance. The achievement of fully MBE grown IB-free III–V buffer layer on on-axis Si (001) is thus highly desirable. Recently, researchers have successfully grown III–V lasers on on-axis Si (001) by MBE using high-temperature annealing and an $Al_{0.3}Ga_{0.7}As$ nucleation layer.[31] However, the mechanism of IB annihilation during growth is not clear, and the critical growth parameters remain uncertain.

In this work, we demonstrate a growth method of IB-free GaAs layers on on-axis Si (001) with periodic *S* steps by high-temperature annealing of Si buffer within the MBE system. The impact of an annealed Si buffer layer on the propagation of IBs is extensively studied. A sufficient self-annihilation of IBs during GaAs growth to achieve IB-free GaAs within 1 µm thickness grown on on-axis Si (001) substrates was demonstrated. Furthermore, a 1.3 µm InAs/GaAs QD laser was grown on the IB-free GaAs/Si substrate, with a low threshold current density of 83.3 A cm^{-2} and a high operating temperature of 120 °C.

2. Results

2.1. Epitaxial Growth, Surface Morphology of III–V Materials on On-Axis Si Substrates

Three samples (A–C) were first studied, which were grown on microelectronic standard on-axis Si (001) substrates with random miscut angles within 0.15° ± 0.1° toward [110] orientation by solid-source MBE system. All the Si (001) substrates used in this paper were not intentionally selected before epitaxy. In sample A, pre-growth heat treatment within the MBE growth chamber was performed before growing a 1 µm thick GaAs layer, and the (Al)GaAs growth follows the method demonstrated by Kwoen et al.[31,32] The deoxidized Si (001) substrate was heated up to ≈1200 °C for 30 min to enable the formation of *D* steps on the Si surface, which were believed to be the key to suppress the IB nucleation at the GaAs/Si interface.[9,33] However, no 2 × 1 RHEED pattern was observed during the heating process and a high density of IBs was observed on the surface of the subsequently grown GaAs layer, as shown in the top-view of scanning electron microscope (SEM) image of **Figure 1**a. The visible deep trenches on the SEM image illustrate the location of IBs since material evaporate easier on IBs due to week bonding than normal III–V crystal.[30,34] Therefore, we further optimized the growth method by employing a three-step 1 µm GaAs growth for Sample B, a 250 nm GaAs nucleation layer was first grown at a low temperature (LT) of 350 °C on the deoxidized Si (001) substrate, followed by a deposition of another 250 nm GaAs layer at a mid-temperature (MT) of 420 °C. Finally, a 500 nm GaAs layer was grown at a high temperature (HT) of 580 °C to finish the growth. A notable reduction of IB density is observed in Figure 1b and most of the IB are closed loops. Even though the material quality has been significantly improved, the IBs are still visible after the 1 µm GaAs growth. To improve the quality of Si epi surface before GaAs growth, a 200 nm Si buffer layer is grown and then annealed inside MBE chamber at 1200 °C for Sample C,[33] followed by an identical growth procedure of GaAs as Sample B. Figure 1c shows IB-free GaAs surface for Sample C. These results clearly indicate that the annealed Si buffer plays

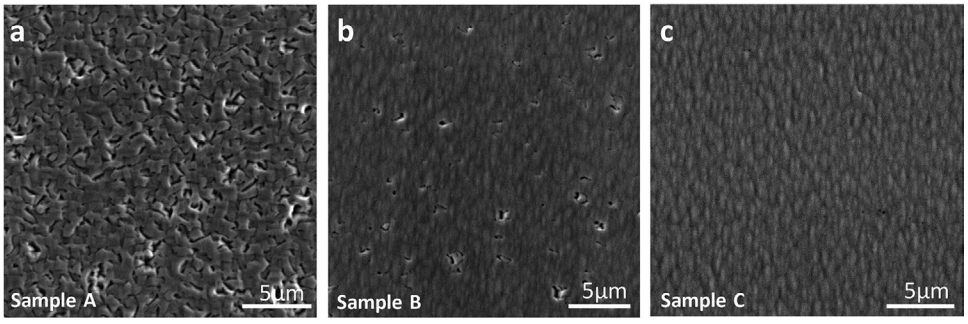

Figure 1. Top-view SEM images of 1 µm GaAs grown on on-axis Si (001) by different growth methods: a) sample A, b) sample B, c) sample C.

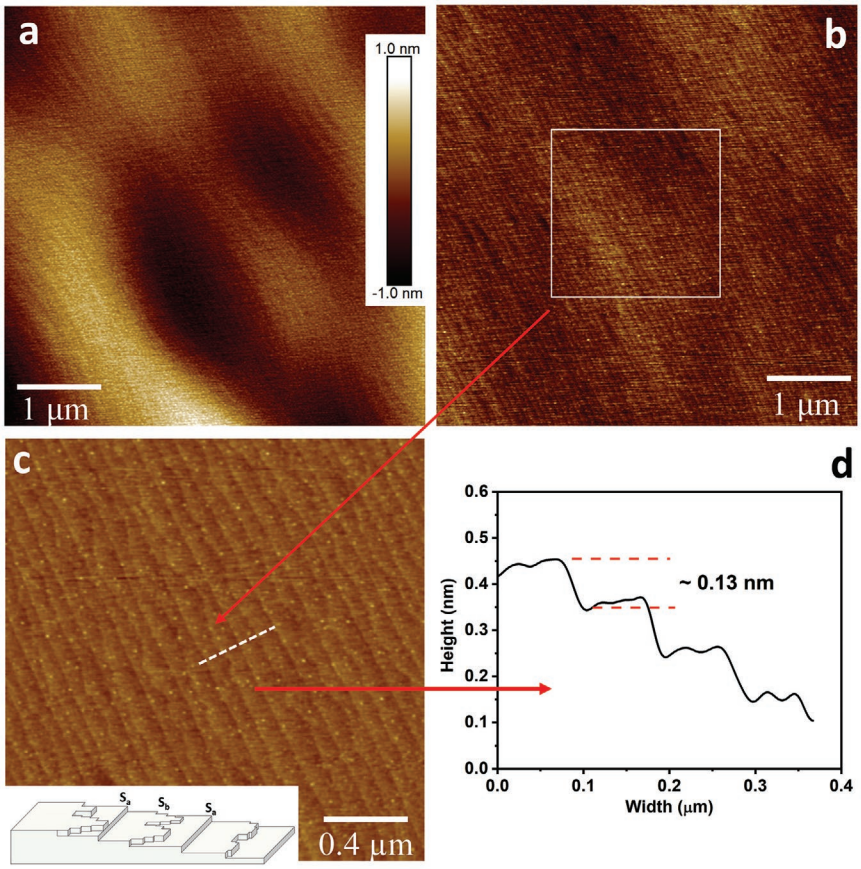

Figure 2. 5 μm × 5 μm AFM images showing surface morphology of Si surface. a) Si surface after 30 min deoxidation. b) Surface of 200 nm Si buffer layer. c) 2 μm × 2 μm AFM image of Si buffer layer surface showing alternating *S* step pairs; inset: schematic diagram of two *S* steps where S_b is meandering when compared with straight S_a. d) Height measurement of each step on the surface of 200 nm Si buffer.

an important role for the annihilation of IBs for GaAs growth on on-axis Si (100) substrates.

To understand the mechanism by which the annealed Si buffer causes IB annihilation, the surface morphology of Si substrates without and with the annealed Si buffer layer was compared through atomic force microscopy (AFM). AFM images of Si surfaces after deoxidation and after the annealed Si buffer layer are shown in **Figure 2**a,b, respectively. For the deoxidized Si surface, a random atomic-step distribution is obtained without a clear step order, as presented in Figure 2a. The formation of these wavy steps is a result of the interaction between different stress domains, which helps to reduce the net elastic energy of the Si surface at small offcut angle.[35,36] In contrast, clearly ordered Si steps are visible in Figure 2b, and a zoomed-in measurement of those ordered Si steps is presented in Figure 2c, showing a combination of alternating straight and meandering Si atomic steps.[16,37] The height of each step was measured around 0.13 nm, as shown in Figure 2d, revealing the existence of only *S* steps instead of the *D* steps after the high-temperature annealing on Si buffer process.[38–41] It is well established that on-axis Si (001) surfaces, which have small offcut angle, exhibit terraces of alternating 2 × 1 and 1 × 2 dimerization separated by two types of *S*.[16,37,42] Based on Chadi's nomenclature, these two step types are denoted as S_a and S_b.[43] S_b steps are relatively rough while S_a steps are straight, as shown in the schematic diagram in the inset of Figure 2c. Each meandering S_b step, which is due to the thermal fluctuation, is sandwiched between two neighboring S_a steps, as shown in Figure 2c. The offcut angle of the used on-axis Si (001) substrate thus can be determined from

$$\frac{a}{L} = \tan\theta \tag{1}$$

where θ relates to the surface misorientation of Si substrate, a represents the theoretical height of *S* step which is 0.136 nm, and L shows the half terrace width of neighboring S_a steps, which is around 80 nm obtained in Figure 2d. The offcut angle representing this terrace width is thus calculated as <0.1°, which is clearly within the typical misorientation range of on-axis Si (001) substrates. The offcut angle of on-axis Si (001) substrates is not intentionally selected before growth. Considering the unavoidable offcut introduced during the cutting process of Si (001) ingot, the parallel *S* step is achievable for on-axis Si (001) substrates with random offcut angle within 0.15° ± 0.1° towards [110] orientation. To investigate the nucleation and the propagation of IBs within GaAs grown on (S_a + S_b) arrays, a cross-sectional annular dark field scanning transmission electron microscope (ADF-STEM) measurement was

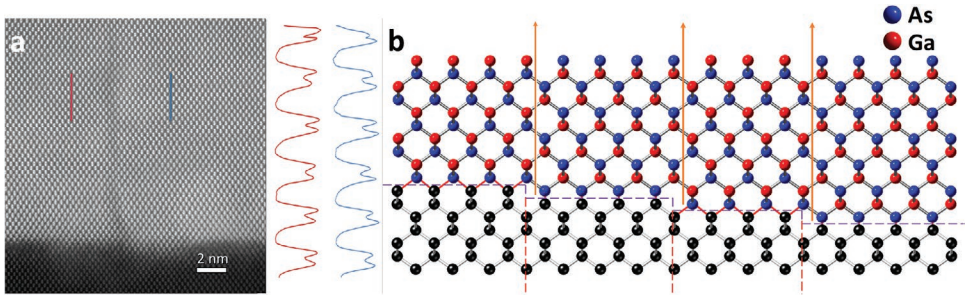

Figure 3. Nucleation of GaAs on Si array. a) ADF-STEM image showing the initial nucleation of IB at a *S* step. The red and blue profile lines show the intensities of the atoms, which appear in pairs (a "dumbbell") in this [110] projection. As is slightly brighter due to its higher atomic number and is on the top of the dumbbell on the left of the IB and on the bottom of the dumbbell on the right. b) Schematic (110) diagram of initial nucleation of IBs on both S_a and S_b.

performed. As shown in **Figure 3**a, IBs are nucleated on the edge of the *S* steps and propagated at low temperature along an energy-favoured (110) plane.[44,45] The measured line profiles obtained from ADF-STEM image indicate the swapping of sublattices of Ga and As atoms across the boundary. Therefore, periodic IBs could be generated on the periodic *S* steps, where the distance between the neighbouring IBs directly relates to the terrace width, the distance between S_a and S_b, as shown in the schematic illustration in Figure 3b and confirmed later by the results shown in **Figure 4**. In addition, a relative high GaAs/Si interface roughness, as a result of Ga melt-back etching, is presented on the Figure 3a. The further improvement of GaAs/Si interface quality can be achieved by carefully controlling III–V on Si nucleation process and compensate any excess of Ga droplet before it etched the Si buffer layer.[46,47]

2.2. Characteristic Measurements of Inversion Boundaries

To further understand the mechanism of IB annihilation on the periodic Si atomic steps of (S_a + S_b) during GaAs growth, the growth of Samples B and C, without and with a Si buffer layer are studied in detail and layer by layer, respectively. The surface morphology at LT, MT and HT GaAs layers of Samples B and C are presented in Figure 4a–c and Figure 4d–f, respectively. A considerable number of nucleated curved IBs appear randomly after the LT GaAs layer is grown for Sample B, as illustrated in Figure 4a, which is consistent with the wavy Si atomic steps after deoxidation as shown in Figure 2a. An increase in the growth temperature for the further MT 250 nm GaAs layer enlarges the boundaries, despite a reduction of IBs density as observed in Figure 4b. Although the density of IBs is visibly lower after the growth of HT 500 nm of GaAs, as illustrated in

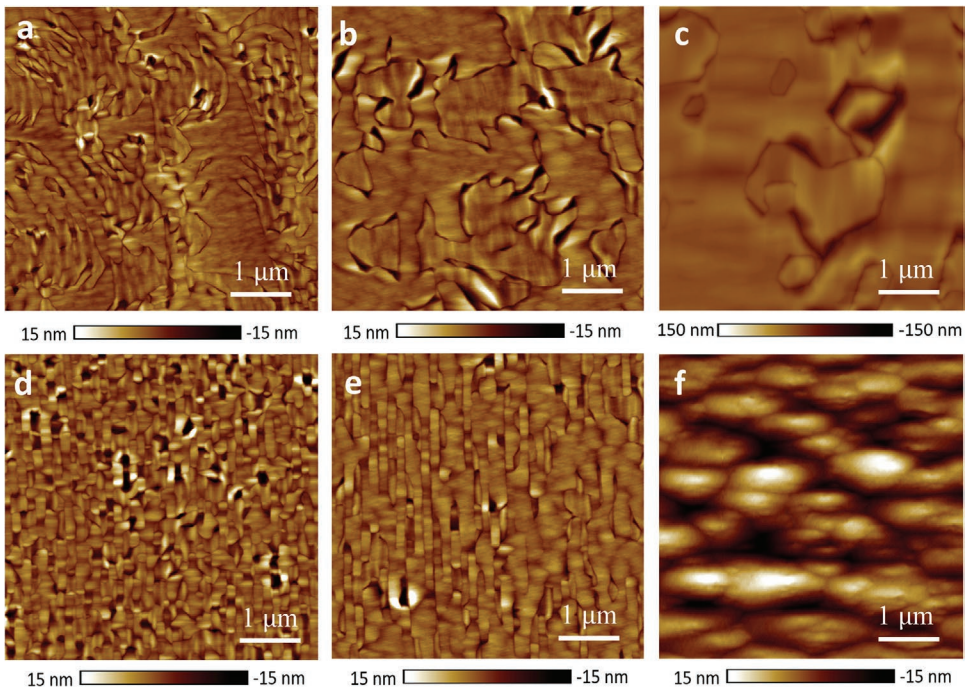

Figure 4. 5 μm × 5 μm AFM images showing annihilation of IBs at different stages. a) 250 nm, b) 500 nm, c) 1000 nm GaAs monolithically grown on deoxidized Si substrate. d–f) 5 μm × 5 μm AFM images of after d) 250 nm, e) 500 nm, f) 1000 nm GaAs grown on the Si buffer layer.

Figure 4c, the size of some IBs is significantly larger than the nucleated ones at LT GaAs, which severely lowers the crystal quality of the materials subsequently grown. These results indicate that full annihilation of the IBs is difficult to achieve for the sample B without annealed Si buffer layer.

By stark contrast, as shown in Figure 4d, well-organized periodic boundaries are observed in sample C after the deposition of the first 250 nm LT GaAs. The formation of these periodic boundaries is the result of IBs nucleated at the edge of periodic *S* steps during the deposition of the LT GaAs layer. The distribution of IBs reproduces the structure of periodic *S* steps, indicating the low temperature implemented for the nucleation layer growth is insufficient to kink IBs from {110} into higher index plane. This GaAs surface pattern is distinctive compared with the previously reported $Al_{0.3}Ga_{0.7}As$ nucleation layer.[31] The gaps between the separated IBs, are visible as dips. During the further growth of 250 nm MT GaAs, the dips are reduced in size and gradually annihilated and the density of IBs also becomes visibly lower, as shown Figure 4e. Finally, Figure 4f shows a single phase of GaAs on the surface, after the 500 nm HT GaAs is deposited. These results suggest that a fully IB-free GaAs surface was obtained after growth of 1 µm thickness of GaAs by utilizing the periodic (S_a + S_b) arrays on Si to promote IB annihilation, and with a relatively low root mean square (RMS) roughness of 4.9 nm.

Cross-sectional TEM measurements have been studied on the Samples B and C to further study the mechanism of IB annihilation by investigating the cross-sectional structural properties of GaAs-on-Si heteroepitaxy. The images were taken through two viewing directions, [110] (**Figure 5**a–d) and [1$\bar{1}$0] (Figure 5e–f). As shown in the dark-field TEM image of Figure 5a, the IBs nucleate through the (110) plane in Sample B in the LT GaAs layer. Subsequently, the IBs start to propagate along a higher index plane, such as {111}, {112} and {113} planes,[30] through the MT and HT GaAs layers. This enhances the probability of IBs' intersecting and annihilating with each other. The twisted patterns observed in Sample B, are due to the randomly distributed IBs nucleation. In contrast, periodic arrays of IBs are visible when GaAs was deposited on the annealed Si buffer layer in Sample C, as shown in Figure 5b. The distance between IB loops corresponds to the half-width of each Si terrace, the distance between S_a and S_b, which is approximately 80 nm in this case. The kinks of IBs are observed in the higher growth temperature region which leads to the annihilation of IBs when they meet. Stacking faults appear occasionally in the GaAs nucleation layer, as shown in the inset image of Figure 5b, without a visible impact on the IBs propagation. Figure 5c and Figure 5d present larger scale bright-field cross-sectional TEM measurements of Samples B and C, respectively. Despite most of the IBs self-annihilating during the growth in sample B, there are still some IBs that penetrate through the whole structure as seen from Figure 5c. Those remaining IBs propagate freely in three dimensions, making annihilation extremely unlikely once the density of IBs becomes lower. However, the IBs that nucleate on (S_a + S_b) arrays follow the shapes of both steps and annihilate within approximately 500 nm of GaAs growth. In addition, the IBs that penetrate through the whole structure can be observed from [1$\bar{1}$0] direction in Sample B, as shown in Figure 5e. In contrast, due to the formation of straight and parallel *S* steps towards [110] orientation, the periodic IB nucleation resembles the distribution of the (S_a + S_b) arrays, which are along (110) plane, leaving no observation of IBs from [1$\bar{1}$0] direction for Sample C, as shown in Figure 5f. This phenomenon is different from the observation in GaP/Si system, which has triangle-shaped *S* islands appear between engineered *D* steps, the resulting IBs formed on that remained triangle-shaped *S* islands reflect the Si surface structure and can be observed from both [110] and [1$\bar{1}$0] directions.[48] X-ray diffraction reciprocal space mapping (XRD-RSM) imaging was used to examine the residual strain inside the IB-free GaAs buffer layers as shown in the inset of Figure 5f. A full-relaxation line passes directly through the center of the patterns representing GaAs and Si, implying that no residual strain is present in the GaAs layers. The compact pattern of GaAs indicates a good crystal quality of the IB-free GaAs layer.

2.3. Performance Characterization of QD Laser on Si

To exploit the feasibility of using this IB-free GaAs layer as a platform for the integration of polar III–V optoelectronic devices on non-polar group IV substrates, a 1.3 µm InAs QD laser structure was monolithically grown on this GaAs/Si (001) platform. The bright-field TEM image demonstrates high quality of the InAs QD gain medium where no apparent TDs and IBs are observed in **Figure 6**a. Comparing room-temperature photoluminescence (PL) for the InAs QD material grown on our IB-free GaAs/Si (001) platform and those without the Si-array GaAs/Si (001) virtual substrate, the sample with annealed Si buffer shows four-fold improvement of PL intensity with a similar peak wavelength of ≈1288 nm, as shown in Figure 6b. The full width at half maximum of InAs QDs on IB-free GaAs/Si (001) is as low as ≈27.8 meV. An AFM image of uncapped InAs QDs grown on fully relaxed IB-free GaAs/Si (001) under the same growth conditions is shown in the inset of Figure 6b, where InAs QDs with a high density of 5.4×10^{10} cm^{-2} are present. A broad-area InAs QD laser was fabricated in order to assess the quality of our IB-free GaAs/Si (001) platform. Figure 6c shows the light–current (*L*–*I*) curves of the InAs QD laser under different operating temperatures. Room temperature threshold current density (J_{th}) is as low as 83.3 A cm^{-2}, which is better than the previously reported J_{th} for 1.3 µm InAs QD laser on an exact Si (001) substrate all grown by MBE.[14,32,49] Since robust temperature stability is necessary to support the Si based laser working in a high-temperature environment, the Si-based laser was tested at a range of operating temperatures. Lasing was observed under a pulsed mode with operating temperatures up to 120 °C. Moreover, the slope efficiency of the single-facet emission of 0.13 W A^{-1} at 20 °C remained stable as temperature increased, showing a good temperature reliability for the InAs QD laser on our IB-free GaAs/Si (001) platform. The room temperature electroluminescence (EL) spectra under different injection current densities are given in Figure 6d. Amplified spontaneous emission was observed below injection current density of 80 A cm^{-2}. When the injection current is increased above the threshold, the ground state lasing spectrum can be clearly observed with a peak wavelength at 1303.9 nm. The inset of Figure 6d shows a characteristic temperature (T_0) of ≈55 K between 20 and 100 °C. Based on these results, the 1.3 µm InAs QD laser grown directly on an

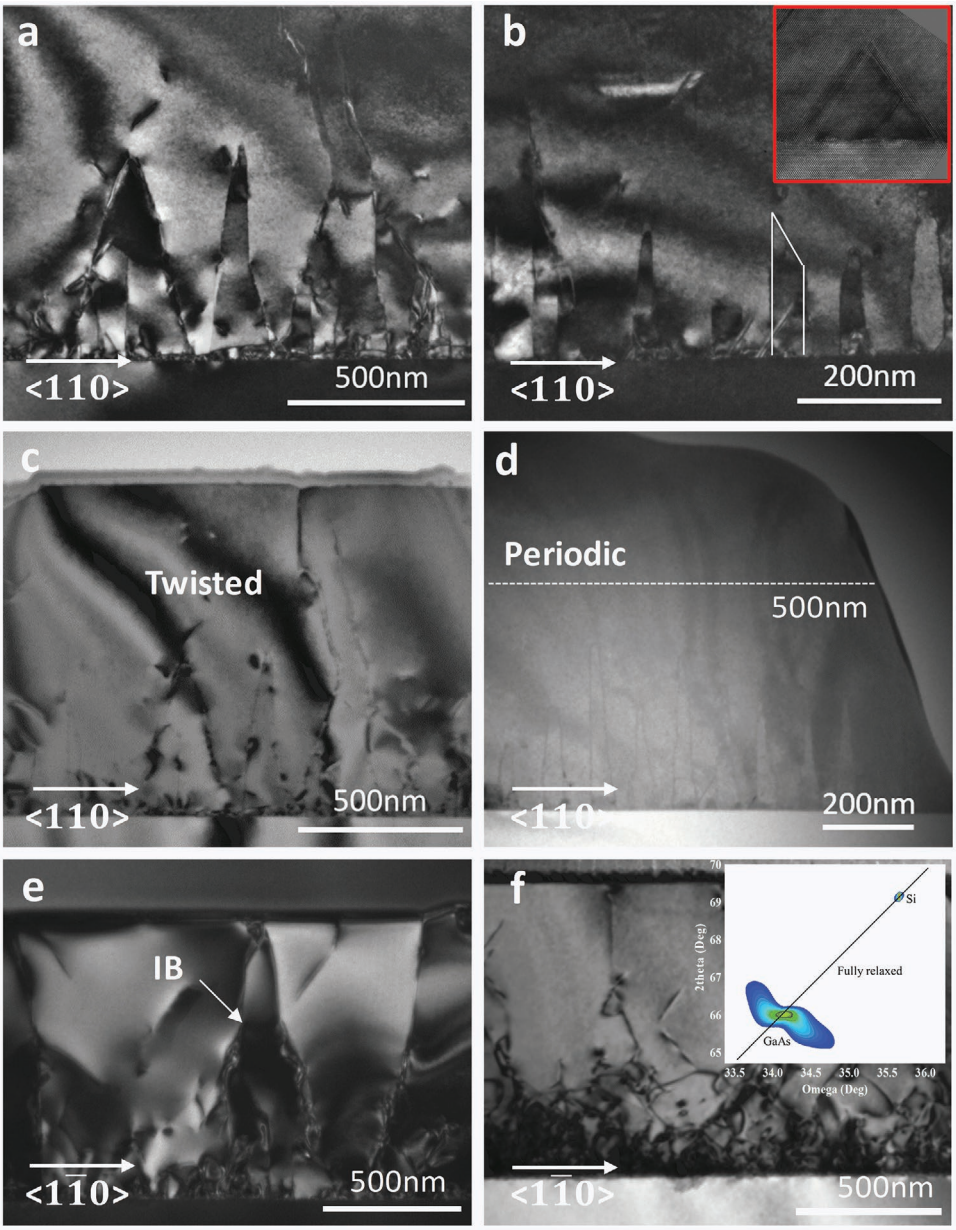

Figure 5. Cross-sectional TEM measurements of IB propagation and annihilation of sample B (without Si buffer) and sample C (with Si buffer). Dark field images with view direction of [110] for a) sample B, and b) sample C; Inset: a stacking fault at nucleation layer. Bright field images with view direction of [110] for c) sample B, and d) sample C. TEM images from viewing direction of [1$\bar{1}$0] for e) sample B, and f) sample C; inset: XRD-RSM image of fully IB-free 1 µm GaAs on on-axis Si (001) substrate.

on-axis Si (001) substrate using our IB-free GaAs virtual substrate demonstrated promising performance in terms of J_{th} and temperature stability.

3. Conclusion

In this paper, we demonstrated IB-free GaAs epilayers monolithically grown on CMOS compatible on-axis Si (001) substrates with periodic *S* Si steps only, instead of the conventionally used *D* Si steps in MOCVD systems. The detailed mechanism of IB annihilation within the GaAs buffer layer grown on periodic *S* Si steps of Si substrates has been studied by using AFM and TEM. After the deoxidation of Si substrates, a random atomic-step distribution without a clear step order is observed for Si epitaxial surface. During the growth of GaAs on Si, IBs within GaAs buffer are generated on the *S* Si steps on Si substrates. Curved IBs are thus formed randomly for GaAs grown Si substrates without annealed Si buffer layer and do not effectively annihilate within the 1 µm GaAs buffer layer. On the other hand, a periodic surface morphology—alternating straight S_a and meandering S_b single atomic steps—on the Si surface has been obtained for the sample with annealed Si buffer layer. During the deposition of GaAs layers, the IBs that

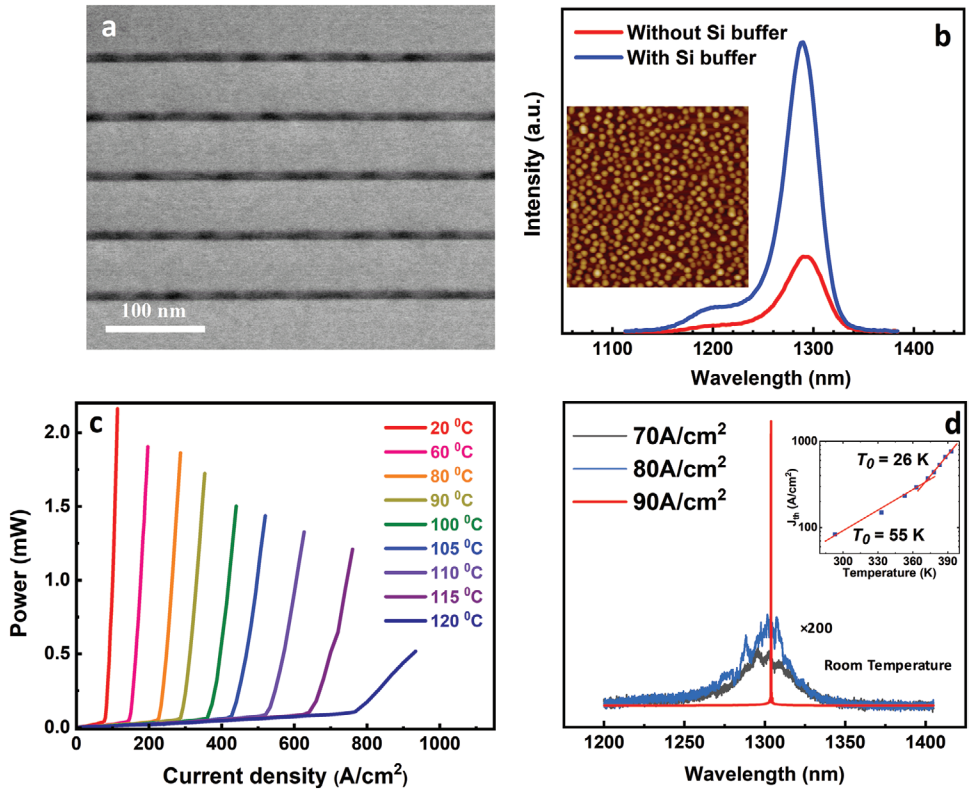

Figure 6. Characteristic measurements of QDs and the laser device. a) Bright-field cross-sectional scanning TEM image of 5 stacks of dot-in-well structure grown on on-axis Si (001). b) Room temperature PL spectra of QD samples grown on deoxidized Si substrates with and without Si buffer layer; inset: 1 μm × 1 μm AFM image of uncapped InAs QD grown on on-axis Si (001) with high dot density. c) Temperature dependent *L–I* curve up to 120 °C of 1300 nm InAs QD laser on on-axis Si (001). d) EL spectra of InAs QD laser on on-axis Si (001) substrate with different injection current density under pulsed mode; inset: Temperature dependence of the J_{th} revealing characteristic temperature T_0 of our laser sample.

nucleate on (S_a + S_b) arrays follow the shapes of both steps, and annihilate within approximately 500 nm GaAs. This approach simplifies growth requirements for a high-quality IB-free III–V platform on CMOS compatible Si (001). Using this GaAs buffer layer acting as a platform for the monolithic integration of III–V optoelectronics on CMOS compatible Si (001), a 1.3 μm InAs QD laser device with a low J_{th} of 83.3 Acm^{-2} at room temperature and highest operating temperature of 120 °C was successfully demonstrated. These results indicate that IBs will no longer be a fundamental issue for the monolithic integration of polar III–V on on-axis Si (100) substrates and form a basis of combing monolithic integration of Si photonics with mature CMOS technology.

4. Experimental Section

Material Growth: The epitaxial materials were grown by a special twin MBE system, consisting of a Group-IV and a III–V growth chamber. The deoxidation of Si substrates, and the growth and annealing of Si buffer layer were performed in the Group-IV chamber before transferring to the III–V chamber for III–V epitaxy. An ultra-high-vacuum transfer chamber between these two chambers was used to keep a pure and smooth Si epi surface before GaAs growth, to avoid potential contamination during the wafer transfer process. Phosphorus-doped on-axis Si (001) wafers with 0.15° ± 0.1° offcut towards [110] were used. In situ deoxidation process of substrates within the Group-IV chamber was performed at 1200 °C for 30 min. For Sample A, a 30 nm $Al_{0.3}Ga_{0.7}As$ nucleation layer with a growth rate of 0.7 monolayers per second (ML s^{-1}) was grown on the deoxidized Si (001) substrate at 500 °C followed by a 970 nm GaAs layer at 580 °C. In Sample B, a 250 nm GaAs nucleation layer was first grown around low temperature of 350 °C, followed by a deposition of another 250 nm GaAs layer around mid-temperature of 420 °C. Finally, a 500 nm GaAs was grown around high temperature of 580 °C to complete the growth. For Sample C, a 200 nm thick Si buffer layer was grown on the deoxidized Si (001) substrate by an e-beam Si source, consisting of a 100 nm of Si layer annealed at 900 °C followed by 5 periods of 20 nm Si layers annealed at 1200 °C. The GaAs growth sequence is the same as for Sample B. The InAs/GaAs QD lasers were grown on the virtual substrate grown using the procedure of Sample C. Si-doped InGaAs/GaAs defect filter layers (DFLs) have been grown after the GaAs layer to reduce the threading dislocation density, which consists of 5 repeats of InGaAs/GaAs superlattice and a 300 nm GaAs spacer layer, along with an in situ thermal annealing after each repeat.[50] After 3 repeats of DFLs, a five-layer dot-in-well structure was grown as the active region, sandwiched by two 1.5 μm N-type and P-type $Al_{0.4}Ga_{0.6}As$ cladding layers. Each layer of the InAs QDs was grown on a 2 nm $In_{0.18}Ga_{0.82}As$ layer and capped by a 6 nm $In_{0.18}Ga_{0.82}As$ layer followed by a 50 nm GaAs spacing layer. Finally, a 300 nm p-type GaAs contact layer was grown.

Device Fabrication: The broad-area lasers with 50 μm wide stripes were fabricated by standard lithography and wet chemical etching techniques. Ti/Pt/Au and Ni/GeAu/Ni/Au were deposited on p+ GaAs contacting layer and exposed n+ GaAs layer to form the p– and n– contacts, respectively. After lapping the silicon substrate to 150 μm, the lasers were cleaved to 3 mm lengths and mounted (as-cleaved) onto the heat-sink and wire-bonded.

Measurements: AFM measurements were performed with a Veeco Nanoscope Dimension 3100 under tapping mode. The PL measurements are performed with a RPM2000 PL at room temperature, excited by a 635 nm red laser. The TEM and STEM measurements were

performed on JEOL 2100 and doubly corrected ARM200F microscopes respectively, both operating at 200 kV. The fabricated laser was characterized under pulsed conditions with 1 µs pulses and 1% duty cycle. The output power of laser was collected from a photodetector normal to the laser facet.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

heteroepitaxy, inversion boundary, molecular beam epitaxy, quantum dot laser, silicon photonics

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