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ABSTRACT

A complementary–metal–oxide semiconductor (CMOS) compatible all-silicon TM-pass polarizer using plasmonic bends is proposed. To simplify the fabrication and be compatible with the CMOS process, we employ only two materials: silicon and silicon dioxide. Highly doped silicon is used to support the plasmons. We obtain an extinction ratio and an insertion loss of 45.4 and 1.7 dB, respectively, at 1550 nm and a maximum extinction ratio of 58 dB. This is the highest reported extinction ratio for a TM-pass polarizer to the best of our knowledge. Furthermore, we achieved >20 dB of extinction ratio and <2 dB of insertion loss over 72 nm bandwidth for a device footprint $<8.8 \times 5.4 \mu\text{m}^2$. To achieve this, we exploit the properties of tight bends in plasmonic waveguides. Another advantage of the device is that it is robust against fabrication variations.

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I. INTRODUCTION

Due to the complementary–metal–oxide semiconductor (CMOS) compatibility, large index contrast, and low-cost mass-production of components and systems, silicon photonics (SiPh) has drawn considerable research interest in the past decades.^{1–11} However, the large index contrast causes the silicon-on-insulator (SOI) platform to be highly polarization dependent, requiring polarization management schemes to maintain the performance of the SOI devices. To solve this issue, polarization diversity schemes are used.¹² A simpler solution for circuits that do not exploit polarization diversity is to use an integrated polarizer to suppress the unwanted polarization while retaining the desired one. To use the existing silicon mass production capabilities, many polarizers are designed using materials and processes compatible with the CMOS technology.

To date, several TM-pass polarizers have been reported in various configurations for different wavelengths of operation.^{13–17} Kim *et al.*¹³ demonstrated a TM-pass polarizer using a 1D photonic crystal based on a sub-wavelength structure achieving 34 dB of extinction ratio (ER) and around 1 dB of insertion loss (IL).

However, this structure is challenging to fabricate using the 193 nm deep ultraviolet (DUV) lithography, and it is highly sensitive to fabrication variations. Bai *et al.*¹⁸ reported a TM-pass polarizer using a hybrid plasmonic grating achieving an ER of 25 dB with an active length of $2.5 \mu\text{m}$. In this case, silver was used to form the plasmonic waveguide that is not CMOS compatible. Hu and Wang¹⁹ proposed a graphene-based TM-pass polarizer having a length of $150 \mu\text{m}$ that is prohibitive for dense integration. Furthermore, graphene is not suitable for mass production. A TM-pass polarizer based on the insulator-to-metal phase transition of vanadium oxide was proposed by Sánchez *et al.*²⁰ However, a critical temperature of 68°C is required to ensure the phase transition that makes it inefficient in terms of energy consumption compared to passive designs. A sub-wavelength grating (SWG) based TM-pass polarizer was reported in Ref. 21 obtaining 27 dB of ER and 0.5 dB of IL. However, this structure is challenging to fabricate using the 193 nm DUV process and is sensitive to tolerance variations. Therefore, most of the reported devices are not CMOS-compatible. It will be interesting to have a compact device by using only silicon and silicon dioxide that will exploit the current CMOS fabrication capabilities and simplify the fabrication.

In this paper, we report a broadband all-silicon hybrid plasmonic TM-pass polarizer on the SOI platform using plasmonic bend waveguides. Initial results were reported in a review paper.²² Herein, we present the simulation and analysis in detail. The TE and TM fundamental modes have different mode profiles and confinement in a rectangular silicon waveguide for a particular cross section geometry. In a bend waveguide, the TE and TM fundamental modes have different radiation losses depending on the geometry. By utilizing this phenomenon, one can design a pass polarizer by cascading different numbers of bends. ^{23,24} Such polarizers are easy to fabricate since the structures are simply bend waveguides and require only two materials: silicon and silicon dioxide. However, the required footprint is quite large for these kinds of polarizers, which increases the cost of the chip. Since plasmonics has the ability to control light at a much smaller dimension (beyond the diffraction limit of light), ^{25–27} it has been used to reduce the dimensions and footprint of many optoelectronic components. ^{28–31} We utilize plasmonic bends to improve the performance and reduce the footprint. To avoid using more materials and increase fabrication complexity, we will use highly doped silicon instead of metals reducing the complexity to two materials: silicon and silicon dioxide. While 220 nm thick silicon wafers are mostly used for device fabrication, it is not the optimum option for many on-chip components. ³² Consequently, there has been a growing interest in building components and systems on SOI wafers with thicker silicon device layers, especially the SOI platform with a 340 nm thick device layer. ^{33–36} The use of highly doped silicon instead of metal to ease the fabrication is an advantage over previous

designs that use vanadium oxide, graphene, and other non-CMOS compatible materials. The ER and IL at 1550 nm are 45.4 dB and 1.7 dB, respectively, and a maximum ER of 58 dB is obtained at 1572 nm. Additionally, the proposed polarizer exhibits $ER > 20$ dB and $IL < 2$ dB over 72 nm bandwidth with a device footprint $< 8.8 \times 5.4 \mu\text{m}^2$. The proposed TM-pass polarizer is robust against fabrication variations.

II. OPERATING PRINCIPLE

The TE modes are laterally confined, while the TM modes are vertically confined in a rectangular waveguide. Both modes are shifted toward the outer part of a rectangular waveguide in a small enough bend. The tighter the bend is, the more the displacement will be produced. However, the amount by which the TE mode is shifted outward is higher than that of the TM modes [shown in Fig. 1(a)]. Hence, by absorbing the deconfined TE modes using highly doped silicon waveguides placed on the sides of a silicon bend waveguide, a TM-pass polarizer can be obtained.

Figures 1(a) and 1(b) present the schematic and cross section of the proposed TM-pass polarizer based on bend waveguides, respectively. The polarizer consists of silicon waveguides and highly doped silicon. The highly doped silicon waveguides are placed on both sides of two consecutive bends of the waveguide to absorb the undesired mode (TE). The height of the silicon device layer is 340 nm and has a $2 \mu\text{m}$ thick silicon dioxide layer as the upper cladding and a $2 \mu\text{m}$ buried oxide layer. The radius of the silicon waveguide is denoted

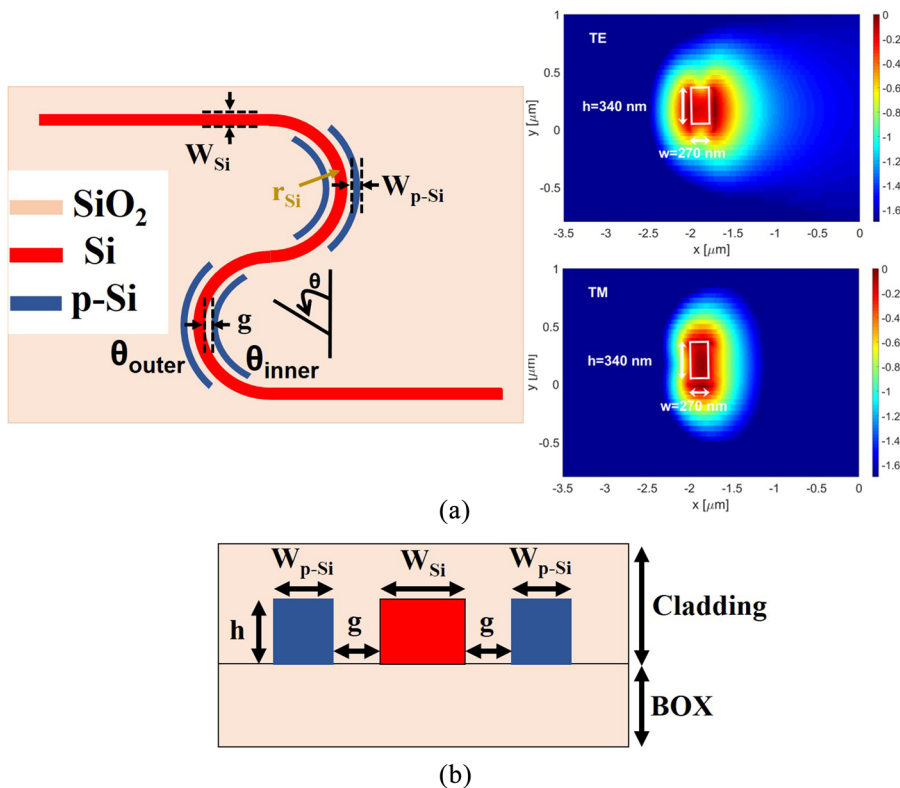


FIG. 1. (a) Schematic of the proposed TM-pass polarizer along with TE and TM mode profiles in a bend waveguide and (b) cross section of the TM-pass polarizer. Reproduced with permission from Saber *et al.*, IET Optoelectron. **14**(3), 109–119 (2019). Copyright 2019 The Institute of Engineering and Technology.

r_{Si} . In Fig. 1(a), W_{Si} and W_{pSi} denote the width of the silicon and the highly doped silicon waveguides, respectively, and the gap between them is denoted g . The start and end points of the highly doped bend waveguides are denoted θ_{inner} for the highly doped waveguide placed inside the silicon bend and θ_{outer} for the highly doped waveguide placed outside the silicon bend. The maximum and minimum values of θ_{inner} and θ_{outer} are 0° and 180° , respectively, which denote a half circle. The minimum and maximum values of θ will change when different bends are desired.

Highly doped silicon demonstrates metal-like properties since the real part of the complex relative permittivity becomes negative when the carrier concentration gets higher than roughly $4.55 \times 10^{20} \text{ cm}^{-3}$.¹⁷ For the proposed TM-pass polarizer, we considered a carrier concentration $10.5 \times 10^{20} \text{ cm}^{-3}$. Doped silicon with an active carrier concentration of $10.8 \times 10^{20} \text{ cm}^{-3}$ was demonstrated experimentally in the past.³⁷

A three-dimensional finite-difference time-domain (3D FDTD) solver from Lumerical³⁸ is used for the simulation. The complex relative permittivity of silicon and silicon dioxide is obtained from Ref. 39, while, for the highly doped silicon, the values are obtained using the Lorentz–Drude model in Eq. (2).

For low carrier concentration, refractive index variation of doped silicon is modeled using Soref's empirical relations.⁴⁰ However, the Lorentz–Drude model needs to be utilized for the complex relative permittivity modeling of highly doped silicon,⁴¹

$$\epsilon(\omega) = \left(\epsilon_\infty - \frac{\omega_p^2 \tau^2}{1 + \omega^2 \tau^2} \right) + i \frac{\omega_p^2 \tau}{\omega(1 + \omega^2 \tau^2)}, \quad (1)$$

where ω_p is the plasma frequency, τ is the electron/hole relaxation time, $\omega = \frac{2\pi c}{\lambda}$ is the angular frequency, ϵ_∞ is the infinite frequency relative permittivity, and c is the speed of light in vacuum. For highly doped degenerate intrinsic semiconductors, this relation can be simplified as¹⁷

$$\epsilon(\omega) = \left(\epsilon_\infty - \frac{\sigma}{\omega^2 \epsilon_0 \tau} \right) + i \frac{\sigma}{\omega^3 \tau^2 \epsilon_0}, \quad (2)$$

where ϵ_0 is the free space permittivity, $\sigma \approx eN\mu$ is the conductivity of the doped silicon, and e is the charge of an electron.

Figure 2 shows the carrier concentration dependence of the complex relative permittivity of highly doped silicon at 1550 nm. We considered $m_{eff} \approx m_0$, where m_0 is the mass of the electron and $\mu = 50 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.⁴² The zero crossing of the real part of the

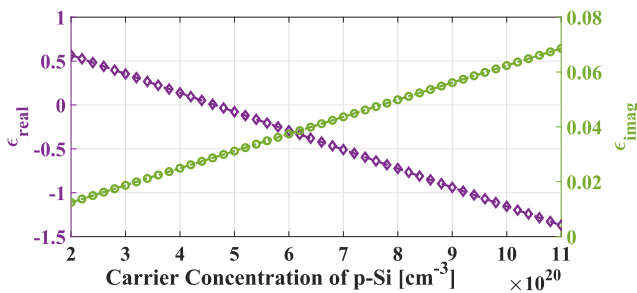


FIG. 2. Real and imaginary parts of the complex permittivity of the highly doped silicon as a function of the carrier concentration at 1550 nm wavelength.

permittivity occurs when carrier concentration exceeds $4.55 \times 10^{20} \text{ cm}^{-3}$. Beyond this concentration, the highly doped silicon behaves like a metal. Thus, it can be used to absorb the unwanted polarization and simplify the fabrication.

III. RESULTS AND ANALYSIS

The plasmonic bend waveguide based TM-pass polarizer has been optimized by studying the design parameters such as the bend radius of the silicon waveguide, r_{Si} , the gap between the silicon and highly doped silicon waveguides, g , the thickness of the silicon and highly doped silicon waveguides, W_{Si} and W_{pSi} , the start and end angles of the highly doped silicon waveguides, θ_{inner} and θ_{outer} , and the carrier concentration of the highly doped silicon waveguides, N . The bend radius of the silicon waveguide, r_{Si} , has to be chosen in a way that it simultaneously offers the minimum bending loss and footprint. A small bend will reduce the footprint by requiring less number of bends to be cascaded but will increase the insertion loss. On the contrary, a large bend radius will help achieve small insertion loss, but more number of cascaded bends will be required to achieve a certain extinction ratio. To be competitive with the state-of-the-art polarizers, we set the target IL to be smaller than 2 dB. After careful simulations, we found $2 \mu\text{m}$ to be the optimum radius of the silicon waveguide to achieve our target IL while maintaining a design with competitive footprint and extinction ratio.

Table I presents the design parameters such as N , W_{Si} , W_{pSi} , and g , which will have their ranges optimized. We will optimize the device at 1550 nm since we target the C-band optical communication.

Figure 3 presents the ER, IL, and figure of merit, $FOM = \frac{ER}{IL}$, variations as functions of the design parameters. The variations of the ER, the IL, and the FOM as a function of the N are shown in Fig. 3(a). A higher doping concentration is desired so that the carriers absorb more light from the evanescent field of the deconfined TE mode, which results in a higher ER. Due to fabrication constraints, the highest value of N is chosen as $N = 10.5 \times 10^{20} \text{ cm}^{-3}$. Both the ER and the IL increase as N is increased. To explain this behavior, one must consider that the wavelength at which the real part of the complex relative permittivity of the doped silicon crosses zero moves toward smaller values as N is increased. As a consequence, the highly doped silicon exhibits more metallic behavior as N is increased at a particular wavelength. Thus, both the ER and IL are increased as N is increased. The FOM is maximum at $N = 10.5 \times 10^{20} \text{ cm}^{-3}$.

The effect of varying W_{Si} on the ER, IL, and FOM is shown in Fig. 3(b). The value of W_{Si} is varied between 260 and 360 nm to maintain the single mode condition⁴³ in the C-band. As seen from Fig. 3(b), both the ER and IL decrease with increasing W_{Si} . When the waveguide width is increased, the mode field is more concentrated in the core of the waveguide. Hence, there is less evanescent

TABLE I. List of parameters to be optimized and their ranges.

Parameter	N (cm^{-3})	W_{Si} (nm)	W_{pSi} (nm)	g (nm)	θ_{inner} (deg)	θ_{outer} (deg)
Min. value	4.55×10^{20}	260	150	150	55, 125	55, 125
Max. value	10.5×10^{20}	350	350	350	0, 180	5, 175

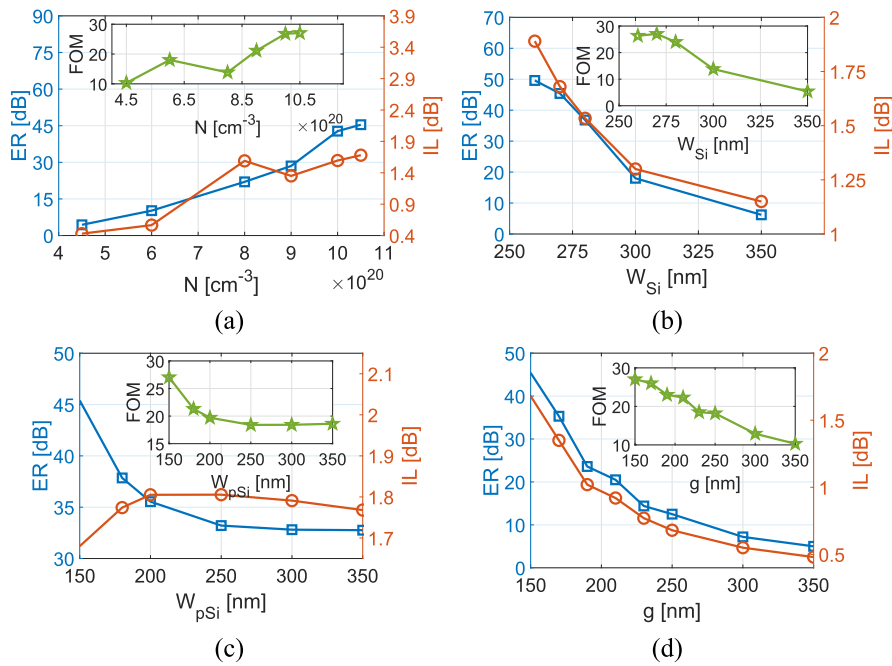


FIG. 3. Variation of the extinction ratio, insertion loss, and figure of merit at 1550 nm wavelength as a function of (a) the doping concentration N for $W_{\text{Si}} = 270$ nm, $W_{\text{pSi}} = 150$ nm, $g = 150$ nm, $\theta_{\text{inner}} = 15^\circ, 165^\circ$, and $\theta_{\text{outer}} = 35^\circ, 145^\circ$; (b) the W_{Si} for $N = 10.5 \times 10^{20} \text{ cm}^{-3}$, $W_{\text{pSi}} = 150$ nm, $g = 150$ nm, $\theta_{\text{inner}} = 15^\circ, 165^\circ$, and $\theta_{\text{outer}} = 35^\circ, 145^\circ$; (c) the W_{pSi} for $N = 10.5 \times 10^{20} \text{ cm}^{-3}$, $W_{\text{Si}} = 270$ nm, $g = 150$ nm, $\theta_{\text{inner}} = 15^\circ, 165^\circ$, and $\theta_{\text{outer}} = 35^\circ, 145^\circ$; and (d) the gap between the waveguides for $N = 10.5 \times 10^{20} \text{ cm}^{-3}$, $W_{\text{Si}} = 270$ nm, $W_{\text{pSi}} = 150$ nm, $\theta_{\text{inner}} = 15^\circ, 165^\circ$, and $\theta_{\text{outer}} = 35^\circ, 145^\circ$. The figure of merits is shown in the inset of each figure.

field outside the waveguide and in the proximity of the doped silicon, resulting in the reduced ER and IL. The highest FOM is found at 270 nm thickness of the silicon waveguide.

In Fig. 3(c), the results of varying W_{pSi} from 150 to 350 nm are presented. The minimum value is chosen as 150 nm to be compatible with the 193 nm DUV lithography.⁴⁴ The highest FOM is found at 150 nm thickness of the highly doped silicon layer. Figure 3(d) shows the effect of varying the gap between the silicon and the highly doped silicon waveguides on the ER, IL, and FOM. The gap is varied from 150 to 350 nm, where the minimum value is chosen to maintain compatibility with the 193 nm DUV lithography. The highest FOM is obtained for a gap of 150 nm.

Finally, we study the impact of varying θ_{inner} and θ_{outer} on the ER, IL, and FOM. As mentioned before, the maximum and

minimum values of $\theta_{\text{inner/outer}}$ are 0° and 180° , respectively. Smaller maximum values and larger minimum values of θ_{inner} and θ_{outer} indicate highly doped bend waveguides are smaller in length. We have obtained the performance metrics for different combinations of the θ_{inner} and θ_{outer} , which are presented in Fig. 4. It can be observed that the ER is highest for $\theta_{\text{inner}} = 0^\circ, 180^\circ$ and $\theta_{\text{outer}} = 5^\circ, 175^\circ$ since, for these values, the doped bend waveguides have the highest length. However, the IL is also the highest for these values of θ_{inner} and θ_{outer} . The best FOM is obtained for a combination of $\theta_{\text{inner}} = 15^\circ, 165^\circ$ and $\theta_{\text{outer}} = 35^\circ, 145^\circ$.

The optimized parameters of the TM-pass polarizers are provided in Table II. The TM and TE mode evolution at different sections of the polarizer with the optimized parameters is shown in Figs. 5(a) and 5(b), respectively. The electric field magnitude profiles

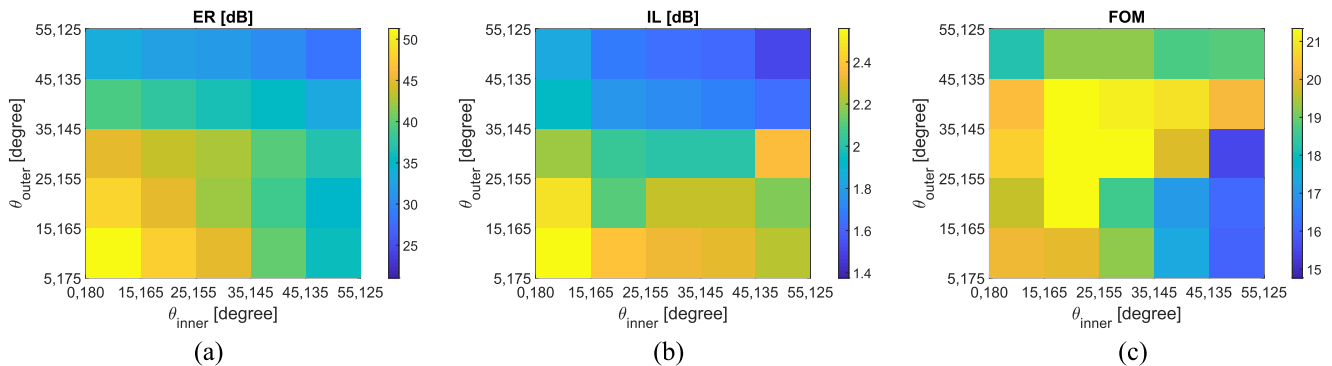


FIG. 4. Variation of the (a) extinction ratio, (b) insertion loss, and (c) figure of merit as a function of θ of inner and outer doped bend waveguides.

TABLE II. Summary of the optimized parameters.

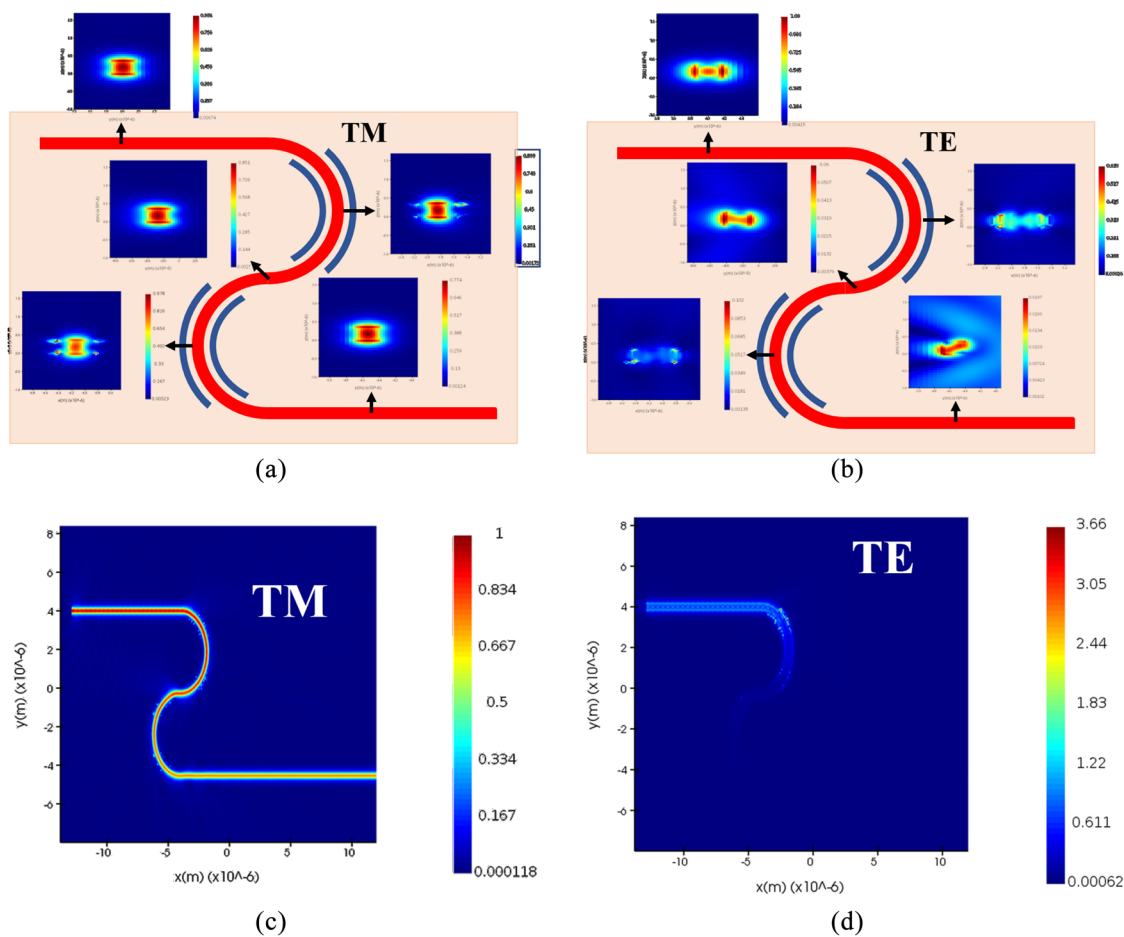
Parameter	N (cm ⁻³)	W_{Si} (nm)	W_{pSi} (nm)	g (nm)	θ_{inner} (deg)	θ_{outer} (deg)
Value	10.5×10^{20}	270	150	150	15, 165	35, 145

of the TM and TE modes can be seen in Figs. 5(c) and 5(d), respectively. After optimizing the parameter, it is important to calculate the bandwidth of the polarizer. It will be highly desirable if the same structure can be used in the different optical telecommunication bands. While short reach optical interconnects use the O-band and E-band, medium and long reach uses the C-band. The wavelength dependence of the ER and IL of the proposed TM-pass polarizer for the optimized parameters is shown in Fig. 6. The bandwidth over which the ER > 20 dB and IL < 2 dB is 72 nm spanning over part of the S-band and the whole C-band. At 1550 nm, the ER is 45.4 dB and the IL is 1.7 dB.

IV. ANALYSIS OF THE FABRICATION TOLERANCE

Many devices in SiPh suffer from reproducibility through the process and yield because they are not very fabrication tolerant. In particular, the sub-wavelength grating based designs^{13,21} are highly sensitive to fabrication variations. Therefore, it is desired to have a device that is highly fabrication tolerant. The fabrication tolerance of the proposed TM-pass polarizer to variations in the key design parameters is analyzed and presented in Fig. 7.

The non-uniformity of the silicon layer thickness in 200 mm SOI wafers has a 3σ of ± 6 nm, and the linewidth uniformity of the 193 nm DUV is controlled with a 3σ of ± 10 nm.^{32,45} Therefore, we vary the height of the silicon layer by ± 6 nm and other parameters by ± 10 nm. It can be observed from Fig. 7 that the insertion loss varies by a maximum of 0.6 dB and the extinction ratio varies by a maximum of 14 dB. A minimum extinction ratio of 36 dB and a maximum insertion loss of 2 dB are maintained with the maximum variations of h , W_{Si} , W_{pSi} , and g . Our device has a compact footprint, uses only two materials, has a large bandwidth, and is highly fabrication tolerant.

**FIG. 5.** Evolution of the (a) TM mode and (b) TE mode throughout different sections of the polarizer. Electric field magnitude of the (c) TM mode and (d) TE mode.

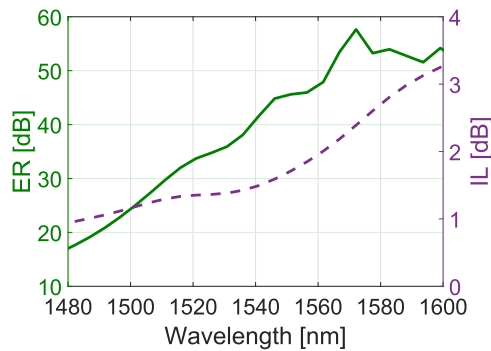


FIG. 6. ER and IL as a function of the wavelength for $N = 1.05 \times 10^{20}$, $W_{Si} = 270$ nm, $W_{pSi} = 150$ nm, $g = 150$ nm, $\theta_{inner} = 15^\circ$, 165° , and $\theta_{outer} = 35^\circ$, 145° . Reproduced with permission from Saber *et al.*, IET Optoelectron. **14**(3), 109–119 (2019). Copyright 2019 The Institute of Engineering and Technology.

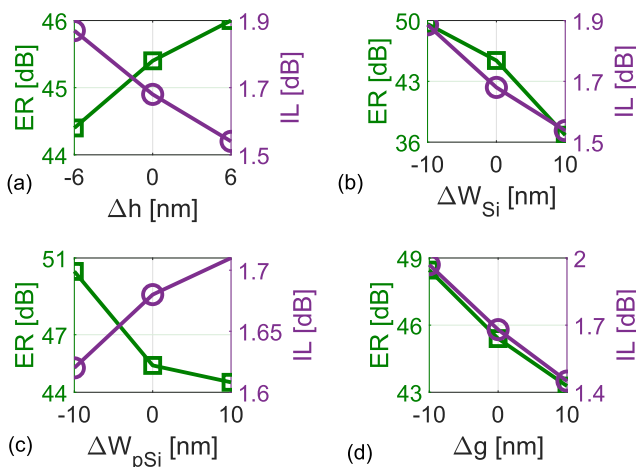


FIG. 7. Fabrication tolerance analysis due to variation of the (a) silicon layer height, h, (b) W_{Si} , (c) W_{pSi} , and (d) g.

V. COMPARISON WITH THE STATE-OF-THE-ART

Finally, in this section, we compare the performance of our reported TM-pass polarizer with the state-of-the-art. The key parameters such as the ER, IL, footprint, and CMOS-compatibility are compared and presented in Table III.

The TM-pass polarizer designs reported in Refs. 16, 18–20, and 46 use non-CMOS compatible materials such as silver, graphene, and vanadium oxide. On the other hand, sub-wavelength structures^{13,49,53} and photonic crystals^{52,54} are challenging to fabricate using the 193 nm DUV lithography that is used for volume production of the silicon photonic devices and circuits and are sensitive to fabrication variations. The device proposed in Ref. 47 has a buried silicon layer, and the ones in Refs. 48 and 50 require deposition of titanium nitride and aluminum-doped zinc oxide, respectively, adjacent to silicon dioxide with no gap in between. Both of these structures pose fabrication challenges. The ER offered by the device proposed in Ref. 15 is small.

TABLE III. Comparison with other TM-pass polarizers. ER = extinction ratio, IL = insertion loss, and NA = not provided.

References	ER (dB)	IL (dB)	Footprint (μm^2)	CMOS	Type of work
This work	45.4	1.7	$<8.8 \times 5.4$	Yes	Simulation
13	34	1	4	Yes	Experiment
15	11.5	NA	0.1	Yes	Simulation
17	30.11	3.08	15	Yes	Simulation
16	15.2	0.84	3.9	No	Simulation
18	25	0.088	2.5	No	Simulation
19	40	3	150	No	Simulation
20	15	3	1	No	Simulation
46	45	1	7.5	No	Simulation
47	20	0.15	1.31	Yes	Simulation
48	20	1	2.84	Yes	Simulation
49	24	0.97	12	Yes	Simulation
50	22	0.11	1	Yes	Simulation
51	38	0.05	20	Yes	Simulation
52	45	0.6	5	Yes	Simulation
53	32	0.2	5.2	Yes	Simulation
54	40	0.4	12.9	Yes	Experiment

Among both CMOS compatible and non-compatible designs, our polarizer offers the highest ER. It is also more tolerant to fabrication variations as shown in Fig. 7 compared to the sub-wavelength grating based designs. The IL and footprint are comparable to most of the previous reports as well. The polarizer reported in Ref. 46 has similar ER while offering a smaller IL and footprint. However, the design is not CMOS compatible. The photonic crystal-based design reported in Ref. 52 also offers similar ER but is challenging to fabricate using the DUV lithography process as mentioned before.

VI. CONCLUSIONS

We report a bend waveguide based TM-pass polarizer achieving an ER of 45.4 dB, an IL of 1.68 dB, and a footprint of $<8.8 \times 5.4 \mu\text{m}^2$. An extinction ratio of >20 dB and an insertion loss of <2 dB are obtained over a bandwidth of 72 nm. The proposed TM-pass polarizer has the highest extinction ratio to the best of our knowledge and offers relaxed fabrication complexity and better fabrication tolerances by incorporating CMOS compatible feature sizes.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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