A Hybrid Modular Interline Current Flow Controller for Meshed HVDC Grids

Shuxin Zhang, Binbin Li, *Member*, *IEEE*, Wei Wang, *Member*, *IEEE*, Yujie Zhang, Dianguo Xu, *Fellow*, *IEEE*, Gen Li, *Member*, *IEEE,* and Jun Liang, *Senior Member*, *IEEE*

***Abstract*—In meshed high voltage direct current (HVDC) grid, the current flows through the lines cannot be controlled with sufficient freedom without additional power electronics based devices, namely current flow controller (CFC). In this paper, a novel hybrid modular interline CFC is proposed based on H-bridge sub-modules (SMs) and thyristor valves. Due to its modularity, the proposed CFC is particularly suitable for applications requiring high voltage and large power capacity. The circuit structure, operation principle and parameter design are presented. In addition, a control strategy is developed for the proposed CFC. Simulations are carried out using a four-terminal meshed HVDC grid to verify the effectiveness of the topology and its control strategy. A downscaled prototype is built which further validates the proposed CFC.**

***Index Terms*—high voltage direct current (HVDC), meshed HVDC grid, current flow controller (CFC), sub-modules (SMs), thyristor.**

I. Introduction

IN the last decade, dozens of voltage source converter based high voltage direct current (VSC-HVDC) links have been installed worldwide [1]-[3]. In order to achieve a more reliable and effective sharing of renewable energy sources across different areas, applications of meshed HVDC grids have been getting widespread attention of the academia and industry in recent years [4]-[7]. The Zhangbei ±500kV/9000MW four-terminal meshed HVDC grid – the world's first meshed HVDC grid project, has already been commissioned in 2020 [8].

Although meshed HVDC grids offer higher flexibility, reliability, and efficiency, they still face the challenge of current flow control. For instance, some of the HVDC transmission lines may experience overload while others may not be fully utilized. This is because DC current flows are passively distributed according to the resistances of transmission lines. To address this issue, a power electronics based device called current flow controller (CFC) has been proposed. The CFC inserts an adjustable DC source in series connection with HVDC transmission lines, which adds an extra control freedom and ensures the line currents in meshed HVDC grids are fully controllable [9], [10].

The most straightforward way to implement a CFC is using an AC/DC converter which connects an external AC source. In [11], two six-pulse thyristor converters are anti-paralleled (a positive converter and a negative converter), where their common DC link is inserted into an HVDC line. This ensures a four-quadrant operation capability and bidirectional DC voltage controllability. This approach features low capital cost and power loss due to the use of thyristors. However, severe harmonics and slow control performance are its shortcomings. To overcome these shortcomings, a modular multilevel converter (MMC) based CFC has been proposed in [12], presenting much better voltage waveform without any filtering effort. The H-bridge sub-modules (SMs) are required to ensure the inserted DC voltage can be bidirectional. On the other hand, isolated DC/DC converters can also be used to implement a CFC, which connects an external DC source [13], [14]. It should be noted that all of these above approaches rely on external power sources and transformers with high insulation requirement (to withstand the HVDC offset voltage stress). This brings great challenges in terms of insulation design and results in significant weight, volume and cost of the transformer.

On the other hand, the so-called interline CFC (I-CFC) is more promising, which is essentially a kind of DC/DC converter, where its DC ports are inserted into two adjacent HVDC lines, respectively. Hence, the line current can be controlled by adjusting the voltage difference between the two DC ports, and there is no need to exchange power with external AC or DC source. The I-CFC concept is initially proposed in [15], where two standard H-bridge cells are used with a common DC-link capacitor. By controlling the IGBTs, the capacitor can be alternatively inserted into two adjacent HVDC lines to regulate the current flow, and this topology has been further validated through an experimental prototype in [16]. In [17], one H-bridge cell is removed and the capacitor is switched by two pairs of anti-series connected IGBTs. In [18], the two H-bridges are further integrated into three half-bridges which saves two IGBTs, and the operation principle, modelling and control strategy are discussed. Moreover, some other simplified I-CFC topologies are proposed in [19]-[22] to further reduce IGBTs, but they only allow unidirectional current flow controllability. Nevertheless, since only one capacitor is used in these I-CFCs, the inserted port voltages contain large ripples, which may cause current ripples in the HVDC lines. To solve this problem, an isolated bidirectional DC/DC converter with two independent capacitors can be employed, where the large ripples of inserted port voltages are eliminated [23], [24].

However, for practical large-capacity long-distance HVDC grid, the line voltage drop that an I-CFC should compensate can be up to tens of kilovolts (approximately 5% of the rated HVDC

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S. Zhang, B. Li, W. Wang, Y. Zhang, and D. Xu are with the School of Electrical Engineering and Automation, Harbin Institute of Technology, Harbin 150001, China (e-mail: zhangshuxin@hit.edu.cn; libinbin@hit.edu.cn; wangwei602@hit.edu.cn; 19S106164@stu.hit.edu.cn; xudiang@hit.edu.cn).

G. Li and J. Liang are with the the School of Engineering, Cardiff University, Cardiff CF24 3AA, U.K. (e-mail: lig9@cardiff.ac.uk; liangj1@cardiff.ac.uk).

voltage), and the power rating of the I-CFC could reach tens of megawatts. As a consequence, the aforementioned I-CFC topologies cannot be used in such large-capacity long-distance HVDC applications, due to the limited voltage rating of each single IGBT device. To realize a powerful I-CFC with sufficient voltage and power rating, a front-to-front (F2F) MMC based DC/DC converter is used in [25], which inherits the distinctive advantages of MMC in aspects of good scalability of voltage and power rating. However, it requires two full-power conversion stages and one high-insulation bulky AC link transformer, so the components count and power losses are too significant. In [26], a more compact I-CFC topology is proposed. It consists of three strings of H-bridge SMs which are connected end-to-end as a triangular ring, whose vertices are respectively connected to the two HVDC lines and the HVDC bus. The inserted DC voltages can be simply realized by adjusting the output voltages of the SM strings. Thanks to its modular structure, this ringlike I-CFC presents good scalability in terms of voltage and power ratings, making itself a promising solution for large-capacity long-distance HVDC grids [27]. Its topology design optimization and dynamic control are further investigated in [28] and [29], respectively. However, on the downside, this ringlike I-CFC must superpose a large AC circulating current in the SM strings to maintain the energy stability of the SM capacitors. This results in higher current stress of the IGBTs and higher power losses. Besides, additional large AC voltage components are needed in the SM strings to realize the power exchange, which requires a higher number of SMs to generate this AC voltage.

In this paper, a novel hybrid modular I-CFC (HMI-CFC) is proposed by combining thyristor valves and H-bridge SM strings. By appropriately triggering the thyristor valves, each SM string can be alternatively inserted into different HVDC lines to regulate the current flow and maintain the stable energy storage in the SM capacitors. Moreover, a polyphase structure is employed and the waveforms are interleaved, as a result the ripples of line currents are small and additional filters are not required. Because the SM strings only generate DC voltage components, the number of SMs can be significantly reduced compared to the ringlike I-CFC in [26]. The power losses are also markedly reduced since no extra AC circulating current is required.

The remainder of this article is organized as follows. In Section II, circuit structure of the HMI-CFC and its operation principle are introduced. This is followed by parameter design in Section III as well as the control strategy in Section IV. In Section V, the operation of an HMI-CFC rated at 20kV/60MW is verified through simulations conducted in a 500kV/4500MW four-terminal meshed HVDC grid. Finally, in Section VI, a 200V/4kW HMI-CFC prototype has been tested which further confirms the effectiveness of the proposed HMI-CFC.

II. HMI-CFC and Its Operation Principle

A. Circuit Structure of the Proposed HMI-CFC

The circuit structure of the proposed HMI-CFC is shown in Fig. 1. There are three terminals in this topology. Terminals 1

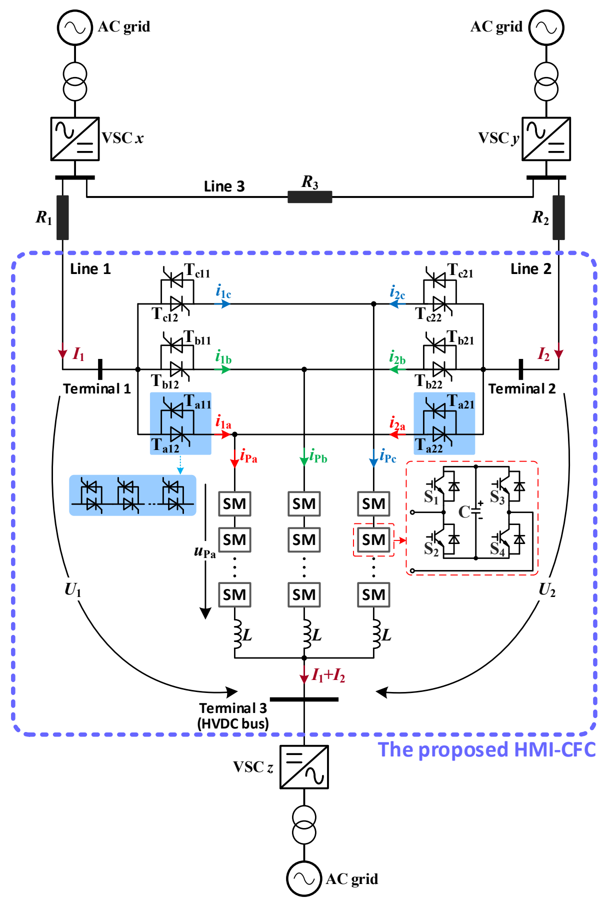

Fig. 1. Configuration of the proposed HMI-CFC.

and 2 are respectively connected to HVDC Lines 1 and 2, and Terminal 3 is connected to HVDC bus. Terminal 1 and Terminal 3 form one DC port, which inserts voltage U_1 into Line 1. Similarly, Terminal 2 and Terminal 3 constitute the other DC port inserted into Line 2, whose voltage is U_2. The currents flowing through Lines 1 and 2 are respectively denoted by I_1 and I_2, and R_1 and R_2 are the line resistances. Either I_1 or I_2 can be chosen as the current flow control object. By adjusting U_1 and U_2, the line voltage drop can be regulated. Hence, the current flow within this meshed HVDC loop can be fully controlled.

The HMI-CFC has a three-phase (j=a, b, c) structure, and each phase is composed of two bidirectional thyristor valves, one SM string, and a buffering inductor L. T_{j11}/T_{j12} forms the thyristor valve linked to Terminal 1, whereas T_{j21}/T_{j22} forms the thyristor valve linked to Terminal 2, and they are all composed of series connection of several thyristors. Each SM string consists of a number of H-bridge SMs. For each phase, once T_{j11}/T_{j12} is in on-state, the SM string will be in series with Line 1 to generate voltage U_1. On the contrary, when T_{j21}/T_{j22} is in on-state, the SM string will be connected in series with Line 2 to generate voltage U_2. i_{Pj} is the current flowing through the SM string and u_{Pj} is the output voltage of the SM string. i_{1j} and i_{2j} represent the currents flowing through the thyristor valves T_{j11}/T_{j12} and T_{j21}/T_{j22}, respectively.

B. Operation Principle

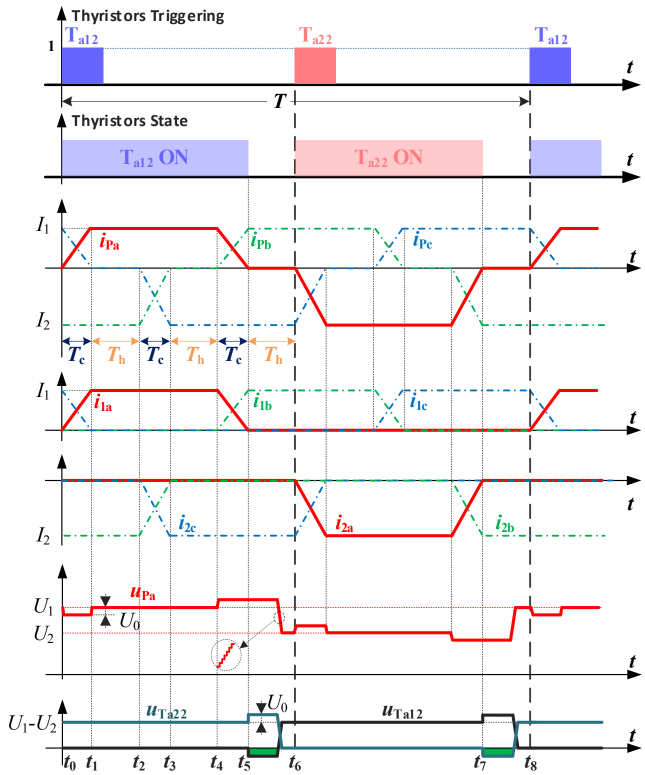

Fig. 2. Sketched key operating characteristics of the proposed HMI-CFC (when the line currents are in opposite directions).

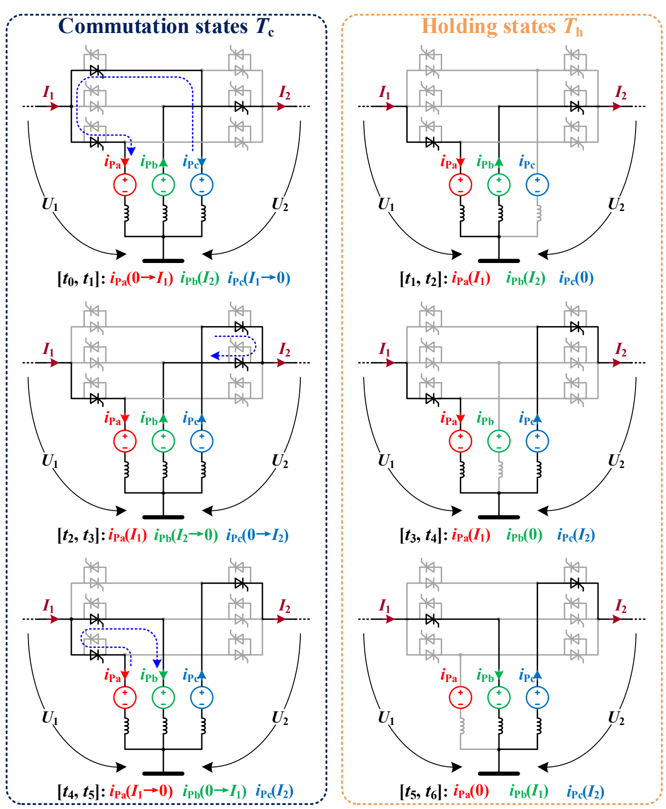

Fig. 3. Six states of the proposed HMI-CFC during [t_0, t_6].

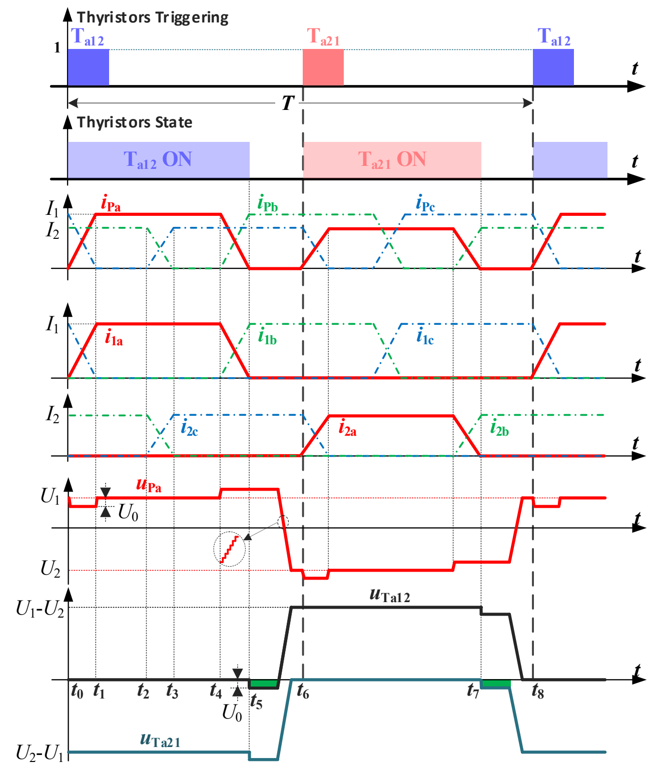

Fig. 4. Sketched key operating characteristics of the proposed HMI-CFC (when the line currents are in the same direction).

Fig. 2 shows the key operating characteristics of the proposed HMI-CFC, when the line currents I_1 and I_2 are in opposite directions. The three phases of the proposed HMI-CFC operate in interleaving mode, and their operating waveforms (including thyristors triggering signals, thyristors current and voltage, and SM string currents and voltages, etc.) are identical but with 120° phase shift. Taking phase a as an example, during [t_0, t_5], the thyristor T_{a12} is triggered on, and the SM string is connected in series with Line 1, which will generate voltage U_1 to regulate the current I_1. Therefore, the current i_{Pa} flowing through the SM string has a positive amplitude I_1. The waveform of i_{Pa} is controlled to be trapezoidal, and it will charge the SM capacitors. On the other hand, during [t_6, t_7], the thyristor T_{a22} is triggered on. The SM string is in series with Line 2, whose output voltage is U_2. The waveform of SM string current i_{Pa} is controlled to be a trapezoid with negative amplitude I_2, so as to discharge the SMs. With such a mechanism, the two thyristor valves in one phase are triggered complementarily to connect the string in series with the two HVDC lines alternately. The energy absorbed by the string during [t_0, t_5] is equal to that released during [t_6, t_7], and the alternation frequency is denoted by f (f=1/T). Due to the design of interleaving operation of the three phases, there are always two strings used to respectively sustain the port voltages U_1 and U_2, and the third string is used to commutate the current with one of the previous two strings. In addition, the energy stored in each string can maintain stable.

The trapezoidal current waveform is regulated by adjusting the voltage applied across the buffering inductor L, which is equal to half of the voltage difference of two SM strings when they are in parallel to implement commutation. For example, when u_{Pa} equals U_1-U_0, u_{Pc} should be U_1+U_0, and U_0 will be applied across the inductor L, making i_{Pa} increase linearly. This can be further interpreted as in Fig. 3, in which the six states in half a cycle [t_0, t_6] are listed. The six states are divided into two types, namely commutation state T_c and holding state T_h, and the two types of states always appear alternately in time sequence. During the commutation state T_c, one of the line currents will be jointly provided by two strings, which are connected in parallel to commutate with each other. For example, as shown in Fig. 3, during [t_0, t_1], I_1 is jointly provided by i_{Pa} and i_{Pc}, and I_2 is equal to i_{Pb}. During this commutation state, i_{Pa} is increasing and i_{Pc} is decreasing with the same rate, and i_{Pb} holds a constant value, hence I_1 and I_2 are all constant DC currents. On the other hand, during the holding state T_h, two line currents are respectively provided by two strings, and the third string is isolated. Therefore, the currents of the three strings will hold their values (one string current is equal to zero). For example, as shown in Fig. 3, during [t_1, t_2], i_{Pa} is equal to I_1, i_{Pb} is equal to I_2, and i_{Pc} is equal to zero. As shown in Fig. 2, the commutation state T_c and holding state T_h are alternate and each appears three times within half a cycle [t_0, t_6]. And the situation is similar in the second half cycle [t_6, t_8]. In consequence, although the thyristor currents of each phase i_{1j} and i_{2j} are discontinuous, they synthesize continuous HVDC line currents I_1=i_{1a}+i_{1b}+i_{1c} and I_2=i_{2a}+i_{2b}+i_{2c} without any filtering effort.

In addition, the string voltage also facilitates the turn-off and turn-on of the thyristors. When a thyristor should be turned off, after the thyristor current decreases to zero, an extra voltage U_0 will be retained for a while by adjusting u_{Pa}, which provides a reverse voltage across the thyristor to ensure it turns off reliably, as emphasized by green rectangle in thyristor voltage u_{Ta12} and u_{Ta22} in Fig. 2. When a thyristor should be turned on, before triggering the thyristor, the string voltage u_{Pa} is adjusted to be equal to U_1 or U_2, so as to counteract the DC port voltage and achieve approximate zero-voltage condition for the thyristor valve to softly turn on. Moreover, during the string voltage rising and falling processes, the SMs are switched sequentially in order to avoid causing excessive du/dt in the waveform of u_{Pa}.

Fig. 4 further shows the key operating characteristics of the proposed HMI-CFC, when the line currents I_1 and I_2 are in the same direction. The waveforms during [t_0, t_6] are similar to that in Fig. 2. However, during [t_6, t_8], the string current is controlled as a trapezoid with positive amplitude I_2, and string voltage u_{Pa} is regulated to match U_2 with a negative voltage polarity. This attributes to the bidirectional voltage output capability of the H-bridge SMs.

Based on the above operation principle, the proposed HMI-CFC can insert port voltages U_1 and U_2 into Lines 1 and 2 simultaneously to regulate the current flow. The proposed HMI-CFC presents high controllability and scalability, and inherits the high maturity of both thyristor valves in line commutated converter (LCC) based HVDC and SMs in MMC based HVDC. Neither high-insulation AC transformer nor additional AC currents/voltages are required. Therefore, the number of SMs, current stress, and footprint can be reduced.

III. Parameter Design

A. Sub-Modules (SMs)

With the proposed HMI-CFC, the current flow within the meshed HVDC loop can be regulated by adjusting the inserted voltages U_1 and U_2, which are applied across the loop resistance. Hence, the corresponding line current variation can be expressed as

$$\Delta I_1 = \frac{U_2 - U_1}{R_{\text{loop}}} \tag{1}$$

where ΔI_1 is the current increment of the controlled current I_1 and R_{loop} is the loop resistance which is equal to the summation of the resistances of all the HVDC lines in the meshed loop (namely, R_{loop}=R_1+R_2+…).

On the other hand, if taking no account of the HMI-CFC power losses, the summation of the power of the two DC ports should be zero, which gives

$$U_1 I_1 + U_2 I_2 = 0. \tag{2}$$

Combining (1) and (2), the values of U_1 and U_2 can be obtained as

$$\begin{cases} U_1 = -\dfrac{I_2 \Delta I_1 R_{\text{loop}}}{I_1 + I_2} \\ U_2 = \dfrac{I_1 \Delta I_1 R_{\text{loop}}}{I_1 + I_2} \end{cases}. \tag{3}$$

In terms of the proposed HMI-CFC, summation of the SM output voltages in each string should be able to provide the required DC port voltage plus an extra current driving voltage component U_0. In consequence, without regard to redundancy, the required number of SMs in each SM string can be calculated as

$$N = \frac{max\left[\left|U_1\right|,\ \left|U_2\right|\right] + U_0}{U_{\text{C}}} \tag{4}$$

where U_C is the nominal capacitor voltage of SMs, max[] denotes taking the maximum value, selecting the larger value between U_1 and U_2.

The current stress of the IGBTs in SMs equals the maximum absolute value of the HVDC line currents, which is

$$I_{\text{stress}} = max\left[\left|I_1\right|, \left|I_2\right|\right]. \tag{5}$$

B. Thyristors

In the proposed HMI-CFC, the series-connected thyristor valves need to withstand the voltage difference between U_1 and U_2 plus an extra current driving voltage U_0. Therefore, the required number of series-connected thyristors can be expressed as

$$N_{thy.} = \frac{\left|U_1 - U_2\right| + U_0}{\lambda_{\text{d}} U_{\text{B}}} = \frac{\left|\Delta I_1 R_{\text{loop}}\right| + U_0}{\lambda_{\text{d}} U_{\text{B}}} \tag{6}$$

where U_B is the rated blocking voltage of each thyristor and λ_d is the voltage derating factor in terms of series connection, which is usually selected no more than 0.9 [30].

As for the current rating of the thyristors, they conduct the line currents during only one third of the operation cycle, hence their forward currents can be respectively calculated as

$$I_{\text{F(AV)-}T_{j11}/T_{j12}} = \frac{1}{2\pi}\int_0^{\frac{2\pi}{3}} |I_1| \mathrm{d}\theta = \frac{|I_1|}{3}, \tag{7}$$

$$I_{\text{F(AV)-}T_{j21}/T_{j22}} = \frac{1}{2\pi}\int_0^{\frac{2\pi}{3}} |I_2| \mathrm{d}\theta = \frac{|I_2|}{3}. \tag{8}$$

C. SM Capacitance

As for the SM capacitors, they need to be designed to ensure an allowed capacitor voltage ripple, which are expressed as

$$\frac{1}{2}NC\left(U_{\text{C},max}^2 - U_{\text{C},min}^2\right) = NC\varepsilon U_{\text{C}}^2 = \Delta E \tag{9}$$

where ε is the specified relative voltage ripple of the SM capacitor. ΔE is the energy variation of one SM string, which can be calculated as

$$\Delta E = \int_0^{0.5T} u_{\text{Pa}} i_{\text{Pa}} \mathrm{d}t = \frac{|U_1 I_1| T}{3}. \tag{10}$$

Substituting (10) into (9), the required SM capacitance can be derived as

$$C = \frac{|U_1 I_1| T}{3N\varepsilon U_{\text{C}}^2}. \tag{11}$$

D. Buffering Inductance

With respect to the buffering inductor L, its inductance is inversely proportional to the switching ripple of string current Δi, hence it is restricted by

$$L \geq \frac{U_{\text{C}}}{4\Delta i f_{\text{s}}} \tag{12}$$

where f_{s} is the equivalent switching frequency of one SM string.

On the other hand, the inductance is also related to the string current rising/falling slope of the trapezoidal waveforms, which can be expressed as

$$L \leq \frac{U_0 T_{\text{c}}}{max\left(|I_1|, |I_2|\right)} \tag{13}$$

where T_{c} and T_{h} meet the relationship shown in Fig. 2, which is

$$T_{\text{c}} + T_{\text{h}} = \frac{T}{6} \tag{14}$$

where T_{h} should be higher than the turn-off time t_{q} of the thyristors (typically 500μs to 800μs for high-voltage thyristors), which is mainly determined by the reverse recovery characteristic of the selected thyristors. In consequence, the alternation frequency f of the HMI-CFC usually can be designed as 100~200Hz.

IV. Control Strategy

In order to effectively operate the proposed HMI-CFC, the control strategy is developed. Taking phase a as an example, as shown in Fig. 5, there are five main tasks involved in the control strategy, which are as follows:

1) *Current Flow Control*: regulating the controlled HVDC line current I_1 to follow the given command. According to (1), this can be implemented by regulating the differential mode voltage between the DC port voltages U_1 and U_2, which is expressed as

$$U_{\text{dif}} = \frac{U_2 - U_1}{2} = \frac{\Delta I_1 R_{\text{loop}}}{2}. \tag{15}$$

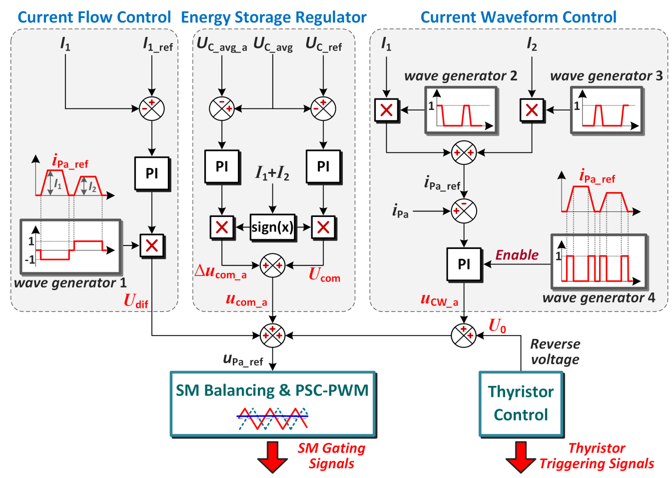

Fig. 5. Control block diagrams of the proposed HMI-CFC.

When there is an error between the given command of Line 1 current I_{1_ref} and the measured I_1, the current flow control will adjust the differential mode voltage U_{dif} by a proportional-integral (PI) controller. The *wave generator* 1 determines the signature of U_{dif} when the SM string is in series connection with Lines 1 and 2, respectively.

2) *Energy Storage Regulator*: ensuring the energy stability of the SM capacitors. If the DC port voltages U_1 and U_2 are simultaneously increased or decreased, the HMI-CFC will absorb or release more energy from the HVDC lines, depending on the direction of line currents. In the meantime, the line currents will not be affected since the differential mode voltage is not changed. Hence, the energy stored in the SM capacitors can be regulated by adjusting the common mode voltage between the DC port voltages, which is

$$U_{\text{com}} = \frac{U_1 + U_2}{2}. \tag{16}$$

The error between the reference capacitor voltage $U_{\text{C\_ref}}$ and the measured average capacitor voltage $U_{\text{C\_avg}}$ is sent into a PI controller, generating the common mode voltage U_{com}. The direction of the total current I_1+I_2 decides the sign of U_{com}. Besides, although the three-phase circuits are identical, in practice, there are inevitably certain parameter differences, giving rise to energy unbalance among the three SM strings. Hence, a small correction $\Delta u_{\text{com\_a}}$ for the common mode voltage is added for phase a, so as to maintain the average capacitor voltages of the SM strings to be equal.

3) *Current Waveform Control*: controlling the trapezoidal waveforms of the string currents. This is realized by generating an extra current driving voltage $u_{\text{CW\_a}}$ during the commutation state T_{c}. This is achieved through a current control loop. The current reference $i_{\text{Pa\_ref}}$ is obtained by adding two trapezoidal waveforms whose amplitudes are I_1 and I_2, respectively.

4) *Thyristor Control*: generating triggering signals of thyristors and providing reverse voltage U_0 to turn off thyristors reliably once the string current decreases to zero.

5) *SM Balancing & Modulation*: providing SM gating signals. At last, U_{dif}, $u_{\text{com\_a}}$, and $u_{\text{CW\_a}}$ are summed to generate the final referenced string voltage $u_{\text{Pa\_ref}}$, which is sent to the phase shifted carrier pulse-width modulation (PSC-PWM) to

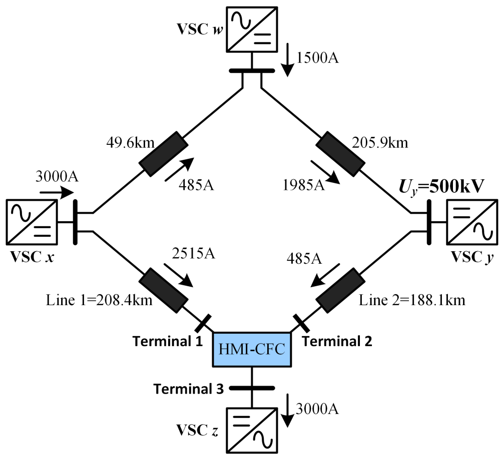

Fig. 6. Four-terminal meshed HVDC grid with the HMI-CFC in station z.

TABLE I
PARAMETERS OF THE HMI-CFC

Parameters	Values
No. of SMs in each string	N=10
Average SM capacitor voltage	U_C=2.4kV
SM capacitance	C=5mF
String inductance	L=0.5mH
PSC carrier frequency	f_c=650Hz
Alternation frequency	f=200Hz
Commutation state time	T_c=313μs
Holding state time	T_h=520μs

synthesize the SM gating signals, where the capacitor voltage balancing mechanism among the SMs in each string is embedded [31]. The SMs in the string are switched sequentially with phase-shifted carriers, which automatically results in a staircase-shaped transition waveform of u_{Pa} to avoid large du/dt. As for the other two phases, the only difference is that the waveform generators are interleaved with a 120° phase shift.

On the other hand, it is worth noting that the proposed control strategy is also effective to start-up the HMI-CFC. When the line currents do not need to be controlled, the two ports of the HMI-CFC are respectively bypassed by two mechanical switches. Once the line current should be regulated by the HMI-CFC, the mechanical bypass switches will be opened. Afterwards, the HMI-CFC will be activated, and the referenced command of Line 1 current I_{1_ref} is set to be equal to the present value of Line 1 current I_1. Therefore, the differential mode voltage U_{dif} will be equal to zero, and the line currents I_1 and I_2 will not be changed. However, the energy storage regulator will generate the common mode voltage u_{com_a} to absorb power to charge the SM capacitors, which will make the SM capacitors voltages change from 0V to the rated value. After this, the referenced command of Line 1 current I_{1_ref} will be updated and the HMI-CFC will begin to regulate the line current to be the desired value.

V. SIMULATION VERIFICATION

A. Simulation Results

In this section, a four-terminal meshed HVDC grid, as shown in Fig. 6, is simulated in MATLAB/SIMULINK to verify the effectiveness of the proposed HMI-CFC. The lengths of the HVDC overhead lines are shown in the figure and the resistance and inductance per kilometer are 0.04Ω and 1.02mH, respectively. The master-slave control is applied in this HVDC grid, in which VSC y is the master station regulating the DC voltage U_y as 500kV. VSCs w and x inject 1500A and 3000A DC currents into the HVDC grid, respectively. While VSC z absorbs 3000A DC current from the HVDC grid. The values of the line currents without CFC are also labeled in Fig. 6. The HMI-CFC is equipped at VSC z and the line current I_1 is controlled. The DC ports of the HMI-CFC is designed to be able to output DC voltage of 20kV, hence the thyristor valves should withstand about 40kV which is twice the DC port voltage. And the parameters are listed in Table I. The holding state time T_h is designed to be 520μs, which is slightly greater than t_q=500μs in order to ensure thyristor turns off reliably. The alternation frequency f is designed to be 200Hz, therefore T_c should be 313μs according to (14).

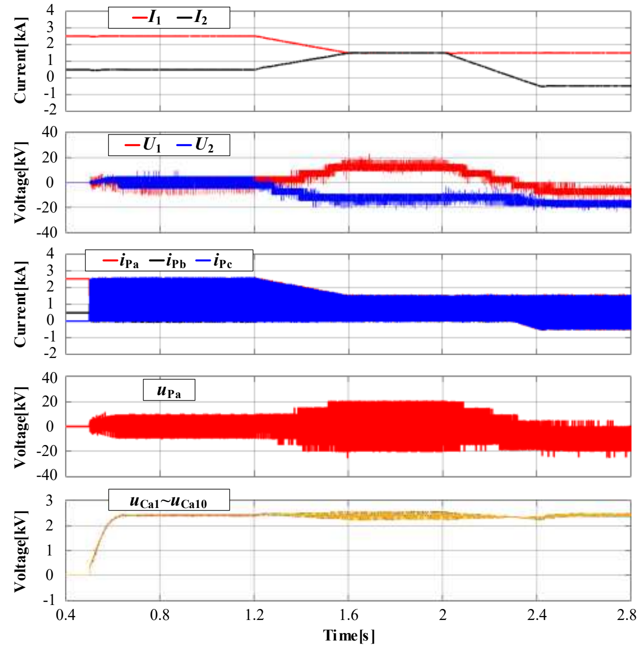

Fig. 7. Simulation results of dynamic current flow control process.

Fig. 7 shows the simulation results of dynamic current flow control process. When the HMI-CFC is not activated, the line current I_1 was 2515A and I_2 was 485A, indicating the Line 1 was overloaded. At the beginning, the voltages of the SM capacitors are equal to zero. Afterwards, the HMI-CFC was activated at 0.5s, and the referenced command of Line 1 current I_{1_ref} was set to be equal to the present value 2515A. In consequence, the line currents I_1 and I_2 maintained unchanged, and the SM capacitors were charged from 0V to the rated value 2.4kV, as shown in Fig. 7 during [0.5, 1.2s]. The proposed HMI-CFC started to regulate the overloaded line current at 1.2s and the referenced current I_{1_ref} was ramped down from 2515A to 1500A during [1.2, 1.6s]. During [1.6, 2.0s], I_1 and I_2 were both sustained at 1500A, and it can be observed that a positive U_1 and negative U_2 are simultaneously generated at the two DC ports by the HMI-CFC to control the line current. Afterwards, the current absorbed by VSC z was intentionally changed from 3000A to 1000A during [2.0, 2.4s]. As I_1 was controlled to be

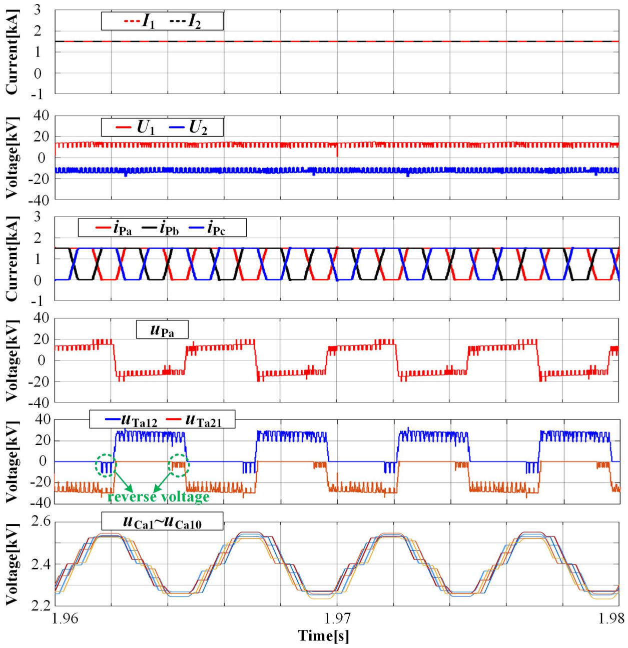

Fig. 8. Detailed simulation results during [1.96, 1.98s].

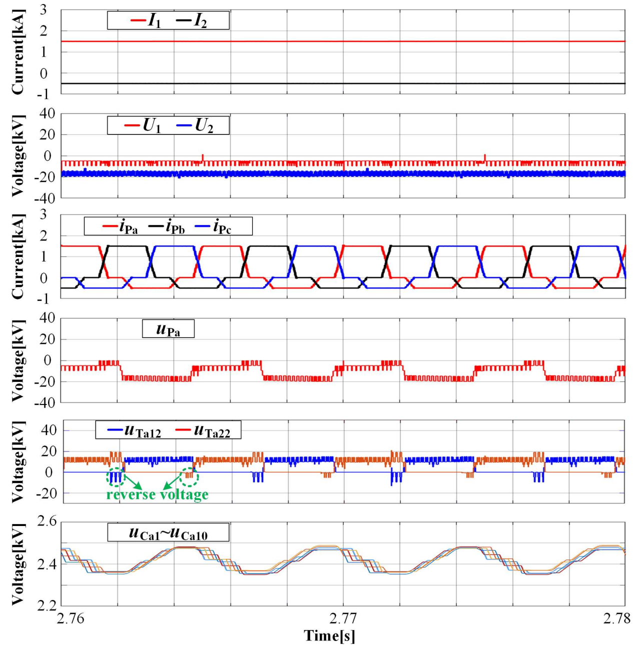

Fig. 9. Detailed simulation results during [2.76, 2.78s].

constant as 1500A, I_2 varied with the change of VSC *z* current. Therefore, during [2.4, 2.8s], I_1 was maintained at 1500A, while I_2 became -500A. Hence, the inserted voltages U_1 and U_2 were both negative. The capacitor voltages were kept balanced during the whole process.

The detailed steady-state waveforms within [1.96, 1.98s] are further zoomed in Fig. 8. During this period, the line currents I_1 and I_2 had the same direction and they were both equal to 1500A. The two DC port voltages were constant U_1 = 13.2kV and U_2 = -13.2kV, which were in good accordance with the values calculated by (3). Although the two ports simultaneously inserted voltage into the two lines, some switching steps can be observed in the waveforms of U_1, U_2 and u_{Pa}. The step voltage is approximately equal to 2.4kV, which is corresponding to insertion/bypass of one SM. The currents of the three strings (i_{Pa}, i_{Pb}, i_{Pc}) were trapezoidal waveforms with the amplitude of 1500A, and they were interleaved with 120° electrical angles, resulting in continuous I_1 and I_2. With the existence of HVDC line reactance (1.02mH/km) and resistance (0.04Ω/km), the voltage steps in U_1 and U_2 will not cause large harmonics in I_1 and I_2, and the analyzed THD values of I_1 and I_2 are 0.18% and 0.25%, respectively. u_{Pa} was composed of only DC components, which was equal to U_1 or U_2 when the SM string was in series with Lines 1 and 2, respectively. And staircase can be observed in u_{Pa} which limited the du/dt. As marked with the green circle, a reverse voltage was applied across the thyristor for t_q=500μs after the string current decreased to zero to ensure the reliable turn-off of thyristors. Furthermore, the voltage across the thyristor u_{Ta12} and u_{Ta21} was almost zero before it began to conduct. The SM capacitor voltages u_{Ca1}~u_{Ca10} were well balanced and the relative voltage ripple of the SM capacitor was 11.5%, which was in accordance with (11).

Furthermore, the detailed operation waveforms during [2.76, 2.78s] are further zoomed in Fig. 9. During this period, the line currents I_1 and I_2 had opposite directions with the values of 1500A and -500A, respectively. The currents of the three strings were still trapezoidal waveforms with the amplitudes of 1500A and -500A, and they were also interleaved with 120° electrical angles. The HMI-CFC DC port voltages both became negative, which were U_1 = -5.7kV and U_2 = -17.1kV, respectively. The SM capacitor voltages were well balanced and the relative voltage ripple of the SM capacitor was 5.0%.

B. Comparison Analysis

Furthermore, the comparison of the proposed HMI-CFC and the ringlike I-CFC in [26] are evaluated by co-simulations using MATLAB/SIMULINK and PLECS, wherein the CFCs both operate at the same condition of 13kV/20MW. Identical SMs are used in the HMI-CFC and the ringlike I-CFC, with the ABB 4.5kV/3kA press-pack IGBT "5SNA3000K452300". Besides, the ABB 5.2kV/2.76kA thyristor "5STP 25L5200" is used in the thyristor valves in the HMI-CFC.

Table II shows the comparison results of the component counts. For the proposed HMI-CFC, there are 10 SMs in each string so as to output 20kV DC port voltage. In each thyristor valve, there are 10 thyristors connected in series to withstand 40kV. On the other hand, for the ringlike I-CFC in [26], there are 5 SM strings, as shown in Fig. 10. *Strings* 1 and 2 inject the required DC voltage to perform the HVDC line current control, while at the same time generate AC voltage to modulate AC circulating current between them to maintain the energy stability of the SM capacitors. *String* 3 provides a path for the AC circulating current, hence it should withstand twice the DC port voltage. *Strings* 4 and 5 are responsible to filter the AC voltages of *Strings* 1 and 2. In this paper, the amplitude of the AC circulating current is 1500A, which is equal to the DC current. In consequence, the amplitude of the AC voltage is twice the DC port voltage because the exchanging AC power is

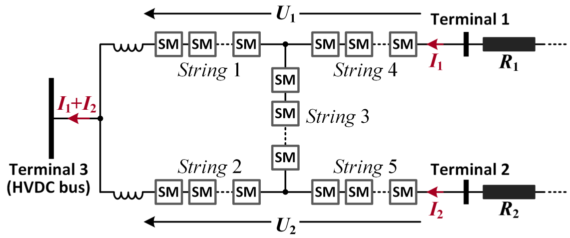

Fig. 10. Topology of the ringlike I-CFC [26].

TABLE II
COMPONENT COUNTS OF THE HMI-CFC AND THE RINGLIKE I-CFC

Quantity	Ringlike I-CFC [26]	HMI-CFC
Maximum current of IGBTs	3000A	1500A
No. of SMs	30×2+20+20×2=**120**	3×10=**30**
No. of IGBTs	4×120=**480**	4×30=**120**
No. of thyristors	**0**	10×12=**120**

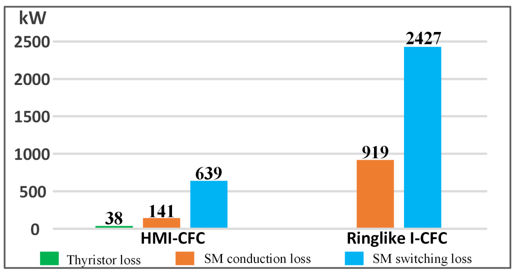

Fig. 11. Power losses comparison results.

equal to the DC power. Under the circumstances, there are 30 SMs in each of *Strings* 1 and 2, 20 SMs in *String* 3, and 20 SMs in each of *Strings* 4 and 5. As a consequence, although HMI-CFC requires additional 120 thyristors, the SM strings only need to match the DC port voltages. Therefore, the number of SMs and IGBTs in HMI-CFC are much less.

Fig. 11 further shows the power losses comparison results. The same PSC-PWM modulation is adopt in both the two CFCs, hence the switching frequency of SMs in HMI-CFC and ringlike I-CFC is the same, i.e. 650Hz. For the proposed HMI-CFC, the losses consist of two parts, i.e., thyristor loss and SM loss. On the other hand, the losses of ringlike I-CFC only include SM loss. However, the on-state voltage of each thyristor is only about 1.3V, therefore their power losses are only 38kW. In the proposed HMI-CFC, there are a total of 30 SMs, and the SM conduction and switching losses are 141kW and 639kW, respectively. As for the ringlike I-CFC, there are a total of 120 SMs, which results in much higher SM conduction and switching losses (919kW and 2427kW, respectively). For the studied 4500MW meshed HVDC grid, the total power loss of the fully loaded 20MW HMI-CFC is 818kW, which is far less than the 3346kW of the ringlike I-CFC.

VI. EXPERIMENTAL VALIDATION

A downscaled prototype has also been constructed and tested to further validate the proposed HMI-CFC, which is shown in Fig. 12. The test circuit is shown in Fig. 13, which is composed of a DC current source I_{total}, resistors R_1 and R_2 mimicking the line resistances, and the proposed HMI-CFC. The detailed parameters of the HMI-CFC prototype are listed in Table III.

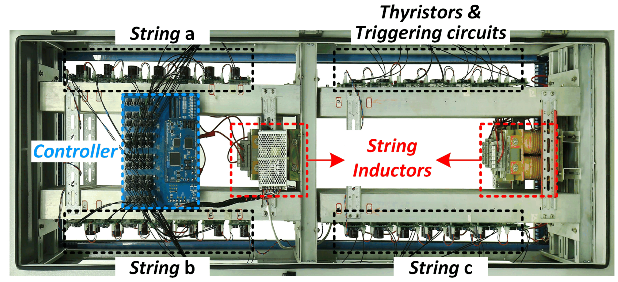

Fig. 12. Photograph of the laboratory HMI-CFC prototype.

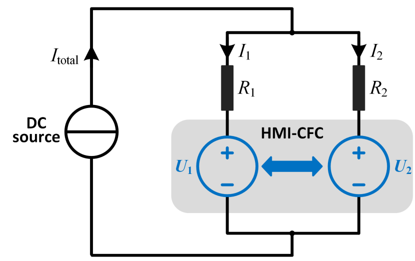

Fig. 13. Configuration of the experimental test circuit.

TABLE III
EXPERIMENTAL PARAMETERS

Parameters	Values
No. of SMs in each string	N=4
Average SM capacitor voltage	U_C=60V
SM capacitance	C=1mF
String inductance	L=2mH
PSC carrier frequency	f_c=6kHz
Alternation frequency	f=100Hz

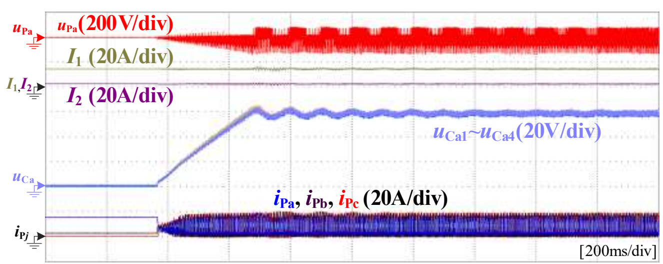

Fig. 14. Experimental results of the HMI-CFC precharge stage.

The thyristor with model Infineon "TT120N16SOF" and the IGBT with model Infineon "IKW30N60T" are used. The proposed control strategy of the HMI-CFC is realized in a TI "TMS320F28377D" DSP. Moreover, an FPGA with model ALTERA "EP3C25Q240C8" is used to implement the signal measurement, thyristor control, PSC-PWM modulation and the SM voltage balancing mechanism. The PWM signals of the thyristors and SMs are transmitted via optical fibers, and each SM is controlled by an independent ALTERA "EPM570T100" CPLD.

A. Case 1: the line currents are in the same direction

In this case, I_{total} was set to be 16A, and R_1 and R_2 were 6Ω and 42Ω, respectively. The waveforms during the precharge stage are shown in Fig. 14. At the begining, the currents of the two lines were I_1 = 14A and I_2 = 2A, respectively. Then the HMI-CFC was activated and the referenced current I_{1_ref} was set to be equal to 14A, hence I_1 and I_2 remained unchanged during the whole precharge stage. The SM capacitors were charged

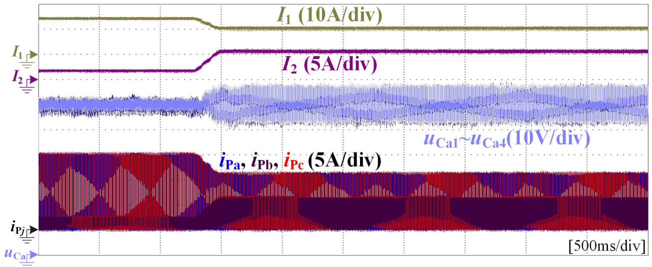

Fig. 15. Experimental results of dynamic current flow control process.

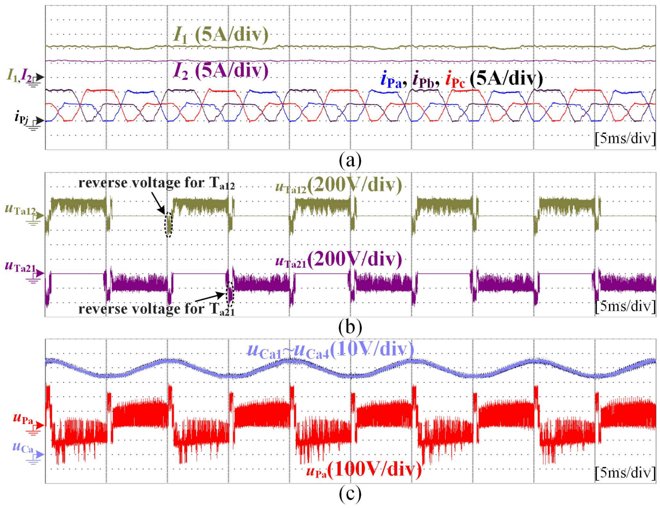

Fig. 16. Zoomed-in waveforms where the line currents are in the same direction. (a) I_1, I_2, i_{Pa}, i_{Pb} and i_{Pc}. (b) u_{Ta12}, u_{Ta21}. (c) u_{Pa} and u_{Ca1}~u_{Ca4}.

from 0V to the rated value 60V. And the HMI-CFC was ready to regulate the line current.

Fig. 15 shows the experimental results of the dynamic current flow control process. After the precharge stage, the HMI-CFC began to regulate the line current I_1 and the referenced current I_{1_ref} was changed from 14A to 10A, so as to lighten the heavy load of I_1. It can be observed that I_1 was reduced from 14A to 10A, and the redundant 4A load was transferred to I_2, making it changed from 2A to 6A. The line currents were smooth during the whole process. The SM capacitor voltages u_{Ca1}~u_{Ca4} were well balanced around the rated value 60V. The experimental results demonstrate the validity of the proposed HMI-CFC when the line currents are in the same direction.

Fig. 16 further shows the zoomed-in waveforms after the HMI-CFC was activated. As shown in Fig. 16(a), i_{Pa}, i_{Pb} and i_{Pc} were trapezoidal waveforms interleaved with 120° electrical angles with amplitudes of 10A and 6A, which synthesized continuous I_1 and I_2, without any filtering effort. Moreover, in Fig. 16(b), reverse voltage for the thyristors turn-off can be observed in u_{Ta12} and u_{Ta21}, after the thyristor current declines to zero. The reverse voltage is maintained for 300μs, which is larger than t_q = 200μs of the adopted thyristor. In addition, as shown in Fig. 16(c), the string voltage u_{Pa} alternately inserted U_1 = 72V and U_2 = -120V into the two lines, which is in accordance with (3). Moreover, the ripple of the SM capacitor voltages was about 10V, which matches the theoretical result from (11).

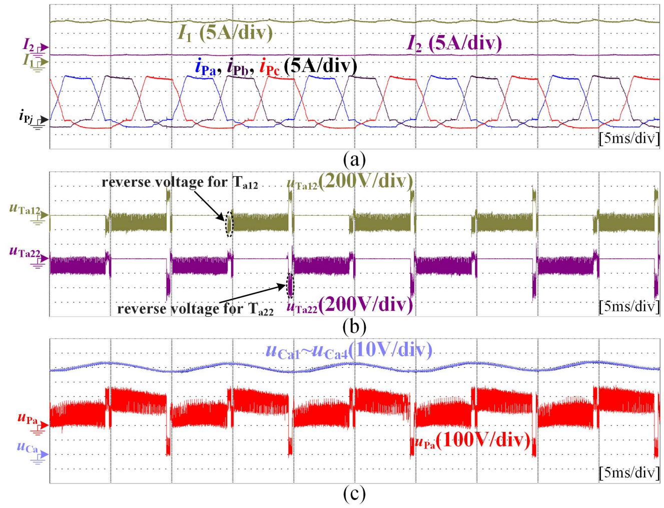

Fig. 17. Zoomed-in waveforms where the line currents are in opposite directions. (a) I_1, I_2, i_{Pa}, i_{Pb} and i_{Pc}. (b) u_{Ta12}, u_{Ta22}. (c) u_{Pa} and u_{Ca1}~u_{Ca4}.

B. Case 2: the line currents are in opposite directions

In this case, I_{total} was set to be 12A, and R_1 and R_2 were 6Ω and 18Ω, respectively. When the CFC was bypassed, I_1 and I_2 were 9A and 3A, respectively. Then the CFC was activated to make I_2 reverse, which was aimed at verifying the current flow controllability when the line currents are in opposite directions. The reference current of I_1 was set to be 14A, then I_2 was -2A. As shown in Fig. 17(a), i_{Pa}, i_{Pb}, i_{Pc} were trapezoidal waveforms with the amplitudes of 14A and -2A, and interleaved with 120° electrical angles. Hence, I_1 and I_2 were continuous and fully controlled as expected. Reverse voltage for thyristor turn-off can also be observed in u_{Ta12} and u_{Ta22} in Fig. 17(b). As shown in Fig. 17(c), the string voltage u_{Pa} was equal to U_1 = 20V and U_2 = 140V alternately, which agrees with (3). And the SM capacitor voltages u_{Ca1}~u_{Ca4} were well balanced around the rated value 60V, and the SM capacitor voltage ripple was about 4V, which is also in accordance with (11).

VII. Conclusion

A novel HMI-CFC is proposed in this paper to facilitate the line current flow control for meshed HVDC grids with large power and long-distance transmission lines. Compared to the classic ringlike I-CFC, the proposed HMI-CFC avoids injecting AC circulating current into the SM strings, therefore no additional AC voltage components are required by the SM strings. Consequently, both the number of SMs and power losses can be reduced significantly. The proposed HMI-CFC has good scalability due to its modular structure, which is applicable to applications needing high voltage and large power capacity. The two ports of the HMI-CFC can simultaneously insert DC voltages into the lines, hence there would not be any large line current ripple despite not having any filtering effort. Operation principle and control strategy are proposed for the HMI-CFC, which are verified by simulations and experiments. The proposed HMI-CFC can be a promising equipment facilitating the development of large-scale meshed HVDC grids.

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Shuxin Zhang received the B.S. and M.S. degrees in electrical engineering from Northeast Electric Power University, Jilin, China, in 2011 and 2016, respectively. He is currently pursuing the Ph.D. degree in electrical engineering at Harbin Institute of Technology. His research interests include modular multilevel converters, high voltage DC/DC converters and DC power flow controller.

Binbin Li (S'15, M'17) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2010, 2012, and 2017, respectively. From 2015 to 2016, he was a Visiting Researcher with the Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow, U.K. He is currently an Associate Professor with the Department of Electrical Engineering, Harbin Institute of Technology, and he has been selected in the Young Elite Scientists Sponsorship Program by China Association for Science and Technology. His research interests include modular power converters, HVDC grid, and MVDC collection/distribution system.

Wei Wang (M'13) received her B.S. degree in Automatic Test and Control from Harbin Institute of Technology, Harbin, China, in 1984, her M.S. degree in Electrical Engineering from Harbin Institute of Technology in 1990, and her Ph.D. degree in Mechanical Electronic Engineering from Harbin Institute of Technology in 2002. In 1984, she joined Harbin Institute of Technology, as an Assistant Professor in the Department of Electrical Engineering, where she was an Associate Professor from 1995 to 2003, and where she has been a Professor since 2003. Her current research interests include regenerative energy converter techniques, micro-grid, soft-switching converters, and lighting electronic technology.

Yujie Zhang was born in 1996. She received the B.S. degree in electrical engineering from Harbin Institute of Technology, Harbin, China, in 2019. She is currently pursuing the M.S. degree in power electronics with the Harbin Institute of Technology, Harbin, China. Her current research interests include high-voltage large-capacity DC/DC converter.

Dianguo Xu (M'97, SM'12, F'17) received the B.S. degree in Control Engineering from Harbin Engineering University, Harbin, China, in 1982, and the M.S. and Ph.D. degrees in Electrical Engineering from Harbin Institute of Technology (HIT), Harbin, China, in 1984 and 1989 respectively. Since 1994, he has been a Professor in the Department of Electrical Engineering, HIT. He is currently the Vice President of HIT. His research interests include renewable energy generation technology, multi-terminal HVDC system based on VSC, power quality mitigation, high performance PMSM servo system. Prof. Xu is an Associate Editor of the IEEE Transactions on Industrial Electronics, IEEE Transactions on Power Electronics, and the IEEE Journal of Emerging and Selected Topics in Power Electronics. He also serves as Chairman of IEEE Harbin Section.

Gen Li (M'18) received the B.Eng. degree in Electrical Engineering from Northeast Electric Power University, Jilin, China, in 2011, the M.Sc. degree in Power Engineering from Nanyang Technological University, Singapore, in 2013 and the Ph.D. degree in Electrical Engineering from Cardiff University, Cardiff, U.K., in 2018.

From 2013 to 2016, he was a Marie Curie Early Stage Research Fellow funded by the European Commission's MEDOW project. He has been a Visiting Researcher at China Electric Power Research Institute and Global Energy Interconnection Research Institute, Beijing, China, at Elia, Brussels, Belgium and at Toshiba International (Europe), London, U.K. He has been a Research Associate at the School of Engineering, Cardiff University since 2017. His research interests include control and protection of HVDC and MVDC technologies, power electronics, reliability modelling and evaluation of power electronics systems.

Dr. Li is a Chartered Engineer in the U.K. He is an Associate Editor of the CSEE Journal of Power and Energy Systems. He is an Editorial Board Member of CIGRE ELECTRA. He is an IET Professional Registration Advisor. His Ph.D. thesis received the First CIGRE Thesis Award in 2018. He is the Vice-Chair of IEEE PES Young Professionals and the Technical Panel Sectary of CIGRE UK B5 Protection and Automation.

Jun Liang (M'02-SM'12) received the B.Sc. degree in Electric Power System & its Automation from Huazhong University of Science and Technology, Wuhan, China, in 1992 and the M.Sc. and Ph.D. degrees in Electric Power System & its Automation from the China Electric Power Research Institute (CEPRI), Beijing, in 1995 and 1998, respectively.

From 1998 to 2001, he was a Senior Engineer with CEPRI. From 2001 to 2005, he was a Research Associate with Imperial College London, U.K. From 2005 to 2007, he was with the University of Glamorgan as a Senior Lecturer. He is currently a Professor in Power Electronics with the School of Engineering, Cardiff University, Cardiff, U.K. He is the Coordinator and Scientist-in-Charge of two European Commission Marie-Curie Action ITN/ETN projects: MEDOW (€3.9M) and InnoDC (€3.9M). His research interests include HVDC, MVDC, FACTS, power system stability control, power electronics, and renewable power generation.

Prof. Liang is a Fellow of the Institution of Engineering and Technology (IET). He is the Chair of IEEE UK and Ireland Power Electronics Chapter. He is an Editorial Board Member of CSEE JPES. He is an Editor of the IEEE Transactions on Sustainable Energy.