Analysis and Protection of Converter-Side AC Faults in a Cascaded Converter-Based MVDC Link: ANGLE-DC Project

Wei Liu, *Member, IEEE*, James Yu, Gen Li, *Member, IEEE*, Jun Liang, *Senior Member, IEEE*, Carlos E. Ugalde-Loo, *Senior Member, IEEE*, and Andrew Moon

***Abstract*—Medium-voltage direct-current (MVDC) technology exhibits advantages over ac transmission due to its enhanced capacity, controllability, and flexibility. A practical example is the ANGLE-DC project from Scottish Power Energy Networks, which converts existing 33 kV ac circuits into dc operation to improve the system transmission capacity in North Wales, U.K. Specially designed cascaded power converters are employed to build up the ±27 kV dc link voltage. Within the converter stations, converter-side single-phase ac faults may threaten the safe operation of the converters. This paper presents an analysis of such faults for an MVDC link based on ANGLE-DC. It is shown that the capacitors of the converters will be overcharged without suitable protection in place. A protection strategy using a bypass thyristor-based branch is presented to relieve overvoltage issues following converter-side faults, and it is verified through simulations conducted in PSCAD/EMTDC. For completeness, case studies considering post-fault operation are also included.**

***Index Terms*—AC/DC conversion, cascaded converter, converter-side ac fault, hybrid AC/DC, distribution network.**

I. Introduction

MEDIUM-VOLTAGE direct-current (MVDC) technology has attracted significant interest in the area of distribution networks due to its enhanced transmission capacity, control flexibility, and improved power quality compared to traditional ac technology [1]–[3]. Distribution networks, for decades, have acted as links between transmission systems and consumers. AC technologies have been regularly adopted at the distribution level as they are technically efficient when power generation and connected electric loads are dominated by ac [4].

With the development of dc power generation, including solar power plants [5] and some types of wind power plants [6], and with the inclusion of energy storage systems [7] and dc electric loads such as electric vehicles [8], hybrid ac/dc distribution networks are required. Although ac/dc networks are more complex than pure ac distribution networks, they offer a higher flexibility and efficiency [9]. By including dc connections, the number of power conversion stages may be reduced, leading to decreased power losses and capital costs.

Several practical projects to build MVDC networks have been planned in recent years and a few are already operational [10]–[14]. Reference [10] reports a demonstration project in which underground grids were built in the campus of RWTH Aachen University, Germany, while [11] presents a multi-terminal MVDC project constructed in Zhuhai, China, to provide reliable power supply to distribution networks. In Shanghai, China, a ±30 kV dc system with a power rating of 18 MW was built, which connects a wind farm to a 35 kV ac grid [12]. This initial deployment demonstrates that converting existing ac cables or overhead lines into dc operation offers promising solutions to increase the power capacity of transmission lines [13].

A practical example in the U.K. is the ANGLE-DC project, Europe's first MVDC link, which converted existing 33 kV double-circuit ac lines between the Llanfair substation in the island of Anglesey and the Bangor substation at mainland North Wales to ±27 kV dc. This is shown in Fig. 1 [14] and Fig. 2. Such a conversion enables an increased transmission

Fig. 1. ANGLE-DC project [14].

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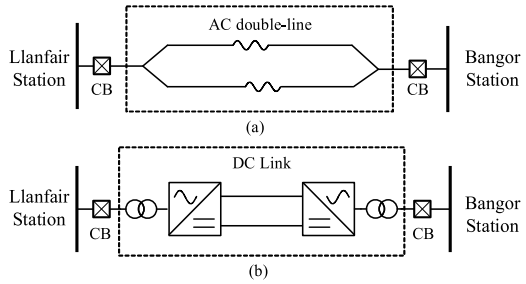

Fig. 2. ANGLE-DC project: conversion from ac into dc. (a) Existing double-circuit ac lines (33 kV). (b) Converted MVDC link (±27 kV dc).

capacity by 23% using the same circuit conductors [15], [16]. This was required due to (i) the increased renewable power generation in Anglesey and a substantial growth in demand of around 11%, expected to reach 81 MW by 2023 [17], (ii) voltage stability concerns, and (iii) ac lines connected to mainland reaching their thermal limits. In addition to tackling the previous issues, the converters at the terminals can flexibly regulate power flows and operate as STATCOMs to support nearby ac networks.

Significant research within ANGLE-DC has been carried out, with attention dedicated to feasibility and reliability analysis [18], start-up sequences, dc fault handling, and fault ride-through of grid-side ac faults [16]. However, converter-side ac faults remain an under-researched area. Such internal faults, which could be caused by the insulation failure of transformer's wall bushings or windings, have been observed in HVDC systems [19]–[21], with protection methods being assessed for modular multilevel converter (MMC) based HVDC grids [22]–[25]. Notwithstanding, attention is required for MVDC systems, particularly to the specially designed cascaded converters employed in ANGLE-DC (see Section II).

Due to the differences in converter topology and system configuration, the cascaded converter-based MVDC system exhibits different fault characteristics compared to MMC-based systems, which makes the protection methods in [22]–[25] not applicable to a cascaded 3L-NPC converter. Further studies still need to be carried out for a system like the one in ANGLE-DC.

Compared to grid-side ac faults, which occur in the transmission line, the possibility of converter-side ac faults is lower. However, since the fault location is much closer to the converters, without a proper protection scheme in place, the fast transients upon fault occurrence may endanger the converters. For instance, overcurrent and overvoltage could be exhibited, which may damage the converters and the MVDC system. Compared to other applications, the cascaded converter-based system exhibits unique characteristics following the fault. Such behavior has not been revealed in single converter-based systems. Detailed analyses are thus required and adequate protection methods needed. To bridge this gap, the characteristics of converter-side single-phase ac faults are analyzed and their effects assessed in this paper. A thyristor-based method is presented to protect the converters following the fault. For completeness, post-fault operation of the system is also examined. The effectiveness of the protection strategy is supported through computer simulations conducted in PSCAD/EMTDC.

II. System Configuration

A. System Configuration of ANGLE-DC

A schematic of one converter station and the dc link of the ANGLE-DC project is shown in Fig. 3. The system employs a symmetrical monopolar configuration (±27 kV dc) to fully utilize the power capacity of the retrofitted 33 kV double-circuit ac transmission lines [15]. The transmission lines consider both cables and overhead lines. The length of cables is ∼2.4 km and the length of the overhead lines is ∼0.6 km. The system is grounded with resistor R_g at the neutral point of its dc-side. This resistor provides a grounding potential but does not carry load current under normal operating conditions and, thus, will not influence the system performance. The dc currents only flow through the positive and negative poles of the dc link. However, when a dc fault occurs, R_g will help to limit the magnitude of the fault current [16].

Cascaded converters (connected in series at their dc-sides) are used to build up the ±27 kV dc voltage at the dc link, as shown in Fig. 3. Each pole consists of six converter cells (i.e., #1 to #6). Each cell is a three-level neutral-point-clamped (3L-NPC) converter. The detailed topology of the converter cell is shown in Fig. 4. This configuration was selected since the voltage ratings of the semiconductor devices may be reduced to half compared to a traditional two-level converter, while the efficiency and the output power quality are increased. The cells are connected with the ac grid through a multi-winding interface transformer. As shown in Fig. 4, the interface transformer separates the ac zone into the grid-side and converter-side. The grid-side refers to the area between the connected ac grid and the primary side of the transformer (see the green shaded area). The converter-side refers to the area between the secondary side of the transformer and the converter cells (see the red shaded area). Delta windings are configured at the converter-side to isolate zero-sequence components between the grid-side and the converter-side. The grounding point is set in the grid-side of the transformer.

B. System Control

The block diagram for the control of the cascaded converters in the MVDC link is given in Fig. 5 and this is based on cascaded loops. The outer control loop at one terminal regulates active power P and, conversely, dc link voltage V_{dc} at the other terminal. Reactive power Q is regulated at both terminals. Vector control in a synchronous dq-reference frame is adopted for the inner current control loops. Voltage balancing control loops are included as well to balance the capacitor voltages.

C. DC-Side Voltage

As shown in Fig. 3, the dc link voltage of each pole is built up by six cascaded 3L-NPC converter cells. Thus, the relationship between the dc voltage of each cell and dc link

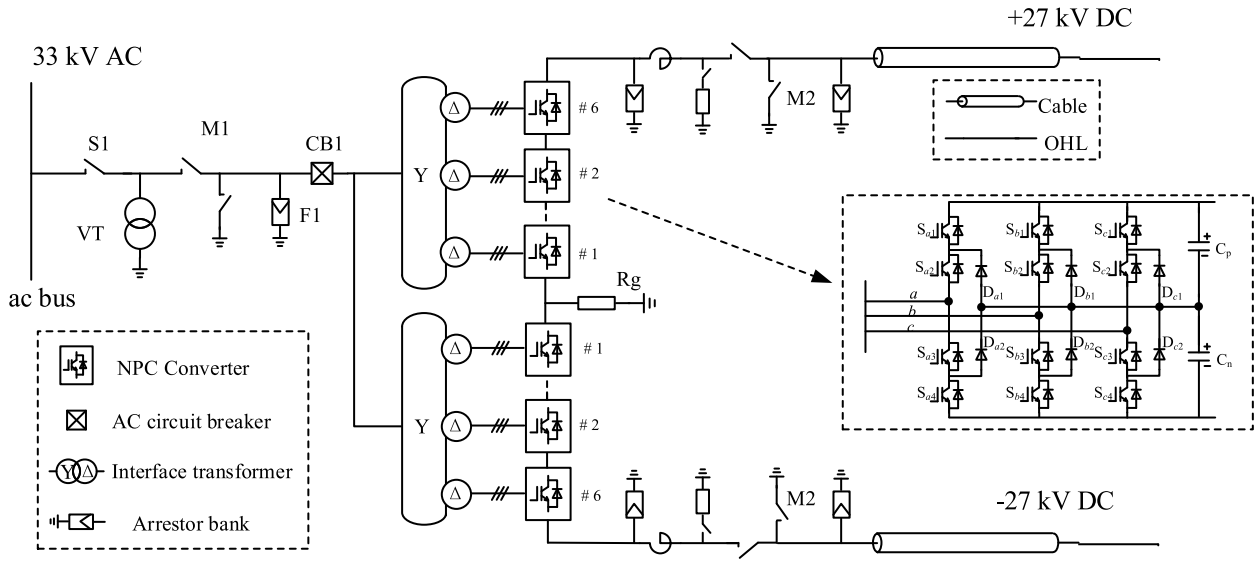

Fig. 3. System configuration of the ANGLE-DC project with cascaded 3L-NPC converters.

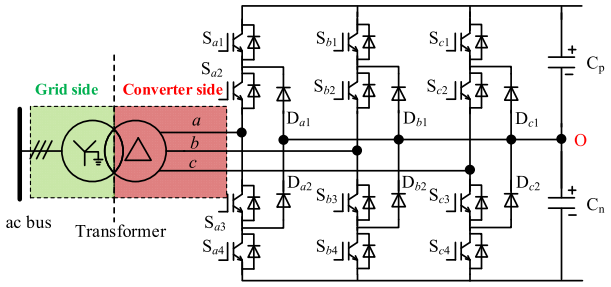

Fig. 4. Topology of 3L-NPC converter cell with interface transformer.

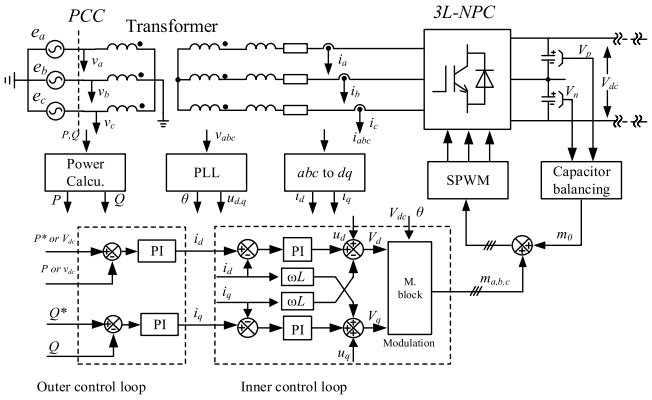

Fig. 5. Control block diagram of the cascaded 3L-NPC converters.

is expressed as

$$U_{dc} = 6V_{dc} \tag{1}$$

where U_{dc} is the rated dc link voltage and V_{dc} is the rated dc voltage for each cell.

As shown in Fig. 6(a), due to the cascaded connection at the dc-side, the dc voltage of each cell referred to the grounding point contains an offset value ${V_o}^n$. This voltage at the neutral point of each cell (i.e., mid-point of the two capacitors in the

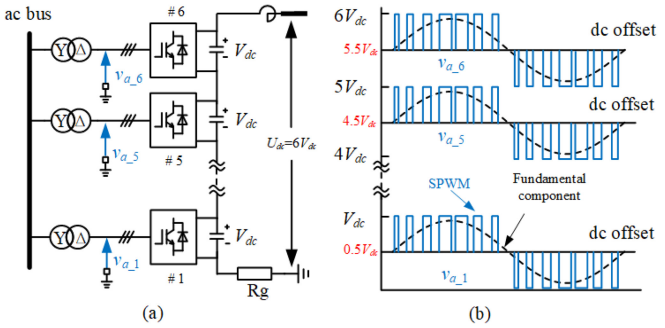

Fig. 6. Relationship of ac-and dc-side voltages. (a) DC-side (b) AC-side.

3L-NPC cell) is expressed as

$$V_o^n = 0.5V_{dc} + (n-1)V_{dc} = (n-0.5)V_{dc}, (n \in 1-6) \tag{2}$$

where n represents the cell number. From (2), it can be seen that the 6th cell contains the largest offset voltage, with a value of $5.5V_{dc}$. Such an offset will reflect on the voltages of the ac-side.

D. AC-Side Voltage With DC Offsets

When the fundamental components are considered in the ac-side of a 3L-NPC converter cell only, phase-to-neutral voltages referred to the cell's neutral point O (see Fig. 4) are given as

$$v_x = \sqrt{2}V_{ac}\sin(\omega t + \varphi_x), \quad (x = a, b, c) \tag{3}$$

where v_x is the phase-to-neutral voltage of the converter cell, V_{ac} the root mean square (rms) value of the phase voltage, and φ_x the phase angle. However, the ac-side phase-to-ground voltages referred to the ground potential are expressed as

$$v_{xg}^n = v_x + V_o^n = \sqrt{2}V_{ac}\sin(\omega t + \varphi_x) + V_o^n \tag{4}$$

where ${v^n}_{xg}$ is the phase-to-ground voltage of the n^{th} converter cell and ${V_o}^n$ the offset voltage reflected on the neutral point of the n^{th} converter.

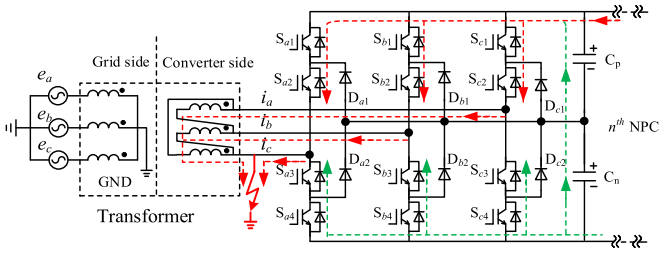

Fig. 7. Zero-sequence current path following a converter-side fault at phase c.

From (4), it can be observed that the ac voltage for each cell will contain a dc offset. This is exemplified in Fig. 6(b), where phase-to-ground voltages of phase *A* for each cell are shown. Both the pulse-width modulation (PWM) and the fundamental components are included. For instance, the ac-side phase-to-ground voltages of the 6th cell, connected to the dc link directly, contain the highest offset of $5.5V_{dc}$, which is consistent with the discussion by the end of Section II-C. For a system like this, the windings of the interface transformers should be thus designed to specifically withstand dc offset voltages under normal operating conditions.

It should be noted that once an ac fault occurs at the converter-side, the dc offsets will be removed. A large inrush current will be induced and the capacitors of the converter cells may be overcharged. Conventional protection methods for grid-side ac faults are not applicable for converter-side ac faults and, thus, suitable methods against converter-side ac faults are still required.

III. Analysis of Converter-Side AC Faults

A. Overcurrent Analysis

Due to no zero-sequence path existing at the converter-side of the delta connected transformers, there is no zero-sequence current flowing through the converters. However, when a converter-side grounding fault occurs, paths for zero-sequence current are created, as shown in Fig. 7 (see the red and green dashed lines). This leads to a significant increase of current magnitude in the faulted converter cell. The contribution to fault current mainly comes from two components initially: the current from the dc link (red lines) and the discharging current of dc capacitors in the 3L-NPC converter cells (green lines). Under such circumstances, the converters will have to block their gate signals to protect the IGBTs from overheating.

An equivalent circuit after all the IGBTs are blocked is given in Fig. 8. It can be observed that although the converters are blocked by switching off the IGBTs, the fault current still flows from the freewheeling diodes in the lower arms of the faulted converter cell. The current from the dc link is transferred from the IGBTs to the capacitors in the cell (see red dashed lines).

Equivalent circuits for the discharging processes of the dc link and dc capacitors within the converter cells are given in Fig. 9. As shown in Fig. 9(a), the dc link current will flow through the capacitors and diodes into the fault point. A system of two first order differential equations is derived from this

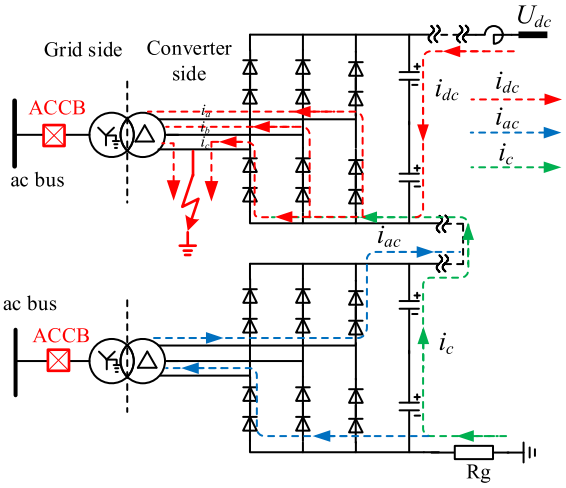

Fig. 8. Current paths through the diodes after blocking of converters.

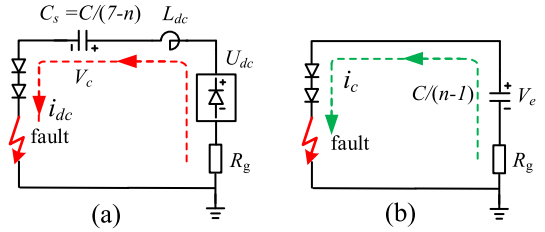

Fig. 9. Equivalent circuits after the fault. Discharging of: (a) dc link; (b) dc capacitors in converter cells.

circuit as follows:

$$\begin{cases} L_{dc}\frac{di_{dc}(t)}{dt} + R_g i_{dc}(t) + v_c(t) = U_{dc} \\ C_s\frac{dv_c(t)}{dt} = i_{dc}(t) \\ C_s = \frac{C}{N} = \frac{C}{7-n} \end{cases} \tag{5}$$

$$\begin{cases} v_c(0_+) = NV_{dc} = (7-n)V_{dc} \\ i_{dc}(0_+) = I_{dc} \end{cases} \tag{6}$$

where U_{dc} is the dc link voltage fed by the healthy terminal, L_{dc} the inductance of the dc link,C is the capacitance of one 3L-NPC converter cell,$i_{dc}(t)$ the dc link current, $v_c(t)$ the capacitor voltage in series with the dc link following the fault, C_s the capacitor in series with the dc link, and N the number of capacitors in series with the dc link. It should be noted that the values of C_s, v_c(t), and N depend on the fault location. When a fault occurs at the n^{th} cell, $N = 7 - n$.

Solving (5) for $i_{dc}(t)$ and $v_c(t)$ considering (6) yields

$$\begin{cases} v_c(t) = K_1 e^{s_1 t} + K_2 e^{s_2 t} + U_{dc} \\ i_{dc}(t) = C_s\left(K_1 s_1 e^{s_1 t} + K_2 s_2 e^{s_2 t}\right) \end{cases} \tag{7}$$

where the s_1 and s_2 are the roots of the characteristic equation for system (5) and constants K_1 and K_2 depend on the initial conditions (6). It should be highlighted that the fault location will have a strong influence on the overcurrent magnitude since the number of capacitors in series with the dc link may change depending on the fault position (i.e., n will change with fault location). This will be verified in Section V-C.

Besides the current from the dc link, the capacitors in the 3L-NPC converter cells also discharge through the diodes into

the fault point (see green dashed line in Fig. 8). The discharging process at the beginning of the fault is represented by the *RC* equivalent circuit shown in Fig. 9(b). The current contributed by the capacitors is expressed as

$$i_c(t) = \frac{V_e}{R_g} e^{-\frac{t}{\tau}} \tag{8}$$

$$V_e = (n-1)V_{dc} \tag{9}$$

$$\tau = \frac{R_g C}{n-1} \tag{10}$$

where V_e is the sum of capacitor voltages during the fault, τ is the time constant of the circuit, and C is the capacitance of one 3L-NPC converter cell.

It can be seen from (8)-(10) that the peak value of the fault current is determined by capacitor voltage V_e and the grounding resistor R_g. The maximum value appears when a fault occurs in the nearest converter to the dc link (i.e., $n = 6$),

$$i_{peak} = \frac{V_e}{R_g} = \frac{5V_{dc}}{R_g} \tag{11}$$

Since fault current will flow through the diodes of the faulted converter, it is important to carefully select the value of R_g to ensure that the surge current remains within the diode's safe region of operation under a converter-side ac fault. For instance, a 10Ω resistor is used in the ANGLE-DC project [16].

It should be highlighted that when the voltage of the capacitors is lower than the peak value of the line-to-line voltage from the ac-side, the 3L-NPC converter cells will behave as a diode rectifier and will keep injecting current to the fault point (see blue dashed lines in Fig. 8) through the transformer. AC-side circuit breakers (ACCBs) need to be switched off to interrupt the fault current permanently.

B. Overvoltage Analysis

As discussed in the previous section, after blocking the converters, the fault current fed by the dc link will transfer from the IGBTs into the capacitors C_s in the 3L-NPC converters [see Fig. 9(a)]. According to (5)-(7), the capacitors in series with the dc link will be charged to the dc link voltage value, that is,

$$v_c(\infty) = U_{dc} \tag{12}$$

$$V_{dc(\infty)} = \frac{U_{dc}}{N} = \frac{U_{dc}}{7-n} \tag{13}$$

where $V_{dc(\infty)}$ is the steady-state capacitor voltage of the converter cell after the fault. As discussed, the fault will be more severe when it occurs at the cell closest to the dc link as the capacitor will be charged to the dc link voltage U_{dc}. The overcharged capacitor will lead to an overvoltage of the IGBT devices which could, in turn, damage the 3L-NPC converter cell. Under such circumstances, switching off the ACCB may not occur in time to avoid the overvoltage since its operating time is 40-100 ms, which is not fast enough. To address this issue, a protection method is presented in Section IV.

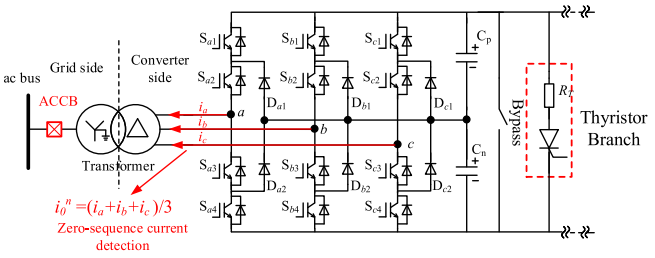

Fig. 10. Thyristor branch-based protection method.

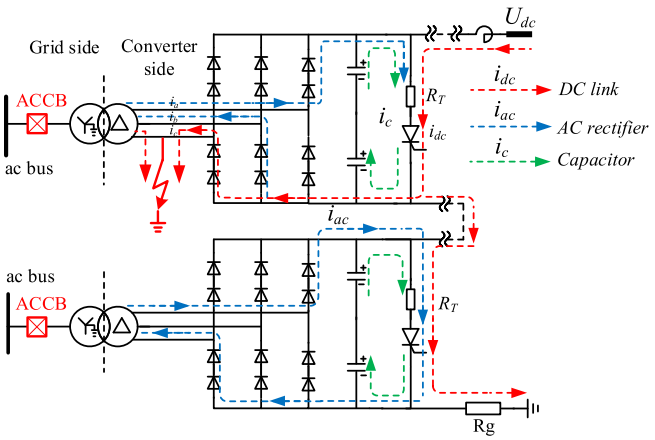

Fig. 11. Current paths after blocking of converters with thyristor branch.

IV. Thyristor-Based Protection Method

A. Fault Detection

Given that zero-sequence currents indicate a converter-side fault, their presence can be used to distinguish from other types of faults (e.g., from grid-side ac or dc-side). The zero-sequence current is expressed as

$$i_0^n = (i_a + i_b + i_c)/3 \tag{14}$$

where $i_0{}^n$ is the zero-sequence current at the converter-side of the n^{th} 3L-NPC converter cell. When the magnitude of current $|i_0{}^n|$ is higher than a pre-defined threshold, it can be concluded that a converter-side fault has occurred.

B. Thyristor-Based Protection Method

A thyristor-based branch is installed in parallel with the 3L-NPC converter cell, as shown in Fig. 10, to protect the converter from overvoltage. When a converter-side fault is detected, all the thyristors at the faulted terminal are triggered and, as a result, the dc link current will flow through the branch instead of charging the capacitors (as described in Section III-B).

The equivalent circuit following triggering of the thyristor-based branch is given in Fig. 11. Part of the discharging currents coming from the capacitor within the cells flows through the branch, which further protects the diode from overcurrent.

It should be noticed that a resistor needs to be in series with the thyristor-based branch to prevent large inrush current generated by its parallel capacitor. Initially following a fault, the dc capacitor discharges through the thyristor-based branch.

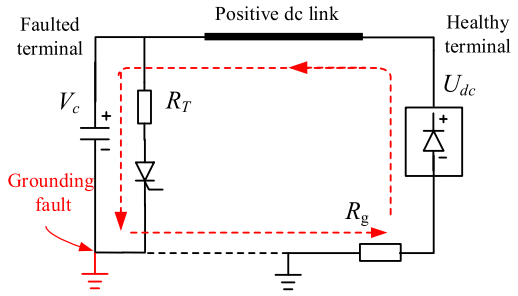

Fig. 12. Equivalent circuit of the post-fault condition (fault occurs at the 6th cell).

When the capacitor voltage is lower than the line-to-line ac voltage, the ac-side operates as a rectifier and continues to contribute to fault current (see blue dashed line in Fig. 11).

C. Design of the Thyristor Branch

1) Resistor: As mentioned in the previous subsection, a resistor R_T is needed in the thyristor branch to prevent the large inrush current coming from the capacitor of the converter cell. A large resistance value leads to a small current magnitude. However, it could also lead to an overvoltage even after this branch is triggered following a fault.

An equivalent circuit following the fault (i.e., the thyristor branches have been triggered) is given in Fig. 12. The most critical case at the positive pole is given as an example, where the fault occurs at the 6th cell. Since it takes time for the ACCB to operate, namely 100 ms in this paper, the healthy terminal behaves as a diode rectifier after being blocked before the ACCB is switched off. Within such a time, the healthy terminal still provides a voltage U_{dc} to the dc link of around 18 kV. As shown in Fig. 12, U_{dc} will be shared between the grounding resistor R_g and R_T of the thyristor branch. The capacitor voltage V_c is derived as

$$V_c = \frac{R_T}{R_g + R_T} \times U_{dc} \tag{15}$$

To avoid overcharging the capacitor, V_c should be smaller than the rated voltage of the converter cells (i.e., 4.5 kV in this application). Therefore, the following criterion is adopted to select the value of the resistor:

$$V_c = \frac{R_T}{R_g + R_T} \times U_{dc} < 4.5\text{kV} \tag{16}$$

Substituting $R_g = 10\Omega$ and U_{dc} =18 kV into (16), yields

$$R_T < 3.33\Omega \tag{17}$$

For the ANGLE-DC project, R_T should be smaller than 3.33 Ω to avoid overvoltage of the converter cell. To leave some margin for transients, a resistance of 1.5 Ω is used in this paper.

2) Thyristor: Since the thyristor branches are installed in parallel with the converter cells, the rated voltage of the selected thyristors should be equal or larger than the rated voltage of the converter cell, that is,

$$V_T \geq V_{dc} = 4.5\ kV \tag{18}$$

TABLE I
NUMBER OF SEMICONDUCTOR DEVICES AND COST ANALYSIS

Semiconductors	Number of Devices	Percentage (number)	Percentage (cost)
IGBT	12	38.7%	56.07%
Diode	18	58.1%	42.06%
Thyristor	1	3.2%	1.87%

To ensure the safe operation of the thyristor, its loading integral I^2t should be also examined, i.e.,

$$I^2t = \int i_T^2 t dt \tag{19}$$

In this application, the peak value of the fault current flowing through the thyristor is ~3 kA and the duration time is around 100 ms (i.e., after 100 ms, the ACCB is switched off to interrupt the fault current). Therefore, when selecting thyristors, the I^2t should be larger than 0.9 MA^2s. This will be verified in Section V-D.

3) Economic analysis: To evaluate the cost of adding a thyristor branch, consider the information in Table I. From the table, it can be seen that, there are twelve IGBTs and eighteen diodes in one 3L-NPC converter cell. (Note: Although in some applications a diode may have been integrated into the packaging of an IGBT, diodes and IGBTs are considered as individual devices in this paper.) Since the voltage and current ratings of a thyristor can be higher than those of an IGBT, one thyristor is used in this analysis. As shown in Table I, the presented protection method only brings a 3.2% increase in the number of semiconductor devices. Since the price of a thyristor is lower than that of an IGBT or a fast recovery diode, the extra cost incurred by adding a new thyristor could be lower than 3.2%. Assuming that the price of a fast recovery diode is 50% of an IGBT and the price of a thyristor is 40% of an IGBT, the cost of the additional thyristor would be around 1.87%.

(Note: The semiconductor devices normally dominate the costs of a converter and are thus here considered only. Other components, such as cooling plates, IGBT drivers, and mechanical devices are not included.)

D. Fault Isolation and Post-Fault Operation

Overvoltage is effectively avoided when the thyristor branch is switched on following the fault. However, fault currents fed by the dc link and the ac-side diode rectifier still exist. To clear the fault current permanently, the ACCBs from both stations need to be switched off to ensure fault current decays to zero.

After the fault current reduces to zero, the faulted cell at the ac-side can be isolated by using additional fast disconnecters and/or ACCBs. At the dc-side, an additional mechanical switch can be used to bypass the faulted cell [see Fig. 13]. Meanwhile, other non-faulted cells can be restored for normal operation. Therefore, the presented scheme minimizes the effect of converter-side ac faults on the power transmission irrespective of the specific position of the converter cell being directly affected.

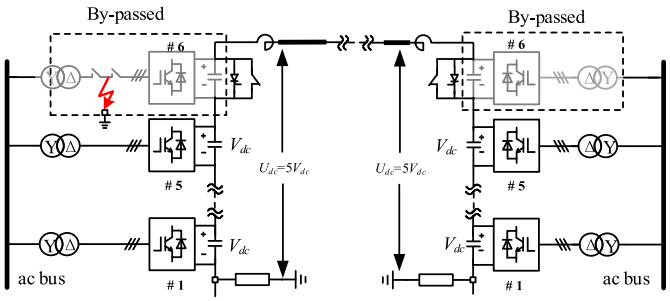

Fig. 13. Post-fault operation (only positive pole is given).

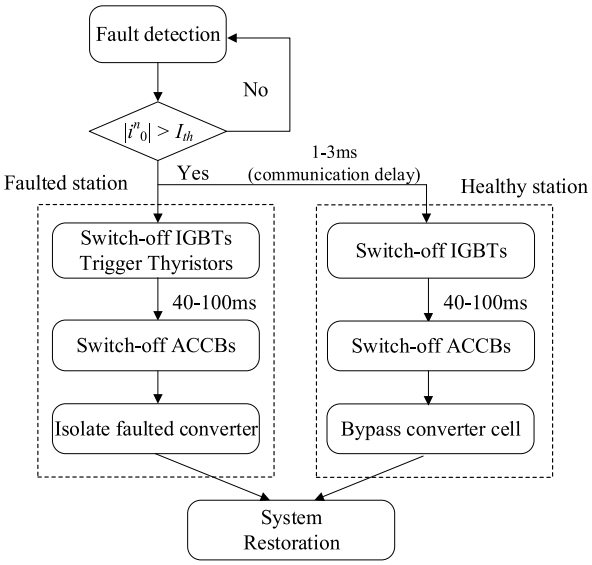

Fig. 14. Fault isolation process.

In order to match the dc voltage, a converter in the other healthy terminal should be also bypassed. After that, the whole system can be restored to an operational state without the faulted converter cell.

As shown in Fig. 3, there are twelve 3L-NPC converter cells in total for each terminal of the MVDC system (i.e., 6 cells per pole × 2 poles = 12 cells). Therefore, when one converter cell is out of operation following a fault, the number of cells that can transmit power is reduced from 12 to 11 at both terminals. The remaining power capacity is therefore

$$\eta = \frac{N-1}{N} \times 100\% = \frac{11}{12} \times 100\% = 91.6\% \qquad (20)$$

This implies that the dc link can still transfer power at 91.6% of its rated capacity. The flowchart shown in Fig. 14 summarizes the protection strategy.

V. Simulation Results and Analysis

A. System Parameters

The system shown in Fig. 3 was built in PSCAD/EMTDC to verify the analysis and the effectiveness of the protection method presented in Section IV. System parameters are given in Table II. DC transmission lines are represented by equivalent resistances and inductances. The parameters of each 3L-NPC converter cell are given in Table III. The 12 cells at each station operate in an interleaved mode to increase the total equivalent switching frequency.

TABLE II
MVDC System Parameters

Parameters	Value	Units
Rated capacity	33	MVA
Rated ac voltage	33	kV
Rated dc link voltage	± 27	kV
Transformer capacity	2.85×6×2	MVA
Transformer ratio	33/2.1	kV
Transformer leakage inductance	0.2	p.u.
Number of 3L-NPC cells	6×2	-
DC current limiting inductor	6	mH
Grounding resistor	10	Ω
Resistance of dc Transmission lines	2.1	Ω
Inductance of dc Transmission lines	2	mH

TABLE III
Parameters of 3L-NPC Converter

Parameters	Value	Units
Rated capacity	2.75	MVA
Rated dc voltage	4.5	kV
Rated ac voltage	2.1	kV
Capacitor of 3L-NPC	4600	μF
Switching frequency	750	Hz
Sample frequency	20	kHz

B. Normal Operating Conditions

Fig. 15 shows relevant waveforms of the system under normal operating conditions. The dc link voltage of the positive pole is 27 kV and the dc voltage of a single 3L-NPC cell is 4.5 kV, as shown in Fig. 15 (a) and (b), respectively. The phase-to-ground voltages of phase *A* for each 3L-NPC cell are given in Fig. 15(c). As it can be observed, the output voltages of the 3L-NPC converter cell exhibit dc offsets as analyzed in Section II-D. Specifically, for the 6th cell this is 5.5V_{dc}, which verifies equation (2). The line-to-line voltage of one 3L-NPC converter cell is shown in Fig. 15(d). The voltages contain five-level voltage steps, which is the typical operating behavior of a 3L-NPC converter. The grid-side and converter-side ac currents are given in Fig. 15 (e) and (f). As it can be observed, the grid-side current (sum up of the 12 cells) contains lower harmonics than that in the converter-side (one cell) due to the interleaved operation mode of the converter cells.

C. Blocking the Converter Only

To observe the effects of converter-side ac faults at different locations and verify the analysis presented in Section III, solid faults have been applied to the system. Since there are six cells per pole, different fault positions (i.e., different 3L-NPC converter cells) have been tested, with results shown in Fig. 16.

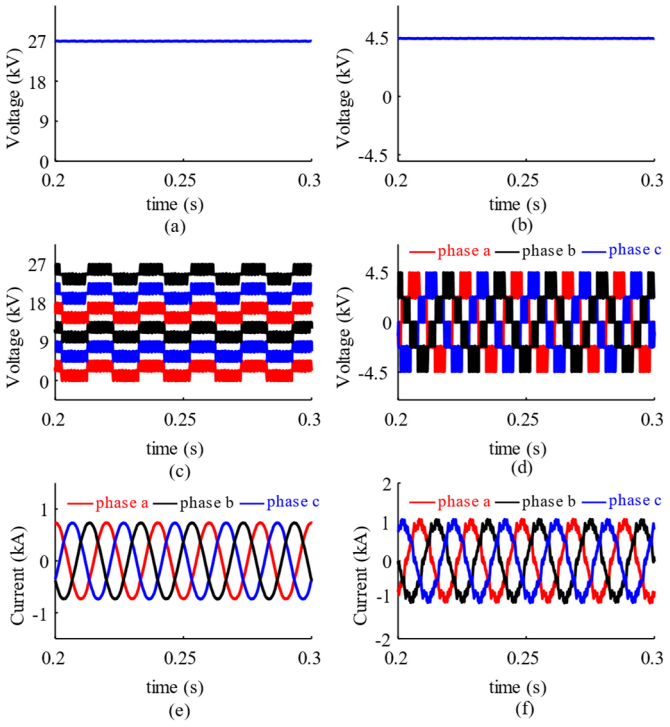

Fig. 15. Relevant waveforms under normal conditions. (a) DC link voltage. (b) DC voltage of one 3L-NPC converter cell. (c) Converter-side phase-to-ground voltages of six 3L-NPC converter cells (phase A). (d) Converter-side line-to-line voltage of one 3L-NPC converter cell. (e) Grid-side ac currents. (f) Converter-side ac currents of one 3L-NPC converter cell.

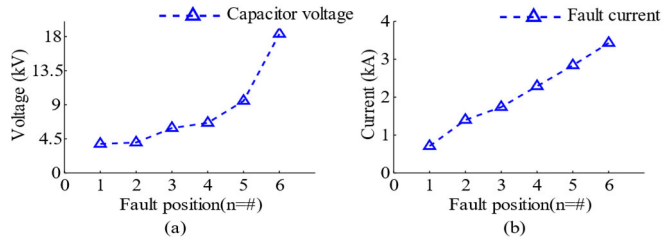

Fig. 16. Effect of the fault location. (a) Capacitor voltages. (b) Peak values of fault current.

The peak capacitor voltage and peak fault current for these locations are given respectively in Fig. 16(a) and (b). It can be seen that the most critical condition occurs when the fault occurs at the cell connecting to the dc link (i.e., $n = 6$ in Fig. 3). In this case, the capacitor is overcharged from 4.5 kV to around 18 kV and the peak fault current is ∼4 kA.

To illustrate the transient process following the fault in the most severe condition, time-domain simulation results are given in Fig. 17. The current flowing through the faulted point is shown in Fig. 17(a), with a peak value of ∼4 kA. As discussed in Section III-A, the fault current comes from two parts: the discharging current from the capacitor of the 3L-NPC converter cells [Fig. 17(c)] and the discharging current from the dc link [Fig. 17(e)]. Fig. 17(b) shows the dc link voltage following the fault. After the fault is detected, both converter stations are blocked to avoid overcurrent of IGBTs. After that, the healthy station starts behaving as a diode rectifier. The maximum dc link voltage reduces to 70-80% of the

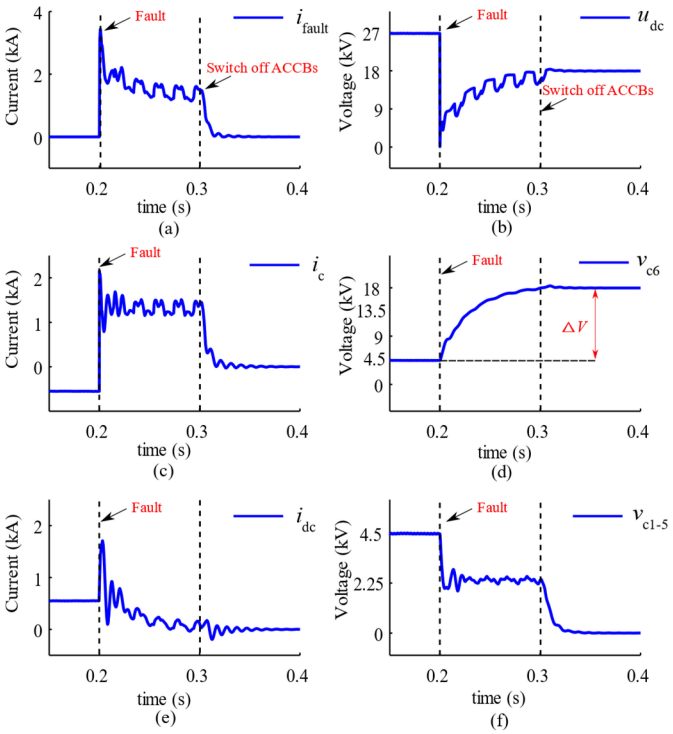

Fig. 17. Blocking the converter only when a fault occurs at n = 6. (a) Fault current. (b) DC link voltage. (c) Capacitor discharging current. (d) Capacitor voltage of the 6th cell. (e) DC link current. (f) Capacitor voltage of the cells ($n = 1, \ldots, 5$).

rated value to ∼18 kV [Fig. 17(b)], but such a voltage will still overcharge the capacitor in the faulted converter cell. This is shown in Fig. 17(d), where the capacitor in the 6th cell is charged from 4.5 kV to ∼18 kV. Therefore, blocking the converter only cannot protect the system from overvoltage. This is consistent with Fig. 16: when the fault is located at the 6th and 5th cells, the resulting overvoltage (18 and 9 kV, respectively) will damage capacitors and power electronic devices without protection in place.

D. Thyristor-Based Protection

Fig. 18 shows simulation results following a fault occurring at the 6th 3L-NPC converter cell when the protection method is in place. The thyristor-based branches are triggered once the fault is detected. As it can be observed in Fig. 18 (b), the dc link voltage at the faulted terminal reduces significantly. Thus, no overcharging occurs at the 6th 3L-NPC converter cell [Fig. 18 (d)]. By comparing Fig. 17(a) and (d) with Fig. 18 (a) and (d), not only the protection method does not increase the fault current magnitude, but it effectively eliminates overvoltage.

The current and the energy absorbed (I^2t) in one of the thyristor branches are given in Fig. 19. It can be seen that the peak current is ∼3 kA and I^2t is ∼0.4 MA^2s, which are within the safe operating area (SOA) of the selected thyristor [26].

E. Post-Fault Operation

It should be highlighted that each 3L-NPC converter cell within the cascaded structure is controlled individually. This

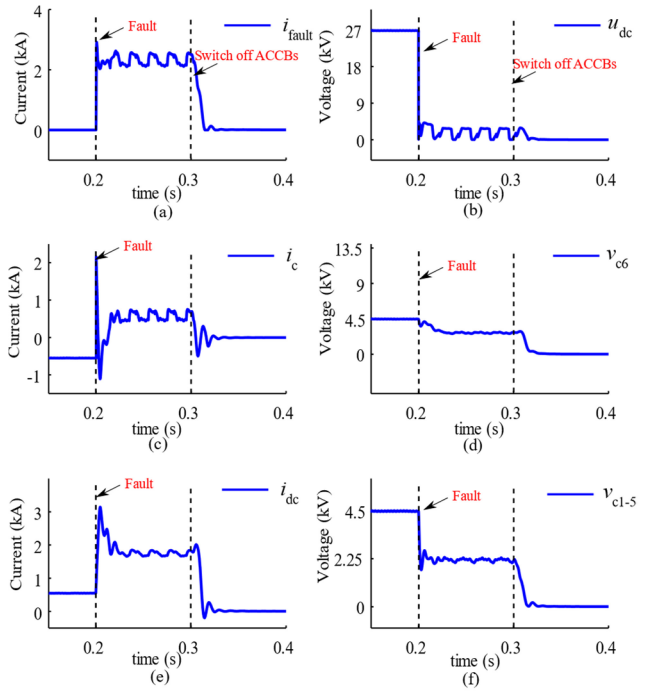

Fig. 18. Trigger the thyristor branch when a fault occurs at n = 6. (a) Fault current. (b) DC link voltage. (c) Capacitor current. (d) Capacitor voltage n = 6. (e) DC link current. (f) Capacitor voltage ($n = 1, \ldots, 5$).

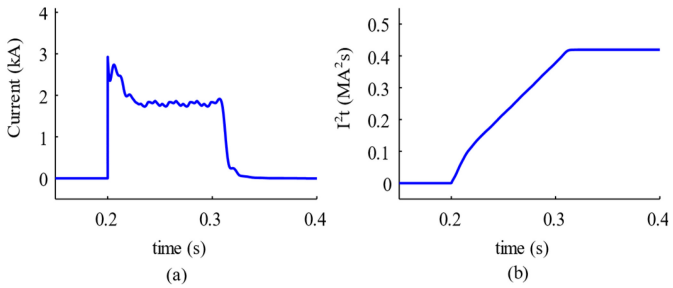

Fig. 19. Waveforms of thyristor branch. (a) Current. (b) I^2t.

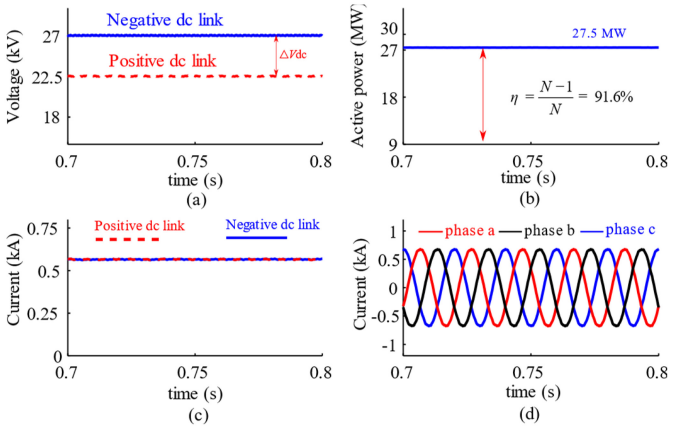

Fig. 20. Post-fault operation. (a) DC link voltage. (b) Active power. (c) DC link current. (d) Grid-side ac currents.

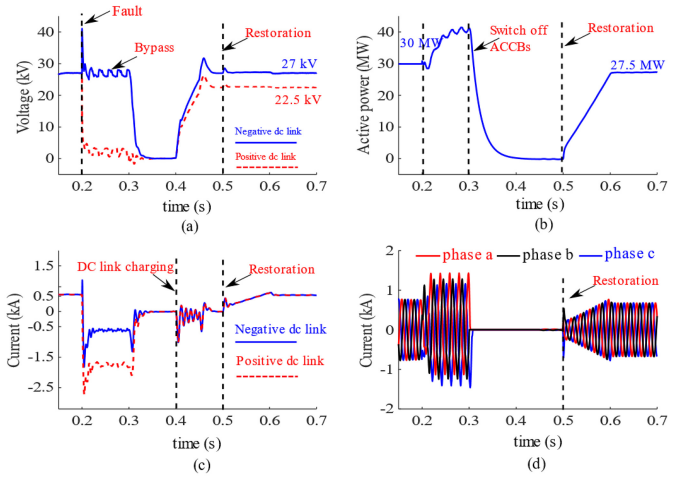

Fig. 21. System protection and restoration following a converter-side ac fault. (a) DC link voltage. (b) Active power. (c) DC link current. (d) Grid-side ac currents.

implies that after one converter cell experiences a fault, it can be isolated by disconnecters at its ac-side and bypassed at its dc-side and, more importantly, that other healthy converter cells may remain operational.

Fig. 20 shows the post-fault operation of the system when the 6th cell in the positive pole is bypassed following the fault. From Fig. 20(a), it can be seen that the voltage of the positive pole of the dc link is 22.5 kV, which is 4.5 kV lower that the negative pole. The dc link currents are given in Fig. 20(c). It can be observed that the positive and negative pole currents are the same for a post-fault condition, which means that the current in the grounding resistor remains zero. The total power transferred is 27.5 MW, which is 91.6% of the rated 30 MW due to the loss of one cell. This verifies the analysis in Section IV-D.

Fig. 21 shows the transients exhibited during the protection and restoration process following a converter-side ac fault at the 6th cell of the positive pole. The fault occurs at $t = 0.2$ s and the thyristor branches are bypassed when the fault is detected. As it can be seen in Fig. 21(a), the dc link voltage in the faulted pole is reduced to a low value (lower than 4.5 kV) after bypassing, which prevents an overvoltage in the converter cells. Due to the blocking of the converters and bypassing of the thyristor branch, the ac-side active power increases from 30 MW (i.e., normal full power conditions) to around 40 MW within 100 ms, as shown in Fig. 21(b). It can be seen from Fig. 21 (c) and 21(d), that both ac-side and dc-side currents are reduced to zero after the ACCBs are switched off at $t = 0.3$ s. After that, the system can isolate the faulted converter cell and may begin to prepare for restoration. As shown in Fig. 21(a), at $t = 0.4$ s, the system begins to re-charge its dc link and the dc link voltage is re-built at $t = 0.5$ s. Due to the removal of one converter cell in the positive pole, the post fault voltage of the positive dc link operates at 22.5 kV, which is 4.5 kV lower than the norminal 27 kV(see the red dashed line). The restoration of active power starts from $t = 0.5$ s. As shown in Fig. 21(b), the total transferred power reaches 27.5 MW, which is 2.5 MW lower compared to the pre-fault condition due to the loss of one cell. The results verify the analysis presented in Sections IV-B and IV-D.

VI. Conclusion

Scottish Power Energy Networks' ANGLE-DC, a Network Innovation Competition project funded by Ofgem, the Great Britain government regulator for gas and electricity markets, is a trial operational MVDC transmission link adopting power electronics devices to convert existing ac lines into dc operation for distribution networks. At the time of construction, ANGLE-DC was the first pilot project of its kind at an international level, aiming to smooth the way for the integration of increasing volumes of renewables and accommodating the growth of local electricity demand. As ANGLE-DC is a real practical project, thorough studies are required to ensure its operational success.

In this paper, theoretical analyses and simulation studies complementing previous work for ANGLE-DC have been conducted to reveal the transient behavior of the MVDC link following converter-side single-phase ac faults. It has been demonstrated that, if left unattended, this type of faults may severely affect the MVDC link operation. For instance, zero-sequence currents of a large magnitude are exhibited, leading to the blocking of the converter. Moreover, severe overvoltage may be present in the converter capacitors if the converter cell is directly blocked which, in turn, could lead to potential damage of the MVDC system.

To relieve the aforementioned issues, a thyristor-based branch protection strategy has been presented, with its effectiveness being verified through simulations conducted in PSCAD/EMTDC. Once the protective branch is triggered after a fault, overvoltage is effectively eliminated at the faulted converter cell. After that, ACCBs and/or disconnecters can isolate such cell without affecting the operation of the healthy cells. When the faulted cell is bypassed, the system can restore system operation to 91.6% of the rated transmission capacity. This demonstrates that even under the event of a converter-side single-phase fault, the MVDC link may remain operational at a slightly reduced capacity and power transfer may be still achieved. Within the context of the ANGLE-DC project, this has practical relevance as the presented protection scheme would avoid the need to curtail renewable generation at Anglesey should the MVDC link be placed out of service.

The analysis presented in this paper and the introduced protection method may serve as a reference for future projects and will contribute to building confidence in the deployment of MVDC technologies by other distribution network operators.

References

[1] F. Capitanescu, L. F. Ochoa, H. Margossian, and N. D. Hatziargyriou, "Assessing the potential of network reconfiguration to improve distributed generation hosting capacity in active distribution systems," *IEEE Trans. Power Syst.*, vol. 30, no. 1, pp. 346–356, Jan. 2015.

[2] S. K. Chaudhary, J. M. Guerrero, and R. Teodorescu, "Enhancing the capacity of the AC distribution system using DC interlinks—A step toward future DC grid," *IEEE Trans. Smart Grid*, vol. 6, no. 4, pp. 1722–1729, Jul. 2015.

[3] A. A. Eajal, M. F. Shaaban, K. Ponnambalam, and E. F. El-Saadany, "Stochastic centralized dispatch scheme for AC/DC hybrid smart distribution systems," *IEEE Trans. Sustain. Energy*, vol. 7, no. 3, pp. 1046–1059, Jul. 2016.

[4] F. Z. Peng, "Flexible AC transmission systems (FACTS) and resilient AC distribution systems (RACDS) in smart grid," *Proc. IEEE*, vol. 105, no. 11, pp. 2099–2115, Nov. 2017.

[5] F. Katiraei and J. Agüero, "Solar PV integration challenges," *IEEE Power Energy Mag.*, vol. 9, no. 3, pp. 62–71, May/Jun. 2011.

[6] F. Kong, C. Dong, X. Liu, and H. Zeng, "Quantity versus quality: Optimal harvesting wind power for the smart grid," *Proc. IEEE*, vol. 102, no. 11, pp. 1762–1776, Nov. 2014.

[7] B. P. Roberts and C. Sandberg, "The role of energy storage in development of smart grids," *Proc. IEEE*, vol. 99, no. 6, pp. 1139–1144, Jun. 2011.

[8] L. Mokgonyana, K. Smith, and S. Galloway, "Reconfigurable low voltage direct current charging networks for plug-in electric vehicles," *IEEE Trans. Smart Grid*, vol. 10, no. 5, pp. 5458–5467, Sep. 2019.

[9] H. M. A. Ahmed, A. B. Eltantawy, and M. M. A. Salama, "A planning approach for the network configuration of AC–DC hybrid distribution systems," *IEEE Trans. Smart Grid*, vol. 9, no. 3, pp. 2203–2213, May 2018.

[10] F. Mura and R. W. De Doncker, "Design aspects of a medium-voltage direct current (MVDC) grid for a university campus," in *Proc. 8th Int. Conf. Power Electron ECCE Asia*, Jeju, South Korea, 2011, pp. 2359–2366.

[11] L. Qu *et al.*, "Planning and analysis of the demonstration project of the MVDC distribution network in Zhuhai," *Front. Energy*, vol. 13, no. 1, pp. 120–130, 2019.

[12] "Medium voltage direct current (MVDC) grid feasibility study," CIGRE, Paris, France, CIGRE Rep. WG C6.31, 2020.

[13] L. Zhang, J. Liang, W. Tang, G. Li, Y. Cai, and W. Sheng, "Converting AC distribution lines to DC to increase transfer capacities and DG penetration," *IEEE Trans. Smart Grid*, vol. 10, no. 2, pp. 1477–1487, Mar. 2019.

[14] "Electricity NIC Submission: SP Energy Networks—ANGLE-DC." 2015. [Online]. Available: https://www.ofgem.gov.uk/publications-and-updates/electricity-nic-submission-sp-energy-networks-angle-dc

[15] J. Yu, K. Smith, M. Urizarbarrena, N. MacLeod, R. Bryans, and A. Moon, "Initial designs for the ANGLE DC project; converting existing AC cable and overhead line into DC operation," in *Proc. 13th IET Int. Conf. AC DC Power Transm. (ACDC)*, Manchester, U.K., 2017, pp. 1–6.

[16] J. Yu, A. T. Moon K. Smith, and N. M. MacLeod, "Developments in the angle-DC project; conversion of a medium voltage AC cable and overhead line circuit to DC," *Water Energy Int.*, vol. 62, no. 1, p. 77, 2019.

[17] "Year One Project Summary." SP Energy Networks. [Online]. Available: https://www.spenergynetworks.co.uk/pages/angle_dc.aspx

[18] G. Abeynayake, G. Li, T. Joseph, J. Liang, and W. Ming, "Reliability and cost-oriented analysis, comparison and selection of multi-level MVDC converters," *IEEE Trans. Power Del.*, early access, Oct. 7, 2021.

[19] J. Yang, J. Zheng, G. Tang, and Z. He, "Internal AC bus fault characteristics of VSC-HVDC system and protection coordination," *Proc. CSEE*, vol. 30, no. 16, pp. 6–11, Jun. 2010.

[20] N. Mei, Y. Li, D. Liu, X. Duan, C. Fu, and H. Rao, "Study on the operational equation for valve short circuit protections in HVDC projects," *Proc. CSEE*, vol. 29, pp. 40–47, Jan. 2009.

[21] J. Cheng and Z. Xu, "Analysis of AC faults in converter station and characteristics of its relay protection," *Proc. CSEE*, vol. 31, no. 22, pp. 88–95, Aug. 2011.

[22] W. Yang, Q. Song, H. Rao, S. Xu, and Z. Zhu, "Converter side phase-to ground fault protection of full-bridge modular multilevel converter-based bipolar HVDC," in *Proc. IEEE Ind. Electron. Soc.*, Beijing, China, 2017, pp. 185–189.

[23] G. Li, J. Liang, F. Ma, C. E. Ugalde-Loo, and H. Liang, "Analysis of single-phase-to-ground faults at the valve-side of HB-MMCs in HVDC systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2444–2453, Mar. 2019.

[24] S. Xue, C. Gu, B. Liu, and B. Fan, "Analysis and protection scheme of station internal AC grounding faults in a bipolar MMC-HVDC system," *IEEE Access*, vol. 8, pp. 26536–26548, 2020.

[25] G. Li, W. Liu, T. Joseph, J. Liang, and Z. Song, "Double-thyristor-based protection for valve-side single-phase-to-ground faults in HB-MMC-based bipolar HVDC systems," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5810–5815, Jul. 2020.

[26] "Datasheet: Phase control thyristor," Data Sheet 5STP 42U6500, ABB, Zurich, Switzerland, 2018.

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