A Single-Input Extended Multilevel Inverter Based on Switched-Capacitor with Reduced Number of Devices

Yaoqiang Wang, *Senior Member*, *IEEE*, Changlong Wang, Yi Wang, Kewen Wang, *Member*, *IEEE*, Jun Liang, *Senior Member*, *IEEE*

***Abstract*—The existing multilevel inverter (MLI) has problems such as a large number of devices, a complex structure, and a large voltage stress of the semiconductor. These shortcomings are not conducive to the modularization, high efficiency and miniaturization of the inverter. Therefore, a topology of extended switched capacitor multilevel inverter utilizing single power supply is proposed. In which, the capacitor is used as a virtual power supply, through the switching control strategy, capacitors and the power supply are reasonably combined, then a multilevel output voltage can be acquired. The proposed topology mainly has the following advantages. Firstly, it can be expanded to further increase the number of output levels. Secondly, the structure of the basic switched capacitor circuit used in the topology is simple, which can reduce the number of devices when the output is the same. Thirdly, the terminal H-bridge for output voltage polarity conversion can be eliminated in the proposed topology, which is beneficial to reduce the total standing voltage and peak inverse voltage. Therefore, an opportunity for the application of the inverter in medium and high voltage is provided. Additionally, the inherent capacitor voltage self-balancing capability of the proposed topology can eliminate the additional balancing control algorithms, therefore, the modulation strategy is simplified. Finally, the correctness and effectiveness of the topology are verified by the extensive simulation and experimental results carried out on the 13-level inverter.**

***Index Terms*—Multilevel, single-input, bipolar inverter, switched-capacitor, self-balancing.**

I. Introduction

In recent years, with the large-scale deployment of distributed generation, as an energy conversion interface between distributed energy and power grid or AC load, the DC-AC link of distributed generation has attracted extensive attention [1]-[2]. Due to the low total standing voltage (TSV), low total harmonic [1] distortion (THD) and effective reduction of electromagnetic interference, multilevel inverters have become one of the preferred circuit configurations for high efficiency in the DC-AC link [3]. There are many traditional multilevel inverters such as neutral point clamped (NPC) multilevel inverter [4], flying capacitor (FC) multilevel inverter [5], and cascaded H-bridge (CHB) multilevel inverter [6]. However, with the number of output voltage levels increasing, the number of power devices they required soars, which will inevitably complicate the structure of the inverter and increase manufacturing costs. The NPC multilevel inverter can reduce the voltage stress of capacitor, but the diode clamped by the topology is subjected to different reverse voltage stress, and the inner switches are turned on for longer than the outer switches. Therefore, the capacitor has the problem of voltage imbalance [7]-[8]. FC multilevel inverter uses capacitors instead of clamped diodes, which solves the problem of slow recovery of diode reverse voltage. However, a large number of capacitors are used. In order to ensure the stable operation of the inverter, the balance of capacitor voltage is the most important issue for this type of topology [9]-[10]. The cascaded H-bridge multilevel inverter uses isolated power instead of capacitors and reduces the use of diodes and capacitors. However, the number of output levels is directly related to the number of isolated power supplies. The extensive use of isolated power supplies complicates circuit protection. Therefore, the application in actual engineering has been limited [11]-[12].

In addition, in the grid-connected system of distributed generation or new energy electric vehicles, the above-mentioned multilevel inverters usually need to increase the voltage transformation link when the input voltage does not satisfy the output conditions. The bulky core and multiple coils of the transformer inevitably complicate the system and increase the area occupied [13]. For which, the research on the more efficient topologies has aroused a wide interest of experts and scholars. In the DC-DC conversion link, the switched capacitor (SC) structure has been widely adopted. In SC convertor, the capacitor is charged in parallel with the power supply, and the high voltage gain is obtained by superposing the capacitor and the power supply in series, avoiding the use of bulky inductance components [14]-[15].

Motivated by which, SC structure was introduced into a multilevel inverter system. Several switched capacitor multilevel inverters (SCMLIs) were proposed in [16]-[22]. The 5-level inverter was proposed in [16], but the boost gain of the inverter is 1. Two 9-level inverters were proposed in [17] and [18], the bipolar level of the topology is generated by the H bridge. A 9-level inverter with inductive load ability was proposed in [19]. In [20] and [21], two 13-level inverters with similar structures

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were proposed. The topology does not use the H-bridge circuit to output bipolar levels, which reduces the voltage stress of the semiconductor device. A 13-level inverter was proposed in [22], which uses a small number of components. However, it should be pointed out that these topologies are fixed, which are not only inconvenient for the expansion of inverter bridge, but also the number of output levels is limited seriously.

In general, with the increase of inverter output level, the quality of output voltage waveform can be improved effectively and the rate of voltage harmonic distortion can be decreased obviously. Therefore, the extensible switched capacitor inverter has become a hot topic.

In [23], a high-efficiency multilevel inverter topology was proposed, where the number of output levels is linear with the number of voltage sources. Thus, the scope of its application is limited seriously. In [24], the proposed topology owns a simple structure and low switching frequency. However, its output voltage is a superposition of the isolated power supply used, resulting that the proposed topology without boosting capability. Two operating modes were introduced in the topologies that designed in [25]-[26]. In the asymmetric mode, two power supplies with a specific voltage ratio were used to make the inverter output more levels, which can reduce the use of semiconductor devices. But due to the special requirements of the voltage source, the flexibility of the inverter application scenarios will be reduced seriously. In [27], a single-input multilevel inverter was proposed. However, many power devices being employed. The disadvantage of the topology developed in [28]-[30] is that with the increase of expansion modules, semiconductor devices need to withstand higher peak inverse voltage (PIV), especially in high-voltage applications, which will severely reduce the choice of devices.

The high voltage stress of semiconductor devices is mainly caused by the use of H-bridge circuit to output bipolar level. Therefore, newly developed topologies tend to reduce the use of H-bridge circuits. An extended switched capacitor topology was proposed in [31]. Although the H-bridge circuit has not been adopted, there are still two switches that need to withstand large voltage stress. The topology proposed in [32]-[33] effectively reduces the voltage stress of semiconductor devices. However, the topology in [32] has a small boost gain and uses many components, and the topology in [33] has a large TSV. In [34] and [35], the proposed topology has a constant PIV. However, the small rated charging voltage of the capacitor leads to low capacitance energy efficiency.

To address the aforementioned drawbacks, in this paper, a novel multilevel topology by utilizing the switched capacitor is proposed. It has the following salient features:

- Relying on the ability of the extended module output bipolar levels, the proposed topology can eliminate the terminal H-bridge and make the inverter has a low TSV and PIV.
- The proposed topology can reduce the number of devices effectively. The structure of the proposed topology is simplified, the voltage of the capacitor has the ability of self-balancing.
- The single-input topology can be extended easily, and the capacitor has high energy efficiency. Furthermore, the proposed inverter can achieve better output efficiency.

The remainder of this paper is organized as follows. In Section II, the general structure of the proposed topology is presented, its operating principle and modulation strategy are also introduced in detail. In Section III, the principle to determine the capacitance value and the losses analysis of the 13-level inverter are given. In Section IV, the comparisons between the proposed topology and other topologies are discussed. In Section V, extensive simulation and experimental results are provided to demonstrate the efficacy of the proposed 13-level inverter, and finally the conclusions are drawn in Section VI.

II. Circuit Description

A. Basic Switched Capacitor Circuit

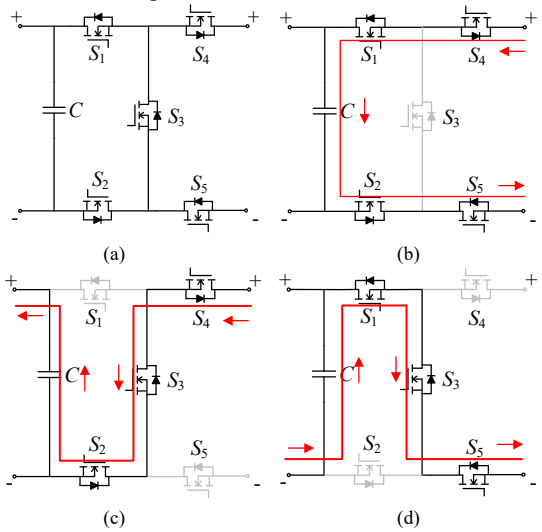

Fig. 1 The structure and operating principle of BSCC. (a) Structure of BSCC, (b) Charging path, (c) Positive discharge path, (d) Negative discharge path.

The structure and operating principle of basic switched capacitor circuit (BSCC) are shown in Fig. 1. In Fig. 1(b), the capacitor is charged to the rated voltage in parallel with the charging path. Fig. 1(c) and Fig.1(d) show the discharge path of the capacitor. Through different switching strategies, the structure achieves the opposite discharge polarity to the outside. Due to the periodicity of the operating principle of the capacitor, the voltage balance of the capacitor does not have to be considered. Therefore, the use of additional voltage balancing circuits and complex modulation strategies can be avoided.

B. Proposed General Switched Capacitor Multilevel Topology

Fig. 2 shows the generalized topology of the proposed switched capacitor inverter, the intermediate switched capacitor circuit (ISCC) consists of a voltage source V_{dc}, a diode D, a capacitor C, and three switches. Unlike other topologies that obtain bipolar levels by using H-bridges, the proposed topology implements bipolar level output by placing equivalent number of BSCC on the both sides of ISCC, respectively. The left half

bridge of the proposed topology is composed of switches S_{01} and S_{02}, and the corresponding right half bridge is composed of switches S_{03} and S_{04}, these two half bridges are placed at the both ends of the topology, respectively. For the proposed topology, if the number of pairs of BSCC placed on both sides of the ISCC is n, the number of required diodes (N_{Diode}), switches (N_{Switch}), capacitors ($N_{Capacitor}$), the number of generated output levels (N_{Level}) and the output gain G can be obtained by

$$N_{Diode} = 1, \tag{1}$$

$$N_{Switch} = 10n + 7, \tag{2}$$

$$N_{Capacitor} = 2n + 1, \tag{3}$$

$$N_{Level} = 2^{n+3} - 3, \tag{4}$$

$$G = 2^{n+2} - 2. \tag{5}$$

In this case, the number of output levels can be increased by adding the same number of BSCCs on the both sides, it is worth noting that the capacitor C in the ISCC is charged to V_{dc} in parallel with the power supply. In the extension step, the capacitors C_{Ln} and C_{Rn} in the extended BSCC are step-charged by the source and the capacitors in the previous extension step. In an ideal situation, the capacitor charging voltage V_{CLn} and V_{CRn} can be computed as

$$V_{CLn} = V_{CRn} = V_{dc} + V_C + V_{CL1} + \quad + V_{CL(n-1)}. \tag{6}$$

Due to the step charging of capacitor, the capacitor in the path of the inverter works can pump more charge, therefore, more voltage levels can be generated by the inverter.

In general, switched capacitor multilevel inverters always face some of the same problems. For instance, the release of charge in the capacitor will reduce its voltage value and cause its voltage ripple loss. Especially, the output voltage of switched capacitor multilevel inverter is superimposed by the power supply and the capacitors participating in the discharge, which will highlight the adverse impact of the capacitor voltage ripple. As a result, the output voltage of inverter may drop greatly and its quality is inevitably reduced. Sometimes, there is no reverse current loop in the topology, this will make it unable to carry inductive load. Next, in order to address these problems, as a typical representative of the proposed generalized topology, the 13-level switched capacitor inverter will be analyzed in detail.

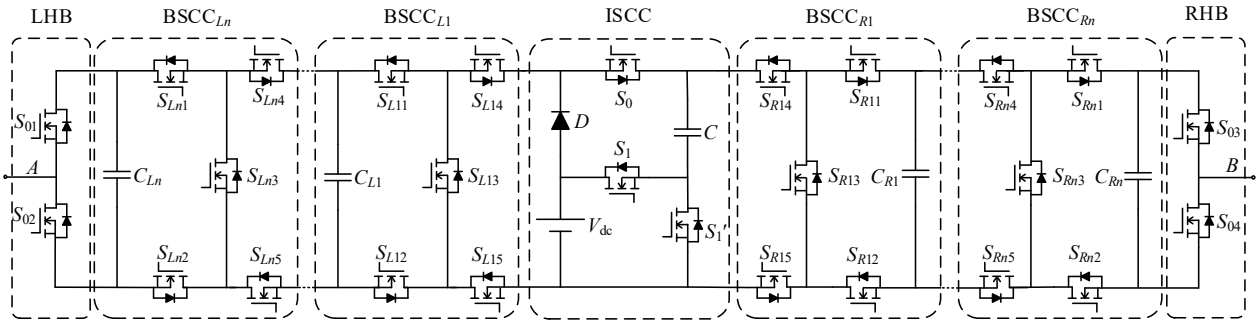

Fig. 2 Generalized topology of the proposed switched capacitor multilevel inverter.

C. Thirteen-Level Inverter

The structure of the proposed 13-level inverter is shown in Fig. 3, which consists of a voltage source V_{dc}, a diode D, three capacitors, and seventeen switches. The state of the switch S_1 and S_1' are complementary and the states of the switch S_{L1n} and the switch S_{R1n} (n = 1, 2, 3, 4, 5) are consistent when the inverter output levels have opposite polarities.

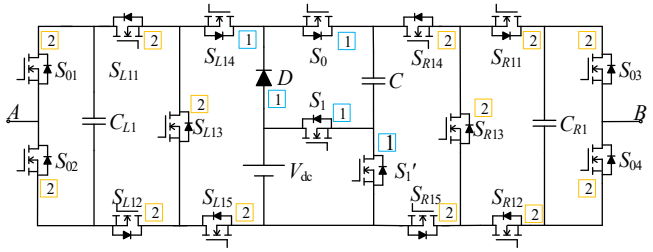

Fig. 3 Topology of the proposed 13-level inverter.

Unlike other topologies that use the H-bridges to acquire bipolar levels, the proposed topology owns inherent level polarity reversal capabilities, which can effectively reduce the PIV of semiconductors. As presented in Fig. 3, the maximum PIV of the semiconductors is $2V_{dc}$, consistent with the maximum charging voltage of the capacitors. The half-bridge of the inverter outputs a peak level of $4V_{dc}$ and a valley level of $-2V_{dc}$, respectively. Therefore, the maximum output level of the inverter is $6V_{dc}$, which obtains a boost gain of 6 times. The output bus voltage V_{bus} of the proposed 13-level inverter can be calculated by

$$V_{bus} = V_A - V_B. \tag{7}$$

D. States of 13-Level Inverter

In general, according to the output level, the 13-level inverter can be divided into 13 operating states. In this part, due to the page limitation, only seven operating states (states A ~ G) of the 13-level inverter during the positive half cycle are shown in Fig. 4. In which, the purple dotted line represents the reverse current circuit of the inverter that ensures its inductive load capacity. Fig. 5 shows the modulation strategy of the 13-level inverter. To make the concept clearly, it is assumed that all the components of the inverter are ideal, and there is no internal resistance and forward voltage drop in the inverter. In addition, the capacitance of the circuit is large enough, and the inverter works in a stable state, voltages of the capacitors are constant at $V_C = V_{dc}$ and $V_{CL1} = V_{CR1} = 2V_{dc}$, respectively.

TABLE I
SWITCHING STATE AND CAPACITANCE STATE OF THE PROPOSED INVERTER

Reference	State	On-State Switches	Output Voltage V_{bus}	Capacitors		
				C	C_{L1}	C_{R1}
$e_s > e_1$	G	S_{L12}, S_{L13}, S_{L14}, S_{R11}, S_{R13}, S_{R15}, S_0, S_1, S_{01}, S_{04}	$6V_{dc}$	▼	▼	▼
$e_1 \geq e_s > e_2$	F	S_{L12}, S_{L13}, S_{L14}, S_{R11}, S_{R13}, S_{R15}, S_1', S_{01}, S_{04}	$5V_{dc}$	▲	▼	▼
$e_2 \geq e_s > e_3$	E	S_{L12}, S_{L14}, S_{L15}, S_{R11}, S_{R13}, S_{R15}, S_0, S_1, S_{01}, S_{04}	$4V_{dc}$	▼	▲	▼
$e_3 \geq e_s > e_4$	D	S_{L12}, S_{L13}, S_{L14}, S_{R12}, S_{R15}, S_1', S_{01}, S_{04}	$3V_{dc}$	▲	▼	–
$e_4 \geq e_s > e_5$	C	S_{L12}, S_{L14}, S_{L15}, S_{R14}, S_{R15}, S_0, S_1, S_{01}, S_{04}	$2V_{dc}$	▼	▲	▲
$e_5 \geq e_s > e_6$	B	S_{L11}, S_{L14}, S_{R12}, S_{R15}, S_1', S_{01}, S_{04}	V_{dc}	▲	–	–
$e_6 \geq e_s > e_7$	A	S_{L12}, S_{L15}, S_{R12}, S_{R15}, S_1', S_{02}, S_{04}	0	▲	–	–
$e_7 \geq e_s > e_8$	-	S_{L12}, S_{L15}, S_{R11}, S_{R14}, S_1', S_{02}, S_{03}	$-1V_{dc}$	▲	–	–
$e_8 \geq e_s > e_9$	-	S_{L14}, S_{L15}, S_{R12}, S_{R14}, S_{R15}, S_0, S_1, S_{02}, S_{03}	$-2V_{dc}$	▼	▲	▲
$e_9 \geq e_s > e_{10}$	-	S_{L12}, S_{L15}, S_{R12}, S_{R13}, S_{R14}, S_1', S_{02}, S_{03}	$-3V_{dc}$	▲	–	▼
$e_{10} \geq e_s > e_{11}$	-	S_{L11}, S_{L13}, S_{L15}, S_{R12}, S_{R14}, S_{R15}, S_1, S_{02}, S_{03}	$-4V_{dc}$	▼	▼	▲
$e_{11} \geq e_s > e_{12}$	-	S_{L11}, S_{L13}, S_{L15}, S_{R12}, S_{R13}, S_{R14}, S_1', S_{02}, S_{03}	$-5V_{dc}$	▲	▼	▼
$e_{12} \geq e_s$	-	S_{L11}, S_{L13}, S_{L15}, S_{R12}, S_{R13}, S_{R14}, S_1, S_{02}, S_{03}	$-6V_{dc}$	▼	▼	▼

As depicted in Fig. 5, during time $0 < t \leq t_1$, the switches S_{L11}, S_{L12}, S_{L15}, S_{01} and S_{02} are respectively driven by the gate-source voltage VGS_{L11}, VGS_{L12}, VGS_{L15}, VGS_{01} and VGS_{02}, the other switches are turned on or off as given in Fig. 5. When the switches S_{L11}, S_{L12}, S_{L15}, S_{01} and S_{02} alternately switch states, the inverter output states shown in Fig. 4(a) and (b) are switched alternately. In the situation of Fig. 4(a), the output bus voltage V_{bus} can be computed as

$$V_{bus} = V_A - V_B = 0. \tag{8}$$

As shown in Fig. 4(b), the capacitor C is charged in parallel with the source V_{dc}. At this time, the output bus voltage is

$$V_{bus} = V_A - V_B = V_{dc}. \tag{9}$$

Therefore, during this time, the inverter outputs a bus voltage of 0 or V_{dc} as shown in Fig. 5.

It can be seen that in Fig. 5, while $t_1 < t \leq t_2$, the switches S_{L11}, S_{L12}, S_{L15}, S_{R12}, S_0, S_1 and S_1' are respectively driven by the gate-source voltage VGS_{L11}, VGS_{L12}, VGS_{L15}, VGS_{R12}, VGS_0, VGS_1 and VGS_1', the other switches are turned on or off. When the switches S_{L11}, S_{L12}, S_{L15}, S_{R12}, S_0, S_1 and S_1' alternately switch states, the inverter output states shown in Fig. 4(b) and (c) are switched alternately. In Fig. 4(c), the capacitors C_{L1} and C_{R1} are charged by a series combination of source V_{dc} and capacitor C, the output bus voltage V_{bus} can be calculated as

$$V_{bus} = V_A - V_B = 2V_{dc}. \tag{10}$$

Therefore, during this time, the inverter outputs a bus voltage of V_{dc} or $2V_{dc}$ as shown in Fig. 5.

In Fig. 5, when $t_2 < t \leq t_3$, the switches S_{L13}, S_{L15}, S_{R12}, S_{R14}, S_0, S_1 and S_1' are respectively driven by the gate-source voltage VGS_{L13}, VGS_{L15}, VGS_{R12}, VGS_{R14}, VGS_0, VGS_1 and VGS_1', the other switches are turned on or off. While the switches S_{L13}, S_{L15}, S_{R12}, S_{R12}, S_0, S_1 and S_1' alternate switch status, the inverter output states in Fig. 4(c) and (d) are switched alternately. As it can be seen in Fig. 4(d), the capacitor C is charged in parallel with the source V_{dc}, the capacitor C_{L1} participates in discharge. the output bus voltage V_{bus} in the state shown in Fig. 4(d) is

$$V_{bus} = V_A - V_B = V_{dc} + V_{CL1}. \tag{11}$$

Therefore, during this time, the inverter outputs a bus voltage of $2V_{dc}$ or $3V_{dc}$ as shown in Fig. 5.

In Fig. 5, while $t_3 < t \leq t_4$, the switches S_{L13}, S_{L15}, S_{R11}, S_{R12} S_{R13}, S_0, S_1 and S_1' are respectively driven by the gate-source voltage VGS_{L13}, VGS_{L15}, VGS_{R11}, VGS_{R12}, VGS_{R13}, VGS_0, $VGS_1$and VGS_1', the other switches are turned on or off. When the switches S_{L13}, S_{L15}, S_{R11}, S_{R12} S_{R13}, S_0, S_1 and S_1' alternately switch states, the inverter output states shown in Fig. 4(d) and (e) are switched alternately. As shown in Fig. 4(e), the capacitors C_{L1} are charged by series combination of source V_{dc} and capacitor C, the capacitor C_{R1} participates in discharge. the output bus voltage V_{bus} in the state shown in Fig.4(e) is

$$V_{bus} = V_A - V_B = V_{dc} + V_C - \left(-V_{CR1}\right). \tag{12}$$

Therefore, during this time, the inverter outputs a bus voltage of $3V_{dc}$ or $4V_{dc}$ as shown in Fig. 5.

In Fig. 5, during the time $t_4 < t \leq t_5$, the switches S_{L13}, S_{L15}, S_0, S_1 and S_1' are driven by the gate-source voltage VGS_{L13}, VGS_{L15}, VGS_0, VGS_1 and VGS_1', the other switches are turned on or off. Fig. 4(e) and (f) present the switched alternately output states, while the states of switches S_{L13}, S_{L15}, S_0, S_1 and S_1' alternated. In Fig. 4(f), the capacitor C is charged in parallel with the source V_{dc}, the capacitor C_{L1} and C_{R1} participate in discharge. the output bus voltage V_{bus} can be derived as

$$V_{bus} = V_A - V_B = V_{dc} + V_{CL1} - \left(-V_{CR1}\right). \tag{13}$$

In this scenario, the output bus voltage of the proposed inverter is $4V_{dc}$ or $5V_{dc}$, which are depicted in Fig. 5.

While $t_5 < t \leq t_6$, the switches S_0, S_1 and S_1' are driven by the gate-source voltage VGS_0, VGS_1 and VGS_1', respectively. The states of other switches are shown in Fig. 5. It can be seen from Fig. 4(f) and (g), while the switches S_0, S_1 and S_1' alternately switch states, the output states of proposed inverter are switched alternately. In addition, in Fig. 4(g), the capacitor C, C_{L1} and C_{R1} in the discharge circuit participates in the output of the inverter and the output bus voltage V_{bus} can be calculated by

$$V_{bus} = V_A - V_B = V_{dc} + V_C + V_{CL1} - \left(-V_{CR1}\right). \quad (14)$$

In this case, $5V_{dc}$ or $6V_{dc}$ output bus voltage can be acquired, which is presented in Fig. 5.

While $t_6 < t \le t_{11}$, the operating state of the inverter is from state F to state A. It can be seen from Table I that the operating state of the capacitor C_{L1} in the positive half cycle is consistent with the operating state of the capacitor C_{R1} in the negative half cycle, the operating state of the capacitor C_{L1} in the negative half cycle is consistent with the operating state of the capacitor C_{R1} in the positive half cycle, and the states of the switches S_{L1n} and the switches S_{R1n} (n = 1, 2, …, 5) are consistent when the inverter output levels have opposite polarities. Therefore, the operating principle of the negative half cycle of the inverter is similar to that of the positive half cycle. The switching state of the inverter in one cycle is summarized in Table I, where the capacitance state is also given.

E. Modulation Strategy

There are many modulation strategies used in multilevel inverters. In this paper, sinusoidal pulse width modulation (SPWM) is used in a 13-level inverter as shown in Fig. 3. For a single-phase z-level inverter ($z \ge 3$, odd number), it is necessary z-1 carrier waves is compared with a sine-modulated wave. As shown in Fig. 5, the proposed 13-level inverter needs 12 carrier waves e_k (k = 1, 2, …, 12) with amplitude A_c and the same frequency and phase, which is required to be compared to sine-modulated wave e_s with amplitude A_{ref}. The modulation index M ($0 < M \le 1$) is defined as

$$M = \frac{A_{ref}}{6A_c}. \quad (15)$$

It can be known from the operating principle of the 13-level inverter that the proposed inverter requires 14 independent driving signals. In addition, the states of the switches S_{L1n} and the switches S_{R1n} (n = 1, 2, …, 5) are consistent when the inverter output levels have opposite polarities. Therefore, the modulation difficulty of the proposed 13-level inverter is reduced.

As shown in Fig. 5, the sine-modulated wave is compared with each carrier wave separately. The high level is output when the sine-modulated wave is larger than the carrier waves, and the low level is output while the sine-modulated wave is smaller than the carrier waves. From this, a set of rectangular pulse signals is obtained. Twelve pulse signals generated by comparing the carrier wave with the sine-modulation wave, after logical combination, the switch driving signals shown in Fig. 5 can be obtained.

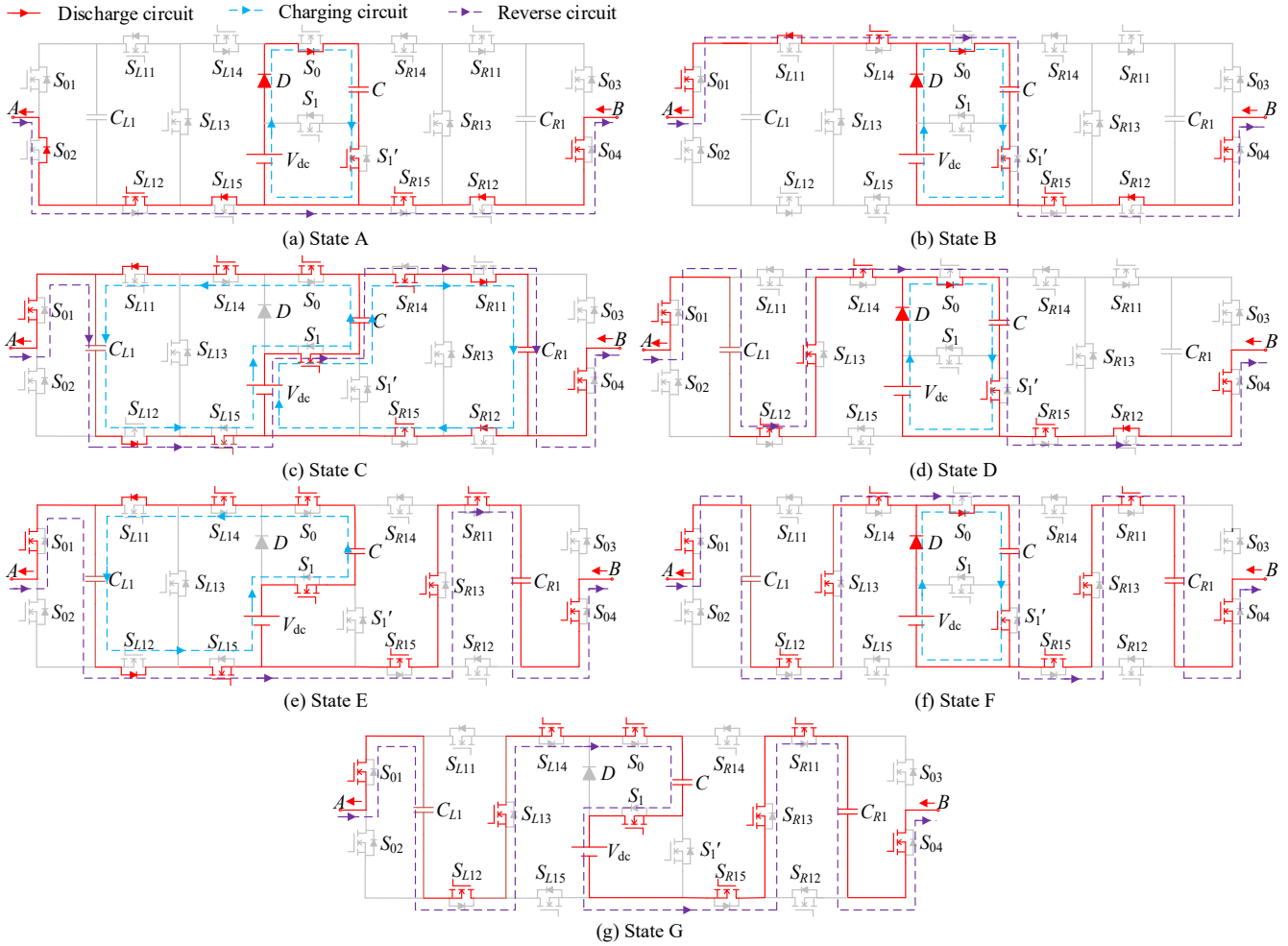

Fig. 4 Current flows in the proposed inverter. (a) V_{bus}= 0, (b) V_{bus}= V_{dc}, (c) V_{bus} = $2V_{dc}$, (d) V_{bus} = $3V_{dc}$, (e) V_{bus} = $4V_{dc}$, (f) V_{bus} = $5V_{dc}$, (g) V_{bus} = $6V_{dc}$.

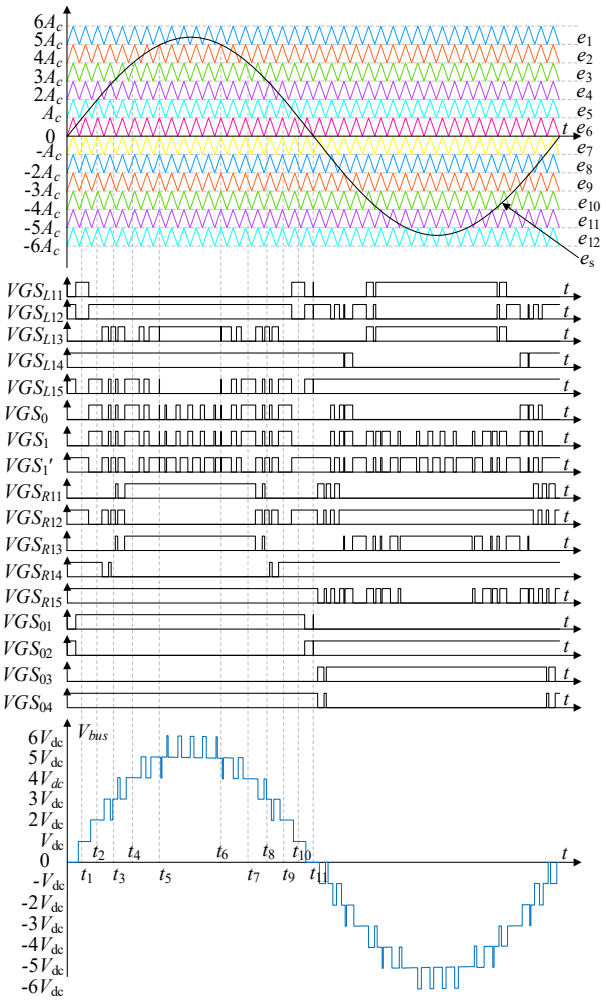

Fig. 5 SPWM modulation and corresponding gate pulses for 13-level inverter.

III. Capacitance Determination and Losses Calculation

A. Determination of Capacitance

The output voltage of the switched capacitor multilevel inverter is a combination of the power supply voltage and the capacitor voltage, and each capacitor has a voltage ripple during the discharge process. A larger voltage ripple will cause deterioration of the inverter efficiency and THD, so that the quality of the output voltage waveform is affected heavily.

In addition, the large voltage ripple caused by the continuous discharge of the capacitor will also damage the stability of the system. When the capacitor is charged in parallel with the charging circuit, an inrush current will be generated. A large inrush current will cause electromagnetic interference, and in severe cases, it will damage the switch. It can be seen from the charging operation of the capacitor that the inrush current is determined by the voltage difference (the difference between the rated charging voltage and the minimum voltage of the capacitor) and the internal resistance of the semiconductor device. Smaller voltage ripple helps to reduce the voltage difference, thereby suppressing the inrush current.

Therefore, it is necessary to choose a suitable capacitor. As expressed in Fig. 5, in the 13-level inverter, t_1, ..., t_5, t_6, ..., t_{10} can be calculated by Eqs. (16) and (17), respectively

$$t_n = \frac{\sin^{-1}\left(\frac{n}{6}\right)}{2\pi f_{ref}}, \tag{16}$$

$$t_{11-n} = \frac{\pi - \sin^{-1}\left(\frac{n}{6}\right)}{2\pi f_{ref}}, \tag{17}$$

where f_{ref} is the output frequency of inverter, n = 1, 2, ..., 5.

It is known that the maximum time period for capacitor C to participate in discharge is (t_5, t_6), during this time, the capacitor C is charged and discharged repeatedly. In the worst case, no charging term is given. Then this discharge period can be used to determine the optimal value of the capacitor under a given voltage ripple limit. the amount of charge Q_C discharged by the capacitor C can be computed as

$$Q_C = \int_{t_5}^{t_6} I_{bus} \sin\left(2\pi f_{ref} - \varphi\right) dt, \tag{18}$$

where I_{bus} indicates the amplitude of the load current, and φ denotes the phase difference between the output voltage V_{bus} and the load current I_{bus}.

When the voltage ripple ΔV_C ($\Delta V_C \le 0.1 V_C$) of the capacitor C is given, the optimal value of the capacitor C can be acquired by

$$C \ge \frac{Q_C}{\Delta V_C}. \tag{19}$$

The maximum time period for the capacitor C_{R1} to participate in the discharge is (t_3, t_8). During this period, the capacitor C_{R1} is not charged, then the amount of charge Q_{CR1} released by the capacitor C_{R1} can be acquired by

$$Q_{CR1} = \int_{t_3}^{t_8} I_{bus} \sin\left(2\pi f_{ref} - \varphi\right) dt. \tag{20}$$

When the voltage ripple ΔV_{CR1} ($\Delta V_{CR1} \le 0.1 V_{CR1}$) of the capacitor C_{R1} is given, the optimal value of the capacitor C_{R1} can be computed as

$$C_{R1} \ge \frac{Q_{CR1}}{\Delta V_{CR1}}. \tag{21}$$

Due to the symmetrical operation of the capacitors C_{L1} and C_{R1}, therefore, the values of capacitor C_{L1} can be calculated by utilizing the similar calculation formulas.

B. Calculation of Losses

In this section, the energy loss of the proposed inverter in the working state is calculated, including ripple losses, switching losses and conduction losses.

1) ***Ripple Losses***: When the capacitor is running in parallel charging state, the voltage ΔV_{Ci} difference between capacitor charging voltage and the capacitor terminal voltage will produce ripple losses P_{rip}, the ripple voltage of the capacitor can be derived as

$$\Delta V_{Ci} = \frac{1}{C_i}\int_{t_{n,i}}^{t_{m,i}} i_{Ci}dt\ , \tag{22}$$

where i_{ci} denotes the current flowing through the ith capacitor in the discharge state, ($t_{m,i}$, $t_{n,i}$) indicates the discharge time of the capacitor in the entire cycle. Therefore, the ripple losses of the entire period can be obtained by

$$P_{rip} = \frac{f_{ref}}{2}\sum_{i=1}^{3} C_i \Delta V_{Ci}^2\ . \tag{23}$$

2) ***Switching Losses***: The switching losses can be estimated from the charging and discharging process of the parasitic capacitor in the switch. It is assumed that the parasitic capacitor is linear. When the switch S_i is in the off state, the voltage of the parasitic capacitor C_S is gradually charged from 0 to $V_{CS,i}$, and $V_{CS,i}$ is approximately equal to the peak invert voltage $V_{S,i}$ of the switch S_i. The PIV of each switch in the proposed 13-level inverter is given in Fig.3. When the switch is turned on, the stored charge of the parasitic capacitor is consumed in the form of heat by the internal resistance. In a switching cycle, the loss is calculated as

$$E_{S,i} = C_S V_{CS,i}^2\ . \tag{24}$$

The loss of the switch during one cycle of inverter operation is

$$P_{S,i} = C_S V_{S,i}^2 f_{S,i}\ , \tag{25}$$

where $f_{S,i}$ is the switching frequency.

$$f_{S,i} = N_{S,i} f_{\text{ref}}\ , \tag{26}$$

where $N_{S,i}$ is the number of switching times in one work cycle of the inverter. According to Fig. 4 and Fig. 5, the switch is repeatedly turned on and off in its working range. Therefore, $N_{S,i}$ can be obtained by the following equation

$$N_{S,i} = \frac{t_{S,i} f_c}{T_S f_{\text{ref}}}\ , \tag{27}$$

where f_c is the carrier frequency, $t_{S,i}$ is the operating time of the switch S_i, which can be obtained in Fig. 5. T_S is one cycle of the inverter. Therefore, the switching losses of the proposed 13-level inverter in one cycle can be estimated as

$$P_S = 50\sum_{i=1}^{17} C_S V_{S,i}^2 t_{S,i} f_c\ , \tag{28}$$

3) ***Conduction Losses***: During the conduction of the semiconductor device, energy losses occur due to the presence of parasitic impedance. The total parasitic impedance r_{eq} of the proposed inverter at various output voltages is presented in Table II, including the internal resistance r_S of the switch's conduction state, the internal resistance r_D of the diode con duction state, and the equivalent series resistance r_{ESR} of the capacitor.

As shown in Fig. 5, when $0 < |e_s| \le A_c$, the inverter alternately outputs 0 level and $+V_{dc}$ level. While the inverter outputs 0 level, the capacitor C is charged in parallel with the source, and the current flows through the anti-parallel diode of the switch S_0, the diode D the switch S_1'. While the inverter outputs $+V_{dc}$ level, current flows through 5 switches and 4 diodes. Therefore, the conduction losses P_{con1} in time $0 < t \le t_1$ can be calculated by

TABLE II
EQUIVALENT PARASITIC IMPEDANCE OF EACH LEVEL

Output Voltage Level (V_{bus})	Total Parasitic Impedance (r_{eq})
0	r_S+2r_D+r_{ESR}
$\pm V_{dc}$	5r_S+4r_D+r_{ESR}
$\pm 2V_{dc}$	8r_S+4r_D+3r_{ESR}
$\pm 3V_{dc}$	7r_S+3r_D+2r_{ESR}
$\pm 4V_{dc}$	9r_S+2r_D+3r_{ESR}
$\pm 5V_{dc}$	9r_S+2r_D+3r_{ESR}
$\pm 6V_{dc}$	*10*r_S+3r_{ESR}

$$P_{con1} = \int_0^{t_1}\left[I_{bus}\sin\left(2\pi f_{ref}t\right)\right]^2 \times\left[\begin{array}{l}\left(5r_S+4r_D+r_{ESR}\right)\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)}{A_c}\\ +\left(r_S+2r_D+r_{ESR}\right)\left(1-\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)}{A_c}\right)\end{array}\right]dt\ . \tag{29}$$

During the period $t_{10} < t \le t_{11}$, the energy losses are the same as interval $0 < t \le t_1$. When $A_c < |e_s| \le 2A_c$, the inverter alternately outputs $+V_{dc}$ level and $+2V_{dc}$ level, and the equivalent impedance in the output path is given in Table II. The conduction losses P_{con2} during time $t_1 < t \le t_2$ can be calculated by

$$P_{con2} = \int_{t_1}^{t_2}\left[I_{bus}\sin\left(2\pi f_{ref}t\right)\right]^2 \times\left[\begin{array}{l}\left(8r_S+4r_D+3r_{ESR}\right)\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)-A_c}{A_c}\\ +\left(5r_S+4r_D+r_{ESR}\right)\left(1-\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)-A_c}{A_c}\right)\end{array}\right]dt\ . \tag{30}$$

In the period $t_9 < t \le t_{10}$, the energy losses are the same as interval $t_1 < t \le t_2$. By utilizing the same analysis method, the conduction losses during the time periods $t_2 < t \le t_3$ ($t_8 < t \le t_9$), $t_3 < t \le t_4$ ($t_7 < t \le t_8$), $t_4 < t \le t_5$ ($t_6 < t \le t_7$) and $t_5 < t \le t_6$ can be obtained by

$$P_{con3} = \int_{t_2}^{t_3}\left[I_{bus}\sin\left(2\pi f_{ref}t\right)\right]^2 \times\left[\begin{array}{l}\left(7r_S+3r_D+2r_{ESR}\right)\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)-2A_c}{A_c}\\ +\left(8r_S+4r_D+3r_{ESR}\right)\left(1-\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)-2A_c}{A_c}\right)\end{array}\right]dt\ , \tag{31}$$

TABLE III
COMPARISON OF THE PROPOSED TOPOLOGY WITH A 13-LEVEL INVERTER AND A 9-LEVEL INVERTER

Items	N_L	N_S	N_D	N_C	PIV (V_{dc})	TSV (V_{dc})	*CF**		*G**	H-bridge	Extended ability
							0.5	1.5			
[18]	9	10	3	3	4	26	3.44	6.78	1.33	Yes	No
[19]	9	8	3	3	4	23	3.06	6.06	1.33	No	No
[20]	13	13	2	3	3	32	2.73	5.42	2	No	No
[21]	13	10	4	4	6	33	2.88	5.88	1.5	No	No
[22]	13	14	1	3	3	33	2.77	5.54	2	No	Not given
[29]	13	10	10	5	6	60	4.46	9.54	1.2	Yes	Yes
[32]	13	34	0	12	3.5	25	4.63	6.83	0.25	No	Yes
[35]	13	23	0	6	4	40	3.92	7.31	1	No	Yes
Proposed	13	17	1	3	2	31	2.88	5.42	2	No	Yes

TABLE IV
COMPARISON OF PARAMETERS BETWEEN THE PROPOSED TOPOLOGY AND TOPOLOGIES IN [30]-[35] WHEN OUTPUT LEVEL $2N$+1

Items	[30]	[31]	[32]	[33]	[34]	[35]	Proposed
N_{Switch}	$2N$+2	$3N$+2	$6N$-2	$4+8\log_2^{(N+2)/3}$	$5N$-1	$3N$+5	$10\log_2^{N+2}-13$
$N_{Capacitor}$	N	N-1	$2N$	$4\log_2^{(N+2)/3}$	N-1	N	$2\log_2^{N+2}-3$
N_{Diode}	N	0	0	$4\log_2^{(N+2)/3}$	0	0	1
*G**	1	$N/(N\text{-}1)$	0.25	$N/\left(4\log_2^{(N+2)/3}\right)$	N/(N-1)	1	$N/(2\log_2^{N+2}-3)$
TSV(V_{dc})	(N^2+11N-4)/2	11N-14	(N^2+3N-4)/2	(16N-4)/3	5N-1	7N-2	5N
PIV(V_{dc})	N	N	(N+1)/2	(N+2)/3	1	4	(N+2)/4
H-bridge	YES	NO	NO	NO	NO	NO	NO

$$P_{con4}=\int_{t_3}^{t_4}\left[I_{bus}\sin\left(2\pi f_{ref}t\right)\right]^2 \times\left[\begin{array}{l}\left(9r_S+2r_D+3r_{ESR}\right)\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)-3A_c}{A_c}\\ +\left(7r_S+3r_D+2r_{ESR}\right)\left(1-\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)-3A_c}{A_c}\right)\end{array}\right]dt, \quad (32)$$

$$P_{con5}=\int_{t_4}^{t_5}\left[I_{bus}\sin\left(2\pi f_{ref}t\right)\right]^2 \times\left[\begin{array}{l}\left(9r_S+2r_D+3r_{ESR}\right)\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)-4A_c}{A_c}\\ +\left(9r_S+2r_D+3r_{ESR}\right)\left(1-\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)-4A_c}{A_c}\right)\end{array}\right]dt, \quad (33)$$

$$P_{con6}=\int_{t_5}^{t_6}\left[I_{bus}\sin\left(2\pi f_{ref}t\right)\right]^2 \times\left[\begin{array}{l}\left(10r_S+3r_{ESR}\right)\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)-5A_c}{A_c}\\ +\left(9r_S+2r_D+3r_{ESR}\right)\left(1-\dfrac{A_{ref}\sin\left(2\pi f_{ref}t\right)-5A_c}{A_c}\right)\end{array}\right]dt. \quad (34)$$

It can be seen from Table I that the operation of the inverter in positive and negative half period is symmetrical. Thus, the conduction losses of the inverter in the two half periods are equal. Therefore, the conduction losses P_{total} of the inverter can be obtained by

$$P_{total}=2f_{ref}\left(2P_{con1}+2P_{con2}+2P_{con3}+2P_{con4}+P_{con5}\right). \quad (35)$$

In summary, the power loss P_{Loos} of the proposed inverter can be calculated by

$$P_{Loos}=P_{rip}+P_{sw}+P_{total}. \quad (36)$$

Under different parameters, 13-level inverters have different losses. When the input voltage of the inverter is 25V and the load is 100 Ω, the ripple losses, switching losses and conduction losses loss can be estimated at 2.14 W, 0.49 W and 1.67 W. Under the current conditions, the output efficiency is 96.32%, and the actual measured efficiency is 95.4%. The measured efficiency is slightly lower than the estimated efficiency due to the existence of error, which is superior to the existing inverters [36-39].

IV. Comparison Between the Proposed Topology and Other SCMLI Topologies

In this section, in order to effectively assess the advantages of the proposed topology in terms of reducing the number of components and reducing voltage stress, it is necessary to make a detailed comparison with the recently proposed similar topology from different perspectives. Here, two different schemes are designed to compare the topology at the output 13 levels and the output level $2N$+1.

A Comparison of 13-Level Inverters and 9-Level Inverters

In order to evaluate the performance of the proposed inverter, a comparative study is conducted between the proposed 13-level inverter and the existing solution, the comparative results are given in Table III. As shown in Table III, the main comparison parameters are the number of switches (N_S), the number of diodes (N_D), the number of capacitors (N_C), the maximum PIV of switches and diodes, the TSV of switches and diodes, the use of H-bridge and extension capacity.

In order to achieve a fair comparison results at different output levels of the inverter, the capacitance energy efficiency G* and the cost function CF* are introduced. G* is defined as the ratio of the output gain G to the number of capacitors (N_C). The cost function CF* represents the total cost of the inverter, as defined below

$$CF^* = \frac{\left(N_S + N_D + N_C + \alpha \times \frac{\mathrm{TSV}}{V_{\mathrm{dc}}} + \beta \times \frac{\mathrm{PIV}}{V_{\mathrm{dc}}} \right)}{N_L}, \qquad (37)$$

where α and β are the specific gravity coefficients, which indicate the significance of PIV and TSV. If the significance of PIV and TSV are greater than the number of switches, then both α and β should be greater than 1. If the significance of PIV and TSV are less than the number of components, then α and β should be less than 1. In Table III, the total cost of each inverter is given when $\alpha = \beta = 0.5$ and $\alpha = \beta = 1.5$.

The topologies in [18] and [19] are 9-level inverters, which use 16 and 14 components respectively. As can be seen from the Table III, the maximum PIV of the 9-level inverter is $4V_{\mathrm{dc}}$, which is higher than the proposed 13-level inverter. Although the proposed inverter uses more components, it has lower cost and higher capacitance energy efficiency. The 13-level inverter in [29] adopts H-bridge output bipolar level, and the inverter has a large PIV. The proposed topologies in [20] and [21] employ fewer components, but the topologies have a large PIV, which is not conducive to the application of inverters in medium-high voltage scenarios. In addition, the topologies proposed in [20]-[21] are fixed and without extensibility.

Compared with the topologies in [32] and [35], the proposed topology uses fewer components, and has a low cost and high capacitance energy efficiency. The topology in [22] uses 18 components, and needs less components than the proposed topology. But the maximum PIV of the components is $3V_{\mathrm{dc}}$, while the proposed topology is only $2V_{\mathrm{dc}}$. In addition, the proposed topology has lower TSV and extensibility.

In summary, the proposed 13-level inverter has higher capacitance energy efficiency and lower PIV. It can be seen from the comparison result of cost that when the significance of the number of components is greater than the voltage stress, the cost of the proposed topology is higher than the topologies in [20] and [22], and lower than the other topologies. When the significance of the number of components is less than the voltage stress, the proposed topology has the lowest cost. Therefore, the proposed topology has a good balance between the number of components and the voltage stress. In addition, the proposed topology has the ability to extend. Through the module extension, the proposed topology can output more levels and further reduce the cost of the inverter.

B Topology Comparison with Outputting 2N+1 Level

In this section, the proposed topology is compared with the topologies in [30]-[35]. When the inverter output level is $2N$+1, the parameter calculation equations of the proposed topology and the topologies in [30]-[35] are summarized in Table IV. For the convenience of analysis, the topologies in the comparison are all based on the switched capacitor principle and can be extended. It can be seen from Table IV that the H-bridge is not needed when the proposed topology outputs bipolar levels. Therefore, the PIV of the semiconductors keep at a reasonable value when the proposed inverter outputs more levels.

Fig. 6 depicts the comparison of the proposed topology with other single-input switched capacitor multilevel topologies. Fig. 6(a) shows that the proposed topology uses the least number of components (including the number of switches, diodes, and capacitors) at the output level of $2N$+1. The comparison results of capacitance energy efficiency are given in Fig. 6(b). It can be seen that the proposed topology has the maximum capacitance energy efficiency, and with the extension of the topology, the capacitance energy efficiency also increases. The larger capacitance efficiency indicates that the topology needs fewer capacitors to achieve higher boost gains and more levels, and further reducing the number of components used.

Fig. 6(c) and Fig. 6(d) are the comparison results of PIV and TSV for semiconductors, respectively. Although the PIV of the proposed topology is larger than the PIV of the topologies in [34] and [35], compared with the topologies in [35], the proposed topology has lower TSV. Furthermore, the TSV of the proposed topology is only one V_{dc} larger than the topology in [34].

In order to make the comparison of the topology fairer, the cost function CF is introduced to analyze the cost of the topology. The comparative analysis of the topology is carried out on

the basis of the same output level, therefore, the cost function *CF* is defined as

$$CF = \left(N_S + N_D + N_C + \alpha \times \frac{\text{TSV}}{V_{\text{dc}}} + \beta \times \frac{\text{PIV}}{V_{\text{dc}}} \right). \qquad (38)$$

Fig. 6(e) and Fig.6(f) are the comparison results with specific gravity coefficients of 1.5 and 0.5, respectively. It can be seen that the proposed topology has the lowest cost in both cases, and the relationship between the voltage stress and the number of components is well balanced. Based on the above discussion, it can be concluded that the proposed topology has high capacitance energy efficiency and can output more levels using fewer components. Moreover, the strategy of H-bridge to realize the output voltage polarity conversion is not used, so that the PIV of the semiconductor can operate at a reasonable level and the topology has a low TSV. In terms of cost comparison, it proves that the proposed topology has better economic efficiency.

V Simulation and Experimental Results

A Simulation Results

In order to validate the effectiveness of the proposed topology, extensive simulations are carried out on the 13-level inverter model. In the simulation, the input voltage is V_{dc}=25V, the output load is R_{L}=100Ω+60mH, the modulation wave frequency is f_{o}=50Hz, the carrier frequency is f_{a}=2000Hz, and the modulation ratio *M* is 0.9. The simulation waveforms of the output voltage and load current are shown in Fig. 7 (a). It can be seen that the inverter outputs a 13-level voltage with the peak voltage is 150V. The output boost gain is 6, the load current is sinusoidal and lags the output voltage. Fig. 7 (b) shows the output voltage waveform of the inverter half-bridge. The peak voltage of the both half-bridges of the inverter is 100V, and the valley voltage is -50V, which is consistent with the theoretical analysis of the inverter output voltage.

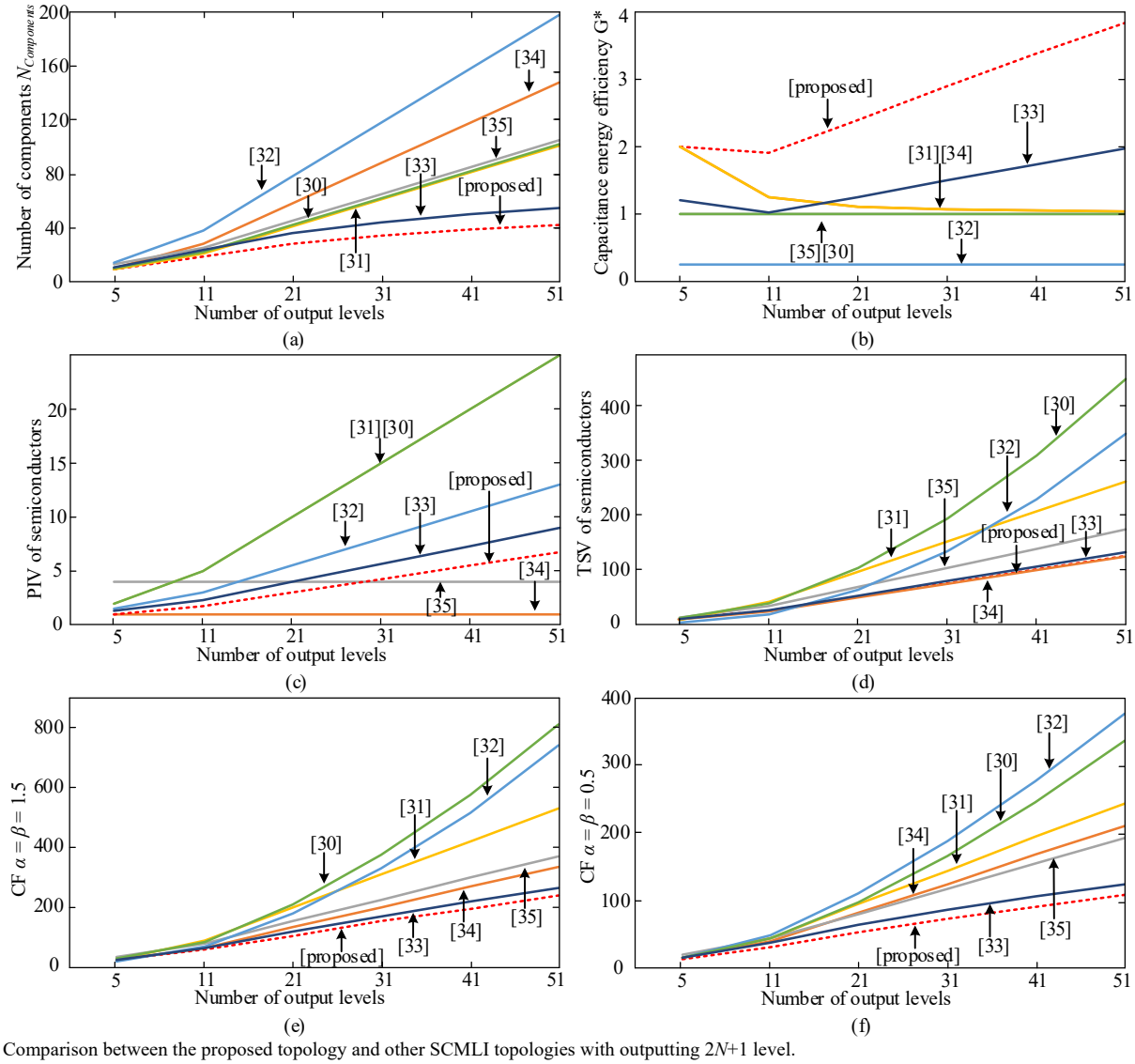

Fig. 6 Comparison between the proposed topology and other SCMLI topologies with outputting 2*N*+1 level.

Fig. 7(c) shows the simulation waveforms of the voltage and current of the inverter under different loads. The resistive inductive load is set to 100Ω and 60mH, and the resistive load is set to 100Ω. It can be seen that the inverter switches from no-load to resistive inductive load, and then switches to resistive load after three cycles. During this period, the inverter output voltage waveform is stable, and the current response is fast. Fig. 7(d) shows the current and voltage simulation waveforms when the inverter input voltage changes. The inverter input voltage is switched from zero to 15V, and then the input voltage rises to 25V. The load current presents a sinusoidal waveform and the angle lags behind the voltage.

B Experimental Results

In order to further demonstrate the performance of the inverter, a small 13-level inverter experimental platform is built. The experimental parameters are given in Table V and the experimental prototype is shown in Fig. 8. According to equations (16)-(21), in the case of meeting the voltage ripple and experimental requirements, the minimum capacitance of capacitor C is estimated to be 2111μF, and the minimum capacitance of capacitors C_{L1} and C_{R1} are 1654μF. Considering the limitations of the experimental equipment and a certain margin, in this experiment, the capacitor selects the design value of 2200 μF.

TABLE V
EXPERIMENTAL PARAMETERS

Items	Specifications
Input voltage V_{dc}	15 V or 25 V
Capacitor C, C_{L1}, C_{R1}	2200 μF
Load resistor	100 Ω or 200 Ω
Load inductor	15 mH
Out frequency	50 Hz or 100 Hz
Carry frequency	2000 Hz
Power switches	SPP20N60C3
Power diodes	TLP250

In this part, the steady-state performance of the 13-level inverter is tested, and the output voltage, load current, and capacitor voltage waveform of the inverter are investigated. In order to check the load-bearing capacity of the inverter under complex operating conditions, several different experiments are designed. For instance, input voltage changes, output frequency changes, load changes, and modulation ratio changes.

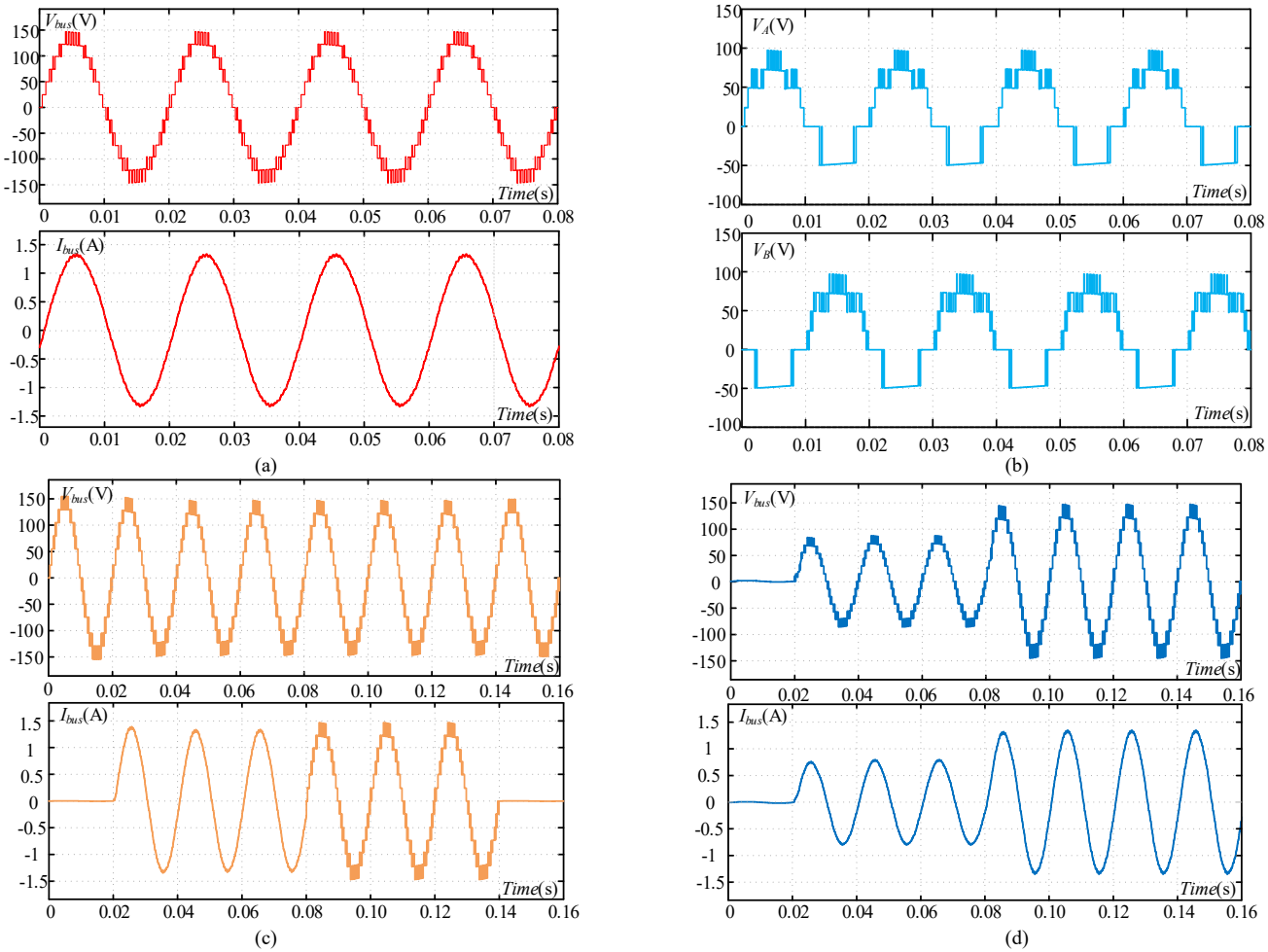

Fig. 7 Simulation waveforms. (a) Simulation waveforms of voltage and current, (b) Simulation waveforms of the voltage output from the inverter half-bridge, (c) Simulation waveforms under different loads, (d) Simulation waveform under input voltage variation.

When the input voltage value of the inverter is 25V, the load resistance is 100Ω, the load inductance is 15mH, and the modulation ratio M is 0.9, the inverter output voltage and load current waveforms are shown in Fig. 9 (a). It can be obtained that the inverter outputs a 13-level step voltage, the peak value of the output voltage is close to 150V, and a boost gain of 6 times is obtained. The experimental results are consistent with the simulation results, verifying the feasibility of the inverter. In addition, the load current is sinusoidal, and the ability of inverter to carry inductive loads is verified. Fig. 9 (b) presents the experimental waveform of the capacitor voltage, where the voltages of the capacitors C, C_{L1} and C_{R1} fluctuate within the allowable range of ripple, and the capacitor voltage achieves self-balancing.

Fig. 10 depicts the waveforms of voltage and current when the input voltage of the inverter changing. In this scenario, the value of the total load is R_L=100Ω+15mH, the modulation ratio is 0.9 and the output frequency is set as 50Hz. It can be seen that during the process of inverter input voltage change, the number of inverter output levels and boost gain remain unchanged, and the load current varies with the amplitude of the output voltage. The change of input voltage was studied in the dynamic experiment. The corresponding change process is relatively smooth compared with the simulation results, which is caused by the large time constant of the capacitor charging circuit.

Fig. 11 presents the waveforms of voltage and current as the output frequency changes. In this case, the input voltage of the inverter is 25V, the value of the total load is R_L=100Ω+15mH, the modulation ratio is set as 0.9. It can be seen that the amplitude of the output voltage and load current of the inverter remains unchanged when the output frequency changes, and the frequency change responds quickly. Therefore, it can be utilized in the complex conditions with frequency fluctuation.

The waveforms of voltage and current under different loads are shown in Fig. 12. In this experiment, the input voltage is 25V, the modulation ratio is set to 0.9 and the frequency is set to 50Hz. In Fig. 12(a), the inverter is switched from no-load to load R_{L1}=100Ω+15mH. It can be seen that the output voltage of the inverter remains unchanged and the load current quickly enters a stable state from 0. In Fig. 12 (b), the inverter load R_{L1}=100Ω+15mH is switched to the load R_2=200Ω. At this time, the load current decreases with the increase of impedance, and the stability of the inverter is excellent.

The waveforms of voltage and current under different modulation ratios are shown in Fig. 13. In this situation, the input voltage of the inverter is 25V, the value of the load is R_L=100Ω+15mH, and the output frequency is set to 50Hz. As shown in Fig. 13(a)~(c), the output level and output voltage amplitude change with the modulation ratio. In Fig. 13(a), when the modulation ratio M=0.7, the inverter outputs 11 levels; in Fig. 13(b), when the modulation ratio M=0.4, the inverter outputs 7 levels; in Fig. 13(c), when the medium modulation ratio M=0.1, the inverter outputs 3 levels. Based on the above discussions, it can be concluded that the inverter can work at different modulation ratios, different boost requirements can be met, and the inverter load current follows better.

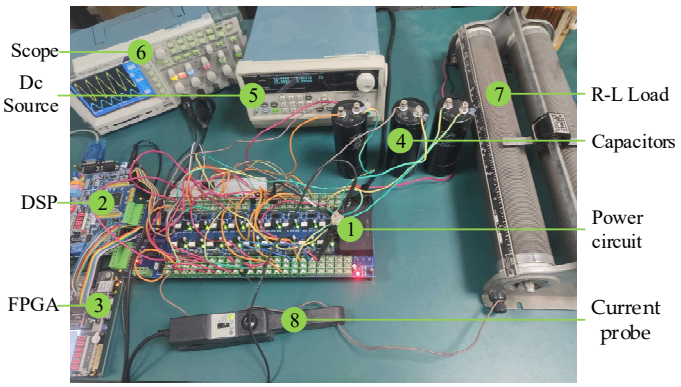

Fig. 8 Experimental prototype.

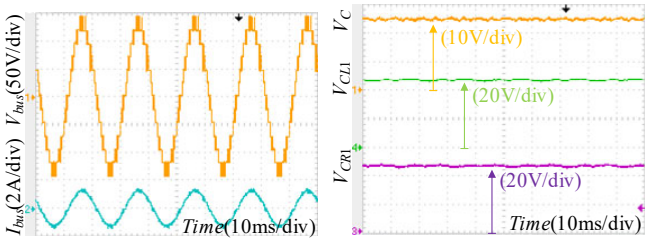

Fig. 9 Experimental waveforms. (a) Experimental waveforms of voltage and current, (b) Experimental waveforms of capacitor voltages.

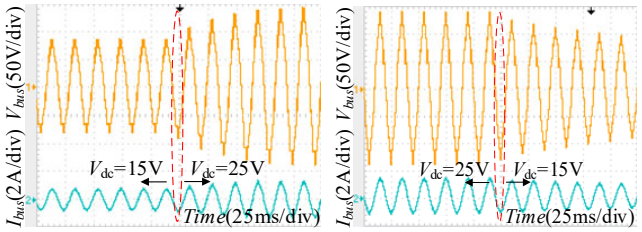

Fig. 10 Experimental waveforms of voltage and current when the change of input voltage.

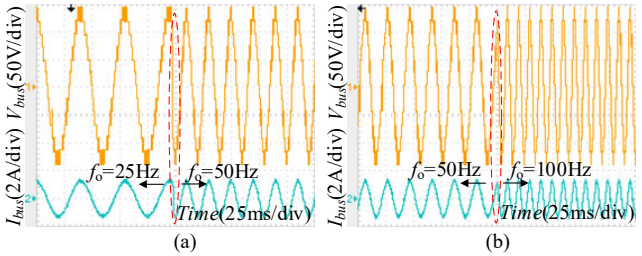

Fig. 11 Experimental waveforms of voltage and current when the change of output frequency.

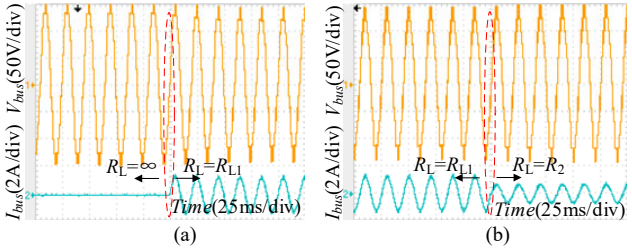

Fig. 12 Experimental waveforms of voltage and current under different loads.

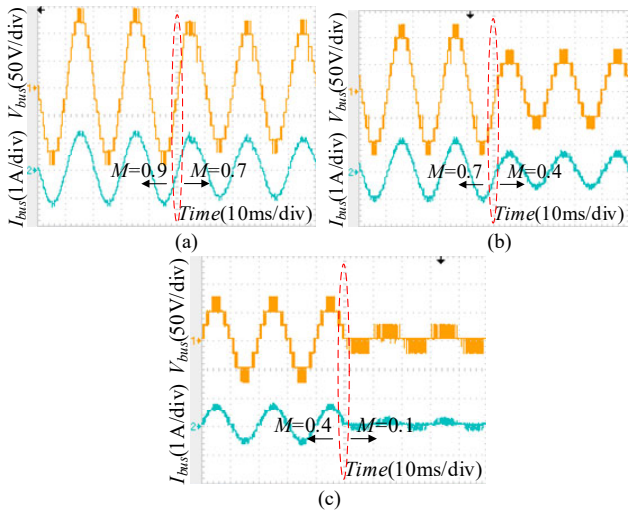

Fig. 13 Experimental waveforms of voltage and current under different modulation ratios.

VI. Conclusions

In this paper, an extended switched capacitor multilevel topology was proposed. The topology uses a single input and its extended structure has the ability to reverse polarity, thus not only the utilization of the H-bridge may be avoided, but also the peak inverse voltage of the semiconductors can be reduced. More importantly, the proposed topology owns a simple extended structure and inherent capacitor voltage self-balancing, which can effectively reduce the utilization of devices and manufacturing costs. To validate the performance of the proposed topology, the voltage ripple and losses of 13-level topology were calculated and analyzed. In addition, a comparative analysis of 13-level inverters is given. The comparison result proves that the proposed topology still has the advantage of reducing cost when outputting a low level. In the comparison of the extended topology, the proposed topology has the advantages of reducing devices, reducing the voltage stress of semiconductors, and reducing the cost of the topology compared with the existing topologies. Finally, the prototype of the 13-level inverter was built to verify the correctness and feasibility of the inverter. The extensive experimental results under various conditions demonstrated the efficacy of the proposed topology.

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