Wideband and High-power Nonlinear Measurement System for the Characterisation of GaN Amplifiers

---

A thesis submitted to Cardiff University in candidature for the degree

of:

Doctor of Philosophy

By:

Yashar Alimohammadi

18/December/2021

Division of Electronic Engineering

School of Engineering

Cardiff University

United Kingdom

This thesis is dedicated to my beloved parents

ABSTRACT

Recent RF applications and cellular networks architecture require to use high-power PAs, therefore it is critical to characterise their behaviour under appropriate operating condition with an accurate, reliable, fast, and flexible measurement system. As high-power PAs are typically operated in the pulsed mode, measurement system should be able to apply pulsed excitation and perform different types of characterisation under pulsed condition. Integrating pulsed capability into a measurement system to characterise large-signal behaviour of the device is relatively expensive and rigid in terms of instrumentation. Moreover, the inaccessible software that is used by the traditional systems has made them a vendor-defined system, where their application cannot be amended to scope specific phenomena. This is contrary to the need for a flexible pulsed system that can be extended and modified according to user preferences.

This thesis presents a high-speed pulsed measurement system that maintains flexibility, upgradability, accuracy, expanded power, and bandwidth ranges. The system is configured around NI modules to apply DC and RF signals and analyse them by employing vector signal transceiver (VST) with up to 1 GHz bandwidth. Due to employing programable VSTs, and accessibility of measured raw samples, different types of measurements can be performed, and small and large-signal behaviour of the device can be analysed. The aforementioned features of the developed measurement system assist to analyse the time-domain behaviour of the device and characterise the

physical phenomenon such as thermal, traps effect on large-signal behaviour of the device.

As an application of developed high-power measurement system and operating it under wideband RF stimulus, the trapping effect on the large-signal behaviour of the PA is investigated. Time-domain behaviour represents significant variation in the input and output of the device. These variation leads to change the optimum load impedance of the device in time-domain, which decreases the performance of the device up to 8% and mostly linked to the traps of the device. moreover, linearity of the device in time-domain is analysed and intermodulation distortion levels of the device are extracted in time-domain at various timeslots of RF pulses. Interesting results are achieved by applying various drain-lag levels to the device, which shows linearity of the device increases up to 5 dB in back-off operation regime.

In this work, for the first time, a nonlinear behavioural model is provided for the surface traps of GaN device. Developed measurement system utilise Cardiff behavioural model during load-pull measurements to decrease the number of load impedances to find the optimum impedance of the device and increase the speed of process. By applying gate-lag levels and pre-charging the surface traps of the device before conducting active load-pull measurements, relation between the Cardiff behavioural model and gate-lag levels of the device is investigated and a new model is achieved by using quadratic function to incorporate the gate-lag effect into the Cardiff behavioural model. Furthermore Cardiff behavioural model variation in time-domain is also achieved at different gate-lag levels and clarifies pre-charging traps can reduce the variation in time-domain.

ACKNOWLEDGMENTS

I would like to express my deepest and special gratitude to my supervisor Prof. Johannes Benedikt who believes in me to start pursuing my dreams in my academic life. He devoted an incredible amount of time during these years of my PhD to impart his experience and knowledge to me. His guidance always shed a light on occurred challenges during my PhD. I am forever thankful to him as without his knowledge, experience and support this PhD would not be achievable.

My sincere appreciation also goes to Prof. Paul J. Tasker for his encouragement and valuable guidance. His challenging questions and constructive ideas helped me to improve my understanding and knowledge. That was a great honour for me to work with him in my academic life.

I would like to profoundly thank Dr. James Bell for his support and friendly advice during the last 3 years.

I owe a debt of gratitude to all my colleagues in CHFE group for their support; specially Dr. Thoalfuker Husseini and Mr. Eigo Kuwata for their help to become an expert in the RF measurement system field.

My deepest appreciation goes to my Mum and Dad who their blessing and support have been always so inspiring to me. They taught me to be hardworking to reach my dreams. I owe them great gratitude as without their constant love, encouragement, and strong support, none of my achievements in my life would have been possible.

I also thankful to my sister Sahar and my brother-in-law Hamid for their emotional and unsparing support and encouragement.

Finally, I would like to express a special " thank you" to the most important friend in my life, my beloved wife Kiana, for her continuing love, friendship, and support. Mainly, without her love, motivation, patience, and support none of the achievements in this work would have been possible.

LIST OF PUBLICATIONS

[1] Y. Alimohammadi, E. Kuwata, X. Liu, J. Bell, L. Wu, P. Tasker, J. Benedikt, "Pulse Profiling Active Load Pull Measurements," 2020 IEEE/MTT-S International Microwave Symposium (IMS), Los Angeles, CA, USA, 2020, pp. 759-762, doi: 10.1109/IMS30576.2020.9223989.

[2] Y. Alimohammadi, E. Kuwata, X. Liu, E. Azad, J. Bell, L. Wu, P. Tasker, J. Benedikt, "Incorporating Gate-Lag Effects into the Cardiff Behavioural Model," 2020 50th European Microwave Conference (EuMC), Utrecht, Netherlands, 2021, pp. 684-687, doi: 10.23919/EuMC48046.2021.9338185.

[3] Y. Alimohammadi, E. Kuwata, X. Liu, J. Bell, L. Wu, P. Tasker, J. Benedikt, " Time-Variant Linearity and Power of GaN Devices within a new RF Pulse PA Regime", to be submitted to Transaction on Microwave Theory and Techniques (T_MTT)

[4] E. Kuwata, Y. Alimohammadi, X. Liu, J. Bell, P. Tasker, S. Shinjo, J. Benedikt, "Effects of Load Impedances at Third Order Intermodulation Tones," 2020 15th European Microwave Integrated Circuits Conference (EuMIC), Utrecht, Netherlands, 2021, pp. 201-204, doi: 10.1109/EuMIC48047.2021.00062.

Table of Contents

LIST OF ABBREVIATIONS

ACLR	Adjacent Channel Leakage Ratio
AM-AM	Amplitude to Amplitude Distortion
AM-PM	Amplitude to Phase Distortion
ALP	Active Load-Pull
CAD	Computer Added Design
CW	Continuous Wave
DPR	Distortion Power Ratio
DUT	Device Under Test
DWLUT	Direct Wave Look-Up Table
FFT	Fast Fourier Transform
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
IF	Intermediate Frequency
IFFT	Inverse Fast Fourier Transform
IMD	Inter Modulation Distortion
LabVIEW	Laboratory Virtual Instrument Engineering Workbench
LSNA	Large Signal Network Analyser
LO	Local Oscillator
NVNA	Nonlinear Vector Network Analyser
NMSE	Normalised Mean Square Error
NI	National Instrument
PA	Power Amplifier

PM	Power Meter
PXIe	PCI Extension for Instrumentation
RF	Radio Frequency
R&S	Rohde & Schwarz
S-parameters	Scattering Parameters
SMU	Source Measurement Unit
SRH	Shockley Read Hall
T-Clk	Trigger Clock
VNA	Vector Network Analyser
VSA	Vector Signal Analyser
VSG	Vector Signal Generator
VST	Vector Signal Transmitter

CHAPTER 1: INTRODUCTION

1.1 BACKGROUND

The power amplifier (PA) is one of the paramount parts of wireless communication systems. In each node of a network, PAs have a vital role to prepare the intended signal and compensate the loss in the network. Their behaviour at different frequency and power regimes can affect the quality of the communication and decline the efficiency of a wireless network. Therefore, it is important to accurately design and comprehensively characterise PAs to meet the requirement for different applications. To measure different performance metrics of PAs, different types of validation techniques are used, and various instruments are designed to accurately characterise the device to correctly employ them in the wireless networks [1-3].

1.1.1 HIGH POWER PA CHARACTERISATION

High-power GaN PAs are becoming popular in communication systems during the recent decades. They are widely used in the base stations of cellular networks and satellite and communication networks where producing high power is required [4, 5]. Generally, transistor characterisation can be classified into three main types: DC, small-signal, and large-signal characterisation. All characterisations on high-power devices should be conducted in the pulsed mode as operating the device in continuous mode, will increase the temperature of the device rapidly and cause damage to the device.

In DC characterisation, current-voltage relation is typically represented to measure the knee voltage, saturation current, and maximum current and voltage of the device. DC-IV curves can also be achieved under pulsed condition, which can be used to investigate the trapping and thermal effect on the device characteristics [6].

Small-signal measurements are conducted to represent the linear behaviour of the device when the transistor is operated in the low-power and linear regime [7]. However, large-signal measurements investigate the device in high-power regime when they start to produce harmonic products during operating in the nonlinear regime. In this kind of characterisations, some important performance metrics are generally considered such as gain, drain-efficiency, linearity (ACLR).

1.1.2 TRAPS

In GaN devices, there are some traps in the different layers of the semiconductor of the device. Traps of the device can capture (or release) the current carriers from (to) channel of the transistor. In fact, they change the density of the carriers in the channel of the transistor, and it can have impact on the input and output of the transistor [8]. There are many trap centres in the different layers of transistor, and they can be activated with various time-constants, therefore by categorising them into slow and fast traps, they can change the low and high frequency behaviour of the device over a wide range of drive level [9].

1.2 MOTIVATION

Due to existing difficulties in driving and analysing high-power PAs in the pulse mode, characterising them is a challenging area for engineers in general, and especially in terms of large-signal characterisation. Acquisition of the pulsed signals

requires wide bandwidth to analyse the narrow pulses which are commercially used in current cellular networks. PNA, NVNA, LSNA can apply and record the pulsed RF signals with different acquisition techniques. These products have wide range of applications in the RF characterisation setups, however, to characterise the large-signal performance metrics of the PA and performing the active load-pull measurements under pulsed condition they have some limitations regarding to their complexity of acquisition techniques, instantaneous bandwidth, memory and speed. To analyse the narrow pulses, mentioned instrumentation employ narrowband technique which operates the receivers in a manner based on filtering the recorded samples of output of PA to only keep the main frequency. Consequently, output of the device is CW and it doesn't contain other frequency terms.

These limitations, urge to design an advanced IQ based measurement system to provide opportunity to tackle the aforementioned issues in pulse measurement systems. Programable IQ based and wideband measurement system leads to analyse the device with pulsed DC, CW-RF, and multitone RF signal, and it can conduct the various types of measurements such as active load-pull to provide the required information to RFPA designers. This kind of measurement system can have a wide range of applications in radar communication, where the PA is operated in pulsed mode and it is crucial to measure the physical and intrinsic behaviour of GaN PAs. Moreover, as an application of developing such measurement system, different physical and intrinsic behaviour of the device such as thermal, traps can be comprehensively characterised and sort out the lack of information on their effect on large-signal behaviour of the device.

1.3 OBJECTIVES

Presented research in this thesis is focused on developing a measurement system to characterise the high-power and wideband power amplifiers for 5G. Instead of employing a rigid and complex measurement setup, a flexible, programable, and rapid measurement system can be beneficial to characterise the power amplifiers of 5G networks. Consequently, the main objective of this research will be as following

- To add a capability to measure high-power PAs with up to 200 W peak power.
- To develop a system to perform multi-tone measurement on high-power PAs with up to 1GHz bandwidth.
- To characterise the intrinsic phenomenon of the device such as thermal and trapping effect and investigate its impact on the large-signal behaviour of the device.

1.4 THESIS STRUCTURE

This thesis is written into six chapters to comprehensively present the achievements of PhD project. Following this introduction, chapter 2 will review some of recent achievements of published literature about pulse measurement systems, trapping effect on GaN power amplifiers, and Cardiff behavioural model. In this chapter, some conventional high-frequency instrumentation, which can characterise the large-signal behaviour of the device and perform active load-pull measurements under pulsed condition are introduced. It also reviews the understanding of the traps of the device at different frequency ranges including, proposed models to analyse traps, and points out the models proposed to investigate them at different layers of the device.

Chapter 3 introduces the developed measurement system‘s structure and some of the important features of its employed modules. The pulse capability is added to the active load-pull measurement system which is based on NI modules. Utilised techniques to prepare the measurement system and synchronising the different pulsed signals are explained and an employed approach to record the pulses in the VST system is described. Important performance metrics which typically evaluate the pulse measurement systems are measured to present the capability of the developed measurement system to generate and record the RF and DC pulses. Then, applied calibrations on the recorded data are mentioned. The performance metrics of the system are provided and illustrated in this chapter. Moreover, to perform the active load-pull measurements on high power PAs at fundamental (1.8 GHz- 2.8 GHz), second harmonic (3.6 GHz- 5.6 GHz) and baseband frequency range (200 MHz- 1 GHz) with 1 GHz instantaneous bandwidth, a dedicated test-set, and phase reference standard (PRS) are designed and introduced in chapter 3.

The focus of the thesis then shifts to trapping large-signal effect in chapter 4. Firstly, to analyse the basic trapping effect PIV measurements are performed at different drain-lag levels and active load-pull measurements are carried out at different time-slots of the RF-pulses then by analysing the recorded data of input and output of the device, time-domain variation of the optimum load impedance, and source impedance variation are observed. All the aforementioned measurements are repeated at different gate-lag and drain-lag levels to extract the trapping effect on the input and output time-domain variation of the device. Moreover, the linearity of the device in time-domain at various drain-lag levels is examined and time-domain intermodulation distortions (IMDs) are analysed at different drain-lag levels.

Chapter 5 focuses on developing the Cardiff behavioural model as one of the applications of the measured data and measurement system. As pulsed measurement enhances some capabilities of the system to investigate the trapping, self-heating, and thermal effect, it would be interesting to analyse the impact of aforementioned phenomenon on the Cardiff behavioural model. This chapter extracts the effect of the surface traps of the device on the Cardiff behavioural model and provides a new behavioural model which can incorporate the gate-lag effect. Moreover, time-domain variation of the Cardiff behavioural model and its reason is analysed.

Chapter 6 concludes the whole work presented in this thesis, while concentrating on the strengths and weaknesses of the presented work. This chapter also proposes possible directions for future research.

1.5 REFERENCES

[1] M. Horibe and I. Hirano, "Vector Network Analyzer Calibration for Characterization of Packaged Power MOSFET Device at RF Frequency," in *2020 95th ARFTG Microwave Measurement Conference (ARFTG)*, 2020: IEEE, pp. 1-4.

[2] A. K. Sahoo and K. Rawat, "Full 2-Port Vector Network Analyzer using Nonlinear Calibration of Six-Port Reflectometer," in *2019 IEEE MTT-S International Wireless Symposium (IWS)*, 2019: IEEE, pp. 1-3.

[3] S. Ahmed, M. S. El Dine, T. Reveyrand, G. Neveux, D. Barataud, and J.-M. Nebus, "Time-domain measurement system using Track & Hold Amplifier applied to pulsed RF characterization of high power GaN devices," in *2011 IEEE MTT-S International Microwave Symposium*, 2011: IEEE, pp. 1-4.

[4] G. Formicone, J. Burger, J. Custer, R. Keshishian, and W. Veitschegger, "A study for achieving high power and efficiency based on high bias operation in C-and X-band GaN power amplifiers," in *2018 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, 2018: IEEE, pp. 39-42.

[5] J. Wong, N. Watanabe, and A. Grebennikov, "High-power high-efficiency broadband GaN HEMT Doherty amplifiers for base station applications," in *2018 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, 2018: IEEE, pp. 16-19.

[6] N. Ramanan, B. Lee, and V. Misra, "A novel methodology using pulsed-IV for interface or border traps characterization on AlGaN/GaN MOSHFETs," in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, 2014: IEEE, pp. 366-369.

[7] C. F. Gonçalves, L. C. Nunes, P. M. Cabral, and J. C. Pedro, "Pulsed I/V and S-parameters measurement system for isodynamic characterization of power GaN

HEMT transistors," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 28, no. 8, p. e21515, 2018.

[8] J. M. Tirado, J. L. Sanchez-Rojas, and J. I. Izpura, "Trapping effects in the transient response of AlGaN/GaN HEMT devices," *IEEE Transactions on Electron Devices*, vol. 54, no. 3, pp. 410-417, 2007.

[9] A. Benvegnù *et al.*, "Trap characterization of AlGaN/GaN HEMTs through drain current measurements under pulsed-RF large-signal excitation," in *2015 IEEE MTT-S International Microwave Symposium*, 2015: IEEE, pp. 1-4.

CHAPTER 2: LITERATURE REVIEW

2.1 INTRODUCTION

The performance of the communication networks strongly depends on the power amplifiers, and their performance metrics such as gain, efficiency and linearity. High power amplifiers, which are generally used in base stations, radar, and satellite communication systems, operate in high power regime to provide strong output for users. GaN devices can deliver high output power, due to their high band gap energy, are becoming popular candidate in various communication systems. However, this type of devices suffers from memory effect which includes traps. To characterise the high-power amplifiers, pulse measurement capability is proposed [1] and it provides an interesting point of view to investigate the intrinsic phenomenon of the power amplifier. One of the applications of the pulse measurements is that to identify the memory effect on the performance of power amplifier, as it provides a manner to recognise the thermal, traps and self-heating effect on the performance metrics of the power amplifiers. Developing a measurement system to perform pulsed measurements in a wide frequency range to extract the small and large signal behaviour of the device is an essential requirement to correctly characterise the device. Some measurement systems have been gradually developed to perform pulse measurements at specific frequency range [2-5], starting from DC to RF fundamental frequency.

Developed instrumentation assist to meticulously extract the trap's effect over a wide range of frequencies, and obtain the circuit model for them [5-7]. The majority of the developed RF instrumentation such as NVNAs, LSNAs, pulsed generator and

analysers, VSTs assist to characterise the trapping effect on the device. Moreover, conducted research is dedicated to the trapping effect on DC-IV behaviour of the device, and provides their circuit model to comprehensively understand them.

The work of this thesis focuses on the development of a fast nonlinear measurement system to perform the pulse measurements over a wide range of frequencies and characterising large-signal effect of traps. This chapter discusses the current instrumentation and setups to provide pulse capability, then reviews the achievements occupied techniques and achievements of pulsed active load-pull measurements. It includes the development of device characterisation and the reasons behind the adoption of nonlinear measurements. Also, it reviews previously achieved results of pulse profiling measurements and traps large signal and small signals effect on DC to fundamental frequencies. Moreover, at the end of this chapter some of the most important achievements around Cardiff model are summarised, since developing the Cardiff model to incorporate the gate-lag effect is considered as one of the applications of the established measurement system.

2.2 PULSE MEASUREMENT SYSTEMS

Pulsed RF measurement capability is becoming prevalent in industrial characterisation in recent decades and prominent industries in RF validation and characterisation technology such as Keysight, Anritsu, and Rohde & Schwarz have introduced various modules to perform different types of large and small-signal characterisations under pulsed condition [8-11]. performed by employing different RF measurement technologies which can generate and acquire RF pulses. Developed technology in industry combined with some technical manners from academic research groups in utilising them to conduct various interesting active large-signal measurements.

Keysight has developed some PNAs, NVNAs to generate and analyse pulsed RF signals. Key parameters of pulsed measurements such as duty cycle, pulse width, pulse repetition interval (PRI), resolution of acquisition are directly linked to instruments' fundamental specifications. Some features of different PNAs with pulse capability are listed in Table 2-1.

Table 2-1: Keysight PNAs important specifications [8]

PNA model	**Frequency range**	**Maximum IF bandwidth**	**Minimum pulse width**	**Minimum PRI**
PNA	20, 40, 50, 67 GHZ	40 kHz	50 µs	170 µs
PNA-L	20, 40, 50 GHz	250 kHz	10 µs	80 µs
PNA-L	6, 13.5, 20 GHz	600 kHz	2 µs	40 µs

These PNAs can be used either in narrowband detection or wideband detection modes with the IF bandwidth ranging from 40 to 600 kHz. Some hardware setups for characterising the pulsed RF-PAs by using the aforementioned PNAs have been suggested [8]. Despite, PNA-L possesses internal IF gate switches, it was recommended to use an external RF switch for receivers gating. This configuration was used for narrowband detection method to provide shorter gate widths (<20 ns) than those obtained using the internal IF gates. The mentioned configuration assisted with the measurement of narrower pulses, however, it increases the complexity of the system. Another configuration was proposed, shown in Figure 2-1, with an external pulse generator to generate the complex pulses which can apply RF pulses with advanced shapes to examine the linearity of the device under pre-shaping condition.

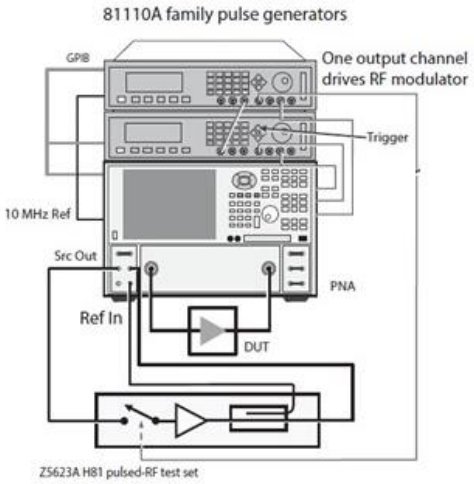

Figure 2-1: Pulse measurements with PNA and external generators and switches [8]

Proposed setup was also extended to bias the device under pulsed conditions and perform wideband and narrowband detection. Note that when using narrowband detection with this condition, three pulse drives were used for the A, B and combined R1/R2 IF gates. If independent control of all the receiver gates is desired for full flexibility, then six pulse output modules were needed, requiring a third pulse generator [8].

Pulse measurement capability is also provided in PNA-X. A setup was proposed in [9] with 81110A RF pulse generator, PNA-X, DC power supply. This setup allows to analyse narrow pulses with 10 ns pulse widths by employing the narrow-band technique in PNA-X. Moreover, it could perform different types of pulse measurements such as pulse-to-pulse to track changes in the behaviour of the PA over a chain of consecutive pulses and pulse profiling measurements to analyse the behaviour of the device at different timeslots within the pulse. However, it suffers from lack of memory and it cannot keep recording for a long time. Due to using different modules to generate DC and RF signals, and analyse waveforms, a more

complex method is required for the external synchronisation of RF generators and receivers.

Time and frequency domain measurements under RF pulse excitation were conducted with R&S real-time scope and its advanced software. The designed system was intended to be used in radar system to characterise the required metrics of these systems such as revolution per minute (RPM), antenna beam pattern, pulse parameters and pulse trends [10]. An IQ-based measurement system was designed with an advanced pulse generator (SMBV K301) to generate complex pulse shapes. 4 channels scope with 4 GHz instantaneous bandwidth and 16-bit resolution, with a maximum 10 GS/s was employed to characterise the behaviour of the device in the pulsed condition. Memory depth was improved in this module in comparison with previously released instrumentation and its available memory varies between 200 MS to 800 MS on one channel, depends on the operating condition. Improved memory depth of the system offered wide range of applications in investigating radar signals, as long-term acquisition is required in such communication systems.

Anritsu also provides pulse capability in their VNA products, which can perform pulse profiling, pulse-to-pulse, and averaged pulse measurements with up to 5 MHz instantaneous bandwidth in 70 kHz-40 GHz frequency range [11]. Regarding VNA's narrow bandwidth, it introduces a limitation to record the pulses with narrower pulse widths than 200 ns, and therefore cannot achieve the points-in-pulse measurement, which requires a wider bandwidth to ensure a certain in-pulse resolution.

To analyse the large-signal behaviour of the high-power PAs, large-signal measurements were performed in pulsed condition. [12, 13] proposed a setup to perform the load-pull measurements with employing LSNA. Suggested approaches

in [12, 13] was recording the whole samples of multiple pulses to generate a set of load-pull data with LSNA. There were some unrecorded pulses in the series of consecutive generated pulses, which led to have memory problem in the operated LSNA-based system. The system was designed to perform CW pulsed load-pull measurements; seemingly the use of multi-tone signals was not possible.

Various RF instruments and techniques, able to perform active load-pull measurements, use different technical methods to analyse pulses. Conventional measurements of modulated RF pulse parameters rely on envelope detectors. However, the non-linear characteristics of the detector lead to uncertainties within the detected waveform profile. If a signal is detected by different envelope detector, even by the same detector but different sampling rates, the results may be significantly different. Thus, a measurement solution that was independent of enveloped detectors was proposed [14]. The proposed solution relied on direct RF sampling and digital down-conversion. Firstly, a digital storage scope was used to record the samples, then FFT was applied to the recorded samples and the intercepted spectrum was centred at the origin of the frequency axis. IFFT was applied to the resulted baseband spectrum of the recorded pulse and finally a single pulse with its rising and falling edge of the pulse was separated in the time-domain. This technical approach has shown enough accuracy to analyse the pulse parameters.

2.3 ACTIVE LOAD-PULL PULSE MEASUREMENTS

Defining the optimum impedance of a transistor is crucial for PAs at various output power regimes to delivering optimal performance, such as high efficiency, gain, linearity, and output power, and providing a clear understanding of various modes of amplifier operation [15].To appropriately terminate the load impedance, different

approaches such as passive load-pull, active and hybrid load-pull are proposed [16]. However, due to the shortcomings of passive load-pull, active load-pull is recommended for specific applications. Characterising the optimum impedance of the high-power PAs, which are typically operated in the pulse mode to limit the device temperature rise during the successive active load-pull measurements. Performing active load-pull measurements in the pulse mode emerges as a novel aspect allowing to investigate the device's dynamic optimal conditions and its dependence on time constants. For instance, to provide a proper load impedance termination under class-B operation, for pulsed-IV biasing and pulsed-RF (pulsed-IV/RF) excitations, an adaptive harmonic active load-pull was investigated in [12]. Pulsed-IV/RF measurement was used as the technique of choice for characterisation and modelling of RF devices as it reduces low-frequency memory effects on transistor and it is also a promising technique to assist with the design of efficient pulsed power-amplifiers for radar applications. In [12], the LSNA based setup was designed to perform multi-harmonic active load-pull measurements at 4 different conditions. These conditions are listed below:

1. Device was biased with continuous DC and CW signals was applied to the PA and $\Gamma_L(2\omega_0) = -1$ by using CW signal in the load side.
2. Device was biased with pulsed DC signals and pulsed RF signal was applied to source side and load impedance was tuned to a broadband 50 Ω.
3. Device was biased with pulsed DC signals and pulsed RF signal was applied to source side with $\Gamma_L(\omega_0)$ still set to 50 Ω but $\Gamma_L(2\omega_0) = -1$ by using pulsed signal in the load side.

4. Device was biased with pulsed DC signals and pulsed RF signal was applied to source side with $\Gamma_L(\omega_0)$ still set to 50 Ω but $\Gamma_L(2\omega_0) = -1$ by using CW signal in the load side.

Load lines of the measured conditions were shown from normal measurement regime (method 2). The expected class B load-line was not achieved, which clarified the importance of correctly terminating of second harmonic and conducting load-pull on the harmonics. The work also illustrated in method 1, self-heating effect led to smaller threshold voltage which results in higher drain currents, in comparison with other pulsed conditions.

An automated and vector error-corrected active load–pull system allowing the characterization of high-power transistors under coherent pulsed RF and pulsed DC operating conditions were conducted in [17]. It focused on the characterisation of a 240 μm^2 GaInP/GaAs heterojunction bipolar transistor (HBT) (Thomson CSF-LCR, Orsay, France). Source and load–pull measurements of such a transistor were reported for different pulse-widths. HBT device was operated in class AB mode and, AM/AM and AM/PM of the device at different sections of the pulse were extracted when the load impedance set to the optimum impedance of the device. It was shown that AM/AM and AM/PM of the device declined within the pulse. Moreover, electrothermal model of an HBT provided in [18] was validated.

Different approaches and techniques are employed to make the active load-pull measurements possible with LSNA to extract new information. Real-time active load-pull (RTALP) characterisation under pulsed multi-tone stimulus was performed on a power transistor with an LSNA [13]. This was achieved using sub-sampling down-conversion technique. The setup is capable of load-pull measurements on device under

pulsed using multi-tone excitation. Here, a multiple-recording time-domain approach was employed to record data from a device under test when applying pulsed three-tone signals. The proposed technique was based on the progressive acquisition of the required number of samples and explained in detail in [19, 20]. In this method, multiple pulses were applied to the device to acquire a single set of data at a specific load impedance and 16 samples were recorded every ten modulation cycles (ten PRI cycles). Maximum bandwidth of applied signal was 25 kHz and duty cycle of pulses was 0.15 %. The proposed method was validated by providing simulation results and offered some capabilities such as real-time active load-pull measurements with reduced measurement time and greater simplicity.

In [21] large-signal characterisations utilising a VNA and a sampler-based LSNA were compared and a robust and reliable relative phase calibration on a dual frequency phase differential was used. This approach involved combining an f_0 reference with a harmonic signal, f_n, and passing it through the LSNA measurement path [22] into the sampling oscilloscope. Figure 2-2 shows the dual-frequency phase differential calibration's setup, and in this way, the relative phase of the two signals was measured by both the LSNA and the sampling oscilloscope. During measuring on wafer devices, it was not possible to attach the oscilloscope directly at the measurement plane, so any dispersion in the output half of the measurement path must be corrected, this was done with routine passive network measurements. RF-IV waveforms under CW and pulsed condition of GaN device were also extracted. It was proved that information for waveform engineering can be collected in pulse mode as well as CW, using either a broadband sampling receiver (LSNA) or a narrow band VNA receiver. The systems have shown precise results to allow accurate analysis of device behaviour.

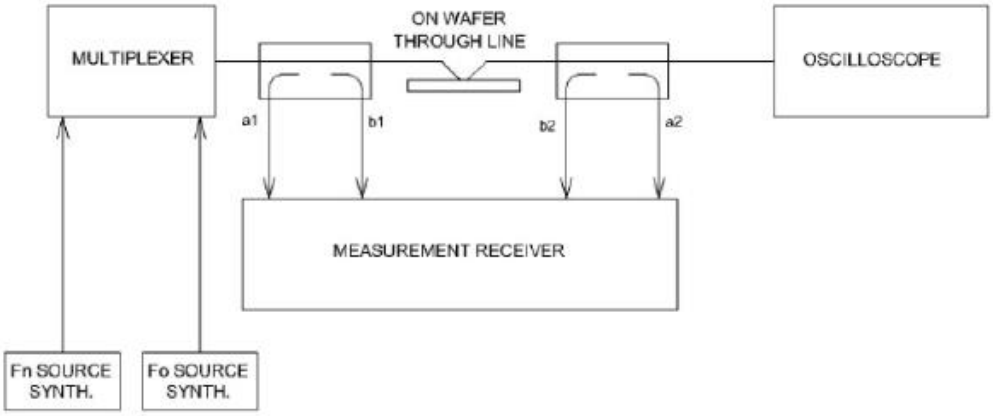

Figure 2-2: Dual frequency phase differential calibration [21]

2.4 PULSE PROFILING

Pulse profiling measurement is an interesting technique to investigate power amplifiers behaviour in time-domain which is used as technical method to understand the trapping and thermal effect in power amplifiers. Through the profiling technique, real-time samples of the output and input waveforms of the device can be captured immediately after applying the RF pulse to the device to cover the whole pulse-width including rising and falling time. In pulse profiling measurements, averaging is not applied on the recorded samples, instead the recorded samples at different sections of the pulse are assembled to directly represent the real-time behaviour of the PA. This high-performance system achieved rapid sampling while maintaining a low noise floor to cover a high dynamic range.

A technique for characterizing the pulse profile of a RF amplifier over a very wide power range under fast-pulsing conditions was presented in [23]. A pulse-modulated transmitter was used to drive a device under test (DUT) with a phase-coded signal that permits for an increased measurement dynamic range beyond standard techniques.

The proposed technique was capable of testing device with 160 dB measurement range, and 5 ns resolution. Figure 2-3 shows the utilised algorithm which is based on generating multiple pulses and using multiple samples of the pulse at a single time location in the pulse profile, along with a correlation technique, to increase the measurement SNR which is linearly related to the number of the recorded pulses.

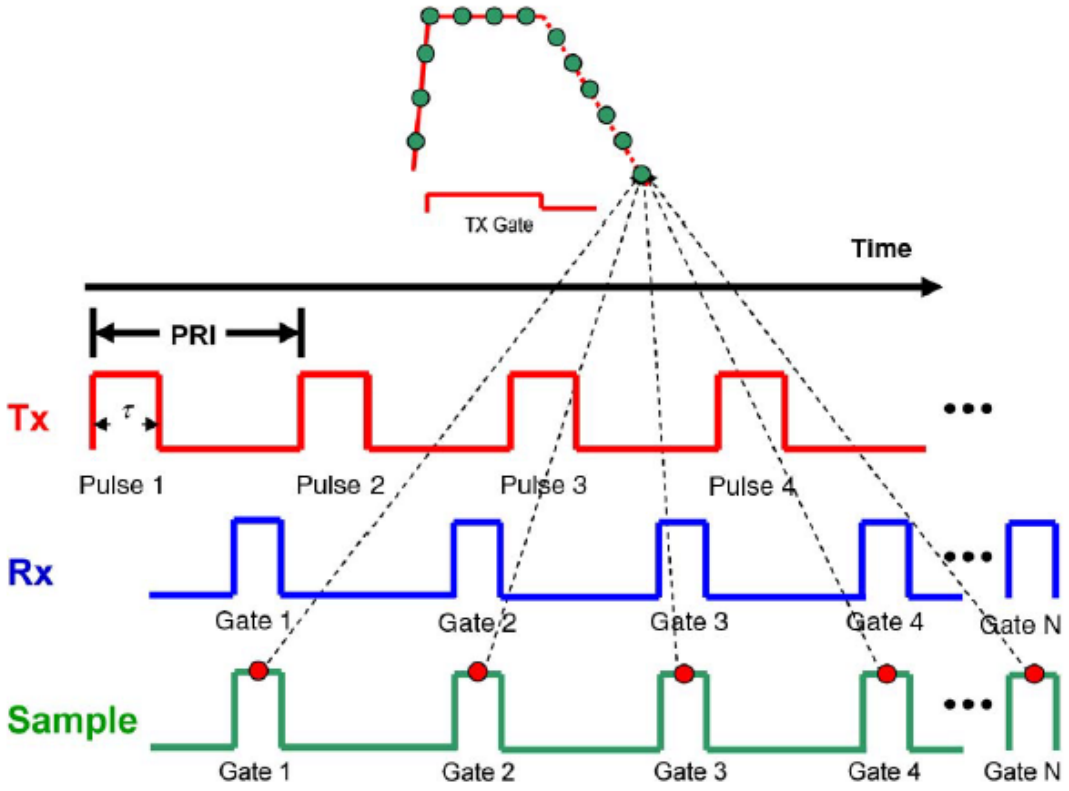

Figure 2-3: Pulse integration used to generate a single sample on the pulse profile [23].

In profiling measurements, the resolution of the measurement is limited to the maximum sample rate of the system to extract samples and achieve the instantaneous response of the device. However, in some publications, profiling measurements have been introduced to measure different sections of the pulse and calculate the average of the recorded samples with different lengths. In [24] an on-wafer set up for the characterization of high voltage (26V) power HBTs under simultaneous pulsed RF

signal and pulsed DC test conditions was presented. A narrow band VNA and sampling scope were operated to measure both RF power and DC profiles. VNA's pulse acquisition was based on narrow band acquisition technique utilizing a 500 Hz band pass filter at IF, to perform vector measurements of power wave ratios at the centre spectral line of the frequency spectrum with its Sin(x)/x shape for pulsed time-domain signals. Typically, a signal with the pulse width of 300 ms and a 10% duty cycle was applied. AM/AM, AM/PM and PAE of the device at beginning and end of the pulse were then measured. Moreover, input and output current variation within the pulse was recorded in HBT, which an increasing, due to a thermal effect, variation within the collector current within the pulse.

2.5 INVESTIGATION OF TRAPPING EFFECTS

Due to the large band gap of GaN-based semiconductors and their capacity for producing high output power, their application in the communication system has tremendously increased. However, this kind of semiconductor suffers from memory effects that are caused by traps. These can capture (or release) the current carriers from (to) channel. Overall, traps can produce a strong effect on a transistor's input and output current and its transients.

Traps are located in different layers of a transistor; hence different energy levels and time scales are required to activate them. For instance, traps of the surface layer typically can be activated by applying low power signals to the device, while deeper layer traps usually require more power to be activated [25]. This phenomenon results in a device performance that varies over a wide range of frequencies and power levels. In this section some of the practical techniques are introduces to identify traps and their impact on the important metrics such as linearity or gain.

2.5.1 TRAPS IDENTIFICATION TECHNIQUES

One main approach to investigate the trapping effect in the GaN PAs is to apply different drain-lag and gate-lag to the device, then observe the intended performance metrics. The term “drain-lag” and “gate-lag” are used to describe the slow transient response of the drain (gate) current when the drain (gate)-source voltage is pulsed [26, 27]. This type of measurements is typically for DC-pulsed characterisations. To apply different drain-lag levels to the device, its gate voltage is less than pinch-off voltage and drain voltage is set different values to populate traps without changing the temperature of channel. Typically, the value is set to be at least 2 times more than the device’s bias point to populate the traps in the buffer layer of the device [28]. Furthermore, during gate-lag measurements the applied voltage to the drain-source is often set be zero to fill the traps of the device in the surface layer.

Trapping effects in the GaN technology was analysed in [29] by employing the pre pulsing technique to populate the traps within the first pulse and then observe the device performance during the second pulse. The DUT was a prototype 0.5 µm GaN-on-Sapphire FET that was manufactured by the Polish Institute of Electronics Materials Technology. As applied voltages in the pre-charging state do not generate I_{DS}, the thermal level of the device remains unchanged and any modification to the measured device performance was related to the traps of the device. Figure 2-4 illustrates the drain-lag effect on the DC curves of the device, which cause knee walk-out and V_T (threshold voltage) variation in the low power regime [30]. Such measurements depict a practical method for characterizing trap-related lag effects in GaN FETs, and were intended both for modelling as well as for assisting further technology developments.

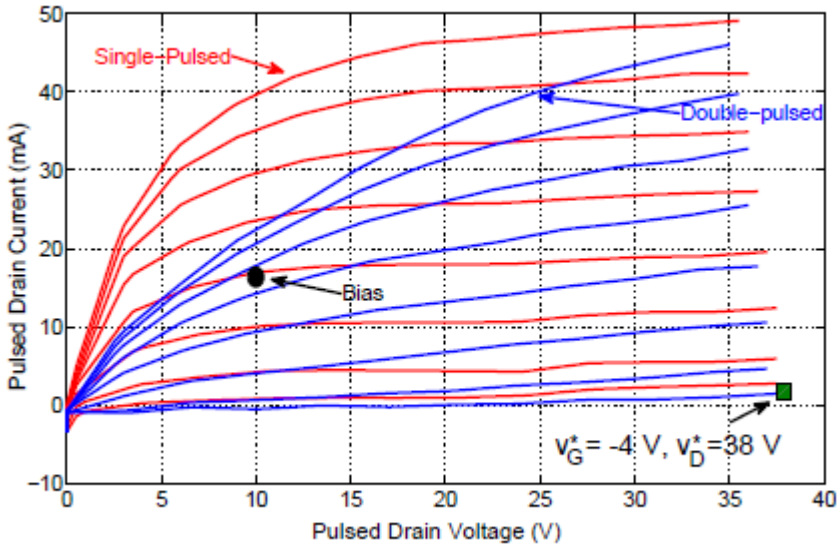

Figure 2-4: drain-lag effect on the DC-IV curves with pre-pulsing V_{GS}= -4 V, V_{DS}= 38 V, DUT is unpassivated GaN on Sapphire FET prototype, gate length= 0.5 µm, device periphery= 2×100 µm, V_{GS} from -3.5 V to 0 V with 0.5 V steps, bias point= (-2 V, 10 V) [30].

However, the pre-charging the traps can be conducted using different approaches. In [30], pre-pulsing was utilised to pre-charge the traps before biasing the transistor. However, another technique was utilised in [4, 31] to periodically pre-charge the traps by applying the voltage levels in the "off" section of the applied pulsed DC. Figure *2-5* illustrates both approaches to apply DC signals to the device.

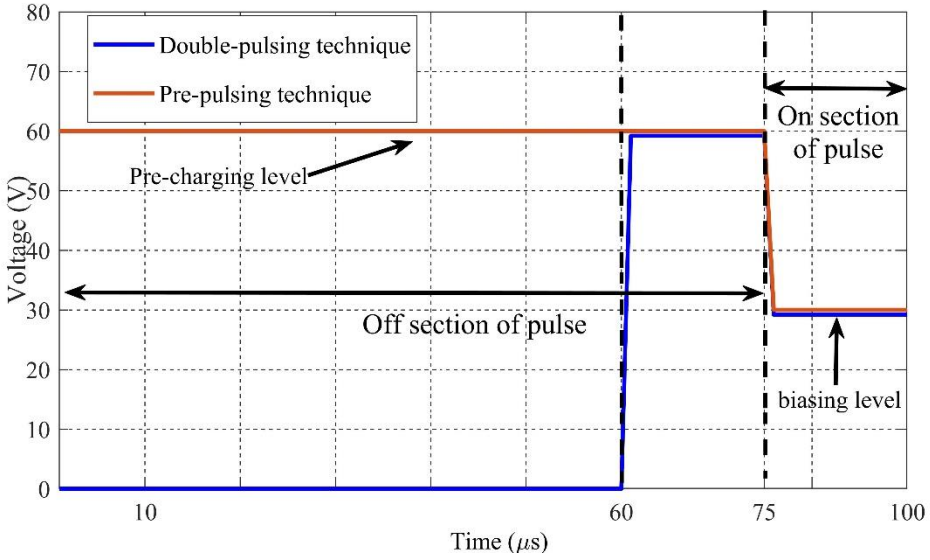

Figure 2-5: Structure of applying DC pulses to pre-charging the traps of the device.

Multi-tone measurements are another method to identify the trapping effects on the device large signal behaviour. In this method, multi-tone excitation with varying frequency spacing (Δf) between the main tones are applied to the device. A specific Δf activates traps which are associated to this specific frequency difference, affect the device behaviour [32]. Thus, by swiping the Δf, different traps centre and their activation frequency and time constants can be achieved. In this method stimulus can be either in pulsed or continuous mode.

2.5.2 LARGE AND SMALL SIGNAL EFFECT OF TRAPS

In [33], the transient analysis of an AlGaN/GaN HEMT device was presented. Drain–current dispersion effects were investigated. Pulsed gate-lag and drain-lag measurements were performed, to reveal clear mechanisms of current collapse and related dispersion effects during transient. Numerical 2-D transient simulations considering surface traps effects in a physical HEMT model were carried out. The presence of donor type traps acting as hole traps, due to their low energy level of 0.25

eV relative to the valence band, with densities $>1 \times 10^{20}$ cm^{-3} ($> 5 \times 10^{12}$ cm^{-2}), uniformly distributed at the HEMT surface, and interacting with the free holes that accumulated at the top surface due to piezoelectric fields, was found to account for the experimentally observed effects [33]. This kind of traps were mainly responsible for the observed negative effects in this technology. Time constants around 10 ms were deduced. Some additional features in the measured transient currents, with faster time constants, could not be associated with surface states [33].

A HEMT physical model was studied to explain the experimental results, and the structure has been analysed by means of a 2-D device simulator that includes time evolution of trap ionization. Based on recorded data, 10 μs time constant is determined during the drain-lag measurements, which can be related to the traps of the device located in layers other than surface layer. This indicated some trap centres in the device can re-act very fast and affect the high frequency behaviour of the device.

In previous paper [33], a single time constant was considered to analyse the traps of the device. However, capture and emission processes of the traps that have different time constants were repeatedly reported in [34]. An advanced microwave characterisation technique was developed in [34] to determine the capturing and emission time constants under wide pulsed-RF large-signal excitation of AIGaN/GaN HEMTs. The proposed approach was based on combined Continuous Waveform (CW) time-domain load-pull measurements and low frequency (LF) drain current transient measurements under a single wide nonperiodic pulsed-RF excitation to investigate trapping phenomena. The measurement system was based on the LSNA, which has limited capability for recording data over longer periods of time, a complex approach was developed to record the pulses with long pulse-widths. The trap capture and emission time constants were obtained by applying the current-transient method

for different RF large-signal input power levels and for varying duration of pulse-width (PW) of the one pulse-RF excitation. Capture and emission mechanisms were reported in Figure 2-6 and variation at the "on" and "off" sections of the pulse were associated with capture and emission, respectively. The capturing effect was observed at high power regime when the strong current collapse occurs, due to trapping effect. Moreover, the impact of pulse width and drive power on the capture and emission time constants were investigated. It was concluded that the capturing time constant is not related to the pulse width of the stimulus, however, emission time constant is increasing by expanding the pulse width.

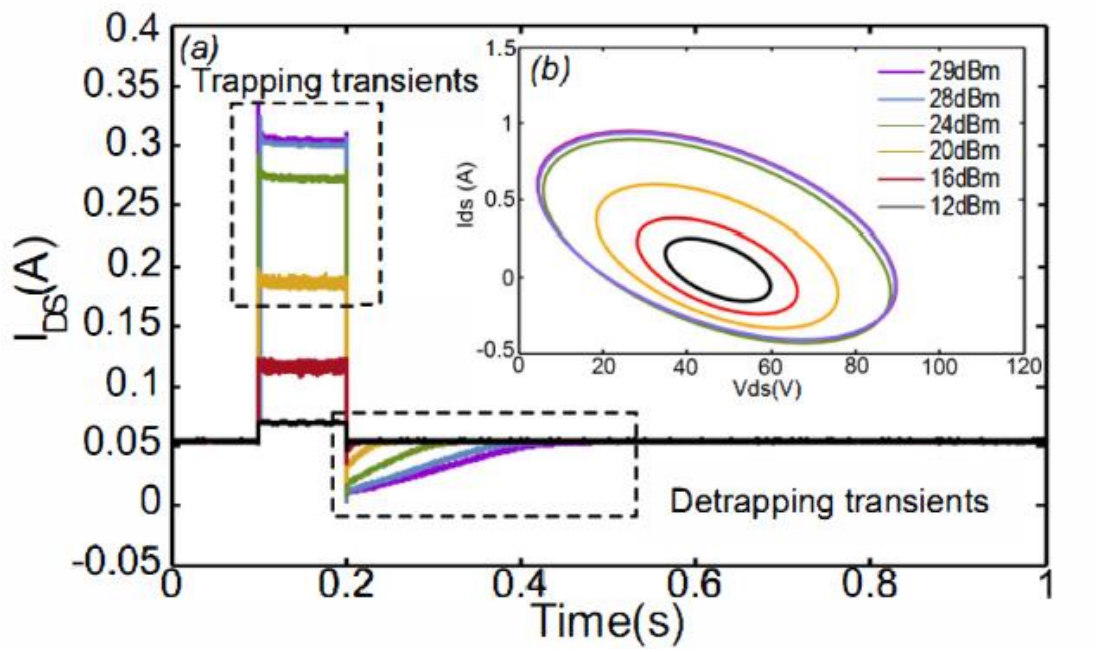

Figure 2-6:(a) trapping and de-trapping mechanisms over 17 dB dynamic range, (b) LF drain current transient measurements for PW=100ms and corresponding extrinsic CW output load cycles measured at f_0, I_{DS}=25 mA/mm at V_{DS}=50 V [34]

The influence of the RF load-line excursion in the drain current collapse after the RF stimulus was also demonstrated. As can be seen from Figure *2-7* by applying higher input power to the device and operating it in higher compression level, current collapse

increases at the start of pulse and its impact last for longer time. Moreover, it shows by increasing drive level, time constant of traps emission increases.

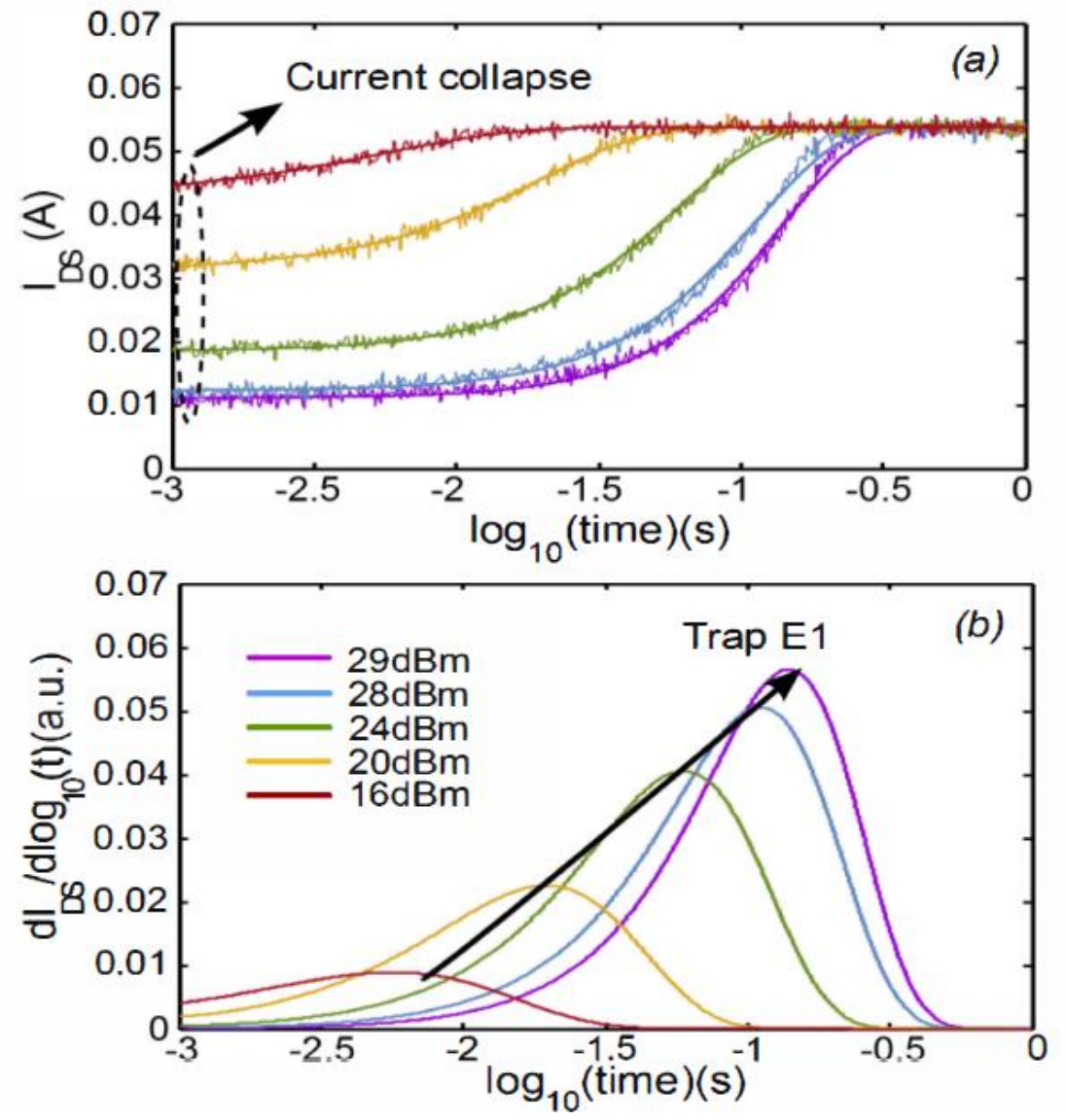

Figure 2-7: (a) Emission LF drain current transient measurements (PW= 100 ms). (b) Time constant analysis of Emission transients [34], I_{DS}=25 mA/mm at V_{DS}=50 V .

Employed setup associated to the developed two-step experimental method provided the definition of trap capture and emission time constants through the application of the current-transient method for different RF large-signal input power levels and for varying pulse-width durations of a one wide pulse-RF excitation. This technique allowed investigation of the trapping behaviour of transistor in real RF conditions. Applied to this GaN technology, this measurement method demonstrated the

logarithmic dependence of capturing and emission effects on RF input-power levels and pulse-width. In fact, the amplitude and time constant of traps increased with longer pulse-width durations and higher the compression levels.

In [35] an explanation for the observed differences on the trapping time constants extracted from low frequency Y_{22} and I_{DS}-Deep-Level Transient Spectroscopy (IDLTS) on GaN HEMT device was presented and for the first time it was shown, traps effect on the large signal and small signal behaviour of the device. It was shown that time constant of traps depends on the stimulus condition and varies in small signal and large signal measurements. Two different time constants have been achieved for large-signal and small signal measurements that are shown in (2-1) and (2-2). Moreover, reported results were validated with Shockley-Read-Hall (SRH) model.

$$\tau_{LS}^{-1} = \omega_0 \left\{ 1 + [1 + (V_0 - v_T) \left(\frac{k2}{V_{th}} \right)] e^{\frac{V_I}{V_{th}}} \right\} \qquad (2\text{-}1)$$

$$\tau_{SS}^{-1} = \omega_0 (1 + e^{\frac{V_{IDC}}{V_{th}}} + \frac{V_T k_2}{V_{th}}) \qquad (2\text{-}2)$$

The achieved time constants encompass both capture and emission dynamics, but depending on the excitation condition, one process can be suppressed by another one. For instance, if the V_{DS} drops a slow transient occurs associated to emission. The extracted time constants depended on V_T (trap voltage which is described by difference of emission and capture rates) and V_I is forcing function which is a linear combination of V_T and V_{DS}, V_{th} which is thermal voltage. Thus, extracted time constants vary in time domain as V_T is a time variant parameter. For the measured device the reported time constant for traps at small signal excitations was about 56 µs and at large signal conditions it was around 896 µs.

Traps of the device were classified in two groups based on their emission time constants [36]. Two types of deep-level traps (slow-emitting and fast-emitting traps) have been characterised apart by performing dedicated pulsed I-V measurements. Slow-emitting traps, triggered by threshold voltages (gate-source and gate-drain) and filled through reverse gate current, were observed. The slow-traps filling mechanism was modelled based upon a metal to channel trap assisted tunnelling (TAT) process. Moreover, the TAT model parameters are extracted from gate-source and gate-drain leakage current measurements. Moreover, the well-known fast-emitting traps were classically RC-like modelled. The authors validated their suggested model by performing load-pull measurement at 4 GHz. It was shown, the influence of fast emission traps, which are more-likely expected to be located in the GaN buffer layer, can be avoided by choosing the appropriate quiescent biasing conditions of 0V, 0V and by using a specific pulse conditions (pulse length: 1 µs, duty cycle: 0.1 %). However, slow emission traps are determined to be activated for drain-source and gate-source voltages of 15 V and -6 V, respectively. Furthermore, a physics-based compact model was developed to accurately predict the slow traps filling mechanisms. The physical location of such traps is more likely to be in the AlGaN barrier layer.

In one interesting researches on characterising the time constant of capturing and emission of traps, researchers proposed an experiment in [37] by performing a series of large signal two tone measurements with varying frequency separation and successive recording. One of the most important achievements of [37] was the observation that the capture time constant are comparable to the slow-varying envelope variaitons of modern radar signals, ranging from less than a microsecond to a few tens of milliseconds. They have investigated the time constant of the traps by applying multi-tone signals and analysing the DUT for different periods of the RF

signals. A VSG-VSA pair was used to generate and receive a single period of waveform, then by considering 30-100 s delay the second period of the waveform was measured. It was reported that by increasing the frequency separation, first period of the excitation was not enough to charge the deep-level traps, since successive results of next periods of signal shows progressively lower output power.

In [38] traps effect on the AlGaN/GaN HEMT of 0.15-μm ultrashort gate length and 8 × 50 μm2 gate width (GH15) was analysed through three different measurement techniques which were low frequency (LF) S-parameters, drain-current deep level transient spectroscopy (I-DLTS), and LF drain noise characterization. These three different measurements techniques were performed for varying chuck temperatures ranging between 25 $^{\circ}C$ and 125 $^{\circ}C$ by keeping the same biasing condition. Furthermore, thermal resistance (RTH) of the device has been characterised by using pulsed I–V measurement and a two-step calibration process. The R_{ON} of the device increases by rising the temperature of the device. The imaginary part of Y_{22} as a signature of traps on small-signal measurements was shown at different temperature levels. with traps responding at increasingly higher frequencies as the temperature increased. Moreover, during IDLTS measurements, transient I_{DS} of the device was determined, when V_{DS} of the device was pulsed from 20 V to 10 V and V_{GS} was constant all the time. Calculated Arrhenius equation based on Y_{22} and IDLTS measurements gave similar results putting the activation energy of the device traps at about 0.49 eV.

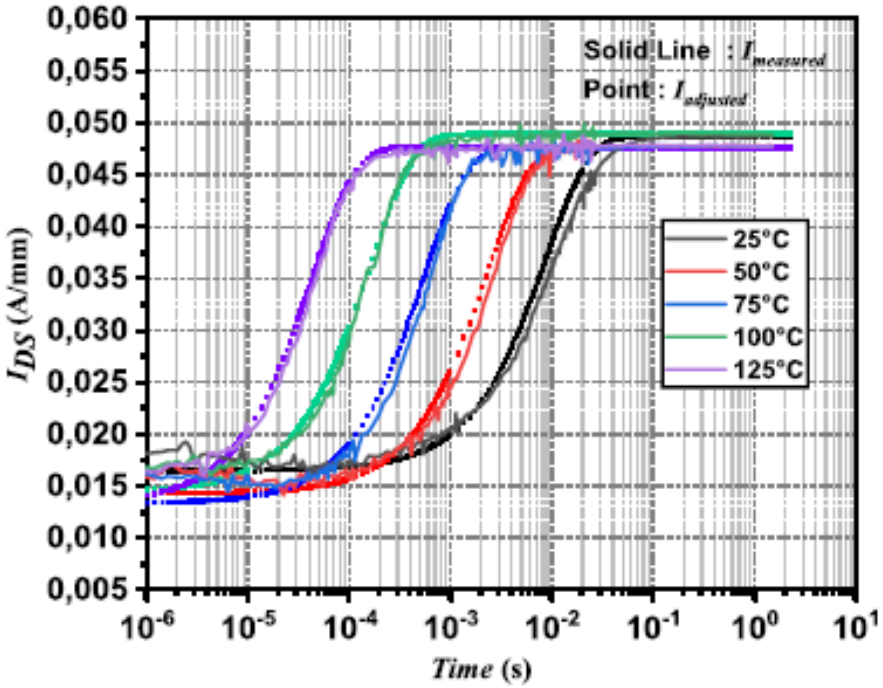

Figure 2-8: Transient drain current recovery related to the emission of traps for different T-chuck ranging between 25 °C and 125 °C for T-filling = 10 µs [38].

Large-signal measurements using an unequally spaced multitone (USMT) signal were also done in order to evaluate the performance of the GH15 transistor around the optimum load impedance in terms of efficiency.

Another technique to extract the trapping effect on the large signal behaviour of the device is utilising modulated signals with different bandwidths [32]. In [32] device was biased at typical class AB mode and two-tone stimulus with varying bandwidth was applied to the device and gain profile of the device was measured. Figure 2-10 shows the gain of the device at different bandwidths of the applied signal to the device and clarified when frequency difference is negligible. As it can be seen, the PA follows initially the typical class-AB gain trend and by applying signals with higher bandwidths, its behaviour changed to a class-C biased PA with a low gain at smaller drive levels. This observation was related to the drain-lag phenomena caused by traps

in the buffer or substrate layers of the PA. It was concluded the threshold voltage of the device was affected by the traps charging level of the device. The capture and emission process were shown in Figure 2-9 and modelled as an RC circuit with two different time constant for charging and discharging.

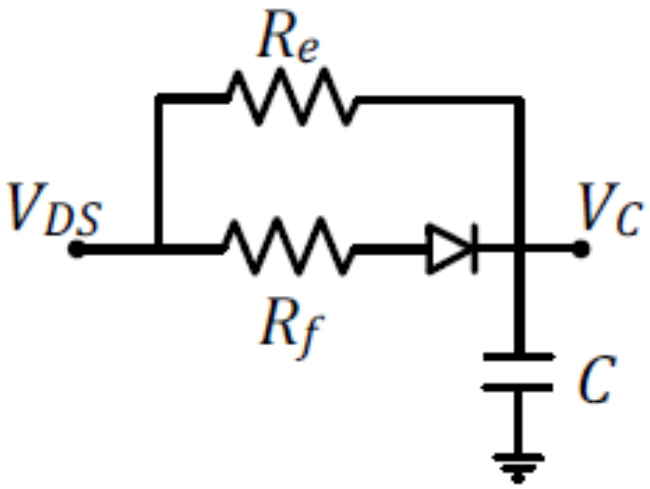

Figure 2-9:charging and discharging model of traps [32]

To extract the charging time constant of the traps, beside extracting two-tone gain profile, small-signal gain at different V_{GS} was determined and time constant of the traps for discharging process was calculated.

Measurements were performed at 900 MHz centre frequency with varying bandwidth from 5 Hz TO 50 kHz.

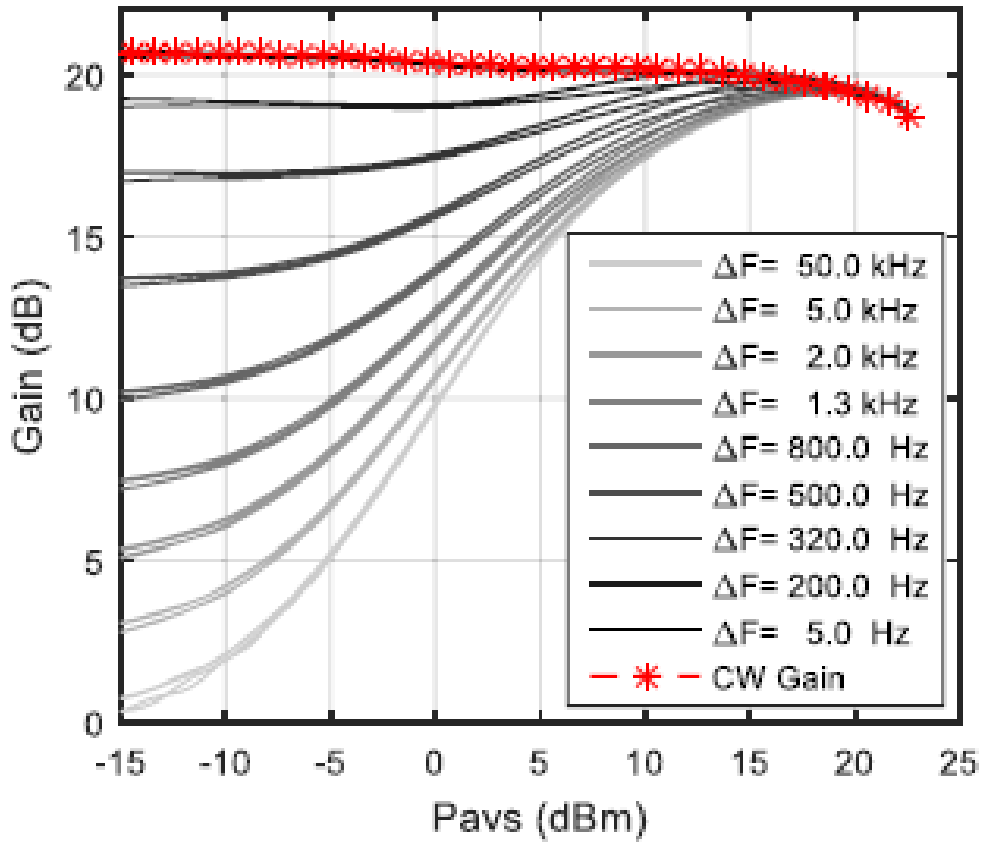

Figure 2-10: Two-tone measured dynamic gain characteristic of a GaN HEMT based PA for different frequency separations in comparison to its static CW gain [32], Pav is average power of two-tone signal.

In [31], pulsed LSNA measurements on the high power AlGaN/GaN transistors were performed in a multi-harmonic passive load-pull environment. Time-domain waveforms were recorded during a 150 ns window and measurement window was moved across the 20 μs duration of pulses. Duty cycle of the applied pulses was 2 % the period is 1 ms. A novel approach was conducted which was called Time-domain Approach (TDA). It was based on a progressive acquisition of all the required samples before sending them to FFT. In each pulse, a defined number of samples was stored and put together with precedent samples. The key point of this technique was to keep phase coherence between the samples to be put together (the last recorded sample of current pulse and first sample of up-coming pulse). Large-signal measurements performed at 2 GHz fundamental frequency and 6 harmonics of the device were

captured and all the applied DC and RF signals were in the pulsed mode. Gain of the device was measured within the pulse by pre-charging the traps of the device and applying various drain-lag levels to it. Reported data demonstrated, within pre-charged condition has produced lower output power in comparison with the condition which traps were not pre-charged. Furthermore, higher compression level, led to have more variation within the pulse, due to knee walkout phenomena, and the variation of the output power within the pulse, declined by applying pre-charging.

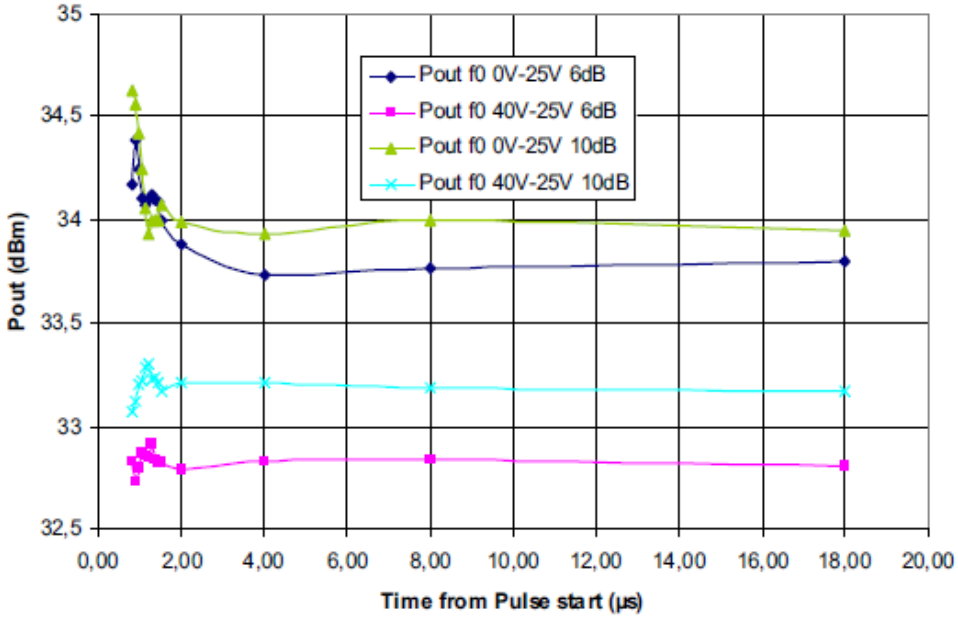

Figure 2-11: Output power of the device at different compression levels and pre-charging condition [31]

The authors of [39] focused on the importance of utilising RF characterisation techniques, in analysing the traps. They evaluated the applicability of pulsed I–V measurements as a tool for accurately extracting nonlinear GaN-based HFET models in [39]. Two different wafers with the identical layer structure but different growth conditions have been analysed and a series of I–V measurements was performed under DC and pulsed conditions expressing a dramatic difference in the kink effect and

current collapse (knee walkout) suggesting different trapping behaviours. However, in RF I–V waveform measurements, which was performed by utilising active harmonic load–pull to analyse the traps effect on RF performance metrics of the device, both wafers gave good overall RF performance with no significant difference observed. From PIV results, as a typical technique to analyse the traps effect on the device, it was expected, traps can degrade the RF performance of the devices. This absence of correlation between pulsed I–V measurement results and RF performance raised a question about the applicability of pulsed I–V measurements alone as an only tool for extracting nonlinear device models in the case of GaN HFETs, and importance of developing a system to characterise the effect of the trap on the different frequency ranges.

2.5.3 LINEARITY

Due to the nature of the pulse acquisition techniques, linearity investigation in the multi-tone stimulus condition is difficult as it requires advanced wideband instrumentation. Most of the pulse measurement instrumentation are narrow-band and not sufficient to perform pulse measurement device characterisation utilising narrow pulses. Such systems just keep the main centre frequency for device analyses. To investigate the device with multi-tone stimulus and extract the behaviour of the device at all main-tones and IMDs, wide-band acquisition is necessary, which is directly related to the maximum available bandwidth of the instrumentation and there is a trade-off between the length, driving the need for extensive memory use, of the pulses and maximum order of the IMDs that is intended to measure.

In [40], a technique was used to extract the IMD3 of the device under pulsed DC and RF signals to analyse the linearity of the high-power devices and trapping effect on

the linearity. Load-pull measurements were performed on a GaN device with 10 % duty cycle and 2 µs pulse width by using a pulsed VNA and multi-tone signal generator. A narrow-band filter with 500 Hz bandwidth was utilised to record the main frequencies (F_1, F_2) and IMD3 ($2f_1$-f_2, $2f_2$-f_1). Measurement was performed at 3 GHz centre frequency with 10 MHz tone spacing. The narrow-band filter was tuned at mentioned frequencies to separate the main spectral and IMD_3 of the output of the device, therefore from each pulse, recorded information at 4 different frequencies was achieved to calculate the $\left(\frac{C}{I}\right)_3$ [40]. The acquisition window can move within the pulse to record the device behaviour at different sections of the pulse, thus the linearity ($\left(\frac{C}{I}\right)_3$) of the device was analysed within the pulse. A technique was used to pre-charge the traps of the device before applying RF signals to it, therefore before biasing the device, traps could be charged during the "off" section of each pulse [40]. As reported, the linearity of the device decreases within the pulse by 7 dB and by applying gate-lag to the device the linearity variation within the pulse declines to 2 dB at the same drive level.

An innovative experimental method for microwave power devices linearity characterization, based on a carefully designed multi-tone signal, was presented in [41]. The generated test signal was based on an unequally spaced multi-tone (USMT) signal, which was tailored to mimic the OFDM signal's statistics. This technique is a useful method to generate commercial telecommunication signals without using complicated techniques to generate them. Multi-tone signal with unequal tone spacing was generated to give the same PDF of OFDM signals. 8-tone USMT signal was generated and applied to the 3 W GaN device with 2.4 MHz bandwidth. Output power, AM/AM, AM/PM and EVM of the device were achieved, at different load impedances

by performing active load-pull measurements with LSNA. Traps effect on the DC I_{DS} of the device was measured over a 30 dB output power dynamic range at different load impedances. Traps showed their signature at back-off levels at all load impedances and when the device was pre-charged at PB=(0 V, 2 V) under USMT applying signal for 20-40 s, the current collapse has been shown resulting from fast emitting traps.

2.5.4 MODELLING TRAPS

Modelling the traps is a prevalent tool to accurately design a PA that incorporates the trap behaviour. Most proposed models for the traps are based on circuit model to interpret the traps of the device. In [42], an accurate large-signal model for AlGaN-GaN HEMT was presented considering traps and self-heating effect on the device. This model was derived from a distributed small-signal model that efficiently describes the physics of the device. To model the dynamic behaviour of traps at the surface and buffer layer of the device, gate lag measurements at these PBs= (Pre-V_{GS}<$_{VPINCH-OFF}$, Pre-V_{DS}=0 V), (Pre-V_{GS}=0 V, Pre-V_{DS}=0 V), and drain lag measurements at PB= (Pre-V_{GS}<$V_{PINCH-OFF}$, Pre-V_{DS}>>0 V), (Pre-V_{GS}<$V_{PINCH-OFF}$, Pre-V_{DS}=0 V), have been performed and pulsed I-V results were used to model the traps. As shown in Figure *2-12* the series RC network was proposed in the gate and drain sides of the device to incorporate the traps effect into the large signal model of the device. The C_{GT}, C_{DT} were used to model the surface and buffer traps, respectively. These charges are controlled with $R_{GT,}$ R_{DT} that define the time constant of the charging traps [42].

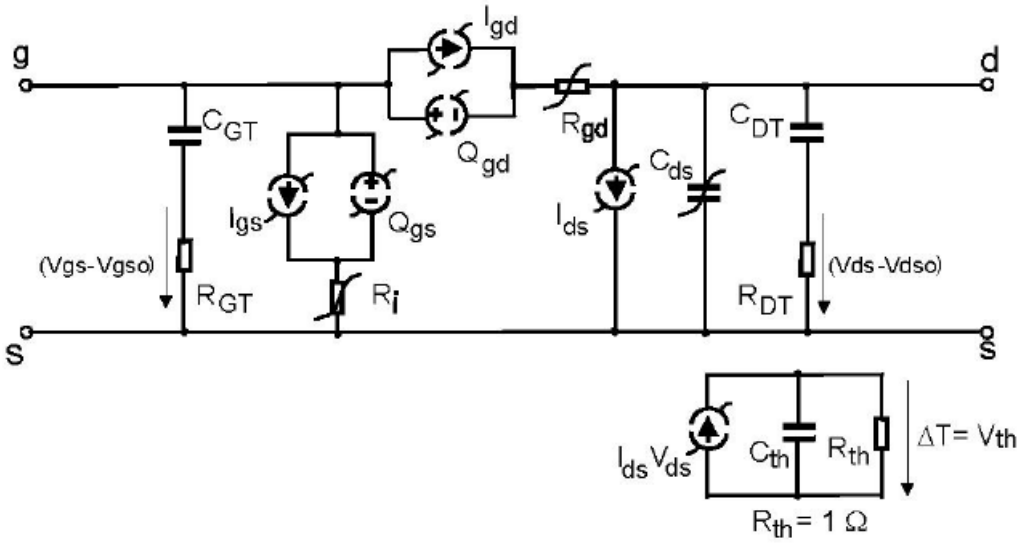

Figure 2-12: large signal model of device with considering traps of surface and buffer layer [42]

An improved drain current model accounts for trapping and self-heating effects was also implemented. The model showed very good results for simulating the high-power operation of the device, even beyond 1 dB gain compression.

In [43] a non-linear electro-thermal AlGaN/GaN model for CAD application was presented including a new additive thermal-trap model to take into account the dynamic behaviour of trap states and their associated temperature variation. The thermal-trap model was extracted through low-frequency small-signal CW S-parameter measurements and large-signal pulsed-RF measurements at different temperatures. The proposed thermal-trap model incorporated the drain-lag effect, since the gate-lag effect has been reduced by using device surface passivation and an addition of a field plate. It was shown traps of the device can affect the pinch-off voltage and to control the drain current source of HEMT, pinch-off voltage should be modified with physical exponential law. Figure 2-13 shows the proposed circuit to modify the $V_{PINCH-OFF}(t)$ which accounts for traps of the device within the buffer layer.

This model has taken into account the asymmetry of GaN device between trapping (capture) and de-trapping (emission) processes. In fact, capture time constant was found to be in the nano- to-microsecond range while extracted emission times were slower in the microsecond to seconds range. The authors have shown the output conductance frequency dispersion is very sensible to drain-lag of the device and by performing CW S -parameter measurements and extracting the imaginary part of Y_{22} in the frequency domain, the time constant of traps has been calculated. Moreover, thermal-trap model was achieved by considering bias drain current during the RF large-signal excitations with temperature variation. It was reported, a declining of the drain current immediately after applying RF signal and its variation after stopping RF excitation, is linked to the capturing and emission of traps of the device and it is sensitive to the temperature. They modelled the I_{DS} of the device as shown in (2-3)

$$I_{DS,FIT}(t) = I_{DS,FINAL} + \sum_{i}^{N} A_{TRAP\_I} \times e^{-\left(\frac{t}{\tau_i}\right)^{\beta_i}} \qquad (2\text{-}3)$$

Where A_{TRAP_I}, β_i, τ_i are the trap amplitude, stretching parameter, and time constant of the traps and N indicates the number of detected traps. Traps amplitude and stretching factor express the capture and emission level in the device. In the above model, the capture and emission of the traps were also considered, where the negative A_{TRAP_I} shows the emission phenomena. To validate the proposed model, output power and gain and PAE of the device with 25 dB dynamic range were compared to the measurement results, which showed a good match between them. They also have shown by increasing the temperature of the package, traps occur at higher frequencies.

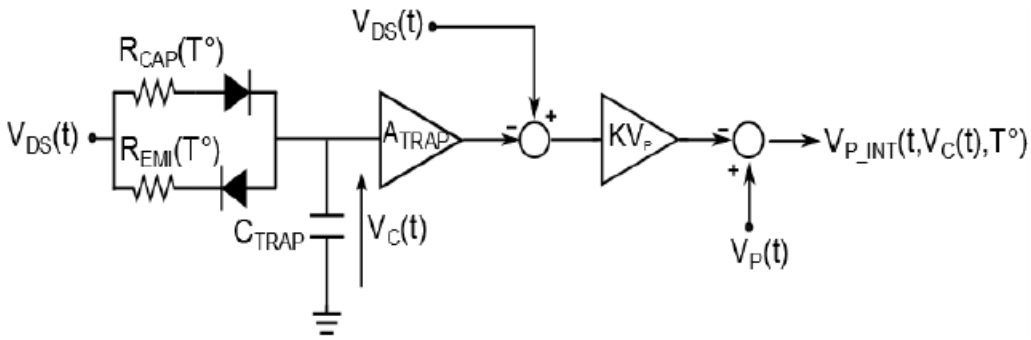

Figure 2-13: Schematic of the new thermal-trap model of a one charge-trapping state [43].

This thermal-trap model allows accurately predicting the physical temperature activation of traps and the thermal signature of traps. It was also achieved that extrapolation of trap model parameters by the stretched multi-exponential function of drain current results for significantly improved envelope simulations.

In [44], a large-signal model was developed for HJFET devices, based Shockley-Read-Hall (SRH). A parallel circuit consisting of a diode and a resistor was suggested to model the capture and emission process of traps which occur at increasing and decreasing V_{DS} levels, respectively. When the drain voltage rises rapidly, the back gate potential plunges following the change in drain voltage and some of the channel electrons are injected simultaneously into the substrate. Following the rapid change, the back gate potential slowly rises by capturing the injected electrons, and the current slowly declines. On the other hand, when the drain voltage falls rapidly, electrons are depleted at the first time slot of measurements and then, deep traps emit electrons and the current slowly increases. It was reported [44], that the required time to increase the current exponentially is about 1ms and when V_{DS} rises, the current gradually decreases over a wide range of time, from ps to ms.

Required data to verify and develop the SRH model can be obtained from an advance pulse measurement system, thus as an application of developed measurement system, in this thesis can be used to provide a SRH model for PAs.

2.6 CARDIFF BEHAVIOURAL MODEL

Cardiff nonlinear behavioural model was firstly established in [45, 46] to predict the device behaviour and provide a CAD-based model for it. It was a development on the look-up table-based model [47] which failed to cover the design measurement space. The Cardiff behavioural model was utilising a formulation that is based on the poly-harmonic distortion approach.

In [47], utilisation of large-signal measurement data in the nonlinear CAD-based modelling was provided, measured nonlinear data was, in the first instance, directly integrated into a nonlinear CAD simulator, and in the second instance, operated for direct extraction of behavioural model parameters. A typical two-port network was considered and the formulation of a-wave based Cardiff model has been achieved, which models the reflected waves of input and output of the device (b_1, b_2) in terms of incident waves (a_1,a_2) during the active load-pull measurements.

In [48] a new technique for identifying the mixing structure, model coefficients of the Cardiff behavioural model for phase-related nonlinearities was proposed. A two-tone excitation was applied to the device and by taking FFT the IMDs of the device have been investigated. Spectral tone visibility explicitly required accurate model coefficients (NMSE < -40dB) for data fitting, which was verified by comparing the model fit for full and truncated model formulations. An a-based model was investigated by applying two-tone stimulus to the device and the second tone's ($a_{21,2}$)

power level varied from -6 dBc to 6 dBc. Based on spectra of the output envelope for the b_{21E} (envelope of reflected waveform of second port at fundamental) signal, required formulation of Cardiff model was exploited consisting of a relative phase polynomial equation for a constant $|a_{21}|$. The equivalent X-parameter formulation has been shown to remain accurate up to $a_{21,2}$=2 dBc. However, the higher order Cardiff model achieved higher accuracy achieving device errors of less than -40 dB NMSE for $a_{21,2}$ variations up to 6 dBc when using an 11^{th} order Cardiff model.

A data analysis approach was introduced in [49] to identify the required model order and directly extract the model coefficients. It was based on operating multi-tone measurements and applying the time-variant multi-tone signal to the load side ($a_{2,1}(t)$). By applying a tailored time-variant multi-tone signal to the device and mapping the Cardiff model equation onto the frequency-domain using FFT a direct relationship between the measured $b_{2,1E}(t)$ spectra and the model parameters was demonstrated, hence allowing to use the measured envelop to directly identify the model parameters. Furthermore, by analysing the spectra of $b_{2,1E}(t)$ above the noise level, it was possible to identify the order of the Cardiff model.

In [50] a technique was proposed to reduce the number of load-pull measurements that are required to achieve the high-density Cardiff model coefficients look-up table, versus input drive level. Coefficients were interpolated to predict the load-pull behaviour of the device over 2-4 dB dynamic range. This technique allowed to rapidly extract the model. Again, an a-wave based model was employed for this investigation. As the Cardiff model coefficients are dependent on the input drive level ($|a_{1,1}|$) is necessary to perform load-pull measurements at different input drive levels for the

extraction of a more comprehensive Cardiff model. However, in [51] the relation of the coefficients and $|a_{1,1}|$ was confirmed as

$$K_{p,q} = \sum_{T=0}^{\infty} L_{p,q} \times (|a1,1|)^{1+q-2T} \quad (2\text{-}4)$$

where T indicates the mixing order and the p and q parameters the input and output port, respectively. To reduce the density of power measurements, an advanced global Cardiff model formulation has been used during model coefficient extraction to allow for accurate interpolation of the model coefficients within a defined power range using a global model formulation by keeping T<2. As a consequence, it was possible to populate a high-density look-up table without the need for a high-density measurement grid.

In [52] a load-based behavioural model was presented, that indicated the b_{21} is a function of the load reflection coefficients. It allowed to automatically extract the model coefficients in a time-efficient manner and the appropriate load-pull impedance space for a DUT. To reduce the number of active load-pull measurements a strategy was proposed based on tracking the maximum output power of each successive measurements, to find the optimum impedance of the device. The first cycle of measurements has been performed around centre of Smith chart and achieved data was managed to extract the load-based model which was used in the next measurement cycle to compute an array of targeted load-pull values (load side reflection coefficients), thus required a_{21} was calculated. This approach was automatically iterated to find the optimum impedance of the device by minimising the time-consuming active load-pull measurements to scope the unnecessary parts of Smith-chart.

2.7 CHAPTER SUMMARY

This chapter discussed the evolution of the pulsed RF characterisation instruments, which can examine the high power amplifiers' large-signal behaviour. Moreover, some techniques adaptable to LSNAs have been introduced.

The development of pulse measurement systems provides for the analysis of the trapping effect. Thus, an overview of the identification methods of traps was provided, and their effect on the large-signal performance metrics of the PA such as gain, linearity has been listed. The reported capturing and emission time constants of PA cover a large range from few microseconds to hundreds of milliseconds. Moreover, it was stated that large signal and small signals time constants are different.

Moreover, a summary of achievements of Cardiff behavioural model was mentioned as the developed measurement system can directly extract required data sets for the generation of behavioural models and can have wide range of applications in modelling.

2.8 REFERENCE

[1] J.-P. Teyssier, M. Campovecchio, C. Sommet, J. Portilla, and R. Quéré, "A pulsed S-parameters measurement setup for the non-linear characterization of FETs and bipolar power transistors," in *1993 23rd European Microwave Conference*, 1993: IEEE, pp. 489-493.

[2] S. Ahmed, M. S. El Dine, T. Reveyrand, G. Neveux, D. Barataud, and J.-M. Nebus, "Time-domain measurement system using Track & Hold Amplifier applied to pulsed RF characterization of high power GaN devices," in *2011 IEEE MTT-S International Microwave Symposium*, 2011: IEEE, pp. 1-4.

[3] M. Marchetti, K. Buisman, M. Pelk, L. Smith, and L. De Vreede, "A low-cost pulsed RF & IV measurement setup for isothermal device characterization," in *2007 70th ARFTG Microwave Measurement Conference (ARFTG)*, 2007: IEEE, pp. 1-4.

[4] Y. Tateno, Y. Kurachi, H. Yamamoto, and T. Nakabayashi, "Investigation of the pulsed-IV degradation mechanism of GaN-HEMT under high temperature storage tests," in *2018 IEEE International Reliability Physics Symposium (IRPS)*, 2018: IEEE, pp. P-WB. 2-1-P-WB. 2-5.

[5] M. Khan, W. Qian, D. Huang, L. Li, and F. Lin, "Enhanced GaN HEMT large-signal model with self-heating and trapping effects for power amplifier design," in *2015 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, 2015: IEEE, pp. 1-3.

[6] A. Huang, Z. Zhong, Y. Guo, and W. Wu, "Fast model generation for AlGaN/GaN HEMTs with the consideration of self-heating and charge trapping effects," in *2016 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, 2016: IEEE, pp. 1-3.

[7] A. Olomo, "Nonlinear GaAs pHEMT model with trapping effect for small signal and dynamic large signal design," in *2016 11th European Microwave Integrated Circuits Conference (EuMIC)*, 2016: IEEE, pp. 345-348.

[8] "Keysight Technologies Pulsed-RF S-Parameter Measurements with the PNA Microwave Network Analyzers Using Wideband and Narrowband Detection," Keysight Technologies, 2014.

[9] "Accurate Pulsed Measurements with the PNA Microwave Network Analyzers," Keysight Technolgies, 2014.

[10] "RF Pulse Measurements in time and frequency domains with VSE-K6," Rohde&Schwarz, 2016.

[11] "Pulse measurements," Anritsu, 2013.

[12] S. J. Doo *et al.*, "Adaptive second harmonic active load for pulsed-IV/RF class-B operation," in *2007 70th ARFTG Microwave Measurement Conference (ARFTG)*, 2007: IEEE, pp. 1-5.

[13] F. De Groote *et al.*, "Pulsed multi-tone measurements for time domain load pull characterizations of power transistors," in *2009 73rd ARFTG Microwave Measurement Conference*, 2009: IEEE, pp. 1-4.

[14] F. Zhou, J.-Z. Liu, Z. Ma, Y.-X. Chen, and K. Cheng, "An RF pulse measuring method non-dependent on envelope detector," in *2016 IEEE International Conference on Microwave and Millimeter Wave Technology (ICMMT)*, 2016, vol. 1: IEEE, pp. 245-247.

[15] P. Poire, D.-L. Le, and F. Ghannouchi, "A PC controlled fully automatic active load-pull measurement system using a pseudo-gradient algorithm," in *Proceedings of 1995 IEEE Instrumentation and Measurement Technology Conference-IMTC'95*, 1995: IEEE, p. 628.

[16] F. M. Ghannouchi, *Load-Pull Techniques with Applications to Power Amplifier Design*. Springer, 2013.

[17] C. Arnaud, D. Basataud, J. Nebus, J. Teyssier, J. Villotte, and D. Floriot, "An active pulsed RF and pulsed DC load-pull system for the characterization of HBT power amplifiers used in coherent radar and communication systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2625-2629, 2000.

[18] D. Siriex, O. Noblanc, D. Barataud, E. Chartier, C. Brylinski, and R. Quéré, "A CAD-oriented nonlinear model of SiC MESFET based on pulsed I (V), pulsed S-parameter measurements," *IEEE Transactions on Electron Devices*, vol. 46, no. 3, pp. 580-584, 1999.

[19] J. Teyssier, S. Augaudy, D. Barataud, J. Nébus, and R. Quéré, "Large-signal time domain characterization of microwave transistors under RF pulsed conditions," in *57th ARFTG Conference Digest*, 2001, vol. 39: IEEE, pp. 1-4.

[20] F. De Groote, O. Jardel, T. Reveyrand, J.-P. Teyssier, and R. Quéré, "Very small duty cycles for pulsed time domain transistor characterization," *Proceedings of the European Microwave Association Vol*, vol. 112, p. 117, 2008.

[21] M. Casbon and P. J. Tasker, "Comparison of sampler and VNA based Large Signal Measurement Systems (LSNA) under CW and pulsed operation," in *2015 85th Microwave Measurement Conference (ARFTG)*, 2015: IEEE, pp. 1-3.

[22] A. Aldoumani, P. J. Tasker, R. Saini, J. Bell, T. Williams, and J. Lees, "Operation and calibration of VNA-based large signal RF IV waveform measurements system

without using a harmonic phase reference standard," in *81st ARFTG microwave measurement conference*, 2013: IEEE, pp. 1-4.

[23] J. B. Lai and C. G. Christodoulou, "A very high sensitivity RF pulse profile measurement system," *IEEE Transactions on Instrumentation and Measurement*, vol. 59, no. 6, pp. 1616-1623, 2009.

[24] T. Gasseling *et al.*, "Large signal pulsed RF and DC load pull characterization of high voltage 10W GaAs-GaInP HBTs," in *IEEE MTT-S International Microwave Symposium Digest, 2003*, 2003, vol. 3: IEEE, pp. 1651-1654.

[25] T. Tsuchiya, "Trapped-electron and generated interface-trap effects in hot-electron-induced MOSFET degradation," *IEEE transactions on electron devices*, vol. 34, no. 11, pp. 2291-2296, 1987.

[26] K. Horio, A. Wakabayashi, and T. Yamada, "Analysis of surface-state effects on gate-lag phenomena in recessed-gate and buried-gate GaAs MESFETs," in *Proceedings of the 1999 7th International Symposium on the Physical and Failure Analysis of Integrated Circuits (Cat. No. 99TH8394)*, 1999: IEEE, pp. 191-194.

[27] A. Gautier-Levine, P. Audren, G. Post, M. Favennec, and J. Dumas, "A study of trap related drain lag effects in InP HFETs," in *Proceedings of 8th International Conference on Indium Phosphide and Related Materials*, 1996: IEEE, pp. 670-673.

[28] Y. Alimohammadi *et al.*, "Pulse Profiling Active Load Pull Measurements," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020: IEEE, pp. 759-762.

[29] A. Santarelli *et al.*, "A double-pulse technique for the dynamic I/V characterization of GaN FETs," *IEEE microwave and wireless components letters*, vol. 24, no. 2, pp. 132-134, 2013.

[30] G. P. Gibiino *et al.*, "Double-pulse characterization of GaN-on-Sapphire FETs for technology development," in *2016 21st International Conference on Microwave, Radar and Wireless Communications (MIKON)*, 2016: IEEE, pp. 1-4.

[31] J. Faraj, F. De Groote, J.-P. Teyssier, J. Verspecht, R. Quéré, and R. Aubry, "Pulse profiling for AlGaN/GaN HEMTs large signal characterizations," in *2008 38th European Microwave Conference*, 2008: IEEE, pp. 757-760.

[32] L. C. Nunes, J. L. Gomes, P. M. Cabral, and J. C. Pedro, "A simple method to extract trapping time constants of GaN HEMTs," in *2018 IEEE/MTT-S International Microwave Symposium-IMS*, 2018: IEEE, pp. 716-719.

[33] J. M. Tirado, J. L. Sanchez-Rojas, and J. I. Izpura, "Trapping effects in the transient response of AlGaN/GaN HEMT devices," *IEEE Transactions on Electron Devices*, vol. 54, no. 3, pp. 410-417, 2007.

[34] A. Benvegnù *et al.*, "Trap characterization of AlGaN/GaN HEMTs through drain current measurements under pulsed-RF large-signal excitation," in *2015 IEEE MTT-S International Microwave Symposium*, 2015: IEEE, pp. 1-4.

[35] J. L. Gomes, L. C. Nunes, and J. C. Pedro, "Explaining the Different Time Constants Extracted from Low Frequency Y 22 and $ I_ {DS} $-DLTS on GaN HEMTs," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020: IEEE, pp. 432-435.

[36] J. Couvidat *et al.*, "Investigation of fast and slow charge trapping mechanisms of GaN/A1GaN HEMTs through pulsed IV measurements and the associated new trap model," in *2018 IEEE/MTT-S International Microwave Symposium-IMS*, 2018: IEEE, pp. 720-723.

[37] P. M. Tomé, F. M. Barradas, L. C. Nunes, J. L. Gomes, T. R. Cunha, and J. C. Pedro, "A transient two-tone RF method for the characterization of electron trapping capture and emission dynamics in GaN HEMTs," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020: IEEE, pp. 428-431.

[38] M. Bouslama *et al.*, "Dynamic Performance and Characterization of Traps Using Different Measurements Techniques for the New AlGaN/GaN HEMT of 0.15-$\mu $ m Ultrashort Gate Length," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 2475-2482, 2019.

[39] H. Hirshy *et al.*, "Evaluation of pulsed I–V analysis as validation tool of nonlinear RF models of GaN-based HFETs," *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5307-5313, 2018.

[40] H. Bousbia, D. Barataud, G. Neveux, T. Gasseling, J.-M. Nebus, and J.-P. Teyssier, "A novel load-pull setup allowing the intermodulation measurement of power transistors under pulsed DC and pulsed RF conditions," in *2006 IEEE MTT-S International Microwave Symposium Digest*, 2006: IEEE, pp. 1452-1455.

[41] V. Gillet, M. Bouslama, J.-P. Teyssier, M. Prigent, J.-C. Nallatamby, and R. Quéré, "An unequally spaced multi-tone load–pull characterization technique for simultaneous linearity and efficiency assessment of RF power devices," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 2505-2513, 2019.

[42] A. Jarndal, B. Bunz, and G. Kompa, "Accurate large-signal modeling of AlGaN-GaN HEMT including trapping and self-heating induced dispersion," in *2006 IEEE International Symposium on Power Semiconductor Devices and IC's*, 2006: IEEE, pp. 1-4.

[43] A. Benvegnù *et al.*, "Non-linear electro-thermal AlGaN/GaN model including large-signal dynamic thermal-trapping effects," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, 2016: IEEE, pp. 1-4.

[44] K. Kunihiro and Y. Ohno, "A large-signal equivalent circuit model for substrate-induced drain-lag phenomena in HJFETs," *IEEE Transactions on electron devices*, vol. 43, no. 9, pp. 1336-1342, 1996.

[45] M. Koh *et al.*, "X-band MMIC scalable large signal model based on unit cell behavioral data model and passive embedding network," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, 2013: IEEE, pp. 1-4.

[46] S. Woodington *et al.*, "A novel measurement based method enabling rapid extraction of a RF waveform look-up table based behavioral model," in *2008 IEEE MTT-S International Microwave Symposium Digest*, 2008: IEEE, pp. 1453-1456.

[47] H. Qi, J. Benedikt, and P. J. Tasker, "Nonlinear data utilization: From direct data lookup to behavioral modeling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 6, pp. 1425-1432, 2009.

[48] A. Al-Rawachy, T. Husseini, J. Benedikt, P. Tasker, and J. Bell, "Cardiff behavioural model analysis using a two-tone stimulus," in *2019 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, 2019: IEEE, pp. 1-4.

[49] A. Al-Rawachy, T. Husseini, J. Benedikt, J. Bell, and P. Tasker, "Behavioural Model Extraction using Novel Multitone Active Load-pull," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019: IEEE, pp. 196-199.

[50] T. Husseini, A. Al-Rawachy, J. Benedikt, J. Bell, and P. Tasker, "Global Behavioural Model Generation Using Coefficients Interpolation," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019: IEEE, pp. 200-203.

[51] M. R. Moure, M. Casbon, M. Fernández-Barciela, and P. J. Tasker, "Direct extraction of an admittance domain behavioral model from large-signal load-pull measurements," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, 2017: IEEE, pp. 1057-1060.

[52] T. Husseini, A. Al-Rawachy, S. S. Anera, J. Bell, P. Tasker, and J. Benedikt, "On the effective modeling of the test-set non-linearity," in *2018 91st ARFTG Microwave Measurement Conference (ARFTG)*, 2018: IEEE, pp. 1-4.

CHAPTER 3: MEASUREMENT SYSTEM SETUP

3.1 INTRODUCTION

Development of an adaptable and manageable high-speed measurement system that can deal with wide bandwidth at a high-power regime is the first step and a paramount factor to precisely characterise 5G power amplifiers and provide the opportunity to expand a user-defined RF measurement system. A robust measurement system should provide an opportunity to simply and comprehensively characterise the different performance metrics of PA. Thus, a fast, and memory-efficient measurement system would be useful to conduct several time-consuming measurements with a large amount of recorded data within a short time. Meanwhile, such a measurement system can easily perform different types of measurements and separately characterise various phenomena such as trapping, thermal and self-heating effect on DC and fundamental frequency of the device. As traditional measurement systems are extremely expensive, complex, rigid which is in contrast with the upcoming RF applications, designing a software-defined measurement system that is based on controllable signal transceivers, leads to overcome the mentioned negative points of the RF measurement systems and boost RF technologies to straightforwardly perform different types of measurements without expensive amendments.

The aforementioned requirements can be achieved by utilising a new generation of instruments such as NI (National Instruments) modules, which allow for the development of a customizable and re-configurable system that can be easily upgraded while maintaining the required synchronization and desired measurement flow.

Moreover, as these measurement systems are based on multi-core processors, they can perform time-consuming measurements and analyse data rapidly. Programmable IQ-based signal transceivers allow tailoring the generated RF signals to perform measurements in different conditions such as pulsed CW, pulsed multi-tone, and also provide an opportunity to characterise the device under different shapes of RF stimulus. Implementing a robust pulse measurement setup to meticulously characterise the high-power PAs is one of the interesting aspects of using the PXIe vector signal transceiver (VST). Wide bandwidth, high sampling rate, and high accuracy of signal transceivers are remarkable features of the VST system that provide an opportunity to characterise the PA under short pulse stimuli. Moreover, by employing advanced PXIe source measurement units (SMUs) that can provide pulsed DC signal, different terms of memory effect on the PA's performance can be analysed and it allows to investigate the trapping and self-heating effect on the large-signal behaviour of the device and their impact on nonlinear behavioural model coefficients and load-pull contours. Consequently, developing a PXIe based measurement system allows to swiftly characterise a larger number of performance metrics of PAs.

Besides providing the RF and DC generator and analyser of the measurement system, a trustworthy RF test-set is urgently required to be able to accurately measure the high-power device over a wide bandwidth. To measure the high-power devices, the designed test set should have sufficient maximum power. Moreover, in high power devices, the level of the output's harmonics and baseband frequencies are high, thus if the designed test-set cannot provide significant isolation between different frequency ranges, the measured behaviour of the device will not be precise. Hence, a robust test-set with a high isolation factor between signal paths should be designed.

This chapter introduces developments of a novel measurement system architecture that is based on commercially available PXIe modules, to characterise the large-signal behaviour of the device under various conditions such as pulsed CW, pulsed multi-tone, and pulse profiling measurements. Then, the structure and features of the RF and DC PXIe modules are explained and some of their important features are pointed out. Pulse measurement capability as a key implementation that is added to the system is explained in detail and employed technique, in RF generator to apply synchronised DC and RF pulses and keep the one-to-one relation between generated and recorded pulses is clarified. Then, different pulse measurement acquisition technique is mentioned and utilised technique with its verification is revealed. Some performance metrics of designed pulse measurements such as memory usage level, pulse-to-pulse stability, DC and RF pulses' transient time, and narrow pulse accuracy are shown.

Applied calibrations on the receivers' recorded data are also mentioned and different small and large signal standards are presented to verify the accuracy of the measurement. The dynamic range, noise floor, standard deviation of the measurement system, are investigated to measure the limitations of the system. Finally designed RF test set to perform active load-pull measurements over a wide frequency range with high instantaneous bandwidth is described and some of the critical features of the passive components of the test set are mentioned.

3.2 MEASUREMENT SYSTEM ARCHITECTURE AND ITS KEY COMPONENTS

The system architecture is configured around PXIe modules [1] with an architecture similar to previously published non-linear measurement systems that are based on an

NVNA [2]. The PXIe modules do not share a common RF reference signal and are synchronised through the available programmatic backplane implementation of triggering signals, and sample-level alignment.

In contrast to previously realised measurement systems, RF instrument modules are based on IQ-architecture similar to software-defined transmitters and receivers that are utilised for the understanding of modern communication systems. Consequently, the realised measurement system shares a commonality with a wireless transceiver with a shared synchronisation channel.

Figure 3-1 shows the block diagram of the developed measurement system. All NI modules are located in a single PXIe-1085 chassis [3] and controlled by a multi-core processor PXIe-8880 controller [4]. It consists of 5 Vector Signal Analysers (VSAs) and Vector Signal Generators (VSGs). In this configuration a VSA-VSG pair is contained within a single Vector Signal Transceiver (VST); NI-PXIe 5840 [5]. VSTs are IQ-based software-defined signal transceivers, allow user to set and control all key settings of receivers and generators. Two VSTs provide fundamental input and output stimulus of the device with 1 GHz bandwidth. Once the applied signal to the device has 1 GHz fundamental bandwidth, the device generates second harmonic with 2 GHz instantaneous bandwidth, thus two VSTs are allocated to the 2^{nd} harmonic and another VST applies the baseband stimulus to the load side of the device, to perform harmonic and baseband load-pull measurements. Moreover, an RF signal generator (PXIe-5652) [6] with a known phase output power amplifier has been assigned for generating the phase reference standard signal.

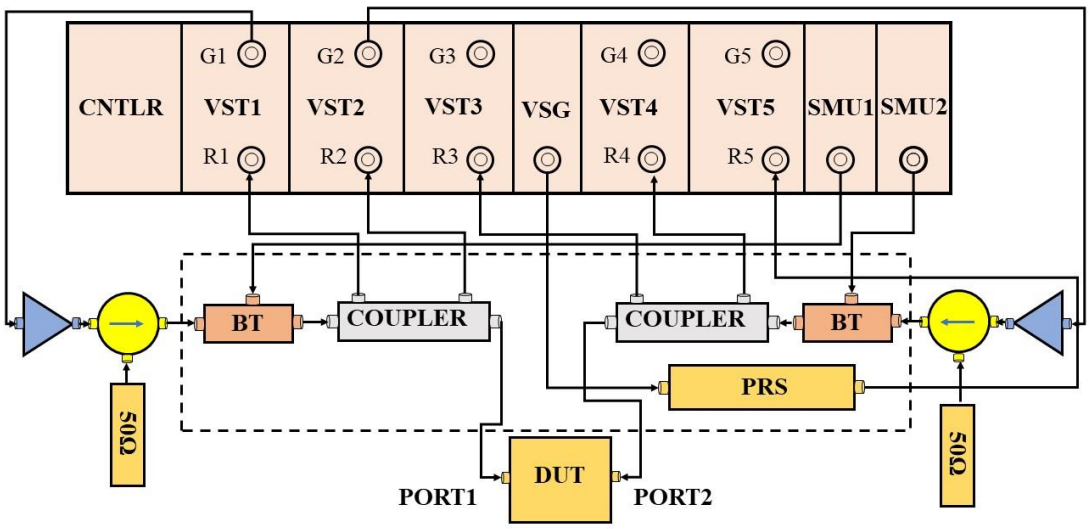

Figure 3-1: schematic of measurement system

In the acquisition side, 4 VSTs are occupied to measure incidents $a_{p,h}$ and reflected $b_{p,h}$ power waves of the device to allow time-domain measurements, and one VST is utilised as a reference receiver extracting the phase relation between harmonics from Phase Reference Standard (PRS). In order to apply the DC bias signals to the device and measure the DC voltages and currents at input and output of the device, two Source Measurement Units (SMUs) PXIe-4139 are employed [7].

Figure 3-2 illustrates the configuration of the local oscillator (LO) of VST. Each VST has an internal LO on the transmitter and receiver side, they also can share the LO in receiver and transmitter ports separately with other VSTs. On the generator side of the VSTs, internal LO is utilised for each VST and on the receiver side, the master-slave method is utilised and the LO of the first receiver is shared with other receivers by using MMPX cables to maximise phase stability between the receivers' data.

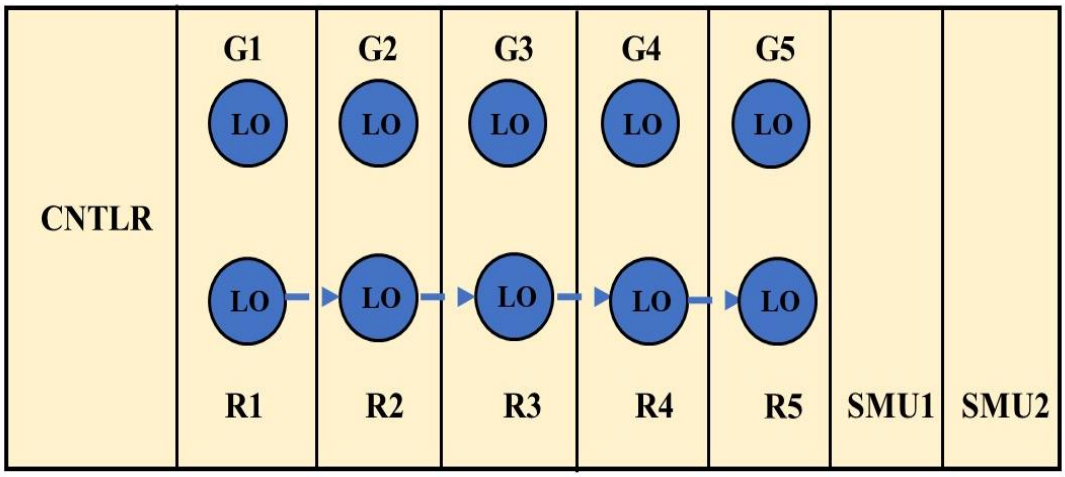

Figure 3-2: Sharing the LO at receiver of VSTs

3.2.1 RF TEST-SET

A passive test- set is designed and assembled to reach the unique features of the project to perform active load-pull measurements over a wide frequency range. To design the test set, the frequency range of fundamental frequency, instantaneous bandwidth, desired harmonics, the power range of the device are key factors are considered.

Based on the desired aims of the project, fundamental frequency (F_0) is 1.8-2.8 GHz with 1 GHz bandwidth. Due to the nonlinear nature of the measurement system, the required components should also cover the frequency ranges for IF (intermediate frequency) and the second harmonic ($2F_0$). Furthermore, the two different power levels are considered during the designing of the test-set. According to project specifications, the frequency ranges are as follows:

- IF frequency is from 200MHz-1GHz,
- Fundamental (F_0) is from 1.8GHz-2.8GHz.
- Second harmonic ($2F_0$) is from 3.6 GHz-5.6GHz.

The maximum power in different measurements are listed below:

- Maximum power at CW condition is 10 Watt
- Maximum power at Pulse condition is 100 Watt

Designed RF test-set can deal with high power devices and perform active load-pull measurements over a wide range of frequencies.

Figure 3-3 illustrates the inner architecture of the test set. The DUT is connected to two-directional couplers which can cover 200 MHz-18+ GHz, therefore, it allows measuring the different frequency ranges simultaneously.

These couplers are connected to four VSTs receiver side. After that, there is a diplexer (consisting of a 90-degree hybrid coupler with a frequency range of 1-6+ GHz & 3GHz low pass filter), which is shown in Figure 3-4, since the low pass filter doesn't allow frequencies more than 3 GHz to go through the diplexer, higher harmonics of the device appear in port 4 of diplexer (isolated port). Fundamental and IF frequencies go through the diplexer and 90-degree hybrid couplers separate the frequencies less and more than 1 GHz and deliver them to port 3 and 2 of the then, by using the bias T, IF frequencies can be separated from DC. The bias T in the load side can deal with up to 100 W peak power and it has a high DC current limitation, and it can separate the frequency with cut-off frequency at 100 MHz.

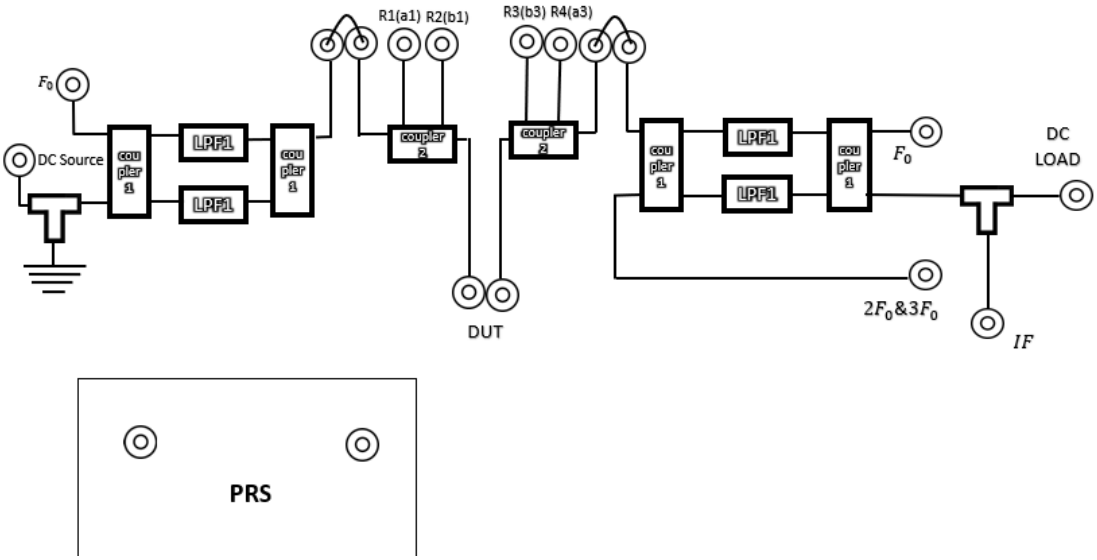

Figure 3-3: Schematic of inner view of test-set to perform load-pull measurements.

Figure 3-4: Diplexer, including low pass filters and hybrid couplers

Figure 3-5 and Figure 3-6 present the test-set and whole measurement system's modules including PRS, drive power amplifiers, and test-set. As can be seen to minimise the loss in the test-set, all components are connected together without cables. Minimising the power loss in system, can be useful to characterise PAs in higher frequency ranges, as in these frequency ranges system should be efficient in terms of power loss.

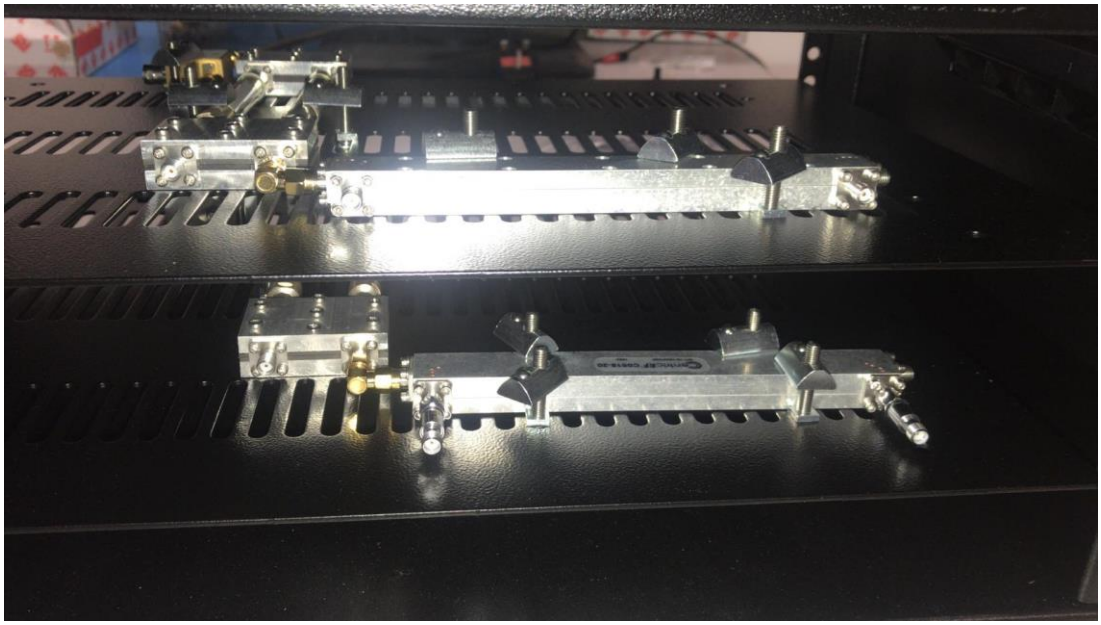

Figure 3-5:Test-set and its passive components including: directional couplers, 90 degree hybrid couplers, low pass filter, bias Ts.

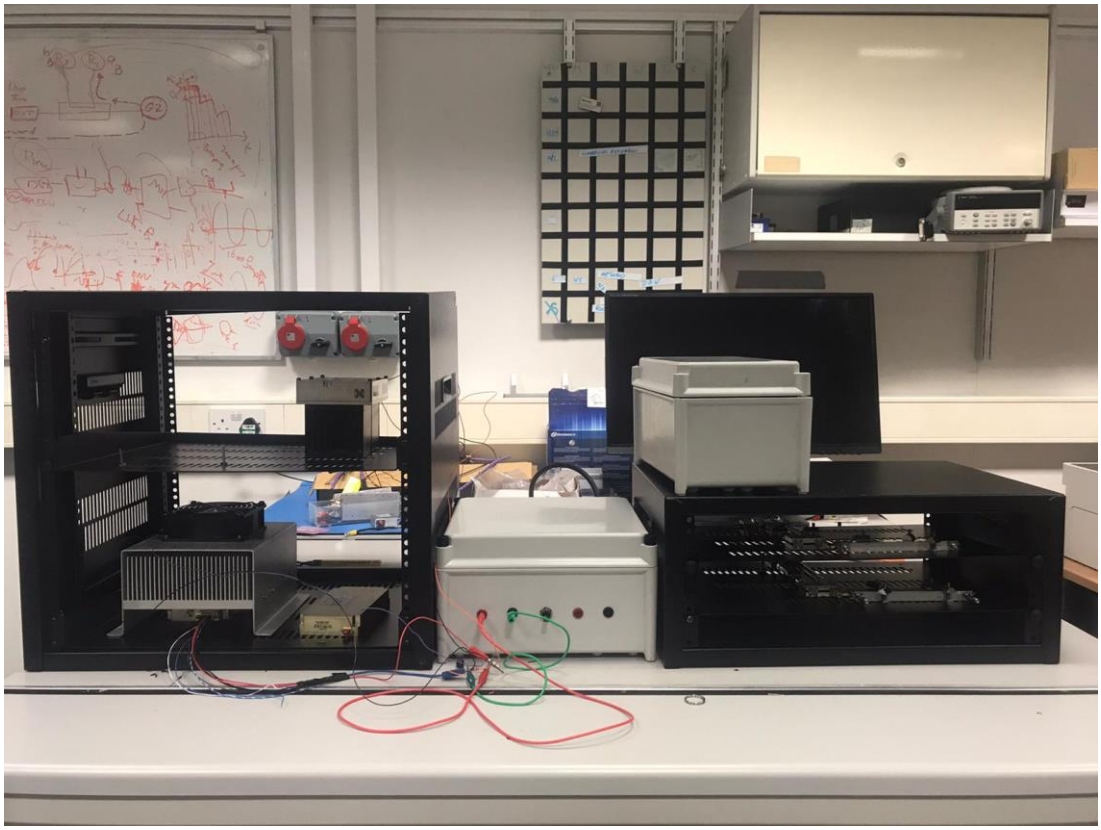

Figure 3-6 : different parts of operating measurement system including PAs, test-set, PRS

S-parameter measurements are conducted by using an NVNA, to characterise and verify the test-set. Figure 3-7 shows test-set's s-parameters at IF port. In this measurement port 1 is the input port of the test-set and port 2 is IF port at the load side. As it shown, IF port passes the frequencies from 200 MHz-1 GHz with 0.382 to 2.52 dB degradation. Higher frequencies have significantly degraded in this port which shows there is high isolation between IF bandwidth and fundamental frequency.

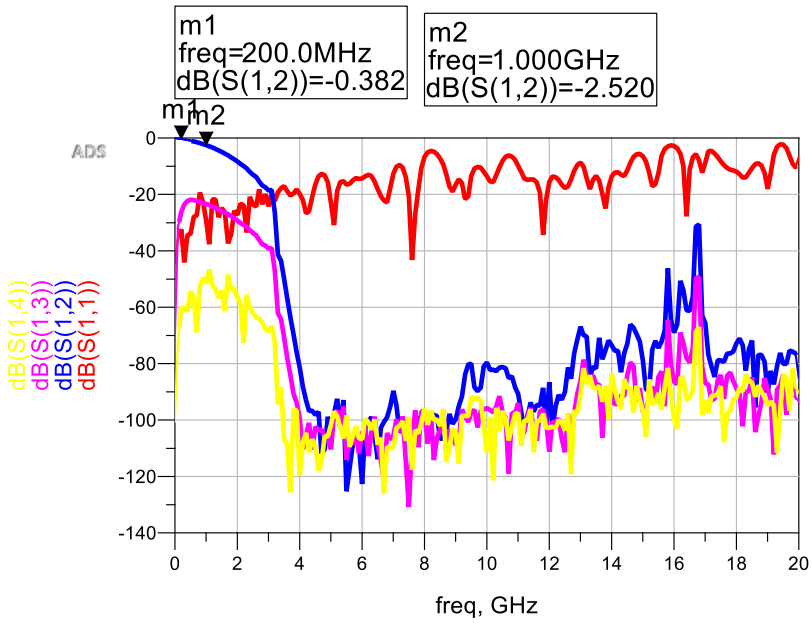

Figure 3-7: Measured s-parameter of the test-set between input and IF port.

Figure 3-8 shows the S-parameter of the fundamental port at the load side, this port is designed to pass frequencies between 1.8-2.8 GHz. As can be seen it provides 20 dB isolation from reflected waveform ($S_{1,1}$). Figure 3-9 also shows the performance of the source fundamental port, which has the similar response to the load side port.

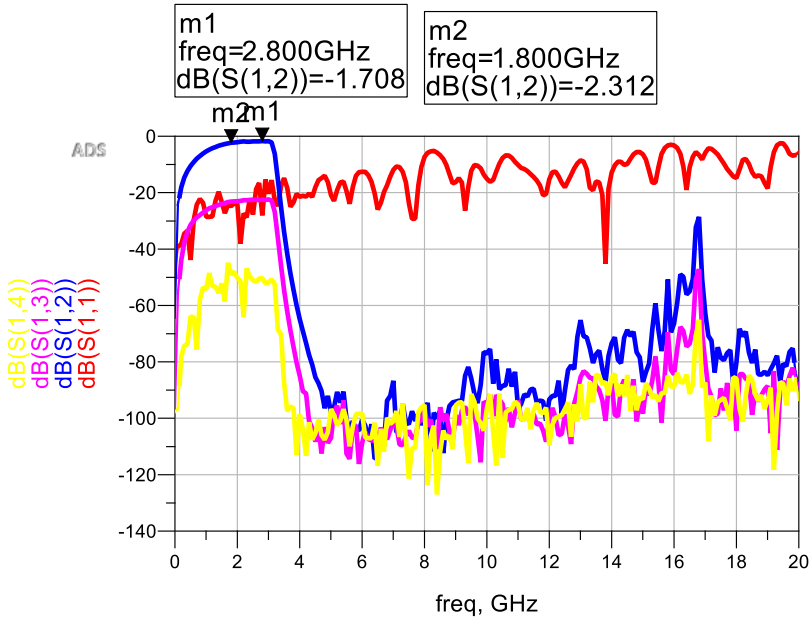

Figure 3-8: Measured s-parameter of test-set at fundamental load side port.

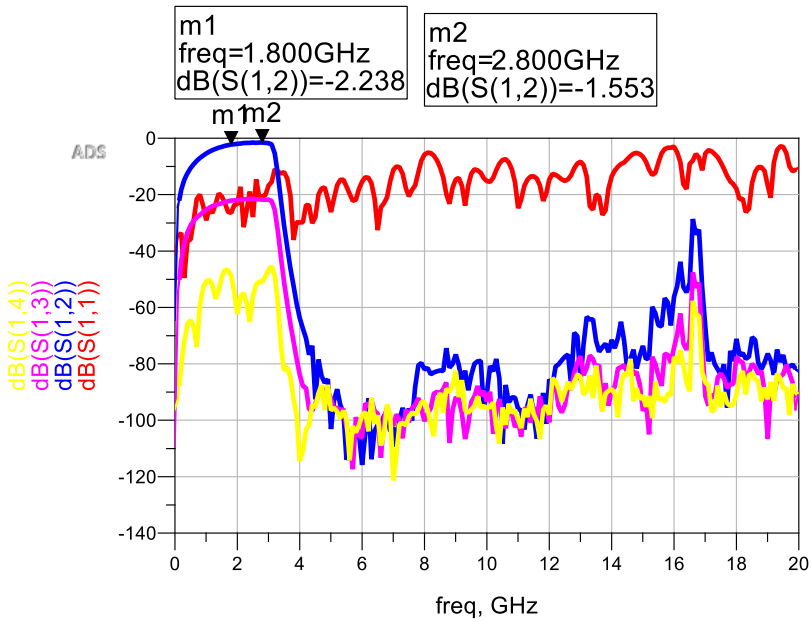

Figure 3-9: Measured s-parameter of test-set at fundamental source side port.

Figure *3-10* illustrates the second harmonic port at the load-side. As it is designed to let pass the frequencies over 3.6 GHz, test-set loss is 1.605 dB which can be compensated by high-power drive amplifier in this port. Analysing the $S_{1,3}$ and $S_{1,4}$

shows, second harmonic power is not appeared at other ports and there is high isolation factor for this frequency range.

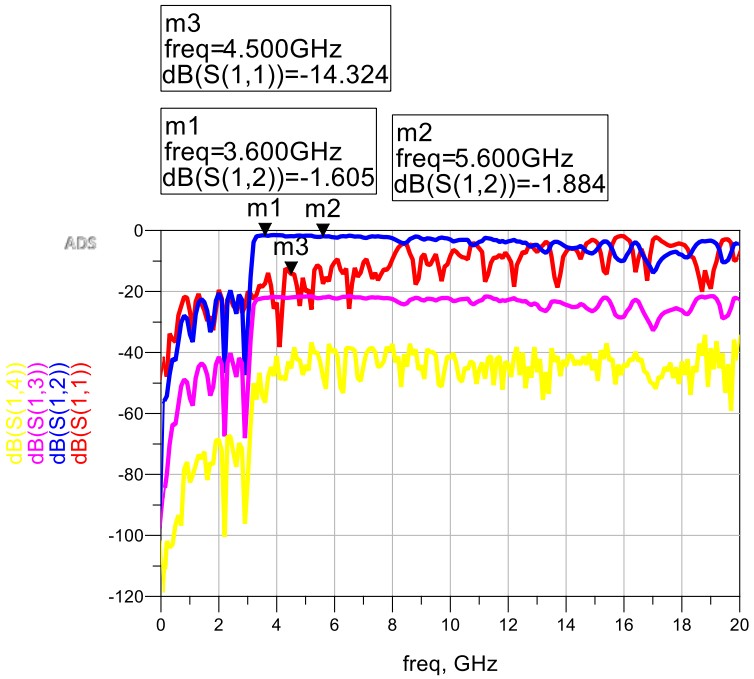

Figure 3-10: Measured s-parameter of test-set at second harmonic port.

3.2.2 COMPONENTS KEY SPECIFICATIONS

The designed test-set is constructed with some RF passive components, which their specifications are important to verify the precision of measurement and ensure to reach the intended objectives of measurement. In this section, some of the essential features of components are revealed.

3.2.2.1 DIRECTIONAL COUPLERS

Directional couplers are manufactured by centric RF (C0518-20) and defined with 3 fundamental metrics, as:

1. Directivity
2. Coupling factor

3. Isolation factor

These couplers can couple the frequencies from 0.2 GHz to 18+ GHz is 20 dB with 2 dB tolerance, to deliver the incident and reflected waves of input and output of the device to the receivers. Their directivity varies in different frequency ranges and is mentioned in Table *3-1*, which expresses coupler can deliver a significant amount of power in direct transmission line. Furthermore, their isolation factor is around -45 dB in their covered frequency.

Table 3-1: Directivity factor of directional couplers

Frequency range	Directivity factor
200 MHz- 4 GHz	22 dB
4 GHz- 12.4 GHz	15 dB
12.4 GHz- 18 GHz	10 dB

3.2.2.2 BIAS T

Two wideband bias T are used in the test-set to allow the wideband characterisation of the DUT. Source side bias T is manufactured by MECA electronics (205S-FF-5) and its bandwidth is from 100 MHz to 6 GHz with 30 dB isolation between the RF and DC paths. Its maximum voltage and current limits are 100 V and 2.5 A, respectively which is suitable for the input of the device as power amplifiers' gate current is not significant and 2.5 A is enough to deal with input of the device. In terms of RF peak power, it can support up to 200 W in the pulse mode and its maximum average power in CW mode is 5 W.

Load side bias (MC2-BT-016347) has a similar bandwidth. However, its maximum voltage and current levels are 100 V, and 7 A. its RF maximum peak power is around 200 W, and its average power for the CW signal is 3 W.

This bias T makes characterising the high power device possible as its current limit is high. For example, in a 100 W device with 70 % efficiency the maximum, 142 W DC power will be produced, therefore current bias T on the load side can deal with such high power devices as its maximum DC power is 700 W.

3.2.2.3 DIPLEXER

Diplexer includes two 90-degree hybrid couplers and low pass filters. Low pass filter can filter the frequencies more than 3 GHz with 50 dB isolation and 90-degree hybrid 3 dB coupler have high power limitation and isolation factor.

3.2.3 PRS

Phase Reference Standard (PRS) is used for obtaining the phase differences among the different harmonics. The signal which is generated by the G_{ref} goes across the amplifier and the output signal is received by the R_{ref}. The accurate measurement requires the precise phase differences among the harmonics. Due to this aim, all the factors that can affect the phase output such as temperature and load dependence should be controlled and fixed. Consequently, a circuit is designed to keep the temperature of the box constant. As the heating process is easier and faster than cooling, the designed circuit aims to fix the temperature at a higher than room normal temperature. A thermistor is used to measure the temperature and a thermo-resistor is used to heat the box anytime that is required. The designed circuit fixes the temperature at 35°C. The circuit can increase or decrease the current flow through the resistor to control the temperature. Finally, the phase output of the reference is

determined and tabulated from a sampling oscilloscope measurement. All the resulted phase differences are saved in a table and imported to the code to compare the phase of the harmonic once the number of investigated harmonics is more than 1.

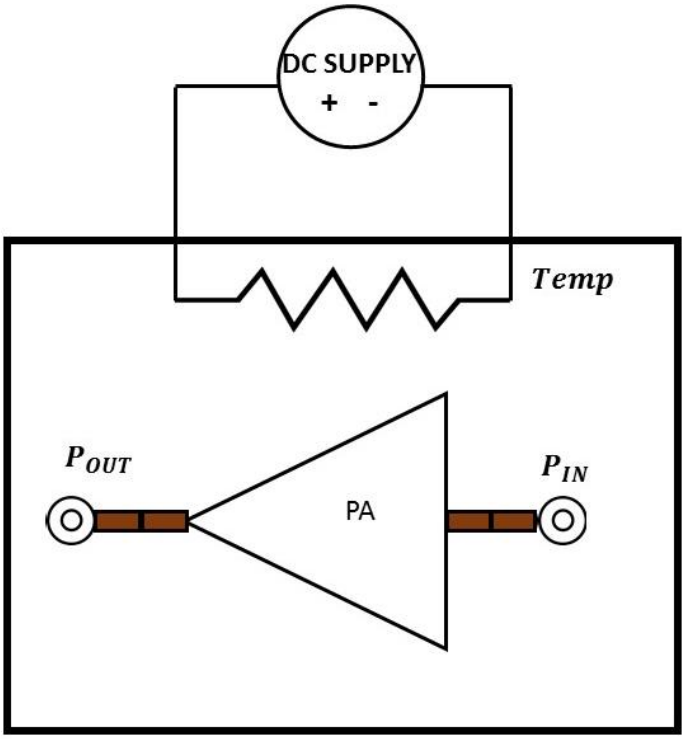

Figure 3-11:PRS schematic

Figure 3-12 demonstrates the inside of the designed PRS that includes a temperature control module and a Low Noise Amplifier (LNA). To design a standalone PRS module a controller, thermocouple, heater, AC relay, LNA and DC supply which provides 12 V at the output to bias the LNA and provide required DC voltage for temperature control system. Heater and thermocouple are connected to LNA to measure its temperature and heat it as required.

3.2.3.1 PRS CALIBRATION

Temperature of the module is set to 35ºC and heater start to heat the LNA when its measured temperature is less than desired temperature level.

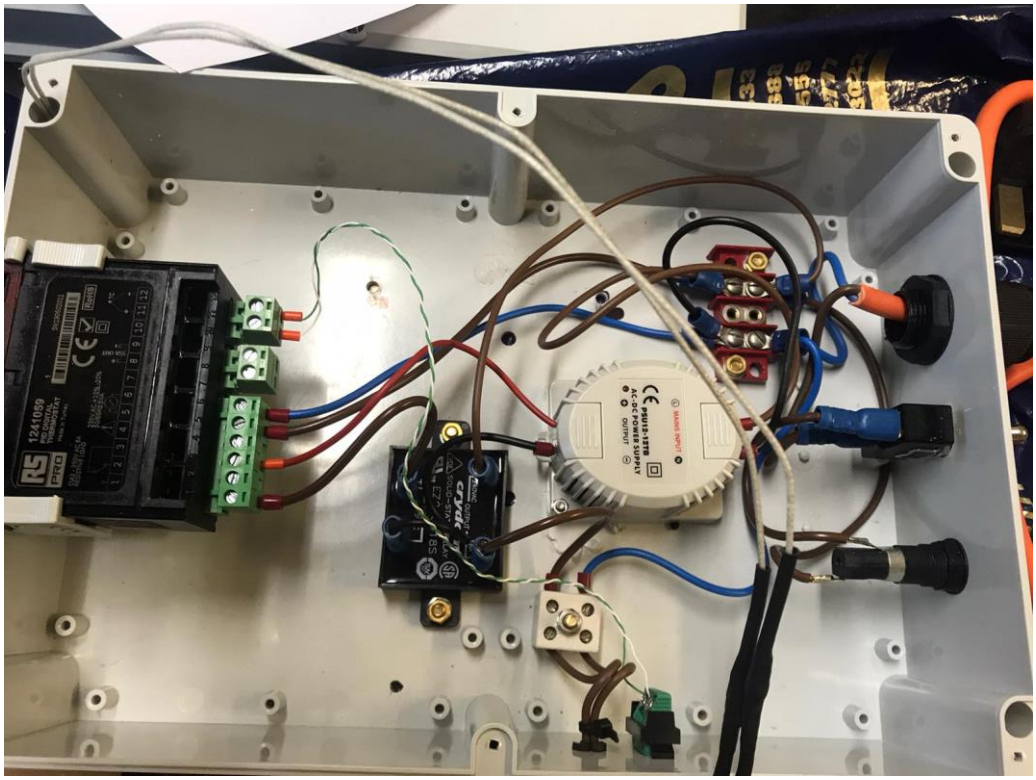

Figure 3-12: Designed PRS block (inside view)

VST5 is utilised to apply the RF signal to PRS and its power level is set to put the PRS's PA in 3 dB gain compression level thus device can be operated in nonlinear regime and generate harmonics. A real-time Tektronix scope is employed to analyse and record the output waveform of the PRS, that allows to record wide range of harmonics. Scope sample rate is set to 5 GS/s and it records 4000 samples on each waveform. P_{in} level of the generator is set to 8 dBm and two 10 dB attenuators are located in the input and output of the LNA. Figure 3-13 shows the spectrum of output of PRS while input power is 8 dBm, frequency is 1 GHz and temperature level is 35ºC.

LNA operates in nonlinear region and up to 8 harmonics are above the noise level of the scope. Therefore phase and magnitude of the each harmonic is recorded and by repeating this measurement with different frequencies, recorded data can be inserted to extract the relation between phase of different harmonics.

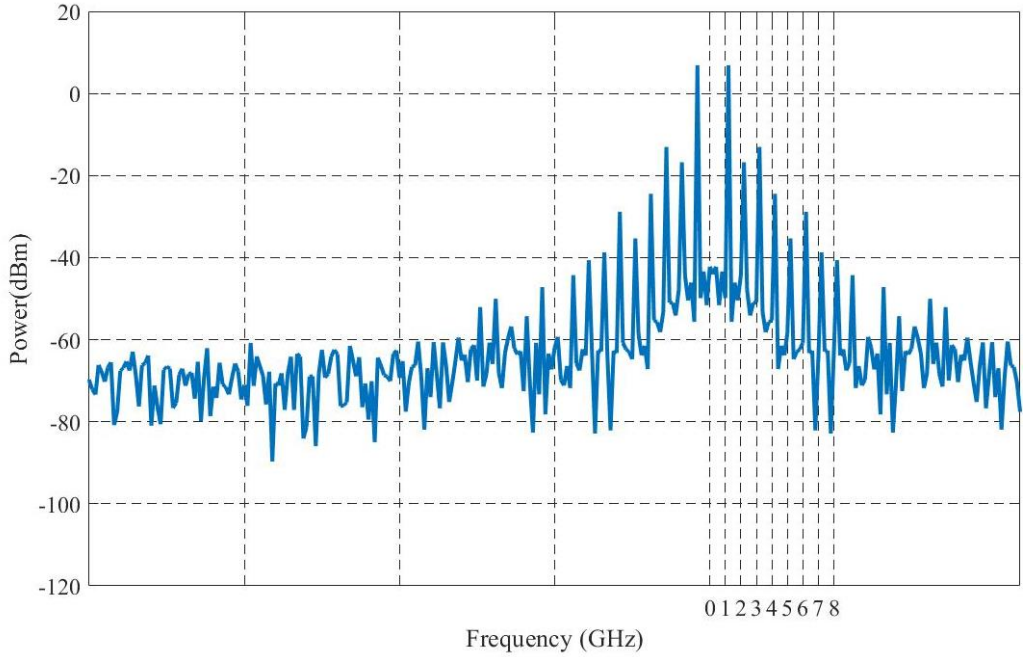

Figure 3-13: spectrum of the output of the PRS. 3 dB gain compression, 1GHz fundamental

3.2.3.2 INTEGRATION OF PRS INTO MEASUREMENT SYSTEM

Calibrated PRS assists us to measure the current and voltage waveforms of the PA, that leads to accurately analyse different phenomenon in device. Waveforms are always helpful for engineers and researchers to distinguish various elements effect on observed behaviour, thus by integrating PRS comprehensive understanding about device behaviour can be achieved. To examine accuracy of the calibrated PRS, the output waveforms of the 10 W packaged GaN (Wolfspeed CG2H40010) device are illustrated in Figure 3-14. These waveforms were measured under pulsed condition at the start of 300 µs pulse width with 3% duty cycle, and sample rate is 100 MS/s and sample per average is 6 k.

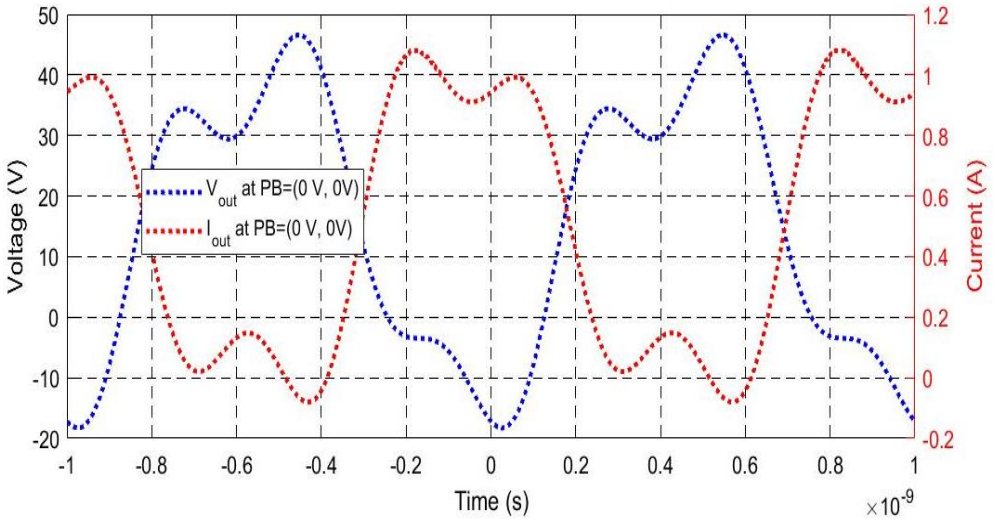

Figure 3-14: Output waveforms of 10 W GaN device under pulsed condition measured with calibrated PRS. PW= 300 µs, duty cycle= 3 %, 3 dB gain compression, bias point =(-3.5 V, 28 V), acquisition length= 60 µs, sample rate= 100 MS/s, 3 harmonics are captured.

3.3 VST STRUCTURE

VST PXIe-5840 is one of the new transceiver models with 16-bit ADC resolution that possesses up to 1 GHz instantaneous bandwidth when the centre frequency is higher than 2.2 GHz. Table 3-2 shows the instantaneous bandwidth of VST at different centre frequencies [5].

The sample rate in VST can vary from 19 kS/s to 1.25 GS/s, which gives time resolutions less than a nanosecond in acquisition side and allows to apply short duration signals to the device.

Figure 3-15 shows the internal architecture of the transmitter of VST, which consists of low pass filter banks, internal amplifiers and variable attenuators in the RF path, which are programmable and can be bypassed in LabVIEW.

Table 3-2: Instantaneous Bandwidth of VST PXIe-5840

Centre Frequency	**Instantaneous Bandwidth**
9 kHz to <120 MHz	<120 MHz
120 MHz to 410 MHz	50 MHz
>410 MHz to 650 MHz	100 MHz
>650 MHz to 1.3 GHz	200 MHz
>1.3 GHz to 2.2 GHz	500 MHz
>2.2 GHz to 6 GHz	1 GHz
The PXIe-5840 uses the LO frequency subsystem to directly acquire or generate any signal below 120 MHz	

In generator path, amplification and attenuation are applied in 3 programable steps to the signal, that set intended power level of generated I and Q samples. Same architecture is used for receiver as shown in Figure 3-16.variable amplification and attenuation are applied in 2 steps to the received signal. In case of Continuous wave (CW) measurements, the individual fundamental and harmonic I and Q signal components are down-converted in succession to DC, in which case the sampling frequency of the analogue-to-digital receiver is used to acquire multiple samples of the same DC measurement to facilitate rapid signal acquisition and processing.

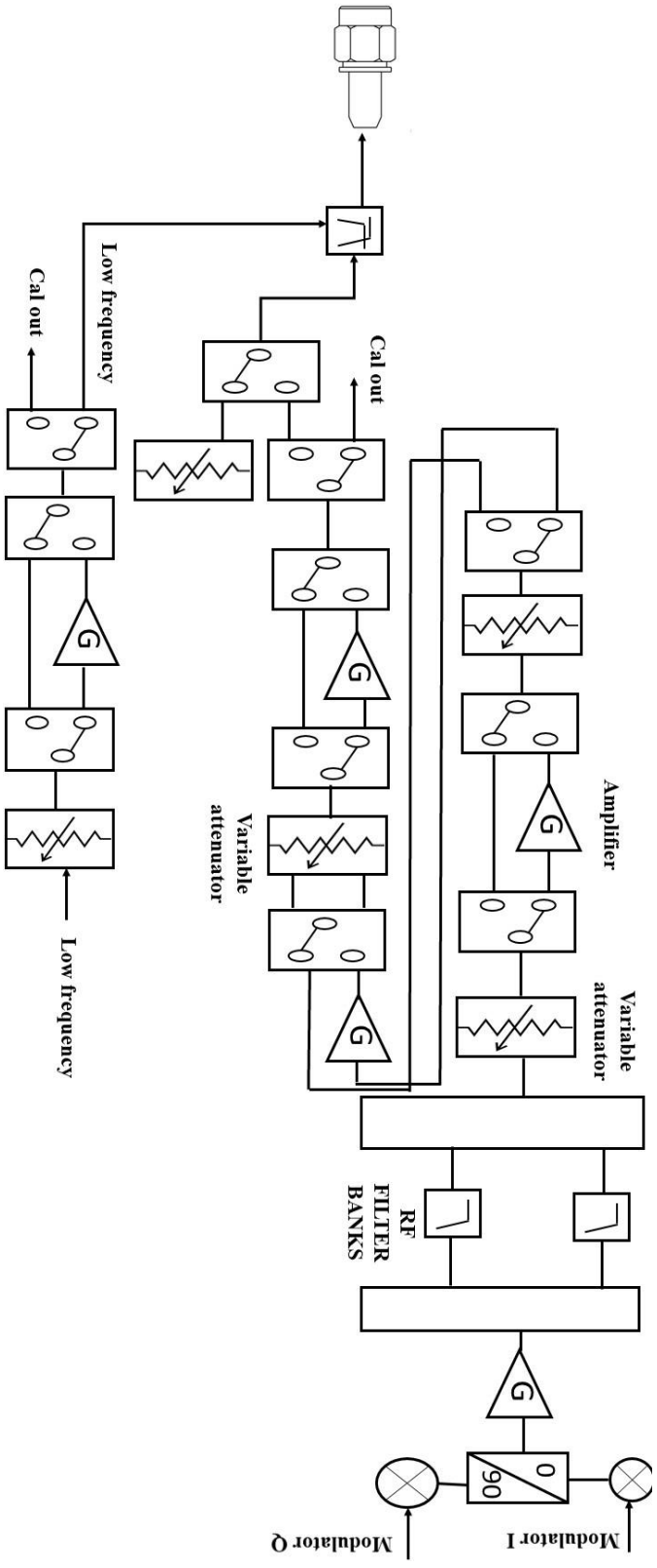

Figure 3-15:Internal structure of generator

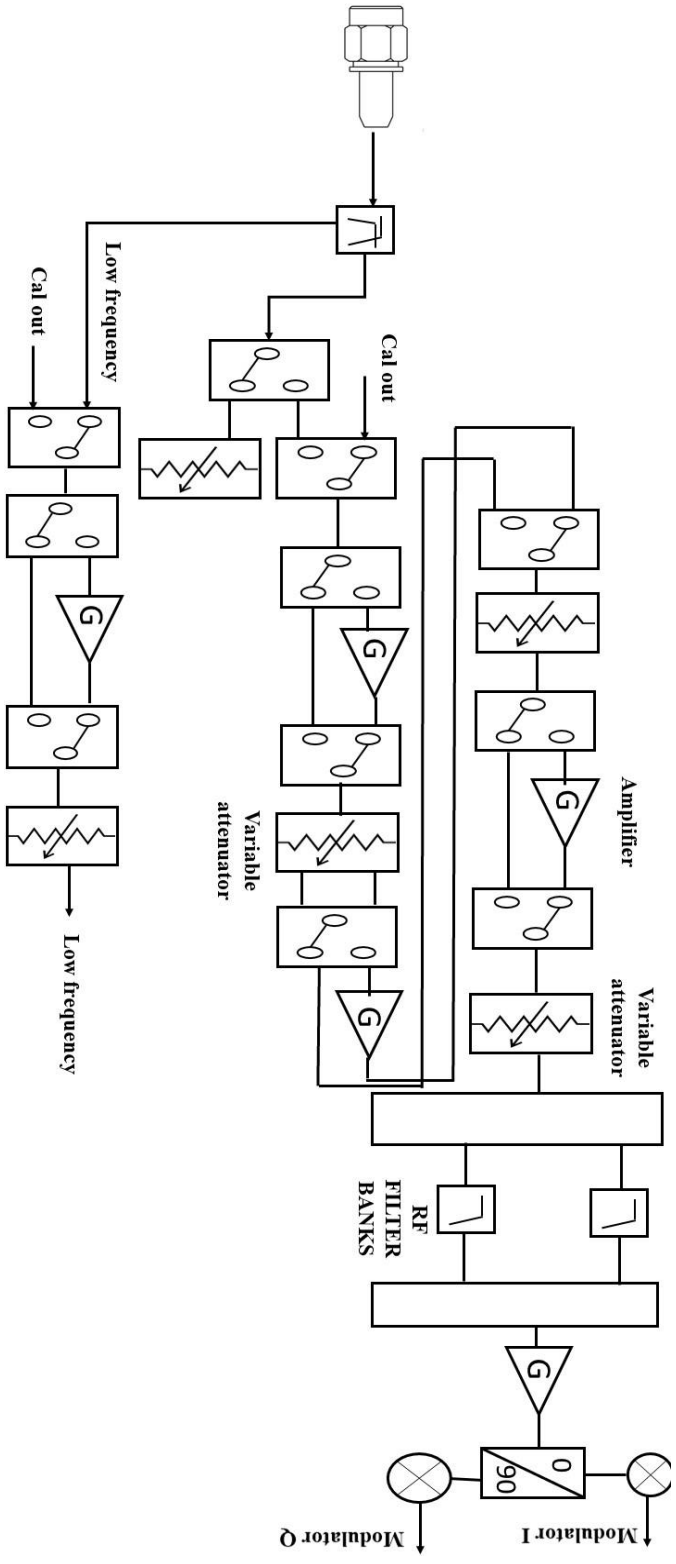

Figure 3-16: Internal structure of VST for receiver side

3.4 GENERATION AND MEASUREMENT OF DC PULSES

Two NI-PXIe 4139 Source Measurement Units (SMUs) are utilised to apply DC voltage to the device and measure DC currents and voltages of gate and drain ports. They can be operated in pulsed and continuous modes and provide voltage and output power up to 60 V and 500 W, respectively. As shown in Figure *3-17*, in the continuous mode they can supply DC signals up to 20 W in the first quadrant plane. These units achieve higher powers up to 200 W and 500 W, when used in pulsed mode with the maximum duty cycle of 5 % and 2 %, respectively.

SMUs can provide pulsed DC signals with at least 50 µs length for each "on" and "off" section of the pulse and they apply pulsed voltages with slow, normal, fast, and custom conditions. In custom condition, user can change the pole and zeros of the transfer function of the output of the SMU to change the value of overshoot and transient time and set specific transient time for SMUs.

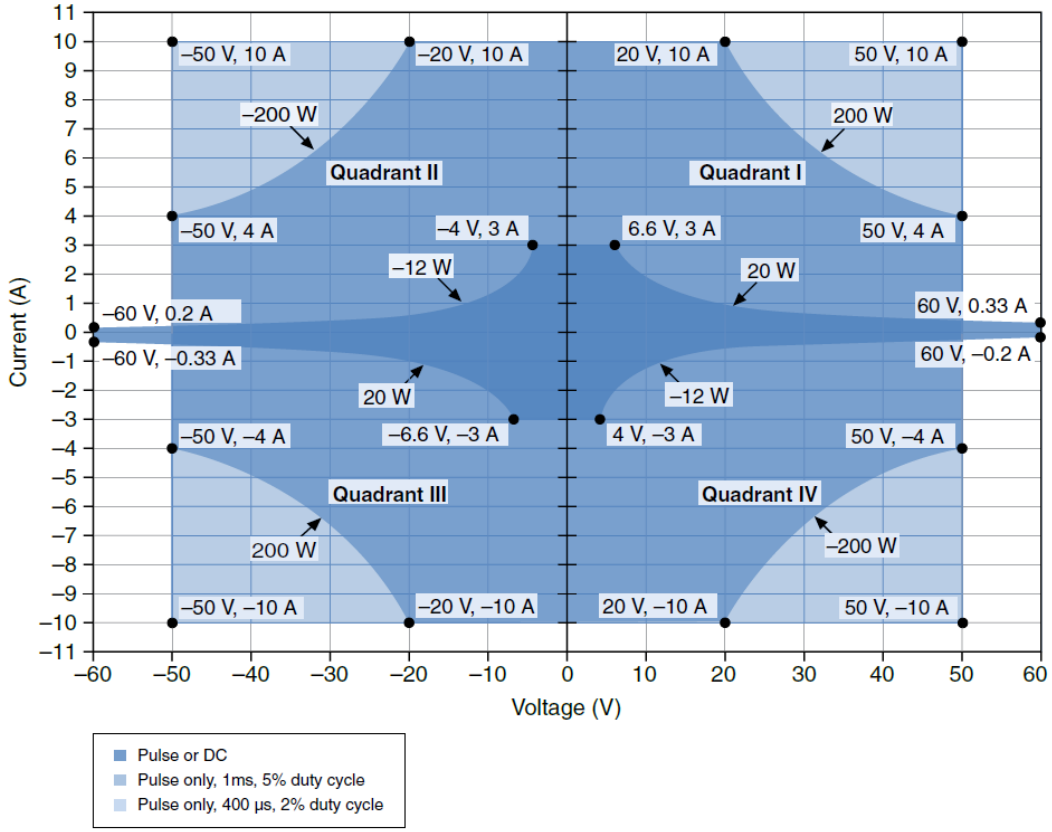

Figure 3-17: Different working areas of SMUs with various output power limitations [7]

Figure *3-18* demonstrates the required transient time of SMUs modules to apply 30 V DC pulses as centre point of SMU's voltage range. As transient time is related to the load side impedance (RC value of the load of the SMU) and voltage value with a measured device connected to SMUs as load impedance. In the fast mode, the transient time to achieve 30 V is around 30 µs to achieve 90 % of the desired voltage level. The transient condition is set to fast mode during all measurements of this thesis to rapidly perform measurements.

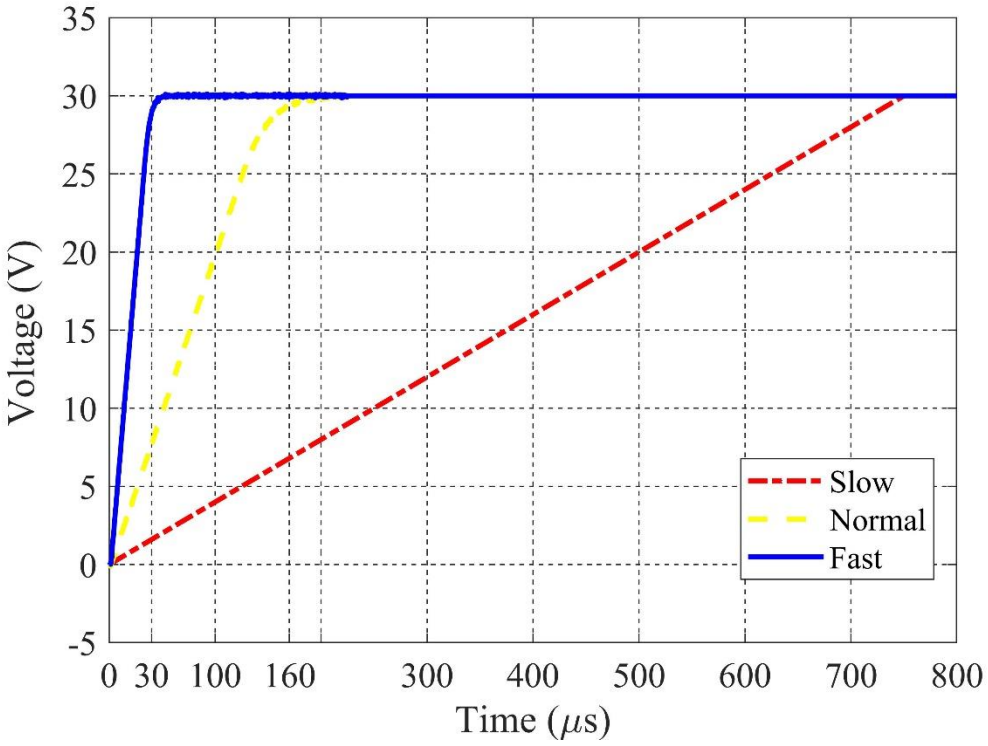

Figure 3-18: Measured transient time of SMU at when a 10 W device is connected to SMU's output.

Furthermore, SMUs provide the capability to measure the DC values with a maximum 1.8 MS/s sampling rate and the minimum aperture time of 555ns. The accuracy of SMUs increases by increasing aperture time as the number of the sample per average increases. The SMUs recording window is synchronized with RF receivers, therefore minimum employed aperture time is 60 µs, which results in less than 100 µV and 10 µA accuracy for measuring voltage and current on load side, respectively. The accuracy of DC data increases by employing different averaging techniques as:

1. Normal averaging

2. Second-order

In the normal averaging, all the samples during the aperture time have the same weight but in the second order, the samples have relative weighting to improve the noise

rejection[7]. In this thesis normal averaging technique is occupied to measure the DC voltage and current of input and output of the device.

3.5 SYNCHRONIZATION AND TRIGGERING FOR FULL MEASUREMENT SYSTEM

In active load-pull measurements, synchronisation is a paramount factor to minimise misalignment between source and load sides. Two generators that are supplying RF signals to the input and output ports of the device should apply the RF signals with intended power level and phase simultaneously, to the input and output of the device. Misalignment between generators leads to set the load impedance to 50 Ω during the misaligned period, therefore, all achieved power and efficiency contours will not be valid.

To synchronise all PXIe modules in a single chassis Trigger Clock (T-Clk) technique is employed. The T-Clk technology ensures time synchronisation across all linked channels and aligning the sample clock edges with a tolerance less than 800 ps. As all modules are in the same chassis and backplane and triggers are sent via the backplane, thus accuracy of synchronisation is better than previous NI based measurement system in [8].

PXIe 1085 is a 18 slots chassis with 3 buses of trigger lines at the backplane that each bus can support 6 slots of chassis, and has 8 trigger lines (PXI-TRIGGER0-7). To send a trigger from one bus of chassis to another one via backplane trigger lines, specified trigger line should be allocated to the sender bus in NI-MAX. To synchronize all occupied modules, NI-TClk is used and all VSTs and SMUs are set to start with a trigger, thus all receivers and SMUs start, once they receive trigger on a specific

trigger line that is allocated to them. As VST is an IQ based signal transmitter and receiver, it can send a marker on each IQ sample of the generated waveform. VST1, as a master slot, sends out three different markers to other slave modules, and slave modules start to work once they receive the desired marker through the allocated trigger backplane. VSTs and SMUs start to work in a proper order that is safe to and reliable to bias the device, set load impedance actively and record the data in receivers accurately. Consequently, generator 1 (G1) generates three markers with a flexible delay between them. The objective is to make the control as straightforward as possible while maintaining a high degree of flexibility and synchronizing the SMUs with VSTs, to generate the synchronized DC and RF pulsed.

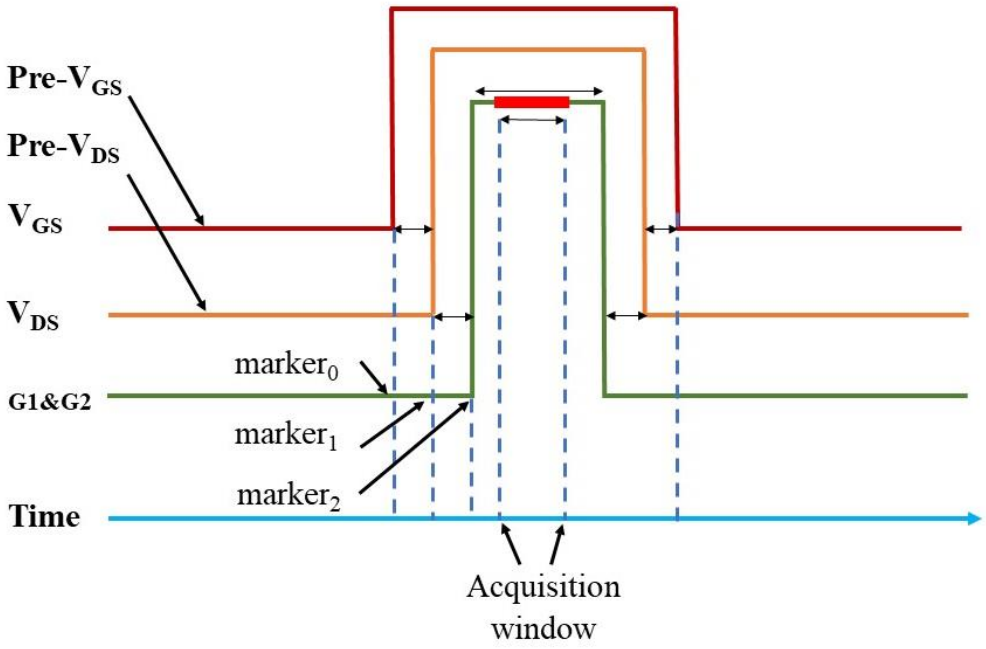

Figure 3-19: Generated pulses order and pattern of the RF generator with employed sequence of markers to synchronise all modules.

Figure 3-19 shows all generated pulses and applied order to synchronously bias the device and performing measurements. Firstly, G1 generates marker0 and marker1 during the off-state of the RF pulse and sends them to SMU1 and SMU2, respectively.

As can be seen from Figure 3-19, SMU1 receives the marker0 and starts to supply the V_{GS} and then SMU2 by receiving the marker1 starts to apply V_{DS}. There is a flexible time delay between marker0 and marker1 ($margin_{START-GS}$) to apply V_{GS} and V_{DS}, consecutively. Therefore, before applying the V_{DS} to the device, gate port is biased and there is no harmful effect for the device at start of applied pulse, since current level is controlled with V_{GS}. Moreover, the duration T_{ON-GS} should be larger than T_{ON-DS} since V_{DS} should return to its off-state value before V_{GS}, otherwise, the device will produce an excessive high power at the output port. According to these points, the T_{ON-GS} and T_{ON-DS} are defined in (3-1) and (3-2).

$$T_{ON-GS} = T_{ON-DS} + margin_{START-GS} + margin_{END-GS} \quad (3\text{-}1)$$

$$T_{ON-DS} = T_{ON-RF} + margin_{START-DS} + margin_{END-DS} \quad (3\text{-}2)$$

As can be seen, the duration of DC and RF pulses are related to each other, and the user can control the length and duty cycle of each pulse by tuning controllable margins between them. Once off-state of the RF generated pulses is finished, RF signals from source and load sides are applied to the device and finally, after providing V_{GS} and V_{DS}, the G1 and G2 generate a specified power level and G1 sends out marker2 to all receivers and they start to acquire data, and SMUs concurrently starts to measure I_{DS} and I_{GS}. By using this method, the transistor will only be biased if the RF signal is applied to it, thus all the factors are controlled to securely bias the device.

As can be seen in Figure 3-19 SMUs can set different voltage levels during the off-section of pulses, thus allowing to pre-charge device traps before its RF operation. This allows the study of various gate-lag and drain-lag levels by a controlled pre-

charging of the device traps utilising programmable pre-V_{GS} and pre-V_{DS} values. For such measurements, the V_{DS} pulses start later than V_{GS} pulses during drain-lag measurements, otherwise for a few microseconds, device will generate high current if large pre-V_{DS} values are used.

3.6 PULSED RF SIGNAL SPECTRUM

Basic concept of pulse measurement is shown in Figure 3-20, switching the signal and repeating the pulses with Pulse Repetition Interval (PRI) with the time-domain and frequency-domain of the signal shown in as (3-3) and (3-4), respectively [9].

$$y(t) = [x(t) \times rect_{PW}(t)] * shah(PRI \times t) \quad (3\text{-}3)$$

$$Y(F) = Duty\ cycle \times X(F) \times sinc(PW \times f) \times shah(\frac{f}{PRI}) \quad (3\text{-}4)$$

Where PW is the pulse width of the signal, PRI the pulse repetition interval, and shah(t) is a train of pulses.

Therefore, either the applied RF signal is CW or multi-tone with its spectrum further broadened by switching mechanism. Figure 3-20 illustrates the simulation results of a spectrum of a burst of ideal pulses with no transient time which is mentioned in (3-4). The length of the side lobes of its spectrum is proportional to the inverse of the pulse with, $\frac{1}{PW}$, and the space between the various spectral components is related to the pulse repetition interval ($\frac{1}{PRI}$). Critical pulse parameters such as duty cycle and pulse width, change the spectrum of the applied pulses and by decreasing the 'on' section of the pulses and make them narrow, the spectrum of the signal spreads in the frequency domain.

To analyse the spectrum of pulses, CW pulses with centre frequency at 1.8 GHz and 3 % duty cycle are generated and directly applied to the receiver. Figure 3-20 shows the spectrum of consecutive pulses when all the generated pulses are captured in a single acquisition window, however, Figure 3-21 shows the spectrum of each RF pulse separately for two different pulse width with the same pulse repetition rate.

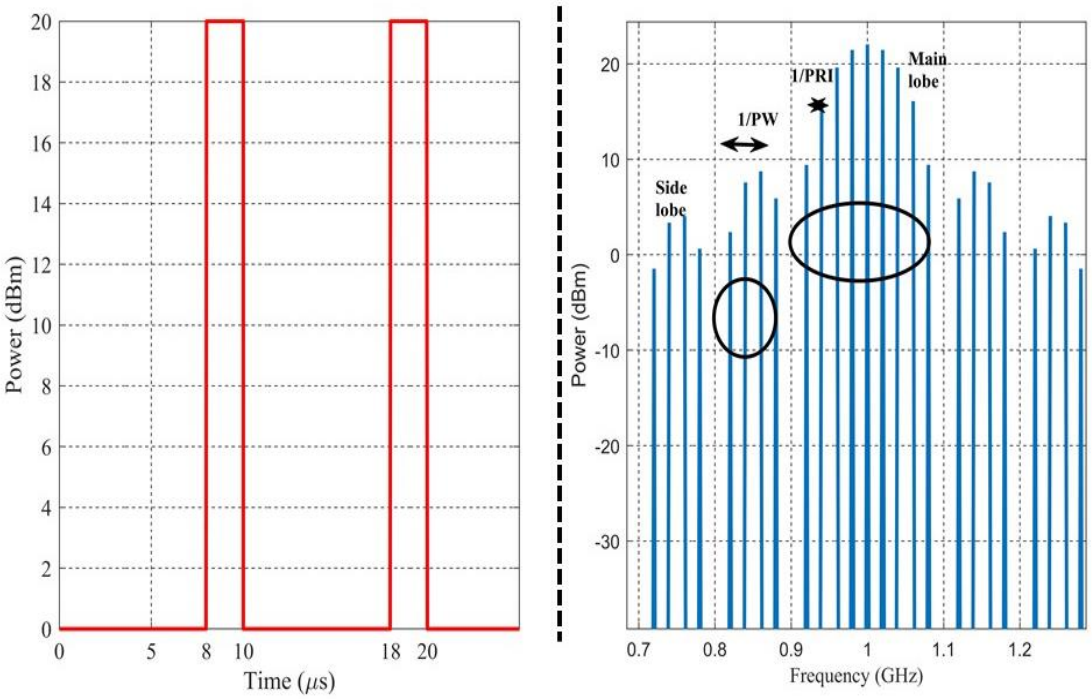

Figure 3-20: Time domain and spectrum of pulse measurement, duty cycle=20 %,PRI=10 µs, PW= 2 µs, sample rate= 50 MS/s, sample per average= 6 k.

As expected, by increasing the pulse width of the signal, width of the lobes of the generated pulses decreases and power of the main increases by $\frac{PW2}{PW1}$.

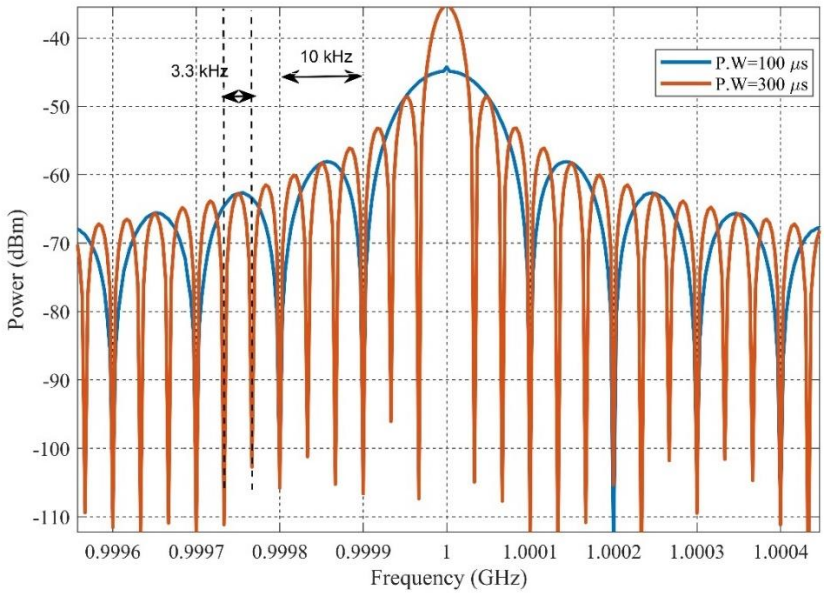

Figure 3-21: Analysing pulse width effect on spectrum of the pulsed signals.

3.7 RF PULSE ACQUISITION TECHNIQUES

Pulse measurements are typically based on two fundamental acquisition techniques applied by NVNAs and LSNAs and other commercial technologies [10].

- Narrowband technique
- Wideband technique

In the narrowband technique, receivers don't have enough bandwidth to cover all side lobes of the applied pulse, an IF filter is used to isolate the centre frequency of the spectrum, thus at the output of the IF filter, a scaled CW signal is generated. Consequently, there is not any limitation for analysing narrow pulses, however, this technique affects the dynamic range of the system. Smaller duty cycle, lower dynamic range will be achieved, as by decreasing the duty cycle (increasing the PRI) the average power of the pulses gets smaller and signal-to-noise ratio decreases. The

degradation in dynamic range of the measurement can be expressed as $20 \times \log_{10}(duty\ cycle)$. Moreover, there is no need to synchronise the analyser's samples with incoming pulses and using a data acquisition trigger. This technique is typically known as spectral nulling acquisition [10].

Therefore, when duty cycle and drive level are low, measurement will not be accurate, and typically, averaging across multiple measurements is performed to increase the accuracy. This is referred as "pulse desensitization" [10].

The second technique that is used to obtain pulse measurements, is the wideband technique. As the utilised receivers have a wider bandwidth, they can record most of the side lobes of the pulse signals spectrum and all the energy of the signal is inside the bandwidth of receivers as shown in Figure 3-22. Therefore, in this approach, synchronization between the pulses and the receiver's acquisition window is an important requirement [10] to account for any delays between the detected pulses and the pulses at the DUT input and output terminals.

The advantages of this technique are, high-speed measurement, simplicity of test-set, and no loss in the dynamic range of the measurement system, thus it is a more robust technique when the applied pulses have low duty cycle and power levels.

However, as receivers are required to have a larger bandwidth, it exhibits a higher noise level in comparison with a narrowband technique. This technique is also severely restricted when the receivers' maximum instantaneous bandwidth is not high enough to measure the narrow pulses. In this thesis wideband technique is employed as VST provides up to 1 GHz instantaneous bandwidth which is enough to measure narrow pulses down with pulse widths of only a few nanoseconds.

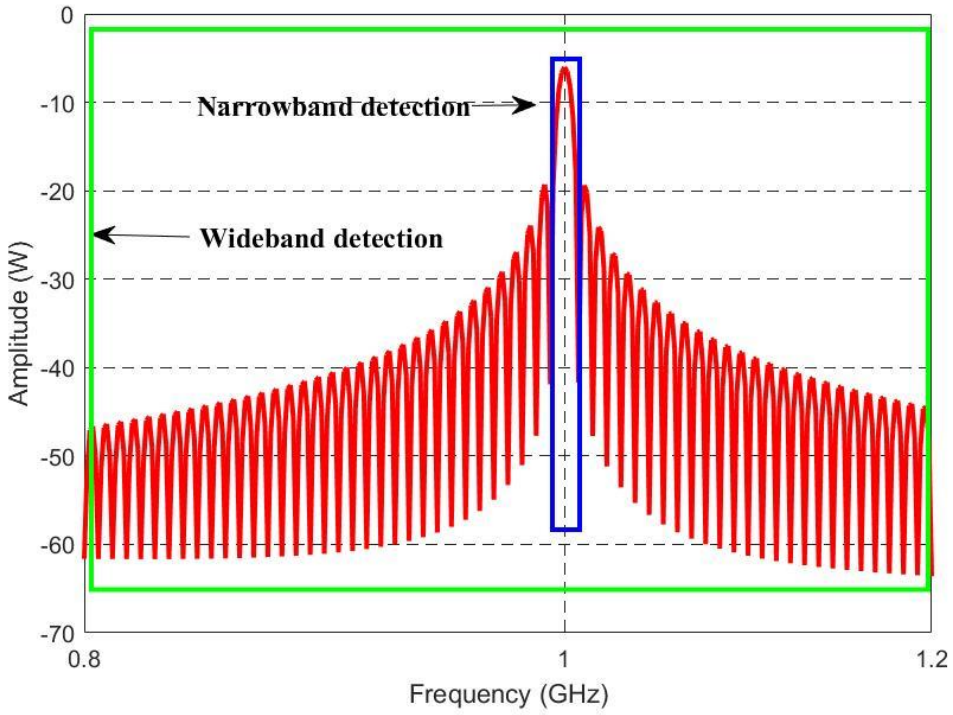

Figure 3-22: Narrow band and wide band detection techniques for pulse measurements.

3.8 VST SYSTEM RF PULSE ACQUISITION FEATURES

VST possesses some unique features to perform pulse measurements. The wideband detection technique is utilised differently in VSTs in comparison with other commercially available pulse analysers. In the VST system, there is a one-to-one correlation between generated and measured pulses which are fully processes during the time between pulses. However, in PNA based pulsed measurements there are some skipped generated pulses to record all measurement points [10], and in LSNAs, to record enough samples to take FFT, multiple pulses are generated. The skipped pulses during the consecutive measurements increase the measurement time. Moreover, to analyse and investigate the trapping and memory effect, it is crucial to have consecutive pulse acquisition without any skipped pulses, since any applied RF pulse,

with time constants often larger than the pulse repetition interval, interrelates multiple traps, and analyser should record it.

Another important difference between VST and other technologies is its large instantaneous bandwidth. As summarised in Table 3-2, it can measure accurately pulses with at least 5 ns time resolution at centre frequencies above 1 GHz. In contrast other instruments such as LSNA and NVNAs with significantly lower instantaneous bandwidth employ stitching techniques to measure narrow pulses.

Typical pulse measurement instruments measure within the frequency domain and compute then time-domain data, and in contrast to VSTs, which measure samples in the time-domain without the need to transfer the acquired samples to frequency-domain.

The employed VSTs with the part number PXIe-5840 have an analogue-to-digital converter with16-bit resolution on receiver side, which is accurate enough to provide meticulous measurement data for characterising 5G's devices. This level of bit resolution is higher than any currently available NVNA and real-time sampling scopes, which provide up to 10-bit resolution.

The developed VST-based system can readily perform different types of pulse measurements such as pulse-to-pulse, sample-by-sample pulse profiling, at the entire RF pulse or specific sections of the pulse, by changing the acquisition window's length and starting point. During pulse profiling measurement, the acquisition window can start before RF pulses are applied to the device to cover rise and fall time with the acquired samples are grouped together into smaller time sections, then processed to obtain a group average to increase the signal-to-noise ratio. To analyse different time-slots of the pulses and minimise the memory requirements, the acquisition window's

length and delay are set to only capture the samples on the specific section. System is capable to conduct 500 measurements with up to 6k sample per average (12 M total samples) in a single execution.

3.9 VSTS RF PULSE GENERATION METHOD

VST provides full access to settings of generated waveforms. IQ samples of waveforms are defined in a dedicated script, to tailor the envelope of the signal, thus a different type of stimuli can be applied to a device such as pulsed CW and pulsed multi-tone. The script can be fully synchronised with the DC pulses of the SMUs and acquisition windows of the VST. In this section, some of the applications of definable IQ-based signals are mentioned.

3.9.1 PRE-SHAPING PULSE

Tailoring the generated signals allows applying pre-shaping to the generated waveforms to determine the performance metrics of the device such as linearity.

For example, Figure 3-23 shows the 4 W device response to a pulsed CW stimulus. As expected, the device does not have constant response in the time domain and its output varies within the pulse. To compensate this variation and obtaining a fixed response from the device, the output of the device is reversed and applied to IQ sample generator function, thus applied pre-shaped pulse led to have fix response at the output and eliminates the variation.

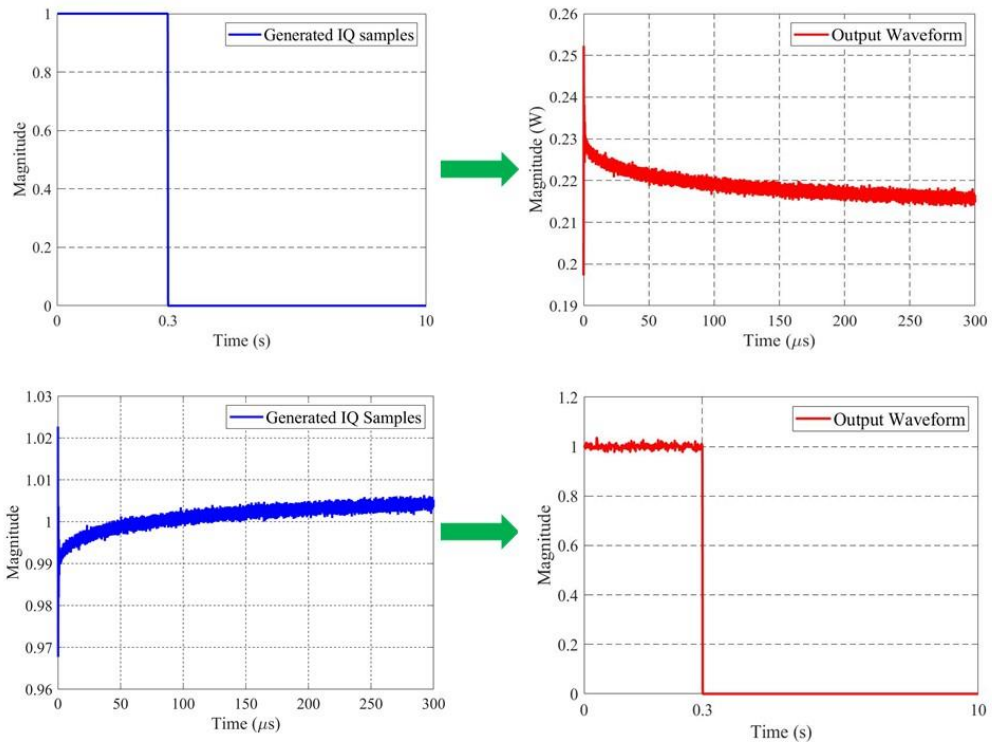

Figure 3-23: Pre-shaping signal and PA's output. PW= 300ms, duty cycle=3 %.

3.9.2 MULTI-TONE PULSE

In the script generator of the VST system, user can define the number of the tones, their frequencies, power levels, and initial phases. IQ-based generator gives this opportunity to readily generate a pulsed signal with any number of tones, that allows to carry out various interesting measurement.

3.10 KEY PERFORMANCE METRICS OF RF PULSE MEASUREMENT SYSTEM

In this section, some of the paramount performance metrics of RF pulses is presented. Rising and falling times of generated RF pulses, pulse-to-pulse stability and phase

alignment of consecutive pulses are investigated to validate PXIe-5840's reliability of pulse generation and acquisition.

3.10.1 RISING AND FALLING TIME OF RF PULSES

To clarify the transient time of the generated RF pulses, the VST generator is directly connected to the VST receiver and the sampling rate of the receiver is set to the maximum rate (1 GS/s) with the acquisition time window set to capture the entire RF pulse including the transients. Within this measurement mode, the receivers effectively acquired a measurement every 1 ns. The sampling rate of the VST generator is then varied to observe the impact on the RF pulse transients. As Figure 3-24 indicates, the transient time of generators decreases from 1.65 µs to 80 ns by increasing the sample rate of the generator from 5 MS/s to 100 MS/s. In both cases, generator requires time equal to generate 8 samples to settle the power in the intended level. The required time to increase the power level at the start of the pulse is the same as the falling time at the end of the pulse. Moreover, to change the power level of the generated pulse, the generator produces about 11% overshoot at the edges of an RF pulse, which is in line with the theoretically predicted Gibb's phenomenon. From the above investigations it can be concluded that the VST generators are sufficiently fast to set accurately the required power level in less than 100 ns.

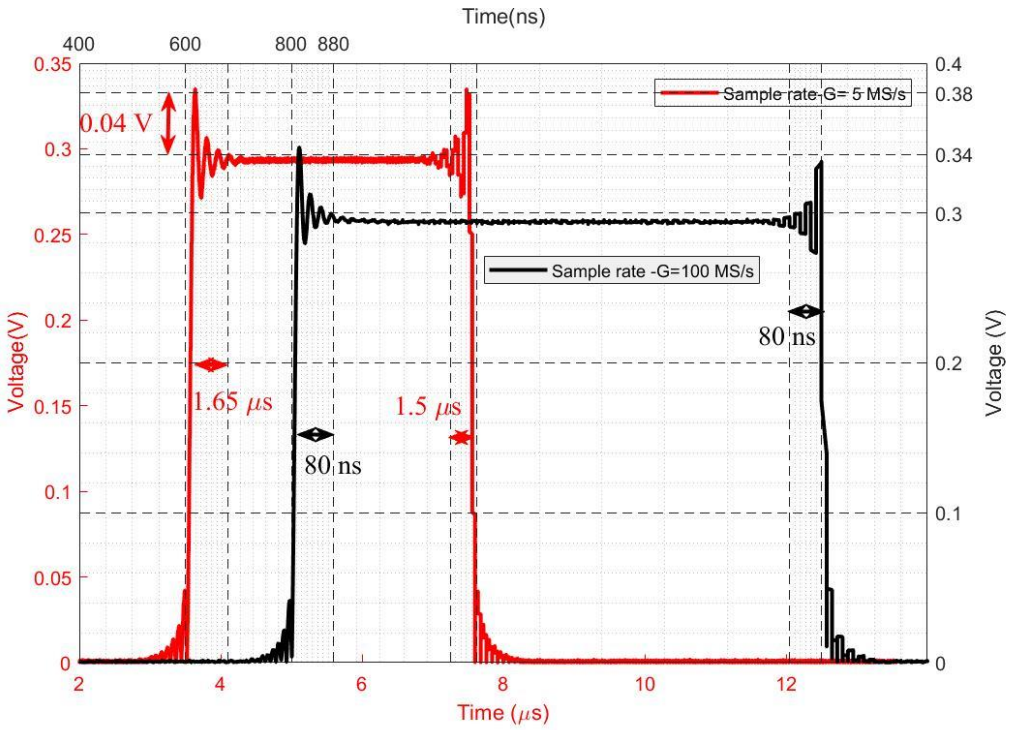

Figure 3-24: Transient time of pulses when generator has two different sample rate, sample rate_R=1 GS/s, Pin= 3 dBm.

3.10.2 PULSE-TO-PULSE STABILITY

To ensure synchronisation between the various pulsed DC and RF signal generators and receivers is important to obtain highly repeatable pulse trains. Any deviation from the set values will make it difficult for the various pulsed data streams and undermine measurement accuracy. Conducting repeatable bursts of pulses is also a paramount factor in some applications such as radar systems when radars want to detect intended targets. Radars receive echoes from the targets, also from surrounding objects such as trees, buildings, and ocean waves. However, signal processing in advanced radar systems can detect and suppress unwanted reflections by comparing the phases and amplitudes of successive echoes and intended target. Consequently, pulse-to-pulse stability is an important metric of phase and amplitude stability of the pulse generator.

To measure the stability of the phase and amplitude of the pulses, a burst of pulses with the same power and phase level is applied to the passive device, and receivers, acquire the section of the consecutive pulses.

Phase and magnitude stability factors are mentioned in (3-5) and (3-6) [11]

$$Phase\ stabilitity = 10\,log_{10}\left(\frac{1}{N-1}\sum_{i=1}^{N-1}(\theta_i - \theta_{i-1})^2\right) \quad (3\text{-}5)$$

Where θ_i is phase of i th pulse and N is the number of consecutive pulses applied to passive device

$$Amplitude\ stabilitity = 10\,log_{10}\left(\frac{1}{N-1}\sum_{i=1}^{N-1}(A_i - A_{i-1})^2\right) \quad (3\text{-}6)$$

Where A_i represents magnitude of i th pulse.

Figure 3-25 shows pulse-to-pulse stability of the VST system. To measure the pulse-to-pulse stability of measurement system, 100 consecutive pulses with 300 µs, pulse width are generated and different points within the pulse are selected to track the pulse-to-pulse stability. The sampling rate of VST system, both the generator and receiver, is 100 MS/s and the RF pulses are captured through consecutive time acquisition windows with a duration of 60 µs. Figure 3-25 shows phase and magnitude stability of VST increases within the pulse, due to the power settling at the start of the pulse. Phase stability of the VST at the start of the pulse is -17 dB and declines by 4 dB within the pulse which means the deviation of the phase is less than 0.1 degree. The magnitude stability of VST at the start of the pulse is -65 dB and it plunges to -80 at end of the pulse.

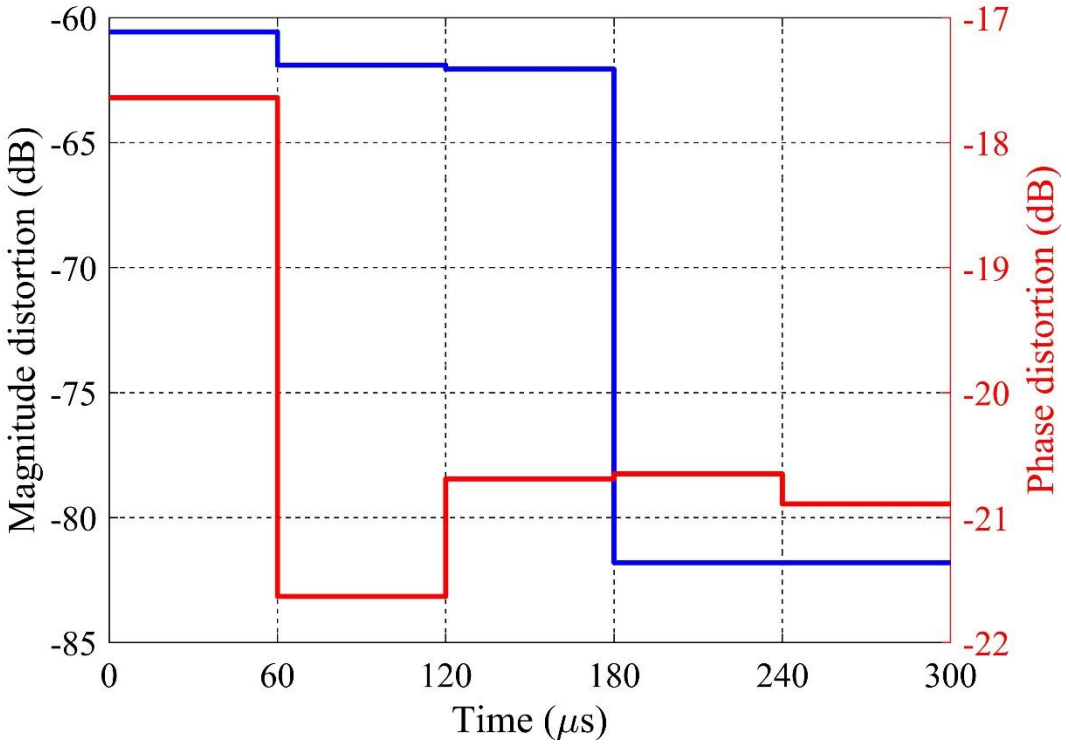

Figure 3-25: Pulse to pulse stability of magnitude and phase at different sections of the pulse, PW= 300 µs, generator sample rate= 100 MS/s, duty cycle= 3 %.

3.10.3 MINIMUM AND MAXIMUM RF PULSE WIDTH

VSTs maximum sample rate in generator and receiver side is 1.25 GS/s, thus it can provide stimulus to the device with the minimum pulse width of 0.8 ns and a flexible duty cycle. Assessing the device with such narrow pulses is an interesting opportunity to characterise any rapid phenomena within a DUT. To explore the RF pulse width settings in the nanosecond range, the VST generator is connected directly to the VST receiver and a narrow pulse with an 8 ns pulse duration and the power step from 50 dBm is generated. Figure *3-26* illustrates the accuracy of the generated pulse and as can be seen, the RF power is settles rapidly to the intended level after about 2ns. This demonstrates that nano-second pulse resolution can be achieved employing high sampling rate of the VST generators. It should be noted

that any averaging of multiple samples across a single pulse becomes difficult for such narrow pulses consisting of only a few samples. This explains the relatively high level of noise within the measured data around the observed -60 dBm power level. If necessary, this can be mitigated by performing averages across multiple measured RF pulses.

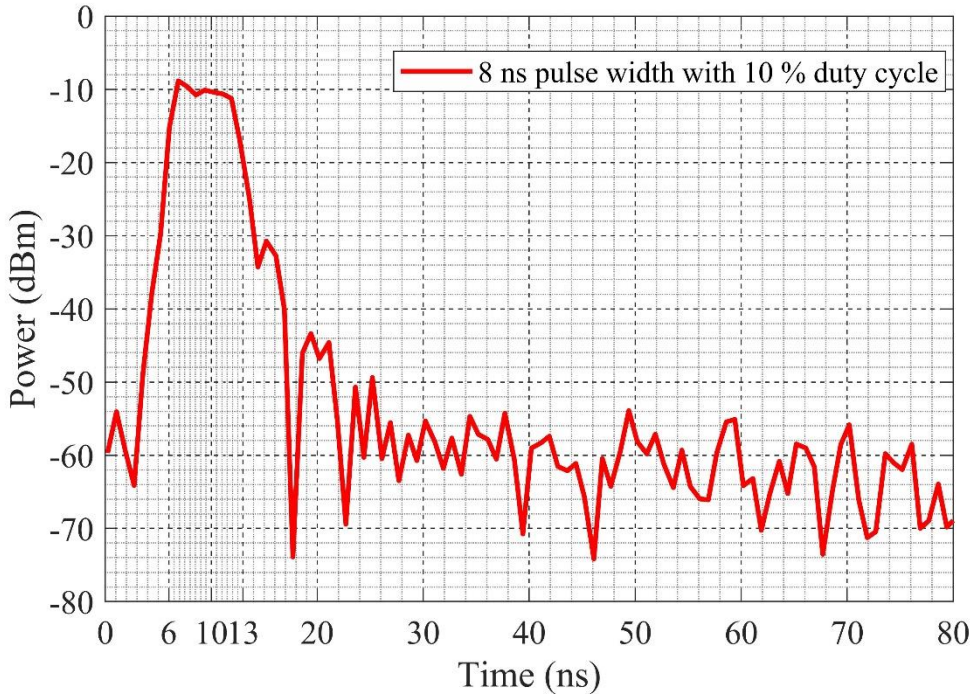

Figure 3-26: Narrow pulse width accuracy, sample rate of generator and receiver = 1 GS/s, PRI= 80 ns.

Modifying the RF pulse duty cycle allows to investigate the self-heating effect on the performance of the device at different pulse width conditions, thus implementing a measurement system with a variable duty cycle is an operational way, to characterise the device. Figure 3-27 demonstrates that VSTs capability the range of RF pulses consisting of varying pulse width and duty cycles. In fact, the only limitation set for maximum pulse width and the duty cycle is the finite high-speed memory storage within the system.

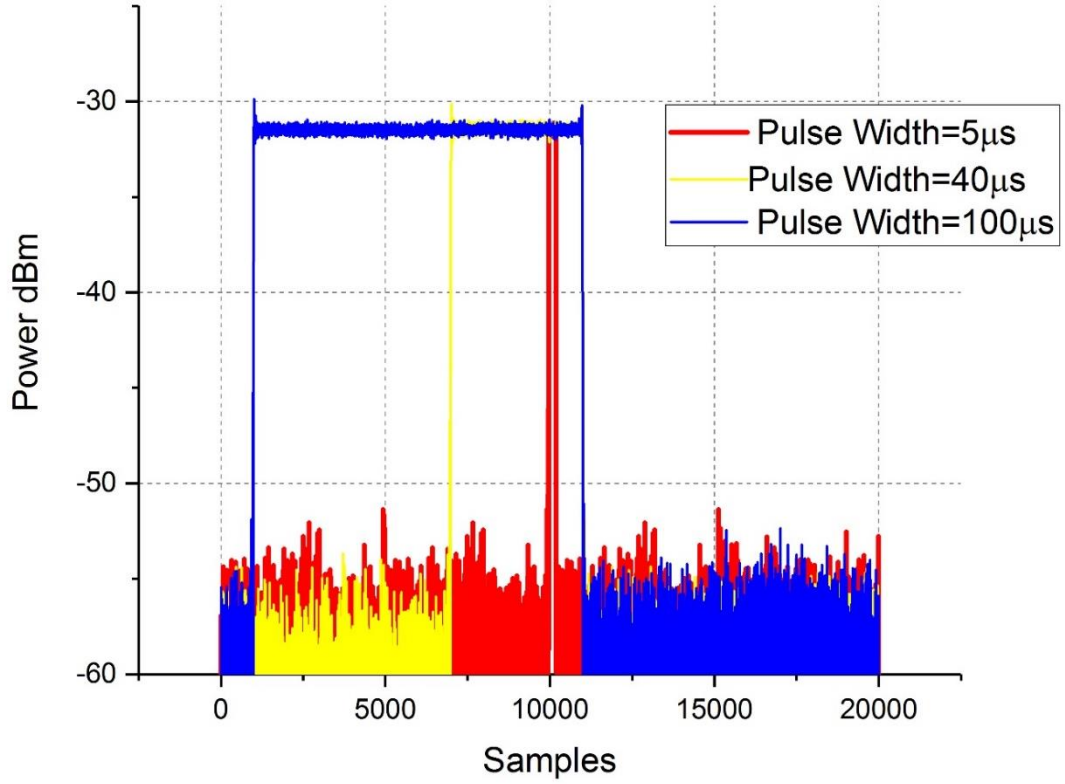

Figure 3-27: RF pulses with different pulse widths and duty cycles, sample rate of generator and receiver =100 MS/s,

3.10.4 MEMORY-FRIENDLY ACQUISITION

Figure 3-27 also shows the large number of samples, which acquired during RF pulse measurements and take a significant amount of memory and RAM of the processor. Memory usage is a severe limitation within the system in conducting consecutive measurements at a high sample rates, as maximum supported RAM is 24 GB within the PC-based chassis controller PXIe 8880. In pulse measurement, the off-state of the RF pulses does not contain any intended information as its key purpose is to keep the device cool. For this reason, the off-state of typical RF pulses constitutes typically more than 97% of the RF pulse signal. Only a small fraction of the off-state data shortly the falling transient is considered to include useful information about the

device. To minimise the storage of irrelevant data the concept of acquisition windows, that are separately defined and setup for the VST receivers. This allows for the acquisition process to be focused on information of interest only. As mentioned in the synchronisation and triggering section, the start of the acquisition controlled by a dedicated trigger, which initiates a user-defined acquisition window that can acquire data at different time-slots of the pulse. Moreover, the number of acquisition windows can be set by the user to record all the intended parts of the pulse. For instance, it allows for the acquisition to focus on the start and end of the RF pulse and disregard the more constant and repetitive device performance in the middle of longer RF pulses. Figure 3-28 shows the recorded samples of all receivers with utilised technique, as can be compared with Figure 3-27. The acquisition is carried out at, the same 100 MS/s sample rate that typically is used in this thesis. A generated signal with a 10 ms pulse repetition interval (PRI) and 3 % duty cycle would produce, 4 million samples per pulse duration. However, when employing the acquisition window technique, only 120 k samples need to be saved and processed. This technique leads us to decrease the memory usage of the system from 32 Mbyte to 0.96 Mbyte for performing one measurement of a single RF pulse. This reduction has been achieved by focusing only on information-bearing sample and will scale with an increasing duty cycle by $\frac{1}{duty\ cycle}$.

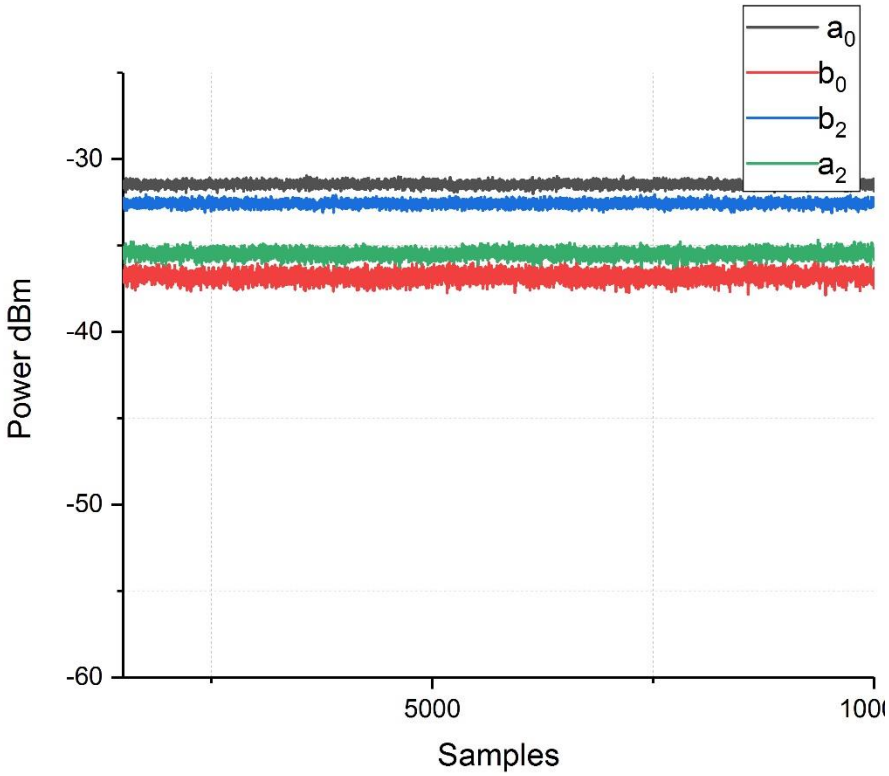

Figure 3-28: Recorded data in specific part of pulses from all receivers, to show the reduced amount of recorded samples in comparison with normal acquisition of pulse

3.11 VERIFICATION OF MEASUREMENT SYSTEM

Calibration applies to raw data that has been delayed and attenuated by imperfect passive elements of the test-set [12]. In nonlinear measurement systems, obtaining the absolute power calibration of each receiver, is important key, thus an absolute two-port calibration [13] has been implemented within the control software of designed measurement system. Embedding and de-embedding routines are also included to extract information of package and intrinsic device planes. The reference planes of calibration can be move towards the device using various calibration techniques that are explained in detail in [14], which has been implemented within the control software for an NI-based VSG-VSA system. The calibration routines have been

expanded to allow for the calibration of the NI VST-based system, which can be now carried out using CW and pulsed RF signals.

3.11.1 RECEIVER PHASE CALIBRATION

Due to the difference in signal paths of the LO, the ADC sample clock and different internal temperature for each receiver, sharing common LO and a common reference clock does not guarantee sufficient phase coherence between receivers [15]. To combat this problem, receiver calibration is designed and applied to the receivers [14] to extract the relative phase relation between receivers. In this calibration the recorded phases from all receivers are compared with a reference receiver, in our case it is the fifth receiver VST5. Figure 3-29 demonstrates the details of receiver calibration measurement setup. Figure 3-30 shows the relative phase relations between the VSTs over a 1-6 GHz frequency range. The phase rotation signifies a subsampled dataset due to the finite centre frequency resolution.

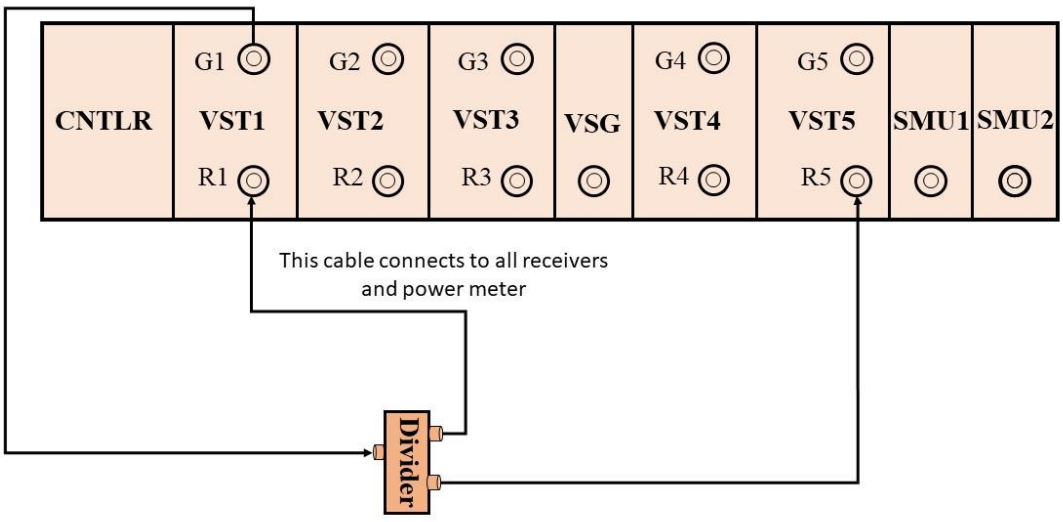

Figure 3-29: Connections of test set in receiver calibration, to measure the delay between the received signals at all receivers.

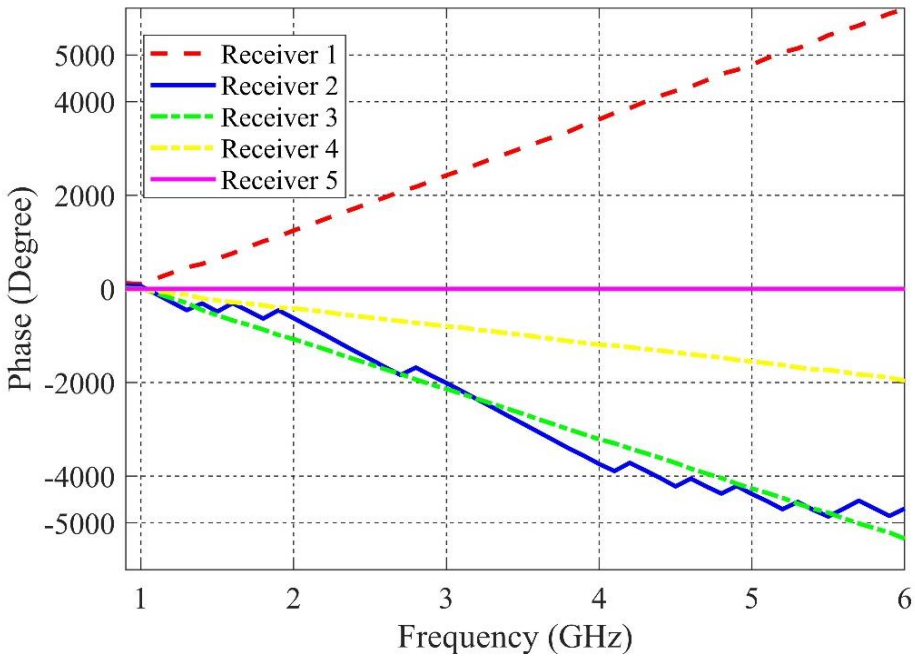

Figure 3-30: Phase relation between receivers, when receiver 5 is the reference receiver.

Moreover, within this calibration, power alignment between the receivers and power meter is achieved. Figure *3-31* compares the power of the VSTs and power meter reading for aforementioned frequency range. As can be seen the power difference varies up to 3 dB.

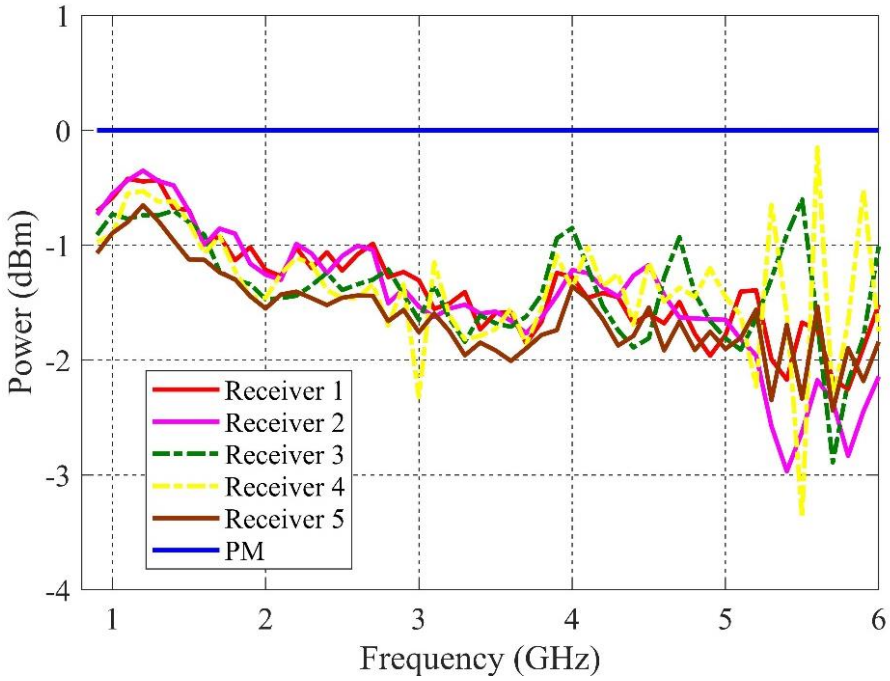

Figure 3-31:power alignment between receivers and power meter

To verify the accuracy of the performed calibration in PXIe-5840 system, some of the small and large signal calibration results are shown in this section. This calibration also considers the attenuation at all receiver paths and take them into account.

As explained, this calibration is carried out to measure the phase relation between receivers and extract power alignment between them, thus type of excitation signal is not important and does not have any difference to apply pulse or CW signal to perform it.

3.11.2 SMALL AND LARGE SIGNAL CALIBRATION

TRL (Thru, Reflect, Line) calibration is conducted over the frequency 1 to 5 GHz.

Small-signal and extended calibration are carried out to measure the error coefficients of test-set. Detailed explanation about conducted calibration is provided in [14].

Firstly, TRL calibration is conducted with pulse and CW RF signals to show the impact of different types of stimulus on the error coefficients of the test-set. Figure 3-32 indicates the differences of achieved error coefficients of the test-set under pulse and CW conditions. One set of error coefficients are measured under CW condition and another one are measured while RF pulsed signals with 5 % duty cycle and 300 µs pulse width are applied to test-set and Δe shows the deviation of error coefficients under pulse and CW conditions. The negligible amount of each Δe clarifies, test-set response is independent from applied signal's type. In fact, it is expected to observe this behaviour as during calibration, all measurements are performed on passive devices (Thru, Short, Line) and their response are independent from applied signal. Moreover, to verify the applied calibration, its output for calibrated short and line are presented in Figure *3-33* at both pulse and CW conditions, which shows applied measurements are calibrated the test-set correctly.

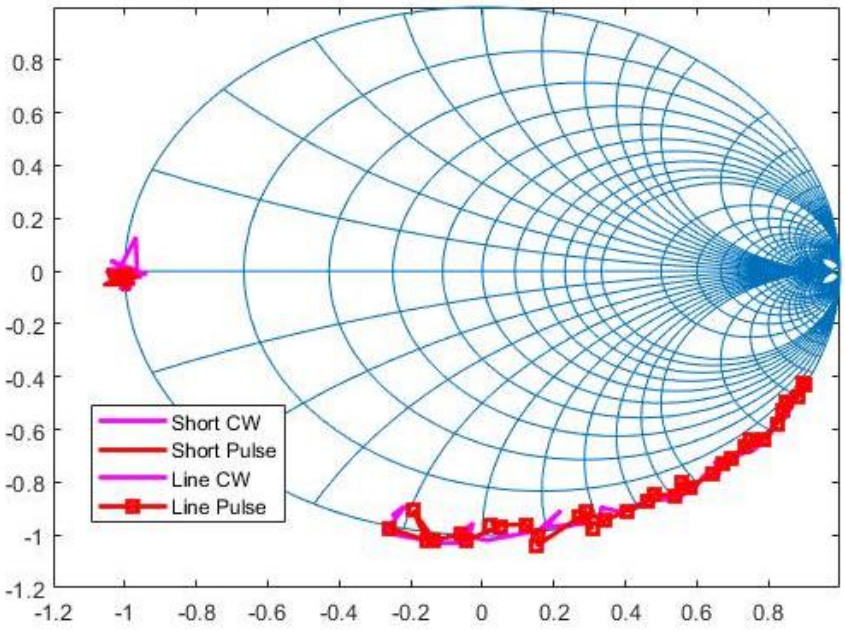

Figure 3-32: Short and line result of pulse and CW calibration, sample rate=100 MS/s, sample per average= 15 K, P_{in}= 5 dBm, in pulse mode, PW= 300 µs, duty cycle= 3 %.

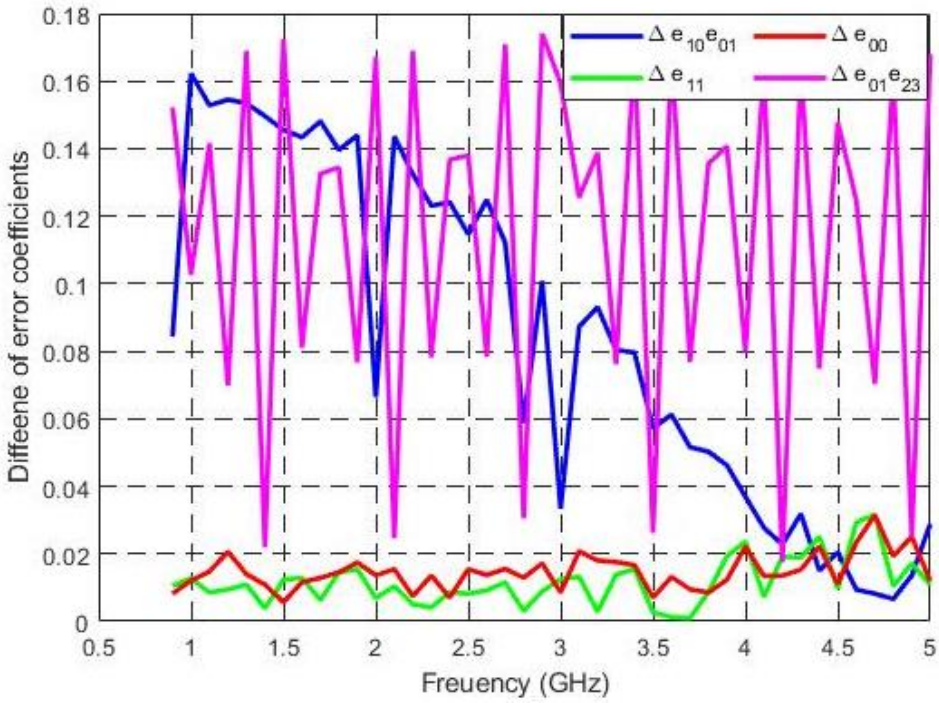

Figure 3-33: Error coefficients of test-set under pulse and CW conditions, sample rate=100 MS/s, sample per average= 15 K, P_{in}= 5 dBm, in pulse mode, PW= 300 µs, duty cycle= 3 %.

3.12 MEASUREMENT SYSTEM PERFORMANCE

To assess the system's performance and to evaluate its adaptability, quality of the measured data, dynamic range, standard deviation, noise floor and the quality of the samples distribution, were performed and results are illustrated in this section. Measurement procedure of each performance metric is also listed.

3.12.1 NOISE FLOOR OF THE MEASUREMENT SYSTEM

Assessing the noise floor of the measurement indicates the lower boundary of accurate measurements and it becomes more important for investigating the intermodulation distortion (IMD) of the device, as higher IMDs are close to the noise level of the measurement system. Hence, to analyse the IMDs and determining them, noise floor of the measurement system should be evaluated.

Pulsed two-tones measurements with 3 % duty cycle and 300 µs pulse width are performed on the 4 W GaN device and spectrum of the output of the device is shown at Figure *3-34*. It depicts two-tone measurements with a 0.5 MHz and 10 MHz tone spacing when the first tone is 1.4 GHz. The signal with the lower bandwidth was sampled at 10 MS/s with 600 samples per measurement using a 60 µs acquisition window. The resulting noise floor is below -65 dBm. For the second signal, a sampling rate of 200 MS/s is set with 12 k samples and a 60 µs long acquisition window. As can be seen, the system allows to establish an effective noise floor below -70 dBm, which is sufficient here for the investigation of inter-modulated distortions (IMDs) up to the 7^{th} order.

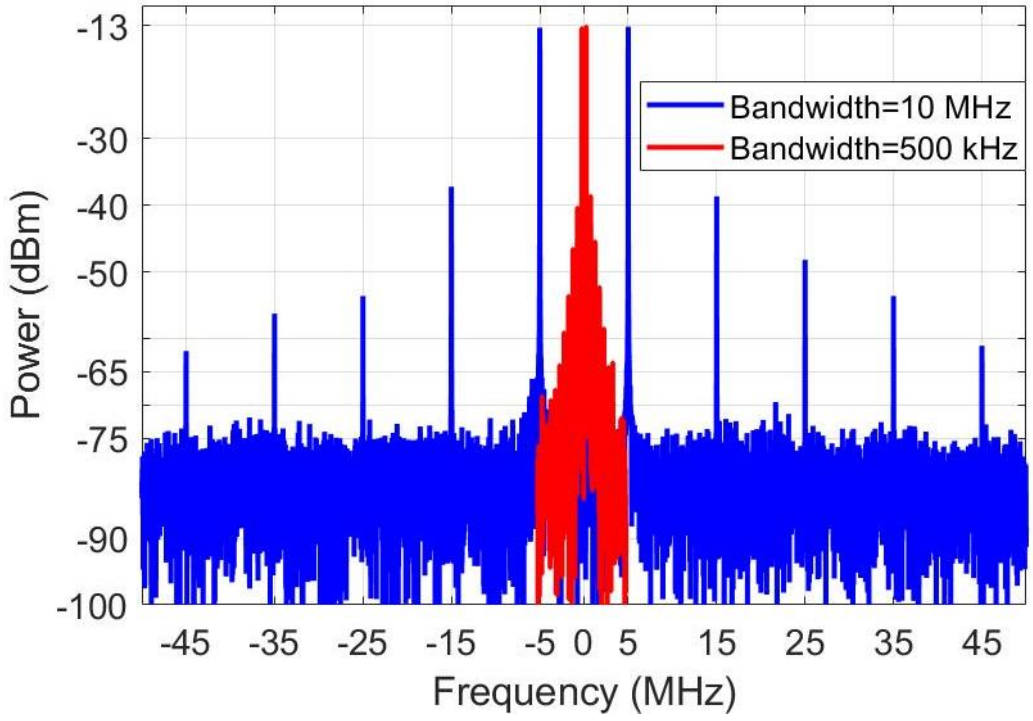

Figure 3-34: Noise floor of the measurement system with two different bandwidths, and sample rates. Sample rates= 10 MS/s, bandwidths= 0.5 MHz, 10 MHz, PW= 300 µs, duty cycle = 3%, 4W device, bias point= (-1.6 V, 40 V), acquisition length= 60 µs.

Noise floor of the measurement system is dependent on the sample rate and sample per average. Figure 3-35 investigates the relation of the noise floor, sample rate and

sample per average. Sample per average effect on noise floor is driven while sample rate is fixed at 200 MS/s and for measuring sample rate impact on noise floor sample per average is 12 k. To measure the noise floor, input power of applied pulsed two-tone signal is decreased, and spectrum of the signal is analysed to find the minimum power which can be meaningfully detected from the other terms at the spectrum of the device. It expresses for increasing sample per average the declining noise level of the measurement system which is in line with theory as noise power decreases by factor of $\frac{1}{n}$ or $10 \times \log(n)$ where n is sample per average. Moreover, increasing the sample rate by fixing the number of the samples per average, produces a higher noise floor and decreases the accuracy of measurement. Both curves show that ultimately the accuracy of the measurements is determined by the time over which a single measurement is carried out. The total measurement time can be increased if the objective of measurement is close to noise floor, thus by averaging the measurement results accuracy of the system can be increased. The graph below demonstrates that the averaging for the measurement system has been implemented correctly.

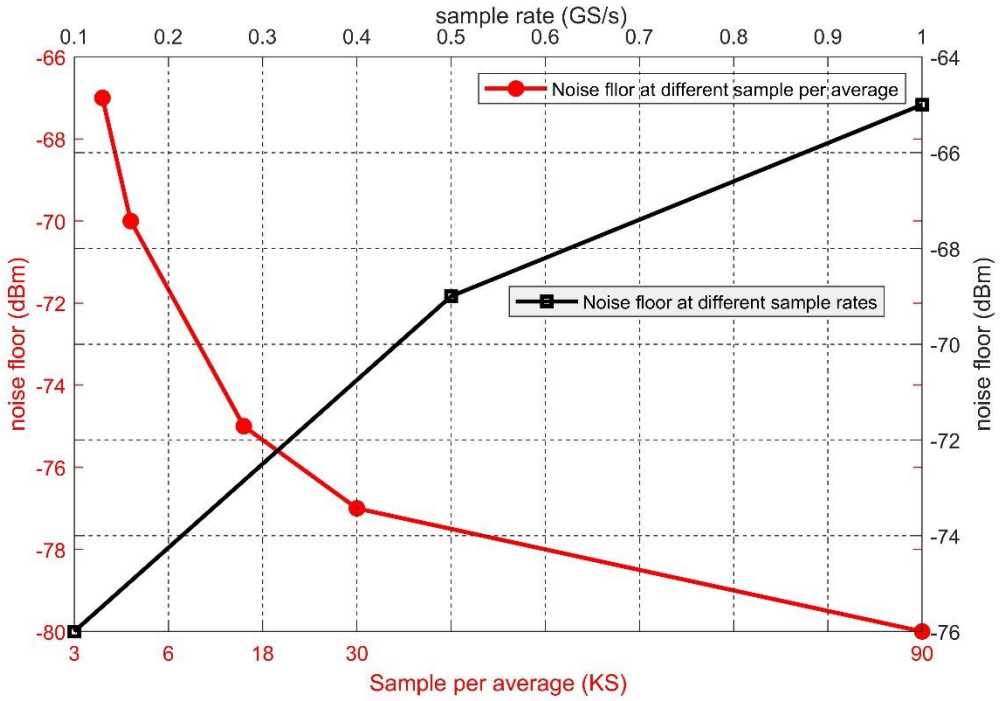

Figure 3-35: Noise level at different sample per average, bandwidth = 10 MHz, pulse width= 300 µs, duty cycle= 3 %, sample rate= 200 MS/s and sample per average =12 k, 4W device, bias point= (-1.6 V, 40 V), acquisition length= 60 µs.

3.12.2 STANDARD DEVIATION OF THE MEASUREMENT SYSTEM

The standard deviation is a measure that is related to the measurement noise floor that can be readily determined from acquired samples that are obtained when performing averaged measurements. It has been determined while measuring the fundamental CW output of a 4 W GaN device. All other settings are the same as applied measurements at the previous section. In this case the sampling rate has been varied from 100 MS/s to 1.2 GS/s, which results in a drop from -65 dB to -55 dB if the number of averages per measurement remains fixed (6 kS), i.e. the acquisition window is continuously shortened. This change in noise floor and standard deviation can be controlled or even compensated by the choice of samples-per-measurement. Figure 3-36 demonstrates this by varying the number of samples per measurement from 2 k samples to 21 kS,

however, the standard deviation remains constant over the entire range of utilised sampling rates.

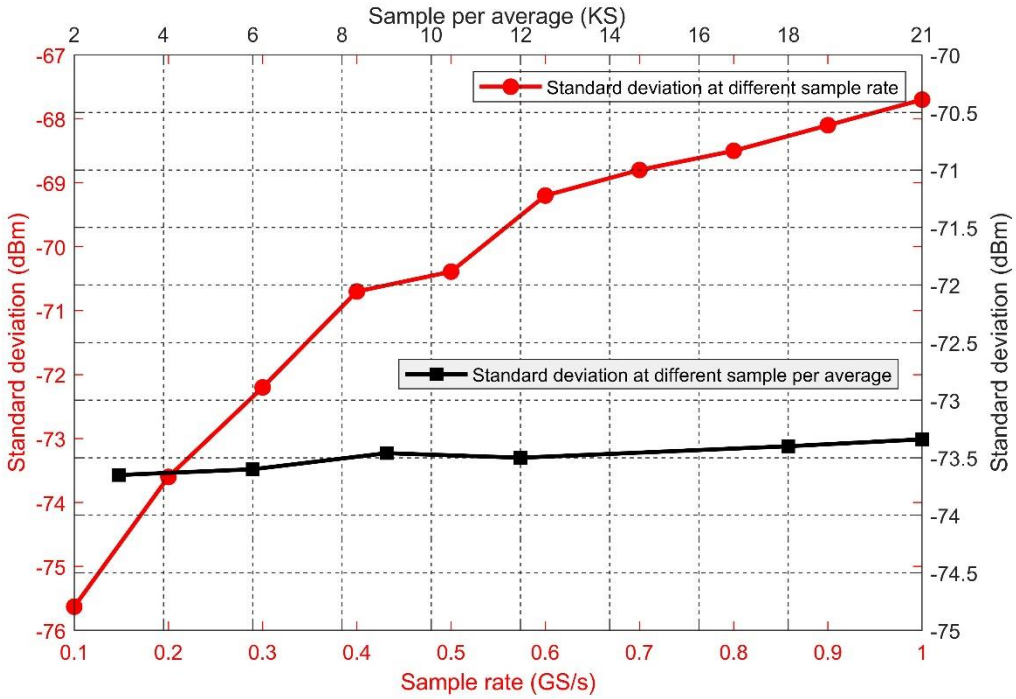

Figure 3-36: Standard deviation of system under pulsed condition. CW signal frequency= 1 GHz, pulse width = 300 µs. sample per average =4 kS with varying sample rate, sample rate:200 MS/s with varying sample per average.

This agrees well with the theory because an increase in averaging does not decrease the noise floor but allows for a more accurate cancellation of the noise contributions contained within each measured sample. The impact of the IQ sampling rate on the measurement system was also assessed. Assuming a constant noise power spectral density, the noise in dB should rise with the instantaneous measurement bandwidth (BW) by $10 \times log10\,(BW)$. Therefore, a drop from 1 GHz to 100 MHz should improve the signal-to-noise ratio (SNR) by about 10 dB. This lines up well with the depicted measurement results.

3.12.3 DYNAMIC RANGE

The dynamic range of presented measurement system has been evaluated. Regarding the dynamic range, five harmonics of the 10 W Cree device have been measured over an input power range of 45 dB from -25 to 20 dBm, as shown in Figure 3-37. The fundamental frequency of 1GHz and five harmonics were chosen to measure the dynamic range of the measurement system while the device was terminated into 50 Ω. The measurement result in Figure 3-37 illustrates that the dynamic range of the system approaches 70 dB.

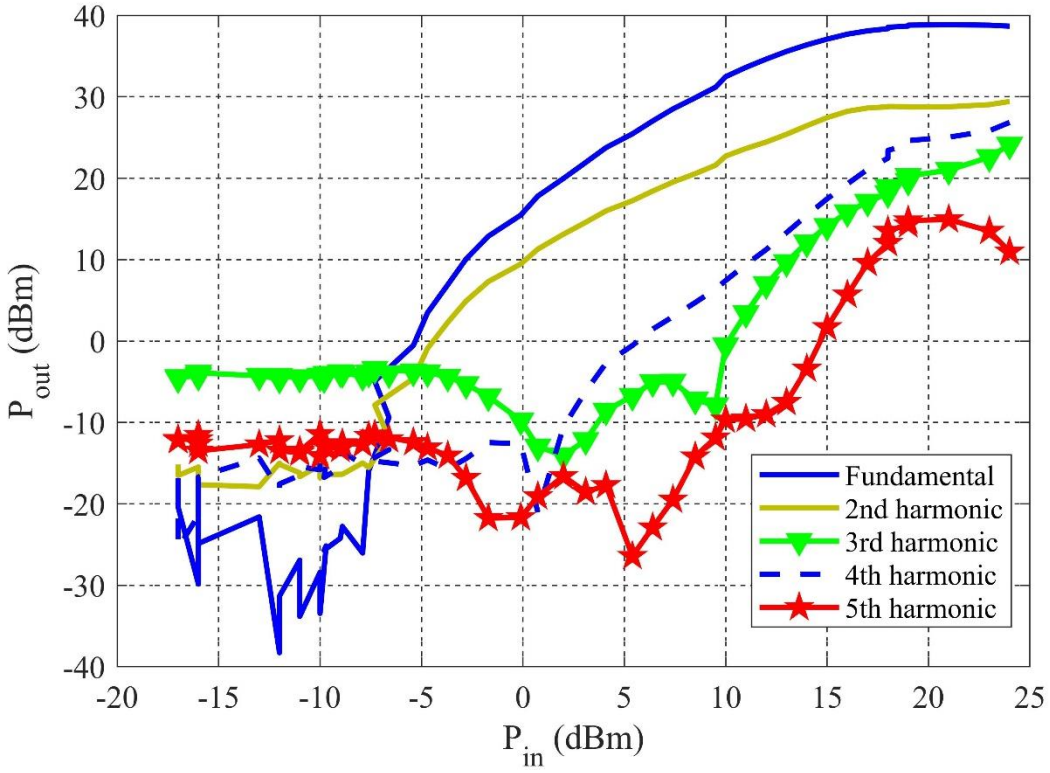

Figure 3-37:Dynamic range of measurement system, sample per average = 6 k, sample rate = 100 MS/s, PW= 300 µs, duty cycle = 3 %, bias point= (-3.5 V, 28 V), frequency= 1 GHz, 3 dB gain compression point, terminated at 50 Ω, 10 W device.

It clarifies measurement system's capability to measure accurate data over a wide range of power sweep at different frequencies.

3.13 CHAPTER SUMMARY

An advanced high-frequency measurement system that can conduct different types of measurements such as pulse, pulse profiling, CW, and multi-tone active load-pull measurements, has been presented and validated. All modules are located in a single chassis with providing accurate and efficient synchronisation and a high degree of customization. The system can readily be re-configured and delivers a high level of flexibility, which provide for a software-defined nonlinear measurement system. In addition, some important specifications of the PXIe modules are pointed out which can affect their operating mechanisms. Unique features of the developed system to perform the pulse measurements are introduced and compared with other existing pulse measurement technologies and the employed method to generate and analyse the RF pulses is presented in details. Key pulse measurements performance metrics such as pulse-to-pulse stability, RF and DC transient time, and nano-second pulse-width accuracy are evaluated to express the reliability of the system.

Critical metrics of the measurement system have been assessed, to ensure the measurement system is accurate measurement boundaries.

All applied calibration to the receivers recorded samples are shown to verify the measurement's result from 1-6 GHz. The phase relation between different receivers is extracted by applying the receiver calibration then, TRL and extended calibration change the calibration plane to the device packet plane and account for the phase rotation and attenuation produced by the test-set. Furthermore, the designed RF test-set has been explained and its components are introduced. It can deal with up to 100 W devices and can characterise baseband, fundamental and second harmonic of the device. The developed test-set is designed to minimise the usage of cables and

connectors to reduce the phase-rotation and loss. A PRS is designed and developed and calibrated to provide harmonic investigation and extracting the phase difference between fundamental and harmonics of the device.

3.14 REFERENCE

[1] Y. Alimohammadi *et al.*, "Pulse Profiling Active Load Pull Measurements," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020: IEEE, pp. 759-762.

[2] P. J. Tasker, "Practical waveform engineering," *IEEE Microwave Magazine,* vol. 10, no. 7, pp. 65-76, 2009.

[3] N. I. (NI). "NI PXIe-1085 Series User Manual." (accessed 06-2018.

[4] N. I. (NI). "NI PXIe-8880 User Manual." National Instruement. (accessed 03-2015.

[5] N. I. (NI). "SPECIFICATIONS PXIe-5840." National Instrument. (accessed 06-04-2020.

[6] N. I. (NI). "SPECIFICATIONS PXIe-5652." National Instrument. (accessed 22-09-2020.

[7] N. I. (NI). "SPECIFICATIONS PXIe-4139." National Instrument. (accessed 30-11-2020.

[8] N. I. (NI). "NI PXI Timing and Synchronization Design Advantages." National Instrument. (accessed 04-12-2020.

[9] C. Rauscher, V. Janssen, and R. Minihold, *Fundamentals of spectrum analysis*. Rohde & Schwarz, 2007.

[10] "Keysight Technologies Pulsed-RF S-Parameter Measurements with the PNA Microwave Network Analyzers Using Wideband and Narrowband Detection," Keysight Technologies, 2014.

[11] Rohde&Schwarz. "Easy measurement of radar pulse stability." Rohde&Schwarz. (accessed.

[12] D. M. Pozar, *Microwave engineering*. John wiley & sons, 2011.

[13] J. Benedikt, R. Gaddi, P. J. Tasker, and M. Goss, "High-power time-domain measurement system with active harmonic load-pull for high-efficiency base-station amplifier design," *IEEE Transactions on Microwave Theory and Techniques,* vol. 48, no. 12, pp. 2617-2624, 2000.

[14] T. Husseini, "On the development and automation of a high-speed load-pull system based on Pxie modules," Cardiff University, 2018.

[15] D. Hall, A. Hinde, and Y. Jia, "Multi-channel phase-coherent RF measurement system architectures and performance considerations," in *2014 IEEE Military Communications Conference*, 2014: IEEE, pp. 1318-1323.

CHAPTER 4: TIME VARIANT LINEARITY AND OUTPUT POWER OF GAN DEVICE

4.1 INTRODUCTION

As Time Division Duplexing (TDD) access to channels in modern wireless communication systems is becoming prevalent in areas with limited frequency spectrum, it is of growing importance to characterise and understand dynamic RF changes that are introduced by the RF pulses and used for establishing bidirectional, i.e. duplex, communication. The resulting gain in information can then serve to identify ways forward for optimizing their performance under pulsed RF conditions. Envelope-domain characteristics of the GaN devices, illustrate the variation of the output of the device at DC and fundamental frequencies [1, 2] for varying RF signals. Figure 4-1, shows the variation of the output of the device, that can change the large-signal behaviour of the device and can lead to a decrease in the optimum performance of the device.

Different phenomena can be the reason for the observed variation in the time-domain behaviour of the device, such as trap charging level, thermal and self-heating effect.

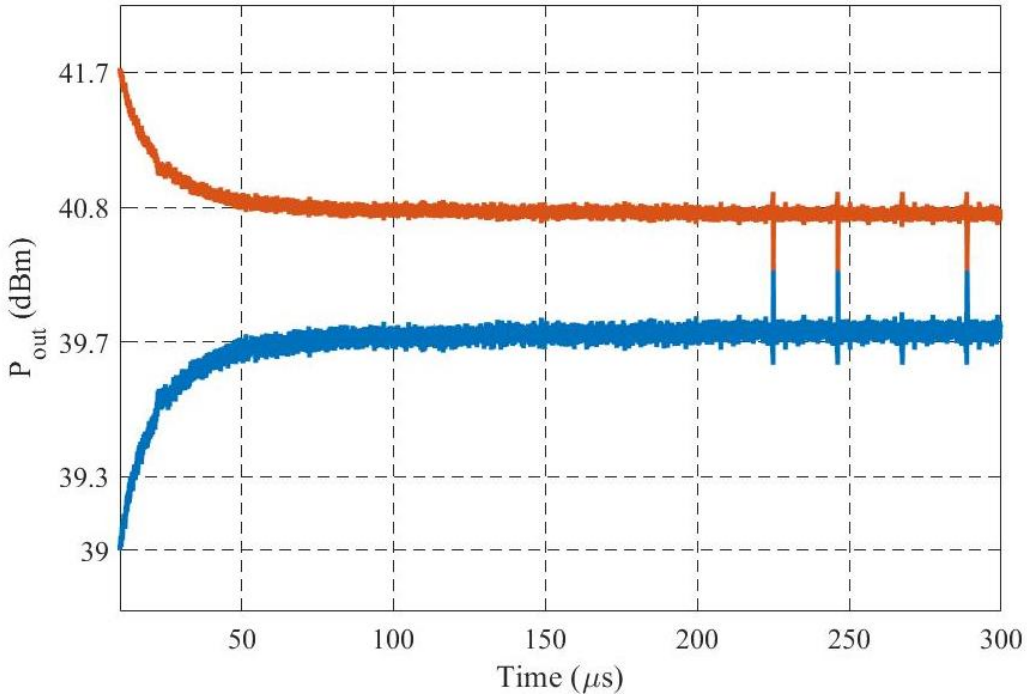

Figure 4-1: Measured output of the 10 W device in time-domain at 1 dB and 3 dB gain compressions, sample rate=100 MS/s, terminated at 50 Ω, bias point= (-3.5 V, 28 V), frequency= 1.4 GHz, PW= 300 µs, duty cycle= 3 %.

In physics of the device, traps restrict the movement of electrons and holes and they are distributed within a semiconductor, and classified to donor and acceptor types based on their behaviour in accepting and releasing carrier to the channel [3]. They affect the output current of PA by capturing (emitting) the electrons from (into) the channel. Their activation occurs within different timeslots of the applied signals and there is a difference between charging and discharging process. Therefore, at the start of an RF pulse when the traps of the device are not charged and the device is in cold condition, the output of the device starts from a higher level and only after a few hundred micro seconds the device response can be assumed in a steady-state condition producing constant output as can be seen in Figure 4-1 after about 60 microseconds, output of the 10 W GaN device is in steady-state condition. However, the specific

establishment of the constant power levels device varies, and varying between a fall, rise or a constant output power level within an RF pulse.

Figure 4-2 illustrates the cross section of the device with traps, as various trap centres exist in the buffer layer of the transistor and their time constants are different, then during applying RF stimulus to the device, as the applied voltage varies fast, thus, traps charging level can vary over time. Due to the wide range of traps' time constants the device output behaviour can be affected over a wide range of frequencies, thus the trapping effect not only changes the DC-IV characteristics of the device but also can change the RF performance of the device from DC to fundamental [4]. Analysing the trapping effect on RF performance metrics of the device such as output power, linearity, and intermodulation distortion levels (IMD) can be beneficial for RFPA designers, and provide valuable information for the design and development of RF devices. Therefore, it is essential to develop a measurement system to characterise the aforementioned behaviour of the device and conducting the complex measurements at higher frequencies.

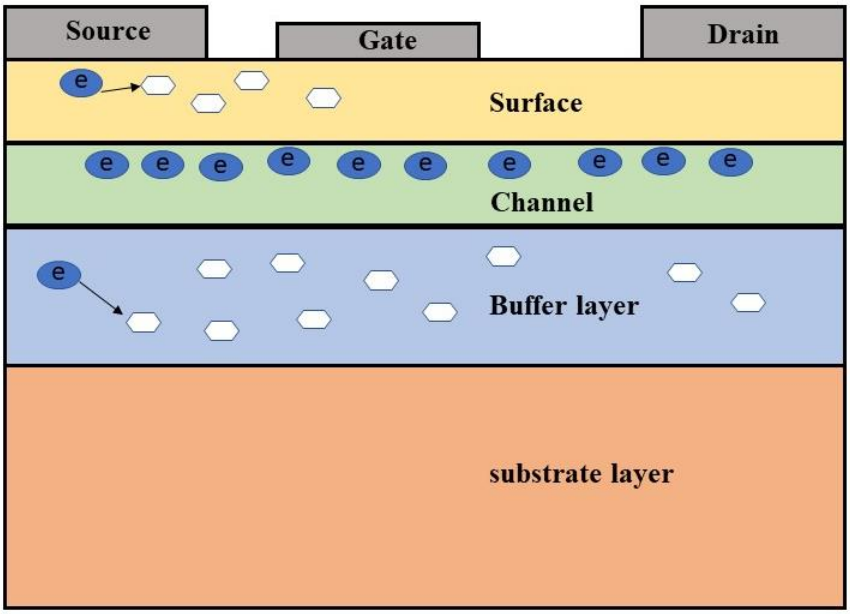

Figure 4-2: Schematic representation of the device. Size of different regions are not scaled for illustration.

This chapter aims at utilizing the new measurement system for the characterisation of RF device behaviour under pulsed RF stimulus utilising a combination of pulsed DC, pulsed RF and pulsed load-pull measurements. The correlation between the established and reliable pulsed DC measurements and the new pulsed-RF and pulsed load-pull measurements will be used to verify the new measurement system. A further verification will be established through comparisons with previously reported pulsed-RF data. To demonstrate the capability of the new measurement system new characterisation technique are developed with the objective to shed new light on traps and their impact on device behaviour. In conjunction with these characterisations a novel technique will be investigated allowing to mitigate the effects of device traps by utilising the slow discharging processes associated with deep-level traps within the buffer or substrate as a new operation regime for pulsed-RF PAs.

In this chapter, procedure of conducted measurements is explained in detail, then DC characteristics of 4 W and 10 W PAs are provided to illustrate, how traps of the device

react while operating the device at different output power regimes and how the DC-IV characteristics of the PA varies in time-domain under various pre-charging levels. These data are also used to verify the further observation of RF pulsed and RF pulsed load-pull measurements. As developed measurement system allows to perform RF measurements at different timeslots of pulse, this unique feature is used, for the first time, during conducting active load-pull measurements to track the optimum load impedance of the PAs within the RF pulse [5] and track the important large-signal performance metrics of the PA such as output power, source impedance (Γ_{in}) in optimum load condition. During aforementioned measurements various gate-lag and drain-lag levels are applied to the PA to measure traps effect on the load optimum and input impedance variations.

Employing developed measurement system under pulsed multi-tone condition, provides capability to investigate the traps effect on the linearity of the PA. In-band and out-band linearity of the device are investigated over a 15 dB input power dynamic range by applying different drain-lag levels to the PA. Moreover, novel measurements are designed to measure the variation IMDs of the device in time-domain up to 7^{th} order.

Based on the measured behaviour of the PA by pre-charging the traps variation of the input and output of the device degraded, and device linearity improves. Therefore, the pre-charging technique is proposed as an approach to tackle the losing performance issue in this chapter.

4.2 MEASUREMENT PROCEDURE FOR PULSED STIMULI

In this chapter, different types of pulse profiling measurements are performed at various drain-lag, gate-lag, and package temperature levels. To perform pulse profiling measurements, instead of measuring the whole of the pulse width, two acquisition windows are set to start and end of the pulse to record 60 µs at different sections of the pulse, although, the RF acquisition window can span the entire pulse duration, which results in a significant amount of measured data. To exclude the generators power settling ripples, a 10 ns delay is considered at the start of the pulse for receivers to start the acquisition.

The device is biased in pulsed condition by applying two pulses to the input and output of the device. V_{GS} pulse width is set to 420 µs and the duty cycle is 4.2 % and V_{DS} pulse width and duty cycle are 360 µs and 3.6 %, respectively. These values for pulse widths of DC & RF signals let us to analyse slow mechanisms in PA. 30 µs delay considered between DC signals and RF pulses, to eliminate the DC transient time's effect and have stable I_{DS} after biasing the device. The observed behaviour at the start of the pulse is not affected by variation of the DC signal and comes from applying the intended RF signals. Figure 4-3 represents I_{DS} and V_{DS} variation in time-domain once pulsed RF is applied to PA. As it shows by considering 30 µs delay between RF and DC pulses, DC signals impact on I_{DS} is disappeared and our observation at start of the pulse relates to RF pulses impact on device. Figure 4-4 shows the device state transient diagram during the pre-bias and bias conditions. During the gate-lag and drain-lag investigations, traps of the device are charged by pre-pulsing signals. Pre-V_{GS} is set to less than pinch-off voltage, to keep the device in cool condition while charging the traps. All timing parameters and triggering of DC signals is set, to avoid producing

current before applying RF signals to it, thus in drain-lag measurements when the pre-V_{DS} is set to non-zero values, V_{DS} pulses start earlier than V_{GS}.

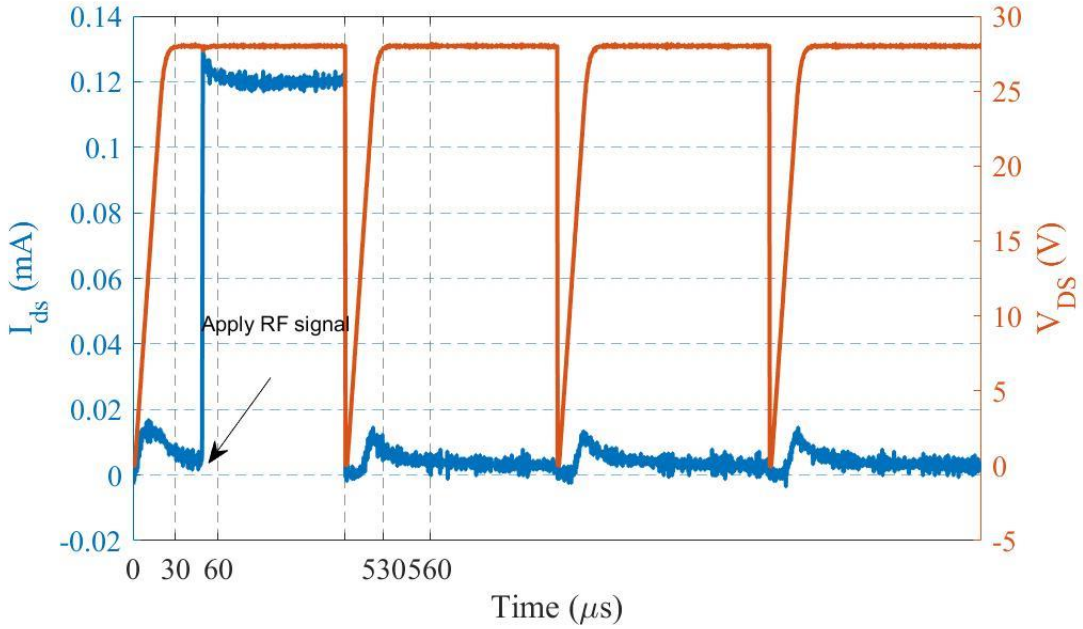

Figure 4-3:Pulsed I_{DS} and V_{DS} variation in time-domain at the presence of RF pulse. Bias point=(-3.5 V, 28 V), 10 W PA, terminated at 50 Ω, RF duty cycle 3 %, PB=(0 V,0 V).

In this chapter two different GaN devices with various design and biasing technology and manufacturer are used to investigate trapping effect and time variation of the behaviour of the GaN device. 4 W device is biased at its typical class AB bias point (BP) BP=(-1.6 V, 40 V) and BP=(-3.5 V, 28 V) is set for 10 W GaN device to have 10 mA at bias points.

Firstly, pulsed CW stimulus is applied to 2 different GaN devices (4 W and 10 W) to perform the active load-pull pulse profiling measurements, to find load optimum impedance, and analyse the input impedance of the device at each section of the pulse.

Two-tone measurements with various bandwidths are performed in pulse condition at 50 Ω load impedance to investigate the linearity of 4 W GaN device. The tone

frequency spacing is set to have the integer ratio between ΔF and pulse width. Figure 4-4 shows the structure of pulses used for both types of measurements. Most pulsed RF measurements within this work have an RF pulse width (PW) of 300 µs with a duty cycle of 3 %. Any pulse widths deviating from this value are clearly pointed out.

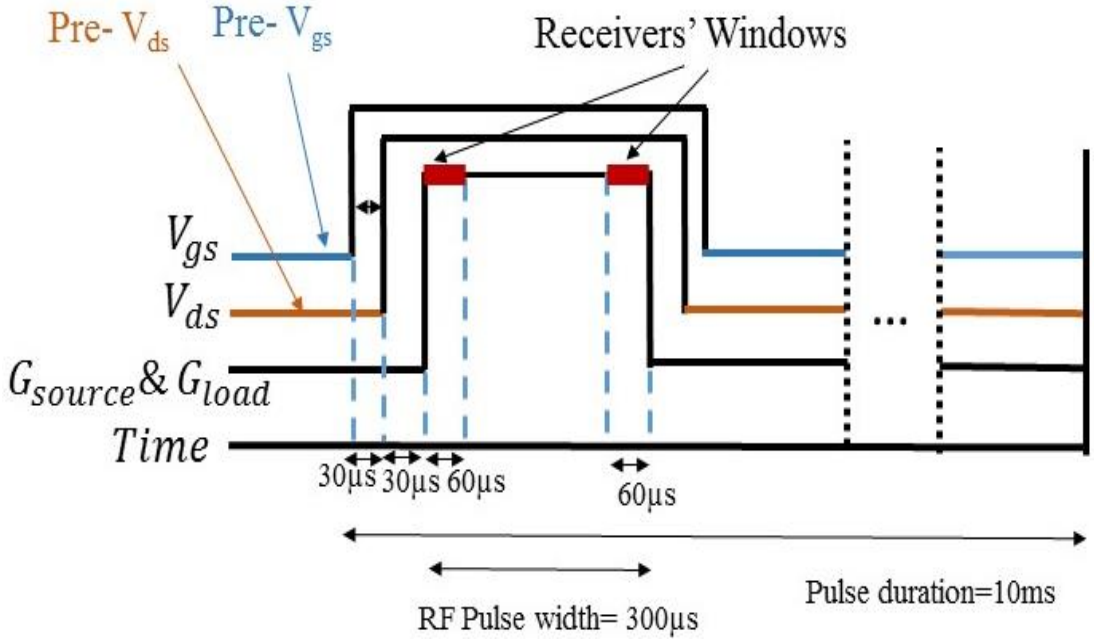

Figure 4-4: Structure of the applied pulses

4.3 CHARACTERISTICS OF UTILISED DEVICES

In this thesis, two different GaN devices with various design technologies from two different manufacturers are measured to investigate GaN devices' behaviour. This section introduces some of their key features.

10 W GaN device that is used in this thesis is the Wolf speed 10 W device, and its characteristics are listed in Table *4-1*.

Table 4-1: key features of 10 W GaN PA

Parameter	**value**
Frequency	Up to 6GHz
P_{sat}	17 W
Gain	18 dB at 2GHz
Efficiency	70 %
V_{GS}	(-10 V,2 V)
I_{DSMAX}	1.5 A
V_{DS}	120 V range
Maximum forward gate current	4 mA
Typical drain bias	28 V
Gate threshold voltage	-3 V (varies -3.6 V to -2.4 V)
Breakdown voltage	84 V

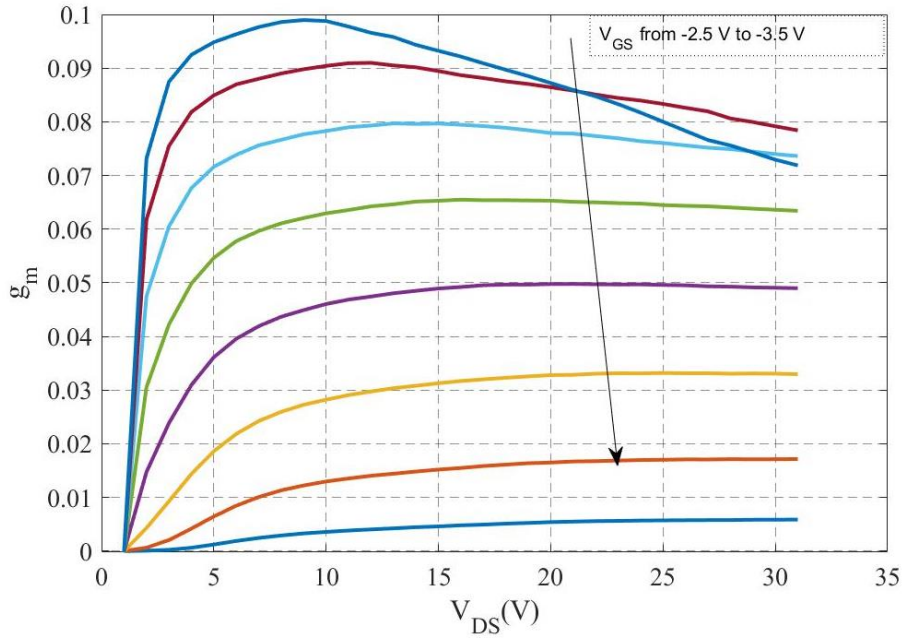

Figure 4-5: conductivity of 10 W device under pulsed condition, pulse width= 300 µs, duty cycle= 3 %.

Figure 4-5 shows g_m of 10 W device, that is derived under pulsed DC stimulus. V_{GS} is varied from -3.5 V to -2.5 V and gm variation at different V_{DS} is represented.

A 4 W GaN device with 0.5 µm gate length is used in this thesis. It is designed to operate at 40 V and its features are listed in Table *4-2*.

Table 4-2: key features of 4 W GaN PA

Parameter	**value**
Frequency	Up to 6GHz
P_{sat}	4.5 W
Gain	19 dB at 1.4 GHz
Efficiency	65 %
V_{GS}	(-10 V,2 V)
I_{DSMAX}	1.5 A
Typical drain bias	40 V

Figure 4-6 shows g_m of 4 W device, that is derived under pulsed DC stimulus.

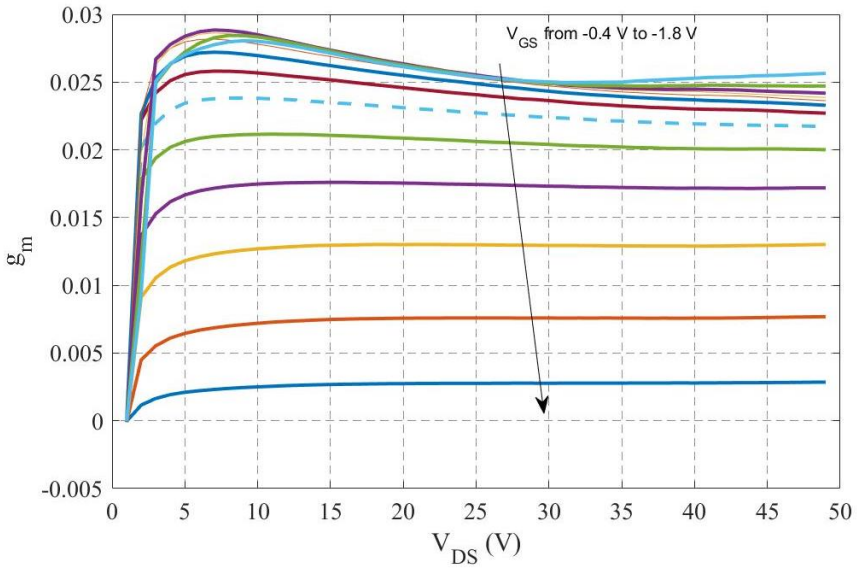

Figure 4-6: conductivity of 4 W device under pulsed condition, pulse width= 300 µs, duty cycle= 3 %.

4.4 DC-IV MEASUREMENTS AT DRAIN-LAG LEVELS

DC-IV characterisations are informative measurements to identify the operating condition of the device and measuring the boundary of the different operating regions. Initial PIVs, as shown in Figure 4-7 and Figure 4-8, are carried out on both 10 W and 4 W GaN devices to identify the knee voltage, saturated area, and pinch-off voltage. As can be seen, the knee voltage of devices are 8 V and 4 V, and pinch-off voltage of 10 W and 4 W devices are -3.7 V and -1.8 V, respectively.

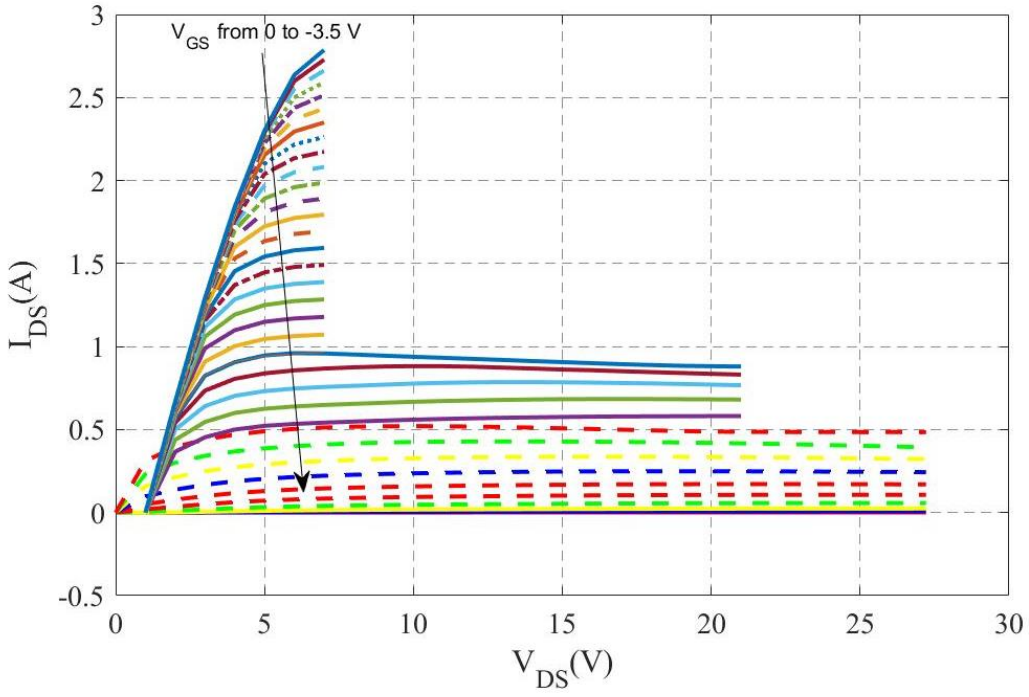

Figure 4-7: PIV characterisation of 10 W device, PW= 300 µs, drain pulse duty cycle= 3 %, terminated at 50 Ω, RF duty cycle 3 %, PB=(0 V,0 V).

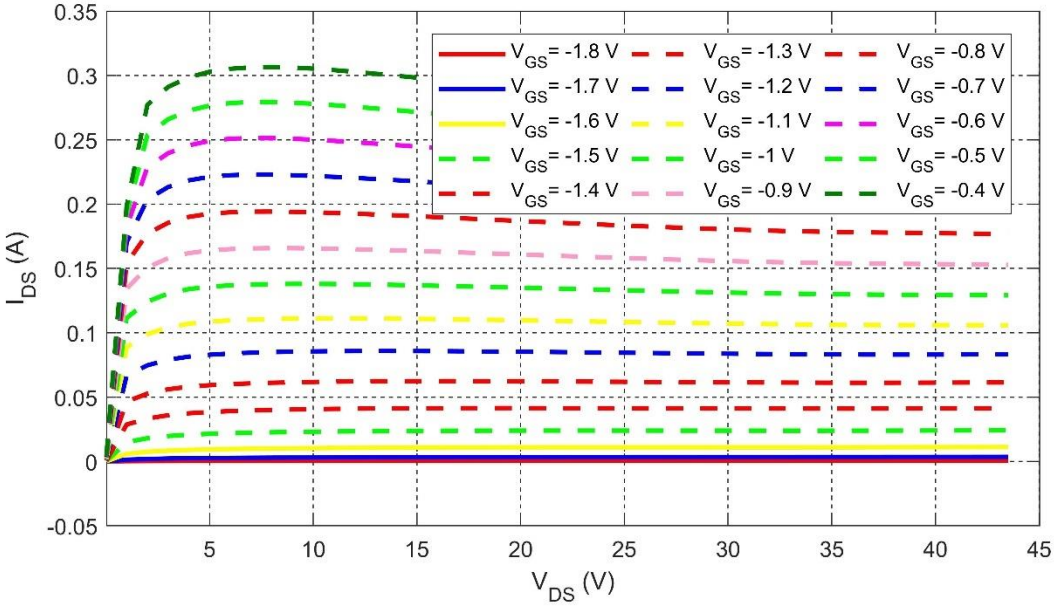

Figure 4-8: PIV characterisation of 4 W device, PW= 300 µs, drain pulse duty cycle= 3%, terminated at 50 Ω, RF duty cycle 3 %, PB=(0 V,0 V).

The impact of the pulse width on the DC characteristics of the device is represented in Figure 4-9 and carried out by applying different pulse widths to the device and recoding over the entire pulse width. Here, DC pulse widths are varied between 200 and 600 µs, while the utilised duty cycle fix at 3 %. Starting with pre-bias values of V_{GS} = 0 V and V_{DS} = 0 V, designated as the pre-bias state PB = (0 V, 0 V). Achieved result of the 4 W GaN device shows, I_{DS} decreases by around 10 mA in increasing the pulse width of DC signals, and there is a decrease of about 50 mA when device is pre-charged at PB = (-10 V, 50 V), that indicates pre-bias condition can change the initial traps level and hold it for at least 200 µs, and decrease the I_{DS} level. After 400 µs recorded I_{DS} is similar to the PB = (0 V, 0 V) condition.

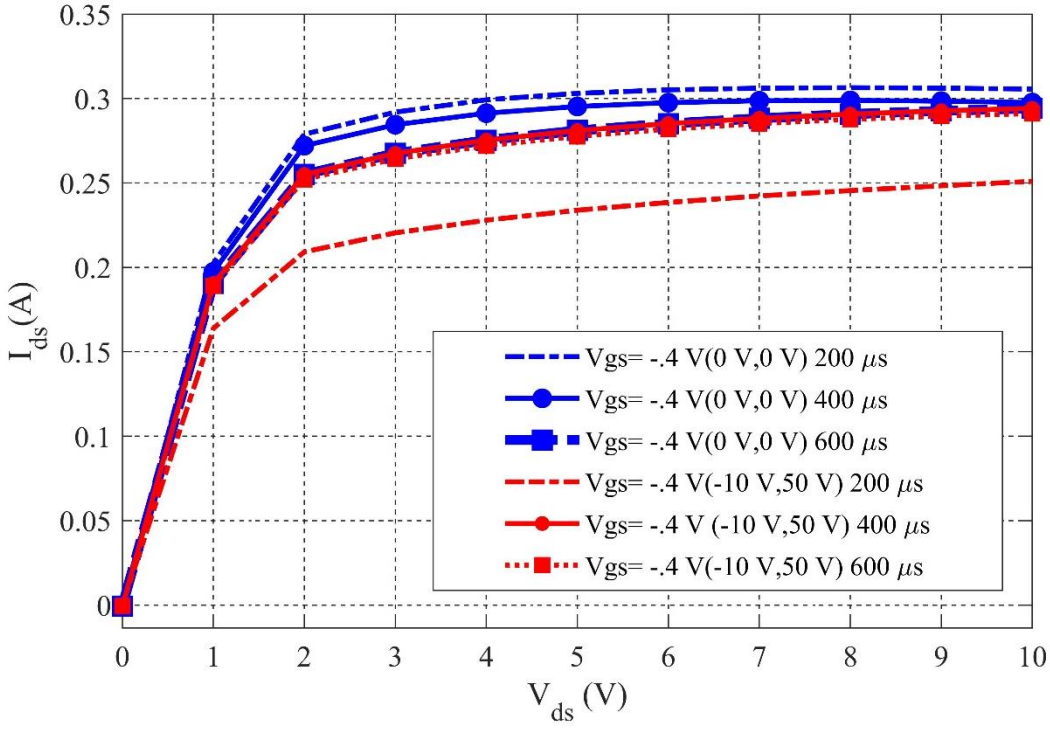

Figure 4-9: Pulse width effect on IDS of 4 W GaN device at different pre-bias conditions, duty cycle 3 %, terminated at 50 Ω.

Based on the above observation a pulse width of 300 µs was chosen in this thesis as a compromise between the maximum duration of an RF pulse and the stability of the pre-charged device regime.

Measurements in Figure 4-10 and Figure 4-11 investigate the pre-pulsing effect on DC-IV characteristics of the devices at high and low output current conditions. The high drain-lag levels cause significant variation in V_T of PA which is related to back gating and buffer layer [6, 7].

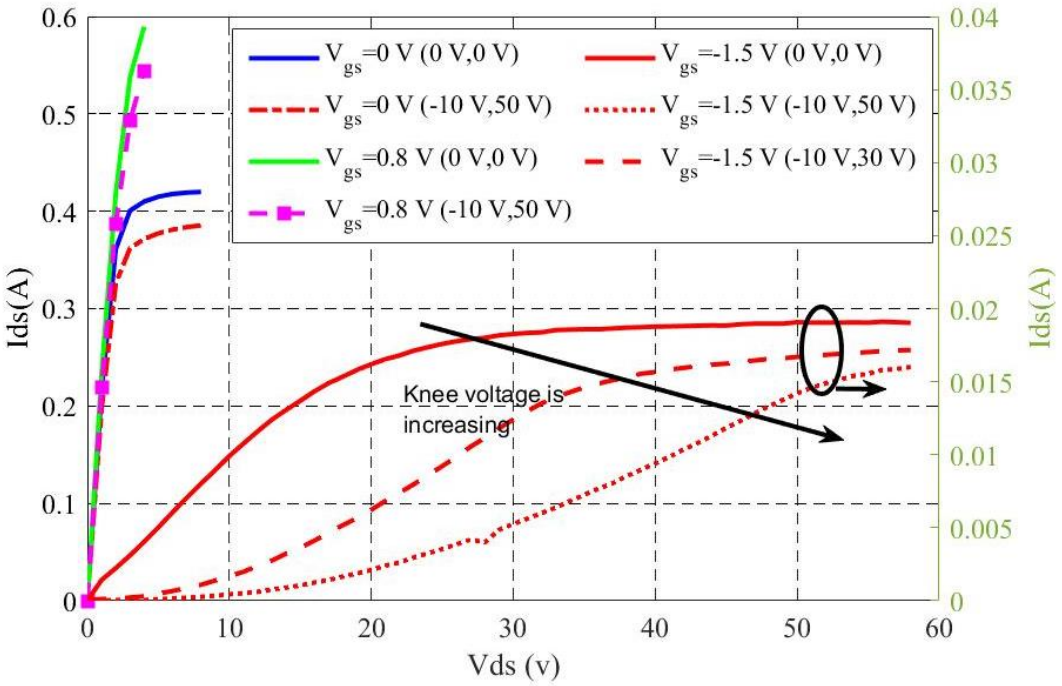

Figure 4-10: Characterization on 4 W devices showing impact of pre-charging on PIV, PW=300 µs, duty cycle= 3%, terminated at 50 Ω.

The ascertained data indicates that the pre-charged device state would affect the device performance over a large range of RF power levels. Most significant changes are to be expected at small I_{DS} values close to device pinch-off, where RF current and voltages of a class-AB PA are predominantly located during large back-off power levels.

As the duty cycle of the applied DC pulses, package temperature, pulse interval repetition (PRI) was fixed during the aforementioned measurements, thus observed changes in the behaviour of the device are related to the traps of the device as various pre-charging levels are applied to devices.

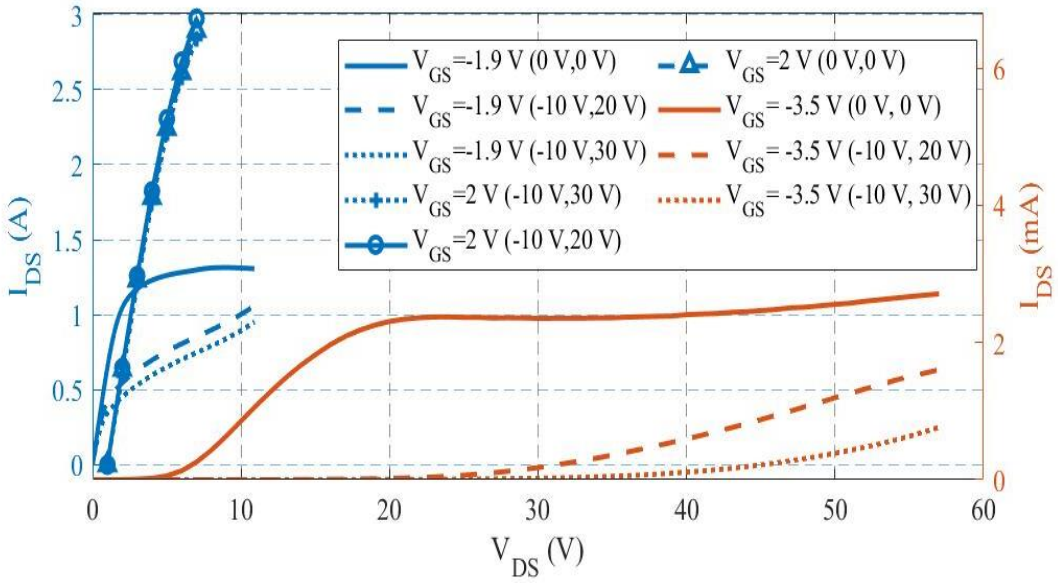

Figure 4-11: Characterization on 10 W devices showing impact of drain-lag on PIV, terminated at 50 Ω, duty cycle= 3 %, PW= 300 µs, sample rate= 100 MS/s.

DC characteristics of the devices are measured to provide deeper understanding about its behaviour over a wide range of output power regime, at different pre-charging levels. These results can be then correlated with prospective results from RF measurements to verify them. Moreover, measured behaviour of drain-lag at both devices is comparable with previously published articles and they reported a similar observation about drain-lag impact on PIV curves [8, 9].

4.5 OPTIMUM IMPEDANCE VARIATION

In this section of the chapter, a novel viewpoint in performing active load-pull measurements is presented by combining the advanced pulsed DC and RF measurements. The capability of the developed system allows to perform the active load-pull measurements in different timeslots of pulse and track the optimum impedance within the pulse, as system can define the receivers window's position and rapidly process the recorded data to find the optimum impedance.

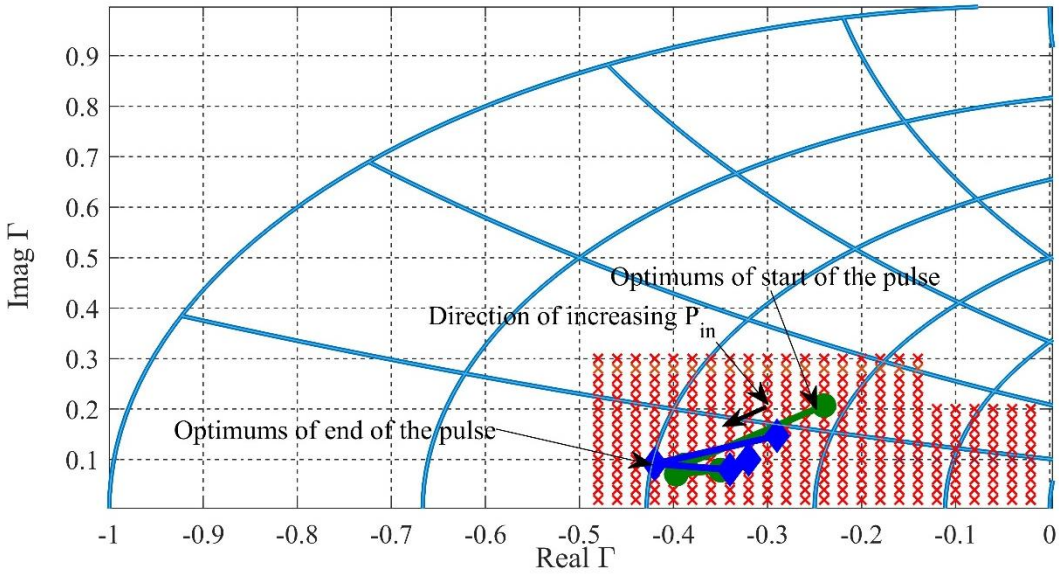

Figure 4-12: Optimum impedance variation of 10 W GaN device over 25 dB dynamic range at fundamental frequency, 10 W PA, duty cycle= 3 %, bias point= (-3.5 V, 28 V), sample rate=100 MS/s, acquisition length= 60 µs, frequency= 1.4 GHz, class AB, PW = 300 µs.

Based on Figure 4-1 output of the PA has a significant variation that can lead to change in the large-signal behaviour of the device such as optimum load impedance. Therefore, to investigate the optimum impedance of the start and end of the pulse, active load-pull measurements are performed at 1.4 GHz fundamental frequency while pulsed signals are applied to the 10 W and 4 W PAs with 300 µs and 3 %.

To perform active load-pull measurements, several sets of load impedances are considered to achieve the optimum impedance to maximize the output power of the device. Initial load-pull measurement is performed around 50 Ω load impedance and then the next set of load impedances are calculated by using the load-based Cardiff behavioural model [10], and starts from the optimum impedance of each spiral to minimize the number of measurements and increase the speed of finding optimum impedance.

The variations of the optimum impedances at the beginning and end of the RF pulse are depicted in Figure 4-12 over a range of output power levels from 15 dB back-off to 10 dB gain compression at 10 W GaN device. As can be seen, by performing load-pull measurement at fundamental frequency, while device is operated at (-3.5 V, 28 V), there is a significant difference between the load optima. This behaviour of the device not only happens at different compression levels but also occurs at the deep back-off levels. In fact, the changes seem to increase with increasing back-off. At compression levels, the output of the device interacts with the knee voltage. Thus, it leads to have a variable P_{out} over the pulse, and the same behaviour is reported at [6]. In the back-off condition, the output of the device varies within the pulse due to threshold voltage changes. As the bias point is in the deep class AB mode (V_{GS}= -3.5 V, V_{DS} =28 V), the RF drive signal at back-off is exposed to a strong interaction with the threshold voltage (V_T) causing this nonlinear behaviour. Moreover, the illustrated results in Figure 4-10 from PIV curves confirm the threshold variation in the low power regime can cause the optimum impedance variation in the device.

Figure 4-13 shows the deviation of the Γ_{opts} ($\Delta\Gamma_{opt}$) between the start and end of the pulse over a 25 dB dynamic range for two different pre-bias conditions. The five input power values are located at (15, 9) dB back-off, and (5, 7, 10) dB gain compression.

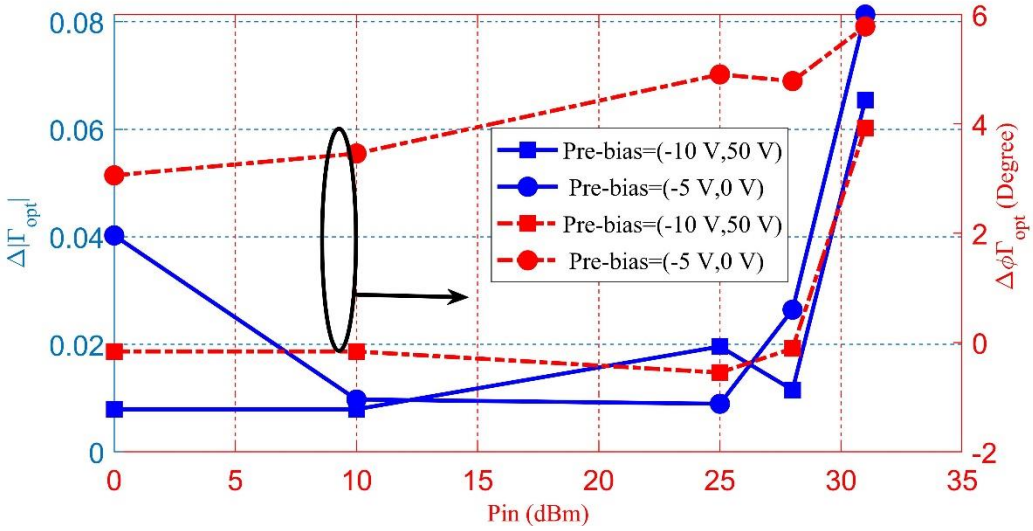

Figure 4-13: Difference between Optimum impedances of the start and end of the pulse at 10 W GaN device over 25 dB Pin range and two different pre-bias conditions, PW= 300 µs, duty cycle= 3 %, class AB, bias point= (-3.5 V, 28 V), sample rate=100 MS/s, acquisition length= 60 µs, frequency= 1.4 GHz.

For the Pre-Bias (PB) condition of V_{GS}= -5 V and V_{DS}= 0 V (PB=(-5 V, 0 V)), the $\Delta|\Gamma_{opt}|$ is significant at either end of the input power range highlighting the nonlinear interaction of the RF signal with the DUT's voltage threshold and knee voltage. The changes in phase between the optima exhibit a rather linear relationship. Due to these changes of optimum impedances for the different sections of the pulse over a varying input power, a constant load impedance for an entire RF pulse, as typically used in an RFPA design, will result only in a sub-optimum efficiency and P_{out} performance.

A different pre-bias of V_{GS}= -10 V and V_{DS}= 50 V shows that the $\Delta\Gamma_{opt}$ across an RF pulse is significantly decreased over the entire range of output power levels with the exception of very high gain compression in excess of 10 dB. Achieved results indicate the variation of the optimum load impedance occurs over a wide P_{in} level, and mostly affect the device in compression and back-off levels when the device starts to interact with knee and threshold voltage, respectively. Figure 4-13 illustrates buffer layer traps

cause the observed optimum impedance variation as by applying high drain-lag level to the PA, $\Delta\Gamma_{opt}$ decreases significantly. The observed results are in agreement with PIV results that are shown in the previous section.

Presented observations from active load-pull measurements show optimum impedance varies within the pulse. In previous researches, active load-pull measurements were performed at different timeslots of the pulse, to measure output power and gain, however, the load impedance was terminated to a fixed impedance and they assumed optimum load impedance was fixed over the pulse width [11].

4.6 GATE-LAG AND DRAIN-LAG EFFECT ON OPTIMUM IMPEDANCE VARIATION

In previous section, optimum impedance variation of the pulse is shown over a 25 dB dynamic range, that comes from variation of the output signal of the device. Applying the RF signal to the device, affects the channel temperature. Moreover, charging level of traps of device varies within the RF pulse, and these two phenomena change the optimum impedance of the device in time-domain. In this section, by applying various gate and drain-lag levels to the device and charging the traps of the device at different levels, before applying intended signals to it, traps effect on optimum impedance variation of the device is investigated. As pre-charging signals charge the traps of the device without generating dissipated power and changing the temperature of the channel of the device, they assist to separately analyse the trapping effect on the large-signal behaviour of the device.

Optimum impedances of start ($\Gamma_{opt\text{-}start}$) and end ($\Gamma_{opt\text{-}end}$) of the pulse are achieved by performing active load-pull measurements and $\Delta\Gamma_{opt}$ indicates the deviation between the optima.

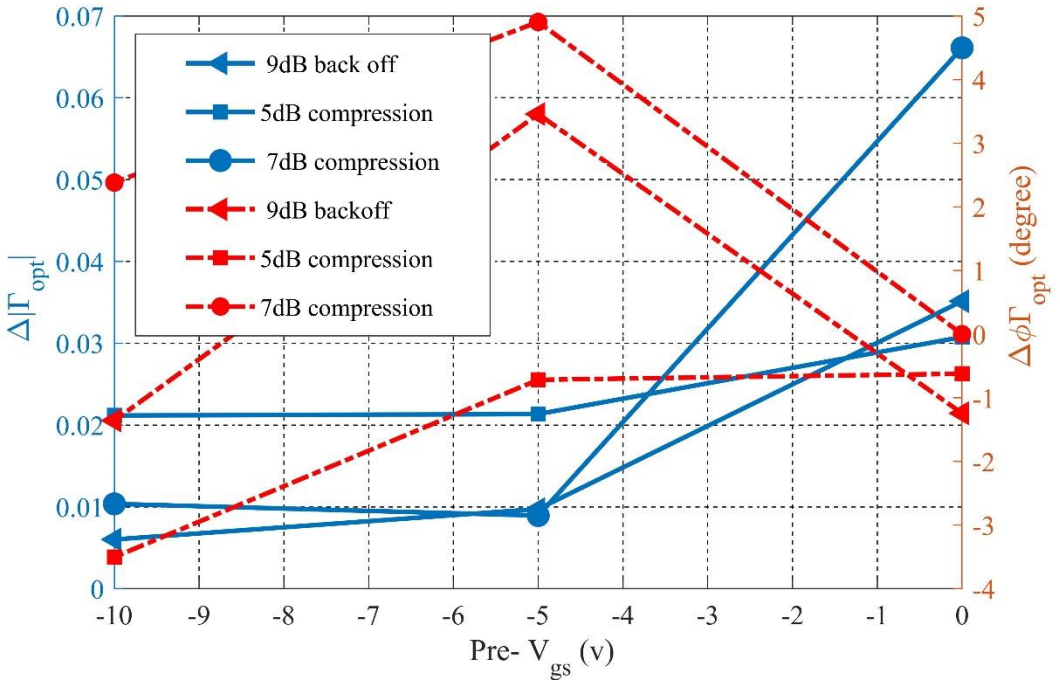

Figure 4-14: Gate-lag effect on the optimum impedance variation of the device over 25 dB dynamic range at 10 W device, PW= 300 µs, duty cycle= 3 %, bias point= (-3.5 V,28 V), frequency= 1.4 GHz, acquisition length= 60 µs, pre- V_{DS}= 0 v.

Figure 4-14 illustrates the impact of different gate-lags on the optimum impedance within the pulse. As can be seen $\Delta\Gamma_{opt}$ decreases for a decreasing pre-V_{GS} when considering the entire 15 dB input power range. The worst-case condition occurs at pre-bias VGS > -5 V, which represents typical class A to B bias value for the device, that shows the optimums difference is significant during these bias levels.

For investigating the drain-lag impact on the $\Delta\Gamma_{opt}$, the measurement process was repeated for different pre-drain voltage levels when pre-V_{GS} is set to -10 V. Figure 4-15 and Figure 4-16 show the drain lag effect on the $\Delta\Gamma_{opt}$ of 10 W and 4 W devices.

The optima within the pulse get closer together with an increasing pre-V_{DS} and when pre-V_{DS} is about two times more than V_{DS} (In 4 W device it was not possible to reach 80 V, as SMU modules cannot provide more than 60 V). By analysing the recorded data from both devices, they show similar behaviour in the variation of the optima, and a clear decrease at high drain-lag levels is observed. Moreover, as reported in [5], considering all drive-levels the worst-case scenario occurs when pre-V_{DS} is equal to the V_{DS} value which is used for biasing the device.

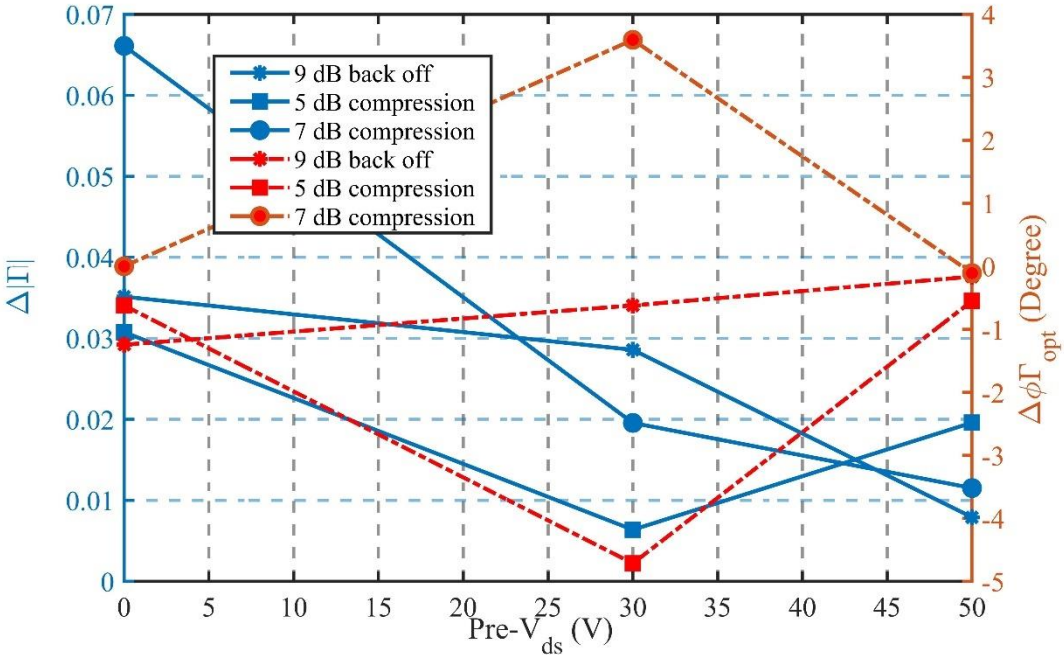

Figure 4-15: Drain-lag effect on the optimum impedance variation at 10 W GaN device, PW=300 µs, duty cycle= 3 % bias point= (-3.5 V,28 V), frequency= 1.4 GHz, acquisition length= 60 µs, pre-V_{GS}= -10 V.

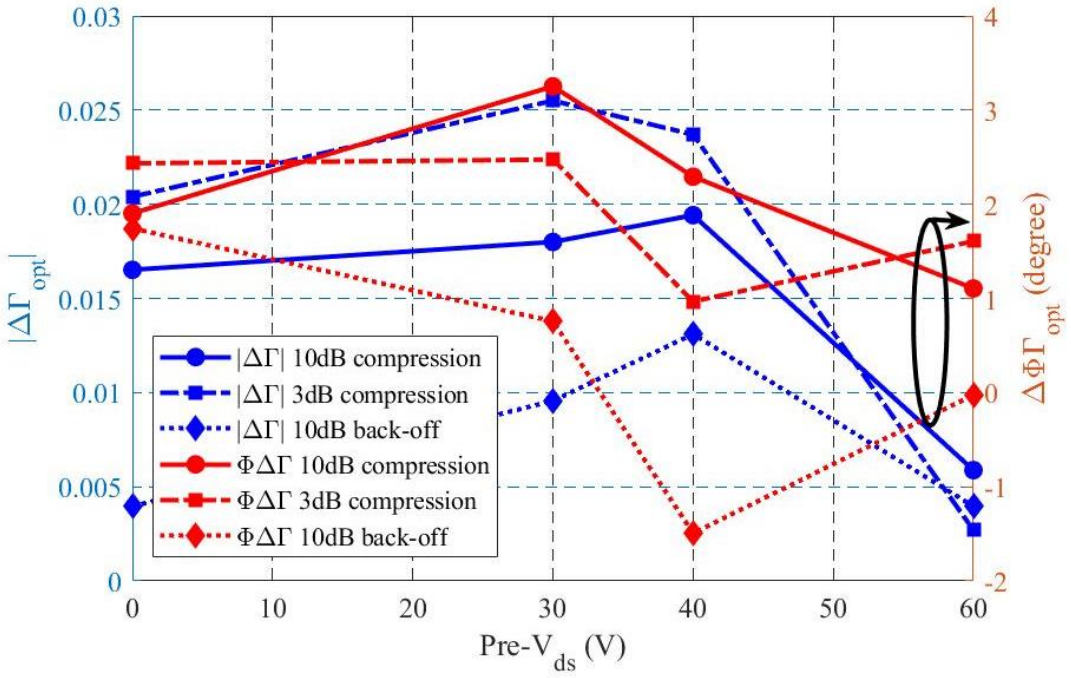

Figure 4-16: Drain-lag effect on the optimum impedance variation at 4 W GaN device, PW= 300 µs, duty cycle= 3 %, pre-V_{GS} = -10 V.

It clarifies the continuous DC voltage for V_{DS} is the worst-case scenario over the different drive levels.

Figure 4-17 shows the impact of bias point on the optima variation. The 4 W device with the higher V_{DS} bias shows a significantly smaller Γ_{out} variation. A possible explanation is that the higher V_{DS} bias results in a shallower load-line with a lower knee voltage and therefore subject to less pronounced knee-walk-out.

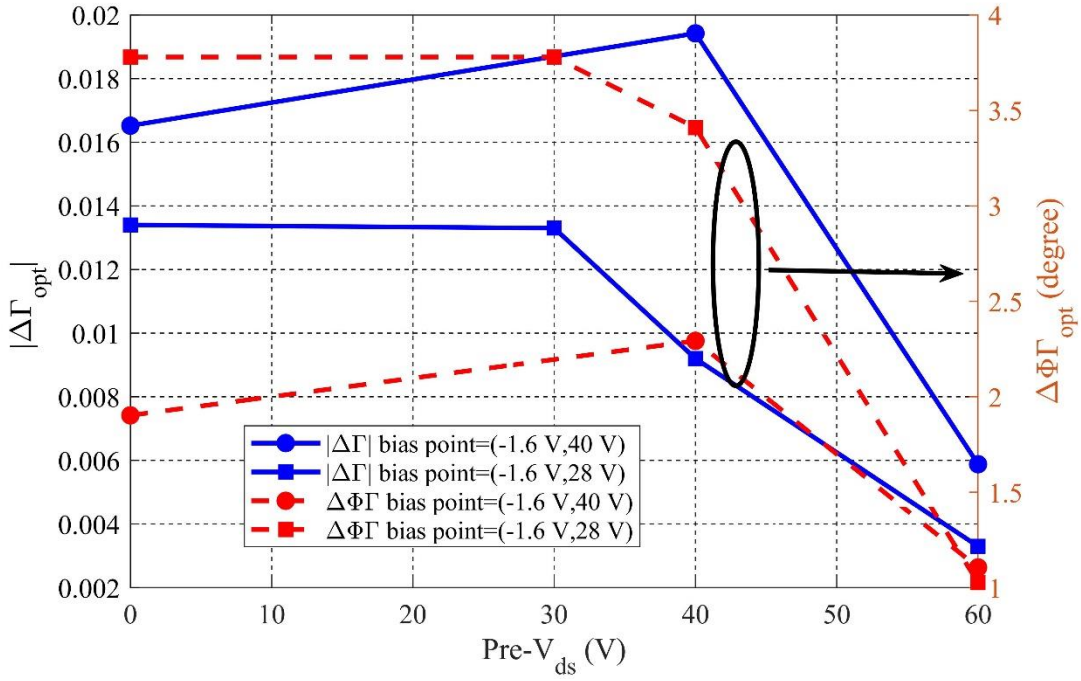

Figure 4-17: Bias point impact on $\Delta\Gamma_{OPT}$ of 4 W device at 7 dB gain compression and pre-V_{GS} = -10 V, frequency= 14. GHz, sample rate= 100 MS/s, acquisition length= 60 µs.

Variation of the optimum impedance within the pulse, leads to drop the optimum performance of the device at specific timeslots as the load impedance of the device typically is fixed within a pulse. Figure 4-18 represents the output power of the 10 W device in time-domain which is continuously decreasing within the pulse. Different achieved optimum impedances of each section of the pulse are shown and depicted values for $\Gamma_{OPT\text{-}START}$, $\Gamma_{OPT\text{-}END}$ and $\Gamma_{OPT\text{-}PULSE}$ represent the optimum impedances at the start, end and for the entire pulse, respectively.

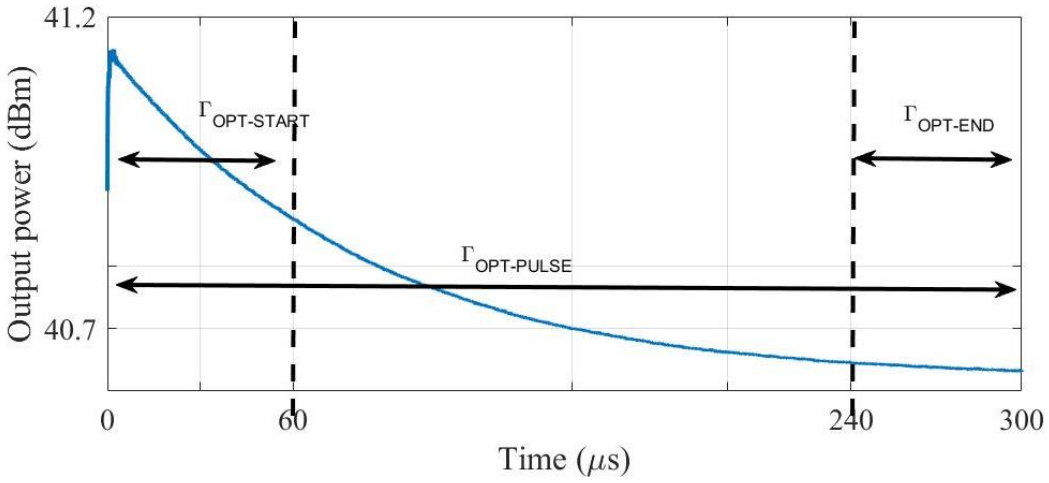

Figure 4-18:Output waveform of the device and optimum impedances of the different sections of the pulse in 10 W GaN, terminated at 50 Ω, frequency= 1.4 GHz, bias point= (-3.5 V, 28 V), 7 dB compression level, sample rate= 100MS/s.

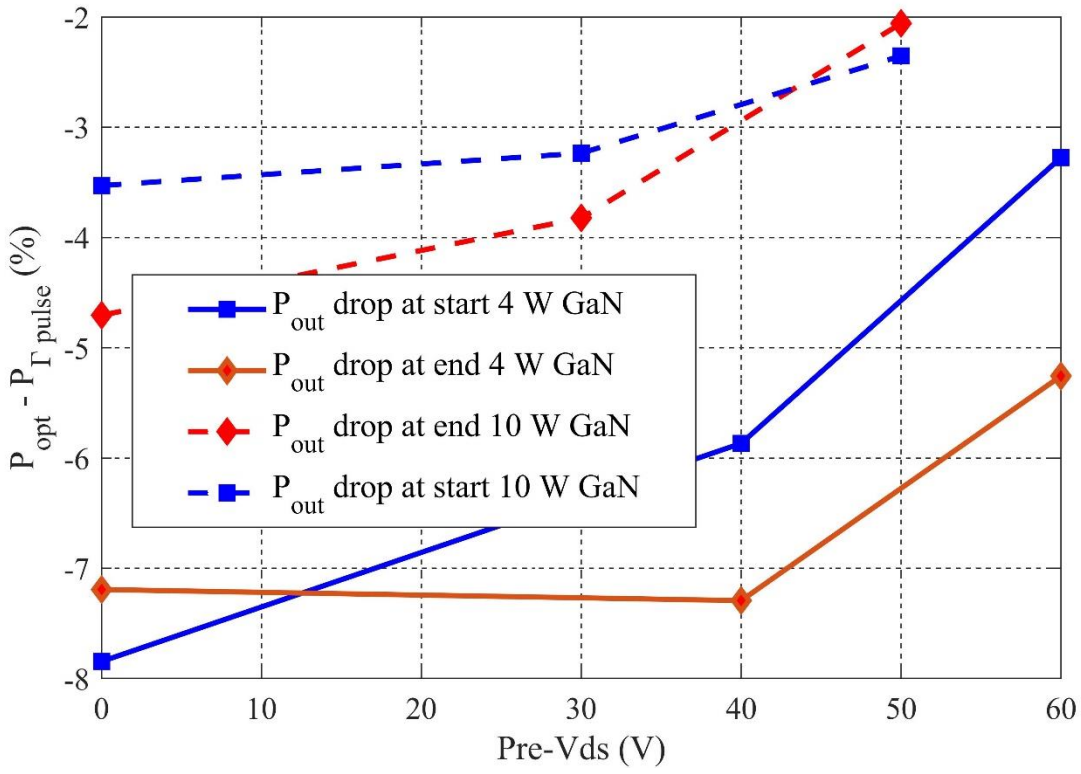

Figure 4-19: performance degradation of the10 W and 4 W devices within a pulse and drain-lag effect on P_{out} degradation at 7 dB gain compression, bias point for 4 W device =(-1.6 V, 40 V), bias point for 10 W evice= (-3.5 V, 28 V) and pre-V_{GS} = -10 V, acquisition length= 60 µs, sample rate= 100 MS/s, frequency= 1.4 GHz.

Since the optimum impedance of each section is different, the device becomes mismatched resulting in sub-optimum device performance over the RF pulse duration. Figure 4-19 shows the difference between $P_{\Gamma PULSE}$ on one side and $P_{OPT\text{-}START}$ and $P_{OPT\text{-}}$

END. $P_{\Gamma PULSE}$ indicates the maximum output power of the device when $\Gamma_{OPT\text{-}PULSE}$ is set to the load side during the whole pulse width and acquisition window is set to the start (end) of pulse. $P_{OPT\text{-}START}$ ($P_{OPT\text{-}END}$) shows the maximum achieved power when the $\Gamma_{OPT\text{-}START}$ ($\Gamma_{OPT\text{-}END}$) is set to the load side. The results are shown for both the 4 W and 10 W GaN devices and depict the drop in power at each section of the RF pulse if Γ_{PULSE} is used instead of the respective optimum impedance. Without pre-pulsing the degradation of output power is around -8 % and improves to -3 % at high pre-bias voltages for the 4 W device. The change for the 10 W device is similar starting with -5 % and recovering to -2 %. Effectively, the pre-charged device state enables RFPAs with a constant load impedance to achieve almost optimum P_{out} during RF pulse operation. Moreover, as optimum impedances of the start and end of the pulse merge together at high drain-lag levels, the difference of the achieved maximum output power at start and end of the pulse declines, and the achieved power at both timeslots are similar to each other.

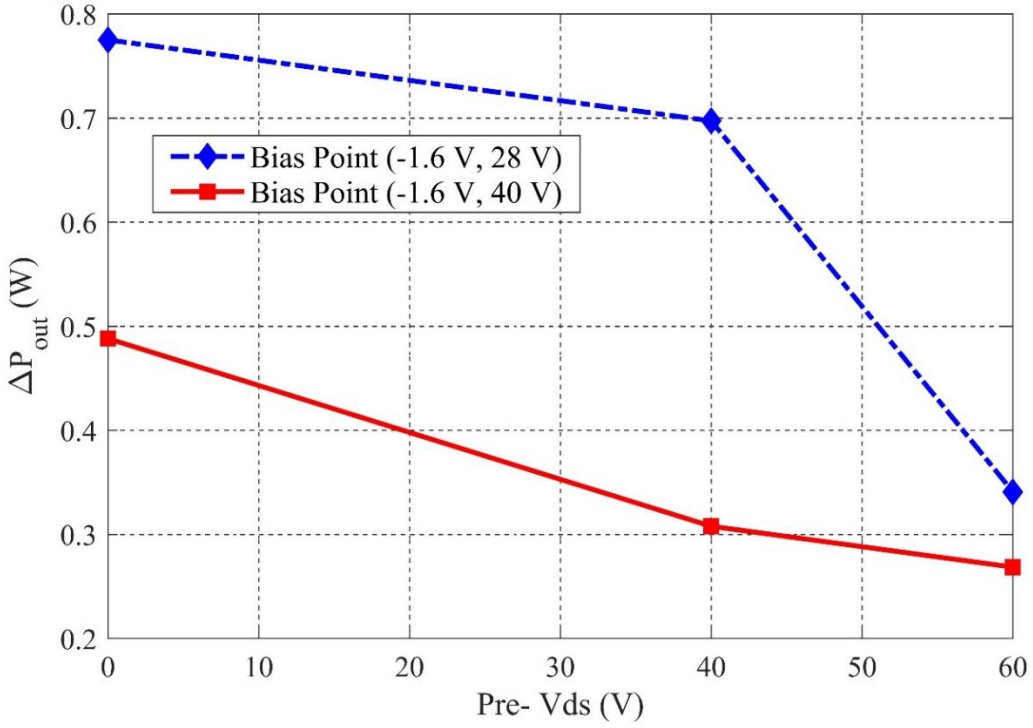

Figure 4-20: Output power variation within a pulse at two different bias points at 7 dB gain compression and pre-V_{GS} = -10 V. PW= 300 µs, duty cycle = 3 %, 4 W device, frequency = 1.4 GHz, acquisition length = 60 µs.

Figure 4-20 presents the output power variation within a pulse at different bias points at 4 W device. Here ΔP_{out} indicates the output power difference between the start and end of a pulse.

Observed variation at the output waveform of the device can be the reason for changing the optimum impedance of the device within the pulse. In [1] gain variation within the pulse was carried out at different pre-bias conditions during performing passive load-pull measurements, and it was shown by applying drain-lag to the device, output variation declines. Thus, new results provided in this section clarifies traps effect on optimum impedance variation within the pulse and are in line with previously reported behaviour of the traps. Utilising pre-pulsing signals to minimise the output variation in the device is an interesting method which is not implemented in practical and commercially available PAs.

So far, it was shown applying the various drain and gate lag levels to the device can minimise the variation in output waveforms of the device and as a result of that, optimum impedance comes to be more constant within a pulse. Following these results, it was investigated how the identified $\Delta\Gamma_{opt}$ depends on the device temperature. Thus, the device is measured at two different temperature levels (room normal temperature (22ºC) and 40ºC). Device is placed in the chunk and heated by using a thermal resistor, then once its temperature is fixed at 40ºC, all active load-pull measurements at the start and end of the pulse are performed. The acquired result is shown in Figure 4-21 where $\Delta\Gamma_{opt}$ is shown at two different pre-bias conditions. As can be seen, the magnitudes of the $\Delta\Gamma_{opt}$ remain relatively constant over the

investigated temperature range at both pre-bias conditions, which expresses the R_{OPT} of the device at the start and end of the pulse varies equivalently by increasing the temperature, thus their difference becomes constant over the mentioned temperature levels. Furthermore, the magnitude difference at PB= (-10 V,50 V) is less than PB=(0 V,0 V) condition over practical temperature levels which confirms pre-charging the traps of the device can minimize the R_{OPT} variation of the device within the pulse. However, the phase change can be rather significant reaching up to 10 degrees over the measured temperature levels. This phase dependence is significantly reduced for the identified optimum PB=(-10 V,50 V). the observed results show pre-charging the traps can minimise the device variation at the load-side and different package temperature levels.

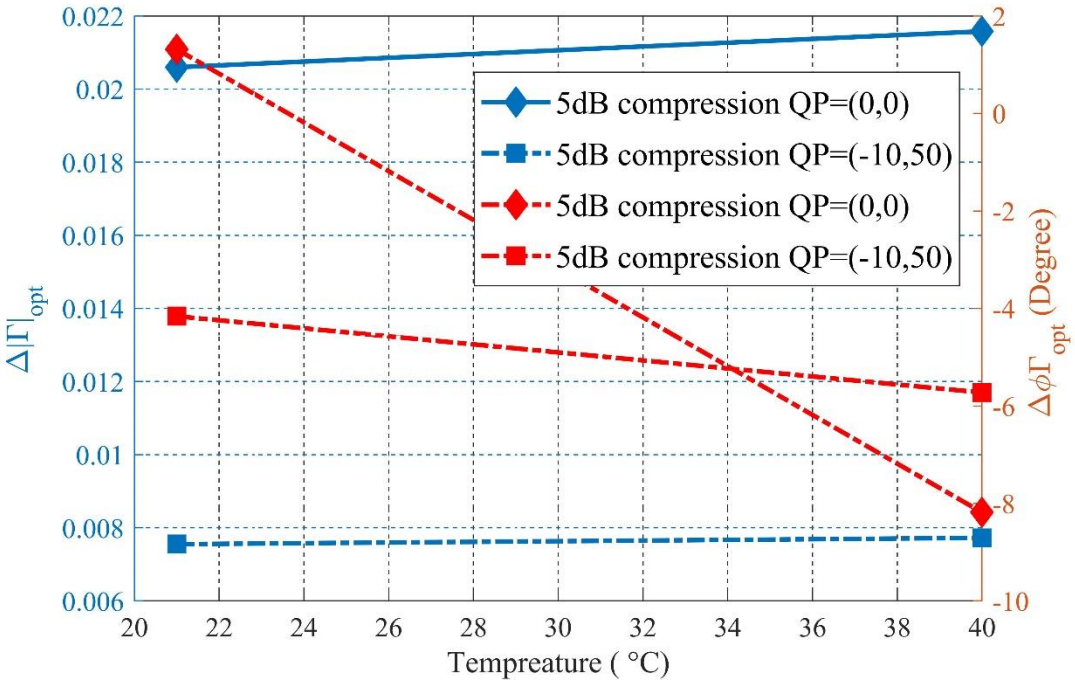

Figure 4-21: $\Delta\Gamma_{opt}$ at different package temperature levels 22°C and 40°C at a constant gain 5dB compression. PW= 300 µs, duty cycle= 3 %, 7dB gain compression, 10 W device, frequency= 1.4 GHz, acquisition length = 60 µs .

4.7 SOURCE IMPEDANCE VARIATION WITHIN AN RF PULSE

PAs are typically designed to have a fix input impedance and optimised to operate in that condition. Provided measurements show optimum load impedance varies within a pulse, in this section, observations at the input of the device during pulsed active load-pull measurements are presented to investigate the time-domain variation of the incident and scattered travelling waves at the input of the device. To characterise the input behaviour of the device, all results are achieved at optimum load impedance of each section of the pulse while pulsed active load-pull measurements with 3 % duty cycle is conducted as described in the previous section. Figure 4-22 shows, as expected, the incident travelling wave (A1) that is generated by the drive amplifiers at the input of the measurement system remains constant over the entire duration of the pulse, that clarifies test set and amplifiers are working well and amplifiers transient time do not affect the observed results. Also, as expected, incident traveling wave at different PBs are the same which clarifies the DC path of the test set does not affect the RF and the reflected traveling wave of the input of the device is completely separated from A1 port. The reflected traveling wave (B1), however, varies significantly within the pulse at PB= (0 V,0 V) condition. Therefore, variation not only happens at the output of the device but also occurs at an input port of the GaN device. For investigating the trapping effect input scattering waves are measured at three different drain-lag levels and as can be seen by increasing the drain-lag level and charging the traps at a higher level, variation of the reflected wave plunges, and at PB = (-10 V, 60 V) the B1 wave is almost stable over the entire pulse. Moreover, Figure 4-23 illustrates the changes of the input reflection coefficient Γ_{in} within the RF pulse with clearly observable variations at low pre-bias values. These variations gradually disappear as the pre-bias is increased and becomes constant for the pre-bias PB = (-10

V, 60 V) setting albeit at a reduced magnitude. The phase variations of the input reflection coefficient remain largely unchanged within the pulse by the applied pre-bias. In summary, the pre-charging of the device has the potential to make input matching more straightforward over the duration of an RF pulse and maintain the optimum matching condition. Especially for devices with input impedances close to the edge of the Smith chart, as decrease Γ_{in} of the device and Z_{in} of the device moves toward 50 Ω.

Observation of the A1 of the device, confirms the input incident wave to the device is constant and all recorded variation at input and output of the device, come from the device and they are not related to the imperfections of the test set or drive amplifiers.

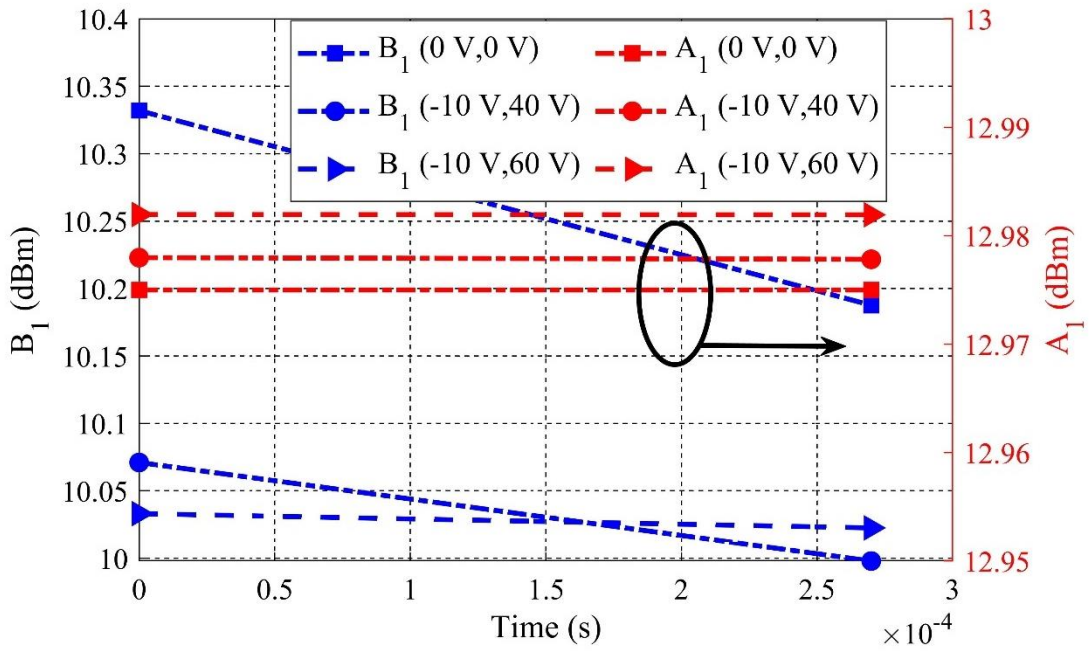

Figure 4-22: $|A_1|$ and $|B_1|$ variation within the pulse at different drain-lag levels at 1dB gain compression, PW= 300 µs, duty cycle= 3 %, acquisition length = 60 µs, frequency = 1.4 GHz, bias point=(-1.6 V, 40 V), 4 W device.

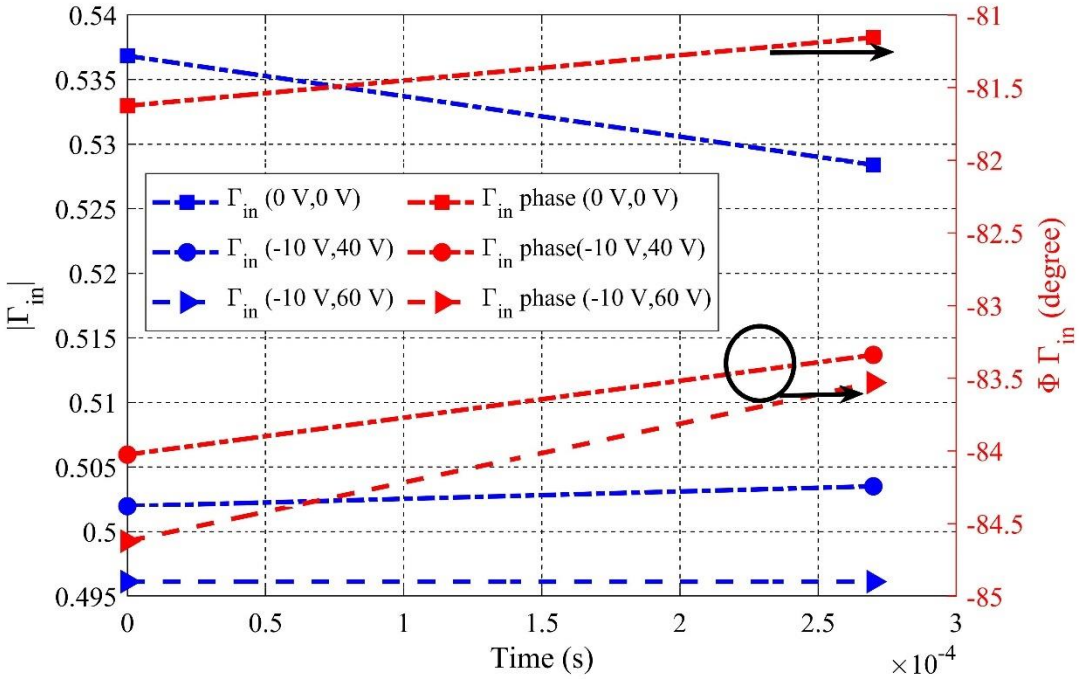

Figure 4-23: Phase and magnitude changes of Γ_{in}. 1 dB gain compression level, PW= 300 µs, duty cycle= 3 %, acquisition length = 60 µs, frequency = 1.4 GHz, bias point=(-1.6 V, 40 V), 4 W device.

Based on the observation provided, the maximum V_{DS} swing during the RF pulse is $2V_{DS\text{-}bias}$ defines the traps charging state, thus by applying pre-pulsing V_{DS} of $2V_{DS\text{-}bias}$ before RF pulse, results in fixe traps charging level during RF pulse.

4.8 TRAPPING EFFECT ON THE LINEARITY OF THE DEVICE

Linearity is an important performance metric of PAs, which RFPA designers try to improve it by employing various techniques such as DPD, which is a signal processing technique to change the input signal by analysing the output of the PA and it is usually useful when the device operates in compression levels.

Besides the employed technique to design PA, different physical phenomena such as self-heating and traps affect the linearity of PA [12]. In this section of the chapter, traps effect on in-band and out-band linearity is analysed, and based on provided

observation a novel technique is proposed to improve the linearity. The proposed technique not only is valid on compression level but also its impact on linearity at back-off level is more significant. Moreover, by moving the acquisition window over the whole pulse width, IMDs variation in time-domain is presented that provides a piece of novel information about linearity variation in time-domain.

4.8.1 IN-BAND LINEARITY OF PRE-CHARGED STATE

The linearity assessment of the pre-charged device state focuses initially on in-band linearity. Two-tone measurements at 50 Ω load impedance are performed to permit investigation of in-band frequencies and distortion levels. In-band linearity is defined as any unwanted changes that occurs inside the main bandwidth of the signal at the output of the device. Here, as only two-tone applied to the PA, thus to analyse the in-band linearity of the device, the difference of the B2 (output waveform of PA) magnitude and phase of two pulsed tones are considered. Figure 4-24 shows the applied pulsed input signal to the device with the 2-tones magnitudes having a 10 dBc difference (asymmetric case) and varying bandwidth from 100 kHz to 10 MHz to achieve 1 dB gain compression level. Centre frequency of the tones is set to F_C=1.4 GHz. The asymmetric case is chosen because the second tone power level is significantly smaller, therefore more sensitive to any in-band distortion tones due to the device nonlinearity. The 4 W GaN device was biased for all measurements at V_{GS} = -1.6 V and V_{DS} = 40 V.

The observed |B2| difference between first and second tones is shown in Figure 4-24. Two acquisition windows are set at the start and end of the pulse to analyse the B2 at different PB levels. Before any applied pre-bias, the device exhibits relatively strong in-band distortions at the start of the RF pulse, which then decrease as the pulse

progresses, and |B2| is more stable at the end of the pulse over the measured bandwidth range. As 10 dB difference between the first tone and second tone is considered at the applied pulses, the linear response of the device should represent the same amount of the difference at |B2| at the output of the device, thus variation in the difference of the |B2| of the main tones, shows in band nonlinearity of the device. The pre-charged state reduces the higher distortions at the start of the pulse. It is interesting to note, that in both cases the distortions exhibit a rather sudden change for bandwidths beyond 1 MHz indicating traps with a time constant of shorter than 1 µs.

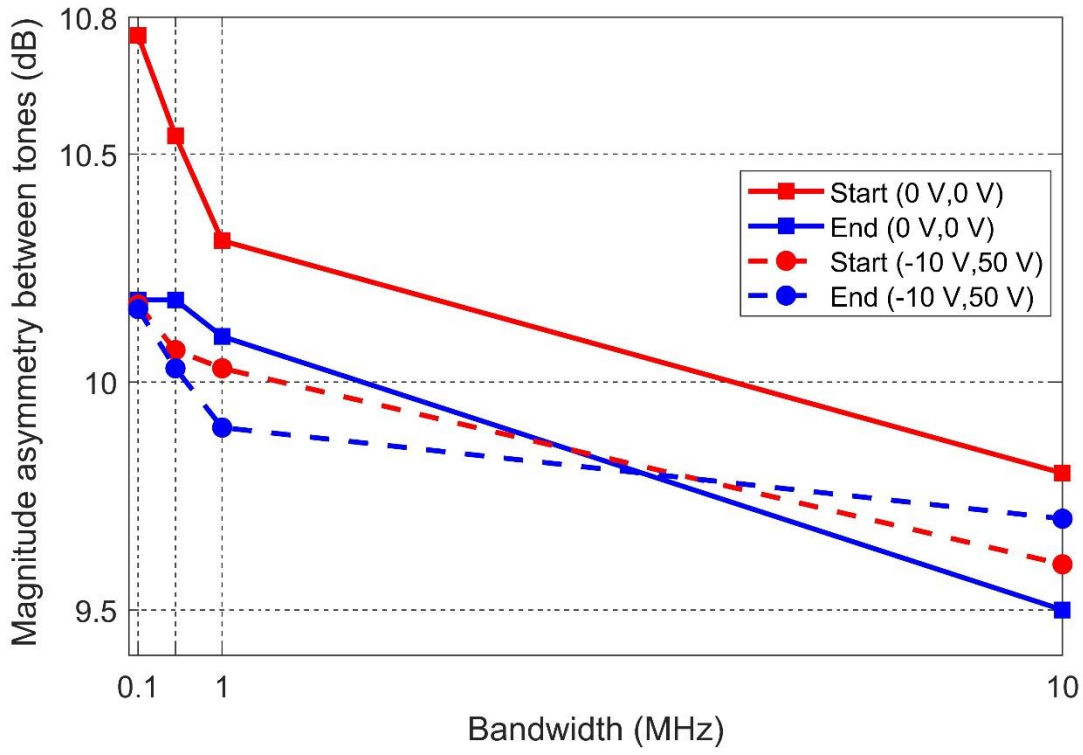

Figure 4-24: In-band signal distortions of the two pulsed B_2 magnitudes at Δf = (0.1, 0.5, 1, 10) MHz, 1 dB gain compression, PW=300 µs, duty cycle= 3 %, Pin= 9 dBm, 4 W device, centre frequency= 1.4 GHz, bias point= (-1.6 V, 40 V), acquisition length= 60 µs.

To investigate phase changes between the in-band tones, the difference of the phases of the B2 tones is considered at the start and end of the pulse.

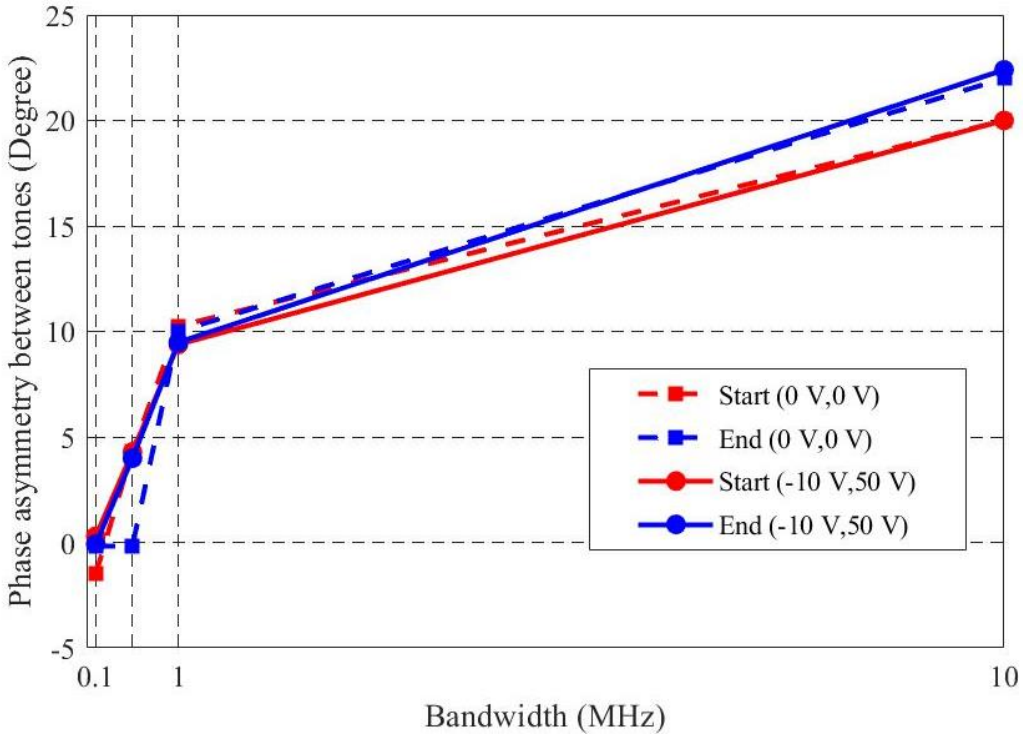

Figure 4-25: In-band phase distortions for a pulsed 2-tone signal at Δf = (0.1, 0.5, 1, 10) MHz, 1 dB gain compression, PW=300 µs, duty cycle= 3 %, Pin= 9 dBm, 4 W device, centre frequency= 1.4 GHz, bias point= (-1.6 V, 40 V), acquisition length= 60 µs.

As can be seen from Figure 4-25, pre-charging the traps does not have any impact on the phases, and they remain the same over the entire bandwidth. However, also the phase behaviour is subjected to the same traps with a minimum 1 µs time constant. In other words, the 2-tone measurements show no apparent traps with time constants less than 1 µs.

4.8.2 OUT-BAND LINEARITY OF PRE-CHARGED STATE

Out-band linearity is defined as comparing the power level of the signal in the main bandwidth of the applied signal with the IMDs power level. Pulsed two-tone measurements with various bandwidths are performed to investigate the linearity of the device attached to a 50 Ω load. For this investigation both symmetric and

asymmetric 2-tones are utilized with FC = 1.4 GHz and tone spacing ΔF = 500 kHz. For the asymmetric case, the second tone is set to a 10 dB lower power and for both 2-tone cases, the drive power is set to attain 1 dB gain compression. To eliminate spectral leakage, the ratio of pulse width and tone spacing is set to an integer number. A Distortion Power Ratio (DPR), shown in (4-1) is used to assess the linearity of the device. During these investigations, the 4 W GaN device was biased at V_{GS} = -1.6 V and V_{DS} = 40 V.

$$DPR_n = \frac{P_{IMD_n}}{P_{main}} \quad (4\text{-}1)$$

The impact of a pre-charged device state on IMD_3 is analysed over a 17 dB dynamic range; from 7 dB gain compression to 10 dB output power back-off. As shown in Figure 4-26, the pre-charging results in increased linearity across the entire dynamic range with the most significant improvements at the higher back-off power levels, which also agrees well with initial PIV observations. PIV observations have shown pre-pulsing can affect the threshold voltage and fix it within a pulse; therefore it is expected at a lower power regime, the impact of pre-bias is more than higher power levels. The improvement here for the asymmetric case is about 5 dB while in the case of the symmetric tones the linearity is improved by about 9 dB. Improvements of linearity are also achieved at higher gain compressions although by a reduced amount. For the asymmetric 2-tones, the improvement is rather minimal at gain compressions above 4 dB. The reason for this is the rather small envelop variation for the asymmetric case that is strongly reduced by modest gain compression levels.

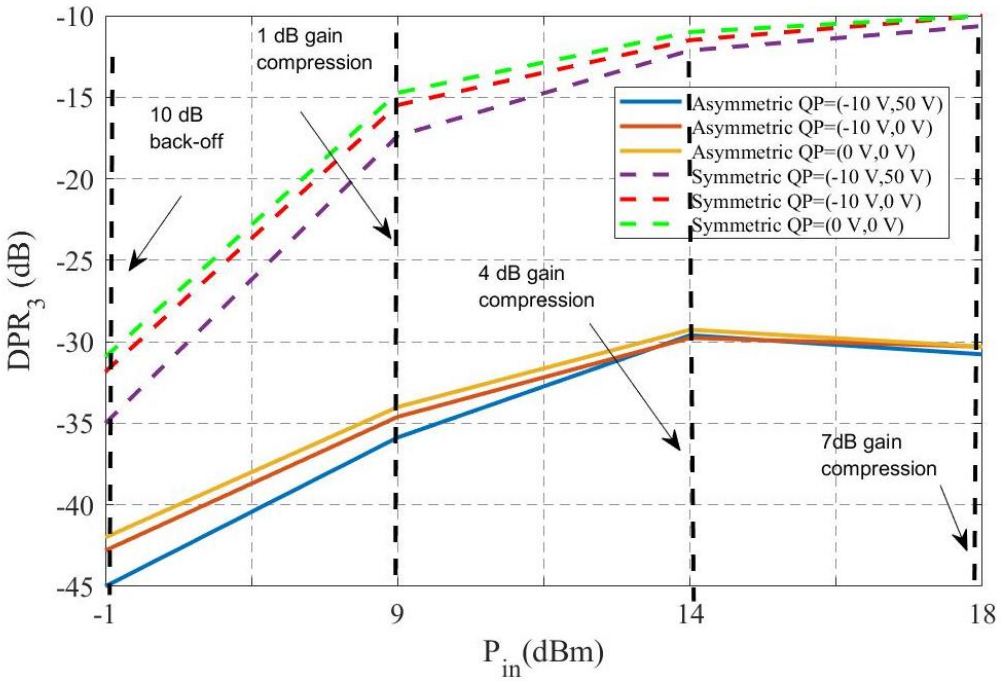

Figure 4-26: DPR_3 for a pulsed 2-tone signal acquisition window is in start of the pulse, sample rate = 10 MS/s, ΔF = 500 kHz, PW= 300 µs, duty cycle= 3 %, 4 W device, centre frequency= 1.4 GHz, bias point= (-1.6 V, 40 V), acquisition length= 60 µs.

Figure 4-26 also indicates the different pre-charging effects on the improvement of the linearity over the aforementioned dynamic range. By applying the gate-lag level and pre-filling the traps at the gate-source junction of the device, the linearity of the device improves. However, the drain-lag effect on linearity improvement is more significant. It expresses the traps of the device is not only in the buffer layer of the device but also exist in the surface layer of the device around the gate-source junction.

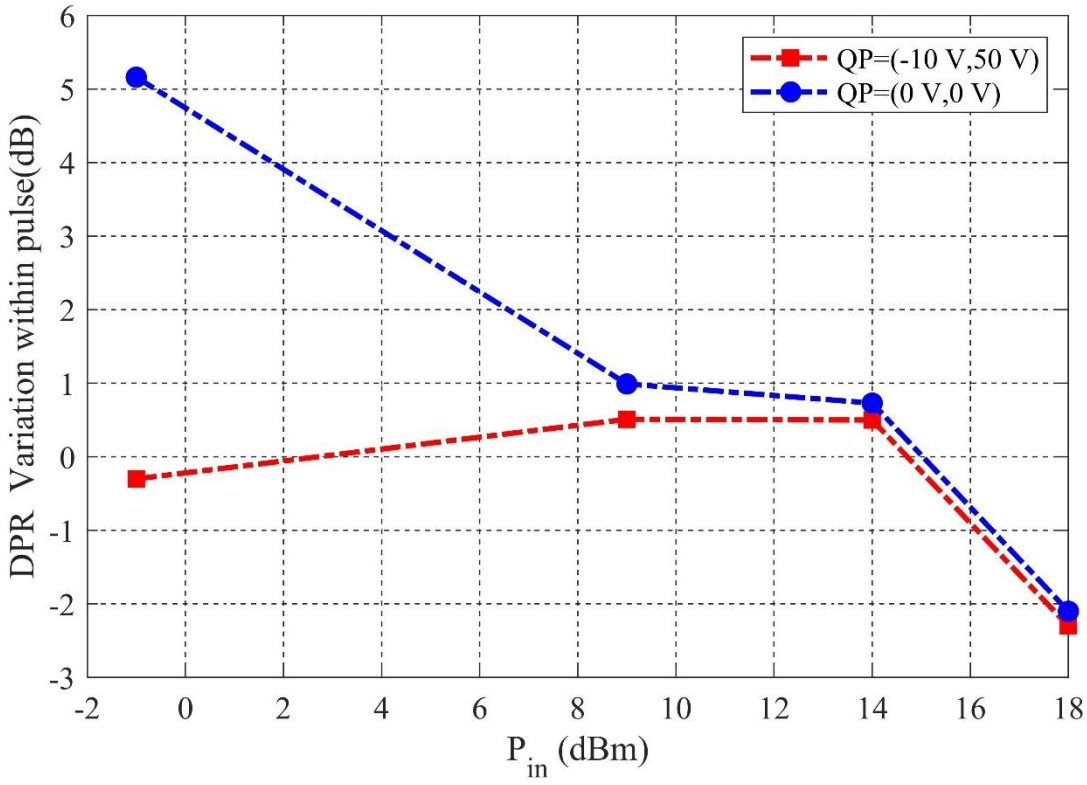

Figure 4-27: Difference of DPR_3 at start and end of the pulse at two pre-bias conditions, sample rate = 10 MS/s, ΔF = 500 kHz, PW= 300 µs, duty cycle= 3 %,4 W device, centre frequency= 1.4 GHz, bias point= (-1.6 V, 40 V), acquisition length= 60 µs.

Figure 4-27 shows the DPR_3 difference between the start and end of each RF pulse over the same 17 dB dynamic range when using the asymmetric 2-tones. For the case when the device is not pre-charged, the DPR_3 shows clear variations at the lowest drive level and decreases rapidly as the device enters gain compression. This is in line with the previous observation and directly linked to the small envelop variation of the stimulus signal that is rapidly squashed by the gain compression. Also, the pre-charged state exhibits DPR_3 variations across the pulse, however, these are only apparent at high drive levels due to increasing AM/AM. At lower drive levels the variations in linearity across the RF pulse have been almost eliminated. The difference of about 5 dB is in close agreement with the observed linearity improvement in Figure 4-26 indicating that these improvements are attributable to a stabilized device state with a

rather constant output power performance over the entire RF pulse. To conclude, the pre-charged device exhibits better linearity at specific times within the RF pulse leading to an overall average improvement as it was observed in Figure 4-26.

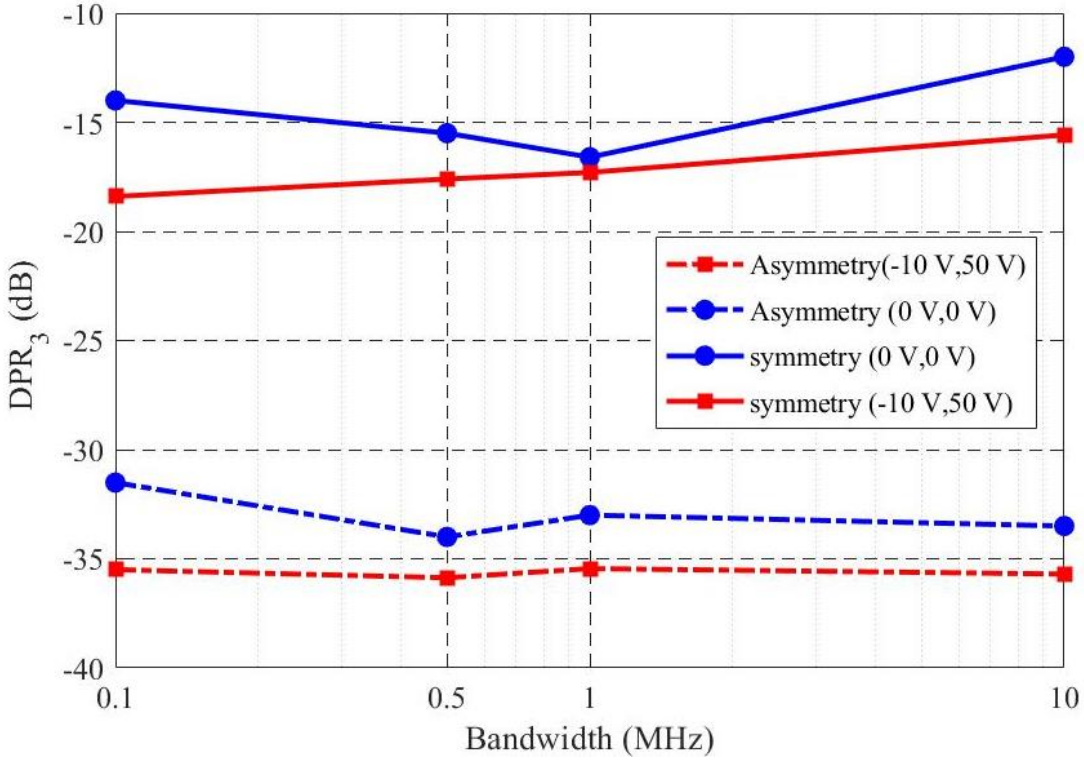

Figure 4-28: DPR_3 of start of the pulse at 1 dB gain compression, PW= 300 µs, duty cycle= 3 %, 4 W device, centre frequency= 1.4 GHz, bias point= (-1.6 V, 40 V), acquisition length= 60 µs.

To establish the bandwidth over which the new device state increases linearity, pulsed two-tone measurements are conducted with a tone spacing from 100 kHz to 10 MHz with an IMD_3 tone spacing going up to 30 MHz. As can be observed from Figure 4-28, the linearity improvement is maintained over a bandwidth of at least 10 MHz.

4.9 ENVELOPE-VARIANT OUTPUT SPECTRA

The capability of the system to provide measurements across the RF pulse is employed to analyse the time-dependence of the spectral tones at the output before and after pre-

charging the device. It allows to analyse the linearity variation within the pulse and measure the time constant of the traps which can affect the out-band linearity, as time-domain data for out-band and in-band tones are provided.

Here, a 60 µs acquisition window is moved in 60 µs steps across the RF pulse to obtain information on the time-variance of output spectra. P_{in} level is the same as other linearity investigation in the previous section and kept at 1 dB gain compression level, i.e. at input power of 9 dBm. All the intermodulation distortion levels (IMD) higher than noise floor of the measurement system at utilised sample rate and sample per average, are illuminated. During these investigations same bias values and 2-tones stimuli are used. Figure 4-29 and Figure 4-30 show such variations for the two main tones and IMD_3 tones in time-domain. The in-band tones during the pre-charged state show a small reduction in power of about 1.1 dB in comparison to PB = (0 V, 0 V), however, demonstrate also a more constant behaviour. This reduced time-variation is because slow-varying traps with a time constant between 60 and 120 µs are stopped from contributing towards the device's RF performance. However, the figure also shows that the impact of the pre-charged device state goes beyond the setting of traps in that it affects the RF performance over the entire RF pulse length. Most probably due to changes in the knee voltage of the IV plane. Arguably, this difference can be considered as small.

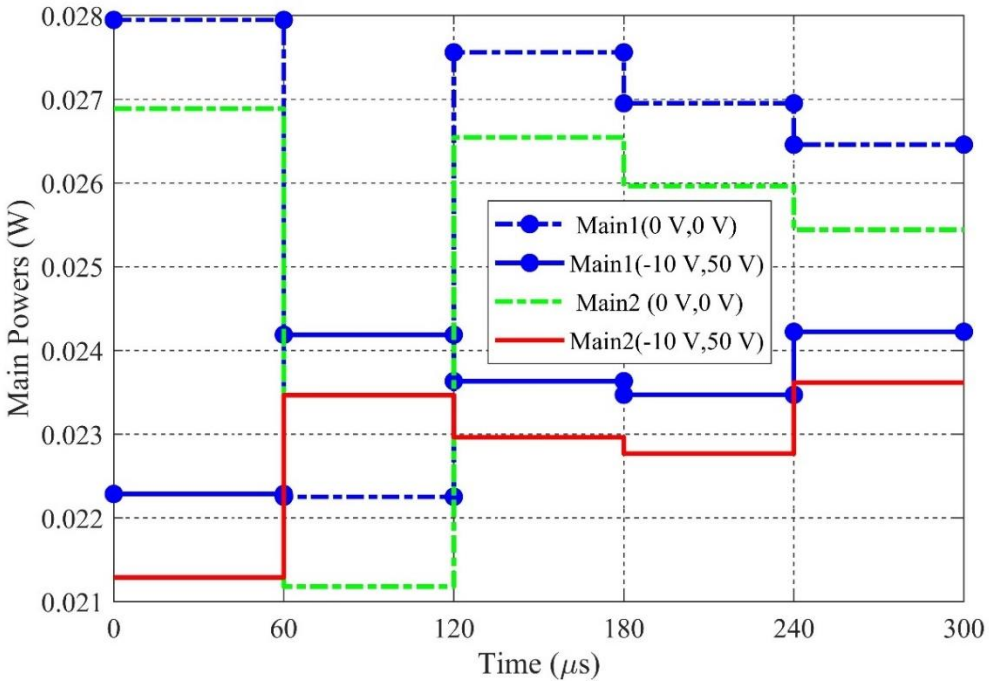

Figure 4-29: Main tones variation within the pulse of symmetric two-tone stimulus, Pin= 9 dBm, PW= 300 µs, duty cycle= 3 %, ΔF = 500 kHz, noise floor level = -75 dB, 4 W device, centre frequency= 1.4 GHz, bias point= (-1.6 V, 40 V), acquisition length= 60 µs, sample rate= 100 MS/s.

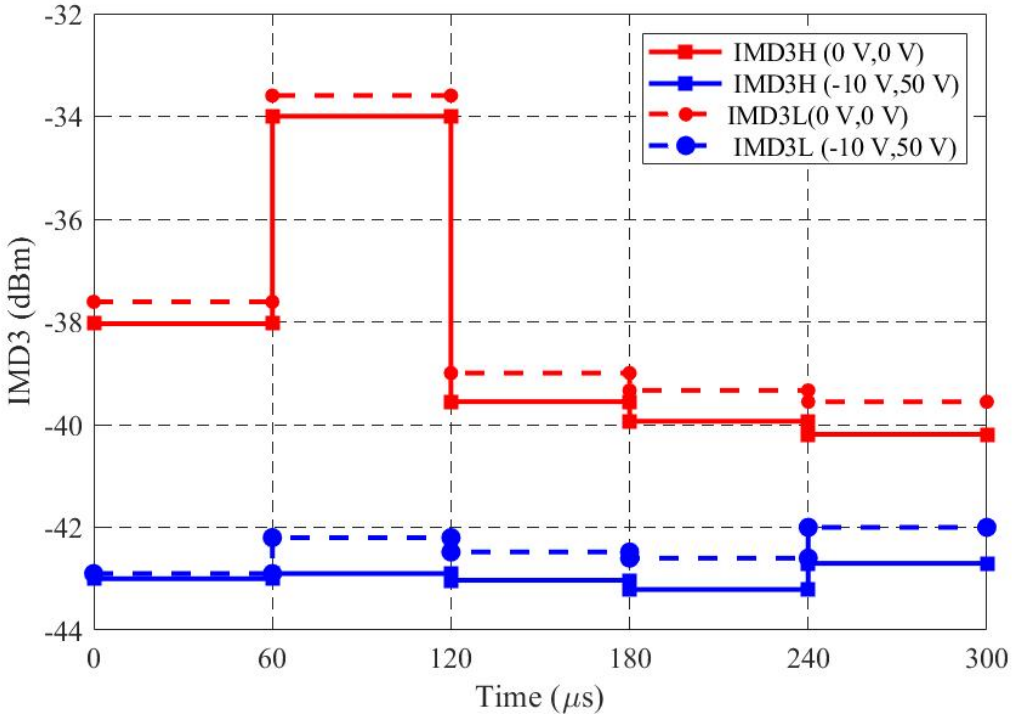

Figure 4-30: IMD_{3L} and IMD_{3H} time variation within the pulse of a symmetric two-tone stimulus, Pin= 9 dBm, PW= 300 µs, duty cycle= 3 %, ΔF = 500 kHz, noise floor level= -75 dB, 4 W device, centre frequency= 1.4 GHz, bias point= (-1.6 V, 40 V), acquisition length= 60 µs, sample rate= 100 MS/s.

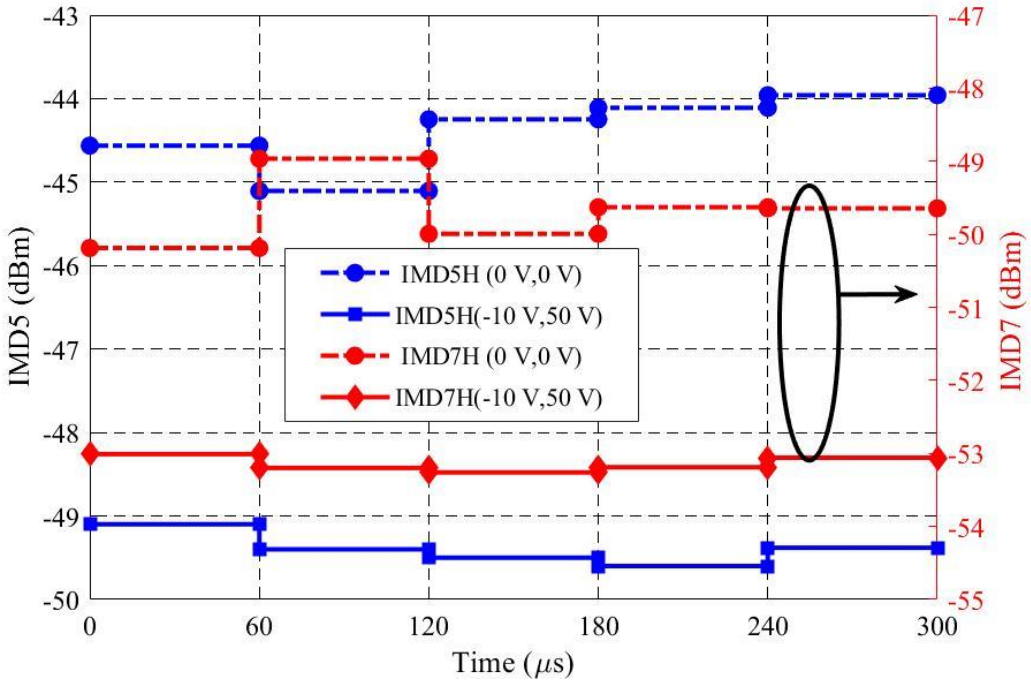

Figure 4-31: IMD5H and IMD7H variations over time of a symmetric two-tone stimulus Pin= 9 dBm, PW= 300 µs, duty cycle= 3 %, ΔF = 500 kHz, noise floor level= -75 dB, 4 W device, centre frequency= 1.4 GHz, bias point= (-1.6 V, 40 V), acquisition length= 60 µs, sample rate= 100 MS/s.

Figure 4-30 illustrates the resulting impact on the IMD_{3H} and IMD_{3L} distortion products. Their absolute power levels have decreased by slightly more than three times the drop of the fundamental tones which is most probably caused by the fact that during the pre-charged state the device's output power is slightly lower. The same traps between 60 µs and 120 µs also impact the IMD_3 distortion tones but their contribution is rendered inert when the device is pre-charged.

Therefore, as the dynamic range of the measurement system allows for the detection of higher order distortion products also IMD_5 and IMD_7 measurements are included in this work. Again, as shown in Figure 4-31 the pre-charged state generated a drop in IMD_5 power levels below the PB = (0 V, 0 V) state that is about five times the fundamental decrease of -1.1dB. The overall drop in IMD_7 levels is less and most probably is limited by the proximity of the power levels to the measurement noise

floor. However, the impact of the traps on the device state with PB = (0 V, 0 V) seems to be smaller producing only about 1 dB change between 60 and 120 µs.

At this stage, it is not possible to make any statement about the nature of the interaction between the main, IMD_3 and IMD_5 tones and the device traps. On one hand, the identified traps with a time constant 60 and 120 µs are far too slow to follow the spectral lines. On the other hand, previous measurements have indicated the existence of faster traps with a time constant as short as 1 µs. It is conceivable that the different traps are coupled to allow for some interaction with the signal's envelope. The main and IMD_3 tones with an offset of 0.25 and 0.75MHz from the centre frequency might be affected this way. This impact on IMD_5 tones might have been cause through some frequency mixing between the tones but it is unlikely that a drop of about 3 dB would reduce the IMD_5 levels by 5 dB. Overall, it doesn't appear likely for the traps to interact directly with the distortion products at the device's output, and it seems pre-charging has an impact on higher order of G_m of device.

Nevertheless, the investigations do not show any degradation in linearity when the device is placed into a pre-charged state that offers an improved device linearity. The biggest improvement in linearity occurs between 60 and 120 µs after the start of the RF pulse. It is relevant to note that the change of power within the RF pulse, which is most probably due to device thermal behaviour, levels off after about 60 µs, and therefore exhibits a similar time constant. It is therefore possible that both the dynamic thermal behaviour and pre-charging are just balancing each other out within the 60 - 120 µs time window. This is supported by the reduced variations in main power, as shown in Fig 4-26.

4.10 CHAPTER SUMMARY

In this chapter, an application of developed measurement system is introduced to investigate some of the large-signal behaviour of the device and traps impact on them. To verify the accuracy of observed results, DC-IV and PIV measurements are provided at different gate-lag and drain-lag levels which represent the current collapse in PAs' PIV characteristics.

It is reported that pre-charging can change the threshold voltage and cause knee walkout in the device. Then, time-domain large-signal behaviour of the GaN devices is investigated and observed results indicated output of the device varies in time-domain and it changes the optimum impedance of the device. It is also shown, variation in optimum impedance of PA leads to degrade the optimum performance of the device up to 8% and 5 % for 4 W and 10 W PAs, respectively. It is shown by pre-charging the traps of the device, optimum impedance variation declines, thus pre-charged device is mostly matched to the optimum impedance. Analysing the reflected wave of the input of the device expressed variation also occurs in the input of the device and pre-charging the PA can resolve the input impedance variation. The aforementioned observations are conducted on two GaN PAs with different power ranges and biasing technologies, to ensure the observations are not related to the specific device and are the intrinsic behaviour of GaN technology.

Linearity of the device is investigated and Pre-charging effect on in-band and out-band linearity is carried out. Pre-charging the traps can also increase the linearity of the device by suppressing the IMDs level up to 6 dB in back-off. Moreover, $IMD_{3,5,7}$ of the device are measured in time-domain with 60 µs steps, to probe the IMDs variation

at different timeslots of the intended signal when the device is pre-charged at a high drain-lag level.

Recorded behaviour of the device illustrates empty traps can impact the linearity and cause variation at the output of the device and by pre-filling them, the device delivers the better performance.

4.11 REFERENCES

[1] J. Faraj, F. De Groote, J.-P. Teyssier, J. Verspecht, R. Quéré, and R. Aubry, "Pulse profiling for AlGaN/GaN HEMTs large signal characterizations," in *2008 38th European Microwave Conference*, 2008: IEEE, pp. 757-760.

[2] S. C. Binari, P. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1048-1058, 2002.

[3] T. Tsuchiya, "Trapped-electron and generated interface-trap effects in hot-electron-induced MOSFET degradation," *IEEE transactions on electron devices*, vol. 34, no. 11, pp. 2291-2296, 1987.

[4] A. E. Parker and J. G. Rathmell, "Bias and frequency dependence of FET characteristics," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 2, pp. 588-592, 2003.

[5] Y. Alimohammadi *et al.*, "Pulse Profiling Active Load Pull Measurements," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020: IEEE, pp. 759-762.

[6] C. Roff *et al.*, "Analysis of DC–RF dispersion in AlGaN/GaN HFETs using RF waveform engineering," *IEEE Transactions on Electron Devices*, vol. 56, no. 1, pp. 13-19, 2008.

[7] M. Uren *et al.*, "Punch-through in short-channel AlGaN/GaN HFETs," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 395-398, 2006.

[8] J. Couvidat *et al.*, "Investigation of fast and slow charge trapping mechanisms of GaN/A1GaN HEMTs through pulsed IV measurements and the associated new trap model," in *2018 IEEE/MTT-S International Microwave Symposium-IMS*, 2018: IEEE, pp. 720-723.

[9] G. P. Gibiino *et al.*, "Double-pulse characterization of GaN-on-Sapphire FETs for technology development," in *2016 21st International Conference on Microwave, Radar and Wireless Communications (MIKON)*, 2016: IEEE, pp. 1-4.

[10] T. Husseini, A. Al-Rawachy, J. Benedikt, J. Bel, and P. Tasker, "Automating the accurate extraction and verification of the cardiff model via the direct measurement of load-pull power contours," in *2018 IEEE/MTT-S International Microwave Symposium-IMS*, 2018: IEEE, pp. 544-547.

[11] C. Arnaud, D. Basataud, J. Nebus, J. Teyssier, J. Villotte, and D. Floriot, "An active pulsed RF and pulsed DC load-pull system for the characterization of HBT power amplifiers used in coherent radar and communication systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 12, pp. 2625-2629, 2000.

[12] K. S. Singh, S. Kumar, and K. Nigam, "Impact of Interface Trap Charges on Analog/RF and Linearity Performances of Dual-Material Gate-Oxide-Stack Double-

Gate TFET," *IEEE Transactions on Device and Materials Reliability*, vol. 20, no. 2, pp. 404-412, 2020.

CHAPTER 5: INCORPORATING GATE-LAG EFFECTS INTO THE CARDIFF BEHAVIOURAL MODEL

5.1 INTRODUCTION

Modelling is crucial to analytically interpret small and large signal behaviour of the PA and facilitate circuit design. Different modelling techniques such as circuit-based models, behavioural models are provided to analyse the device behaviour at different stimulus conditions, to comprehensively analyse the device as its nonlinear behaviour depends on the stimulus condition. Besides circuit-based models, a behavioural model is a practical tool to transport device data from developing technology to CAD. The behavioural model as a data-based model is a black-box framework that reduces the prototyping cost and development time by allowing for the application of CAD tools much earlier in the design procedure.

Operating the device under pulse condition, allows to separately extract the thermal constant of the PA and trapping effect on the large signal behaviour of the device. Thus, pulse measurement provides an opportunity to extract a model for traps of the device, which is of interest to PA designers. Researchers provided comprehensive circuit-based models to increase the understanding of the traps in GaN [1-5]. However, no investigations were carried out whether the device trap behaviour can be incorporated into behavioural models.

In this chapter, the general Cardiff behavioural model is introduced, and its formulation is explained and then followed up with an investigation of how large-signal trapping effects can be incorporated into the Cardiff model. For this the capability of the new system to perform large-signal measurements active load-pull under RF pulsed conditions is utilised.

Active load-pull measurements are performed under pulsed DC/RF conditions, about the optimum load impedance for maximising output power, to extract the Cardiff model coefficients for a range of RF pulse conditions. The impact of gate-lag on the model coefficients is investigated at different pre-V_{GS} levels. The obtained data shows the model coefficients have a gate lag level dependency that can be readily modelled. Furthermore, Cardiff model coefficients variation within the pulse is also analysed to achieve the required discharging time constant of the traps. Finally, a new Cardiff model formulation is introduced that allows incorporating the gate-lag effect for the first time.

5.2 MEASUREMENT PROCEDURE

A typical pulsed DC/RF measurement sequence is shown in Figure *5-1*, which is similar to the sequence that is reported in chapter 4. However, acquisition starts after 10 ns delay (to exclude generators ripples) at the start of RF pulse to record 60 µs, and it moves within the pulse. All measurements have been performed on a 10W packaged transistor from Wolf speed device (CG2H40010). The pulse width of the applied RF signal is 300 µs to allow for low-frequency traps to be observed while the duty cycle is 3% to ensure minimal self-heating. Active load-pull measurement at 1.4 GHz fundamental frequency are conducted and all other harmonics and baseband frequencies are terminated with 50 Ω. Moreover, the device is biased at (V_{GS}= -3.5 V,

V_{DS}=28 V) under pulsed condition and pulse width of V_{GS} is 600 µs and V_{DS} is 400 µs and their duty cycle is 6 % and 4 %, respectively.

To investigate the impact of gate-lag on the measured RF performance, a DC pre-V_{GS} is considered, and shown in Figure *5-1*. In this case, the pre-V_{GS} value is kept on for the entire duration, between the V_{GS} DC-pulses. It is the value of this pre-V_{GS} that is varied to modify the trap levels associated with the gate-lag process.

To provide simultaneous RF pulses at the input and output of the DUT, two synchronised VSTs, referred to as G1 and G2, are employed. The G1 signal provides the device input stimulus and G2 the injected signal into device's output to achieve load-pull. All measurements are performed at 1.4 GHz fundamental frequency to obtain the Cardiff model coefficients at different gate lag levels, defined by the value of the pre-V_{GS}. The active load-pull measurements are performed around the optimum load for P_{out} with the measured load-pull contours covering an area around the optimum load for each gate-lag level. The input power during the characterisations is varied between -1 dB gain compression to 15 dB power back-off.

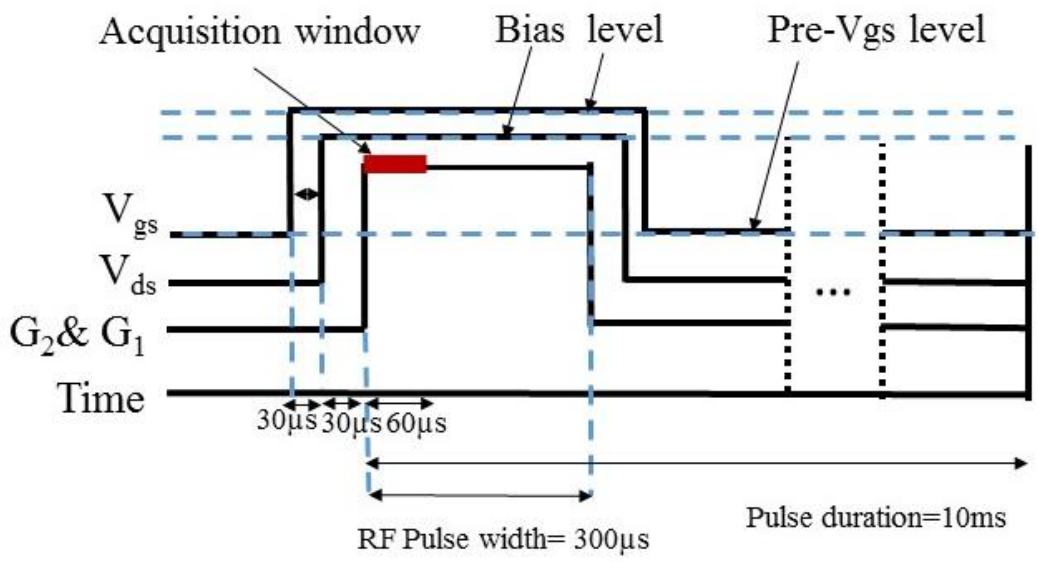

Figure 5-1: Sequencing of DC and RF pulses and the location of the data acquisition window during the measurements.

5.3 GENERAL FORMULATION OF CARDIFF MODEL

The Cardiff behavioural model is a polynomial based mathematic equation based on travelling waves, where the reflective B waves ($b_{p,h}$) are a function of stimulus scattering waves ($a_{p,h}$) and its harmonics, due to nonlinear behaviour of the device [6].

$$b_{p,h} = f(a_{1,h}, a_{2,h}) \qquad (5\text{-}1)$$

Where, h indicates the harmonic and p indicates the port number. It can be re-written to consider the magnitude and phase of each waves.

$$b_{p,h} = f(|a_{1,h}|, P_h, |a_{2,h}|, Q_h) \qquad (5\text{-}2)$$

where P_h and Q_h indicates the phase of $a_{1,h}$ and $a_{2,h}$, respectively [6]. As shown in (5-3) it can be normalised in terms of the phase of the $a_{1,h}$ waves to expand it into a power of the relative phase.

$$b_{p,h} = P_1^h \sum_{n=-\frac{N-1}{2}}^{n=\frac{N-1}{2}} \left\{ k_{p,h,n} \left(|a_{1,1}|, |a_{2,1}| \left(\frac{Q}{P}\right)^n \right) \right\} \quad (5\text{-}3)$$

with $k_{p,h,n}$ as the coefficients of the polynomial.

And finally input wave-based Cardiff model is represented in (5-4)

$$b_{p,h} = Q_{1,1}^h \sum_{r=0}^{r=\frac{w-h}{2}} \cdot \sum_{n=-(\frac{w-h}{2}-r)}^{n=h+(\frac{w-h}{2}-r)} L_{p,h,m,n}(a_{1,1}) |a_{2,1}|^m \left(\frac{Q_{2,1}}{Q_{1,1}}\right)^n \quad (5\text{-}4)$$

Where, 'm' and 'n' subscripts represent the coefficient related power wave's magnitude and phase exponent, respectively [7]. The parameters m=|n|+2r and w show the model order which determines the complexity and number of the model coefficients. The model order is usually selected to ensure that the Normalized Mean Square Error (NMSE) between modelled and measured $b_{p,h}$ is at least -40 dB. Selecting the higher-order model may cause over prediction, which will reduce the reliability of the model and introduce noise.

5.4 GATE-LAG DEPENDENCY OF THE CARDIFF MODEL

The current formulation of the Cardiff behavioural model is shown in (5-4), which does not consider the traps of the device. Within the RF signal, the charging level of the traps of the device varies over the pulse, therefore it would change the state of the device and cause variation of the device's incident and reflected scattering waveforms from the device. Hence, the model coefficients, which represent the state of the device, can be affected by the traps and their charging level. To extract the dependency of the Cardiff model coefficients to varying traps' charging levels, the device is pre-charged

during the "off" section of the pulses, then pulsed CW load-pull measurements at the fundamental frequency are carried out around optimum output power impedance.

The measured data is then used to extract the Cardiff model coefficients at fundamental frequency for both input and output ports. Figure *5-2* emphasises the difference of load-pull spirals that have been performed around optimum impedance for different pre-V_{GS} values. In both cases, the same RF signal $a_{2,1}$ was injected with the resulting device response $b_{2,1}$ producing a change in the achieved load impedances, hence demonstrating quantifiable and significant differences in measured data that is used for the extraction of Cardiff models, which is then used in ADS simulations. As the load impedances of a load-pull spiral are given by the Cardiff model, thus observed difference between the spirals indicates, Cardiff model coefficients are dependent on the gate-lag level.

As the load-pull contours are determined during the first 60 µs of the V_{GS} pulse, which is causing the device to dissipate power, any changes due to device heating has been minimised and the only remaining reason for the difference in the measured load-pull contours can be attributed from different traps charging levels. This highlights how the device's large-signal behaviour depends on pre-V_{GS} values, which change the trap levels within the device. Consequently, a new behavioural model which can deal with trapping effects and incorporates the gate-lag into the mathematical CAD-based analysis, can increase the accuracy of the nonlinear behavioural modelling.

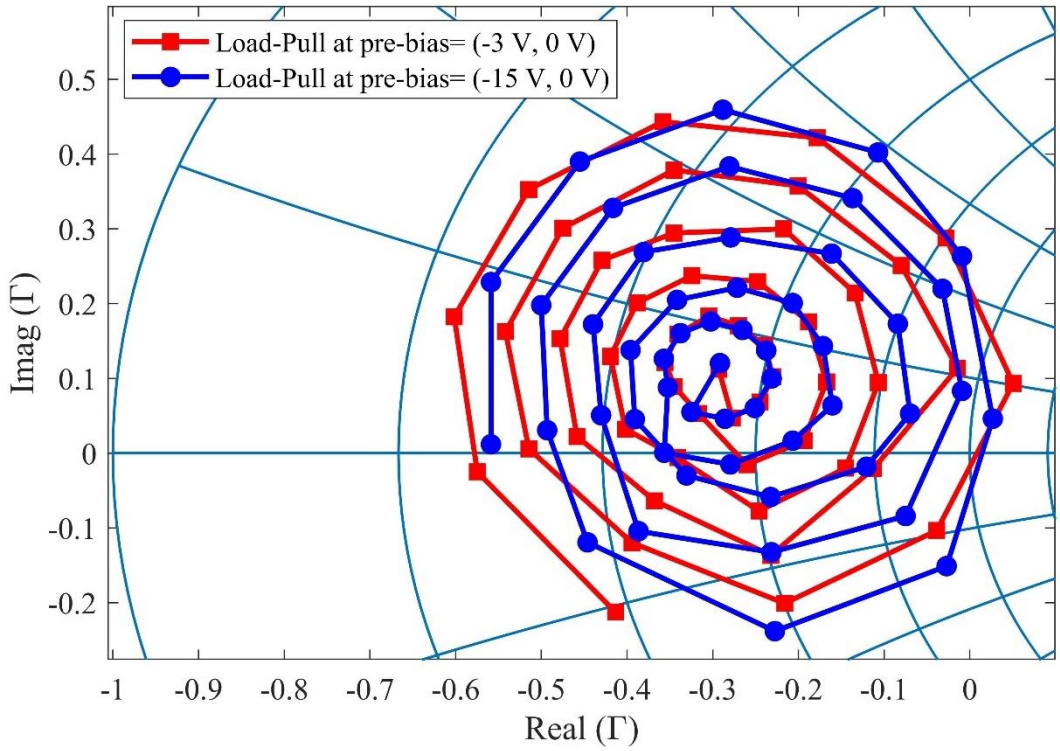

Figure 5-2: Differences of load-pull spirals at two different gate-lag levels. P_{in}= 12 dBm, PW= 300 µs, duty cycle= 3 %, bias point= (-3.5 V, 28 V), frequency= 1.4 GHz, 10 W device, acquisition length=60 µs, sample rate= 100 MS/s, 10 W device.

5.5 VARIATION OF MODEL COEFFICIENTS AT CONSTANT POWER

Cardiff model coefficients are extracted [8] at different gate-lag levels to model the device ($b_{p=2,h=1}$) response. Different PB conditions are applied to the device and extracted coefficients are listed in Table *5-1*. The model coefficients for modelling the input ($b_{p=1,h=1}$) are also represented in Table 5-2, which shows input model coefficients are independent of different gate-lag levels as their variation is not significant. Figure 5-3 and Figure *5-6* summarise the magnitude and phase variations of the output model coefficients over the 15 V range, in comparison with the reference pre-bias setting; PB=(-3 V,0 V). The reference pre-bias condition is chosen to compare other PBs with

continuous DC voltage on gate port condition as DC bias setting within the RF pulse was set to V_{GS}=-3.1 V and V_{DS}=28 V.

Table 5-1: Cardiff model coefficients at load side at different Pre-V_{GS} levels, P_{in}= 12 dBm, PW= 300 µs, duty cycle= 3 %, bias point = (-3.5 V, 28 V), frequency =1.4 GHz, 10 W device

Coefficients	**Pre-Bias Conditions**					
	(0 V, 0 V)	**(-3 V, 0 V)**	**(-6 V, 0 V)**	**(-9 V, 0 V)**	**(-12 V, 0 V)**	**(-15 V, 0 V)**
$L_{2,1,0,0}$	0.65+ 1.971*i	0.658+ 1.983*i	0.663+ 1.979*i	0.656+ 1.970*i	0.62+ 1.89*i	0.568+1.77 *i
$L_{2,1,1,1}$	0.158- 0.859*i	0.155 -0.917*i	0.1703 -0.941*i	0.189 -0.935*i	0.234 -0.846*i	0.281- 0.749*i
$L_{2,1,1,-1}$	0.020- 0.133*i	-0.030 -0.132*i	-0.041 -0.144*i	-0.036 -0.145*i	0.013- 0.130*i	0.075- 0.143*i
$L_{2,1,2,2}$	-0.18+ 0.015*i	-0.266 -0.108*i	-0.265 -0.181*i	-0.222 -0.184*i	-0.118 -0.0735*i	0.002+0.06 2*i
$L_{2,1,2,0}$	-0.227+ 0.248*i	-0.219+ 0.225*i	-0.239+ 0.219*i	-0.265+ 0.218*i	-0.339+ 0.248*i	- 0.394+0.20 1*i
$L_{2,1,3,1}$	-0.045+ 0.122*i	-0.069+ 0.143*i	-0.076+ 0.156*i	-0.066+ 0.15*i	0.012+ 0.136*i	0.050+0.09 4*i

Table 5-2: Cardiff model coefficients at source side at different pre-bias conditions, P_{in}= 12 dBm , PW= 300 µs, duty cycle= 3 %, , bias point = (-3.5 V, 28 V), frequency =1.4 GHz, 10 W device.

Coefficients	**Pre-Bias Conditions**					
	(0 V, 0 V)	**(-3 V, 0 V)**	**(-6 V, 0 V)**	**(-9 V, 0 V)**	**(-12 V, 0 V)**	**(-15 V, 0 V)**
$L_{1,1,0,0}$	-0.166363 -0.550345*i	-0.16633 -0.52045*i	-0.1612 -0.5305*i	-0.14636 -0.5201*i	-0.146367 -0.5105*i	-0.146363 -0.53345*i
$L_{1,1,1,1}$	0.00456079 +0.165378*i	0.004607 +0.1637*i	0.0045179 +0.1658*i	0.004569 +0.161178*i	0.004079 +0.165278*i	0.004579 +0.163278*i
$L_{1,1,1,-1}$	0.02899345 -0.048705*i	0.0289932 -0.04870*i	0.028919 -0.04875*i	0.028527 -0.048702*i	0.0289437 -0.046605*i	0.02992 -0.04705*i
$L_{1,1,2,2}$	0.02199 -0.152307*i	0.02179 -0.15307*i	0.02149 -0.152607*i	0.0213 -0.15265*i	0.02124 -0.152097*i	0.02156 -0.152354*i
$L_{1,1,2,0}$	0.023428 -0.042022*i	0.0231285 -0.04262*i	0.02344285 -0.04202*i	0.023425 -0.040126*i	0.02385 -0.04302*i	0.023521 -0.042062*i
$L_{1,1,3,1}$	0.01440 +0.035864*i	0.014432 +0.03864*i	0.014412 +0.03564*i	0.014423 +0.03564*i	0.01442 +0.035314*i	0.014398 +0.0353864*i

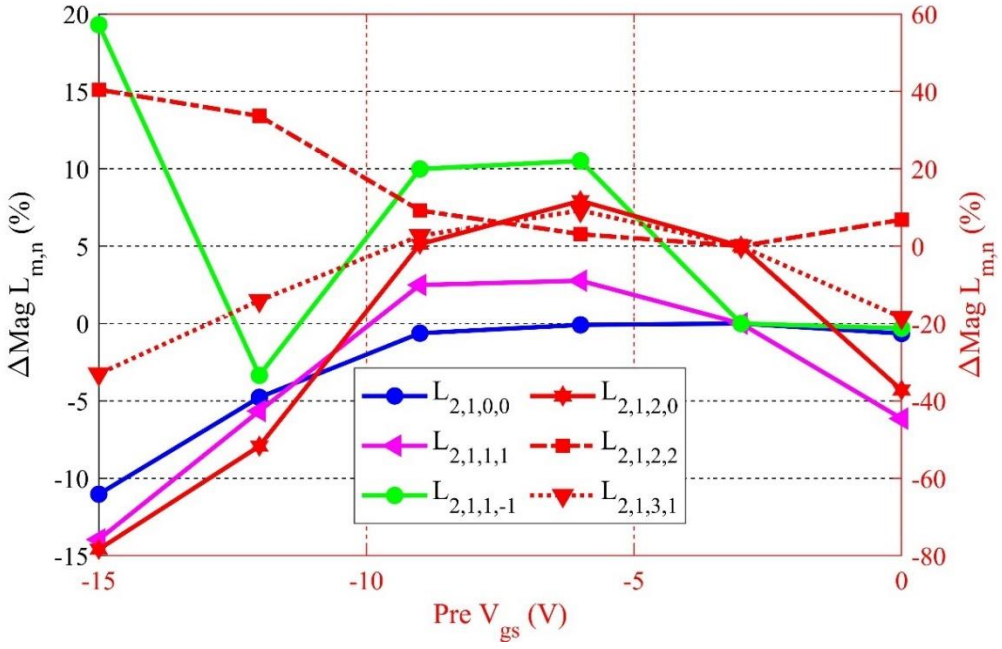

Figure 5-3: Differences of the Cardiff model coefficients' (L2,1,m,n) magnitude at different gate-lag levels in comparison with reference pre-bias setting (pre-V_{GS}= -3 V, pre-V_{DS}=0 V). Pre-V_{DS}=0 V, Pin=12 dBm, bias point=(-3.5 V,28 V), frequency = 1.4 GHz, acquisition length= 60 µs, 10 W device.

Figure 5-3 shows the magnitude of coefficients of the load side. As can be seen the magnitude of the $L_{2,1,0,0}$ decreases by up to 11% with decreasing pre-V_{GS} levels. $L_{2,1,0,0}$ is directly related to the gain of the device.

This is shown in Figure 5-4 where the gain of the device at different gate-lag levels declines with decreasing the gate-lag levels. This result is also consistent with the observed g_m of the transistor during PIV measurements with the IV curves being more compressed for increasing negative pre-V_{GS} values.

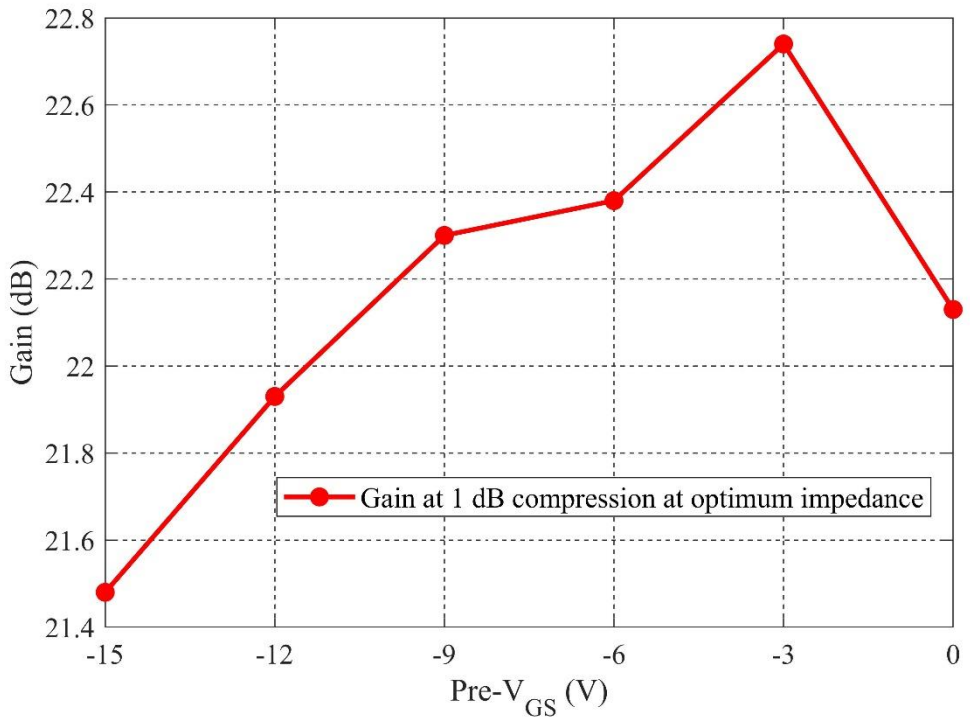

Figure 5-4: Gain of the PA at 1 dB compression level, 10 W device, PW= 300 µs, duty cycle= 3 %, load impedance is terminated at the optimum impedance of output power, bias point = (-3.5 V, 28 V), frequency =1.4 GHz, 10 W device.

$L_{2,1,1,1}$ is mentioned in [9] and it is linked to the location of the optimum impedance of the device. By decreasing the $L_{2,1,1,1}$, optimum impedance of the device moves toward

the centre of Smith chart. As can be seen in Figure 5-3 $|L_{2,1,1,1}|$ has an increasing trend with pre-V_{GS}. Most of the $|L_{2,1,1,1}|$ decrease occurs for pre-V_{GS} values below -9 V.

Figure *5-5* reveals the optimum impedance of the device under different gate-lag levels which shows a decreasing trend start at PB=(-9 V,0 V). In fact, the accelerated decrease below -9 V occurs for most output model parameters. As the device is in deep pinch-off for such low gate bias values, thermal effects can be excluded as a possible reason leaving device traps as the most likely explanation.

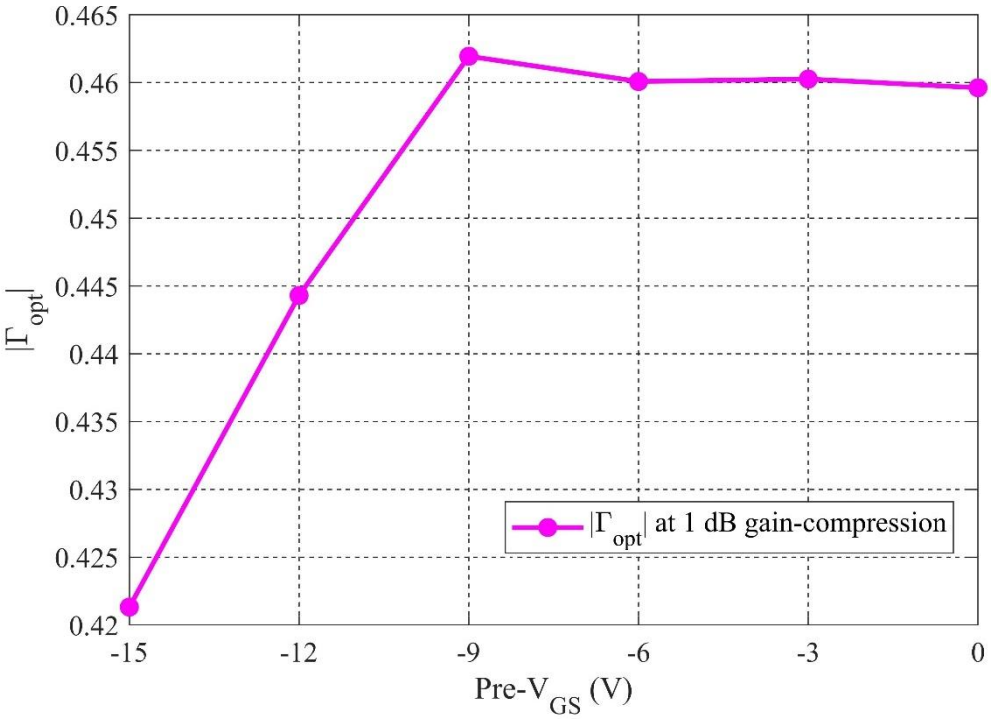

Figure 5-5: Distance of the optimum impedance of the device from centre of Smith-chart. Pin=12 dBm, PW= 300 µs, duty cycle= 3 %, bias point = (-3.5 V, 28 V), frequency =1.4 GHz, 10 W device.

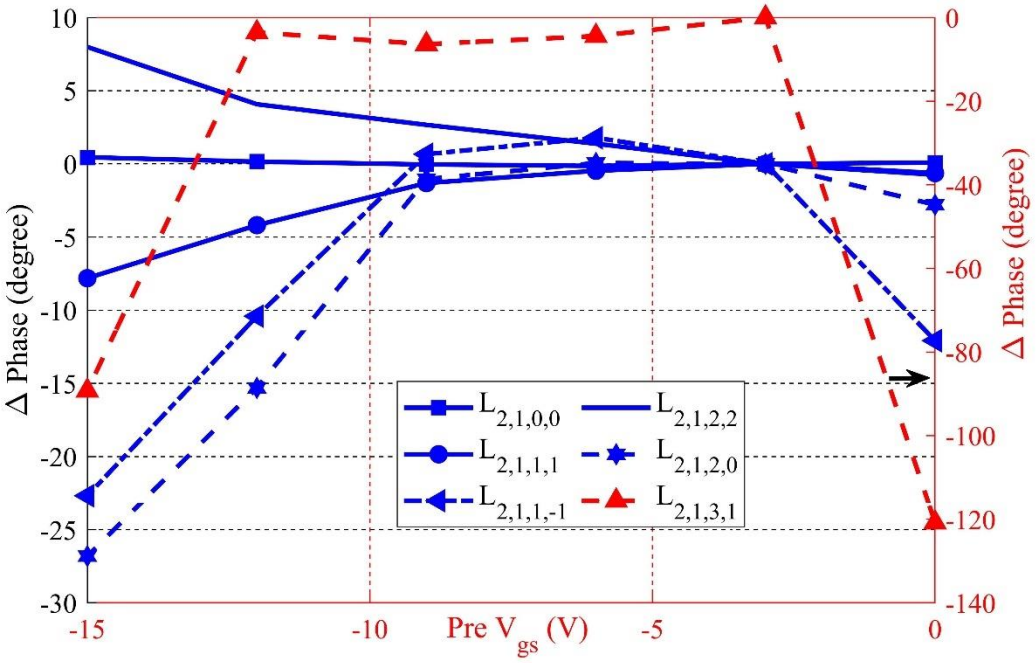

Figure 5-6: Phase differences of the Cardiff model coefficients at output port at different gate-lag levels in comparison with reference pre-bias setting (pre-V_{GS}= -3 V, pre-V_{DS}=0 V. Pre-V_{DS}=0 V, P_{in}=12 dBm, bias point = (-3.5 V, 28 V), frequency =1.4 GHz, 10 W device..

Figure *5-6* illustrates the phase variation of model coefficients due to various gate-lag levels. Based on achieved results, the phase of the $L_{2,1,0,0}$ remains constant over different gate-lag levels and the phase of the $L_{2,1,1,1}$ declines up to 6 degree. Consequently, charging the traps of the gate-source junction at the surface of the device change significantly only the phase of a subset of the coefficients. The changes tend to increase towards lower pre-V_{GS} values.

All the Cardiff model coefficient variations due to gate-lag can be modelled with second-order polynomials using an additional function of $Ø_{gs}$ as shown in (5-5)

$$b_{p,h} = Q_{1,1}^{h} \sum_{r=0}^{r=\frac{w-h}{2}} \cdot \sum_{n=-\left(\frac{w-h}{2}-r\right)}^{n=h+\left(\frac{w-h}{2}-r\right)} L_{p,h,m,n}(|a_{1,1}|, \emptyset_{gs}).|a_{2,1}|^{m}\left(\frac{Q_{2,1}}{Q_{1,1}}\right)^{n} \qquad (5\text{-}5)$$

With $L_{p,h,m,n}(|a_{1,1}|, \emptyset_{gs}) = C_{p,h,m,n} + D_{p,h,m,n}\emptyset_{gs} + E_{p,h,m,n}\emptyset_{gs}^2$.

and $\emptyset_{gs}$ representing the pre-V_{GS} values. Polynomial fitting is used to extract the expanded set of new coefficients ($C_{p,h,m,n}$, $D_{p,h,m,n}$ and $E_{p,h,m,n}$) at each P_{in} level. By following this process, the number of coefficients is tripled in the new model. It is interesting to note that this formulation enables to interpolate and extrapolate the Cardiff model coefficients in terms of the gate-lag control variable.

The new extended model is used to model the gate-lag variation of the coefficients and extract the polynomials. Pre-V_{GS} is changed from -15 V to 0 V with 3 V steps, and Cardiff model coefficients are extracted. Polynomials equations with different orders are examined to incorporate the gate-lag effect into the model with sufficient accuracy (-40 dB NMSE), then second-order equations are utilised to achieve sufficient accuracy.

Table 5-3: Accuracy of new model with different polynomial orders to incorporate the gate-lag effect

Polynomial order	**1st order**	**2nd order**	**3rd order**	**4th order**
Accuracy of modelled Γ (NMSE)	-34 dB	-47 dB	-50 dB	-55 dB

Table 5-3 shows the accuracy of different order polynomials, which clarifies second-order polynomial is accurate enough (accuracy is higher than -40 dB) to reduce the complexity and model the gate-lag effect. Polynomials are determined for BP= [(0 V,0 V), (-3 V,0 V), (-6 V, 0 V), (-9 V, 0 V), (-12 V, 0 V), (-15 V, 0 V)] and then used to extrapolate a model prediction at pre-V_{GS}= -18 V to evaluate the accuracy of the model by comparing it with measured values.

5.6 GATE-LAG PREDICTION

In this section accuracy of the achieved model is derived over a 15 dB dynamic range with power levels including a 15 dB back-off and 1 dB gain compression.

Figure *5-7* presents the comparison between the measured and modelled load-pull contours that were generated by using extrapolated Cardiff model's coefficients ($L_{2,1,m,n}$) for $Ø_{gs}$= -18 V at 1 dB gain compression (P_{in}=12 dBm). It shows, the new Cardiff model has accurately predicted the variation of load-pull contours resulting from different gate-lag levels with the measured $\Gamma_{measured}$ and predicted $\Gamma_{modelled}$ load impedances showing an excellent agreement with an NMSE of -49 dB.

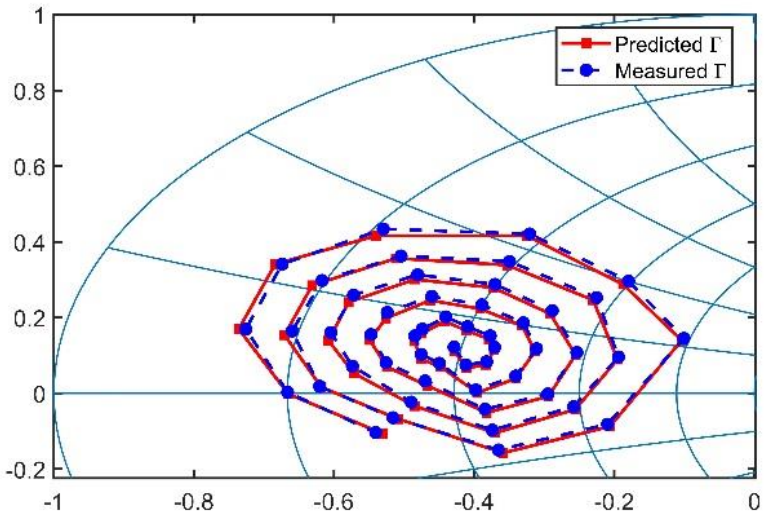

Figure 5-7: Comparison between the new incorporated Cardiff model and measurement results. Pre-V_{GS}= -18 V, Pre-V_{DS}=0 V, P_{in}=12 dBm, bias point = (-3.5 V, 28 V), frequency =1.4 GHz, 10 W device.

This ability to account for the gate-lag dependence of the Cardiff model coefficients is also investigated as a function of P_{out} levels. Figure *5-8* demonstrates the accuracy of the prediction achieved over a 15dB output power dynamic range. The computed Cardiff model coefficients predicted the device behaviour during load-pull with a

deviation below -47 dB NMSE, therefore the achieved model can precisely analyse the trap's effect of the device when traps are charged at different gate-lag levels over a 15 dB dynamic range. Hence, the new model increases the prediction accuracy from -10 dB to -47 dB by using only a quadratic polynomial to incorporate the gate-lag effect into the Cardiff model coefficients and can incorporate surface traps effect into Cardiff model over a 15 dB dynamic range.

As the first order Cardiff model is the same as X-parameter, thus by setting the model's order to one and extracting quadratic function for X_F, X_T, X_S, X-parameters can also accurately model the traps.

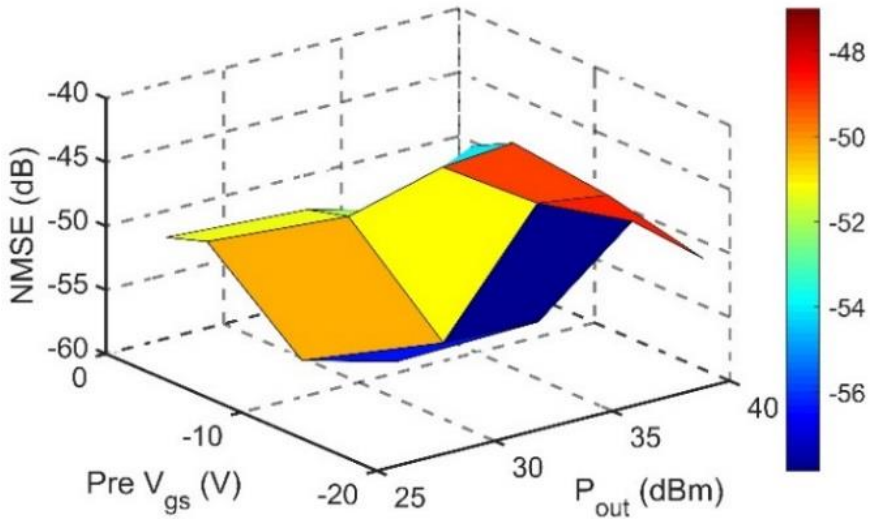

Figure 5-8: Accuracy of the new model over 15 dB output power dynamic range and gate-lag levels, bias point = (-3.5 V, 28 V), frequency =1.4 GHz, 10 W device.

5.7 VARIATION OF CARDIFF MODEL COEFFICIENTS IN TIME-DOMAIN

In the previous section, it was shown that the extracted Cardiff model coefficients were sensitive to the initial gate-lag levels. In addition, an investigation is carried out to illustrate the recovery of the Cardiff model coefficients towards their CW values over the duration of the RF pulse.

This is achieved by extracting Cardiff model coefficients from pulsed DC/RF load-pull measurement performed at different time locations within the pulse. Here, the 60 µs RF measurement window is moved within the DC/RF pulse with 60 µs steps. By moving the acquisition window within a pulse, 5 sets of Cardiff models are extracted for each timeslot of pulse. Figure *5-9* and Figure *5-10* illustrate the magnitude and phase changes of the output and input of measured $L_{p,1,0,0}$ Cardiff model coefficients as a function of time for different pre-V_{GS} levels. As it has been shown in the previous chapter and in [8, 10] by applying the higher gate-lag or drain-lag levels to the device, the overall reflected waveforms from input and output of the device are more constant and device response variation within the pulse decreases. Figure *5-9* shows similar behaviour, however, an accelerated decrease in $|L_{2,1,0,0}|$, obtained for $Ø_{gs}$ = 0 V and -15 V, occurs about 200 µs after the start of the RF pulse. By applying the higher negative $Ø_{gs}$, the variation of $|L_{2,1,0,0}|$ decreases within the pulse and the $|L_{2,1,0,0}|$ at $Ø_{gs}$ = -25 V is almost constant throughout the entire RF pulse. Also, all $|L_{2,1,0,0}|$ traces converge onto the same value at about 250 µs after the start of the RF pulse. Applying the higher gate-lag level to the device and pre-charging the traps leads to decrease the starting value of the $|L_{2,1,0,0}|$ which is in line with achieved results of previous sections.

In contrast to the $|L_{2,1,0,0}|$ behaviour, the $L_{2,1,0,0}$ phase remains constant within the entire RF pulse for all $Ø_{gs}$ levels. Reported results of chapter 4 have demonstrated that the overall observed changes in the device response to varying pre-V_{GS} are not due to a rise in device temperature. Therefore, the most likely explanation for the sudden change in device output at T=250 µs are changes of trap states.

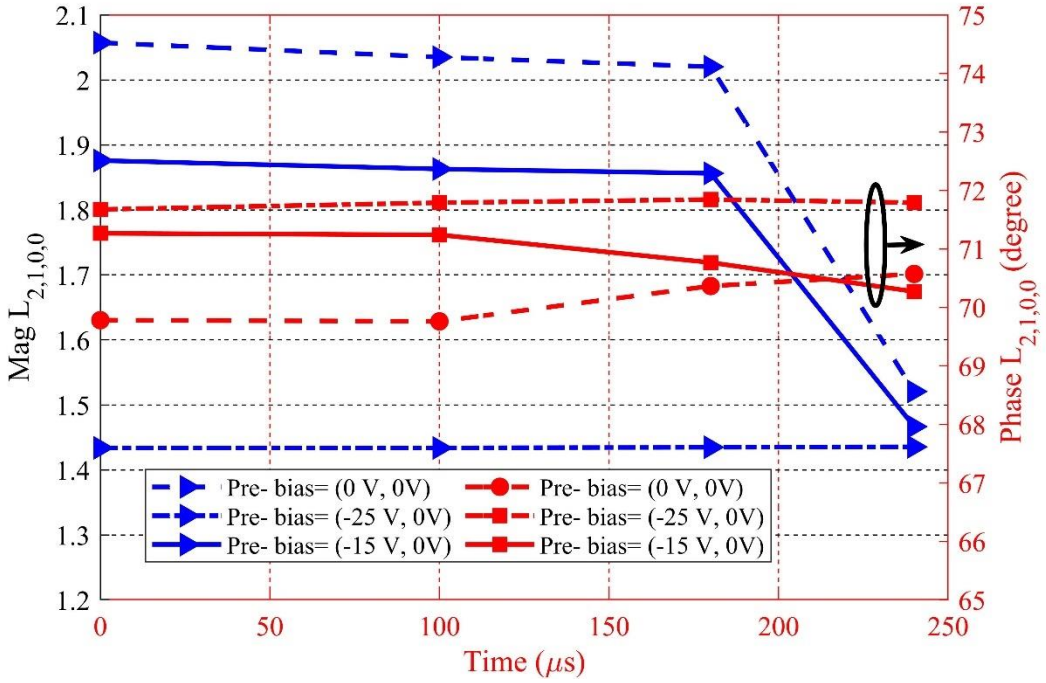

Figure 5-9: Variation of $L_{2,1,0,0}$ at the output of the device within the pulse at different gate-lag levels. P_{in}= 7 dBm, bias point = (-3.5 V, 28 V), frequency =1.4 GHz, 10 W device.

Figure *5-10* shows the variation of the $L_{1,1,0,0}$ at different gate lag levels within the RF pulse. As can be seen, the variation of $L_{1,1,0,0}$ within the pulse is much smaller and unaffected by the different gate-lag levels and over the duration of the RF pulse. Hence, the model parameters effecting the variation of the input charge and current appear to be insensitive to gate-lag.

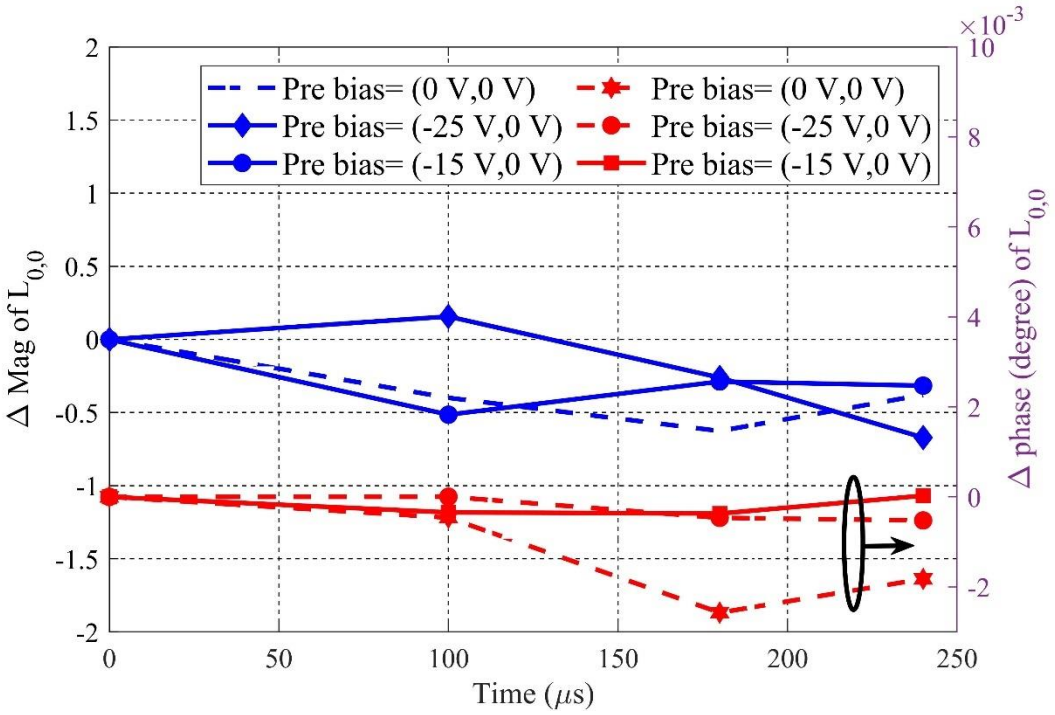

Figure 5-10: Variation of $L_{1,1,0,0}$ at the input of the device within the pulse at different gate-lag levels. P_{in}=7 dBm, bias point = (-3.5 V, 28 V), frequency =1.4 GHz, 10 W device.

5.8 CHAPTER SUMMARY

In this chapter, the basic formulation of the a-based Cardiff model is pointed out and by performing advanced pulsed active load-pull measurements with pre-pulsing technique, gate-lag dependency of the Cardiff model is illustrated. The observed variation of the coefficients is linked with the large-signal characteristics of the device. For instance, as $|L_{2,1,0,0}|$ is related to the gain of the device, it is shown they have similar trend at different gate-lag levels. To model the gate-lag effect on the coefficients, curve fitting techniques is utilised and accounted for using a quadratic polynomial providing a very high accuracy over a large dynamic range. New Cardiff model can incorporate the gate-lag effect by tripling the number of coefficients and its accuracy is more than -47 dB (NMSE) over 15 dB output power dynamic range. Moreover, to analyse how coefficients vary in time-domain, $L_{2,1,0,0}$ is investigated in different

timeslots of the pulse, and conducted measurements within the pulse at different pre-bias conditions show the $|L_{2,1,0,0}|$ decreases within the pulse and the coefficients become more stable by applying the negate pre-V_{GS}. The measured data quantified the different gate-lag levels leading to variation of the Cardiff model coefficient at least 11% in magnitude, thus it expresses the importance of incorporating the gate-lag effect into the Cardiff behavioural model.

5.9 REFERENCES

[1] O. Jardel *et al.*, "An electrothermal model for AlGaN/GaN power HEMTs including trapping effects to improve large-signal simulation results on high VSWR," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 12, pp. 2660-2669, 2007.

[2] A. Prasad, M. Thorsell, H. Zirath, and C. Fager, "Accurate modeling of GaN HEMT RF behavior using an effective trapping potential," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 2, pp. 845-857, 2017.

[3] S. C. Binari *et al.*, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 465-471, 2001.

[4] J. Couvidat *et al.*, "Investigation of fast and slow charge trapping mechanisms of GaN/A1GaN HEMTs through pulsed IV measurements and the associated new trap model," in *2018 IEEE/MTT-S International Microwave Symposium-IMS*, 2018: IEEE, pp. 720-723.

[5] M. Khan, W. Qian, D. Huang, L. Li, and F. Lin, "Enhanced GaN HEMT large-signal model with self-heating and trapping effects for power amplifier design," in *2015 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, 2015: IEEE, pp. 1-3.

[6] A. Al-Rawachy, "Developing a multi-tone load-pull system for the direct extraction of Cardiff behavioural model coefficients," Cardiff University, 2019.

[7] T. Husseini, A. Al-Rawachy, J. Benedikt, J. Bell, and P. Tasker, "Global Behavioural Model Generation Using Coefficients Interpolation," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019: IEEE, pp. 200-203.

[8] Y. Alimohammadi *et al.*, "Incorporating Gate-Lag Effects into the Cardiff Behavioural Model," in *2020 50th European Microwave Conference (EuMC)*, 2021: IEEE, pp. 684-687.

[9] S. Woodington, R. Saini, D. Williams, J. Lees, J. Benedikt, and P. J. Tasker, "Behavioral model analysis of active harmonic load-pull measurements," in *2010 IEEE MTT-S International Microwave Symposium*, 2010: IEEE, pp. 1688-1691.

[10] Y. Alimohammadi *et al.*, "Pulse Profiling Active Load Pull Measurements," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020: IEEE, pp. 759-762.

CHAPTER 6: CONCLUSION

6.1 CONCLUSION

The work presented in this thesis has successfully achieved its objectives and developed a high-speed and user-defined pulsed measurement system to characterise the high-power devices. In particular, an advanced measurement system allowed to investigate the trapping effect by performing complex and high-speed load-pull measurements. It provided unique features to investigate the large-signal behaviour of traps by conducting load-pull measurements under pulsed DC and RF excitations.

Chapter 2 has summarised the evolution of the pulsed measurement systems and their configuration to conduct different types of measurements from DC to higher frequencies. It has been mentioned by performing pulsed measurements, thermal and trapping phenomenon in PAs can be characterised and some of the achievements of the investigation around trapping effect has been pointed out. Traps can affect the large-signal behaviour of the device, and change its time-domain behaviour with different time scales. Cardiff behavioural model was also introduced in this chapter and some of its developments were mentioned, to show the impact of achievements through this thesis.

In chapter 3 measurement system setup was introduced and verified. The designed test-set to perform load-pull measurements at baseband, fundamental, and the second harmonic was presented in detail, including the major specifications of the passive components used in the test-set. An efficient approach on the VST system to apply signals and record them under pulsed was proposed and explained in detail. Pulse

measurement system typically was validated by some performance metrics such as pulse-to-pulse stability, transient time, and amount of memory usage. These metrics have been measured and illustrated in this chapter. Moreover, some of the performance metrics of measurement systems such as noise floor, dynamic range were verified to provide limitations of the measurement system.

Trapping effect on the time-domain variations of the input and output of the device was explored in chapter 4. It was shown the variation in device mostly related to the traps of the device and by pre-charging the traps before applying the intended signals, output and input of the device are more constant in time-domain, which led to stabilise the optimum load impedance. In this chapter, a new viewpoint to linearity investigation was presented, which analyse it as a factor of time by measuring DPR and IMDs at different timeslots of the pulses and was shown by pre-charging the traps at pre-$V_{DS} > 2V_{DS}$ can minimise the variation of IMDs and increase the linearity of the device up to 5 dB in back-off levels. Achieved results proposed drain-lag effect is more severe than gate-lag, however by pre-charging the surface layers traps output impedance variation can be decline by 3 %.

Chapter 5 was focused on the development of the Cardiff behavioural model to include the gate-lag effect and provide a behavioural model for surface traps. Sensitivity of 3rd order Cardiff model coefficients to various gate-lag levels has been demonstrated. It also indicated the X-parameter dependency to gate-lag levels. Demonstrated results suggested the relation between the applied pre-V_{GS} (gate-lag) and coefficients can be modelled by using a quadratic function and it improves the accuracy of the model from -10 dB to -40 dB. Time-domain variations of coefficients were also shown by applying higher gate-lag levels to the device output coefficients variation plunges within the

pulse. All observed behaviour of Cardiff model coefficients during the active load-pull measurements were in line with related large signal performance metrics, and with observations that has been presented in chapter 4.

6.2 FUTURE WORK

The developed flexible and user-defined IQ-based measurement system in chapter 3 allows to deeply characterise the device over a wide range of frequencies, which will be considered in the future. Tuning the device load impedance at IF to its optimum value can affect the efficiency and linearity of the device, thus developed system can be used to investigate a novel approach to increase the performance of the device. Moreover, increasing the employed bandwidth up to 1 GHz and performing active load-pull measurements will report new data for an active load-pull system, which will be considered in the future. Another interesting topic for future research is, tailoring the multi-tone signals to be generated with the same statistical metrics as 5G signals, then performance metrics of the device can be driven under commercial cellular communication conditions and load-pull measurements will be conducted on real-world commercial signals.

Chapter 4 was focused on the trapping effect on the linearity and optimum impedance variation of the device in the time-domain, Its results provide an interesting approach for RFPA designers to increase the performance of the device during the long-time operation, by pre-charging the device. Therefore, incorporating the pre-charging mechanism into the design of power amplifiers will be beneficial for RFPA designer can emerge a novel approach in PA design. Moreover, an interesting investigation can be conducted on the characterising the trapping and thermal effect on the harmonics of the device.

Recorded data and added capability to the measurement system are used in chapter 5 to incorporate the surface layer traps into the Cardiff behavioural model and demonstrate how traps can affect nonlinear behavioural models. This can be expanded to include the drain-lag effect into the Cardiff behavioural model, which can explain the deeper layer traps effect and model them. The proposed method on pre-filling the traps at different levels by using DC signals can be expanded to investigate traps behaviour under RF signal, by providing the current and voltage waveforms.

It is shown the Cardiff model coefficients are sensitive to the parameters that can be changed by pulse measurements (e.g., traps level). It is interesting to provide a time-variant nonlinear behavioural model, for the first time, to incorporate thermal, self-heating effects, by providing time-variant polynomials. This can be possible by performing load-pull measurements at different timeslots of the pulse and find a time-variant function to fit the measured coefficients. Moreover, by changing the pulse width and package temperature of PA, the self-healing and thermal effect on the Cardiff model can be achieved, which can make the Cardiff model as an inclusive time-variant model.