Gate bias voltage dependence of Cardiff admittance model in Ka-band GaAs pHEMTs

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***Abstract*—This paper analyzes the dependence vs. gate bias voltage of the coefficients of the Cardiff model in the admittance form. The load-pull measurement data used to extract the model, inclusive of input power sweep, is taken on a GaAs pseudomorphic high electron mobility transistor (pHEMT) at the frequency of 36 GHz. The gate bias is swept in class C and in class AB and a different set of coefficients is extracted at each bias point.**

It is observed that the model coefficients can be fitted vs. bias using a linear function within the class C and class AB ranges. This allows to predict the model coefficients within a range of bias voltages with load-pull measurements at only a few bias points, significantly reducing the measurement effort. Using the predicted coefficients, the model shows a global error lower than -31 dB for the DC and fundamental output current.

I. Introduction

The use of millimeter-wave frequencies is gaining traction in a number of applications, ranging from ground to satellite communications, radar, and imaging, thanks to the good availability of bandwidth and the possibility to miniaturize circuits and antennas. The power amplifier (PA) remains the most critical component in the transmitter, heavily affecting the quality of the transmitted signal and the power consumption.

Advanced PA architectures, such as the Doherty PA [1], can be used to improve the performance for specific applications. However, they require a significant effort in the design that must rely on accurate device models that can predict the response over a range of operating conditions, especially bias voltage.

State function models, such as the Angelov model [2], can achieve great accuracy and are extremely versatile, but extracting them is a complex and lengthy operation, involving several characterization steps and a final validation by means of load-pull measurements. Alternatively, load-pull measurement results can be used directly in the design phase, but this is not trivial when designing advanced PA architectures. As an alternative bridging the two options, behavioural models can directly represent measured data in a simulator, allowing to simulate advanced PA architectures [3], and leading to a quicker turn-around between device samples availability and design compared to more complete models. An example of a behavioural model is the Cardiff model [4], which is based upon rigorous mathematical formulation supported by mixing theory.

Being a behavioural model, the Cardiff model requires the measurement domain to cover the possible application domain. Therefore, the model must be extracted on measurements at different gate bias voltages to ensure a valid model when designing advanced PAs. Finding a way to minimize the number of required measurements is therefore important in order to accelerate the model extraction procedure. The dependence of the Cardiff model vs. gate bias has been presented in [5], and parameters' fitting vs. gate bias was adopted to reduce the number of measurements needed. In this work, we apply a similar concept to the admittance form of the Cardiff model, i.e. based on voltage and current rather than power waves. The use of the admittance model is an important step forward since it is a preferred form of the model for having a closer link to the device physics, allowing in future to perform frequency and size scaling in a more accurate way than with a power wave-based model [6].

II. Model

The Cardiff model is used in its admittance form with an order of 5 [7], expressing the output fundamental current as:

$$I_{21} = \angle V_{11} \sum_{\mathrm{t}=0}^{1} \sum_{\mathrm{r}=0}^{1} \sum_{\mathrm{n}=\mathrm{n}_{\min}}^{\mathrm{n}_{\max}} L_{2,1,\mathrm{x},\mathrm{m},\mathrm{n}} \left|V_{11}\right|^{x} \left|V_{21}\right|^{\mathrm{m}} Q_{21}^{\mathrm{n}} \quad (1)$$

and the DC current as:

$$I_{20} = \sum_{\mathrm{t}=0}^{1} \sum_{\mathrm{r}=0}^{1} \sum_{\mathrm{n}=\mathrm{n}_{\min}}^{\mathrm{n}_{\max}} L_{2,0,\mathrm{x},\mathrm{m},\mathrm{n}} \left|V_{11}\right|^{x} \left|V_{21}\right|^{\mathrm{m}} Q_{21}^{\mathrm{n}} \quad (2)$$

where V_{11} is the fundamental input voltage, V_{21} is the fundamental output voltage, and Q_{21} is a unitary phasor with phase as the difference between output and input voltage. The coefficients m and x are calculated as:

$$\begin{cases} m = |n| + 2r \\ x = |h - n| + 2t \end{cases} \quad (3)$$

with h=1 for fundamental and h=0 for DC. The range of n is:

$$\begin{cases} n_{\min} = -(mix - t - r) \\ n_{\max} = h + (mix - t - r) \end{cases} \quad (4)$$

where $mix = \left\lfloor \frac{5-h}{2} \right\rfloor$. A model, i.e., a set of L coefficients (16 for I_{21} and 12 for I_{20}), can be extracted for each bias point at which the load-pull measurements have been performed, using

a least-mean square algorithm since the model is linear in its parameters. The insertion of the input voltage in the model is due to the impossibility of performing a "voltage pull" on high frequency devices that would give a constant input voltage when sweeping the output voltage. Therefore, as explained in detail in [6], including the input voltage in the model and performing the load-pull characterization over a few dBs of input power solves this issue providing a sufficient variation of input voltage for the model to be fitted.

III. Load-pull measurements

An active open-loop load-pull system was used for the measurements presented in this paper, see picture in Fig. 1.

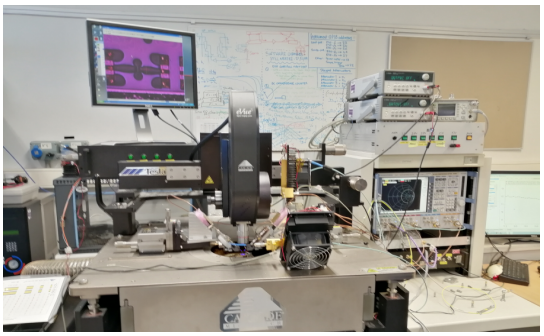
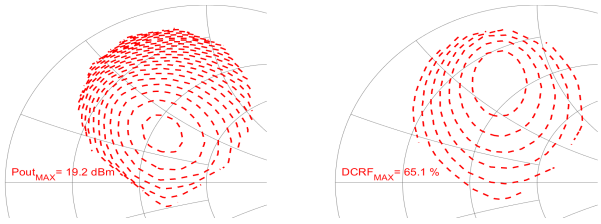
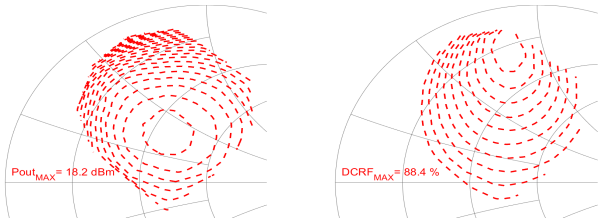


Fig. 1. Active open-loop load-pull measurement set-up



(a) (b)

Fig. 2. Power (a) and DCRF (b) measured contours at V_{GG}=−0.4 V (class AB). 0.25 dBm and 5 % contours, respectively. Drive power of 15.6 dBm.



(a) (b)

Fig. 3. Power (a) and DCRF (b) measured contours at V_{GG}=−1.25 V (class C). 0.25 dBm and 5 % contours, respectively. Drive power of 17.7 dBm.

The device under test was placed on a probe station, and the measurement process driven by the Mesuro ALPS software, using the receivers and sources of a Rohde & Schwarz ZVA67 vector network analyzer. The driver and load-pull PAs are the RFLUPA28G42GA from RF-LAMBDA.

The load-pull measurements were conducted on a GaAs 6x25 µm pHEMT fabricated with the Qorvo QPHT09 process, at the frequency of 36 GHz and at the drain bias voltage of 3.5 V. The gate bias voltage was swept between −0.65 V and −0.4 V, with a step of 50 mV, for the class AB range, and between −1.25 V and −1.0 V, with a step of 50 mV, for the class C range. The power drive is swept on a 6 dB and 3 dB range in class AB and class C, respectively, and pushed to around 1.5-2 dB compression.

Fig. 2 and Fig. 3 show the measured output power and efficiency contours at V_{GG}=−0.4 V and V_{GG}=−1.25 V, respectively.

IV. Fitting of coefficients vs. bias point

The extracted model coefficients can be plotted vs. V_{GG}, and they all result to be very close to a linear relationship in both the class AB and C ranges. Fig. 4 shows some of the low order coefficients. For example, $L_{2,1,1,0,0}$ represents the trans-admittance between input voltage and output current, and its real part is related to the trans-conductance of the device. Therefore, it makes sense for it to be increasing with bias voltage in both the class AB and class C ranges. On the other hand, its imaginary part is expected to be less dependent on the gate bias voltage. $L_{2,1,0,1,1}$ is related to the output admittance of the device, and also shows only a loose dependence on gate voltage.

Having identified a linear trend vs. bias for the model coefficients, we can reduce drastically the number of bias points measured, and determine the coefficients at non-measured bias-points using a linear function fitting the measured points, that is in general expressed as:

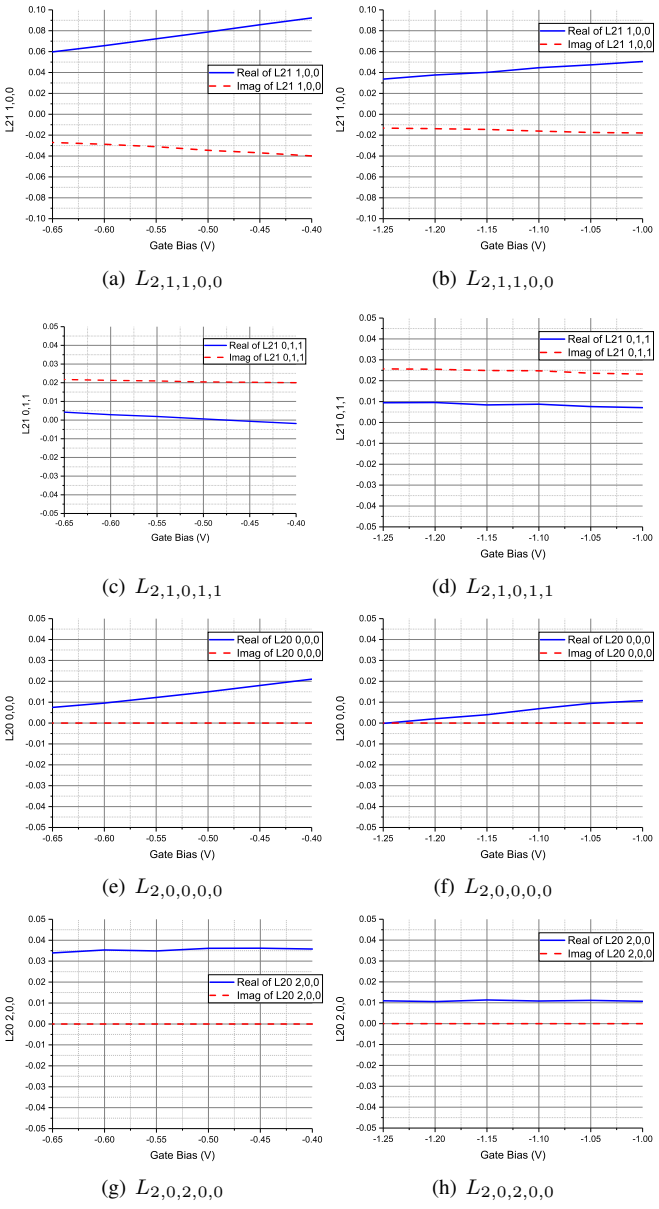
$$\begin{cases} L_{2,1,\mathrm{x,m,n}}\left(V_{GG}\right) = m_{1,\mathrm{x,m,n}} V_{GG} + q_{1,\mathrm{x,m,n}} \\ L_{2,0,\mathrm{x,m,n}}\left(V_{GG}\right) = m_{0,\mathrm{x,m,n}} V_{GG} + q_{0,\mathrm{x,m,n}} \end{cases} \tag{5}$$

where m is the slope coefficient and q is a reference gate voltage. These approximations are valid within defined V_{GG} ranges.

To prove that this method is effective, we use the coefficients at the extremes of the class AB and C ranges as data points for the model extraction, and determine the values of m and q. Then, we calculate the model at any bias points not used in the model extraction using (5) and validate it against the measurements at that bias point. For class AB, we use the measurements at V_{GG}=−0.65 V and V_{GG}=−0.4 V for the model extraction, while for class C we use V_{GG}=−1.25 V and V_{GG}=−1 V.

The validation is performed at all the other points measured, and the resulting normalised mean square error (NMSE) for fundamental and DC output current is reported in Fig. 5.

Fig. 6 and Fig. 7 show the measured vs. modelled output power and efficiency contours for V_{GG}=−0.5 V and V_{GG}=−1.1 V, respectively. The good agreement shown is related to the very low NMSE obtained when modelling the output DC and fundamental currents. It is important to remark that the measured data at these bias points was not used to extract the models, hence this is a proper validation of the model accuracy.



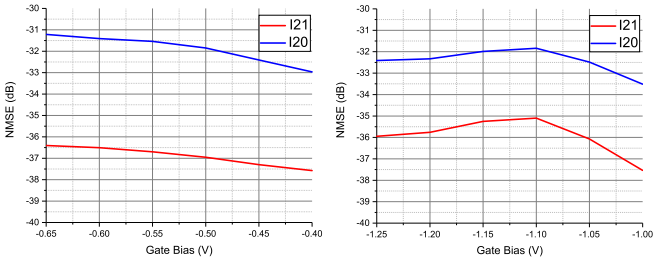
(a) $L_{2,1,1,0,0}$ (b) $L_{2,1,1,0,0}$

(c) $L_{2,1,0,1,1}$ (d) $L_{2,1,0,1,1}$

(e) $L_{2,0,0,0,0}$ (f) $L_{2,0,0,0,0}$

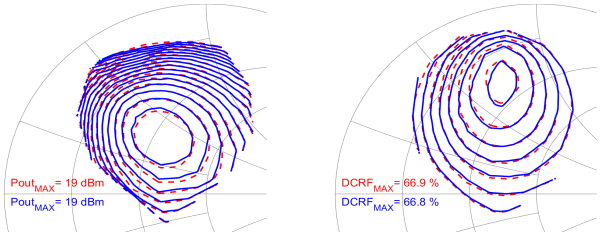
(g) $L_{2,0,2,0,0}$ (h) $L_{2,0,2,0,0}$

Fig. 4. Some of the extracted coefficients vs. V_{GG} in the class AB (left column) and class C (right column) ranges.



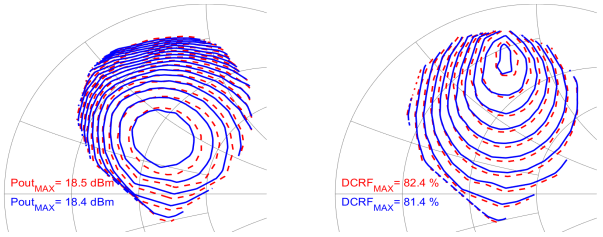
(a) (b)

Fig. 5. Model accuracy in terms of NMSE vs. gate bias voltage, for the class AB model (a) and the class C model (b). The model has been extracted at the extremes of the voltage ranges only, and the models within the ranges are extracted by linearly fitting the coefficients.



(a) (b)

Fig. 6. Power (a) and DCRF (b) contour comparison between modelled (blue solid) and measured (red dashed) at V_{GG}=−0.5 V. 0.25 dBm and 5 % contours, respectively. Drive power of 15.6 dBm.



(a) (b)

Fig. 7. Power (a) and DCRF (b) contour comparison between modelled (blue solid) and measured (red dashed) at V_{GG}=−1.1 V. 0.25 dBm and 5 % contours, respectively. Drive power of 17.7 dBm.

V. Conclusion

The paper has shown that the Cardiff admittance model coefficients for a millimetre-wave GaAs pHEMT can be linearly interpolated vs. gate bias voltage within class AB and class C ranges. This opens the possibility of applying frequency and periphery scaling. More work will be required to identify a method to extend the admittance model across class AB and C ranges and a larger input drive dynamic range.

Acknowledgment

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