Extendable Space-Type Switched-Capacitor Multilevel Inverter with Fault-Tolerant Capability

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Abstract

Low reliability is one of the main concerns in terms of multilevel inverters (MLI) due to the presence of a large number of switches and capacitors. Therefore, the fault-tolerant operation of MLIs has recently gained a great deal of attention. An extendable space-type switched-capacitor multilevel inverter topology with fault-tolerant characteristics is proposed in this paper. The proposed inverter employs a single direct-current voltage source and three capacitors to output staircase voltage levels with low distortion. The proposed topology is capable of tolerating open-circuit faults due to the separated charging paths of the inverter. Under pre-fault and post-fault operations, it preserves capacitor voltage balancing, voltage boost capability, as well as the ability to supply inductive loads. Furthermore, the voltage stresses of the switches and the voltage ripple of the capacitors are decreased or remain under post-fault operations. The proposed topology has been validated with a laboratory prototype in both dynamic and steady-state operations.

Keywords: Reliability, Multilevel inverter, Extendable, Switched-capacitor, Fault-tolerant, Single source

1 Introduction

Multilevel inverters have been widely applied in the fields of renewable energy generation systems (especially in photo-voltaic systems), power distribution systems, electric vehicles, and so on [1]. The main advantages of these topologies include realizing staircase voltages with a lower total harmonic distortion, mitigating electromagnetic interference, and allowing for switches with lower voltage stress [2].

Neutral-point clamped (NPC), flying-capacitor (FC), and cascaded H-bridge (CHB) multilevel inverters have been thoroughly studied as traditional multilevel inverters [3]. However, a large number of diodes or capacitors is needed in NPC and FC multilevel inverters [4]. In addition, requiring a voltage self-balance or extra charging circuit for capacitors raises their complexity and cost [5]. Multiple isolated sources are utilized in CHB multilevel inverters to increase the output levels [6]. Moreover, the low voltage gain (the ratio of the maximum output voltage to the input voltage) and single extension style limit the development of traditional multilevel inverters. In order to solve these problems, novel multilevel inverters based on the switched-capacitor technique have been proposed and developed. The capacitors of switched-capacitor multilevel inverters (SCMLIs) have been charged in parallel with a direct-current (DC) source and discharged in series to obtain high voltage gain [7]. In addition, SCMLIs output the same levels with fewer devices than the traditional multilevel inverters, and they have the advantages of capacitors voltage self-balance and low voltage ripple [8,9].

Different topologies of SCMLIs have been proposed in the past decade. Staircase boost units based on the switched-capacitor technique were applied in the topologies proposed in [10,11]. Both of these topologies can be easily extended to expand the output levels by adding boost units or CHBs. A modular extension topology was proposed in [12] to decrease the voltage stresses of switches. Another modular extension topology was proposed in [13] to increase the output levels by connecting DC source with capacitors in series. The voltage stresses of the switches in modular extension inverters are lower than that those in inverters with an H-bridge, while more devices are applied. When compared with the above topologies, the cross-switched multilevel inverter proposed in [14] decreases the number of switches. In addition, asymmetrical DC sources were applied to topologies in [15,16] to improve the output levels. However, the use of multisource makes their topologies complex.

None of the above SCMLIs possess the fault-tolerant capability. Power devices, such as insulated-gate bipolar transistors (IGBTs) and metal oxide semiconductor field-effect transistors (MOSFETs), are vulnerable to failures based on field experiences. Low reliability is one of the major concerns of multilevel inverters. Therefore, fault-

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tolerant techniques have been proposed as an effective approach to enhance the reliability of inverters [17]. One hardware solution for fault-tolerant operations was achieved by adding a redundant leg to the inverter [18]. The redundant leg was configured to bypass and isolate a faulty leg once a failure occurs. This solution maintains the continuity of output levels [19]. However, it also increases the number of devices, the cost of the inverters, and the control complexity. Another control solution without extra devices was achieved by directly changing the control strategy of inverters [20]. However, the inherent defect of this solution, i.e., the degraded output levels under post-fault conditions, limits its application. The control solution of fault tolerance is suitable for the extended topology.

To integrate fault-tolerant capability into SCMLIs, a space-type SCMLI is proposed in this paper. It consists of only one DC source and can be extended by adding capacitors and switches. In addition, the inverter has voltage boost capability, the abilities to supply inductive loads, and operation under an open-circuit fault.

The remainder of this paper is organized as follows. Section 2 includes the topology configuration, operation principle, and topology extension. The modulation strategy and an analysis of capacitor ripples are given in Section 3. The operation of the topology under open-circuit faults is explained in Section 4. A comparative study with several switched-capacitors and fault-tolerant multilevel inverters is presented in Section 5. Simulation and experimental results are shown in Section 6. Finally, the conclusion is presented in Section 7.

2 Proposed Topology

2.1 Topology Configuration

A space-type SCMLI topology is proposed in this paper. As shown in Fig. 1, the basic circuit of the proposed inverter consists of one DC source, three capacitors, eight switches with anti-parallel diodes, three switches without anti-parallel diodes, and three diodes.

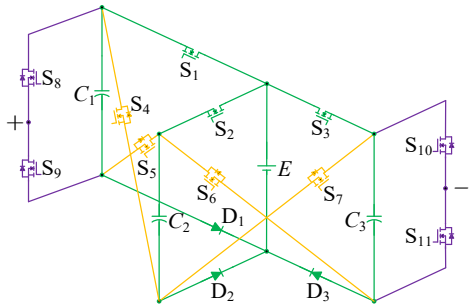


Fig. 1 Proposed space-type SCMLI

In this concept, the capacitors in parallel with the input DC voltage source (e.g., photovoltaic panel, fuel cell, or batteries) are charged with the source voltage E. The maximum output level is gained by the series connection of capacitors. The series connection of capacitors is achieved by controlling the on-off states of the switches S_4~S_7. The capacitors are charged by controlling the switches S_1~S_3 at the turn-on state. Instead of an H-bridge, two half-bridges are applied to connect loads with the inverter. Therefore, the voltage stresses of the four switches are decreased. To be specific, the switches S_8 and S_9 as well as the switches S_{10} and $S_{11}$are turned on alternately to generate negative levels.

According to the above analysis, a seven-level output ($\pm3E$, $\pm2E$, $\pm E$, 0) and a voltage gain of 3 are generated by the proposed inverter with only one DC source. In addition, decreased maximum voltage stresses of the switches, equal to $2E$, are achieved.

2.2 Operation Principles

The operation states of the power switch S_i are complementary to S_{i+1} (i=4,6,8,10), which means less control complexity for the proposed inverter. The states of the capacitors and switches are listed in Table 1. It is noted that 0 and 1 refer to the turn-off and turn-on states of the switches, respectively. The states of the capacitors are shown by "C," "D," and "–," which indicate the charging, discharging, and idle states, respectively.

Table 1 States of Components At Each Output Level

Level	3E	2E	E	0	-E	-2E	-3E
C_1	C/D	C/D	–	–	C	–	D
C_2	D	D	C	–	–	D	D
C_3	D	–	D	C	D	C/D	C/D
S_1	1	1	0	1	1	0	0
S_2	0	0	1	0	0	0	0
S_3	0	0	0	1	1	1	1
S_4	0	0	1	0	0	1	1
S_5	1	1	0	1	1	0	0
S_6	0	0	0	1	1	1	1
S_7	1	1	1	0	0	0	0
S_8	1	1	1	0	0	1	0
S_9	0	0	0	1	1	0	1
S_{10}	0	1	0	0	1	1	1
S_{11}	1	0	1	1	0	0	0

The bidirectional current paths (red lines) for an inductive load, and the charging circuits (green lines) of the proposed inverter can be obtained from Fig. 2. It is shown in Fig. 2a that the output level of the proposed topology is 3E. The switch S_1 is at the turn-on state, and the capacitor C_1 is charged to E by the DC source. The switches S_5, S_7, S_8, and S_{11} are at the turn-on state, and the capacitors C_1, C_2, and C_3 are discharged in series. It is shown in Fig. 2b that the output level of the proposed topology is 2E. The switch S_1 is at the turn-on state, and the capacitor C_1 is charged to E by the DC source. The switches S_5, S_7, S_8, and S_{10} are at the turn-on state, and the capacitors C_1 and C_2 are discharged in series. It is shown in Fig. 2c that the output level of the

proposed topology is E. The switch S_2 is at the turn-on state, and the capacitor C_2 is charged to E by the DC source. The switches S_4, S_7, S_8, and S_{11} are turned on, and the capacitor C_3 is discharged. It is shown in Fig. 2d that the output level of the proposed topology is 0. The switches S_1 and S_3 are at the turn-on state, and the capacitors C_1 and C_3 are charged to E by the DC source. The switches S_5, S_6, S_9, and S_{11} are at the turn-on state, and no capacitor is discharged. As shown in Fig. 2e, Fig. 2f, and Fig. 2g, the operation states of the proposed topology in the negative half cycle are similar to those in the positive half cycle.

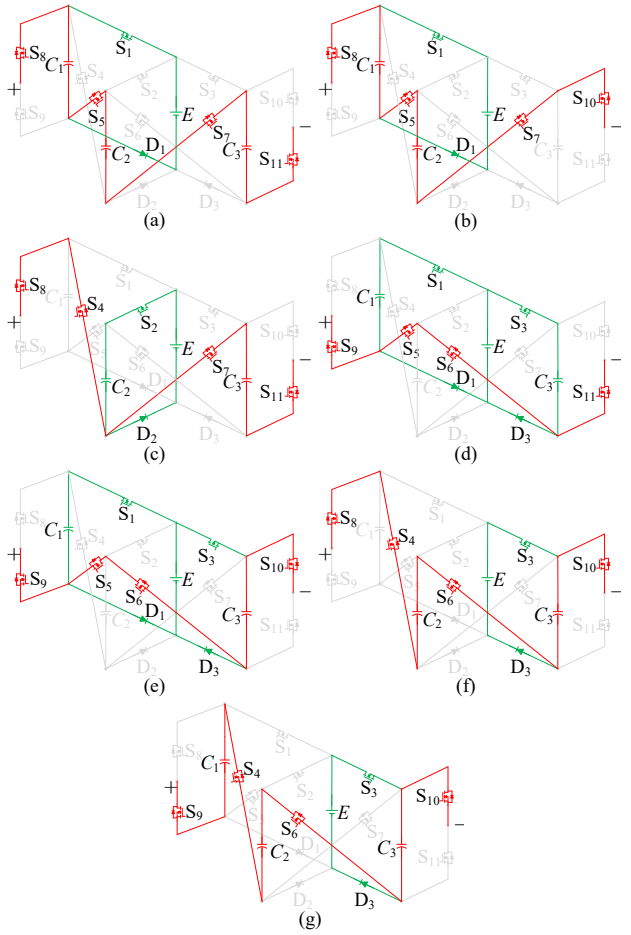


Fig. 2 Current flowing paths and components states at each level: **a** 3E; **b** 2E; **c** E; **d** 0; **e** -E; **f** -2E; **g** -3E

Obviously, the reverse current paths, which are composed of switches, anti-parallel diodes, and capacitors, are exactly in line with the forward current paths in each mode of the output levels. Consequently, it is indicated that the proposed inverter can supply inductive loads.

2.3 Topology Extension

A modular extension style that adds capacitors and switches to improve the output level is proposed in this paper. The nine-level topology shown in Fig. 3 contains one DC source, four capacitors, ten switches with anti-parallel diodes, four switches without anti-parallel diodes, and four diodes. The cascaded extension can be used in the proposed topology. Moreover, the output levels can be expanded if the diodes in the charging circuits are replaced by switches.

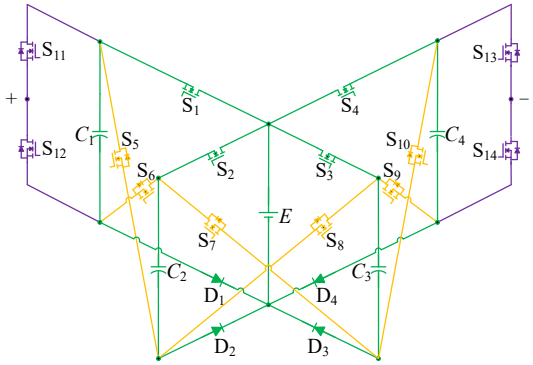


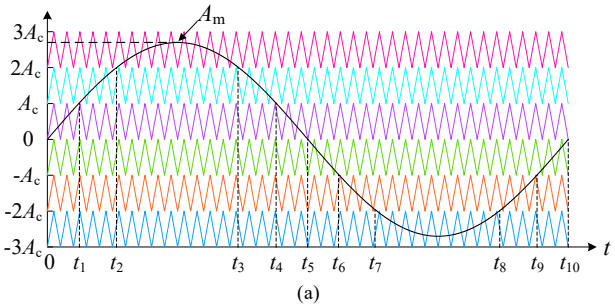
Fig. 3 Extended topology with a nine-level output

The operation principle of the nine-level space-type topology is similar to that of the seven-level topology. The capacitors C_1 and C_3 are charged by the DC source at the output levels of E and 2E, and the capacitors C_2 and C_4 are charged at the levels of 0 and -E. The proposed extendable topology has the advantage of a low voltage ripple since at least one capacitor is charged at any level. Another advantage is that the capacitors are independently charged by the DC source. Thus, faulty capacitors in the extended topology can be isolated by changing the control strategy.

3 Modulation Strategy and Capacitor Analysis

3.1 Modulation Strategy

The carrier disposition pulse width modulation technique is adopted in the proposed topology. It is widely used as a control strategy for SCMLIs due to its easy implementation and its performance in terms of harmonic cancellation. As shown in Fig. 4, six triangular carrier signals are provided with the same amplitude (A_c), frequency (f_c), and phase but with different offsets. A sinusoidal modulation signal is provided with the amplitude of A_m and the frequency of f_o, which means the output frequency. The six triangular carrier signals are compared with a sinusoidal modulation signal to generate pulses u_1~u_6. Control signals for the switches are obtained by logical combinations of these pulses. Then the switches are driven, and the inverter outputs the target waveform.



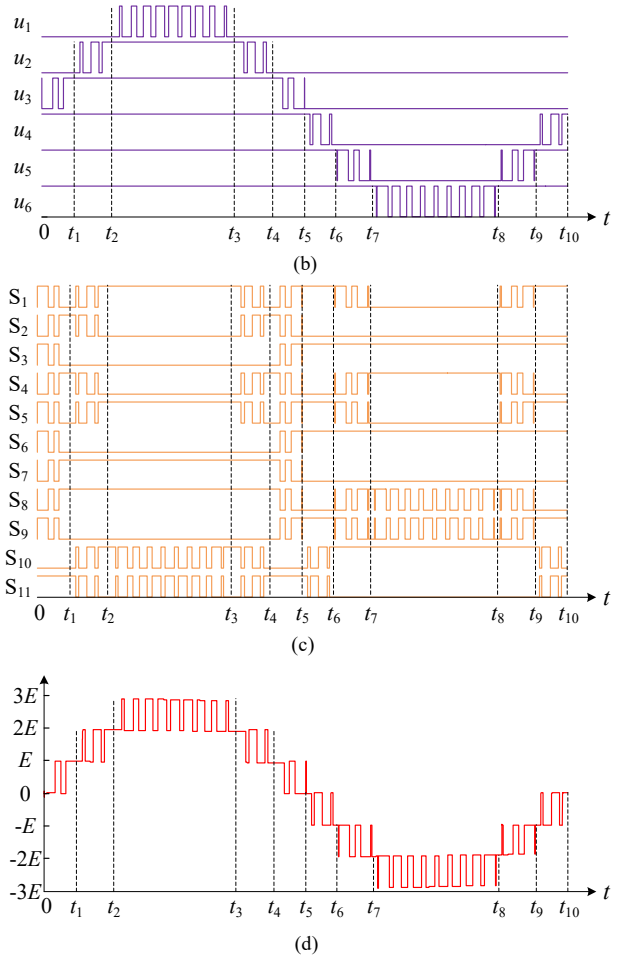


Fig. 4 Carrier-disposition pulse width modulation strategy: **a** carrier and modulation waves; **b** pulses from comparison results of carrier signals and modulation signal; **c** gate signals of switches; **d** target output waveform

The number of triangular carrier signals is determined based on the number of output levels except for 0. The states of the switches are determined beforehand based on the operating status of the proposed inverter shown in Table 1, where redundancy switching combinations have been taken into consideration. The on-off states of the switches in one cycle are analyzed and compared with the pulses shown in Fig. 4b. As a result, the gate signal logics of the switches can be calculated as follows:

$$S_1 = u_2 + \overline{u}_3 u_5, \tag{1}$$

$$S_2 = \overline{u}_2 u_3, \tag{2}$$

$$S_3 = S_6 = \overline{S}_7 = \overline{u}_3, \tag{3}$$

$$S_4 = \overline{S}_5 = \overline{u}_2 u_3 + \overline{u}_5, \tag{4}$$

$$S_8 = \overline{S}_9 = u_3 + \overline{u}_5 u_6, \tag{5}$$

$$S_{10} = \overline{S}_{11} = \overline{u}_1 u_2 + \overline{u}_4. \tag{6}$$

3.2 Analysis of Self-Balance Performance and Capacitor Ripple

The three capacitors C_1, C_2, and C_3 are employed in the proposed inverter, and the voltage self-balance of each capacitor is achieved by being charged independently. To avoid a short circuit, the capacitor C_1 can only be charged when the switch S_4 is turned off. Likewise, the capacitor C_3 can only be charged when the switch S_7 is turned off, and the capacitor C_2 can only be charged when the switches S_5 and S_6 are turned off.

As shown in Fig. 2d and Fig. 2e, the capacitors C_1 and C_3 are charged to E during the output levels of 0 and -E. Only one capacitor is charged in the other output levels. The above alternate charging strategy ensures that the voltages of the three capacitors are held at E, which achieves the self-balance capability of the capacitor voltages.

Capacitor calculation is one way for SCMLIs to prevent high-voltage ripple across the capacitors and to ensure the output power quality. The discharging quantity of the capacitors during times t_a~t_b is obtained as:

$$\Delta Q_C = \int_{t_a}^{t_b} I_o \sin\left(2\pi f_o t\right) \mathrm{d}t \tag{7}$$

and the output current is presented as:

$$i_o = I_o \sin(2\pi f_o t) \tag{8}$$

where I_o means the amplitude of the output current. Considering k as the ripple factor for describing the maximum acceptable voltage ripple and V_C as the rated voltage of the capacitors, the capacitance can be described as follows:

$$C \geq \frac{\Delta Q_C}{k V_C}. \tag{9}$$

For the modulation strategy of the seven-level inverter shown in Fig. 4, t_1~t_5 are calculated as follows:

$$t_1 = \frac{\arcsin\left(\dfrac{1}{3M}\right)}{2\pi f_o}, \tag{10}$$

$$t_2 = \frac{\arcsin\left(\dfrac{2}{3M}\right)}{2\pi f_o}, \tag{11}$$

$$t_3 = \frac{\pi - \arcsin\left(\dfrac{2}{3M}\right)}{2\pi f_o}, \tag{12}$$

$$t_4 = \frac{\pi - \arcsin\left(\dfrac{1}{3M}\right)}{2\pi f_o}, \tag{13}$$

$$t_5 = \frac{1}{2 f_o} \tag{14}$$

where M is the modulation index, which is defined by:

$$M = \frac{A_m}{3A_c}. \tag{15}$$

It can be concluded from the capacitor states shown in

Table 1 and Fig. 4 that the longest continuous discharging interval of the capacitor C_2, t_1~t_4, is greater than that of C_1 and C_3. For the sake of simplicity, the capacitances of C_1 and C_3 are designed to equal to C_2. In addition, the voltage ripple of C_2 is given by:

$$\Delta V_{C2} = \frac{\int_{t_1}^{t_4} I_o \sin(2\pi f_o t)\,\mathrm{d}t}{C_2}. \tag{16}$$

4 Open-Circuit Fault Tolerance

The operation principle of the open-circuit fault tolerance of the proposed inverter is analyzed in this section. In this section, fault detection is not considered since the focus is on developing a fault-tolerant topology. Two kinds of faults are considered; one occurs in the switches S_1~S_3 or the diodes D_1 ~ D_3 (Type-A fault), and the other occurs in the switches S_4~S_{11} (Type-B fault).

The capability of open-circuit fault tolerance is implemented by transformations of the control strategy and topology that separate the charging paths of capacitors from their discharging paths. The severity of the faults that occur in the proposed space-type SCMLI depends on the location of the faults. Its effect on the output level is summarized in Table 2.

Table 2 Switching States For Open-Circuit Fault Tolerance

Faulty switch	Switches in the same state	Switch keeping on-state	Output level
S_1 or D_1	S_4 and S_8; S_5 and S_9	None	5
S_2 or D_2	S_4 and S_7; S_5 and S_6	None	3
S_3 or D_3	S_6 and S_{11}; S_7 and S_{10}	None	5
S_4	None	S_5	3
S_5	None	S_4	3
S_6	None	S_7	3
S_7	None	S_6	3
S_8	None	S_9	5
S_9	None	S_8	5
S_{10}	None	S_{11}	5

4.1 Type-A Fault

As shown in Fig. 1, the corresponding capacitor cannot be charged if an open-fault fault occurs in the switches S_1, S_2, or S_3, or in the diodes D_1, D_2, or D_3. Once an open-circuit fault occurring in the switch S_1 or the diode D_1 is detected, the capacitor C_1 is isolated from its discharging paths by changing the control strategy. The switches S_4 and S_8 are turned on or off simultaneously, as well as the switches S_5 and S_9. As a result, the proposed inverter operates as a five-level inverter with switches S_8 and S_9 turned on alternately. The current flowing paths at each level are shown in Fig. 5.

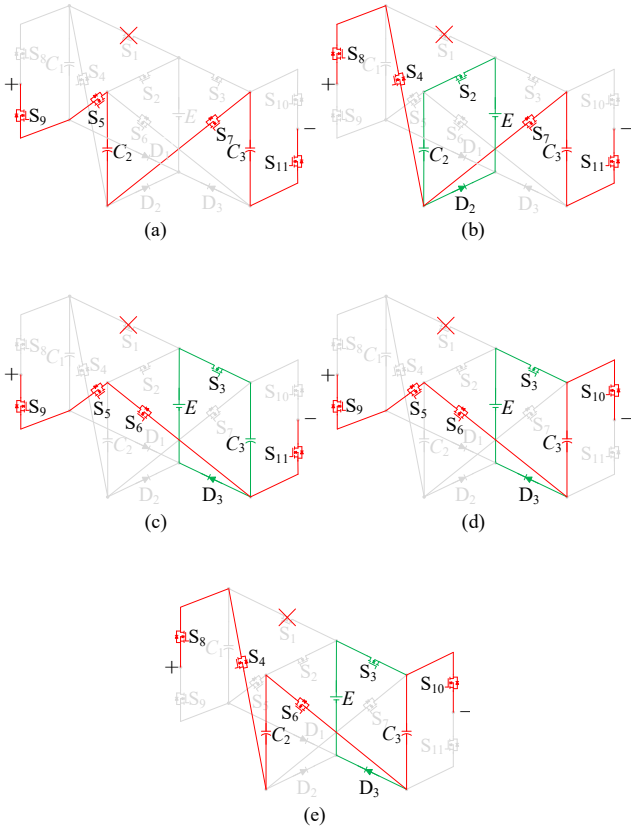


Fig. 5 Current flowing paths of an inverter with an open-circuit fault in S_1: **a** $2E$; **b** E; **c** 0; **d** $-E$; **e** $-2E$

Similarly, the proposed inverter operates as a five-level inverter if a fault occurs in S_3 or D_3. As for a fault occurring in S_2 or D_2, the switches S_4 and S_7 are turned on or off simultaneously, as well as the switches S_5 and S_6. The capacitors C_1 and C_3 cannot be discharged in series. As a result, the proposed inverter operates as a three-level inverter.

4.2 Type-B Fault

The switches S_4 and S_5 operate in complementary states, as do the switches S_6 and S_7, S_8 and S_9, as well as S_{10} and S_{11}. The other one maintains the on-state once an open-circuit fault occurs in one of the two switches. The proposed inverter operates as a three-level inverter if a fault occurs in S_4, S_5, S_6, or S_7. Similarly, it operates as a five-level inverter if a fault occurs in S_8, S_9, S_{10}, or S_{11}. For example, the switch S_9 maintains the on-state once an open-circuit fault occurring in S_8 is detected. Three capacitors are charged as normal, and at most, two capacitors are discharged in series during the maximum output level. As a result, the proposed inverter operates as a five-level inverter. The states of the capacitors and switches in one cycle and the current flowing paths at each level are shown in Fig. 6.

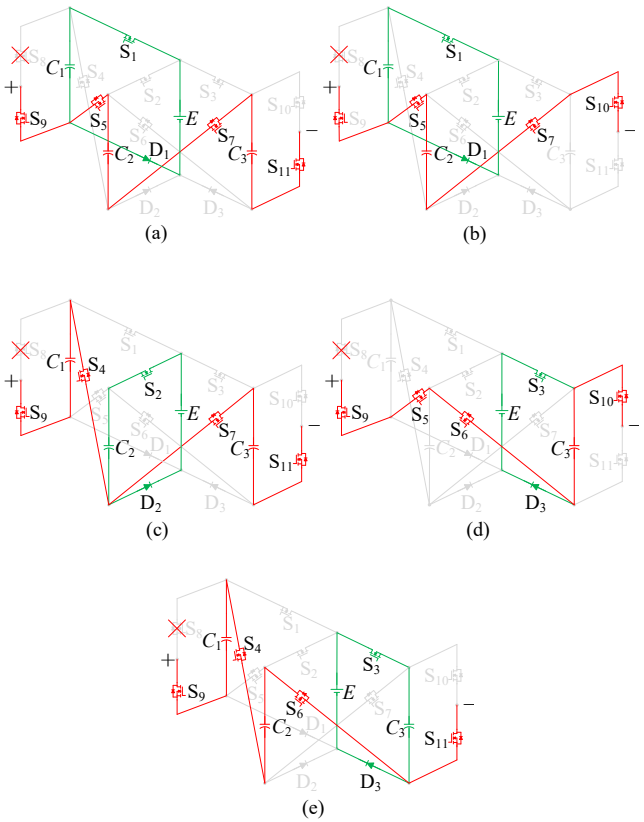


Fig. 6 Current flowing paths of an inverter with an open-circuit fault in S_8: **a** $2E$; **b** E; **c** 0; **d** $-E$; **e** $-2E$

The voltage stresses of the switches and the voltage ripple of the capacitors are decreased or remain under post-fault operations. The capabilities of the capacitors voltage self-balance and ability to supply inductive loads are kept in the proposed fault-tolerant topology. This topology can be applied for short-circuit fault tolerance if fast fuses or circuit breakers are used to isolate the short-circuit switches [21]. It is important to point out that this fault-tolerant technique, which decreases four levels at most, can be outfit for extendable topologies.

5 Comparative Study

An analysis has been carried out to compare the performances of different topologies. In order to compare topologies outputting different levels, the output level of the proposed extendable topology is given as $2m+1$, where m indicates the number of capacitors. The compared parameters include the number of output levels (N_L), the number of DC sources (N_{DC}), the number of capacitors (N_C), the number of switches (N_S), the extra charging circuit, the type of fault tolerance, and the modular extension.

The typical topology with an H-bridge in [22] employs staircase switched-capacitor cells to achieve voltage boost capability. The capacitors are charged in parallel with the DC source and discharged in series. The number of capacitors determines the maximum output voltage level. However, the voltage stresses of the switches in the H-bridge are equal to the maximum output voltage. The topology in [11] eradicates the current spikes in the capacitor charging process through the auxiliary charging circuit. However, it utilizes many devices and needs an extra charging circuit. A single-phase seven-level inverter topology with a reduced number of power components and mitigated voltage stresses was proposed in [23]. This inverter has a three-time step-up ratio and self-balance capability of the capacitor voltages. However, the above topologies cannot achieve fault-tolerant capability.

In [24], a fault-tolerant nine-level inverter with a redundant leg was proposed to maintain full-voltage levels under a switch fault case. In this topology, the faults that occur in the main inverter are bypassed by the activation of redundant leg switches. However, it needs a lot of devices due to the two flying capacitors charged by extra circuits. The hybrid CHB topology proposed in [25] consists of two CHB cells and a cross-coupled CHB (X-CHB). Under normal operation, the X-CHB works as a three-level inverter with its capacitor idle. Meanwhile, it operates as a five-level boost inverter to compensate for the missing voltage level if a fault occurs in the CHB cells. However, a fault occurs in switches of the X-CHB is not taken into consideration. The topology in [26] can be synthesized with several H-bridge cells. Two relays are employed in this topology to change the full-bridge cells to half-bridge cells, which removes the failed sections. To realize fault tolerance, this topology requires relays and an extra reserved load-side CHB.

A fault-tolerant topology based on a full-bridge NPC inverter was proposed in [27]. It utilizes an additional redundant leg composed of six IGBT devices to compensate for faults in the main inverter. However, there is a large number of switches in this five-level inverter. A fault-tolerant single-phase five-level inverter for photovoltaic applications was presented in [28]. It comprises a half-bridge two-level inverter, a three-level diode clamp inverter, and a bidirectional switch. The topology operates as a three-level inverter through a redundant switching combination. However, its application is limited due to its low output levels under post-fault conditions and no extended topology. A multi-level inverter was proposed in [29]. It consists of one leg of an NPC, one leg of an H-bridge, and one additional bidirectional switch. The topology keeps the full-voltage levels without increasing the capacitor voltage ripple under faulty conditions. However, it replaces the faulty switch with a redundant leg composed of four switches, which results in higher power loss under post-fault conditions.

It is seen from Table 3 that the number of devices of topologies with a redundant leg is higher than that of topologies achieving fault tolerance by changing the control

strategy when outputting the same levels. The proposed topology achieves open-circuit fault tolerance with the least sources when outputting the same levels. The number of switches in the proposed topology is only higher than the topologies in [22, 23, 28]. The parameters of the topology in [29] are similar to those of the proposed topology. However, it requires an extra charging circuit for its flying capacitor. In addition, the output levels of the topologies in [24, 27-29] are low and cannot be extended. The topologies in [25, 26] can be extended by an H-bridge. However, there are more devices employed in their extended topologies than there are in the proposed extendable topology.

Table 3 Comparison With Several Topologies

Topology	N_L	N_{DC}	N_C	N_S	Extra charging circuit	Fault tolerance	Modular extension
[22]	7	1	3	10	No	No	Yes
[11]	7	1	3	12	Yes	No	Yes
[23]	7	1	2	9	No	No	No
[24]	9	2	2	16	Yes	Redundant leg	No
[25]	7	3	1	16	No	Redundant leg	Yes
[26]	7	3	0	16	No	Control strategy	Yes
[27]	5	2	0	14	No	Redundant leg	No
[28]	5	2	0	7	No	Control strategy	No
[29]	5	1	1	8	Yes	Redundant leg	No
Proposed	$2m$+1	1	m	$3m$+2	No	Control strategy	Yes

6 Simulation and Experimental Results

6.1 Simulation Results

A closed-loop simulation model of the proposed inverter and its controller was built based on MATLAB/Simulink, as shown in Fig. 7. The output power of the proposed inverter was changed by making the grid-connected current i_g track its reference value i^*. Specifically, the phase of the reference current i^* is kept consistent with the grid voltage v_g through the phase-locked loop (PLL), while its amplitude tracks the given current amplitude I_m. The error signal, the comparison result of the reference value i^* and the grid-connected current i_g, is sent to the quasi proportional resonant (QPR) controller. The transfer function of the controller is:

$$G_i(s) = K_p + \frac{2K_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{17}$$

where K_p is the proportional coefficient, K_r is the integral coefficient, ω_c is the resonance bandwidth, and ω_0 is the center frequency [30]. In this simulation, the filter inductance is 5mH, K_p and K_r are set to 50 and 5000, and ω_c and ω_0 are set to 0.2π and 100π, respectively.

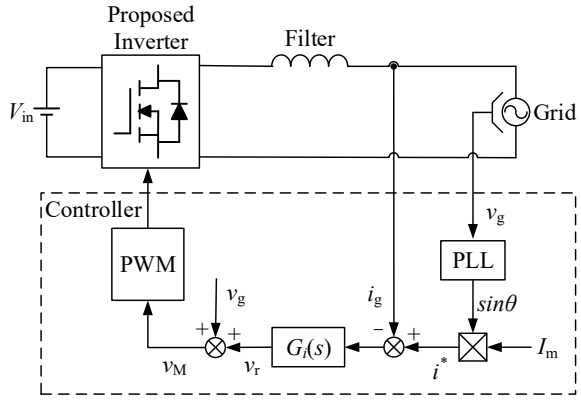
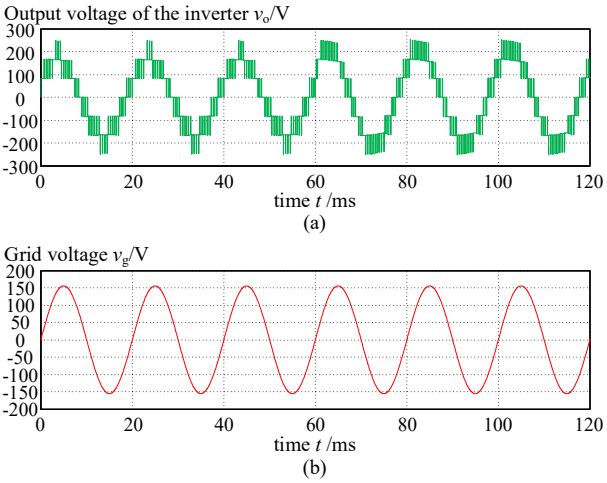


Fig. 7 Structure of a closed-loop controller

The root means square (rms) of the grid voltage is 110V (50Hz) and the amplitude of the input voltage in the proposed inverter is 85V. As shown in Fig. 8, the grid-connected current varies from 10A (rms) to 20A (rms). Meanwhile, the output voltage of the inverter is kept steady. It can be seen that the grid-connected current rises rapidly to its target value without impulse current. These simulation results show that the proposed inverter has satisfactory steady-state and dynamic performances.



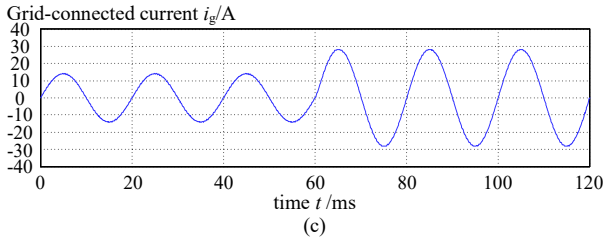


Fig. 8 Closed-loop simulation results of the proposed inverter: **a** output voltage of the inverter; **b** grid voltage; **c** grid-connected current

As shown in Fig. 9, the output voltage of the inverter varies from a seven-level to a five-level wave when an open-circuit fault occurs in S_1. At the same time, the grid voltage and grid-connected current of the inverter are kept steady. These simulation results verify the fault-tolerant capability of the proposed inverter.

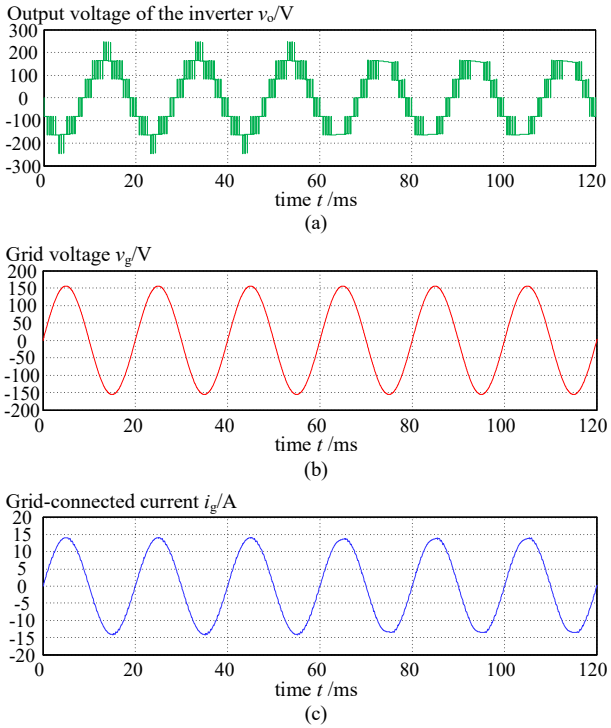


Fig. 9 Simulation results of the proposed inverter with a faulty S_1: **a** output voltage of the inverter; **b** grid voltage; **c** grid-connected current

6.2 Steady-State and Dynamic Experiments

A seven-level prototype was constructed and tested to validate the feasibility of the proposed topology. The selection of experimental parameters considers the existing equipment in the laboratory. A photograph of the experimental prototype is shown in Fig. 10, and the detailed parameters are given in Table 4.

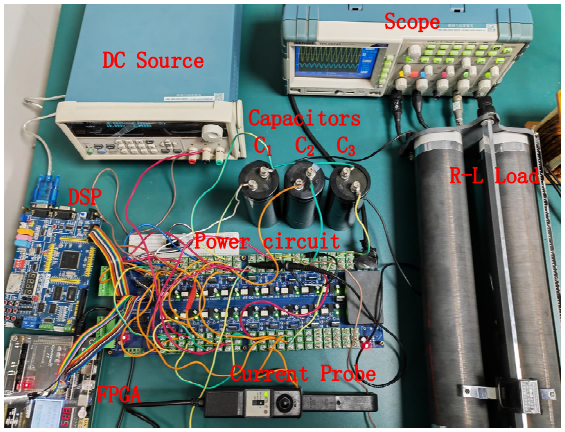


Fig. 10 Experimental prototype of the proposed inverter

It is considered that the output waveform of the prototype is under the resistance-inductance (R-L) load condition. Experimental results of the output voltage and current, as well as the capacitor voltages, are depicted in Fig. 11.

Table 4 Experimental Parameters

Parameters	Values
Input DC source (V_{DC})	30 V
Output frequency (f_o)	50 Hz
Switching frequency	2 kHz
Modulation ratio (M)	0.9
Capacitors (C_1, C_2 and C_3)	2200 μF
Loads	100 Ω & 15 mH
Switches (MOSFET)	SPP20N60C3
Optocoupler-driver	TLP250
Current probe	Tektronix A622

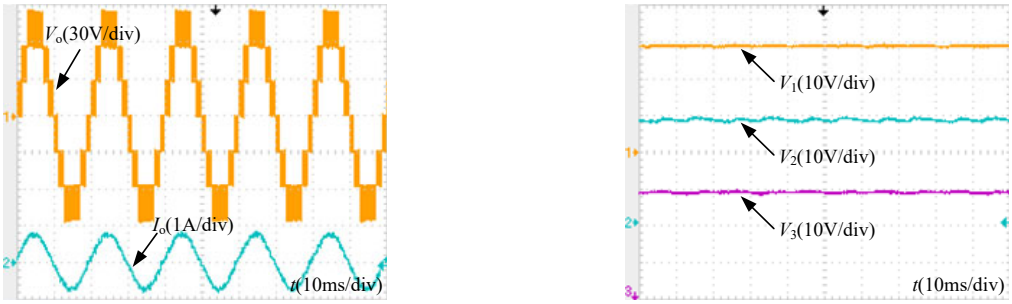
It is obvious that a boost gain of 3 is achieved, and that the current lags behind the voltage in phase. The voltages of three capacitors are balanced with a small ripple. It is shown that the proposed inverter has the capabilities of supplying inductive loads and the self-balance capability of capacitor voltages. This is in agreement with the previous analysis.

The following experiments are conducted to test the performance of the prototype under dynamic conditions. The dynamic responses of the prototype under load variations are depicted in Fig. 12a. Fast responses of the load current are achieved when the load varies from R-L load to no-load conditions. Irrespective of load variation, no deterioration is observed in the output voltage. The dynamic responses of the prototype under input voltage variation are shown in Fig. 12b, which emulates the reality of solar cells. It is indicated from the experimental results that the output voltage and load current of the prototype quickly reach the steady state. The dynamic performances of the proposed inverter have been presented from the fast variation process in the above experiments.

6.3 Fault-Tolerant Experiment

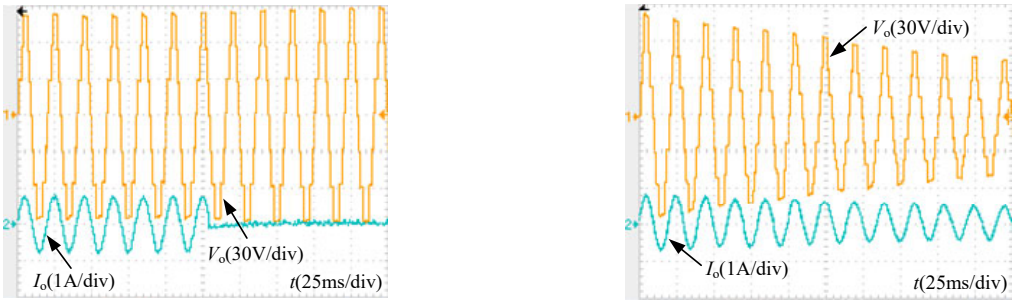
An experiment on open-circuit fault tolerance is conducted to validate the reliability of the proposed inverter.

In this experiment, an open-circuit fault occurs in the switch S_1. With a change of the pre-fault condition to the post-fault condition, the capacitor C_1 is in the idle state. The switches S_4 and S_8 are turned on or off at the same time, as are the switches S_5 and S_9. It can be seen from Fig. 13 that the prototype is quickly stabilized in the five-level working state. Therefore, the open-fault tolerant capability of the proposed inverter is verified.



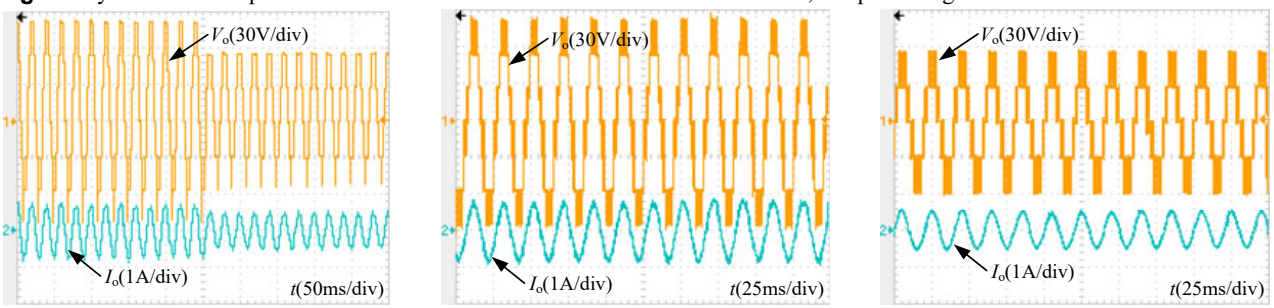
(a) (b)

Fig. 11 Experimental results in the steady state: **a** output voltage and current with an R-L load; **b** voltages of the capacitors



(a) (b)

Fig. 12 Dynamic-state experimental results: **a** load variation from 100Ω-15mH to 0; **b** input voltage variation from 30V to 15V



(a) (b) (c)

Fig. 13 Fault-tolerant experimental results: **a** transition of the prototype from pre-fault to post-fault conditions; **b** enlarged view of the normal condition; **c** enlarged view of the post-fault condition

7 Conclusions

An extendable space-type SCMLI with fault-tolerance capability was proposed in this paper. The topology configuration, analysis of the capacitors, and open-circuit fault tolerance mechanisms were presented, as well as a comparative study. Finally, a prototype was constructed, and the obtained experimental results validate the feasibility and performance of the proposed inverter. The following conclusions are drawn.

1) The proposed inverter can achieve voltage boost gain and supply inductive loads. Moreover, it can be extended to increase the output levels and voltage boost gain.
2) Fault tolerance operation is achieved, which improves the reliability of the inverter. The capacitor voltages of the proposed inverter are balanced under both pre-fault and post-fault operations. In addition, the voltage stresses of the switches and the voltage ripple of capacitors are decreased or remain under post-fault operations.
3) The performances of the proposed inverter have been validated by a seven-level experimental prototype. Experimental results show that the proposed inverter has fault-tolerant capability and a fast response under dynamic conditions.

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