An Auxiliary Circuit Enhancing DC Fault Clearing Capability of Hybrid MMCs with Low Proportion of FB-SMs

Xiongfeng Fang, Gen Li, *Member, IEEE*, Canfeng Chen, Jian Xiong, Kai Zhang

***Abstract*—The hybrid modular multilevel converter (HMMC) composed of half-bridge (HB) and full-bridge (FB) submodules (SMs) is an alternative to the FB-MMC with lower loss and cost. However, the HMMC's maximum reverse-biased voltage (RBV) is lower than the FB-MMC, so does the dc fault clearing capability (DCFCC). Reduced RBV will prolong the fault clearing time, especially when the dc side inductance is large. In this letter, an auxiliary circuit is proposed for HMMCs, which can change the fault current paths and enable both HB- and FB-SMs to participate in the fault clearing. Thus, the maximum RBV of the HMMC is increased to be equal to an FB-MMC. Moreover, the proportion of FB-SMs can be reduced. With the auxiliary circuit, the DCFCC of the HMMC is enhanced with the reduction of the power losses and semiconductor costs. Simulations and scaled-down experiments validate the proposed method.**

***Index Terms*—High-voltage dc (HVDC), hybrid modular multilevel converter (HMMC), dc fault clearing capability, submodules (SMs).**

I. Introduction

Dc fault clearing is an important challenge for modular multilevel converter (MMC) based high-voltage direct current (HVDC) transmission systems [1], [2]. The full-bridge submodule (FB-SM) based MMC features its dc fault clearing capability (DCFCC) and boosted maximum modulation index [3], [4]. However, FB-SMs have higher losses and costs than half-bridge (HB) SMs. Thus, the hybrid MMC (HMMC) consisting of HB- and FB-SMs can be an option for practical applications due to reduced capital cost and power loss [5], [6]. The HMMC has been applied in China's three-terminal ±800 kV Kun-Liu-Long project [7].

Either blocking all SMs in the HMMC or regulating the dc voltage to a negative value can clear the dc fault current [8]. However, the SM blocking method requires a lower proportion of FB-SMs than the dc voltage regulating method, which can be a more economical solution with a proper design. In the traditional HMMC, only FB-SMs can provide reverse-biased voltages (RBVs) in the fault current path to clear the fault current. However, a small RBV prolongs the fault clearing time, especially if the dc side inductance is large. Solutions enhancing HMMC's DCFCC with a low proportion of FB-SMs are still under-researched in HMMC-based HVDC systems.

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Several new dc fault clearing approaches have been proposed to improve the techno-economic performance of the HVDC system. In [9], the ac grid is bypassed (short-circuited) by crossing thyristor branches within the HMMC to accelerate the speed of dc fault clearing. In this case, the proportion of the unipolar FB-SMs can be reduced. However, a three-phase ac short-circuit is created within the converter. The short-circuit will exist until the thyristors are turned off by line commutation voltages, which is undesirable for the ac grid. In [10], the proposed hybrid dc breaker can bypass the large dc inductor and transmission line to simplify the converter side dc fault clearing. However, the decreasing of the dc line fault current is slowed down. At the same time, large ac inductors should be used at the converter valve-side to limit arm currents during the fault clearing period. In [11], the proportion of FB-SMs is reduced at the expense of increased FB-SM capacitor voltage and dc fault clearing time, which may threaten the security of the converter. In [12], thyristors and metal oxide varistors (MOVs) are employed to adjust the converter terminal dc current decreasing rate. Thus, the FB-SMs overvoltage can be mitigated, and the costs of SM capacitors can be reduced. However, this method cannot accelerate the dc line fault current clearing. In [13], a dc fault is cleared by changing the current direction in one arm with an additional H-bridge circuit. Although these methods can clear the dc fault current, their dc fault clearing capability is much weaker than the FB-MMC.

An auxiliary circuit using semiconductor devices is proposed in this letter for enhancing the DCFCC of HMMC-based HVDC systems. Contributions of this work include: 1. This letter proposes a novel circuit and control strategy of FB-SMs to change the direction of the converter terminal dc fault current and enable both HB-SMs and FB-SMs to participate in the fault clearing process. 2. The proposed method significantly strengthens the dc fault clearing capability of the HMMC with low loss and cost, which has never been proposed in the open literature. With the proposed method, the maximum RBV of the HMMC is the same as the FB-MMC. Moreover, the dc fault clearing speed is no longer determined by the proportion of FB-SMs. Therefore, the number of FB-SMs can be reduced, bringing down the overall cost and power loss. Simulations and experiments validate the proposed method.

II. The Proposed Auxiliary Circuit

A. DCFCC and FB-SM Proportion of Traditional HMMCs

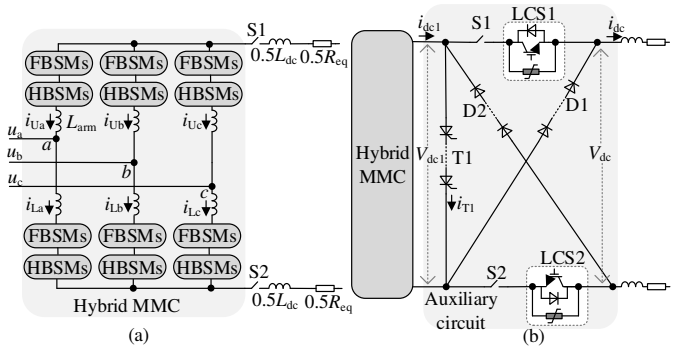

Fig. 1. Topologies of the HMMC and the proposed auxiliary circuit. (a) The traditional HMMC, (b) the HMMC with the auxiliary circuit.

As a pole-to-pole fault in a symmetric monopolar MMC-HVDC system is more severe than a pole-to-ground fault, this letter proposes the dc fault clearing method for the pole-to-pole fault. Moreover, the proposed method can be readily used in a symmetric bipolar HVDC system as a pole-to-ground fault in a symmetric bipolar system is equivalent to a pole-to-pole fault in a symmetric monopolar system. The topology of the HMMC is shown in Fig. 1(a). Only blocked FB-SMs can provide the RBV in the fault current paths during the dc fault clearing process. Thus, the maximum RVB V_R in each arm is decided by the proportion η of FB-SMs, as shown in (1). S1 and S2 are mechanical switches employed to isolate the faulted line after clearing the dc fault current.

$$V_R = V_{FB} = \eta V_{dc} \tag{1}$$

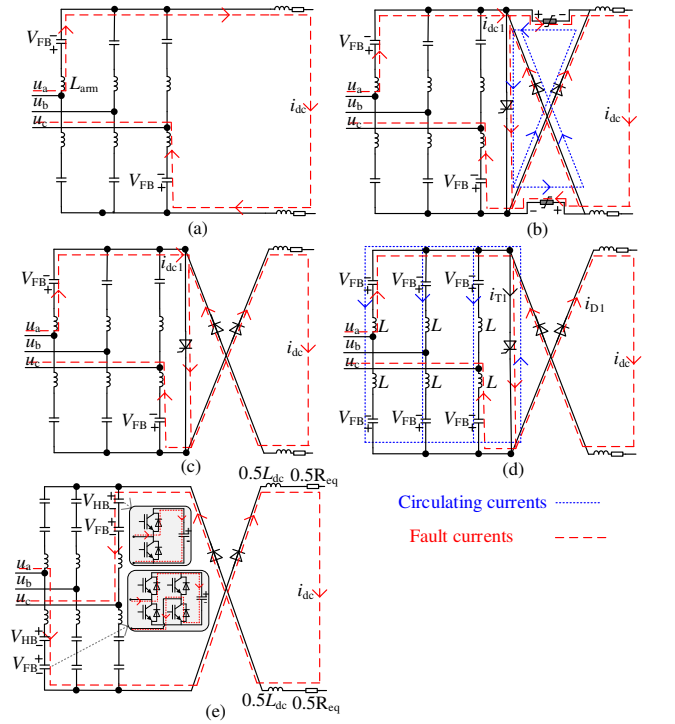

Fig. 2. Equivalent circuits of the HMMC with the auxiliary circuit (when $u_a > u_b > u_c$). (a) After converter blocking, (b) opening process of LCSs, (c) opening process of S1 and S2 after LCSs are fully opened, (d) FB-SMs inserted negatively to turn-off T1, (e) SMs blocked after T1 turns off.

The dc fault current will only flow through two arms after a short period of current commutation among arms [12], as shown in Fig. 2(a). To simplify the analysis, the fast current commutation process among arms is ignored in this letter. The decreasing rate of the dc fault current i_{dc} and the dc voltage V_{dc} can be obtained by

$$-\frac{di_{dc}}{dt} = \frac{2V_R - u_{\max} + i_{dc}\times R_{eq}}{L_{dc} + 2L_{arm}} = \frac{2V_{FB} - u_{\max} + i_{dc}\times R_{eq}}{L_{dc} + 2L_{arm}} \tag{2}$$

and

$$-V_{dc} = \frac{(2V_{FB} - u_{\max} + i_{dc}\times R_{eq})\times L_{dc}}{L_{dc} + 2L_{arm}} - i_{dc}\times R_{eq}, \tag{3}$$

where $u_{\max}$ is the maximum ac line voltage (maximum value among u_{ab}, u_{ba}, u_{ac}, u_{ca}, u_{bc}, u_{cb}), V_{FB} is the total voltage of all FB-SMs in one arm, R_{eq} is the equivalent resistance on the dc side, L_{dc} is the dc-side equivalent inductance, and L_{arm} is the arm inductance. The relationship of the root mean square value of ac line voltage U_{line} and the rated dc voltage V_{dc} is

$$\frac{\sqrt{2}U_{line}}{\sqrt{3}} = \frac{MV_{dc}}{2}, \tag{4}$$

where M is the modulation index. M is usually less than 1. If the current commutation process can be ignored due to its short period, the mean value of $u_{\max}$ can be estimated as

$$\bar{u}_{\max} = \frac{3\sqrt{2}U_{line}}{\pi} = \frac{3\sqrt{3}MV_{dc}}{2\pi} \approx 0.83MV_{dc}. \tag{5}$$

According to (2), when $2V_{FB}$ is larger than the amplitude of $u_{\max}$, i_{dc} will decrease immediately after blocking the converter, which requires η to be larger than 43.3%. A higher V_{FB} can lead to faster dc fault current decreasing, which requires a larger η. However, more FB-SMs will also lead to extra costs and power losses. Thus, the proportion of FB-SMs is usually chosen as 50% to make a trade-off between the DCFCC and cost & loss [5]. In an HMMC with 50% FB-SMs, $2V_R$ will be equal to the rated dc voltage V_{dc}, while an FB-MMC can create an RBV of $2V_{dc}$. Therefore, the dc fault current decreasing will be slower, which means the DCFCC of the HMMC is inferior to an FB-MMC.

B. Topology of the Proposed Auxiliary Circuit

The proposed auxiliary circuit is shown in Fig. 1(b). T1 is a branch of series-connected thyristors. D1 and D2 are two branches of series-connected diodes. S1 and S2 are two fast mechanical switches. LCS1 and LCS2 are load commutation switches used in hybrid dc breakers (DCCBs). MOVs are employed in LCSs to protect IGBTs from overvoltage. Only S1, S2, LCS1, and LCS2 are conducted during normal operation, which will result in very small power losses.

C. Dc Fault Clearing Sequence with the Auxiliary Circuit

The fault clearing sequence of HMMCs with the proposed auxiliary circuit is shown in Fig. 3.

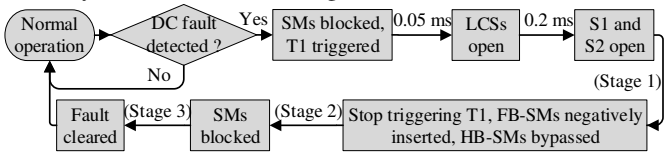

Fig. 3. Dc fault clearing sequence using the auxiliary circuit.

Stage 1: All SMs will be blocked, and T1 will be triggered if a dc fault is detected. T1 should conduct reliably in 0.05 ms, after which LCS1 and LCS2 can be opened to transfer their

currents to D1, D2, and T1, as shown in Fig. 2(b). The decreasing speed of the current of LCS1 i_{LCS1} is influenced by the voltage of LCS1 V_{LCS1}, the conducting voltage of D1 V_{D1} and T1 V_{T1}, and the stray inductance of the circuit L_{stray1}, as shown in (6). The current commutation process will complete in 0.2 ms by choosing proper voltages of the LCSs. S1 and S2 can be opened after their currents decrease to zero, as illustrated in Fig. 2(c). During this stage, the converter terminal fault current i_{dc1} is limited by the RBV provided by FB-SMs, described by (7). The line side dc fault current i_{dc} is almost unchanged. A longer opening time of S1 and S2 will only influence the duration of Stage 1, while it will not lead to overcurrent.

$$-\frac{di_{LCS1}}{dt}=\frac{V_{LCS1}-V_{D1}-V_{T1}}{L_{stray1}} \tag{6}$$

$$-\frac{di_{dc1}}{dt}=\frac{2V_{FB}-u_{\max}}{2L_{arm}} \tag{7}$$

Stage 2: Once S1 and S2 are fully opened, T1 will not be triggered anymore (firing angle removed), all HB-SMs will be bypassed, and all FB-SMs will be inserted with negative capacitor voltage. FB-SMs will discharge through T1, as illustrated in Fig. 2(d). The current of T1 i_{T1} will decrease quickly, described by (8). T1 will turn off once i_{T1} decreases to zero. The duration t_2 of Stage 2 can be estimated by (9), where i_{dcf} is the dc fault current.

$$-\frac{di_{T1}}{dt}=\frac{3V_{FB}}{L_{arm}} \tag{8}$$

$$t_2<\frac{2i_{dcf}L_{arm}}{3V_{FB}} \tag{9}$$

Stage 3: After turning off T1, all SMs are blocked again. Since the arm currents have been reversed, both HB- and FB-SMs can provide RBVs in the fault current path to clear the fault current. After a short period of current commutation among arms, the dc fault current will only pass through two arms, as shown in Fig. 2(e). The dc fault current decreasing rate is

$$-\frac{di_{dc}}{dt}=\frac{2V_R-u_{\max}+i_{dc}\times R_{eq}}{L_{dc}+2L_{arm}}=\frac{2V_{FB}+2V_{HB}-u_{\max}+i_{dc}\times R_{eq}}{L_{dc}+2L_{arm}}, \tag{10}$$

where R_{eq} is the equivalent resistance on the dc side, including the resistance of the auxiliary circuit, the transmission lines, and the fault resistor.

In the above current changing processes (except for the opening process of LCSs), the effect of the stray inductance of the proposed circuit can be ignored since the arm inductors and dc inductors are much larger than the stray inductance and therefore, will withstand most of the voltage. To simplify the analysis, the stray inductance of the proposed circuit is not included in the analysis.

D. Design of the Auxiliary Circuit

The maximum current stress of D1, D2, LCS1, LCS2 are equal to the dc fault current. The maximum current stress of T1 is equal to twice the dc fault current in Stage 1. Since thyristors have high surge current capability, the current stress is acceptable. The maximum voltage stress of D1 and D2 is equal to the rated dc voltage during normal operation. The maximum voltage stress of T1 is less than twice the rated dc voltage in Stage 3. LCSs will withstand the conducting voltage of T1, D1, D2, and the inductive voltage of the stray inductance of T1, D1, D2. Usually, one IGBT is enough to sustain the voltage stress.

The V_R of the HMMC is equal to the rated dc voltage at Stage 3. The dc fault current decreasing rate has been described in (10). By comparing (2) and (10), it can be seen that the dc fault current decreasing is accelerated thanks to the participation of HB-SMs' voltage. The fault clearing speed is not relying on the proportion of FB-SMs. FB-SMs have two functions in the proposed method. One is to limit the increase of i_{dc1} in Stage 1 to ensure arm currents are within the acceptable range, as shown in (7). The second is to turn off T1 in Stage 2, shown in (8). η should be designed according to (7). η can be chosen according to the mean value of u_{max}. According to (1), (5), (7), the expected η is in (11). If the modulation index is 0.85, the expected η will be 35%, which is lower than the traditional value (50%).

$$\eta=\frac{\bar{u}_{\max}}{2V_{dc}}\approx\frac{0.83MV_{dc}}{2V_{dc}}=0.415M \tag{11}$$

E. Comparison with the Traditional HMMC

An HMMC with 35% FB-SMs and the proposed auxiliary circuit is compared with a traditional HMMC with 50% FB-SMs, as described in Table I. The 3.3 kV IGBTs (FZ1500R33HL3 $2758), 2.4 kV thyristors (T460N24TOF $168), and 4.5 kV diodes (VS-SD553C45S50L $198) are considered. The total number of IGBTs is 18N in the traditional HMMC, where N is the number of SMs in each arm. 16.2N+2 IGBTs, 2.75N thyristors, 1.47N diodes are needed in the proposed method. Fast mechanical disconnectors are employed in traditional HMMC as well, thus are not compared here [14]. The total semiconductor cost of the proposed method is about 91.5% of the traditional HMMC.

The power losses of the proposed auxiliary circuit are mainly caused by the LCSs, which are much lower than the losses of FB-SMs. Since the proportion of the FB-SMs has been reduced, the total loss of the proposed method is about 91.4% of the traditional HMMC. V_R of the proposed topology is twice of the traditional HMMC. According to (2) and (10), the proposed method's fault current decreasing rate is about 4.4 times of the traditional HMMC (M = 0.85). The dc fault current decreasing rate is decisive for the dc fault clearance time. Since the proposed method has a much higher decreasing rate of the dc fault current than the traditional HMMC, its dc fault current clearance time will be shorter.

Although the proposed auxiliary circuit uses extra devices, fewer IGBTs are needed in the HMMC since the proportion of FB-SMs is reduced. The loss and total semiconductor cost of the converter with the proposed circuit are lower than the traditional HMMC (with 50% FB-SMs). The size, footprint, and reliability of the proposed circuit should be further assessed in future work. Thanks to the participation of HB-SMs, the DCFCC of the proposed topology is much strong than the traditional HMMC.

TABLE I
COMPARISON WITH THE TRADITIONAL HMMC

Methods	Traditional HMMC	Proposed method
FB-SM proportion	50%	35%
Total semiconductor cost (p.u.)	1	0.915
Total Loss (p.u.)	1	0.914
V_R	$0.5V_{dc}$	V_{dc}
Decreasing rate of i_{dc} (p.u.)	1	4.4

III. SIMULATION RESULTS

An HMMC HVDC link is built in Matlab/Simulink to verify the proposed method. Parameters of the HMMC are shown in Table II. The aggregate module in [15] is used to model the HB-SMs and FB-SMs in the HMMC to accelerate the simulation speed. The model can also simulate the dc fault blocking capability using the anti-parallel diodes in the arm. Since the rectifier mode converter suffers from a larger dc fault current than the inverter mode converter, the simulation results are from the rectifier in a point-to-point HVDC link. The polo-to-pole dc voltage of the MMC is 640 kV. A dc side short circuit fault occurs at $t = 0.5$ s. The MMC starts to clear the dc fault at $t = 0.503$ s. The opening time of S1 and S2 is set as 5 ms in the model.

TABLE II
SETUP OF THE HMMC

Parameters	Simulation	Experiment
Dc voltage	640 kV	200 V
Rated dc current	1.56 kA	5 A
AC line voltage	333 kV	98 V
Modulation index	0.85	0.8
Number of HB-SMs per arm	231	2
Number of FB-SMs per arm	125	1
FB-SMs proportion	35.11%	33.33%
SM voltage	1.8 kV	66.67 V
SM capacitance	17 mF	1.12 mF
Arm inductance	52.94 mH	4.62 mH
Dc inductance	1515 mH	92 mH

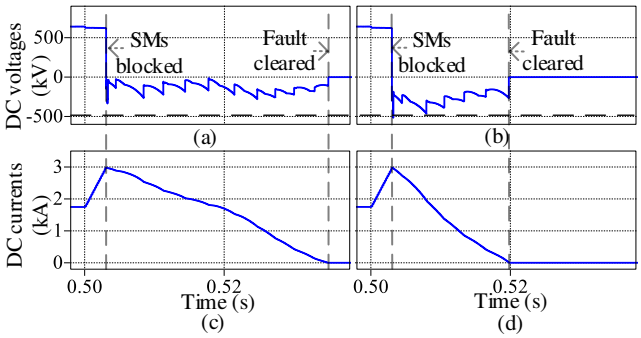

Fig. 4. Simulation results of the traditional HMMC. (a) V_{dc} when η is 0.35, (b) V_{dc} when η is 0.5, (c) i_{dc} when η is 0.35, (d) i_{dc} when η is 0.5.

Fig. 4 shows simulation results of the traditional HMMC when η is 0.35 and 0.5. The dc fault current of the traditional HMMC with 35% FB-SMs and 50% FB-SMs are cleared at t = 0.535 s and t = 0.52 s, respectively. It can be seen that the dc fault current is cleared faster, and the negative dc voltage is larger when η is 0.5, which is consistent with (2) and (3).

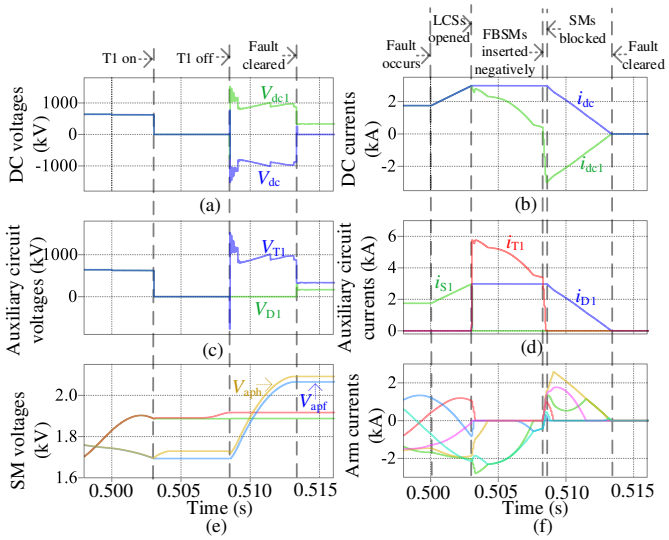

Fig. 5. Simulation results of the proposed topology. (a) Converter terminal dc voltage V_{dc1} and line side dc voltage V_{dc}, (b) converter terminal dc current i_{dc1} and line side dc current i_{dc}, (c) voltages of D1, T1; (d) currents of S1, D1, T1, (e) HB- and FB-SM voltages in one phase, (f) arm currents.

Simulation results of the proposed topology are shown in Fig. 5. In Fig. 5(a), the dc voltages are clamped to zero when T1 is conducting. After T1 is turned off, V_{dc1} and V_{dc} are opposite. The maximum negative value of V_{dc} is much larger than that of the traditional HMMC. In Fig. 5(b), i_{dc1} decreases after LCSs are opened, while i_{dc} is nearly unchanged. i_{dc1} and i_{dc} decrease rapidly after blocking the converter. The dc fault current of the proposed method is cleared at t = 0.513 s, which is 7 ms earlier than the traditional HMMC with 50% FB-SMs. Since the ac voltage and the SM voltages in the fault current path are changing during the dc fault clearing process, the dc fault current changes nonlinearly. In Fig. 5(c), the maximum voltage stress of D1 is close to the rated dc voltage, the maximum voltage stress of T1 is close to twice the rated dc voltage. In Fig. 5(d), the current of S1 i_{S1} is transferred to D1 and T1 when LCSs are opened. The current of T1 decreases to zero rapidly after FB-SMs are inserted negatively. The maximum current stress of D1 is close to the dc fault current, the maximum current stress of T1 is close to twice the dc fault current. As shown in Fig. 5(e), the capacitor voltages in both HB- and FB-SMs increase, which indicates that they have participated in blocking the dc fault current and absorbing the fault current energy stored in inductors. Thanks to this feature, the proposed method can avoid the expensive main breaker (mainly IGBTs) and large capacity energy absorbing components (MOVs) employed in the typical hybrid DCCB and therefore has a better techno-economic performance. Fig. 5(f) shows that the arm currents are within the acceptable range. Simulation results are consistent with the analysis.

IV. EXPERIMENTAL RESULTS

A three-phase HMMC with two HB-SMs and one FB-SM in each arm is built to validate the proposed method, as shown in Fig. 6. Parameters of the prototype are shown in Table II.

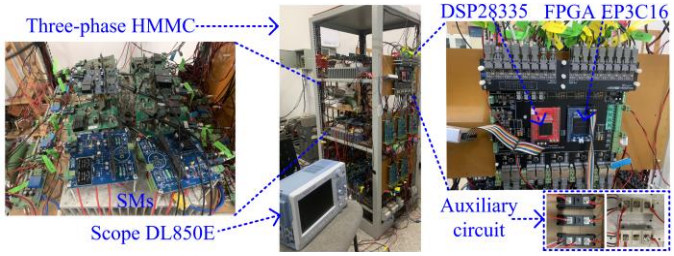

Fig. 6. Photography of the experimental setup.

Experimental results of the traditional HMMC when η is 0.33 and 0.5 are shown in Fig. 7. By comparing Figs. 7(a) and (b), it can be seen that a larger η can lead to a larger negative dc voltage and therefore, a larger fault current decreasing rate.

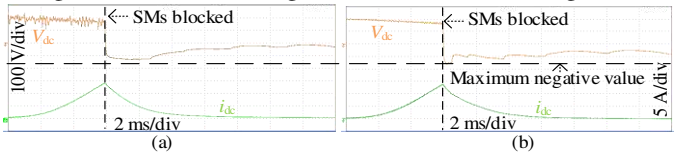

Fig. 7. Experimental results of the traditional HMMC. (a) V_{dc} and i_{dc} when η is 0.33; (b) V_{dc} and i_{dc} when is η is 0.5.

Experimental results of the proposed topology are shown in Fig. 8. In Fig. 8(a), V_{dc1} and V_{dc} are clamped to zero when T1 is on. After T1 is off, V_{dc1} is opposite to V_{dc}. In Fig. 8(b), i_{dc1} decreases much faster than i_{dc} after LCSs are opened. When all SMs are blocked, i_{dc1} and i_{dc} are opposite and decrease to zero rapidly. Comparing Fig. 8(b) with Fig. 7(b), the dc fault current of the proposed method is cleared 4 ms earlier than the traditional HMMC with 50% FB-SMs. In Fig. 8(c), D1 and T1 withstand the rated dc voltage during normal operation. The maximum voltage stress of T1 is close to twice the rated dc voltage. In Fig. 8(d), i_{S1} is transferred to T1 and D1 when LCSs are opened. i_{T1} decreases rapidly when FB-SMs are inserted negatively. In Fig. 8(e), both HB- and FB-SM voltages increase. Fig. 8(f) shows the waveforms of arm currents, which are within the acceptable range. Experimental results are consistent with simulation results, which validate the effectiveness of the proposed topology.

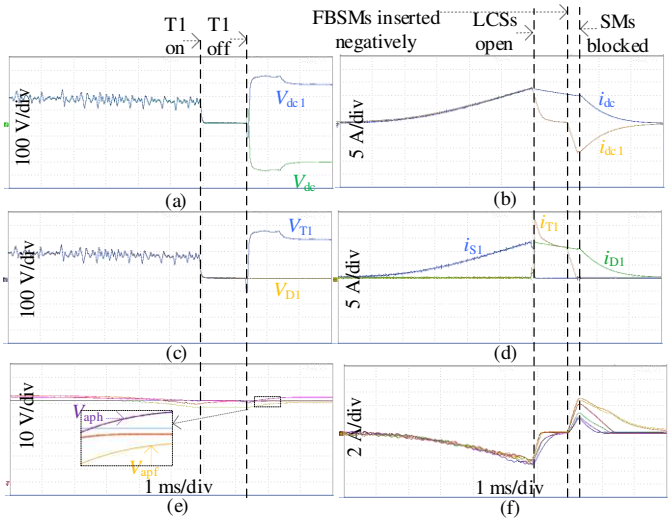

Fig. 8. Experimental results of the proposed topology. (a) V_{dc1} and V_{dc}, (b) i_{dc1} and i_{dc}, (c) V_{D1}, V_{T1}, (d) i_{S1}, i_{D1}, i_{T1}, (e) HB- and FB-SM voltages in one phase, (f) arm currents.

VII. Conclusion

An auxiliary circuit is proposed for the hybrid MMC, which can significantly increase the maximum reverse-biased voltage by enabling both HB- and FB-SMs to participate in the dc fault clearing. Thanks to the proposed circuit, not only the dc line fault clearing speed is accelerated, but also the proportion of MMC's FB-SMs is reduced. The proposed method can enhance the dc fault clearing capability of the HMMC with reduced loss & semiconductor cost, which is more techno-economical than the traditional HMMC.

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