Modeling for Complex Modular Power Electronic Transformers Using Parallel Computing

Moke Feng, Chenxiang Gao, Jianzhong Xu*, Senior Member, IEEE, Chengyong Zhao,
Senior Member, IEEE, and Gen Li, Member IEEE

Abstract—The modular power electronic transformer (PET) faces difficulty carrying out microsecond-level electromagnetic transient (EMT) simulations. This paper provides a high-speed and high-precision simulation method capable of eliminating the internal nodes and reducing the order of the nodal admittance matrix. Meanwhile, the parallel computing is integrated into the whole solution process, which achieves a significant simulation speedup. A physical prototype is established to prove that the detailed model is sufficient to reflect the dynamics of physical devices. Moreover, simulations in PSCAD/EMTDC are carried out to compare the proposed method with the detailed model in terms of accuracy and time efficiency. Simulation results show that the proposed method is accurate to simulate the external and internal dynamics of PET with hundreds of times simulation speed acceleration.

Index Terms—**power electronic transformer (PET), electromagnetic transient (EMT) modeling, order reduction of matrices, parallel computing.**

I. INTRODUCTION

As one of the key equipment in energy conversion and grid interconnection, power electronic transformers (PETs) have attracted extensive research on designing their topologies [1], control strategies [2], and modeling methods [3], [4]. With the increasing deployment of medium- and low-voltage (MV and LV) DC distribution networks, it is foreseen that there will be wide applications of PETs in AC/DC and DC/DC conversion between grids with multiple voltage levels. However, due to the sophisticated configuration and a large number of power modules (PMs), using detailed switching models of PETs will result in a heavy computational burden in electromagnetic transient (EMT) simulations. Especially when focusing on converter-level and system-level studies, e.g., capacitor voltage ripple, arm current, converter power flow, system operation, control, and protection, such problems are more prominent.

The computational burden will be hefty if a complex system (e.g., a multi-terminal MVDC grid with several multi-port

PETs) is modeled in EMT simulation tools, for instance, in PSCAD/EMTDC. Simulating one second may take several hours or even longer if the converters and PET are all modeled using the detailed switching models [5]. This is unacceptable for off-line EMT simulations and will induce significant challenges for real-time simulations as well.

Some modeling approaches have been proposed but focus on some specific needs. Small-signal modeling and impedance modeling are used for steady-state stability analysis and control system design but not for EMT simulations [6]-[8]. Averaged-value modeling ignores the internal characteristics of PETs, such as capacitor voltage ripples, transformer voltages and currents, and internal switching stresses. They are inaccurate or even inapplicable for EMT simulations, especially when simulating very fast transient processes, e.g., DC fault analysis [9], [10].

Conventional modeling methods have a narrow scope of applications. In order to address the dilemma of simulation accuracy and speed, some high-speed and high-precision modeling methods for power electronic (PE) equipment have been proposed. A nested fast and simultaneous solution for time-domain simulation of PE systems is first proposed by Kai Strunz [11]. Based on this algorithm, A. M. Gole and Udana G. propose the efficient modeling method for the modular multilevel converter (MMC) [12]. This underpinning method provides a solid foundation for high-speed and high-precision modeling of PE equipment. Afterwards, optimized algorithms are proposed to enhance the existing methods. In [13], the circuit analysis is changed to a matrix solution, and the modeling method becomes applicable for arbitrary multi-port PMs. Relying on the research of [3], [14], and [15], the method in [14] is now applicable to various kinds of multi-port PM topologies and can be used for PETs and other PE equipment.

However, the rapid development of PE-based systems brings new challenges to EMT simulations. For instance, the modeling approach used for the common single-phase transformer is not applicable to the multi-winding transformer in the multiple-active-bridge (MAB) of PETs [16] because the multi-winding transformer does not have a star equivalent. As a result, new modeling theories and techniques are required for EMT simulations.

Meanwhile, parallel computing technology brings new possibilities for EMT simulations. There are various types of parallelization, including CPU parallelization based on shared memory, multi-core parallelization using GPUs, and

distributed parallelization among multiple computational nodes. These techniques can effectively increase the speed of simulation. However, the computational loads and power networks need to be appropriately designed to achieve efficient parallelization.

In order to adapt to the needs of PE-based systems, it is necessary to enhance the existing modeling methods for system analysis. In this paper, a modeling approach for complex PET is proposed. The main contributions of this paper are:

1) A unified magnetic equivalent circuit (UMEC) model of a specifically designed multi-winding transformer is derived, which bridges the gap that the existing UMEC transformer models are mainly for single-phase or three-phase transformers [17], [18].

2) A PM equivalent model in which the internal nodes are eliminated is proposed to reduce the number of electric nodes. Thanks to this PM model, the simulation efficiency is significantly improved.

3) An efficient cascading scheme for a large number of multi-port sub-modules (SMs) is proposed to transform the complex matrix calculations into simple addition operations.

4) The proposed model exhibits fault blocking capability without involving additional circuits, which also avoids the sophisticated state variable passing procedure.

5) Parallel computing is organically integrated into the modeling procedures to develop a high-speed and high-precision model. In the proposed method, the calculations of transformers, PMs, and bridge arms are assigned to different CPU cores for parallel computing to speed up the calculation.

Finally, the proposed method is validated through simulations. The modeling and parallelization steps are summarized in Fig. 1.
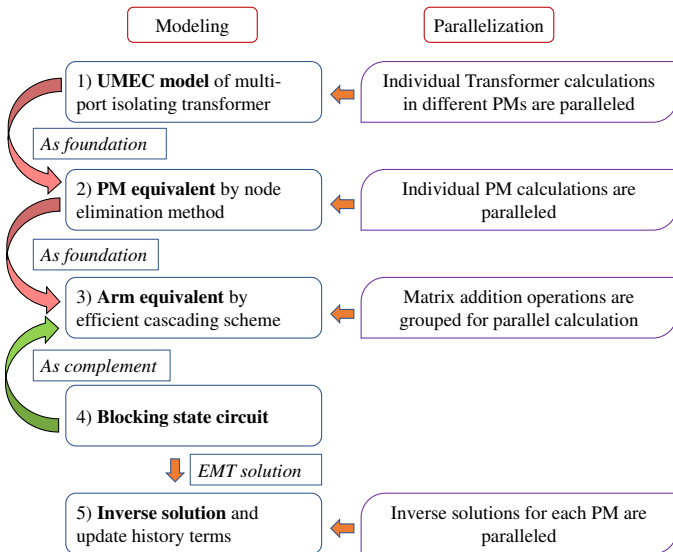

Fig. 1. Procedures of the modeling and parallelization.

II. MODELING PROCESS OF PET

In this section, the Xiaoertai PET (XET-PET) constructed in Zhangbei, China, is used to demonstrate the proposed modeling approach. The topology of the XET-PET is shown in Fig. 2. The reason we investigate this topology is not only because it features in higher power density, smaller transformer size, and higher flexibility than existing PETs, but also its technology readiness has been validated by this Xiaoertai project [19]. The XET-PET is composed of an upper arm and a lower arm. The three phases are coupled through PMs using a three-phase MAB. Each PM consists of four energy conversion units: AC/DC, DC/AC, AC/AC (high-frequency isolating transformer), and AC/DC. The carrier-phase-shifted PWM (CPS-PWM) and single-phase-shifted (SPS) modulation [20] strategies are used to regulate the power between the MVDC and LVDC ports.
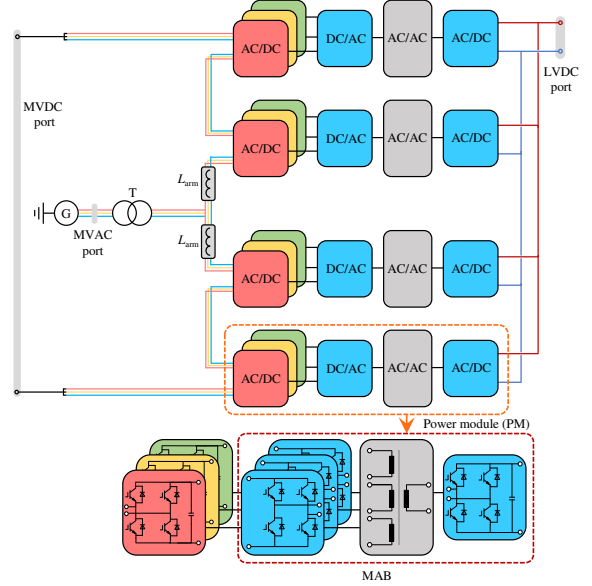
Fig. 2. Topology of the XET-PET.

A. Modeling for the Isolating Transformer

The circuit in Fig. 2 needs to be discretized before it can be used for simulation. IGBT/Diode switch group is usually seen as a two-value (ON/OFF) resistor whose resistance is determined by the IGBT gate signal. The discretization of fundamental LC components has been well described in [21]. Taking the capacitor as an example, the differential equation of a capacitor is:

$$u(t) = C \frac{di(t)}{dt}. \qquad (1)$$

where u is the voltage across the capacitor, i is its current and C is its capacitance.

Change the form of (1):

$$i(t) = \frac{1}{C} \int_0^{t-\Delta t} u(t)dt + \frac{1}{C} \int_{t-\Delta t}^t u(t)dt$$
$$= i(t-\Delta t) + \frac{1}{C} \int_{t-\Delta t}^t u(t)dt \qquad (2)$$

In (2), Δt is the simulation time-step. Discretize (2) with the trapezoidal integration method:

$$i(t) = i(t - \Delta t) + \frac{\Delta t}{2C} \left[u(t - \Delta t) + u(t) \right]$$

$$\Rightarrow i(t) = \frac{\Delta t}{2C} u(t) + \left[i(t - \Delta t) + \frac{\Delta t}{2C} u(t - \Delta t) \right]. \qquad (3)$$

$$\Rightarrow i(t) = G_C u(t) + J_{C\_HIS}(t)$$

Equation (3) shows that the equivalent circuit of the capacitor is a Norton circuit, as in Fig. 3. The history current source $J_{C\_HIS}(t)$ is determined by the voltage and current of the last time-step.
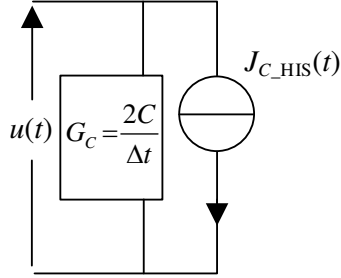

Fig. 3. Discretized capacitor equivalent circuit.

The modeling of the transformer is presented as follows. There are several transformer models: matrix representation (BCTRAN) model, saturable transformer component (STC) model, and topology-based model [22]. BCTRAN is the simplest model derived from matrix equations without considering the structure of the transformer and saturation characteristics. BCTRAN will only be reasonably accurate when the frequency is below 1 kHz and the number of windings is less than 3. STC is capable of simulating saturation with an additional current source, but the issue of numerical instability has been reported in [23]. The topology-based model considers the core geometry of the transformer, and saturation effects of each limb of the core are well simulated. The computational burden varies according to the complexity of the transformer topology.

The UMEC model is a kind of topology-based model, its parameters are easy to obtain, and more importantly, it is not computationally expensive [24]. Therefore, UMEC is selected for modeling the four-winding transformer in the XET-PET. The structure of the four-winding high-frequency transformer is shown in Fig. 4(a).
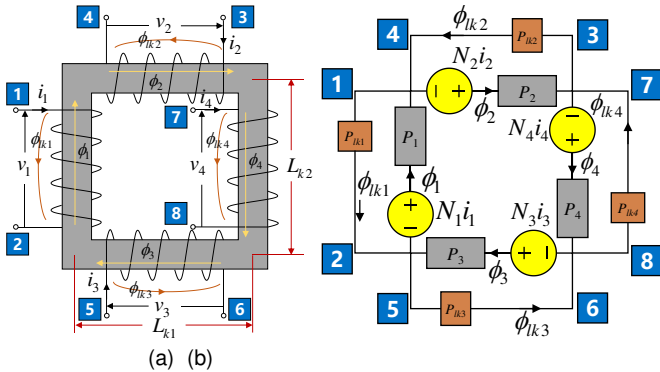

(a)   (b)

Fig. 4. The four-winding transformer and its UMEC. (a) four-winding transformer; (b) UMEC structure.

The windings share the same core and are wound around the four limbs. ϕ_1 to ϕ_4 are the winding limb fluxes, ϕ_{lk1} to ϕ_{lk4} are the leakage fluxes. The limb lengths are L_{k1} and L_{k2}. The winding voltages v_1 to v_4 and currents i_1 to i_4 are illustrated in Fig. 4(a) as well. The port nodes are numbered from 1 to 8. The UMEC structure of Fig. 4(a) is represented by Fig. 4(b). Magnetomotive force (MMF) sources $N_1 i_1(t)$ to $N_4 i_4(t)$ represent each winding individually. The winding voltages are used to calculate the winding limb fluxes. P_1 to P_4 are the permeances of the transformer winding limbs, P_{lk1} to P_{lk4} are the permeances of the leakage circuits.

According to [25], the voltages v_i (i=1,2,3,4) and currents i_i (i=1,2,3,4) satisfy the following relationship:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} y_{T11} & y_{T12} & y_{T13} & y_{T14} \\ y_{T12} & y_{T22} & y_{T23} & y_{T24} \\ y_{T13} & y_{T23} & y_{T33} & y_{T34} \\ y_{T14} & y_{T24} & y_{T34} & y_{T44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} + \begin{bmatrix} i_{ns1} \\ i_{ns2} \\ i_{ns3} \\ i_{ns4} \end{bmatrix}, \qquad (4)$$

where y_{Tij} (i, j=1,2,3,4) are the equivalent admittances, i_{nsi} (i=1,2,3,4) represent the influences of the winding currents of last time-step.

Equation (4) represents a Norton equivalent circuit (EC) shown in Fig. 5, which is like a diamond. A branch is formed between every two nodes. Hence there are total $\sum_{i=1}^{8-1} i = 28$ branches. In the diamond circuit, each blue line represents an admittance branch with a time-varying admittance value. The Norton current sources are connected across the two nodes of each port.
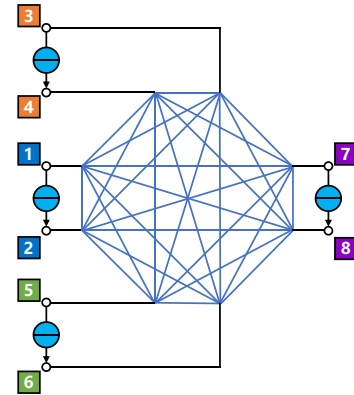
Fig. 5. Diamond Norton equivalent circuit of the four-winding transformer, PM EC, and arm EC.

It is worth noting that all of the 8-node circuits have the same pattern as the diamond circuit. Therefore, in the following analysis, the structures of PM EC and arm EC are diamond circuits as well.

B. Modeling for the Power Modules

Replace the capacitor, switch and transformer models with the corresponding discretized circuit, and select the node NDC as the reference node. The PM companion circuit is obtained as in Fig. 6. The cascaded H-bridge (CHB) sides are connected in cascade to withstand the MVDC voltage. AC voltages and currents are rectified, and the energy is transmitted to the MAB side.

G_1-G_{28} represent the admittance of the two-value resistors, G_{C1}-G_{C4} represent the equivalent capacitor conductance, and J_{HIS_C1}-J_{HIS_C4} are the capacitor history current sources; J_{tr_1}-J_{tr_4} are the transformer history current sources.

In each PM, there are 21 nodes (excluding the reference node NDC) and 60 branches (32 circuit branches and 28 transformer equivalent branches). The node-branch incidence matrix A is 21×60, and the branch admittance matrix Y_{branch} is 60×1.
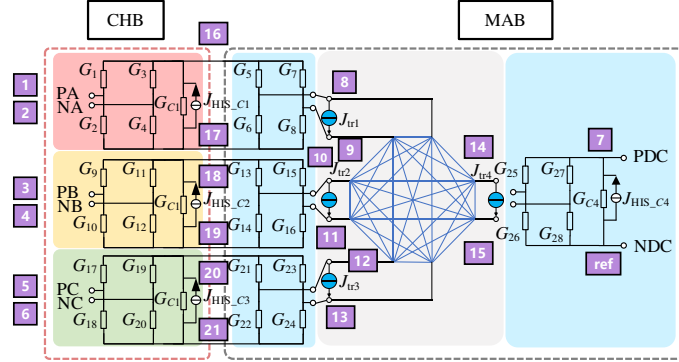

Fig. 6. Companion circuit of PM in the XET-PET.

Nodal admittance matrix Y is obtained with A and Y_{branch}:

$$Y = AY_{branch}A^T. \tag{5}$$

Y is 21×21, as illustrated in Fig. 7, in which the orange cubes represent the non-zero elements in the matrix. Y is arranged in the order of external nodes and internal nodes.
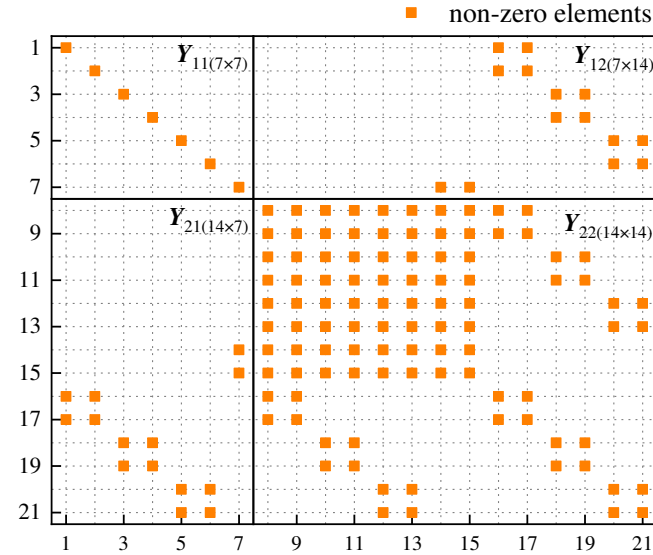

Fig. 7. Structure of the nodal admittance matrix Y.

Injection current vector J is directly written according to Fig. 6:

$$\begin{cases} J = \begin{bmatrix} \mathbf{0}_{(6\times1)} & -J_{HIS\_C4} & J_{tr(1\times8)}^T & J_{C(1\times6)}^T \end{bmatrix}^T \triangleq \begin{bmatrix} J_{EX(1\times7)}^T & J_{IN(1\times14)}^T \end{bmatrix}^T \\ J_{tr} = \begin{bmatrix} -J_{tr\_1} & J_{tr\_1} & -J_{tr\_2} & J_{tr\_2} & -J_{tr\_3} & J_{tr\_3} & -J_{tr\_4} & J_{tr\_4} \end{bmatrix} \\ J_C = \begin{bmatrix} -J_{HIS\_C1} & J_{HIS\_C1} & -J_{HIS\_C2} & J_{HIS\_C2} & -J_{HIS\_C3} & J_{HIS\_C3} \end{bmatrix} \end{cases} \tag{6}$$

According to Fig. 6, the node voltage equation of the PM is:

$$YV = J \tag{7}$$

Rewrite (7):

$$\begin{bmatrix} Y_{11(7\times7)} & Y_{12(7\times14)} \\ Y_{21(14\times7)} & Y_{22(14\times14)} \end{bmatrix} \begin{bmatrix} V_{EX(1\times7)} \\ V_{IN(1\times14)} \end{bmatrix} = \begin{bmatrix} J_{EX(1\times7)} \\ J_{IN(1\times14)} \end{bmatrix} \tag{8}$$

where the subscript "EX" indicates external voltage and "IN" indicates internal voltage. Y is partitioned according to the external and internal node division.

Expand (8):

$$\begin{cases} Y_{11}V_{EX} + Y_{12}V_{IN} = J_{EX} \\ Y_{21}V_{EX} + Y_{22}V_{IN} = J_{IN} \end{cases} \tag{9}$$

Consequently, we can obtain:

$$(Y_{11} - Y_{12}Y_{22}^{-1}Y_{21})V_{EX} = J_{EX} - Y_{12}Y_{22}^{-1}J_{IN}$$
$$\Rightarrow Y_{EQ}V_{EX} = J_{EQ} \tag{10}$$

$$V_{IN} = Y_{22}^{-1}\left(J_{IN} - Y_{21}V_{EX}\right) \tag{11}$$

From the perspective of the circuit, V_{EX} can either be obtained with a complex matrix Y in (5) or by a simple one Y_{EQ} in (10). Replace Y with Y_{EQ}, although the circuit is more simplified, the calculation result of V_{EX} does not change. Therefore, the EC, which only contains the external node, is obtained without losing accuracy.

Y_{EQ} is the Schur's complement matrix [26] of Y, whose values are:

$$Y_{EQ} = Y_{11} - Y_{12}Y_{22}^{-1}Y_{21}$$

$$= \begin{bmatrix} y_{eq11} & -y_{eq12} & -y_{eq13} & -y_{eq14} & -y_{eq15} & -y_{eq16} & -y_{eq17} \\ -y_{eq12} & y_{eq22} & -y_{eq23} & -y_{eq24} & -y_{eq25} & -y_{eq26} & -y_{eq27} \\ -y_{eq13} & -y_{eq23} & y_{eq33} & -y_{eq34} & -y_{eq35} & -y_{eq36} & -y_{eq37} \\ -y_{eq14} & -y_{eq24} & -y_{eq34} & y_{eq44} & -y_{eq45} & -y_{eq46} & -y_{eq47} \\ -y_{eq15} & -y_{eq25} & -y_{eq35} & -y_{eq45} & y_{eq55} & -y_{eq56} & -y_{eq57} \\ -y_{eq16} & -y_{eq26} & -y_{eq36} & -y_{eq46} & -y_{eq56} & y_{eq66} & -y_{eq67} \\ -y_{eq17} & -y_{eq27} & -y_{eq37} & -y_{eq47} & -y_{eq57} & -y_{eq67} & y_{eq77} \end{bmatrix}, \tag{12}$$

$$J_{EQ} = J_{EX} - Y_{12}Y_{22}^{-1}J_{IN} = \begin{bmatrix} j_{eq1} & j_{eq2} & j_{eq3} & j_{eq4} & j_{eq5} & j_{eq6} & j_{eq7} \end{bmatrix}^T, \tag{13}$$

where $y_{eqik}(i=1,2,\dots,7; k=1,2,\dots,7)$ are nodal admittances of the EC. As Y_{EQ} is symmetric, the lower left corner elements are in gray for better redability. $j_{eqi}(i=1,2,\dots,7)$ are injection currents from the reference node to nodes 1 to 7 respectively.

C. Modeling for the Arms

In [3], the cascading of arms uses a lot of matrix operations, which slows down the simulation speed. A method with better performance is presented as follows.

In PM, external nodes form four ports. The circuit isolation feature of the four-winding transformer makes the ports strict ports wherein the input and output currents are equal. Therefore, Y_{EQ} and J_{EQ} have more characteristic forms:

$$Y_{eq} = \begin{bmatrix} g_{11}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} & g_{12}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} & g_{13}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} & g_{14} \\ g_{12}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} & g_{22}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} & g_{23}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} & g_{24} \\ g_{13}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} & g_{23}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} & g_{33}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} & g_{34} \\ g_{14} & g_{24} & g_{34} & g_{44} \end{bmatrix}, \tag{14}$$

$$\boldsymbol{J}_{eq} = \begin{bmatrix} l_1 & -l_1 & l_2 & -l_2 & l_3 & l_4 & -l_4 \end{bmatrix}^T, \quad (15)$$

where g_{ik} (1=1,2,3,4; k=1,2,3,4) are the port admittance coefficients. $l_i(i$=1,2,3,4) are the input port currents. The last column of $\boldsymbol{Y}_{eq}$ only contains single values because the rows and columns of the reference node NDC are removed.

Based on (14) and (15), the port equation is obtained:

$$\begin{bmatrix} i_{p1} \\ i_{p2} \\ i_{p3} \\ i_{p4} \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & g_{13} & g_{14} \\ g_{12} & g_{22} & g_{23} & g_{24} \\ g_{13} & g_{23} & g_{33} & g_{34} \\ g_{14} & g_{24} & g_{34} & g_{44} \end{bmatrix} \begin{bmatrix} v_{p1} \\ v_{p2} \\ v_{p3} \\ v_{p4} \end{bmatrix} + \begin{bmatrix} l_1 \\ l_2 \\ l_3 \\ l_4 \end{bmatrix}, \quad (16)$$

where i_{pi} and v_{pi}(i=1, 2, 3, 4) are the port currents and voltages. PA-NA, PB-NB, and PC-NC ports are defined as the input ports. PDC-NDC port is the output port.

Rewrite (16) in partitioned matrix form:

$$\begin{bmatrix} \boldsymbol{i}_{in(3\times1)} \\ \boldsymbol{i}_{out(1\times1)} \end{bmatrix} = \begin{bmatrix} \boldsymbol{g}_{in\text{-}in(3\times3)} & \boldsymbol{g}_{in\text{-}out(3\times1)} \\ \boldsymbol{g}_{out\text{-}in(1\times3)} & \boldsymbol{g}_{out\text{-}out(1\times1)} \end{bmatrix} \begin{bmatrix} \boldsymbol{v}_{in(3\times1)} \\ \boldsymbol{v}_{out(1\times1)} \end{bmatrix} + \begin{bmatrix} \boldsymbol{j}_{in(3\times1)} \\ \boldsymbol{j}_{out(1\times1)} \end{bmatrix}. \quad (17)$$

Re-arrange (17) and obtain $\boldsymbol{h}$ and $\boldsymbol{j}_h$ as in (18)-(20):

$$\begin{bmatrix} \boldsymbol{v}_{in(3\times1)} \\ \boldsymbol{i}_{out(1\times1)} \end{bmatrix} = \begin{bmatrix} \boldsymbol{g}_{in\text{-}in}^{-1} & -\boldsymbol{g}_{in\text{-}in}^{-1}\boldsymbol{y}_{in\text{-}out} \\ \boldsymbol{g}_{out\text{-}in}\boldsymbol{g}_{in\text{-}in}^{-1} & \boldsymbol{g}_{out\text{-}out} - \boldsymbol{g}_{out\text{-}in}\boldsymbol{g}_{in\text{-}in}^{-1}\boldsymbol{g}_{in\text{-}out} \end{bmatrix} \begin{bmatrix} \boldsymbol{i}_{in(3\times1)} \\ \boldsymbol{v}_{out(1\times1)} \end{bmatrix}$$

$$+ \begin{bmatrix} -\boldsymbol{g}_{in\text{-}in}^{-1}\boldsymbol{j}_{in} \\ \boldsymbol{j}_{out} - \boldsymbol{g}_{out\text{-}in}\boldsymbol{g}_{in\text{-}in}^{-1}\boldsymbol{j}_{in} \end{bmatrix}, \quad (18)$$

$$\triangleq \boldsymbol{h}_{(4\times4)} \begin{bmatrix} \boldsymbol{i}_{in} \\ \boldsymbol{v}_{out} \end{bmatrix} + \boldsymbol{j}_{h(4\times1)}$$

where

$$\boldsymbol{h} = \begin{bmatrix} \boldsymbol{g}_{in\text{-}in(3\times3)}^{-1} & -\boldsymbol{g}_{in\text{-}in}^{-1} \begin{bmatrix} g_{14} \\ g_{24} \\ g_{34} \end{bmatrix}_{(3\times1)} \\ \begin{bmatrix} g_{14} & g_{24} & g_{34} \end{bmatrix}\boldsymbol{g}_{in\text{-}in(1\times3)}^{-1} & g_{44} - \begin{bmatrix} g_{14} & g_{24} & g_{34} \end{bmatrix}\boldsymbol{g}_{in\text{-}in}^{-1}\begin{bmatrix} g_{14} \\ g_{24} \\ g_{34} \end{bmatrix}_{(1\times1)} \end{bmatrix}, \quad (19)$$

$$\boldsymbol{j}_h = \begin{bmatrix} -\boldsymbol{g}_{in\text{-}in}^{-1}\begin{bmatrix} l_1 \\ l_2 \\ l_3 \end{bmatrix}_{(3\times1)} \\ l_4 - \begin{bmatrix} g_{14} & g_{24} & g_{34} \end{bmatrix}\boldsymbol{g}_{in\text{-}in}^{-1}\begin{bmatrix} l_1 \\ l_2 \\ l_3 \end{bmatrix}_{(1\times1)} \end{bmatrix}, \quad \boldsymbol{g}_{in\text{-}in}^{-1} = \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{12} & g_{22} & g_{23} \\ g_{13} & g_{23} & g_{33} \end{bmatrix}^{-1}. \quad (20)$$

The input ports of PMs are connected in series. Thereby, they have the same current. The output ports are in parallel, of which the voltages are equal. Then, the arm input voltage v_{inarm} and output current i_{outall} are obtained by adding the $\boldsymbol{h}$ and $\boldsymbol{j}_h$ of all PMs:

$$\begin{bmatrix} \boldsymbol{v}_{inarm} \\ \boldsymbol{i}_{outall} \end{bmatrix} = \sum_{k=1}^{N} \boldsymbol{h}_k \begin{bmatrix} \boldsymbol{i}_{in} \\ \boldsymbol{v}_{out} \end{bmatrix} + \sum_{k=1}^{N} \boldsymbol{j}_{hk}, \quad (21)$$

where N is the number of the PMs in an arm.

Re-arrange (21) to make $\boldsymbol{i}_{in}$ and $\boldsymbol{i}_{outall}$ on the left-hand side of the equation and we can obtain:

$$\begin{bmatrix} \boldsymbol{i}_{in} \\ \boldsymbol{i}_{outall} \end{bmatrix} = \boldsymbol{Y}_{arm} \begin{bmatrix} \boldsymbol{v}_{inarm} \\ \boldsymbol{v}_{out} \end{bmatrix} + \boldsymbol{j}_{arm}. \quad (22)$$

Equation (22) indicates the equivalent circuit of the arm, in which $\boldsymbol{Y}_{arm}$ is the final result of the arm equivalent admittance matrix, and $\boldsymbol{j}_{arm}$ is the arm injection current.

D. Blocking State Circuit

In the blocking state, all the IGBTs are turned OFF. Diodes are uncontrollably turning ON and OFF. The gate signal no longer determines the resistance of a switch group. To simulate such a situation, special modifications should be done on the equivalent circuit. Generally, the blocking state circuit is obtained by analyzing the operation states of the network. In [3] and [15], an additional blocking circuit is established to describe the blocking state dynamics. When the PET is blocked, the additional circuit will replace the normal operation circuit. The state variables (mainly capacitor and transformer history current source values) are transferred between the two circuits when the operating state changes. However, this approach is slow and inconvenient to program.

In this paper, an integrated blocking state circuit is introduced. The blocking state circuit analysis is given first. The freewheeling process of the transformer is rapid in the blocking state. It can be considered as finished immediately. As a result, the MAB side switches are all set as large resistors. The situation is not the same on the CHB side. Although all IGBTs are turned off, there are still currents flowing through the capacitors and freewheeling diodes as long as the input AC port voltage of the H-bridge is larger than the capacitor voltage, as the solid and dashed lines show in Fig. 8. Three phases are symmetrical, only phase A is shown.
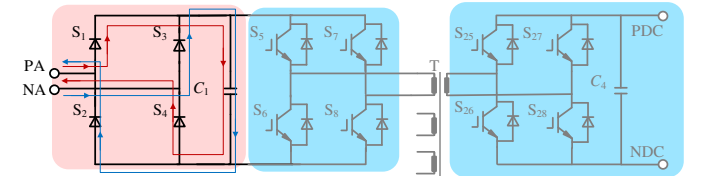

Fig. 8. Current paths of the blocking state.

To simulate the blocking characteristics, a three-phase diode H-bridge is added to the diamond arm EC to regulate the blocking state current paths, as shown in Fig. 9. To facilitate understanding, the original structure of arm EC is illustrated in Fig. 9, but it should be noted that the arm EC has already been equivalent to a diamond circuit. In each phase, two identical diode H-bridges are connected across the upper and lower arms, respectively. BRK1 to BRK4 are the switches that determine the operation state of the bridge. The detailed operation mechanism of the three-phase diode bridge will be introduced later in this subsection.
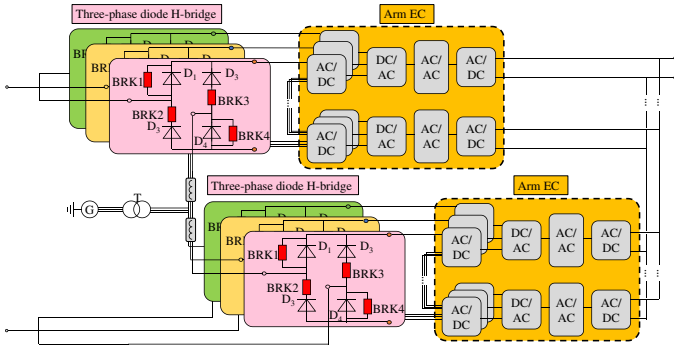
Fig. 9. Three-phase diode H-bridge together with the arm equivalent circuit.

Under normal operation state, BRK1 and BRK4 are turned on; BRK2 and BRK3 are turned off. The three-phase diode H-bridge is bi-directional with a very small resistance, which does not affect the normal operation of XET-PET.

During the fault blocking state, the current flowing over PM capacitors is unidirectional because S_1 to S_4 are turned off so that the diodes are uncontrollably conducting the current to a fixed direction, see Fig. 8. In order to simulate this operating condition, BRK1-BRK4 are turned off in the simulation program. The diode H-bridge becomes uncontrollable to regulate the current flowing over PM capacitors. Moreover, to receive the arm current, G_1 and G_4 (corresponding to S_1 and S_4) are set as a small resistor (0.001 Ω). G_2 and G_3 (corresponding to S_2 and S_3) are set to a large resistor (10^6 Ω). G_5 to G_8 and G_{25} to G_{28} are set to large resistors because the current of the MAB circuit (framed by the blue box in Fig. 8) is 0.

(a)

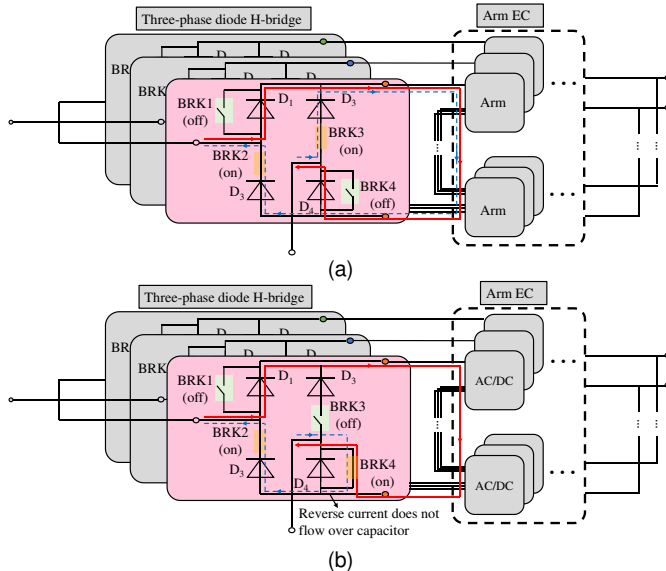Reverse current does not flow over capacitor

(b)

Fig. 10. Charging current paths in the XET-PET (upper arm): (a) general method; (b) BRK4 on and BRK3 off.

Referring to Fig. 9, BRK1 and BRK4 are turned off and BRK2 and BRK3 are turned on during the start-up charging process to realize the uncontrollable charging. The charging current path of the upper arm is shown in Fig. 10(a), which is the same as the lower arm. However, this scheme will cause a sudden voltage change in the MVDC side when the PET is deblocked [27]. A feasible solution is to slow down the charging speed by turning on BRK4 and turning off BRK3

during the start-up charging. In this way, the inverse current (dotted blue) does not charge the PMs, as in Fig. 10(b).

By integrating the three-phase diode H-bridge into upper and lower arms, and with the appropriate control scheme of the H-bridges, the blocking function is realized without additional circuits and complex state variable transmission.

E. Inverse Solution of the Circuit

Until this stage, the modeling is accomplished. Once the ECs of all arms are obtained, they will be interfaced with the external system network in the EMT simulation tool (PSCAD/EMTDC, etc.). PSCAD/EMTDC will solve the network and obtain the voltages of every node. The external node voltages of arm ECs are used to solve the internal node voltages and update the history terms. The inverse solution process is illustrated in Fig. 11. Arm node voltages are obtained from the EMT solver, with which the PM node voltages, internal capacitor voltages, and internal currents will be calculated.
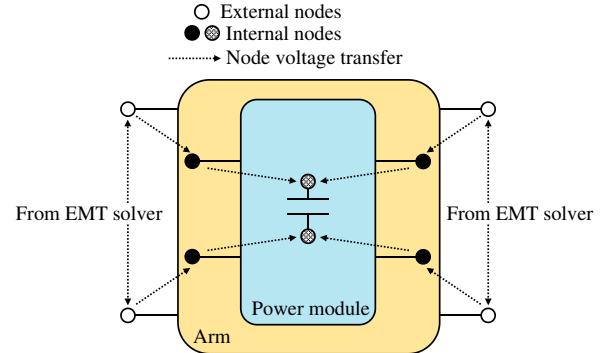

Fig. 11. Schematic diagram of the inverse solution.

The modeling and parallelization steps are summarized in Fig. 1. The modeling procedures are on the left side. The blocks on the right side explain how the parallelization is integrated into the proposed method. The UMEC transformer model is the foundation to build the PM companion circuit. The node elimination method is used to obtain the PM equivalent circuit in which the internal nodes are eliminated. With the efficient cascading scheme, the PM equivalents are connected to form the arm equivalent circuit. At last, the three-phase diode H-bridge are added to the equivalent circuit to realize the blocking function. After the EMT solution, a necessary inverse solution is carried out to update the history terms. Thanks to the modularized structure of XET-PET, the calculation of UMEC transformers, PMs, arms and inverse solutions are parallelized because the calculation of one module does not rely on the result of another one. The simulation procedure using the proposed method can be presented as the following pseudocode in Algorithm 1.

After modeling and programming, the proposed model can be used as a Blackbox in a user-defined library in EMT simulation tools. The configuration of the proposed model is easy. Users only need to input the circuit structure and necessary electric parameters, and connect it with the external system.

Algorithm 1: Modeling process for complex PET using parallel computing	
1 obtain power module companion circuit	
2 t←0	*//simulation begins*
3 **while** t<=t_max do	
4 **for** i←1 **to** L do	*//Calculate ECs of power modules. L is the number of arms, normally 3 or 6*
5 **#begin parallel calculation**	
6 **for** k←1 **to** M do	*//M is the number of power modules in an arm*
7 calculate EC of PM(i,k)	
8 calculate h(i,k) and j(i,k)	
9 **end**	
10 **#end parallel calculation**	
11 initialize h_{arm}(i) and j_{arm}(i)	
12 **#begin parallel calculation**	
13 **for** k←1 **to** M do	*//Calculate arm equivalent*
14 h_{arm}(i) = h_{arm}(i) + h(i,k)	
15 j_{arm}(i) = j_{arm}(i) + j(i,k)	
16 **end**	
17 **#end parallel calculation**	
18 calculate Y_{arm}(i) and j_{arm}(i)	
19 **end**	*//End EC calculation*
20 overlay arm ECs onto EMTDC system	
21 EMTDC solution by PSCAD	
22 **#begin parallel calculation**	
23 inverse solution to obtain eliminated node voltages and update history terms	
24 **#end parallel calculation**	
25 t←t+Δt	*//Δt is the simulation step*
26 **loop**	

III. HARDWARE EXPERIMENT VALIDATION

A down-scaled PET prototype of the XET-PET is built to validate the proposed method, as shown in Fig. 12. The high-voltage side consists of three identical boards which are connected to the three phases. Each PM capacitor is made up of three small capacitors in parallel. Delfino™ TMS320F2837xD DSP is used as the controller. IGBT triggering signals are generated from the Cyclone IV FPGA. Parameters of the prototype are in the given TABLE I.

TABLE I
PARAMETERS OF THE XET-PET PROTOTYPE

Symbols	Parameter Description	Values
$R_{startup}$	Start-up resistor (Ω)	100
f_{sys}	System fundamental frequency (Hz)	50
$V_{L\text{-}Lrated}$	Line-to-line RMS voltage on AC grid side (V)	30
$V_{C1Rated}$	Rated capacitor voltage in CHB side (V)	40
C_{CHB}	CHB side PM capacitance (μF)	4700×3
C_{MAB}	MAB side PM capacitance (μF)	4700×3
$V_{o2Rated}$	LVDC rated output DC voltage (V)	10
R_{load_MAB}	LVDC output load (Ω)	20

A detailed model (DM) with the same parameters as the prototype is also established in PSCAD/EMTDC. Fig. 13 and Fig. 14 show the comparisons of experimental results and simulation results.

In the simulation model, the hysteresis characteristic of transformer iron cores, the non-linear switching characteristics, and the parasitic parameters are not considered. Therefore, during the start-up process and steady state, there are errors between the experiment and simulation results. In Fig. 13, after isolating the start-up resistor, the periods and envelopes of the two curves match well. The maximum error is 0.1441A (3.57%) in the first peak.
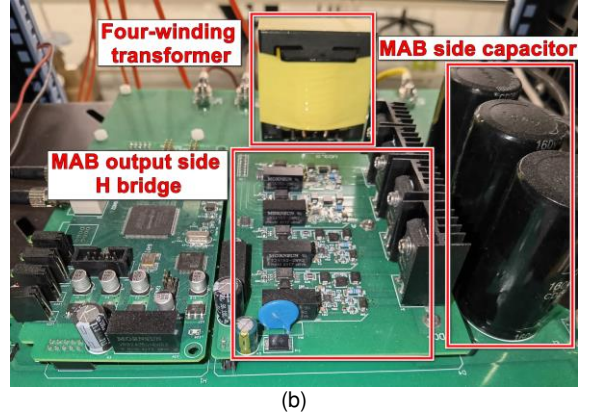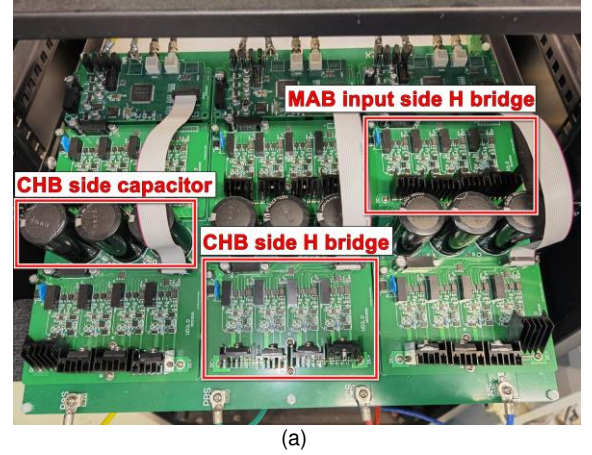

(a)

(b)

Fig. 12. Prototype of XET-PET: (a) CHB side H bridge, capacitor, and MAB input side H bridge; (b) four-winding transformer, MAB output side H bridge, and MAB side capacitor.
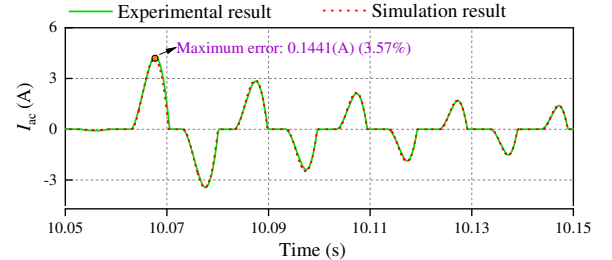

Fig. 13. Experimental and simulation results: AC current.

In Fig. 14, the comparisons of U_{trdc} and I_{trdc} in time-domain are given. To better compare the accuracy of the simulation models, the fast Fourier transform (FFT) results of experiment and simulation results are given as well. It is seen that the absolute errors between experiment and simulation at the fundamental frequency (1000 Hz) and odd harmonics (3000, 5000, 7000 Hz) are very small for both U_{trdc} and I_{trdc}. There are two reasons why the percentage current error at 5th and 7th harmonics are high. One is that some of the characteristics like parasitic parameters are ignored, which smooth the simulation current. The other is the base value is small so a very small absolute error can also lead to a large relative error. However, the dominating fundamental current is accurate enough to

reflect the dynamic of the current output and therefore, the two current curves match well.
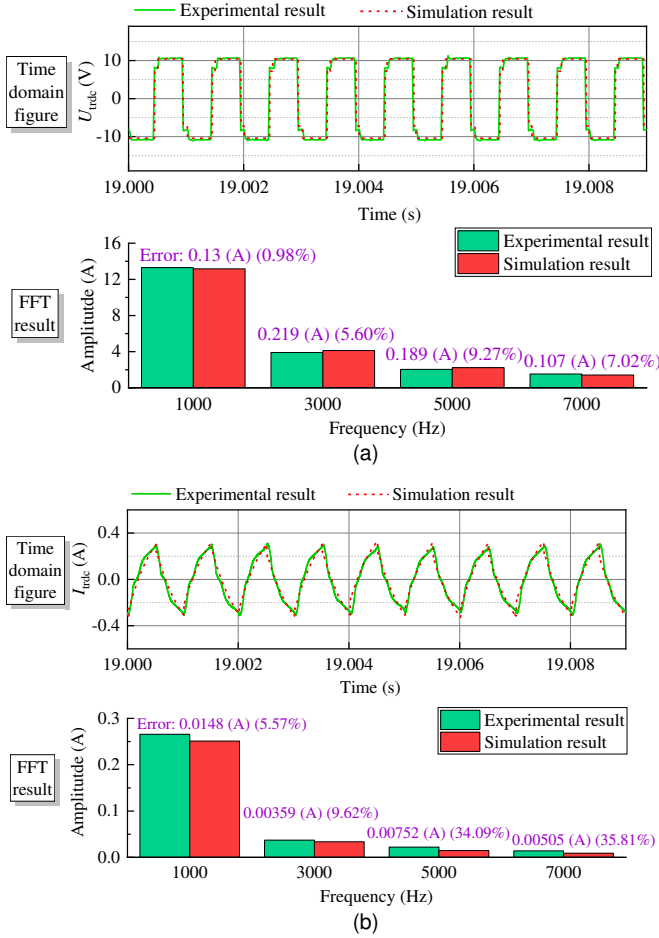

Fig. 14. Low-voltage side voltage and current: (a) voltage; (b) current.

The experimental results indicate that digital simulation is capable of reflecting the dynamics of the physical device. In the following section, the DM will be used as the benchmark to compare with the equivalent model (EM) to validate the proposed method further.

IV. SIMULATION VALIDATION

In PSCAD/EMTDC, the DM established by individual components and the EM proposed in this paper are compared in terms of accuracy and time efficiency.

A. Accuracy Test I: Individual XET-PET

First, the accuracy of individual XET-PET, as shown in Fig. 2, is tested. Parameters of XET-PET are listed in Table II. On the CHB side, the CPS-PWM is adopted to control the capacitor voltages. As for the MAB side, the SPS control is used to maintain the LVDC side capacitor voltages.

The working condition is set as follows:

1) **Startup**: in the first **0.3 s**, the PET is blocked to charge the CHB side capacitors. During **0.3 - 0.8 s**, the CHB side is de-blocked, and the CPS-PWM control is activated, then the CHB side capacitors start to be charged with a fixed ramp-up slope. After **0.8 s**, the SPS control acts to charge the MAB side capacitors. The system reaches a steady-state at t = **1.0 s**.

2) **LVDC fault**: at t = **1.5 s**, an LVDC fault occurs, and MABs are **blocked** at t = **1.502 s**. The fault is cleared at t = **1.6 s,** and the PET is de-blocked and restarts at t = **1.602 s**.

3) **MVDC fault**: At t = **2.0 s**, an MVDC fault occurs and the PET is blocked at t = **2.002 s**. The fault is cleared at t = **2.1 s**. the PET is de-blocked and re-starts at t = **2.102 s**.

TABLE II
SYSTEM PARAMETERS OF THE XET-PET

Symbols	Parameter Description	Values
M_{PM}	Number of PMs per arm	4
X_{ACtrPU}	AC Transformer's leakage inductance (p.u.)	0.15
f_{sys}	System fundamental frequency (Hz)	50
$V_{L-Lrated}$	Line-to-line RMS voltage on AC grid side (kV)	115
$V_{L-Lvalve}$	Line-to-line RMS voltage on valve side (kV)	10.5
S_{tr}	AC transformer's rated capacity (MVA)	2.5
$V_{C1Rated}$	Rated capacitor voltage in CHB side (kV)	5
$V_{o1Rated}$	MVDC rated output voltage (kV)	20
P_{oRated}	MVDC rated output real power (MW)	0.8
C_{CHB}	CHB side PM capacitance (μF)	1000
R_{load_CHB}	MVDC output load (Ω)	500
S_{tr_hf}	Rated capacity of high-frequency transformer (MVA)	0.1875
X_{hftrPU}	High-frequency Transformer's leakage inductance (p.u.)	0.188
V_{tr1}	High-frequency Transformer's CHB side voltage rating (kV)	5
V_{tr2}	High-frequency Transformer's MAB side voltage rating (kV)	0.75
C_{MAB}	MAB side PM capacitance (μF)	3500
$V_{o2Rated}$	LVDC rated output DC voltage (kV)	0.75
R_{load_MAB}	LVDC output load (Ω)	0.703

Fig. 15 to Fig. 17 show the converter-level dynamics. CHB capacitor voltage (the first capacitor in phase A) and LVDC capacitor voltage of the stages 1) – 3). The results show that EM agrees with DM well. The maximum relative error (MRE) is 2.99%, 4.20%, and 2.75% at t = 1.069 s, 1.643 s, and 2.583 s, respectively.
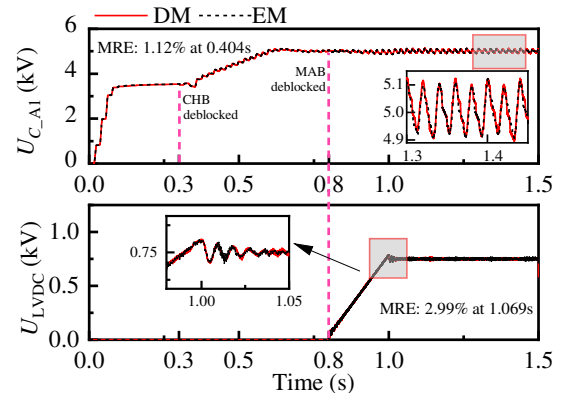

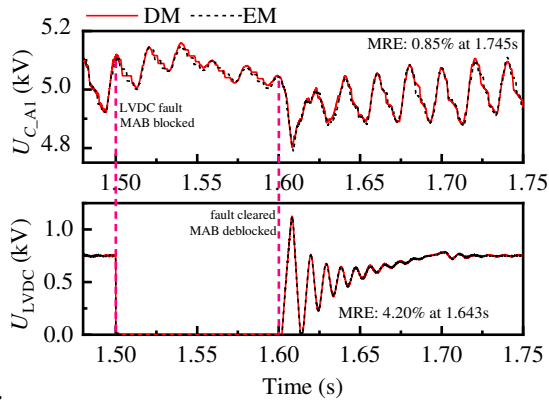Fig. 15. Startup capacitor waveforms.
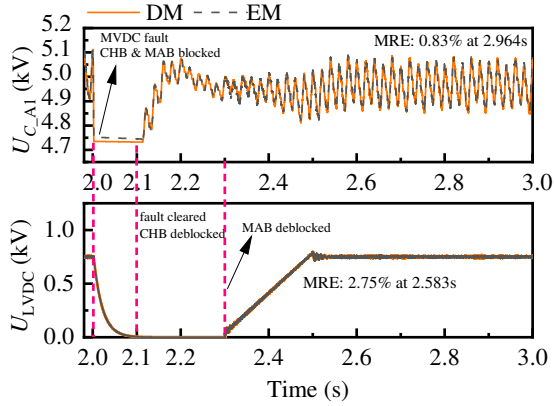
.

Fig. 16. LVDC fault capacitor waveforms.

Fig. 17. MVDC fault capacitor waveforms.

As for system-level dynamics, during **0 - 3.0 s**, the MVDC voltage and the output power of the MVDC and LVDC ports are shown in Fig. 18 and Fig. 19. It shows that the EM can reflect the transient and steady-state characteristics of DM very well.
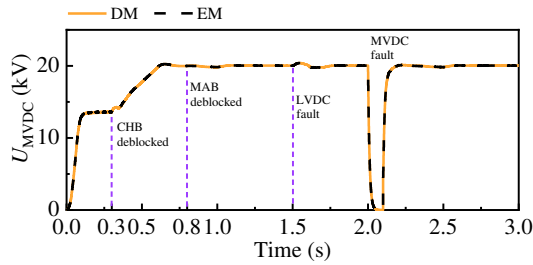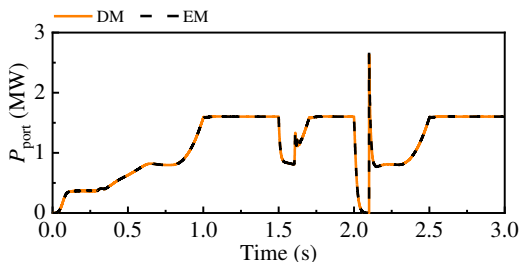

Fig. 18. Overall MVDC voltages.

Fig. 19. Overall sum power of MVDC and LVDC ports

Moreover, the voltages and currents under harmonic injecting, AC grid voltage sag/swell, and AC grid three-phase fault are tested. Fig. 20(a) shows the transients after injecting harmonics into the AC grid at t = 1.5 s. The 3rd, 5th, 7th and 9th harmonics are injected into the AC grid in amounts of 8%, 5%,

3% and 1%, respectively. In Fig. 20(b), the AC grid voltage U_{ac} swells 10% at t = 1.5 s, goes back to normal at t = 1.53 s and then sags 10% at t = 1.56 s. Fig. 20(c) shows that a three-phase short-circuit fault occurs at t = 1.5 s and the PET blocks at t = 1.505 s. It can be seen that the results of EM and DM agree well during the transient processes, indicating that the EM has the full ability to capture the dynamics of various transients.

(a)

(b)
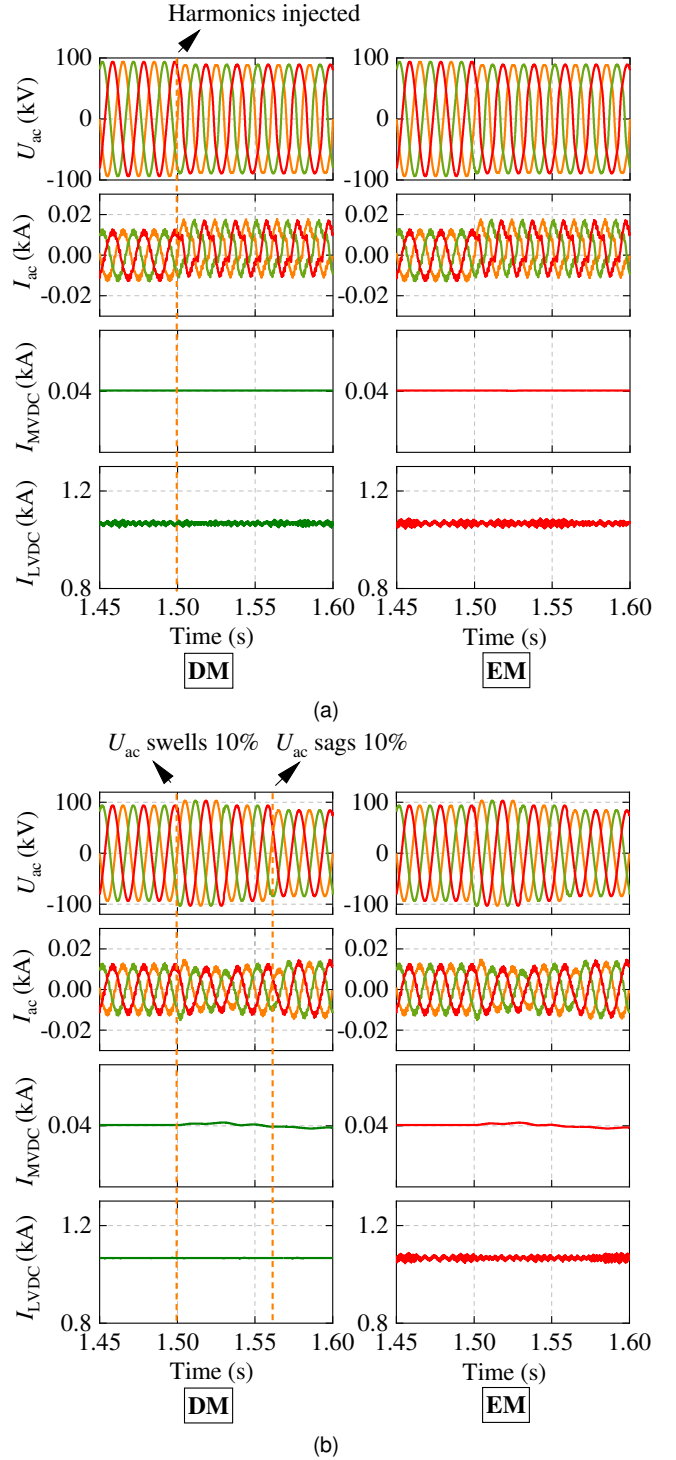
Fig. 20. Comparisons of DM and EM under various transients: (a) harmonic injecting; (b) Uac swells/sags; (c)three-phase short-circuit fault on AC grid.
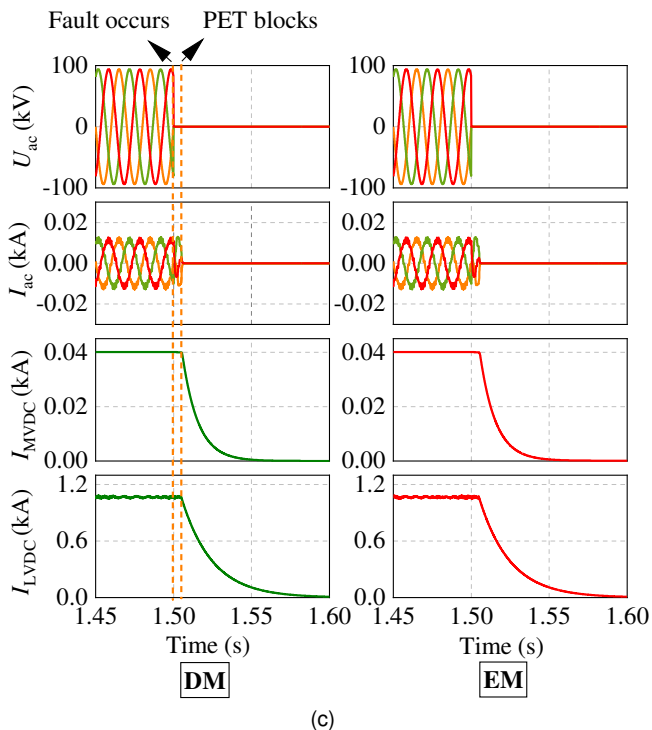
B. Accuracy Test II: Xiaoertai Distribution Network

The structure of the Xiaoertai distribution network is shown in Fig. 21. The XET-PET works as an energy router to connect PV station, supercapacitor bank and AC/DC loads. AC and DC voltage levels are marked in the figure. The power flow of the equipment in the network are shown in TABLE III, in which the positive values indicate the power is flowing out of the XET-PET and the negative values indicate the power is flowing into XET-PET. Fig. 21.

TABLE III
POWER FLOW IN XIAOERTAI DISTRIBUTION NETWORK

Equipment	Power flow
PV station	-0.3 MW
AC load	0.89 MW
DC load	0.28 MW
AC grid	-0.9 MW
XET-PET (10 kV MVAC port)	-0.9 MW
XET-PET (±10 kV MVDC port)	-0.28 MW
XET-PET (750 V LVDC port)	1.16 MW

Fig. 22(a) shows the dynamics of power redistribution when

AC load steps from 0.89 MW to 2.1 MW at t = 4.5s. Fig. 22(b) shows the results when AC grid frequency drops to 49.5 Hz at t = 4.5 s. It can be seen that the EM matches well with the DM during dynamics.

(a)

(b)

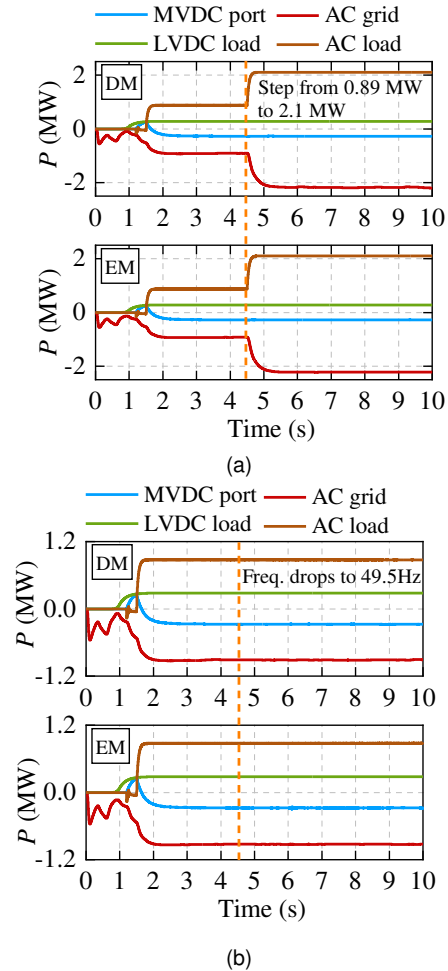Fig. 22. Simulation results when a disturbance occurs at t = 4.5 s: (a) AC load steps from 0.89 MW to 2.1 MW; (b) grid frequency drops to 49.5 Hz.

The simulation result leads to the result that the proposed model can precisely describe the dynamic characteristics of the external system in time-domain and therefore, it can capture system instabilities and reflect them through the changes of the electrical quantities of the system.
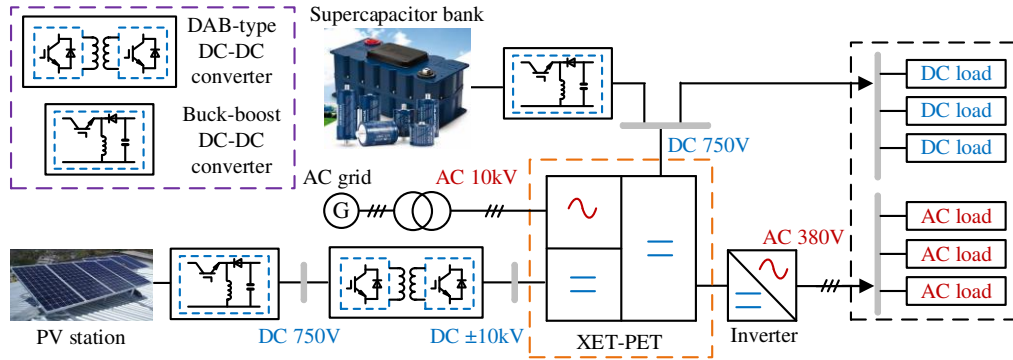
Fig.21. Xiaoertai distribution network.

C. Speedup Factor Test

The DM and EM of the XET-PET models with 4, 8, 10, 20, and 30 PMs per arm are established in PSCAD/EMTDC. The simulation time-step is set to 5 µs, and the duration is 1.5 s. The CPU is Intel(R) Core(TM) i9-10900K @ 3.70GHz. The CPU time is recorded by the PSCAD/EMTDC built-in function. The speedup factor and parallel factor is defined as:

$$F = \frac{t_{DM}}{t_{EM\_p}} , \quad F_p = \frac{t_{EM}}{t_{EM\_p}} \quad (23)$$

TABLE IV
SPEEDUP FACTOR TEST

| Number of PMs | CPU time (t_{DM}) | EM CPU time | | Speedup factor (F) | Parallel factor (F_p) |
		NOT paralleled (t_{EM})	Paralleled (t_{EM_p})		
4	302.97s	110.01 s	59.20 s	5.12	1.86
8	1800.01 s	185.84 s	83.00 s	21.69	2.24
10	2566.34 s	219.42 s	85.25 s	30.83	2.56
20	34068.77 s	408.09 s	129.78 s	262.51	3.14
30	116205.38 s	594.78 s	157.45 s	738.05	3.78

*OpenMP is used for parallelization

According to TABLE IV, the proposed modeling method is capable of realizing a remarkable simulation acceleration. From t_{DM} and t_{EM}, it is seen that the node elimination method increases the simulation speed by 116205.38/594.78=195.38 times when the PM number is 30. After employing parallel computing, the simulation is further accelerated by about 4 times, resulting in a speedup factor of 738.05.

The performance of the CPU model is also a factor that influences the simulation speed. In the same simulation configuration, the speedup and parallel factors of the proposed method are evaluated under the following 4 CPU models.

1) **Model 1**: Intel® Core™ i9-9900K @3.7GHz 3.7GHz(10 cores).

2) **Model 2**: **Intel**® Xeon™ E5-2670 v2 @2.5GHz 2.5GHz (Dual Processor) (20 cores).

3) **Model 3**: Intel® Core™ i7-10710U @1.1GHz 1.61GHz (6 cores).

4) **Model 4**: Intel® Core™ i7-7700HQ @2.8GHz 2.8GHz (4 cores).

From Fig. 23, an obvious speedup is achieved with the proposed method under all 4 CPU models. The speedup

factors range from 3 to 5, as the orange columns show. The parallel factor is 1 to 2 times, as the blue columns show. The speedup capability and the acceleration effectiveness using the parallelization are related to the number of cores. However, although some multi-core processors have a high speedup factor, their overall performance is not obvious. Consequently, its simulation time is still long after speedup, as shown in Model 2, where the speedup factor is 4.81 but the simulation time of EM is still up to 131.41 s. Fig. 23 proves that the proposed model is applicable on various CPU models, and is able to effectively accelerate the simulation speed.
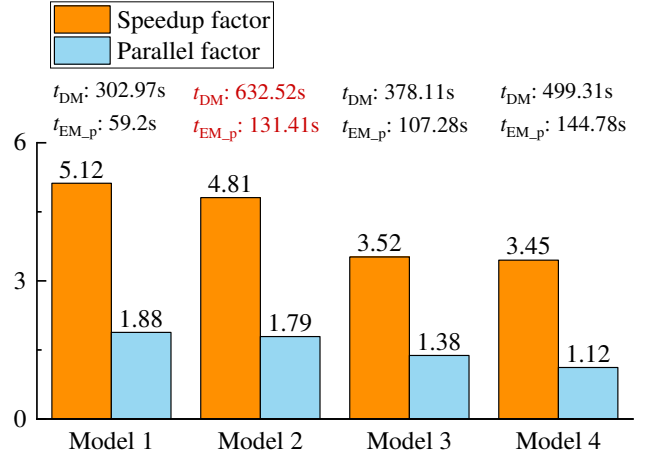
Fig. 23. Comparisons of the speedup factor under different CPU models.

Compared with the detailed model, the proposed model is significantly accelerated, due to the two main reasons:

1) The internal nodes are eliminated in the proposed model. For the XET-PET, the number of nodes is $17N+5$ (N is the number of PMs) per arm in the detailed model. But in the proposed model, the node number is always 14. The computational burden is therefore remarkably reduced.

2) Parallelization is employed in the proposed model to fully exploit the performance of multi-core CPU to improve the calculation speed.

At last, the performance of the proposed equivalent model (EM) is compared with the detailed model (DM), averaged value model (AVM) [9] and high-speed equivalent model (HEM) [15] in terms of system-level and internal accuracy, speedup capability and applicability, as shown in TABLE V.

TABLE V
COMPARISON WITH DM, AVM AND HEM

Items	DM	AVM	HEM	EM
System-level accuracy	★★★★★	★★★☆☆	★★★★★	★★★★★
Internal accuracy	★★★★★	☆☆☆☆☆	★★★☆☆	★★★★★
Speedup capability	☆☆☆☆☆	★★★★★	★★★★☆	★★★★☆
Applicability	★★★★★	★★☆☆☆	★★★★★	★★★★★

*More stars (★) indicate better performance.

As the benchmark model, the DM is accurate and applicable in various situations, but the simulation speed is very slow. AVM is fast but sacrifices accuracy, and it is inapplicable during fast transients because high-frequency responses are lost. HEM and EM balance the simulation speed and accuracy, and they are applicable in modeling MMC, PET and other modularized topologies. However, some of the internal dynamics of HEM are not accurate because the circuit is decoupled with a one-step approximation in the transformer equivalent algorithm. EM has high external and internal accuracy because its circuit is not decoupled. The drawback of its coupling circuit is low efficiency. However, this issue is improved by parallel computing.

V. CONCLUSION

In this paper, a modeling method using parallel computing is proposed for complex modular power electronic transformers. In the proposed method, a four-winding UMEC transformer model is derived and employed in the XET-PET. The order of the nodal admittance matrix is reduced using the node elimination algorithm to construct the PM equivalent. Taking the advantage of the particular pattern of Y_{EQ} and J_{EQ}, the equivalent method of the bridge arm is improved to avoid matrix calculation, which is beneficial to reduce the simulation time further. The blocking state circuit is integrated into the normal operating circuit without involving an additional circuit. Throughout the modeling process, the individual calculations are parallelized to remarkably accelerate the simulation speed.

Hardware experiment demonstrates that the DM is sufficient to reflect the dynamics of physical devices. Then DM and EM are established in PSCAD/EMTDC to test the accuracy under the startup, steady-state, and fault operation conditions. A distribution network of XET-PET is also established to test the performance of the proposed model in an area network. The simulation results show that the proposed modeling method is sufficiently accurate, with a maximum relative error under 4.2%. The speedup factor test shows that the proposed method can accelerate the simulation by 2 orders of magnitude. Parallelization contributes to the simulation acceleration by 2 to 4 times.

However, there are certain limitations of the proposed model as well. The voltages and currents of eliminated nodes cannot be measured directly. It requires an inverse solution step with (11). Additionally, the three-phase diode H-bridge cannot be simplified together with the arm equivalent circuit.

Model developers must use the embedded diode component of the simulation tools to deal with blocking state situations.

As the proposed method reduces the computational burden and properly designs the paralleled structure of the model, it is independent of the platform or simulation pattern. Therefore, it is suitable for large-scale system-level EMT simulations and can be applied in real-time simulations. Also, the proposed method is designed for modularized topologies. It is applicable for other configurations like CHB-PET and MMC as well.

REFERENCES

[1] G. Zhang, J. Chen, B. Zhang, and Y. Zhang, "A critical topology review of power electronic transformers: In view of efficiency," *Chinese Journal of Electrical Engineering*, vol. 4, no. 2, pp. 90-95, June 2018.

[2] F. An, B. Zhao, J. Wang, B. Cui, Q. Song and T. Xiong, "An Adaptive Control Method of DC Transformers Imitating AC Transformers for Flexible DC Distribution Application," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020, pp. 332-337.

[3] M. Feng, C. Gao, J. Ding, H. Ding, J. Xu and C. Zhao, "Hierarchical Modeling Scheme for High-Speed Electromagnetic Transient Simulations of Power Electronic Transformers," *IEEE Trans. Power Electron.*, vol. 36, no. 9, pp. 9994-10004, Sept. 2021.

[4] Shaodi Ouyang, J. Liu, X. Wang, X. Wang, Fei Meng and J. Riffat, "The average model of a three-phase three-stage Power Electronic Transformer," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), Hiroshima*, 2014, pp. 2815-2820.

[5] J. Xu, Y. Zhao, C. Zhao and H. Ding, "Unified High-Speed EMT Equivalent and Implementation Method of MMCs With Single-Port Submodules," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 42-52, Feb. 2019.

[6] A. R. Sadat and H. S. Krishnamoorthy, "Fault-Tolerant ISOSP Solid-State Transformer for MVDC Distribution," *IEEE Journal of Emerg. and Sel. Topics in Power Electron.* (Early Access)

[7] Q. Ye, R. Mo and H. Li, "Impedance Modeling and DC Bus Voltage Stability Assessment of a Solid-State-Transformer-Enabled Hybrid AC–DC Grid Considering Bidirectional Power Flow," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6531-6540, Aug. 2020.

[8] F. Shi, D. Shu, Z. Yan and Z. Song, "A Shifted Frequency Impedance Model of Doubly Fed Induction Generator (DFIG)-Based Wind Farms and Its Applications on S^2SI Analysis," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 215-227, Jan. 2021.

[9] M. T. A. Khan, A. A. Milani, A. Chakrabortty and I. Husain, "Dynamic Modeling and Feasibility Analysis of a Solid-State Transformer-Based Power Distribution System," *IEEE Trans. Ind. Appl.*, vol. 54, no. 1, pp. 551-562, Jan.-Feb. 2018.

[10] M. A. Rahman, M. R. Islam, K. M. Muttaqi and D. Sutanto, "Modeling and Control of SiC-Based High-Frequency Magnetic Linked Converter for Next Generation Solid State Transformers," *IEEE Trans. Energy Convers.*, vol. 35, no. 1, pp. 549-559, March 2020.

[11] K. Strunz and E. Carlson, "Nested Fast and Simultaneous Solution for Time-Domain Simulation of Integrative Power-Electric and Electronic Systems," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 277-287, Jan. 2007.

[12] U. N. Gnanarathna, A. M. Gole and R. P. Jayasinghe, "Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 316-324, Jan. 2011.

[13] J. Xu, S. Fan, C. Zhao and A. M. Gole, "High-Speed EMT Modeling of MMCs With Arbitrary Multiport Submodule Structures Using Generalized Norton Equivalents," *IEEE Trans. Power Del.*, vol. 33, no. 3, pp. 1299-1307, June 2018.

[14] C. Gao, M Feng, J. Ding, et al., "Accelerated Electromagnetic Transient (EMT) Equivalent Model of Solid-State Transformer," *IEEE Journal of Emerg. and Sel. Topics in Power Electron.* (Early Access)

[15] J. Xu, C. Gao, J. Ding, "High-Speed Electromagnetic Transient (EMT) Equivalent Modelling of Power Electronic Transformers," *IEEE Trans. Power Del.*, vol. 36, no. 2, pp. 975-986, April 2021.

[16] L. F. Costa, G. Buticchi and M. Liserre, "Optimum Design of a Multiple-Active-Bridge DC–DC Converter for Smart Transformer,"

IEEE Trans. Power Electron., vol. 33, no. 12, pp. 10112-10121, Dec. 2018.

[17] L. Qing, Z. Shihe and S. Shuai, "Study of DC bias of power transformer based on UMEC model," *2015 7th Asia-Pacific Conference on Environmental Electromagnetics (CEEM)*, Hangzhou, China, pp. 65-68, 2015.

[18] X. Li, J. Wu, C. Ye, et al., "Transformer model with hysteresis characteristic for electromagnetic transients based on PSCAD/EMTDC," *2015 5th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT)*, Changsha, China, pp. 1689-1694, 2015.

[19] J. Xu, Fast Electromagnetic Transient Simulation Methods and Prospects of High-frequency Isolated Power Electronics Transformers, CIGRE ELECTRA, no. 316, pp. 29-35, June 2021. [Online] Available: https://electra.cigre.org/316-june-2021/technology-e2e/fast-electromagnetic-transient-simulation-methods-and-prospects-of-high-frequency-isolated-power-electronics-transformers.html.

[20] F. An, B. Zhao, J. Wang, et al., "An adaptive control method of DC transformers imitating AC transformers for flexible DC distribution application," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA*, 2020, pp. 332-337.

[21] A. M. Gole, *et al.*, "Guidelines for modeling power electronics in electric power engineering applications," *IEEE Trans. Power Del.* vol. 12, no. 1, pp. 505-514, Jan. 1997.

[22] J. A. Martinez and B. A. Mork, "Transformer modeling for low- and mid-frequency transients - a review," *IEEE Trans. Power Del.*, vol. 20, no. 2, pp. 1625-1632, April 2005.

[23] X. Chen, "Negative inductance and numerical instability of the saturable transformer component in EMTP," *IEEE Trans. Power Del.*, vol. 15, no. 4, pp. 1199–1204, Oct. 2000.

[24] J. Arrillaga, W. Enright, N. R. Watson, and A. R. Wood, "Improved simulation of HVDC converter transformers in electromagnetic transient programs," *in Proc. Inst. Elect. Eng., Gen. Transm. Distrib.*, vol. 144, Mar.1997, pp. 100–106.

[25] N. Watson and J. Arrillaga. "Power systems electromagnetic transients simulation," *Institution of Engineering & Technology*, London, UK, p.448, (2003).

[26] Mahmood, Lynch and Philipp, "A fast banded matrix inversion using connectivity of Schur's complements," *IEEE 1991 International Conference on Systems Engineering*, Dayton, OH, USA, pp. 303-306, 1991.

[27] J. Xu, C. Zhao, Z. He and Y. Guo, "Start-up control and DC fault ride-through strategies of a hybrid MMC-HVDC system suitable for overhead line transmission," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, *Taipei, Taiwan*, 2015, pp. 1-6.

Moke Feng was born in Suining City, Sichuan Province, China. He received the B.Eng. degree in Electrical Engineering and Its Automation from North China Electric Power University, Beijing, China, in 2017.

He is currently pursuing the Ph.D degree in Electriacal Engineering in the State Key Laboratory Of Alternate Electrical Power System with Renewable Energy Resources, North China Electric Power University (NCEPU), Beijing, China. His research interests include the modeling of the key equipment in distribution network and HVDC transmission system.

Chenxiang Gao was born in Shanxi, China. He received the B.S. degrees in Electrical Engineering and Its Automation from North China Electric Power University (NCEPU) in 2019.

Currently, he is working towards the Master degree in Electrical Engineering with NCEPU. His research interests include the electromagnetic transient (EMT) equivalent modelling of MMC-HVDC and solid-state transformers (SST) in DC Grid.

Jianzhong Xu (M'14-SM'19) was born in Shanxi, China. He received the B.S. and Ph.D. degrees in Electrical Engineering from North China Electric Power University (NCEPU) in 2009 and 2014 respectively.

Currently, he is an Associate Professor and Ph.D. Supervisor of the State Key Laboratory Of Alternate Electrical Power System with Renewable Energy Resources, North China Electric Power University (NCEPU), China, where he obtained his Ph.D. degree in 2014. From 2012 to 2013 and 2016 to 2017, he was a Visiting Ph.D. student and Post-Doctoral Fellow at the Uni-versity of Manitoba, Canada. He is an Associate Editor of the CSEE Journal of Power and Energy Systems. He is now working on the Electromagnetic Transient (EMT) equivalent modelling, fault analysis and protection of HVDC Grids.

He has published 24 IEEE Transaction/Journal papers and 4 of them are 'Scopus Top 1% highly cited paper'. He also serves as reviewers of 10 IEEE/IET journals and 9 Chinese journals.

Chengyong Zhao (M'05-SM'15) was born in Zhejiang, China. He received the B.S., M.S. and Ph.D. degrees in Power System and Its Automation from NCEPU in 1988, 1993 and 2001, respectively.

He was a Visiting Professor at the University of Manitoba from Jan. 2013 to Apr. 2013 and Sep. 2016 to Oct. 2016. Currently, he is a professor at the School of Electrical and Electronic Engineering, NCEPU. His research interests include HVDC system and DC grid.

Gen Li (M'18) received the B.Eng. degree in Electrical Engineering from Northeast Electric Power University, Jilin, China, in 2011, the M.Sc. degree in Power Engineering from Nanyang Technological University, Singapore, in 2013 and the Ph.D. degree in Electrical Engineering from Cardiff University, Cardiff, U.K., in 2018.

From 2013 to 2016, he was a Marie Curie Early Stage Research Fellow funded by the European Commission's MEDOW project. He has been a Visiting Researcher at China Electric Power Research Institute and Global Energy Interconnection Research Institute, Beijing, China, at Elia, Brussels, Belgium and at Toshiba International (Europe), London, U.K. He has been a Research Associate at the School of Engineering, Cardiff University since 2017. His research interests include control and protection of HVDC and MVDC technologies, power electronics, reliability modelling and evaluation of power electronics systems.

Dr. Li is a Chartered Engineer in the U.K. He is an Associate Editor of the CSEE Journal of Power and Energy Systems. He is an Editorial Board Member of CIGRE ELECTRA. He is an IET Professional Registration Advisor. His Ph.D. thesis received the First CIGRE Thesis Award in 2018. He is the Vice-Chair of IEEE PES Young Professionals and the Technical Panel Sectary of CIGRE UK B5 Protection and Automation.