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GaN HEMT Based Technology Development for Millimetre Wave Applications

by

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ABSTRACT

High Electron Mobility Transistors (HEMTs) based on Gallium Nitride (GaN) and grown on Silicon (Si) substrates are emerging as one of the most promising candidates for high-power, switching-speed, low-losses, cost-effectiveness, and high-frequency Integrated Circuits (ICs) applications operating at microwave and millimetre frequencies (3-300 GHz). As silicon approaches its theoretically expected limitations, enhancements in energy efficiency of silicon power electronics are becoming less significant. Due to a unique combination of features that offer higher power density per unit area, compared to Si, GaN transistors are alternatives for the next generation of power electronics. Because GaN can be processed on current Si process lines employing GaN-on-Si heteroepitaxy, the industrial shift to GaN is also cost effective.

In GaN HEMTs devices, the mesa structure is a three-dimensional device structure that is conventionally created by traditional dry etching methods applied to establish device-isolation used for GaN-based transistor technologies. As a result, this leads to significant leakage currents which have an immense influence on the device's noise performance and breakdown voltages. In this thesis, a novel technique designed to establish a device-isolation in GaN HEMTs is proposed to overcome mesa etch concerns such as sidewall profile, common gate discontinuity and gate leakage originated from a gate direct contact with two-dimensional electron gas (2DEG). The proposed method requires a miniature extension of the mesa to deposit the gate-feed to ensure a fully planar gate formation. As a result, this reduced the gate leakage by an order of magnitude. However, since the gate-feed is situated on an active layer with a very low resistance due to a relatively larger length in comparison with the actual gate, the gate became conductive above pinch-off point and gate leakage increased. Consequently, a dielectric is deposited below the gate-feed to counter the arising problem which led to an increase in the drain leakage at the off-state due to a substantial dielectric thickness. This can be prevented using methods such as atomic layer deposition for a denser yet a shallower (a few nm) dielectric

deposition below the gate feed. Finally, the proposed structure will allow a deeper etch of the active layer for heat management purposes while keeping the integrity of the gate metal intact. Leakage currents reduction of unity A/mm were attained, which are equivalent to those obtained using the more sophisticated and costly ion implantation process. Additionally, a small-signal-model was developed to evaluate the behavior of the GaN HEMT devices with respect to the high frequency operation and the parasitic associated with it. The process began with the extraction of the extrinsic elements using various methods followed by the extraction of the intrinsic parameters.

Finally, novel GaN Schottky barrier diodes (SBDs) with multi-channel trenches positioned below the anodes to reduce the turn-on voltage caused by the reduction of the diode barrier height due to the direct contact to the 2DEG. To compete with existing III-V technologies, GaN-based SBDs with low reverse-current leakage (I_S), low onset voltage (V_{ON}), high switching speed (R_{ON}), high reverse-breakdown (V_B) voltage, and high cutoff frequency (f_c) are mainly essential to be considered. Conventional GaN-based SBD DC and RF performance, when fabricated using LR-Si substrates, is still constrained by their significant V_{ON}, RF leakage, and switching losses. Methods such as recessed anode, dual-channel field-effect rectifier, regrowth cathodes, and dual-filed plates have been employed to suppress these problems. In this work, a cost-effective RF AlGaN/GaN SBDs on LR-Si structure is developed utilizing the technique of multi-channel and trenches below anodes, which is completely compatible with III-V THz monolithic integrated circuit (THz-MIC) technology. The newly designed devices outperformed traditional SBDs in terms of switching loss, turn-on characteristics, ideality factor (η_n), and cutoff frequency, with R_{ON} = 0.97 Ω.mm, V_{ON} = 0.84 V, V_B > 30V, η_n = 1.69, and f_c = 600 GHz. These outcomes are attributed to the direct contact acquired between the Schottky anode and the 2DEG channel occurring at the sidewalls of the trenches due to multi-mesa, as well as the precise design geometries utilized to limit substrate coupling effects.

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أولا, الحمد والشكر والثناء **لله الرحمن الرحيم الملك القدوس السلام المؤمن المهيمن العزيز الجبار المتكبر الخالق البارئ المصور الغفار القهار الوهاب الرزاق الفتاح العليم القابض الباسط الخافض الرافع المعز المذل السميع البصير الحكم العدل اللطيف الخبير الحليم العظيم الغفور الشكور العلي الكبير الحفيظ المُقيت الحسيب الجليل الكريم الرقيب المجيب الواسع الحكيم الودود المجيد الباعث الشهيد الحق الوكيل القوي المتين الولي الحميد المحصي المبدئ المعيد المحي المميت الحي القيوم الواجد الماجد الواحد الصمد القادر المقتدر المقدم المؤخر الأول الاخر الظاهر الباطن الوالي المتعالي البر التواب المنتقم العفو الرؤوف مالك الملك ذو الجلال والاكرام المقسط الجامع الغني المغني المانع الضار النافع النور الهادي البديع الباقي الوارث الرشيد الصبور**. فالفضل يعود له وحده من قبل ومن بعد. والصلاة والسلام على خاتم النبيين.

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PUBLICATIONS

Journal articles:

- **M. Alathbah**, and K. Elgaid, “Miniature Mesa Extension for a Planar Submicron Gate Formation,” *IEEE Electron Device Lett.*, accepted with minor revision (ID: EDL-2022-03-0363).

- A. Eblabla, X. Li, **M. Alathbah**, Z. Wu, J. Lees, and K. Elgaid, “Multi-Channel AlGaN/GaN Lateral Schottky Barrier Diodes on Low-Resistivity Silicon for Sub-THz Integrated Circuits Applications,” *IEEE Electron Device Lett.*, vol. 40, no. 6, pp. 878–880, 2019, Doi: 10.1109/LED.2019.2912910.

Conference papers:

- **M. Alathbah**, A. Eblabla and K. Elgaid, "Frequency Doubler Based on a Lateral Multi-Channel GaN Schottky Barrier Diode for 5G Technology," *2020 13th International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM)*, Smolenice, Slovakia, 2020, pp. 14-18, Doi: 10.1109/ASDAM50306.2020.9393861.

- **M. Alathbah**, A. Eblabla and K. Elgaid, "Novel Slotted mmWave CPW Branch Line Coupler for MMIC and Sub-THz Applications," *2020 13th International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM)*, Smolenice, Slovakia, 2020, pp. 111-114, Doi: 10.1109/ASDAM50306.2020.9393863.

- A. Eblabla, **M. Alathbah**, Z. Wu, J. Lees and K. Elgaid, "Membrane Supported GaN CPW Structures for High-frequency and High-power Applications," *2019 IEEE Asia-Pacific Microwave Conference (APMC)*, Singapore, Singapore, 2019, pp. 1179-1181, Doi: 10.1109/APMC46564.2019.9038731.

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1. INTRODUCTION

In this chapter, an overview of the gallium nitride (GaN) HEMT based technology with the justification of this project and its application was given. Previous state-of-the-art AlGaN/GaN devices were provided as well. Finally, a summary and the main objectives of this project were also mentioned.

1.1. GaN Technology: An Overview

Since the invention of the first solid state transistor in the mid of the last century, silicon has been exclusively the prime semiconductor for electronic devices. However, recently, silicon has reached its maximum practical and theoretical capabilities, especially in high power and high frequency applications. Therefore, with these limitations posed by silicon, alternatives are needed to meet the market demand of technological advancement in semiconductor industry. This has led to the shift of interest toward material with wide bandgap of III-V technologies such as gallium arsenide (GaAs), gallium nitride (GaN), and indium phosphide (InP), which allowed the application of high electron mobility transistor (HEMT) to emerge. III-V based HEMTs exhibited high electron mobility, due to inherit characteristic of current transport via majority carries as supposed to minority carries in silicon, which translated to operation at a smaller wavelength and higher frequency. On the other hand, wider bandgap has led to higher output power and more power density allowing for smaller size circuit with better performance. GaN is the most attractive among the III-V group and it is a direct bandgap with a band energy of 3.4 eV, which categorises it to be a wide-bandgap, WBG, material ($2.0 < WBG < 4.0$ eV [1]). Although GaN emerged around 1930, a synthesis done by Johnson et al., [2], the first GaN-based transistor fabricated on sapphire substrate, was only demonstrated in 1993 by Khan et al. as detailed in [3]. Due to GaN's superior electrical properties such as electron velocity, energy gap, breakdown electric field and power density, GaN is emerging as the future semiconductor replacing silicon in electronics.

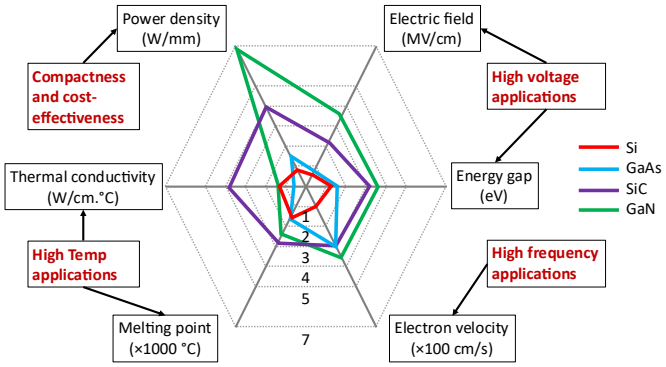


Figure 1.1. Summary of GaN against Si, GaAs and SiC properties with the corresponding advantages and applications

GaN material as illustrated in **Figure 1.1**, surpasses the other semiconductors in most features. For example, GaN offers a power density about 7 W/mm whereas, GaAs and Si demonstrate a power density less than 2 and 1 W/mm, respectively. Hence, GaN is considerably compact and can be fabricated in smaller size/volume resulting in lower system and operation costs (efficiency). **Table 1.2** summarizes the properties and characteristics of widely used semiconductors with GaN.

Table 1.1. Physical parameters comparison of epitaxial GaN layers in comparison with other materials at 300 K [4], [5]

↓ Parameter / Material →	Si	GaAs	SiC	GaN
Bandgap (eV)	1.1	1.4	3.2	3.4
Dielectric constant	11.8	10.9-12.9	6.7-9.7	5.3-9.5
Breakdown electric field (kV/cm)	300	500	2200	3300
Saturation velocity (km/sec)	100	200	200	270
Electron mobility ($cm^2/V{\cdot}sec$)	1500	8500	370	1500
Thermal conductivity (W/cm·°C)	1.3	0.5	3.7	1.3
Melting point (°C)	1400	1240	2700	2500
Power density (W/mm)	0.8	1.5	4.0	7.0

Beyond particular material attributes, multiple figures of merit (FOM) metrics have been developed to compare the merit of various semiconductor materials for a given application, with the greater the figure of merit evaluation acquired, the better the performance. These figures of merit integrate the most important

material attributes for high-power and high-frequency applications into a single value that approximates the relative strengths of competing materials. Johnson's Figure of Merit (JFOM), which can be computed using Eq.(1.1) and offers a notion of material compatibility for high-power applications at high frequencies, is one of the most often utilized ones [6].

$$JFOM = \frac{E_c v_{sat}}{2\pi} \tag{1.1}$$

where, v_{sat} is the saturation velocity and E_c is the critical electric field.

For power switching devices where the operating frequency is relatively low, conduction losses become the dominating effect on the FET performance. Baliga's figure of merit (BFOM) is computed to estimate the performance using the following expression [7]:

$$BFOM = \varepsilon_r \mu_e {E_c}^3 \tag{1.2}$$

Where, μ_e is the electron mobility and ε_r is the dielectric constant of the material. However, at high frequency where switching losses become dominate, Baliga's figure of merit can be rewritten as [7]:

$$BHFFOM = \frac{\mu_e {E_c}^2 \sqrt{V_g}}{2{V_B}^{3/2}} \tag{1.3}$$

where, V_B is the breakdown voltage of the device and V_g is the gate voltage bias.

Another important indicator used to characterise material as an ideal switch is ratio between high breakdown voltage and low specific on-resistance (R_{on}). This is known as the power-device-figure-of-merit (FOM) [8], and it is equal to the ratio of the square of breakdown voltage by the specific on-resistance as given in Eq. (1.4). As a result, a trade-off is established between the off and on states of a given ideal switch, where the off-condition requires a high breakdown voltage to block reverse current and the on-state must have as low R_{on} as possible in order to minimise the switching losses as depicted in **Figure 1.2**.(a).

$$FOM = \frac{{V_B}^2}{R_{on}} \tag{1.4}$$

Therefore, it is manifested that the intrinsic limit of power semiconductor is defined by FOM. GaN devices, whether vertical or lateral, outperform their counterpart fabricated with Si and SiC. Additionally, FOM is mainly determined by the doping profile of a material including GaN-based vertical devices. However, in GaN lateral devices where two-dimensional-gas is responsible for current transport that stems from the AlGaN/GaN heterojunction, $Al_xGa_{(1-x)}N$ barrier layer structure and its aluminum composition (x) are the sole techniques, currently utilized to influence their FOM and the trade-off between V_B and R_{on} [9].

It is also instructive to plot and observe the changes in power density of GaN material as a function of the operational frequency, which is an inversely proportional type of relation as demonstrated in **Figure 1.2**.(b), in order to compare it with other materials as a key performance parameter used in measuring the compactness and cost-effectiveness of a material. Theoretically, it is evident from **Figure 1.2**.(b) that GaN material is far superior in power density capabilities in comparison with Si and GaAs and better than SiC by more than a half order of magnitude.

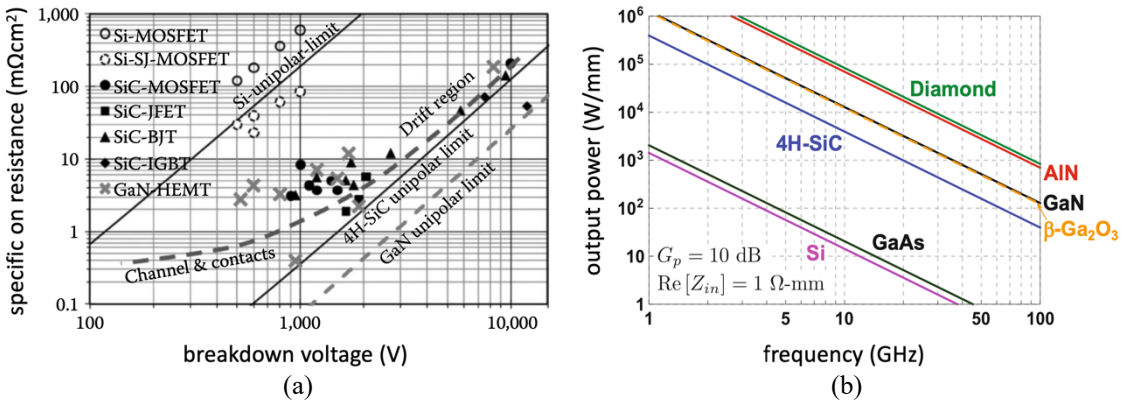


Figure 1.2. Specific on resistance as a function of breakdown voltage (a) and output power density as a function of frequency (b) for various materials, [4], [10], respectively

Another important FOM is Keyes, which is related to the maximum thermal capabilities of the device originating from the transistor being in a switching mode and it is evaluated as [7]:

$$KFOM = \lambda \sqrt{\frac{c v_{sat}}{4\pi\varepsilon_r}} \tag{1.5}$$

where c is the speed of light ($\approx 3 \times 10^8\, meter/second$) and λ is the material thermal conductivity.

Ultimately, to combine the overall effects of high power, high frequency and high temperature, a combined figure of merit (CFOM) is developed to account for them at the same time; and it is computed using the following equation [8]:

$$CFOM = \lambda \varepsilon_r \mu v_{sat} {E_c}^2 \tag{1.6}$$

Table 1.2 compares different materials about their FOMs. Clearly, GaN supersedes Si and GaAs on all fronts. However, better thermal performance is observed from SiC in comparison with GaN. This is manifested in the KFOM with more than double of the evaluation obtained from SiC (4.7) and 1.4 for GaN. It is worth noting that GaN is exceptionally superior, due to its high breakdown voltage and extremely low R_{on} and that is manifested by the evaluation of FOM where GaN is exhibiting a value of 3000 which is almost more than 5 times that of the SiC material.

Table 1.2. Various figures of merits for different material in comparison with GaN

↓ FOMs / Material →	Si	GaAs	SiC	GaN
*JFOM	1.0	2.7	215	480
*BFOM	1.0	12	7-13	17-35
*FOM	1.0	20	675	3000
*BHFFOM	1.0	11	45	80-172
*KFOM	1.0	0.4	4.7	1.4
*CFOM	1.0	4	300	220

*Normalised to the corresponding Si figures of merits

1.2. History of GaN Technology Advancement

During the early decades of the last century, Johnson et al. synthesised gallium nitride by pumping ammonia gas through metallic gallium at high temperatures between 900-1000°C [11]. Juza and Hahn created GaN in 1938 by passing ammonia (NH_3) over liquid gallium at high temperatures [12]. The powder produced by this approach was made up of tiny needles and platelets. Their goal was to learn more about GaN crystal structure and lattice constant. The first large area GaN epitaxially grew on sapphire substrates using Hydride Vapor Phase Epitaxy (HVPE) was demonstrated only in 1968 [12]. Following that discovery, GaN technology advanced rapidly, culminating in the discovery of two-dimensional electron gas (2DEG) production at an AlGaN/GaN heterojunction formed by metal organic chemical vapor deposition (MOCVD) on sapphire by Khan et al. in 1991. Khan et al. announced the first GaN metal semiconductor field effect transistor (MESFET) and heterostructure field effect transistor (HFET) produced on sapphire substrates using metal organic chemical vapor deposition (MOCVD) in 1993 and 1994, respectively [13]. Since Khan's discovery in 1994, great strides have been achieved in the advancement of GaN technology. Kaiser et al. successfully transferred AlGaN/GaN HEMT technology onto silicon substrates in 2000 by constructing the heterostructure using Metal Organic Chemical Vapor Deposition (MOCVD). Finally, Tripathy et al. reported the epitaxial development, characterisation, and device properties of crack-free AlGaN/GaN heterostructures on a 200mm (8 inch) diameter Si (111) substrate in 2012, which was a significant step forward in GaN technology within the last decade [14].

1.3. GaN Future Forecast

Due to the intrinsic capability of GaN technology which enables the integration and fabrication of both power-level components and signal-level devices on the same wafer, it will possibly, as a result, affect power conversion system in future implementation leading to a considerable enhancement in performance [15]. This is triggered by the absence or minimal parasitic interaction between the different devices that are fabricated on the same substrate when using GaN technology

[16], making GaN material a potential candidate for replacing silicon in the semiconductor market in the foreseeable future. In fact, in the year of 2020, the overall GaN market size (including both semiconductor segments of power and optoelectronic) was approximated to be more than $1.65 billion ($ = US dollar) despite the worldwide lockdown measures taken in an effort to control and slowdown the spread of Covid-19 pandemic (coronavirus) that had erupted in December, 2019 [17].

According to the Lyon, a market research and strategy consulting firm *Yole Developpement* based in France, the current market of GaN power semiconductors reached $740 million by the end of 2019. The phenomenal growth rate of approximately 10 to 20% year-on-year is expected for the following years. The forecasted revenue for GaN power semiconductors is $2 billion by the end of 2025 at a compound annual growth rate (CAGR) of 12%. Lyon also claims that with the support of governments heavily investment, military will begin to adopt GaN power devices in their applications replacing the travelling wave tube (TWT) to enhance national security, generating a revenue of around $1.1 billion by 2025 as shown in **Figure 1.3**.(a). The bubbles represent the main market for different sectors for GaN technology, whilst the bubble size is related to the corresponding market share of each sector. Apart from power semiconductors, GaN is predominantly used in optoelectronics for LEDs and laser diodes. Also, in telecommunication, which is the second largest sector predicted to generate more than $700 million in 2025 at a CAGR of 15%, the deployment of GaN is inevitable especially in active antenna systems (AAS) for bandwidth increase and in backhaul connections. Consequently, the total GaN semiconductors (including both, power and optoelectronics) market revenue is projected to reach $2 billion by 2025 [18] and $5.85 billion at a CAGR of 19.8% by the year of 2027 [17]. Furthermore, according to Inkwood Research, a leading market & industry research firm based in Boston Massachusetts in the US, North America and Japan will remain the major market where GaN material is being integrated into their technology as illustrated in **Figure 1.3**.(b).

(a)

(b)

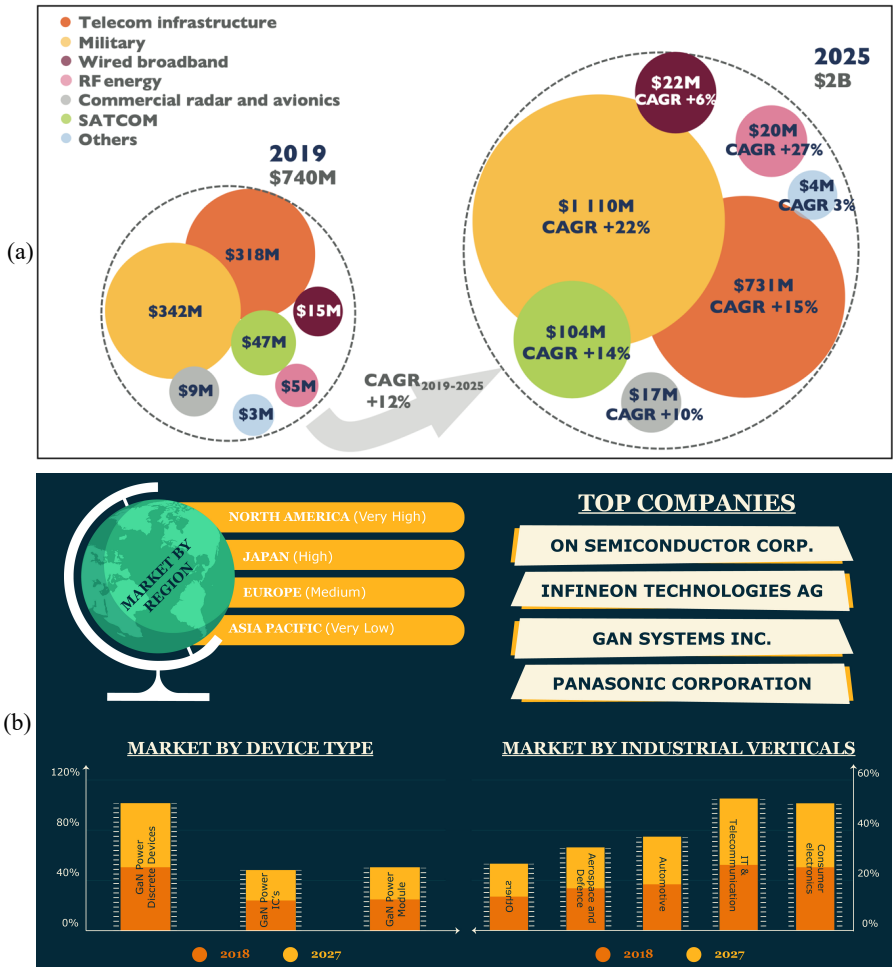


Figure 1.3. GaN market forecast split by the type of applications for 2025 and (b) by device types and region for year 2027, [18], [19], respectively

1.4. Current Research Challenges

GaN-based HEMTs are available in a variety of structures, including AlGaN and InGaN. These HEMTs may be fabricated with heterostructures that include various materials and band gap energies. Buffered layers are utilized in the construction of GaN-based HEMTs to reduce the lattice mismatch between the crystalline structures. Some of the difficulties in the AlGaN/GaN HEMTs device include lowering the gate leakage current, lowering the noise, and increasing the drain current. The most essential criteria for high performance AlGaN/GaN HEMT devices are high-quality growth of the epilayers, less conductive substrates, and high thermal conductivity [20], [21]. Despite their capabilities, HEMTs devices have several essential drawbacks. For instance, the presence of imperfections and traps in the construction of these devices has an impact on commercial use

and repeatability. Also, other problems such as trapping have an impact on device dependability, and results in reduced drain current loss of output/input sensitivity [22], and degraded output power [23], [24]. The impact of the traps in AlGaN/GaN HEMT devices may be investigated using a variety of techniques. For example, the relationship between the output power and the traps is one of these investigative approaches [25]. However, these defects cause electron trapping and resulting in a decrease in device performance in the first place [26]. Therefore, other approaches have recently been employed to examine the trapping effect in AlGaN/GaN HEMTs. The transient spectroscopy approach [27], the gate to drain conductance method [28], the high to low frequency method [29], [30], and the capacitance and conductance method [31]–[33] are also examples of these techniques. Furthermore, the conducting channel of AlGaN/GaN HEMTs devices suffers from self-heating [34]. This heating impact rises as the power density increases [35], [36], resulting in a decrease in device performance [20], [21]. Self-heating activates a variety of degradation processes, including mechanical, electrical, and material deterioration [36]. As a result, one of the most important challenges in attaining device stability and reliability in AlGaN/GaN HEMTs is regulating device temperature [36], [37]. In AlGaN/GaN HEMTs, the self-heating effect causes the channel temperature to rise, which directly affects the current transport characteristics [38]–[40]. The device's usually-ON behavior, a depletion mode, [41], [42] is one of the most challenging aspects of AlGaN/GaN HEMTs, especially in power electronics applications. Hence, using various architectures for the device gate is one of the proposed solutions to overcome the issue [43], [44]. Other alternatives include using a thin AlGaN barrier layer with high Al composition up to 100% [45] or p-type GaN [46]. In addition, these devices have the added challenge of a low gate voltage [47]. Currently, the gate voltage has a maximum limitation of approximately 6 volts at a low threshold, beyond which the gate will behave as an Ohmic electrode and will start to conduct rapidly. The necessity for a minimum current to keep the transistor ON is another disadvantage of AlGaN/GaN-based HEMTs [47], [48]. Other significant problems with AlGaN/GaN HEMTs compromise their performance such as the gate leakage current [49] and the drain current collapse [50] are two examples. The gate leakage current lowers power efficiency and the breakdown voltage which leads to an increase in noise [51]. Furthermore, as the

device temperature rises, the device's gate leakage current rises as well, resulting from the presence of surface traps and conventional mesa isolation due to a sidewall contact with 2DEG [52], [53].

1.5. Research Aim

The aim of this research is to study the effect of device dimensions such as the drain width, gate width and finally the distance between source and drain was also examined. Alternative isolation approaches between devices were analysed to lower the leakage current and potential metallic discontinuity caused by the formation of a non-planar gate resulted from mesa conventional isolation method. Also, novel passives such as transmission lines, inductors and capacitors were studied which can be utilized in MMIC design and fabrication.

1.6. AlGaN/GaN RF HEMTs Literature Review

A broad research literature was conducted to gain an overview of the previous research of the state-of-the-art of AlGaN/GaN HEMTs and their RF performance. The findings of this study are summarized in **Table 1.3**, which includes the most important design characteristics culled from the literature, mainly the gate length L_g and the barrier thickness t_{bar}. **Table 1.3** also contains the main output characterisation parameters such as f_T, f_{max} and $g_{m\text{-}dc}$. In case where a parameter is not given, a dash is replaced instead. Additionally, the ratios $f_t \cdot L_g$ and L_g/t_{bar} are calculated and positioned in the table, the latter ratio is used to sort the table with respect to their evaluation in a descending order.

Table 1.3. Literature review of the state-of-the-art GaN RF-HEMT devices

Ref.	L_g/t_{bar} (AR)	f_T (GHz)	$f_T \cdot L_g$ (GHz.µm)	L_g (nm)	t_{bar} (nm)	f_{max} (GHz)	f_{max}/f_T	L_{SD} (µm)	$g_{m\text{-}dc}$ (mS/mm)
[54]	200	10	19	2000	10	38	3.94	6.0	126
[54]	100	13	26	2000	20	46	3.59	6.0	134
[54]	67	8	15	2000	30	24	3.11	6.0	120
[55]	65	14	18	1300	20	-	-	-	125
[56]	65	14	18	1300	20	-	-	-	110
[57]	40	14	14	1000	25	35	2.60	-	-

Ref.	L_g/t_{bar} (AR)	f_T (GHz)	$f_T \cdot L_g$ (GHz.μm)	L_g (nm)	t_{bar} (nm)	f_{max} (GHz)	f_{max}/f_T	L_{SD} (μm)	$g_{m\text{-}dc}$ (mS/mm)
[58]	33	21	11	500	15	34	1.63	-	320
[59]	30	19	14	750	25	-	-	-	220
[60]	30	15	15	1000	33	24	1.60	3.0	229
[61]	24	24	17	700	30	45	1.88	-	-
[62]	22	20	14	700	31	56	2.80	-	155
[63]	19	37	11	300	16	55	1.49	4.8	200
[64]	14	70	11	150	11	135	1.93	1.7	-
[65]	14	75	17	250	17	-	-	-	245
[66]	13	70	11	160	12	100	1.43	-	450
[66]	13	130	21	160	12	170	1.31	-	450
[67]	13	67	17	250	20	126	1.88	2.0	354
[67]	13	61	15	250	20	89	1.46	2.0	354
[68]	13	82	21	250	20	103	1.26	0.6	321
[68]	13	52	13	250	20	85	1.63	2.0	321
[69]	13	40	10	250	20	86	2.14	2.1	322
[59]	12	43	13	300	25	-	-	-	220
[70]	11	107	6.4	60	5.5	160	1.50	-	-
[71]	11	55	17	300	28	121	2.2	2.3	425
[72]	10	55	11	200	20	-	-	1.5	-
[72]	10	35	7.0	200	20	-	-	5.5	-
[73]	10	50	10	230	20	92	1.84	1.7	240
[74]	10	66	17	250	25	-	-	2.0	314
[75]	10	55	14	250	24	100	1.82	2.0	250
[76]	10	37	11	290	29	-	-	-	-
[77]	9.5	45	9	200	21	48	1.07	1.0	-
[78]	9.3	103	13	130	14	170	1.65	2.9	-
[79]	9.1	23	5.8	250	28	70	3.04	5.0	118
[80]	9.0	92	17	180	20	102	1.11	0.6	290
[81]	8.7	85	8.5	100	12	210	2.47	-	-
[82]	8.7	85	8.5	100	12	210	2.47	2.1	-
[83]	7.7	153	15	100	13	230	1.5	-	-
[84]	7.7	90	9.0	100	13	-	-	-	-
[85]	7.6	65	7.8	120	16	-	-	-	210
[86]	6.7	190	11	60	9.0	241	1.27	2.0	424

Ref.	L_g/t_{bar} (AR)	f_T (GHz)	$f_T \cdot L_g$ (GHz.μm)	L_g (nm)	t_{bar} (nm)	f_{max} (GHz)	f_{max}/f_T	L_{SD} (μm)	$g_{m\text{-}dc}$ (mS/mm)
[87]	6.7	70	7.0	100	15	41	0.59	2.1	-
[58]	6.7	70	7.0	100	15	41	0.59	-	320
[75]	6.3	80	12	150	24	120	1.50	2.0	250
[59]	6.0	74	11	150	25	-	-	-	220
[88]	5.7	52	8.8	170	30	-	-	3.3	10
[89]	5.6	48	4.8	100	18	75	1.56	1.0	-
[90]	5.3	163	9.8	60	11	192	1.18	2.0	417
[91]	5.1	83	8.3	100	20	123	1.48	-	330
[92]	5.0	160	11	70	14	200	1.25	1.6	374
[93]	4.9	75	7.5	100	21	125	1.67	7.0	175
[74]	4.8	102	12	120	25	133	1.30	2.0	314
[74]	4.8	121	14	120	25	162	1.35	2.0	314
[94]	4.8	121	14	120	25	162	1.35	2.0	314
[77]	4.8	121	12	100	21	146	1.21	1.0	-
[95]	4.5	152	9.1	60	13	173	1.14	2.0	400
[96]	4.3	102	8.7	85	20	-	-	2.0	349
[97]	4.3	79	12	150	35	124	1.57	2.6	-
[98]	4.0	101	12	120	30	155	1.53	1.0	217
[91]	3.8	86	6.5	75	20	122	1.42	1.5	310
[77]	3.6	152	11	75	21	148	0.97	1.0	540
[99]	3.0	81	7.3	90	30	187	2.31	-	174
[100]	2.7	181	5.4	30	11	186	1.03	2.0	402
[100]	2.7	145	4.4	30	11	161	1.11	2.0	-
[101]	2.3	81	5.7	70	30	190	2.35	2.0	-
[102]	2.1	110	5.5	50	24	140	1.27	2.0	-
[103]	1.9	43	3.0	70	36	100	2.33	1.1	-
[104]	1.3	102	3.6	35	27	-	-	2.0	-
[104]	1.3	110	3.9	35	27	-	-	1.5	-
[105]	-	70	4.2	60	-	300	4.29	2.0	370
[105]	-	63	3.8	60	-	270	4.29	1.1	410
[106]	-	163	15	90	-	185	1.13	1.5	-
[107]	-	25	13	500	-	40	1.59	-	-
[87]	-	21	11	500	15	34	1.63	-	-

1.7. Thesis Structure

Chapter 1 (this one) highlights the significance of GaN as a semiconductor in comparison with other materials currently used in the industry. Also, a comprehensive review of GaN HEMTs is also included to observe the maturity process over the last two decades. **Chapter 2** encompasses the theory and working principles of GaN HEMT devices, and the most important methods applied for the characterisation of HEMTs in DC and RF conditions. **Chapter 3** underlines the fabrication techniques and the processes utilised into the formation of HEMT devices such as lithography and etching. **Chapter 4** includes the DC and RF results of HEMTs fabricated in various dimensions such as device width and source-drain distance while using different GaN materials grown on Si and SiC for comparison purposes. Also, passives are developed to study the substrate effects on RF performance. **Chapter 5** proposes novel isolation approaches to overcome issues such as gate metal discontinuity and gate leakage current. Furthermore, the proposed devices DC and RF performance will be examined and compared to conventional mesa etch. **Chapter 6** discuss the development of a small signal model for GaN HEMT using the 16-element equivalent circuit model. **Chapter 7** proposes novel Schottky barrier diodes using trenches below the anode. Various diodes are included to study the effects of number of anodes and width on the diode performance especially under RF operation. **Chapter 8** concludes with a summary of findings and a recommendation of future work.

2. GaN HEMTs Theoretical Background and Characterisation

In this chapter, an overview of the GaN theoretical background was discussed and analysed to appreciate the complexity of HEMT devices. Furthermore, the key HEMT parameters were outlined to enable the appropriate characterisation of the devices and analyse their main figure of merits to evaluate their performance under the juxtaposition of DC and RF operating condition.

2.1. Polarisations in AlGaN/GaN Heterostructure

Unlike conventional semiconductor where their crystallisation occurs in a cubic face such as silicon, GaN on the other hand, as in the case of most III-nitride materials, forms a hexagonal crystal structure known as wurtzite crystal as shown in **Figure 2.1**.(a). Due to this ionic bond, GaN is mechanically robust, chemically stable which as a result enables GaN to withstand a higher temperature than the other standard semiconductors [108]. Also, as depicted in **Figure 2.1**.(a), GaN usually forms in a polar wurtzite crystal structure and is only grown along its polarity axis with opposite atoms on each surface (Ga-face or N-face). As a result of the presence of face-polarity and the ionic bond, polarisations are induced within the material with charge of opposing polarity at each of GaN surfaces resulting in an internal electric field generated in the material. The induced internal electric field can be influenced by the addition of atoms in the Ga-face such as aluminum or indium. The induced polarisations are either spontaneous or piezoelectric in nature with different directions engineered by the growth direction, structure conditions and the surface-face orientation of the gallium nitride. Both polarisations, i.e., spontaneous, or piezoelectric are induced within GaN material with the absence of an external electric field. This is manifested when two different GaN materials are grown to form a heterostructure, a two-dimensional electron gas (2DEG) appears near the interface where confined electrons exhibit higher mobility. An example of a Ga-face with an AlGaN barrier grown on top of GaN (AlGaN/GaN Ga-face heterostructure) as illustrated in **Figure 2.1**.(b) where an AlGaN tensile stress, triggered by the lattice mismatch

due to aluminum inclusion, enhances the presence of the 2DEG confinement. Various GaN heterostructures are available which enables the engineering of HEMT as required by the application [109].

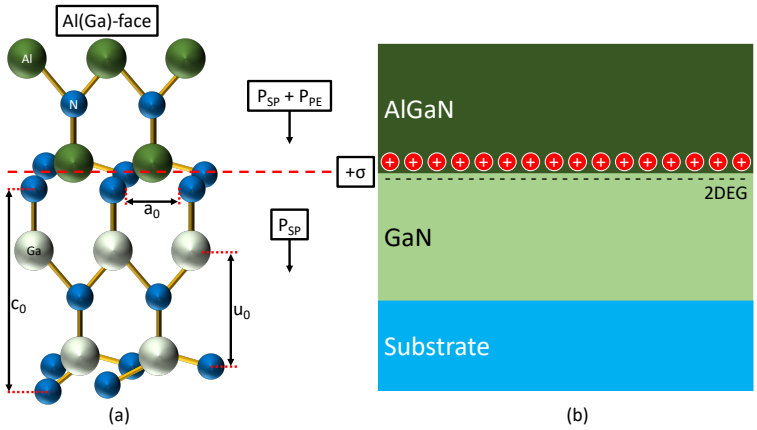


Figure 2.1. Crystal structure of Ga-face AlGaN/GaN (a), the induced polarizations and their directions in AlGaN/GaN Heterostructure (b)

2.1.1. Spontaneous Polarisation

Spontaneous polarisation (P_{SP}) naturally occurs from the asymmetry presence in wurtzite crystal when GaN is grown in y-plane. The spontaneous polarisation can generate a substantial electric field in the order of 3 MV/cm. Using the same $Al_xGa_{1-x}N$/GaN heterostructure presented in **Figure 2.1**.(b), the spontaneous polarisation can be calculated using the following expression [110]:

$$P_{SP}(x) = -(0.029 + 0.052x) \quad Cm^{-2} \tag{2.1}$$

where *x* is the aluminum mole fraction in the AlGaN layer. For a typical AlGaN/GaN heterostructure, 25% of aluminum composition is commonly used in industry, which produces a P_{SP} level of 0.042 Cm^{-2}, whereas an AlN layer with 100% Al content gives a P_{SP} magnitude of 0.081 Cm^{-2}. Therefore, almost 100% increase in P_{SP}, which corresponds to a fourfold increase of Al content in the AlGaN barrier layer. Furthermore, it is evident from Eq.(2.1) that P_{SP} charge is induced even with a heterostructure formed between GaN grown on another GaN layer owning to the fact that an ideal symmetry of wurtzite crystal is naturally unachievable.

2.1.2. Piezoelectric Polarisation

Piezoelectric polarisation (P_{PE}) on the other side, is the result of a lattice mismatch between the channel and the barrier grown on top of it. This is achievable only by the introduction of an additional atoms such as aluminum into either layer channel or barrier. Hence a heterostructure formation is a requirement. This results in a further increase of the generated internal electric field to a total of 5 MV/cm. In the case where the barrier has an aluminum content with Ga(Al)-face crystal structure, as demonstrated in **Figure 2.1**.(b), the acquired condition is an AlGaN tensile strain form of P_{PE} calculated using the expressions [111].

$$P_{PE} = e_{33}\varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_y) \tag{2.2}$$

$$where\ \ \varepsilon_z = \frac{(c + c_0)}{c_0} = 2\frac{C_{13}(a - a_0)}{C_{33} \cdot a_0}\ and\ \varepsilon_x = \varepsilon_y = \frac{(a - a_0)}{a_0} \tag{2.3}$$

$$\therefore P_{PE} = 2\frac{(a - a_0)}{a_0}\overbrace{\left(e_{31} - \frac{e_{33}C_{13}}{C_{33}}\right)}^{always < 0} \tag{2.4}$$

where C_{13} and C_{33} are elastic constants, e_{31} and e_{33} are piezoelectric constants, and finally, a_0 and c_0 are lattice parameters under equilibrium condition without P_{EP} in pure GaN wurtzite crystal. From Eq.(2.4), P_{PE} always gives a negative evaluation since the term $\left(e_{31} - \frac{e_{33}C_{13}}{C_{33}}\right)$ is always < 0 for the entire range of Al compositions. Therefore, the absolute magnitude is calculated and a positive or a negative sign is assigned, for tensile strain or compressive stress barriers respectively, to indicate the direction of piezoelectric polarisation to or from the substrate correspondingly.

2.1.3. HEMT Structure Engineering via AlGaN/GaN Polarisations

The total polarisation in gallium nitride material is equal to the sum of the juxtaposition of spontaneous and piezoelectric polarisations when no external electric field is applied. In a conventional $Al_xGa_{1-x}N$/GaN HEMT structure, a 2DEG

produces a sheet density directly proportional to *x* Al composition and vice versa for the thickness of the barrier (d_{AlGaN}). Therefore, a binary AlN of 100% Al, a maximum sheet density is exhibited for a given d_{AlGaN}. On the other hand, the expansion of d_{AlGaN} results in an increase of the 2DEG charge density. However, implications are observed when barrier thickness is enhanced and its Al mole content is increased, such as surface defects acquired from the severe strain in the barrier. Thus, stress management is critical during the growth process of GaN material heterostructure to minimise the bow effects on the surface.

Figure 2.2 shows a typical Ga(Al)-face AlGaN/GaN HEMT structure under two conditions: a tensile strained AlGaN barrier and a compressively stressed GaN barrier. In both conditions, induced polarisations can be controlled by decreasing or increasing the P_{PE} corresponding to lattice mismatch alteration. Moreover, the final induced polarisation at the interface of the top/bottom layers is equal with different signs to indicate the direction only regardless of the type of stress and strain. **Figure 2.2**.(a) demonstrates the condition where AlGaN is a top layer and under tensile strain, a 2DEG quantum well is formed at the interface indicating a positive charge density driven by the accumulation of free electrons. On the other hand, when GaN is the top layer and under compressive stress, a two-dimensional hole gas (2DHG) is established at the interface confined by the accumulation of holes **Figure 2.2**.(b). Owning to electron mobility being five times larger than the hole mobility in gallium nitride, the AlGaN/GaN heterostructure is preferred for high frequency operational HEMT devices.

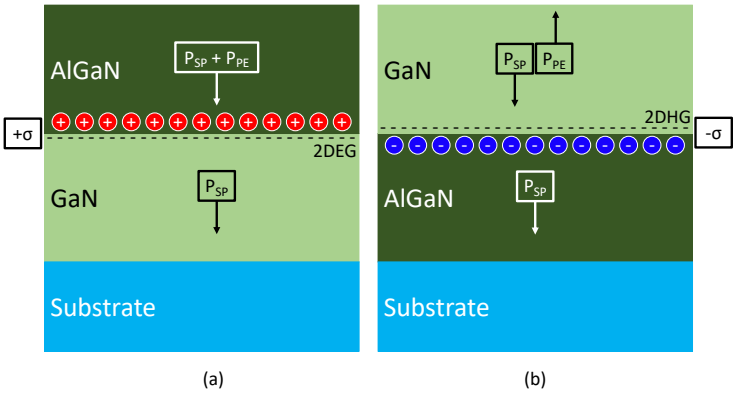


Figure 2.2. Polarisation's direction and charge density (σ) polarity with respect to AlGaN tensile strain (a) vs GaN compressive strain (b) in a Ga-face heterostructure

The total polarisation (σ) can be obtained using the following expression [110]:

$$\begin{aligned}\sigma &= P(bottom) - P(top) \\ &= [P_{SP}(bottom) + P_{PE}(bottom)] - [P_{SP}(top) + P_{PE}(top)]\end{aligned} \tag{2.5}$$

For AlGaN/GaN conventional structure shown in **Figure 2.2**.(a), where a strained AlGaN is grown on a relaxed GaN (zero P_{PE}(GaN)), the total polarisation induced is given by [110]:

$$\begin{aligned}\sigma &= \left[P_{SP}(GaN) + \overbrace{P_{SP}(GaN)}^{=0}\right] - [P_{SP}(AlGaN) + P_{PE}(AlGaN)] \\ \therefore \quad \sigma &= [P_{SP}(AlGaN) + P_{PE}(AlGaN)] - P_{SP}(GaN)\end{aligned} \tag{2.6}$$

In order to deduce the total induced charge density at the interface, a set of equations are used where Al mole fraction is included in linear interpolations between barrier and channel layers physical properties as follows [110]:

Lattice constants:

$$a(x) = (3.189 - 0.077x) \quad \text{Å} \tag{2.7}$$

Piezoelectric constants:

$$e_{31}(x) = -(0.49 + 0.11x) \quad Cm^{-2}$$
$$e_{33}(x) = 0.73(1 + x) \quad Cm^{-2} \tag{2.8}$$

Elastic constants:

$$C_{13}(x) = (103 + 5x) \quad GPa$$
$$C_{33}(x) = (405 - 32x) \quad GPa \tag{2.9}$$

Using Eq.(2.1) and rewriting Eq.(2.4) with (2.7), (2.8) and (2.9) included, the total charge density, defined in Eq.(2.6), at the heterojunction of AlGaN/GaN is then computed using as follows:

$$|\sigma(x)| = \left| P_{SP}(x) + \frac{2\big(a(0) - a(x)\big)}{a(x)} \left(e_{31}(x) - \frac{e_{33}(x) \times C_{13}(x)}{C_{33}(x)} \right) - P_{SP}(0) \right| \tag{2.10}$$

The band gap difference between the AlGaN and GaN generates a large conduction band offset, ΔE_C. Consequently, a quantum well is established at the conduction band near the barrier/channel interface. **Figure 2.3** demonstrates the band diagram of a conventional GaN HEMT. Since the total charge must be neutral and in an equilibrium state, the free electrons accumulate in the quantum well to compensate the highly positive polarisation induced sheet charge at the AlGaN/GaN interface for material with Ga-face configuration.

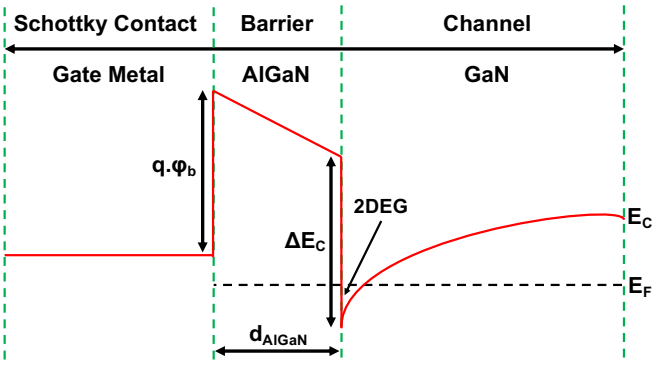


Figure 2.3. AlGaN/GaN heterostructure HEMT band diagram

The electrons in the quantum well form a 2DEG channel. The 2DEG is highly conductive as it exhibits a high-level of electron density, and the mobility rises

from nearly 900 cm^2/Vs in the relaxed GaN, and reaching up to a maximum of 2000 cm^2/Vs in the 2DEG region [112]. Therefore, the maximum 2DEG sheet carrier concentration accumulated in the quantum well near the interface is defined by [112]:

$$n_s(x) = \frac{\sigma(x)}{q} - \frac{\varepsilon_0 . \varepsilon_r(x)}{d_{AlGaN} . q^2} . [q\varphi_b(x) + E_F(x) - \Delta E_C(x)] \quad (2.11)$$

where *x* is the aluminum mole fraction content in the barrier layer, $\sigma(x)$ is the total sheet charge, q is the electron charge (1.6E-19 C), ε_0 is the permittivity of vacuum (8.85E-12 F/m), ε_r is the relative permittivity of the barrier layer (dielectric constant), d_{AlGaN} is the thickness of the barrier layer, $q\varphi_b$ is the Schottky barrier height of the gate contact, E_F is the Fermi level with respect to the GaN conduction band edge energy and ΔE_C is the conduction band offset at the AlGaN/GaN interface where the 2DEG is formed as illustrated in **Figure 2.3**.

2.1.4. 2DEG Sheet Density Simulation

To determine the sheet carrier concentration from the polarization induced sheet charge from Eq.(2.11), the following approximations were used [112], [113]:

AlGaN barrier dielectric constant:

$$\varepsilon_r(x) = 9.5 - 0.5x \quad (2.12)$$

Gate Schottky barrier height:

$$\varphi_b(x) = 0.84 + 1.3x \quad eV \quad (2.13)$$

Fermi energy level:

$$E_F(x) = E_0(x) + \frac{\pi h^2}{m^*(x)} n_s(x) \quad (2.14)$$

where the ground sub-band energy level is computed by:

$$E_0(x) = \left[\frac{9\pi hq^2 n_s(x)}{8\varepsilon_0.\varepsilon_r(x)\sqrt{8m^*(x)}}\right]^{2/3} \quad (2.15)$$

with the effective electron mass, $m^*(x) \sim 0.22m_e$ where m_e is electron rest mass (9.12E-31 kg) and the conduction band offset is approximated by:

$$\Delta E_C(x) = 0.7\left(E_g(x) - E_g(0)\right) \quad (2.16)$$

where the AlGaN barrier band gap is estimated to be:

$$\begin{aligned} E_g(x) &= xE_g(AlN) + (1-x)E_g(GaN) - x + x^2 \\ &= x6.13 + (1-x)3.42 - x + x^2 \end{aligned} \quad (2.17)$$

Figure 2.4 illustrates the calculated 2DEG density as a function of Al alloy composition in the AlGaN barrier with different thickness ranging from 6-35nm. It is apparent that a saturation of n_s is reached at a barrier layer thickness > 22-25nm, where only a fractional change in n_s is obtained with a few nanometers thickness increase. On the other hand, doubling the Al composition in the barrier layer can result in an n_s increase by more than 4 times. For example, a constant barrier thickness of 25nm is considered, the sheet carrier concentration, n_s will be approximately (0.94, 2.43 and 3.95) × 10^{13} cm^{-2} for alloy compositions of *x* = 25%, 50% and 75%, respectively. If the thickness of an AlGaN barrier of alloy composition of *x* = 25% is increased from 15nm to 22nm, the sheet carrier concentration is increased from approximately 0.71 to 0.89 × 10^{13} cm^{2}.

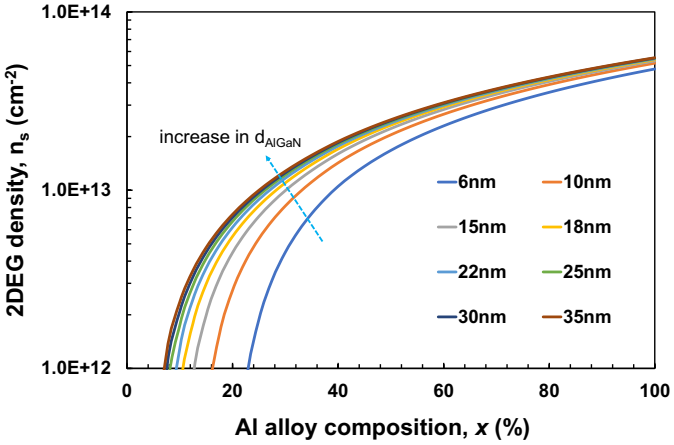


Figure 2.4. 2DEG sheet carrier concentration as a function of Al composition factor, *x*, of $Al_xGa_{1-x}N$

2.2. GaN-HEMT Growth Basics

The transfer of atoms of necessary species from high purity sources to the surface of a substrate wafer is known as epitaxial material growth. Growth factors such as temperature, gas flow rates, and pressure have a significant impact on the quality and uniformity of the developed layered epitaxial structures, hence these parameters must be tuned for the application. Molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) are the two major growth processes for GaN-based heterostructures. Wafers used in this work were grown using MOCVD method for cost-effectiveness and availability.

2.2.1. Molecular Beam Epitaxy

MBE is a growth process that has a highly fine definition and increases the selection flexibility of the polarity of the interface, which makes MBE advantageous in comparison to MOCVD. The temperature of typical growth is roughly 700°C, which is lower than MOCVD. Nevertheless, average GaN material growth rates in an MBE system are approximately 0.5-1 μm/hr, which is slower than MOCVD growth; and makes it a more costly technology. MBE is mostly employed in research since it is a high-quality material that may be used for experiments that require a laboratory proof-of-concept. Fundamental MBE system comprises of the subsequent components [114]:

- Reaction chamber: in which all the reactions necessary to create the epilayers for wafers take place. It includes pumps, growth cells (effusion

cells), a sample manipulator, cryo-shrouds, and a process control reflection high-energy electron diffraction transmission mode monitoring system.

- Load lock: employed to transport wafers into and off the reaction chamber. Load lock is generally kept at high vacuum (10^{-9} Torr) with a single ion pump and a mechanical pump as well.
- Effusion cells: comprised of a heating source and a crucible containing the source material, which is commonly made of pyrolytic boron nitride. The crucible is then heated using one of two methods: electron beam heating or ohmic heating using a filament coiled around the crucible. Thermionic electrons are propelled toward the source material through a potential of a few kV and deposit dozens of watts of power, causing the source material to heat up. Typically, a thermocouple is employed to provide a temperature control.

2.2.2. Metal Organic Chemical Vapor Deposition

One of the fundamental objectives of the growth of epilayer structure is to acquire a wafer with a minimised defect density on the surface and within the bulk. Improved quality material and growth conditions result in superior electron concentration density within the 2DEG region and greater carrier mobility as well. MOCVD is the most widely used growth process in the GaN technology development due to its low cost in comparison to other existing techniques within the growth of industry. MOCVD growth rates are normally 1-2 μm/h, which is almost twice as fast as MBE growth rates. The growth temperature of MOCVD method is usually above 1000°C, which is considerably higher than MBE.

The essentials of MOCVD system comprises of the subsequent elements:

- Reaction chamber: in which all the reactions necessary to create the epilayers for wafers take place.
- Load lock: employed to transport wafers into and off the reaction chamber. Load lock is generally kept at high vacuum with a turbo molecular pump.
- Gas handling unit: the precursors, as well as all the valves and instruments required to regulate the gas flow to the reaction chamber, are included in this system.

- Heating and temperature system: this regulates the temperature in the reaction chamber, which is necessary for a variety of MOCVD operations.
- Exhaust, pressure control, and pumping system: this comprises of a vacuum pump for low-pressure operation and a waste-product exhaust component.

A conventional gas reaction of GaN growth is given by the following chemical reaction formula [115]:

$$TMG + NH_3 \rightarrow TMG{:}NH_3 \rightarrow GaN + 3CH_4 \quad (2.18)$$

where, TMG is trimethylgallium compound [$(CH_3)_3Ga$], which introduces the GaN element into the chemical reaction, NH_3 is ammonia and CH_4 is methane.

2.3. Standard Substrates for GaN-HEMT

Due to the cost and immaturity of Gallium nitride, it is normally grown on a foreign substrate. The choice of substrates varies with options such as Si, SiC and others. The key considerations and material properties when determining an adequate substrate for GaN epilayer growth are the following:

- The lattice mismatch between the grown GaN and the substrate, larger lattice mismatch results in increased surface defects and a degradation of the electron mobility
- Substrate electrical resistivity and its insulation from affecting the signal integrity propagated on its surface and within the GaN epilayer is significant, especially at RF
- Thermal conductivity of the substrate is also an important factor which dictates dissipation capability of the heat generated from the device
- Cost and wafer size availability for ease and cost-effective reproducibility

Therefore, substrates utilised for growth considerably affect the performance of the HEMT device with respect to output power, power density and thermal management. Most widely used substrates will be discussed, and their effects on GaN HEMT performance will be analysed in the next few sections. **Table 2.1**

includes the most common substrates for GaN growth with their properties affecting the growth quality and conditions.

Table 2.1. GaN epilayer common growth substrates and their key properties [116]

↓ Parameter / Material →	GaN	Si	SiC	Sapphire	Diamond
Lattice mismatch (Å)	3.189	5.43	3.08	2.75	3.57
Mismatch to GaN (%)	0	17	3.1	13.9	11.9
Defect density (mm^{-2})	10	10^7	10^6	10^7	10^8
Insulation (Ω·mm)	10^7	100	10^9	10^{14}	10^{14}
Thermal conductivity (W/mK)	130	150	400	35	2000
***TEC (10^{-6} K^{-1})**	5.6	3.4	4.2	7.5	0.8
****Wafer size availability (mm)**	100	200	150	75	100
$Wafer cost (£/die)	3.5	1	2	1.6	-

*Thermal expansion coefficient
**With respect to GaN epi-layer growth quality
$Prices attached for MOCVD grown wafers only per a single die (≈25×25mm^2) normalized to GaN on Si substrate price (£107/die)

2.3.1. Silicon

Silicon is the most attractive substrate material for GaN growth which stems from the low-cost nature of silicon since it is well-established in the CMOS semiconductor industry and thereby silicon substrates are available in large sizes with lowest cost per unit area. However, Si substrates presents two major challenges when utilised for GaN epi-layer growth: Firstly, the low electrical insulation (only 100 Ω·mm) which results in a considerably lossy substrate for RF/microwave distributed elements and transmission lines. This is commonly solved by doping the silicon substrate to increase the resistivity which as a result lowers RF coupling. Secondly, and most importantly, from a technology development point of view, Si substrate has a high lattice mismatch with GaN (17%). Hence complicating the GaN growth process and requiring a careful design of the transition layers to accommodate the lattice mismatch in order to obtain lower defects and a flatter surface with a minimum bow condition. In this project, both low and high resistivity silicon substrates are used for GaN growth [116].

2.3.2. Silicon Carbide

By far, silicon carbide substrate is the most compatible material for GaN growth process and widely used for commercial applications. This is attributed to the low lattice mismatch between GaN and SiC (around 3%) which results in lower defects per unit area. Also, SiC substrate must be made in semi-insulating form (greater than 10E9 Ω·mm) which allows for a superior environment for MMIC circuits with a high suppression of RF coupling between substrate and microwave components fabricated on its surface. Additionally, SiC substrate is desirable for high power applications because of the high thermal conductivity (around 400 W/mK) which enables for higher power operation per unit area, thus higher power density. Therefore, semi-insulating SiC, which is approximately twice the cost of Si ones, is remarkable and surpasses other substrates for GaN growth. In this project, GaN on SiC substrate is used as a benchmark for RF devices and passives characterisation [116].

2.4. Epitaxial Layers of GaN-based HEMT

GaN epitaxy consists of several layers as shown in **Figure 2.5**. In the next sections, the role of each layer is given in the order of their growth from substrate and up.

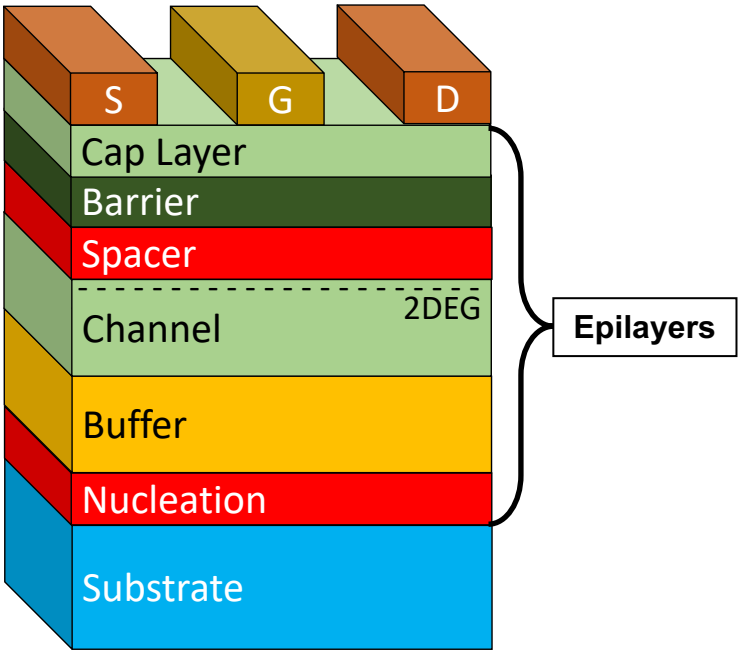


Figure 2.5. Basic HEMT device and wafer structure

2.4.1. Nucleation

Between the substrate and the GaN buffer layers, the nucleation layer remains. GaN, AlN, AlGaN, or graded AlGaN layers can be used as the nucleation layer. This layer is necessary because of the significant mismatch in lattice constant and dissimilarity between GaN and the substrate materials, resulting in a low-quality material with high surface roughness. In the buffer layer, the nucleation layer lowers the density of threading dislocations. The GaN buffer should be extremely resistive; nucleation conditions also have an impact on the resistivity of the GaN buffer. Various materials are used for the nucleation layer depending on the substrate type, with different optimisation variables such as growth temperature and thickness. Sapphire and SiC substrates, for example, can benefit from low-temperature GaN or AlN nucleation layers to considerably reduce the lattice mismatch. For defect concentrations, residual conduction, and the distribution of defects and traps in all layers formed on top of it, the parameters for the nucleation layer's development are crucial. Additionally, the choice of substrate has a significant impact on the nucleation layer as well. Several methods to nucleation have been proposed, including AlGaN (on SiC and sapphire), GaN (on sapphire), and AlN (on SiC and sapphire) nucleation. The latter imposes a challenge due to its low heat conductivity resulting in

considerable amount of heat being encapsulated within the devices and epi-layers rather than being dissipated into the buffer and ultimately to the substrate as it is manifested in **Figure 2.6**. This is referred to as the thermal boundary resistance (TBR) of the GaN epi-layers [117].

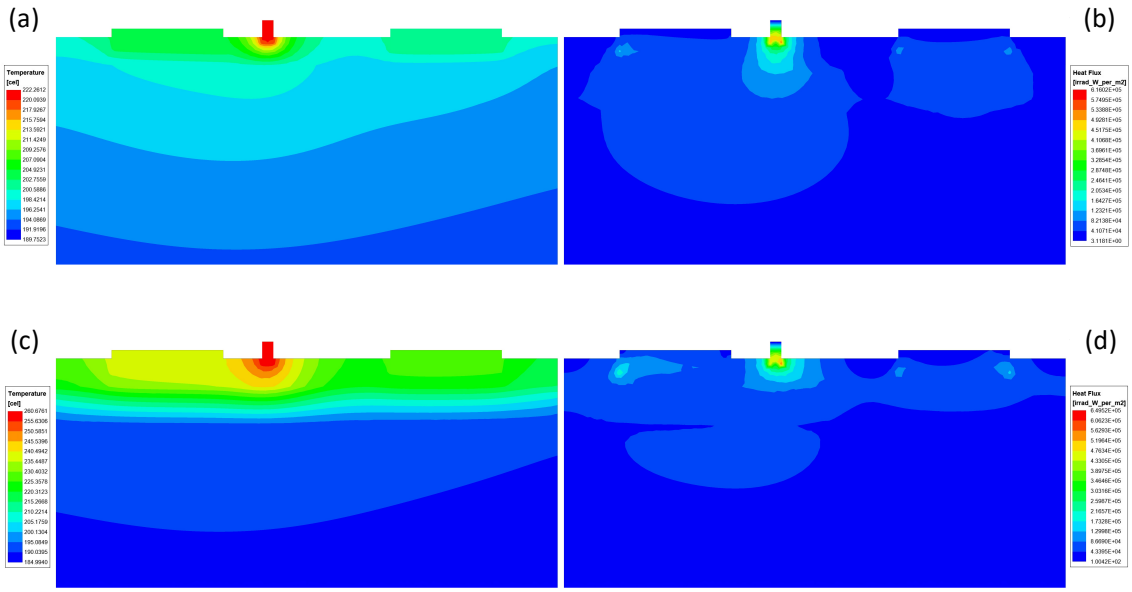


Figure 2.6. Thermal simulation of HEMT without AlN layers, temperature (a), heat flux (b) vs HEMT with AlN, temperature (c) and heat flux (d)

Figure 2.7 illustrates the difference between a pure AlN and a compound of material such as AlGaN as nucleation layer. In this simulation, a thermal resistance (all in W/mK) values were assigned to the different layers as follows: 25 for the AlGaN barrier, 130 for the GaN channel 3 for the AlN nucleation and 150 for the Si substrate. The simulation results show that by introducing Gallium into the nucleation layer, the maximum temperature generated at the gate, is dropped by almost 40 from 260 to less than 220 (all in °C) where the heat clearly dissipates into the substrate evident by the increase in temperature within the substrate. Since GaN HEMTs have high power densities (≈ 7W/mm), this is significant to consider and minimise during material design and growth.

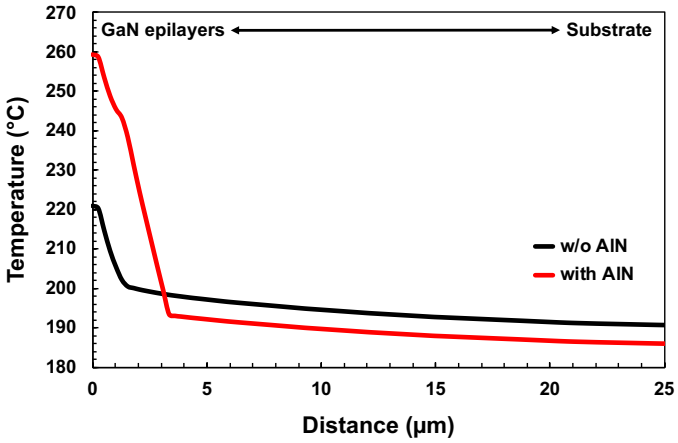


Figure 2.7. Temperature distribution profile from top to bottom of the GaN/Si wafers

2.4.2. Graded Buffer

To achieve an optimal device performance, the GaN buffer layer must be of very high quality, with low defect density and low electrical conductivity with a semi-insulating behaviour to prevent both charge trapping of the 2DEG electrons at the surface, which results in a collapse of the device drain current and consequently output power reduction, and high buffer leakage, which in return makes the pinch-off process of the device almost unachievable. As a result of the failure to pinch off a HEMT device, the available current swing and hence, the possible microwave output power are substantially degraded. Moreover, even if mesa structures are implemented to isolate the active devices on the same chip, buffer leakage might induce electrical interaction irrespective of the applied isolation. Furthermore, the GaN buffer layer's surface should be smooth to provide a suitable accommodation for the subsequent GaN channel and AlGaN barrier layers. To attain high mobility and excellent confinement of the 2DEG electrons, a smooth surface profile is fundamentally required. Also, a device pinch-off is considerably enhanced by a higher carrier confinement implementation [118].

2.4.3. Channel

The channel is the second most important layer if not equally important with the barrier layer. It is utilised during growth to form the heterostructure with the barrier situated at the top (back barrier is possible as well). Generally, the channel has

a lower bandgap with respect to the barrier layer. Hence, the 2DEG is generated near the interface as explained in section 2.1.

2.4.4. Spacer

Comparing the AlGaN/GaN heterostructure with the same Al mole percent, the heterostructure with the AlN spacer layer provides superior channel electron confinement, due to the peak in the conduction band structure as illustrated in **Figure 2.8**. This is because AlN spacer prevents channel carrier penetration through the AlGaN barrier, and electron transport is less susceptible to alloy disorder and/or interface roughness scattering. As a result, structures containing a spacer layer have enhanced mobility. Owning to the high polarisation-induced charge generated by the substantial lattice mismatch between AlN and GaN, the introduction of an AlN spacer layer may enhance the sheet density. In AlN/GaN heterojunctions, sheet carrier concentrations of up to 5E13 cm^{-2} have been obtained using this technique. The potential energy in the AlGaN barrier layer should not fluctuate with distance if the AlN spacer thickness is set to 1-2nm. As a result, the sheet carrier concentration n_s is less reliant on the AlGaN barrier thickness with the assistance of an AlN spacer. Nevertheless, long-term reliability issues arising from the strong built-in electrical field may be a probable disadvantage stemming from the addition of an AlN spacer layer between the barrier and the channel [118], [119].

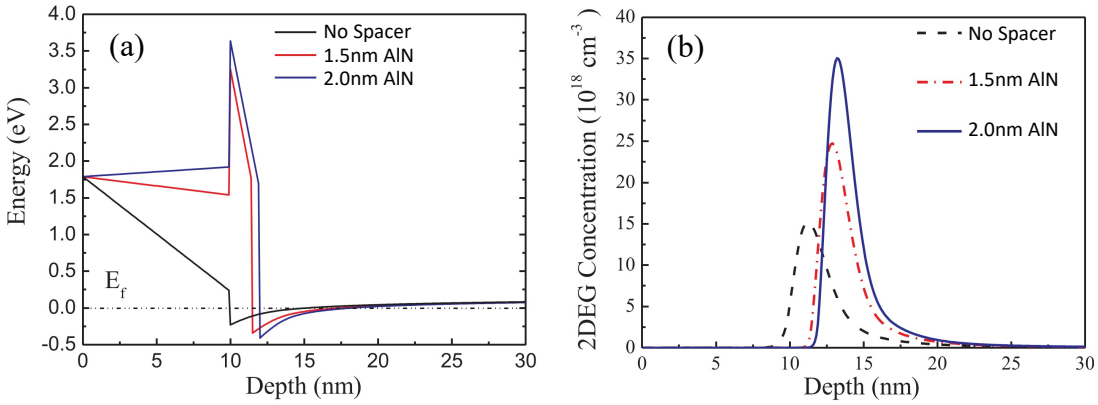


Figure 2.8. AlGaN/AlN/GaN HEMT (a) energy band diagram and (b) 2DEG sheet concentration [120]

2.4.5. Barrier

This is the most important layer which is also known as the supply layer through which electrons are supplied to the 2DEG confinement formed at the interface between the barrier and the channel. The barrier layer or the cap layer is sometimes heavily doped with Si to ease the tunneling of electrons due to the reduction of the ohmic contacts resistance [121]. Furthermore, the barrier layer is designed with a higher conduction band energy than the channel (GaN) and the common materials used are primarily InAlN and AlGaN. The latter can be adjusted to increase the 2DEG sheet concentration by influencing the amount of Al within the compound and the barrier thickness as described in section 2.1.4.

2.4.6. Cap Layer

The final layer of the HEMT structure growth is the cap layer (usually GaN). It has several advantages, including eliminating barrier relaxation which decreases gate leakage current as the barrier height rises. It also acts as a surface passivation layer, reducing oxidation and increasing the charge density of the 2DEG and lowering the electron traps. GaN has a smaller band gap (3.4 eV) than the barrier (4.1 eV with 25% Al content), which further enhance the Ohmic contact performance by reducing the resistance on an AlGaN/GaN structure. As a result of the increased effective Schottky barrier height, gate leakage is enhanced and the breakdown voltage of AlGaN/GaN HEMTs is also considerably improved by introducing a p-doped GaN cap into the HEMT structure [122].

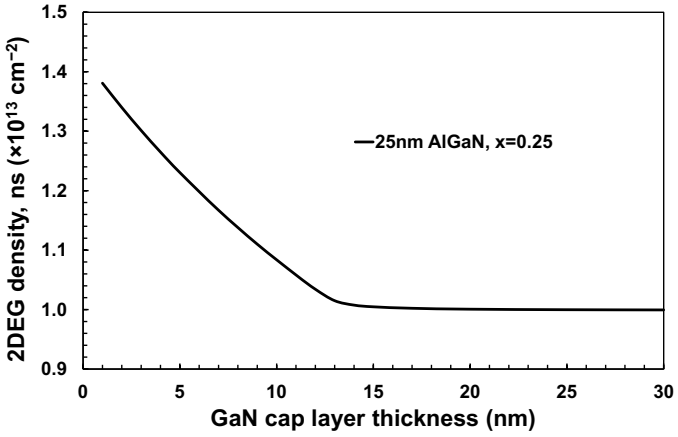


Figure 2.9. 2DEG sheet carrier concentration as a function of the GaN Cap layer

A GaN cap thickness is typically in the range between 1-2 nm. However, thicker cap layer is implemented where the use of S_3iN_4 passivation is omitted. An obvious drawback of GaN cap is illustrated in **Figure 2.9**, where the 2DEG electron density is linearly reduced by less than an order of magnitude with the thickness of the cap layer and saturates at a point between 10-15nm. This is attributed to the reduction of the barrier between the supply layer (AlGaN) and the channel (GaN) that arose from the cap introduction at the surface [122].

2.5. GaN HEMT Contacts

HEMT devices comprises two types of metal-semiconductor interface: Ohmic and Schottky. The former is used for the source and drain formation where the barrier between the metal and the semiconductor is reduced for maximum current transport and minimum voltage drop. The Schottky, however, which is also known as the rectifying contact is used as the gate between the source and drain to control the current transport. It should have low current flow and maximum control over the 2DEG channel through the electric field.

2.5.1. Ohmic Contacts

Low resistance and thermally stable ohmic connections are required for excellent performance of GaN-based HEMTs. Ohmic contacts ideally should exhibit a negligible electrical resistance (R) to the flow of current (I) to minimise power dissipation (P_{diss}) which is given by the following expression:

$$P_{diss} = I^2R \tag{2.19}$$

The maximum drain current, ON-resistance, extrinsic transconductance, power dissipation at ohmic contacts, and therefore the unity gain cut-off frequency can all be influenced by the ohmic contact quality. For GaN-based HEMTs, forming a good ohmic contact with low contact resistance is critical. Generally, wide bandgap semiconductors pose challenges with respect to the realisation of low ohmic contact resistance. The metal layer should be in touch with the 2DEG channel to achieve a minimal contact resistance. As a result, just by implementing low work function metals will not result in a satisfactory ohmic contact. Multilayer

metals are commonly utilised to make the source/drain contact on III-Nitride HEMTs, which after annealing creates an alloyed-ohmic contact with the 2DEG. As a result, high temperature annealing is required to activate the ohmic contact in GaN-HEMT devices, making annealing a vital element of ohmic contact fabrication. However, diffusion of metals and out-flow of their liquid phase because of high temperature thermal annealing makes it difficult to achieve good surface morphology and acceptable edge acuity, which affects the subsequent processing and can diminish source-drain distance. Apart from low contact resistance, the ohmic contact's thermal stability is also a major problem that must be taken into consideration during the ohmic formation. Mostly, Ti/Al metallisation-based Ohmic connections are used in AlGaN/GaN heterostructures [123]. The metal schemes Ti/Al/Ni/Au, Ti/Al/Mo/Au, Ti/Al/Pt/Au, and Ti/Al/Ti/Au are the most often reported schemes [124]. Many researchers choose Molybdenum (Mo) as a diffusion layer over Nickel (Ni), Platinum (Pt), or Titanium (Ti) because it has a low contact resistance of about 0.2 Ω·mm, good edge definition, and better surface morphology. Every metal layer in the Ohmic contact stack up serves a specific function [124]:

- **Titanium** ensures excellent stability by acting as an adhesive layer. It dissolves the native oxide on the AlGaN surface and creates nitrogen vacancies in the AlGaN layer by reacting with nitrogen atoms to form TiN, which then act as n-type donor states, increasing doping concentration and allowing electrons to tunnel through the thinner metal/semiconductor barrier with little/no resistance.
- **Aluminum** interacts with Ti to create an Al_3Ti layer, which inhibits oxidation of the underlying Ti layer. It also acts as a diffusion barrier for the metals on top, which forms Schottky barriers.
- The Al is then prevented from combining with the Au by **Nickel**, **Platinum**, **Titanium**, or **Molybdenum**, since the reaction of such a combination creates a highly resistant of intermetallic layer Au_5Al_2 and $AuAl_2$ known as white and purple plague respectively.
- Due to its great electrical conductivity and high resistance to corrosion and oxidation, **gold** is typically utilised as a point of contact with the outside environment.

2.5.2. Schottky Contacts

The thermionic emission which permits electrons to pass over the Schottky barrier, is the primary mode of transport in rectifying contacts. The work function of the contact metal has a significant impact on the barrier height of wide bandgap materials like GaN. Metals with high work functions are commonly utilised to create Schottky connections for GaN-based semiconductors. The work functions of several metals are shown in **Table 2.2**. Nickel, Platinum, and Gold are the best metals for Schottky connections, as seen in this table, since they have the highest work functions of all the metals on the list. Nevertheless, as Platinum is directly deposited on GaN, it tends to suffer from adhesion issues, and the presence of Gold at the semiconductor interface causes significant leakage current at the gate. As a result, Nickel (Ni) is commonly utilised as the Schottky contact metals for GaN-based semiconductors. Au is typically applied as the second layer on top of Ni to prevent it the oxidation and native oxide formation on the Ni surface.

Table 2.2. Work function of various metals for Schottky [125]

Metal	Work function (eV)
Ag	4.26
Al	4.28
Ti	4.33
Mo	4.60
Au	5.10
Ni	5.15
Pt	5.65

2.5.3. Drain/Source Ohmic Electrode Characterisation

For evaluating the quality and performance of Ohmic contacts, the Transfer Length Method (TLM) that is also known as the Transmission Line Model, is utilised. Reeves and Harrison were the first to present this approach, and a comprehensive study can be found in [100]. **Figure 2.10** shows the measurement set up, where four probes are applied to adjacent pads with a known width (W) and spacing between the pads, L_x. The currents are then injected between the two pads and measured by the four probes to cancel the effects of the probe resistance. This is repeated between pads with various spacing distances and

then each measurement is used to extract the contacts total resistance given by the following expression [126]:

$$R_T = 2R_C + R_{ch} = 2R_C + \frac{L}{W}R_{sh} \tag{2.20}$$

where R_T is the total resistance, R_C is the contact resistance, R_{ch} and R_{sh} are the channel resistance and the sheet resistivity respectively.

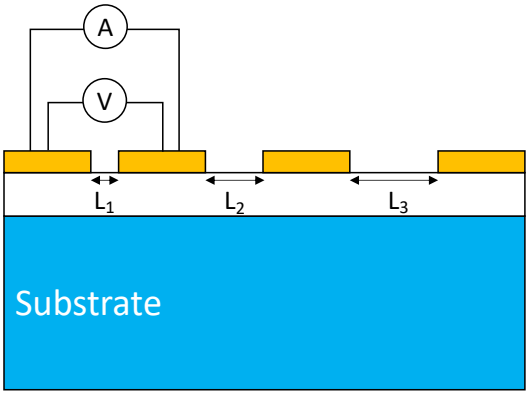


Figure 2.10. Ohmic contact resistance LTLM setup

These total resistances are then plotted as a function of the corresponding spacing distance as demonstrated in **Figure 2.11**. A fit line is then plotted as well to obtain the contact resistance R_C and the transfer length L_T at the y and x axis intercepts respectively.

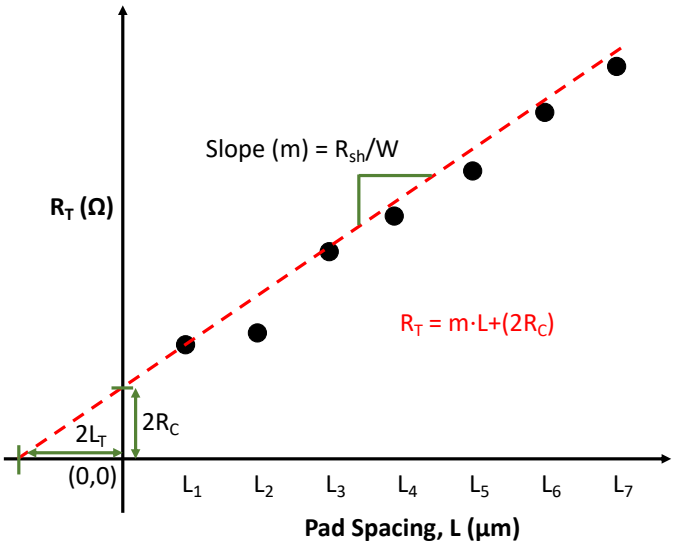


Figure 2.11. Measured total resistance as a function of gap spacing

As a result, using this method, the resistance arising from the metal contact, is extrapolated and the semiconductor channel resistance is computed using Eq.(2.20).

2.6. Operational Principles of HEMT and Characterisation Parameters

The 2DEG occurs in a conventional depletion mode HEMT structure without the requirement for an external bias. This is due to the previously discussed polarisation effect. A negative gate bias is provided to turn the device off, and the 2DEG channel begins to deplete until a gate bias that is larger than the threshold voltage is achieved, at which point the channel is completely drained of electrons and the device is switched off. When the gate bias is positive, however, the electron density in the 2DEG rises, resulting in a greater current flowing between the source and the drain. The gate voltage for a Schottky gate is restricted to +1 V, beyond which the gate turns on and begins to conduct, like a Schottky diode. The 2DEG channel does not occur naturally in enhancement mode devices, thus an extra gate voltage must be provided to collect enough electrons to generate the 2DEG channel. The use of a p-type GaN cap layer to deplete the 2DEG channel, recessing the AlGaN barrier under the gate to locally deplete the 2DEG channel, or the reduction of AlGaN barrier thickness to 3nm which is below the critical thickness for inherently forming the 2DEG channel are examples of enhancement mode structures (normally off devices). Unlike depleted HEMT devices (normally-on), a positive gate voltage is needed for the enhancement mode devices to collect sufficient electrons in the channel to initiate the conduction between the source and the drain.

Gan HEMTs current is generated in a similar method as in a typical field effect transistor (FET). The drain current which flows between the drain and the source can be estimated from the charge moved across and the time the electrons take to pass by the channel controlled by the applied electric field at the gate. The total charge donated Q_T is equal to $qn_sL_{SD}W_g$ and the time (τ_T) is equal to the distance between the source and drain L_{SD} divided by the effective velocity (v_{eff}) of the

electrons within the channel. Therefore, the current flowing in the device can be expressed as [127]:

$$I_{ds} = \frac{Q_T}{\tau_T} = \frac{qn_s L_{SD} W_g}{\frac{L_{SD}}{v_{eff}}} = qn_s v_{eff} W_g \tag{2.21}$$

where n_s is the sheet carrier concentration, q is the electron charge and W_g is the device/gate width.

Typical characteristics of HEMT current voltage is shown in **Figure 2.12**. It depicts the drain current as the drain voltage is raised at various gate voltages. More electrons accumulate in the 2DEG channel when the gate voltage is positively increased, resulting in a rise in the drain current.

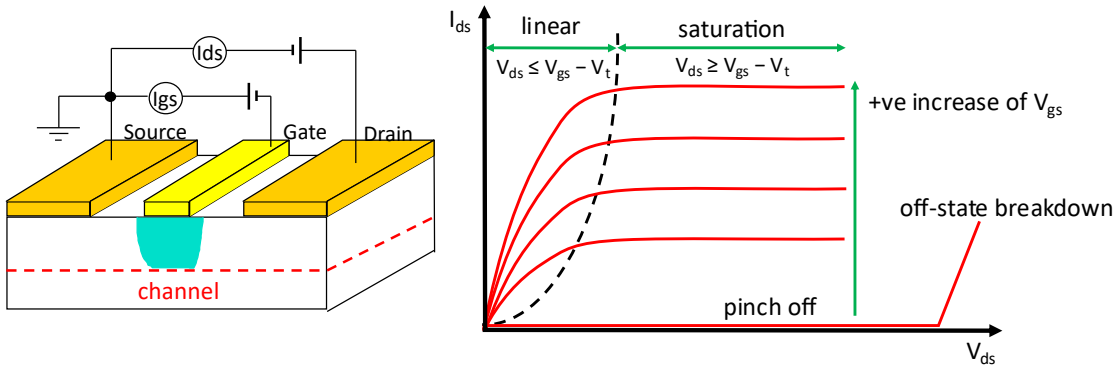


Figure 2.12. AlGaN/GaN HEMT biasing configuration and the output *I-V* characteristics

The total charge in the channel can also be calculated using the gate voltage as follows:

$$Q_T = CV = \frac{\varepsilon_{AlGaN}}{d_{AlGaN} + \Delta d}(V_g - V_t) \tag{2.22}$$

Where *C* is the gate capacitance, Δd is the effective distance of the 2DEG from the heterointerface, *V* is the effective voltage at the gate electrode and V_t is the threshold voltage. Similarly, the sheet charge concentration can also be expressed in terms of gate voltage as:

$$n_s = \frac{CV}{q} = \frac{\varepsilon_{AlGaN}}{q(d_{AlGaN} + \Delta d)}(V_g - V_t) \tag{2.23}$$

It is evident that to deplete the channel from the charge, the applied gate voltage must be equal to the threshold voltage giving a total of n_s equal to zero. This will stop the flow of current between the ohmic contacts and put the device into a pinched off state. Furthermore, the effective velocity (v_{eff}) of the electrons is given by:

$$v_{eff} = \mu_e E = \mu_e \frac{V_{ds}}{L_{DS}} \tag{2.24}$$

where μ_e is the electron mobility and E is the applied electric field? By substituting v_{eff} with the applied electric field and electron mobility in expression (2.21), it becomes:

$$I_{ds} = qn_s\left(\mu_e \frac{V_{ds}}{L_{DS}}\right) W_g \tag{2.25}$$

By rearrangement of Eq.(2.21), the derivation of the channel resistance R_{ch} using Ohm's law is obtained as:

$$R_{ch} = \frac{V_{ds}}{I_{ds}} = \frac{L_{DS}}{qn_s\mu_e W_g} \tag{2.26}$$

When the device is operated at a low drain voltage, electron velocity is proportional to the electric field strength ($V_{ds} < V_{gs} - V_t$) (linear mode). The effective electron velocity saturated and became independent of the drain bias at high drain biases where $V_{ds} > V_{gs} - V_t$ (saturation mode) is found. Due to electron scattering, velocity saturation (v_{sat}) occurs, causing the drain bias under the gate to start pinch-off the channel at the drain end of the gate limiting the further increase of the flow of current. This continues until the electrons are totally restricted by the channel, limiting the number of electrons within the channel, causing the device to operate in the saturation region. For further increase of electrons flow within the channel, the device/gate width must be increased from

a device design point of view. Alternatively, the expansion of the barrier thickness is also a possible solution to enhance the current flow from a growth design point of view. To attain high output powers operation, devices are typically biased at high drain voltages (in the saturation region). The drain current is estimated in this example by:

$$I_{ds} = \frac{\varepsilon_{AlGaN} v_{sat} W_g}{d_{AlGaN} + \Delta d} (V_g - V_t) \tag{2.27}$$

The DC transconductance of the HEMT device, $g_{m\text{-}DC}$ (G_m) is defined by the following expression:

$$g_{m-DC} = \left. \frac{\partial I_{ds}}{\partial V_g} \right|_{V_{ds} = constant} \tag{2.28}$$

In the saturation region, the transconductance can be given as follows:

$$g_{m-DC} = \frac{\varepsilon_{AlGaN} v_{sat} W_g}{d_{AlGaN} + \Delta d} \tag{2.29}$$

High $g_{m\text{-}DC}$ requires high saturation velocity and shallow depletion region depth, so the $g_{m\text{-}DC}$ is expected to decrease as depletion region width increases, i.e., with increasing the negative gate bias. On the other hand, $g_{m\text{-}DC}$ is directly proportionally increasing to the width of the device. Hence an increase in the device or gate width will directly result in an increase of the DC transconductance.

A TCAD simulation of a GaN HEMT device is performed using SILVACO to estimate its performance and the output current capable of delivering. The 2D device is illustrated in **Figure 2.13**, where the dimensions of the barrier layer thickness and the aluminum composition are set at 25nm and 25% respectively to imitate the wafers available at Cardiff University. Similarly, the device width is set at 125μm as a nominal value for subsequent fabrication steps to enable the use of Cardiff Model to extract the large-signal parameters.

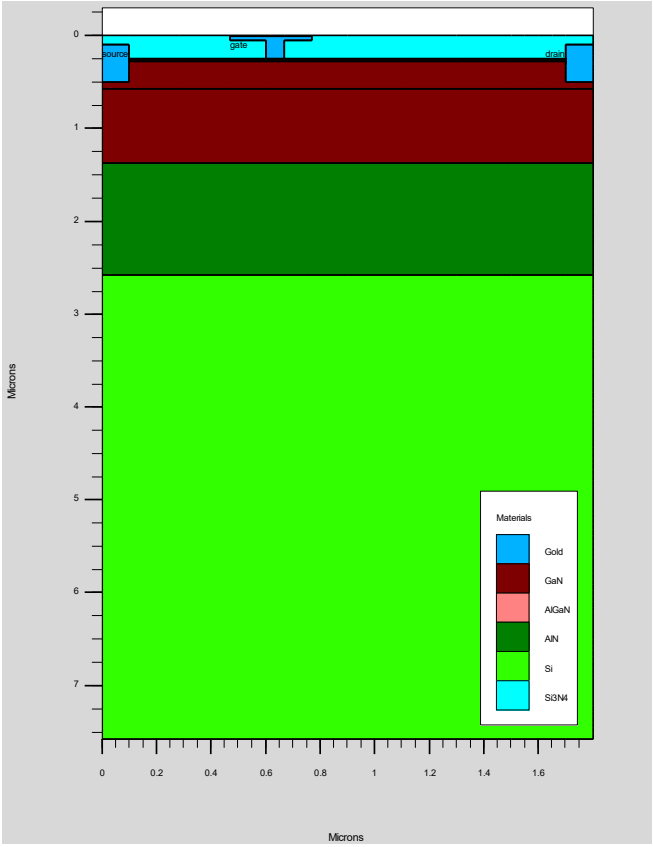


Figure 2.13. TCAD AlGaN/GaN HEMT simulation 2D layout with a device width of 125 µm

The normalised DC results of the simulation is depicted in **Figure 2.14**. The device has a maximum current of 760mA/mm when biased at V_{ds} = 10V and V_{gs} = 1V. Moreover, the highest DC transconductance is obtained at V_{ds} = 5V and V_{gs} = -2.6V with a value of 160mS/mm. Finally, the device has exhibited a well behavior of pinch-off at V_{gs} = -5V indicating a lack of drain to source leakage current when operating below the pinch-off of the device.

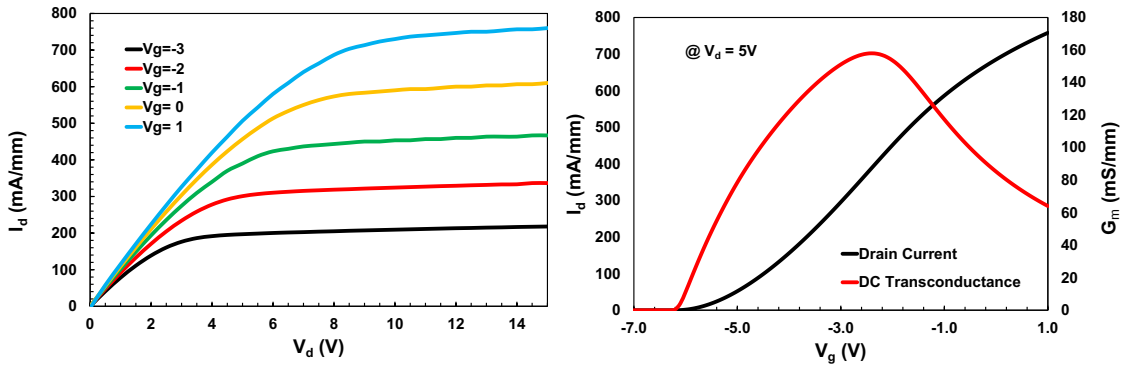


Figure 2.14. I_{ds}-V_{ds} family curves of a TCAD simulated 125 µm device of AlGaN/GaN HEMT and the transfer characteristics

2.7. High Frequency Operation

The measurement and assessment of scattering parameters are used in the high frequency study of HEMT devices (S-parameters). When an n-port network is introduced into a transmission line, S-parameters are linked to the travelling waves that are dispersed or reflected. The input port corresponds to the gate-source, and the output port corresponds to the drain-source in HEMT as illustrated in **Figure 2.15**.

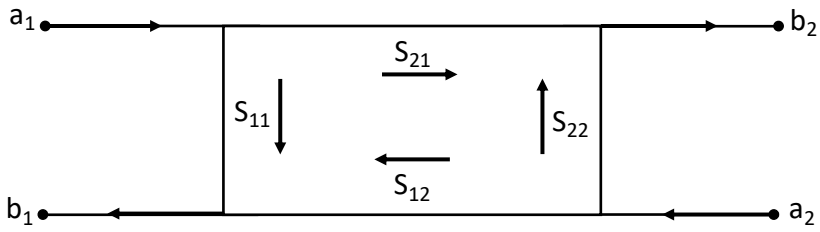


Figure 2.15. Two-port network S-parameters

The S-parameters in a simple 2-port network can be estimated using the following equations:

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2 = 0} \tag{2.30}$$

$$S_{21} = \frac{b_2}{a_1}\Big|_{a_2 = 0} \tag{2.31}$$

$$S_{12} = \frac{b_1}{a_2}\Big|_{a_1 = 0} \tag{2.32}$$

$$S_{22} = \frac{b_2}{a_2}\Big|_{a_1 = 0} \tag{2.33}$$

where $a_{1,2}$ and $b_{1,2}$ represents the incident and reflected waves at the input (left side) and the output (right side), respectively, as shown in **Figure 2.15**. The S-parameters are calculated as a function of frequency. S_{11} is the input reflection coefficient, which is the ratio of the reflected and the incident waves at the input port. S_{21} is the forward transmission coefficient related to the ratio between the reflected and incident waves at the output and input ports respectively. In contrast, S_{12} is the reverse transmission coefficient defined as the ration between the reflected wave at the input to the incident wave at the output port. Finally, S_{22}

is the output reflection coefficient measuring the ratio of the reflected and the incident waves at the output port.

The fundamental figure of merit required for RF device characterisation may be derived directly from the obtained S-parameters measurements. They are as follows:

1. Short circuit current gain (h_{21}):

$$h_{21} = \frac{I_{out}}{I_{in}} = \frac{-2S_{21}}{S_{21}S_{22} + (1 + S_{22})(1 - S_{11})} \tag{2.34}$$

where h_{21} is the forward transmission coefficient of a network expressed in hybrid parameters (H-parameters). It is also defined as the maximum current gain attained when the transistor output is short circuited to ground. This is useful to calculate the next important parameter as follows:

2. Current gain cutoff frequency (f_T):

$$f_T = f(h_{21} = unity = 0\ dB) \tag{2.35}$$

where f_T is the frequency at which the h_{21} coefficient, deduced directly from the measured S-parameters using Eq.(2.34), falls to unity or 0dB.

Furthermore, another important parameter is the transit time of electrons is related to the cut-off frequency where current gain, as aforementioned, falls to 0dB is given by:

$$\tau_T \approx \frac{1}{2\pi f_T} \approx \frac{L_{SD}}{v_{eff}} \tag{2.36}$$

3. Maximum available gain (MAG):

$$MAG = \frac{P_{ava}}{P_{in}} = \frac{\overbrace{S_{21}}^{MSG}}{S_{12}}\left[K - \sqrt{K^2 - 1}\right] \tag{2.37}$$

MSG is the maximum stable gain at the point where *K* is equal to unity. *MAG* is the maximum available power gain obtained by an ideal conjugate matching between the input and output ports. *K* is referred to as the Rollet's stability factor and it describes the stability of a transistor at the frequency range. *MAG* is only valid for $K \geq 1$ and it is given by the expression:

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}| \cdot |S_{21}|} \tag{2.38}$$

K factor indicates whether the device is unconditionally stable or conditionally stable (prone to oscillation if left without a stabilising network). When K > 1, the device is considered unconditionally stable, which means that oscillation is impossible regardless of the passive source/load network architecture. However, if K < 1, it indicates that the device is conditionally stable, i.e., stability depends on source and load terminations and network design.

4. Unilateral power gain (GU):

In general, transistors exhibit a reverse capacitance from the output toward input. *GU* considers only the power gain that is obtained by compensation of these reactive power parameter by introducing losses neutralisation mechanism. *GU* is calculated directly form the measured S-parameters and is given by:

$$GU = \frac{P_{out}}{P_{in}} = \frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{2\left[K \cdot \left|\frac{S_{21}}{S_{12}}\right| - Re\frac{S_{21}}{S_{12}}\right]} \tag{2.39}$$

This is useful to compute the next important parameter as follows:

5. Maximum oscillation frequency (f_{max}):

$$f_{max} = f(U = unity = 0\ dB) \tag{2.40}$$

where f_{max} is the maximum oscillation frequency at which the *GU* coefficient, deduced directly from the measured S-parameters using Eq.(2.39), falls to unity or 0dB.

Figure 2.16 illustrates a typical graphical representation of high frequency parameters extraction technique where the gains and the extracted figure of merits computed using Eq.(2.34) - (2.40) are plotted as a function of the operating frequency. This method is valid and can be directly computed from the measured S-parameters if the extrapolated figures of merits fall within the frequency range of the measurement's capability, which can extend to a maximum of 110GHz available at Cardiff High Frequency Center. However, beyond this limit of frequency measurement, a small signal model becomes essential to calculate the aforementioned figure of merits, which is to be explained in the next segment.

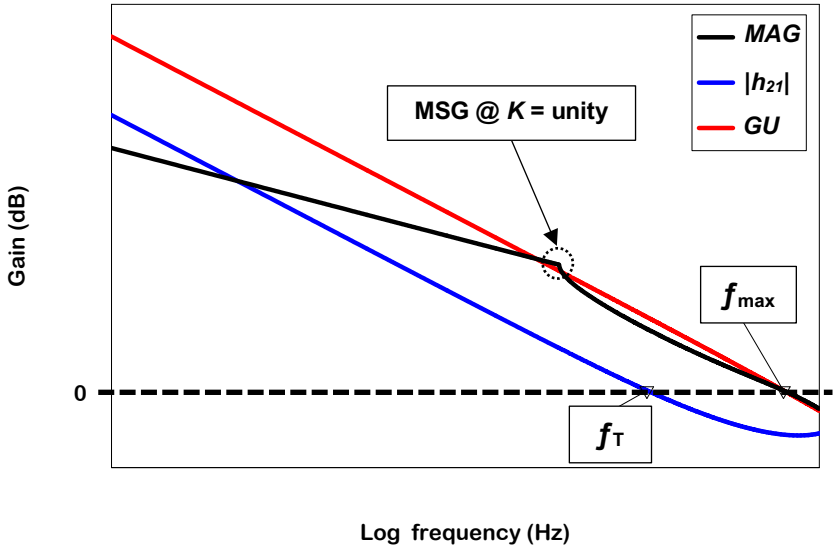


Figure 2.16. MAG, $|h_{21}|$ and *GU* as a function of operating frequency in log format

To accurately assess the fabricated device at high frequency, a de-embedding process is executed to remove the pads parasitic impedances from the device under test (DUT) as shown in **Figure 2.17**. A smile de-embedding method begins with three measurements, the embedded-DUT (eDUT), an open and short "dummy" structures of the pads without the device.

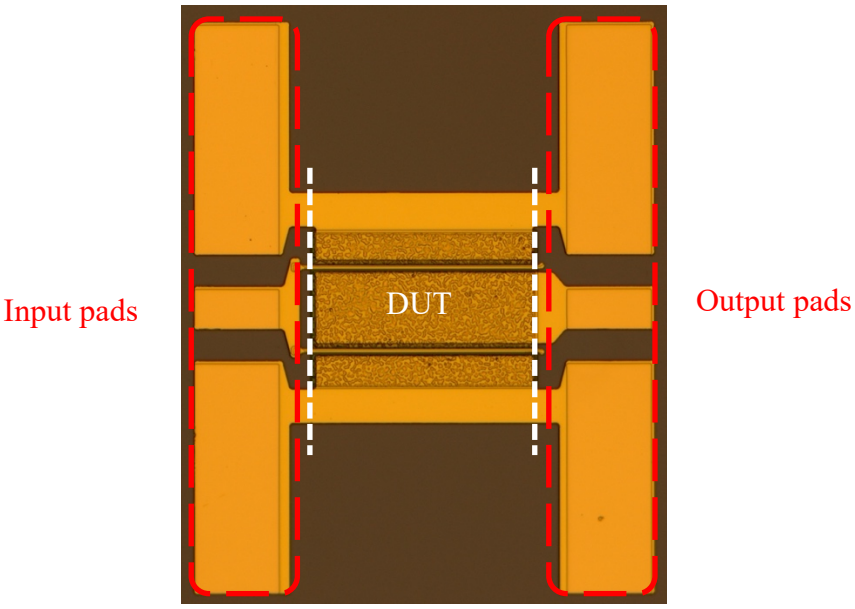


Figure 2.17. DUT and the input and output CPW pads

All measurements are initially stored in S-parameters format. This is followed by conversion to Y-parameters for the three measurements. The Y-parameters of the open fixture is then subtracted from the eDUT and the short measurements.

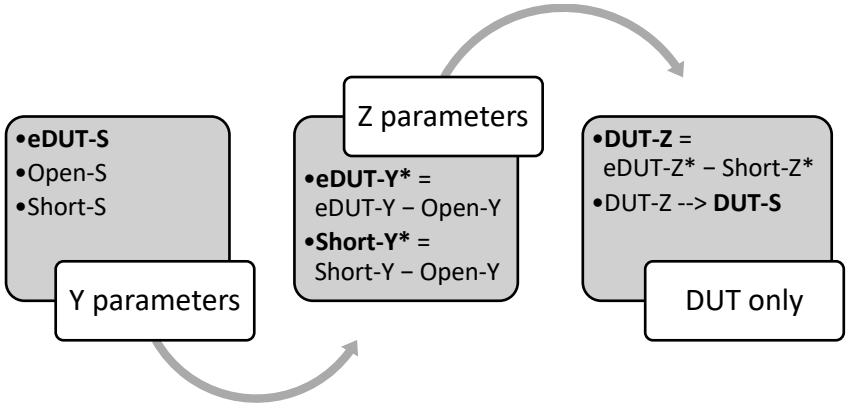


Figure 2.18. RF measurements CPW pads de-embedding process flow

Finally, the partial de-embedded data of DUT and short fixture are converted to Z-parameters where the latter is subtracted from the DUT resulting in a fully de-embedded data which is then converted back to S-parameters format for further mathematical manipulation. **Figure 2.18** summarises the process flow utilised in this project for de-embedding.

2.8. Small Signal Circuit Model

The drain and gate electrodes of FETs employed in MMIC amplifiers are typically biased with respect to the source in the common source mode. An RF signal is then injected to the gate electrode (input port), with an amplified version obtained from the drain electrode (output port). The design engineer in MMIC design is concerned with the equivalent circuit of the FET determined from RF measurements. Hence, only the values of the analogous circuit elements are determined by the DC bias conditions. The equivalent circuit is a simplification and abstraction of the HEMT that result in an electrical representation of the device that can be managed in circuit design software like Microwave Office.

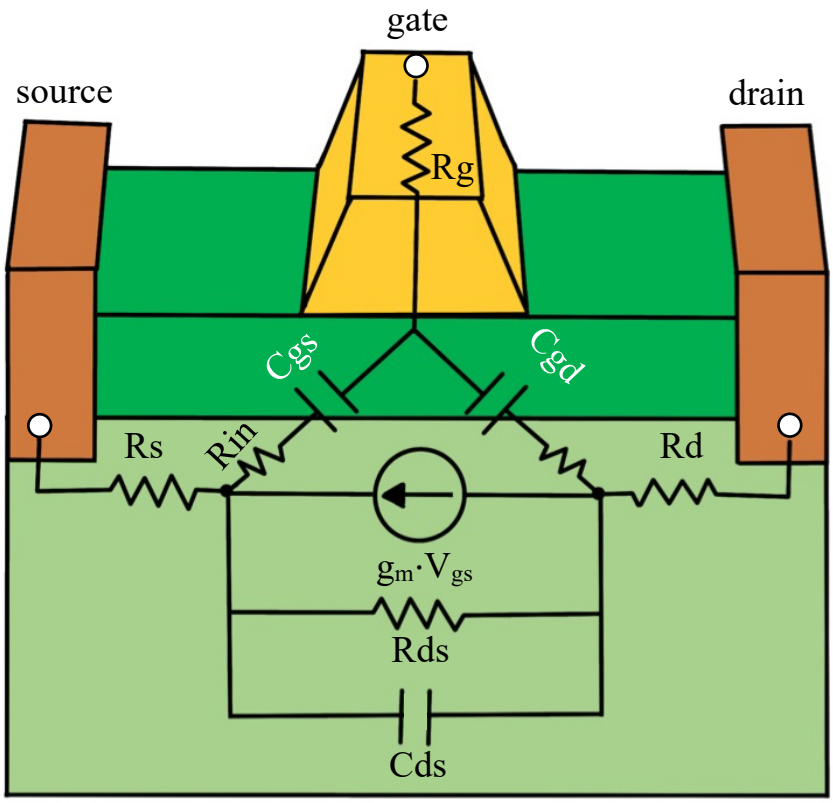


Figure 2.19. GaN HEMT device cross-section with the electrical network superimposed on the diagram

Figure 2.19 illustrates the entire electrical network superimposed on the cross-sectional view of the GaN HEMT device. Each element is designed to reflect the electrical character of a specific region of the device. For example, the lumped element R_g represents the metallurgical resistance associated with the gate. The fundamental equivalent circuit needed to illustrate the electrical behavior of the

physical structure of the FET at microwave frequencies is shown in **Figure 2.20**. The area of the HEMTs, which is physically located below the gate and the channel between the drain and the source, is defined as the intrinsic region located within the dashed box. The device's extrinsic (parasitic) elements are the remaining components outside the dashed area illustrated in **Figure 2.20**. Unlike intrinsic elements that are altered by the bias conditions, extrinsic components are bias-independent.

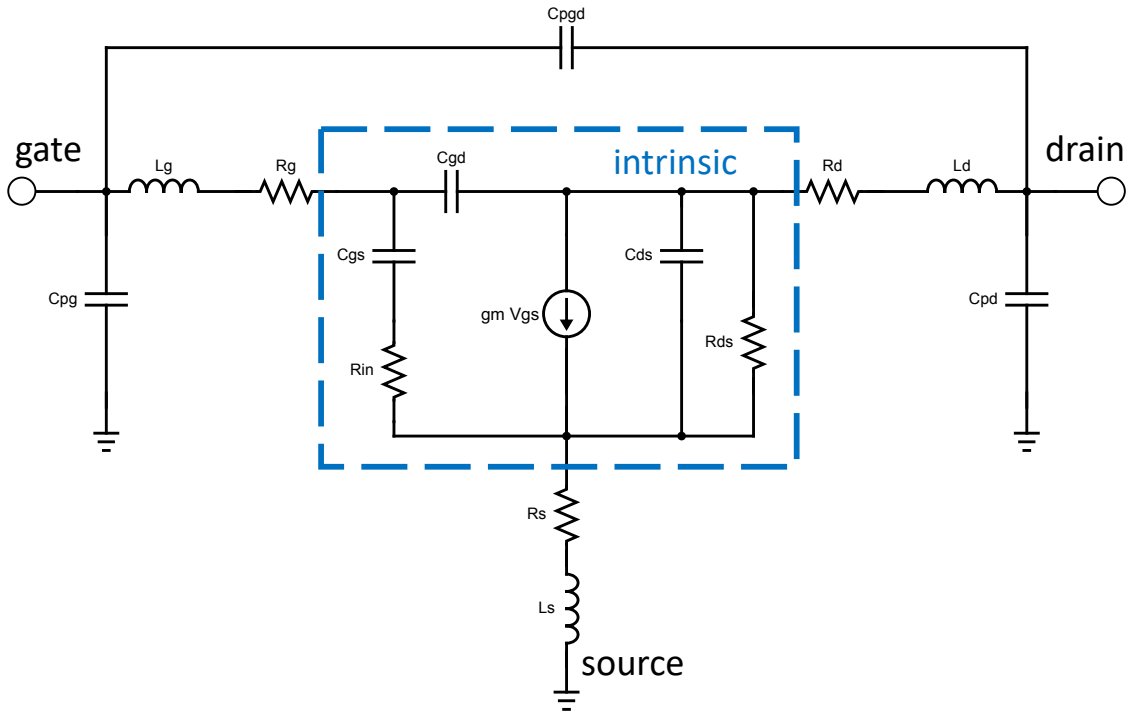


Figure 2.20. AlGaN/GaN HEMT's small signal model

The charge in the depletion area under the gate at the gate-source side of the device is represented by the gate-source capacitance (C_{gs}). The resistance of the semiconductor under the gate is represented by the channel resistance or input resistance (R_{in}) in series with C_{gs}. The capacitance of the gate drain C_{gd} is the capacitance associated with the charge created and modulated by the gate-drain voltage in the depletion area at the drain edge of the space-charge layer. The gain of the device is represented by the current generator $g_m \cdot V_{gs}$, where g_m represents the inherent transconductance and V_{gs} represents the voltage dropped across the gate capacitance. The device's finite output resistance is represented by R_{ds}. Because of dispersion, which is mostly due to charge

exchange with deep levels situated at the interface of the device channel and the buffer along with the surface charge trapping, the output resistance at microwave frequencies is frequently lower than the DC value. Because the states cannot follow the supplied voltage at high frequencies, the output resistance decreases linearly. The capacitive coupling between the drain and source separated by the depletion area (the depletion channel in-between them) results in the drain source capacitance (C_{ds}) in parallel with R_{ds}.

Figure 2.20 also shows the parasitic (extrinsic) parts of the corresponding circuit outside the dotted line. The source resistance (R_s) and drain resistance (R_d) of the series parasitic resistances each contain two components. First, there's the contact resistance component (R_c), which comes from the ohmic contact's resistance to the semiconductor. The semiconductor's second bulk resistance in the source-gate (or drain-gate) accesses areas. The number of gate fingers (m), the gate cross section area [gate length (L_G) x gate height (t_g)], and the gate width (W_g) determine the gate resistance (R_g). When multi-finger gates are combined in parallel, gate resistance is lowered by a factor of m^2, and the gate resistance is then given by:

$$R_g = \frac{\rho W_g}{3m^2 t_g L_G} \tag{2.41}$$

where ρ is the gate metal's resistivity and t_g is the gate fingers' thickness. The RF gate resistance is usually distributed, which results in a factor of three in the expression's denominator. The parasitic inductances L_g, L_d, and L_s, which emerge from the electrode feed pads, are gate, drain, and source parasitic inductances respectively. The configuration of the device determines the parasitic geometrical capacitances, C_{pg}, C_{pd}, and C_{pgd}, induced by the electrical field distributions between metallic contacts in a HEMT device. Now the aforementioned high frequency figure of merits (f_T, f_{max}, and MAG) can be estimated from the small signal model as detailed in the following segment:

1. Current gain cutoff frequency (f_T):

Considering only the intrinsic circuit shown in **Figure 2.20**, and by shortening the drain to the source i.e., $V_{out} = 0$. The current gain can be derived from the small signal model as:

$$I_g \approx j\omega V_{gs}(C_{gs} + C_{gd}) \tag{2.42}$$

$$I_d = g_m V_{gs} \tag{2.43}$$

$$h_{21} = \frac{I_{out}}{I_{in}} = \frac{I_d}{I_g} = \frac{g_m}{j\omega(C_{gs} + C_{gd})} \tag{2.44}$$

When the output drain current (I_d) is equal to the input gate current (I_g), the current gain falls to unity and the frequency at which this occurs is the cutoff frequency of the transistor and is given by:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}\Bigg| h_{21} = 1 \tag{2.45}$$

By considering the extrinsic patristics shown in **Figure 2.20**, the cutoff frequency can be evaluated as:

$$f_T = \frac{g_m}{2\pi\left[(C_{gs} + C_{gd})\left(1 + \frac{R_s + R_d}{R_{ds}}\right) + g_m C_{gd}(R_s + R_d)\right]} \tag{2.46}$$

2. Maximum oscillation frequency (f_{max}):

f_{max} is equal to the frequency at which the Power gain (PG) falls to unity. PG is defined as the ratio between the power consumed by the load and the power applied at the input of the transistor and is given by:

$$PG = \left(\frac{I_d}{I_g}\right)^2 \cdot \frac{R_{load}}{R_{input}} = (h_{21})^2 \cdot \frac{R_{load}}{R_{input}} = \left(\frac{g_m}{j\omega(C_{gs} + C_{gd})}\right)^2 \cdot \frac{R_{load}}{R_g + R_{in}} \tag{2.47}$$

where R_{load} is the output load resistance and R_{input} is the input resistance equal to the gate resistance (R_g) and FET intrinsic input resistance (R_{in}) as shown in **Figure 2.20**.

To obtain a maximum power transfer from the source to the load, the load resistance must be equal to the FET's output resistance (R_{ds}). In addition, by substituting for f_T as given in Eq.(2.45),the expression (2.47) can be rewritten as:

$$PG = \frac{1}{f^2} \cdot \left(\frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \right)^2 \cdot \frac{R_{ds}}{4\left(R_g + R_{in}\right)} = \frac{1}{f^2} \cdot (f_T)^2 \cdot \frac{R_{ds}}{4\left(R_g + R_{in}\right)} \tag{2.48}$$

Since the maximum oscillation frequency takes place at unity power gain, it can be defined as:

$$f_{max} = \frac{f_T}{2\left[\frac{R_g + R_{in}}{R_{ds}}\right]^{1/2}} \tag{2.49}$$

Taking into consideration the extrinsic parasitic effects, f_{max} can be rewritten as:

$$f_{max} = \frac{f_T}{2\left[\frac{R_g + R_{in} + R_s}{R_{ds}} + (2\pi f_T R_g C_{gd})\right]^{1/2}} \tag{2.50}$$

3. Maximum available gain (MAG):

Final RF figure of merit calculated from the small signal model is the maximum gain available assuming a perfect match between input and output, which is given by the following expression:

$$MAG = \frac{\left(f_T/f\right)^2}{4\left(\frac{R_g + R_{in} + R_s}{R_{ds}}\right) + 4\pi f_T C_{gd}\left(2R_g + R_{in} + R_s\right)} \tag{2.51}$$

2.9. Large Signal Characteristics

AlGaN/GaN HEMTs are primarily designed for high-frequency power applications. The maximum power level that may be achieved, as well as the accompanying gain, is the most important parameters that a power device must consider. Large drain breakdown voltage, high gain at high frequencies, and good drain efficiency are all desirable for this. The basic device geometrical elements that are required to determine the current voltage characteristics must first be

defined, just as they must be established in small signal modelling. Once they are determined, the output characteristics overlaid on the load line may be used to estimate the power level that can be generated from the device, assuming it is not limited by the input drive, as shown in **Figure 2.21**. The operating point on IV characteristics, around which the AC microwave signal swings, is significant. The maximum power that may be expected from the device's drain circuit in Class-A operation is given by:

$$P_{max} = \frac{I_{dss}}{8}(V_B - V_{knee}) \tag{2.52}$$

where I_{dss} is the maximum drain current, V_B is the drain breakdown voltage, and V_{knee} is the knee voltage as shown in **Figure 2.21**. The DC load line plotted on **Figure 2.21** would be utilised in a Class-A, for example, RF amplifier with maximum drain voltage $V_d = \frac{V_B}{2}$. The slope of the load line is $\frac{1}{R_L}$ where R_L is the value of the load resistance at the output of the HEMT.

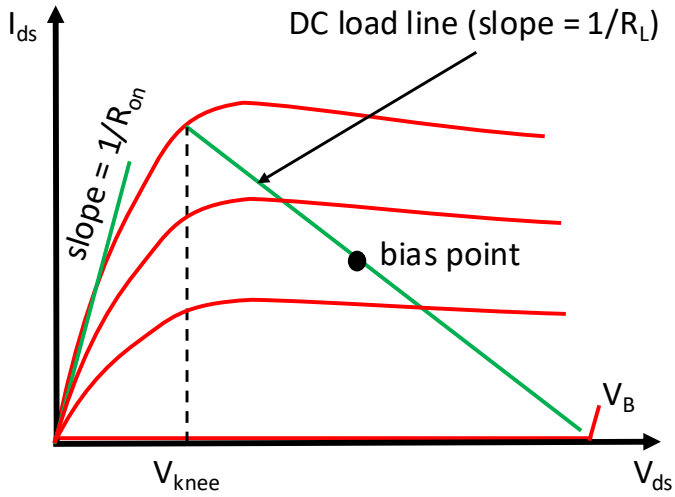


Figure 2.21. AlGaN/GaN HEMT output I-V characteristics with class-A power amplifier DC load line

The values of V_B and I_{dss} must be as large as feasible to produce high power, as shown in Eq.(2.52). GaN devices have a higher breakdown voltage than traditional III-V semiconductors. Larger breakdown voltage and thermal conductivity, as well as the capacity to endure greater junction temperatures, result in increased power handling capabilities. The breakdown voltage may be

effectively regulated by adjusting the source-to-drain distance L_{SD}, with greater L_{SD} resulting in increased V_B. A larger L_{SD} increases source to drain resistance and moves V_B to higher values, which has a detrimental impact on maximum output power. Additionally, the cap layer below the gate has a strong influence on the breakdown voltage. Finally, the power added efficiency (PAE), which is defined as the ratio between the total power consumption of the device to the output RF power, can be estimated using the following expression:

$$PAE = \frac{P_{RFout} - P_{RFin}}{P_{DC}} \tag{2.53}$$

where P_{RFout}, P_{RFin} and P_{DC} are the RF output power, the RF input injection and the supply power used to bias the drain, respectively.

3. GaN HEMT Fabrication Techniques and Process

This chapter details the methods and tools utilised in this project to carry out the fabrication of GaN HEMT devices and technologies including passives and actives. These methods include material growth, metal patterning, etching lithography and film deposition technique are all defined in this chapter. GaN on Si based material grown and supplied by Cambridge Center for Gallium Nitride, Cambridge University. Device fabrication is conducted at the Institute for Compound Semiconductor cleanroom and device characterization at the Center of High Frequency Center Engineering (CHFE), Cardiff University.

3.1. Material Growth and Design

The substrate structure used to fabricate the active and passive device for this project depicted in Figure 3.1. The wafers, from surface of the structure, comprises of a 2nm GaN cap to manage the stress on barrier layer, a 25nm AlGaN with Al fraction of x = 0.25 to target an n_s value of ≈ $8x10^{12}$ cm^{-2}, and finally 1nm spacer to further control the 2DEG density. The wafers share identical channel layer (250nm GaN), buffer (750nm unintentionally doped GaN and a 1.7µm AlGaN Fe-doped to ≈ 10^{18} cm^{-3} with a decay to $5x10^{16}$ cm^{-3} at the 2DEG) and a nucleation layer (180nm AlN). The epi-layers structures are grown on two different types of 675µm thick and 150mm diameter substrates namely, p-type low resistivity (LR), and carbon-doped high resistivity (HR) silicon substrates. The latter is more desirable due to its advantage of reducing substrate conductivity and suppressing any associated coupling especially at high operational frequency leading to a loss of signal power. The wafers were crack-free with a concave bow less than 30µm after cooling from growth temperature of 1100°C. The GaN (002) and (102) X-ray rocking curve FWHMs were < 650 and < 900 arcsecs, respectively, indicating a satisfactory crystal quality of the graded buffer layer.

Figure 3.1. GaN on Si wafer structure used in this project for HEMTs. *Epi layer of the shown structure was designed by Prof. David Wallis.*

The MOCVD grown wafers were characterised by Van der Pauw (VdP) process control management structure (PCM) as illustrated in **Figure 3.2**. The material was evaluated using Hall measurement to extract Hall electron mobility (μ_e), sheet resistance (R_{sh}) and carrier density (n_s) using expressions (3.1) and (3.2). To achieve a high-quality material suitable for HEMT devices, an optimal R_{sh} value of 400±50 Ω is required. This target of sheet resistance determines the acceptance criteria of each layer of the materials provided. Besides the marker level, two steps of photolithography were used to fabricate VdP PCM in this project. The first one was applied to etch the conductive layers (with a depth of 100nm or deeper to ensure the complete removal of the active layer), thus creating an isolated mesa for VdP square patterns to be deposited on the next. Then, ohmic level was aligned on top of the mesa followed by an ohmic level metal deposition and annealing at 800°C.

$$n_s = \frac{1}{q.R_H} \tag{3.1}$$

$$\mu_e = \frac{R_H}{\rho}, \ \rho = R_x.t \tag{3.2}$$

where q is the electron charge, ρ is the resistivity extracted from adjacent VdP measurements, R_x is the longitudinal resistance (equal to R_{sh}, assuming square VdP patterns), t is the metal-stack thickness and R_H is

the Hall resistance extracted from diagonal measurements of VdP patterns.

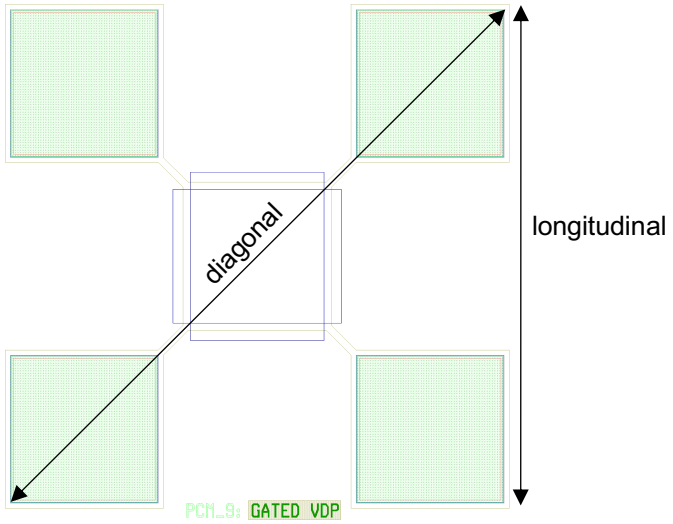


Figure 3.2. Gated VdP test structure

Hall electron mobility (μ_e), sheet resistance (R_{sh}) and carrier density (ns) measured at 300k in the light using a Bi-Rad Polaron HL5200 Hall measurement system for wafers used throughout this project are summarised in Table 3.1.

Table 3.1. VdP parameters and measurements of GaN on Si used in this project

	Wafer #	d_{2DEG} (nm)	Substrate	R_{sh} (Ω/□)	μ_e ($cm^2/V{\cdot}sec$)	n_s (cm^{-2})	Bow (μm)
A	EU2001014	28	p-Si (111)	425	1700	8.1E12	-20

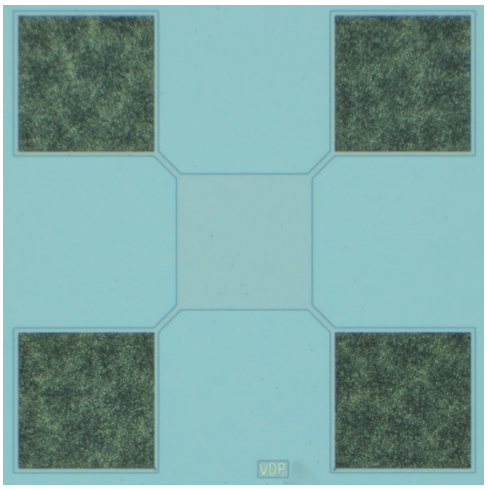


Figure 3.3. VdP structure after processing mesa etch

3.2. Lithography

Lithography is the process of transferring desired patterns onto the surface of wafers using a mask in case of UV light photolithography or through a writing file loaded directly to the machine as in the case of electron beam lithography (EBL) and laser lithography.

3.2.1. Photolithography

Photolithography or optical lithography is the process of using UV light to alter the solubility of a photo-sensitive resist where under the influence of developer, this alteration either becomes dissolvable for positive photoresist or indissoluble when using negative photoresist. The UV light is passed through a photomask containing the desired patterns, which as a result are transferred onto the surface of the substrate for further processing such as metallisation or etching. Although photolithography is used for relatively large feature size ≥ 1μm with an alignment accuracy ≥ 0.5μm, it does offer a faster process since all patterns are exposed and developed simultaneously. Hence, photolithography is ineffective for submicron feature sizes with high precision of alignment. Furthermore, an important control parameter of photolithography is the exposure time, which dictates the development quality to avoid over or under development issues, and can be computed using the following expression:

$$Expose\ Dose\ (sec) = \frac{Exposure\ energy\ (mJ/cm^2)}{Lamp\ intensity\ (mW/cm^2)} \tag{3.3}$$

where exposure energy is obtained from vendor, datasheet or iterative trial and error. Lamp intensity is measured directly by presenting an optical power meter to the UV light source and reading off the obtained value.

All pattern steps in this project are photolithography based except the gate foot/trench level where EBL is used to obtain smaller feature sizes of 250nm.

3.2.2. E-beam Lithography

Unlike photolithography, no physical mask is needed, instead the design file is directly loaded to the system to control the stream of the electron beam, also uses a different resist than photolithography, which is sensitive to electrons rather than ultraviolet light. Furthermore. Although it is a slow process, it is advantageous in three aspects, resolution, which translates to small feature size in the order of a few nanometers, superior alignment accuracy, and finally, flexibility which translates to ease of design modifications due to the lack of physical mask prerequisite. In EBL, three control parameters which affect the process, charge dose per area ($\mu C/cm^2$), beam current (nA) and the resolution (a fraction of the minimum feature size in nm). It is worth noting that a thin metallic discharge-layer such as aluminum (Al) or copper (Cu) is a necessary step, deposited after e-beam resist is spun and baked to create a ground path for the accumulated charge on the surface of the substrate to prevent electron repulsion and avoid an arbitrary misalignment.

3.3. Metallization and Lift-Off

Metal deposition or metallisation is the process of depositing metal on a predeveloped substrate to form the designed patterns. This is the most crucial step through which the contact between a metallic electrode and the semiconductor is formed. Hence, it dictates the quality of the device and the operating performance. Also, since metalisation requires a few control factors such as vacuum level, temperature, thickness, and type of metal. It is more prone to failure within the fabrication than other steps especially for ohmic contacts. In

this project, three techniques are used, evaporation, sputtering and electroplating.

3.3.1. Evaporation

Metal evaporation is directional deposition method operates by heating up a metallic source to a specific temperature at which the metal evaporates thermally by means of resistive or electron beam heating. In the former, a current is passed through a crucible that mimics the behavior of an electrical resistor, dissipating power in the form of heat as current flow through it, which in return heats up the metal to a desired temperature to evaporate. On the other hand, electron beam evaporation current is initially routed through a tungsten filament, which causes a joule heating and electron thermionic emission. Between the filament and the hearth, a high voltage is applied to drive the released free electrons towards the crucible containing the metal to be deposited. The electrons are then, focused into a cohesive beam by a high magnetic field, and the energy of this beam is transmitted to the deposition material, causing it to evaporate and deposit onto the substrate. If the desired deposition material is metallic, a vacuum condition is required to refrain the metal from becoming an insulator. However, if non-metallic layer of deposition is needed then a pressure is introduced into the chamber with a gas of choice such as nitrogen and oxygen.

The benefits of using electron beam evaporation over resistive thermal evaporation are various. For example, an e-beam source could heat the materials to considerably greater temperatures than a resistive boat or crucible heater is. This enables the deposition and evaporation of high-temperature materials and refractory material such as tantalum, tungsten, and graphite at extremely faster rates. Secondly, films formed by electron beam evaporation exhibit higher purity of the source material resulted from the water cooling of the crucible, which translate to a more of a controlled heating to the source, preventing contamination from adjacent source of the crucible itself. Finally, in electron beam evaporation, a single source comprises of several pockets allowing a deposition of different materials from a single source at the same run without the need of pumping and venting the chamber for material change.

Due to the relatively slow and precise deposition rate (< 500pm/sec), metal evaporation is predominantly used for thickness below 1μm and when a highly pure metal layer is required in a directional form of deposition. Thickness beyond 1μm, metal evaporation is impractical, time consuming and thickness management becomes a challenge. As illustrated in Figure 3.4, the process begins with loading the wafer/sample into the chamber of the machine. After that, the chamber is pumped to a vacuum level of 10-8 mbar. Once the desired vacuum level is reached, the electron beam is switched on to heat the metal. As soon as the electron gun is switched on, metal evaporation is obtained. Therefore, a shutter is used to protect the wafer until the required rate of deposition is achieved. The shutter is then opens and the metal is deposited onto the substrate and metal thickness is monitored by a quartz crystal microbalance thickness monitor. Once the desired thickness is acquired, the shutter closes, and the metal is gradually cooled off to avoid splatter and crucible shatter. Finally, the chamber is vented to room pressure and the sample is offloaded for further processing.

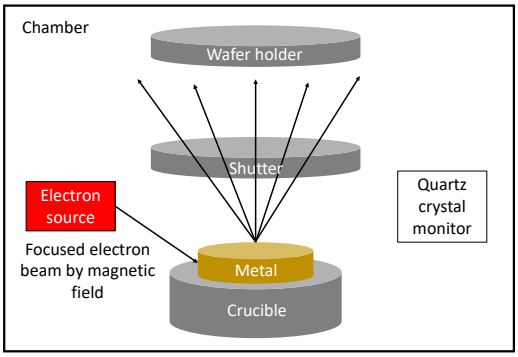


Figure 3.4. Electron beam evaporation metallisation tool

3.3.2. Metal Lift-Off Process

This is a standard technique for selectively pattering a wafer with metal structures. For a thin film deposition, metal lift-off is generally performed in a bi-layer photoresists with different density for undercut profile. The bi-layer lift-off procedure is illustrated in **Figure 3.5** as follows:

1- Spin and coat the first photoresist with lower density than the succeeding second layer of photoresist, this ensures an undercut

profile which is acquired with an overhang profile resulting in a discontinuity of the deposited metal, and thus improving the reliability of the metal lift-off process.

2- Spin and coat the second layer of photoresist with a higher density.

3- Expose with UV light with a photomask which passes the light through its clear glass to alter the resist solubility corresponding to the desired patterns on the mask.

4- Develop in a solution to remove the resist and expose the patterned substrate.

5- The substrate is exposed and ready for the subsequent metal deposition. It is important to descum the surface to ensure the complete removal of any residue of the photoresists.

6- After surface deoxidisation (this is greatly a critical step for ohmic process in particular), deposit the metal with the required stack using evaporation tool.

7- After metallisation, the substrate is immersed into a stripper or acetone solution, where the unexposed photoresist is dissolved, and the metal situated on top of it is lifted off.

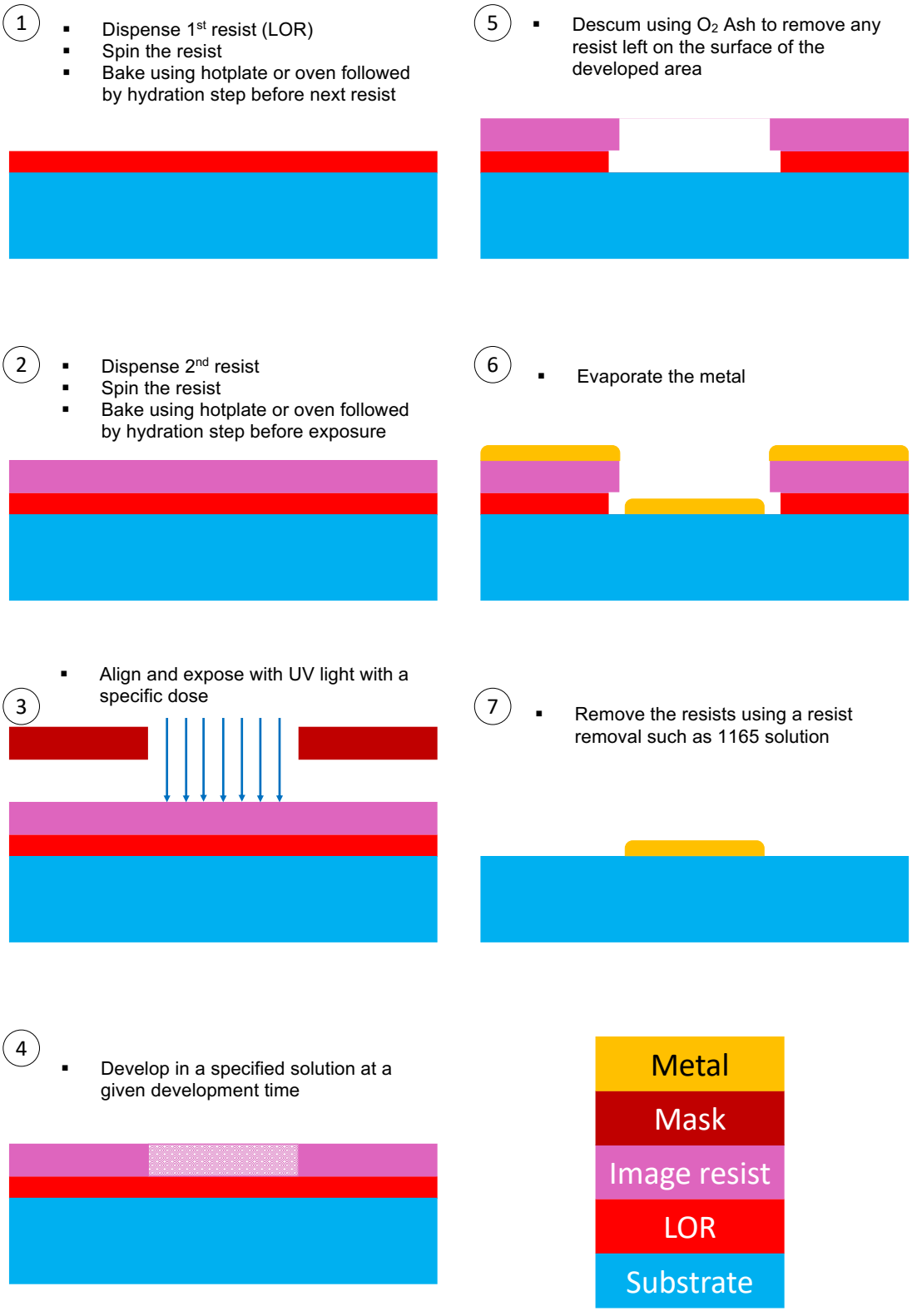


Figure 3.5. Pattern transfer process using bi-layer positive resists and lift-off

For high reliability of metallisation and lift-off, the deposited metal thickness must be less than the thickness of the first layer of the photoresist with the lower density characteristic to ensure the overhang the discontinuity of metal to enhance lift-off process.

3.4. Rapid Thermal Annealing

Rapid thermal annealing (RTA) is the process of heating up a sample to an extremely high temperature for a short amount of time with the purpose of diffusing ohmic contact into the active layer to reduce the contact resistance and the bandgap between the semiconductor and the electrode. This process of electrical properties alteration is performed in an ambient environment filled with a specific gas to form the desired alloys such as titanium nitride (TiN) in the case of standard HEMT ohmic contact metal stack-up (Ti/Al/X/Au, where X can be Ni, Mo, Pt, Ta, Ir, etc.) [128], which will enhance the ohmic performance by the betterment of electron flow from the 2DEG to the contact. The main control parameters are the temperature and the time duration of RTA. It is worth noting that after RTA process is complete, the temperature should be slowly decreased to prevent a potential thermal shock of samples, which can translate to dislocations and cracking of the samples. In this project, an RTA temperature of 790°C is applied for ohmic contacts formation.

3.5. Etching

This is a standard process of pattern transfer where the substrate is selectively etched via windows in the photoresist defined by UV light radiation exposure and development. The procedure is illustrated in **Figure 3.6** as follows:

1- Spin and coat the substrate with photoresist.

2- Expose with UV light with a photomask which passes the light through its clear glass to alter the resist solubility corresponding to the desired patterns on the mask.

3- Develop in a solution to remove the resist and expose the patterned substrate.

4- The substrate is exposed and ready for the subsequent etching process.

5- Etch to physically remove the substrate in the exposed area.

6- Dissolve the unexposed photoresist in acetone.

There are two methods of etching a substrate: dry and wet, where the etchant used is either gaseous or liquid solution, respectively. Unlike wet etch where etching occurs in an isotropic manner through chemical reaction, dry etch is the preferred method for etching GaN material as it is more controllable, especially with the sidewall profile due to the anisotropic etching nature of dry etching.
Dry etching is a standard process of pattern transfer where the substrate is selectively etched via using excited ionic matters to bombard the exposed area of surface causing to dislodge from the surface. The ions are energised either by means of plasma and reactive gases such as argon and oxygen.

3.5.1. Reactive Ion Etch

Reactive ion etching (RIE) is a form of a dry etching in which a single RF power is used to create plasma in a vacuum chamber and determining the plasma energy and density. The stripped electrons from the atoms of the gases are accelerated within the chamber striking its wall and partially accumulating at the surface of the substrate, thereby negatively charging it. The wall of the chamber is grounded to flush the excess electrons collected at the wall to prevent ions attraction. The positively charged ions, then, attack the substrate due to the electrostatic attraction; and chemically react with the exposed surface which dislodges material at a rate of approximately 100nm/min.

3.5.2. Inductively Coupled Plasma

Inductively coupled plasma (ICP) process is like RIE, but with an extra ICP power to control the ions density in the chamber. In other words, two separate power sources are used to determine the plasma energy and its density. This addition of ICP power source allows for a higher etching rate of up to 500nm/min and higher. However, ICP etching could lead to a surface damage of GaN if the powers applied are not managed properly, which can lead to an imbalance between the physical and chemical aspects of the process.

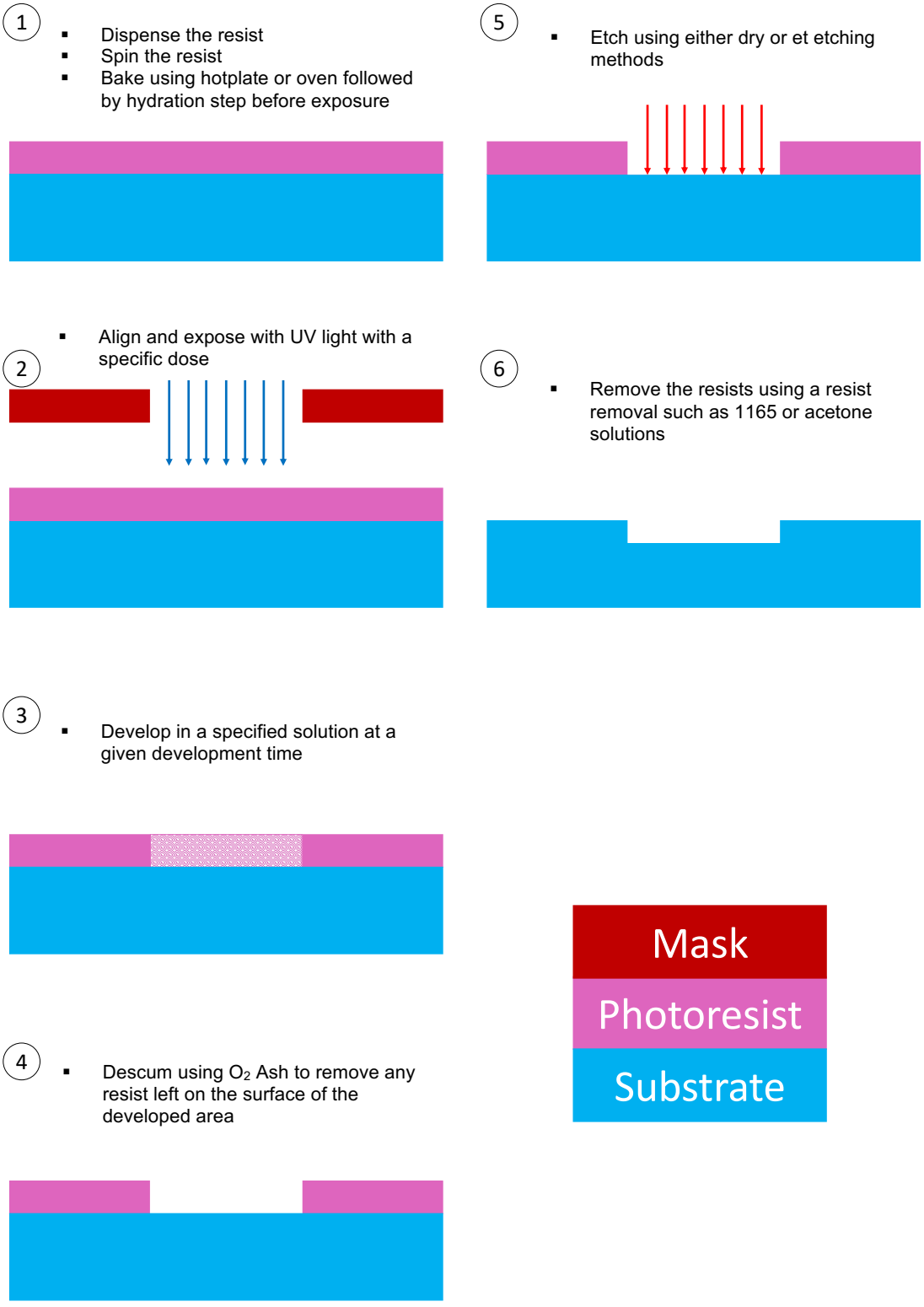


Figure 3.6. Material-etch process schematic diagram

3.6. Dielectric Deposition

Dielectric deposition is utilised in this project to insulate different electrodes to prevent any short circuit between them, and to passivate devices for protection reasons from the atmospheric environment. The method employed throughout this work is plasma enhanced chemical vapor deposition (PECVD). The process begins by placing the substrate on platen in the chamber. The chamber is then pumped to about 1mbar of pressure to clean the environment within the chamber. Next, gases are flown inside the chamber through the gas input source. Once chamber filled with gases and the pressure is stabilised, the RF electrode is switched on to ionise the molecules of the gases. These molecules are then deposited as thin film on the substrate. The deposition rate is constant and only the time duration is the control parameter to acquire the desired thickness. The RF power is turned off and the gas flow is stopped once required thickness is achieved. The chamber is then vented to room pressure before it can be opened, and the substrate is retrieved. The main advantage of PECVD is that it operates at a relatively low temperature of 300°C, which is critical consideration to avoid diffusion of metal such as the gate metal where the Schottky behavior of the gate is altered under high temperature deposition environment.

3.7. Substrate Preparation

Devices were fabricated on one-inch square dies (25x25 cm^2) diced from a full 6” wafer. This enables for excess of material at hand for further fabrication and ease of processing. Sample cleaning is an essential step which is performed before fabrication commences. The cleaning and degreasing of each sample are achieved using 5min of ultrasonic agitation in each of Trichlorethylene, 1165 stripper and Isopropyl Alcohol (IPA). The sample is then blown to dry by a nitrogen gun and immediately coated with photoresists in preparation for fabrication of the first step, which is the alignment markers level.

3.8. Layout Design and Fabrication Process

For the layout design, a computer aided design (CAD) software was utilised to generate the device various levels of process hierarchically to produce the photomask and the writing data for photolithography and e-beam, respectively.

As depicted in **Figure 3.7**, each mask is about 22cm square, and it comprises of four unique cells with respect to HEMT gate length and the corresponding aspect ratio. Only one of the cells (identified with an “O-PL” tag) is entirely photolithography-based including the gate trench level, which was set, lengthwise, at the photolithography minimum feature size capability (1µm). The remaining three cells are dedicated for the submicron gate length with different aspect ratios. After an iterative process of troubleshooting the layout, the photomask is realised to be used in the fabrication of the different levels of the device starting with the markers.

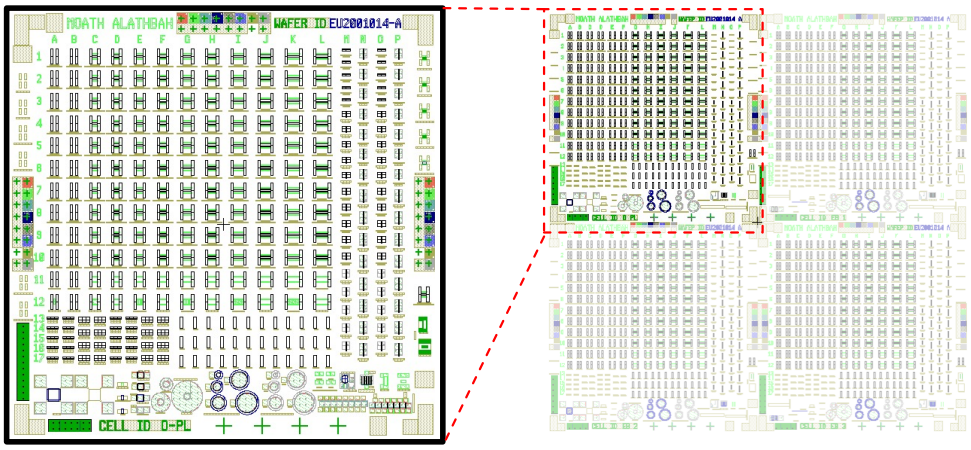


Figure 3.7. Full mask layout of devices and PCMs

3.8.1. Alignment Markers

Since the device fabrication comprises more than one level and an alignment precision of less than 500nm, alignment markers are essential to produce well aligned, reproducible devices with high yield and optimised performance. As illustrated in **Figure 3.8**, two groups of alignment markers used in this project, preprocessing markers which are utilised as a reference point for the subsequent lithography level (optical and e-beam). The other one, known as vernier, is postprocessing markers used to assist with the fabrication quality and control inspection of optical lithography process exclusively.

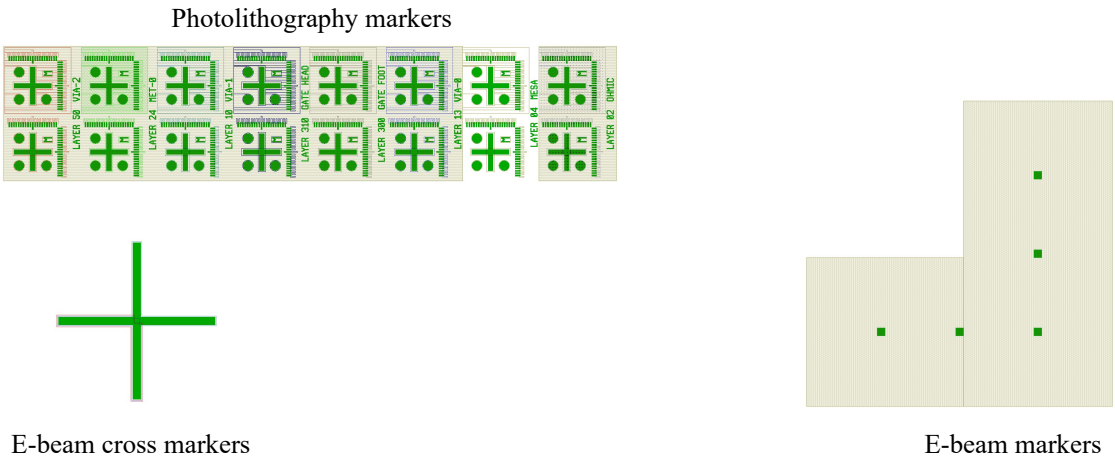


Figure 3.8. Alignment markers for photolithography, e-beam and vernier for post-process alignment inspection.

Alignment markers which is level one on the fabrication sequence, is performed using the metal and lift-off technique. The metal/metals applied for alignment markers require a few factors to be considered when processing excellent adhesion to the surface, heat withstand for smooth morphology and high metal to background contrast. The latter is especially of importance for the e-beam markers since alignment is performed automatically, the metal must be reflective of the light and have a contrasting color to the background for clearer visibility such as Au or Pt. Secondly, the metal must endure a high temperature annealing environment and maintain its integrity such as surface morphology and edge acuity. Finally, the metal must be strongly adhesive to the surface of the wafer and is chemically and mechanically stable to tolerate the various fabrication process steps. Hence, a bi-layer metal (Ti/Pt) is commonly opted for GaN HEMT process to acquire all these factors with bottom metal layer dedicated merely for the adhesion requirement. More metallic layers can be added in the case where the first level of a particular device lithography is integrated with the markers level such as the bottom plate of a MIM capacitor. In this case, the thickness of the metal becomes an additional factor of consideration at the markers level. Moreover, each level of fabrication has a unique marker to a further improvement of the alignment process and e-beam registration.

The process of alignment markers begins with cleaning the sample as mentioned in substrate preparation section for the subsequent bi-layer metal lift-off process.

After that, an LOR-3A is coated onto the surface, treated, and baked. Spinning the LOR-3A at a speed of 6k rpm ensures a uniform resist distribution which results in a thickness of 250-300nm across the surface of substrate. Hence, the deposited metal thickness must be <250nm to guarantee the presence of an overhang and a metal discontinuity for ease of lift-off. Then, the second layer of photoresist (S1805) is spun and backed as well. Next, depending on the light power intensity measured beforehand, the sample is exposed with UV light for 8 seconds calculated using Eq.(3.3). The patterns are then developed for one and a half minute in MF319 solution. The sample is then rinsed with deionised water (DI) to ensure the complete removal of the developer solution. Prior to metallisation, an O_2 plasma aching is performed to remove any resist residue and to oxidise the surface for further adhesion improvement. After metal deposition by evaporation, a lift-off is performed as detailed in the metal lift-off section to dissolve the unexposed resist with the metal deposited on top. An excellent alignment is obtained with an accuracy less than 0.5μm as shown in **Figure 3.8**.

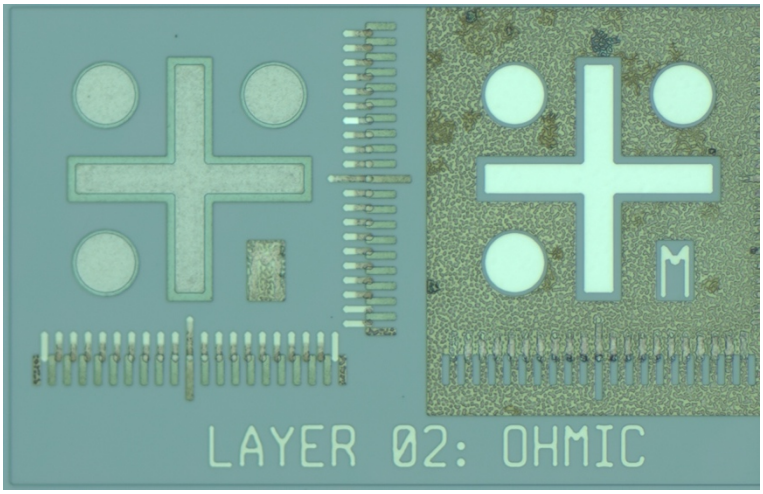


Figure 3.9. Post-ohmic microscopic image of alignment markers, shown < 0.5μm alignment.

3.8.2. Ohmic Contacts

The formation of low resistance ohmic contact is critical to the optimised performance of a GaN HEMT device. Therefore, the fabrication process of ohmic contacts poses the highest challenge among the HEMT fabrication levels because it involves several vital steps, such as surface deoxidisation, adhesion,

metal deposition and diffusion. Thus, each of these steps requires a significant consideration to deliver a working device with a high current output capability.

The TLM test structure was used to extract the ohmic parameters such as the contact resistance (R_C) and the transfer length (L_T) using the Semiconductor Parameter Analyzer and DC needle probes. The LTLM test structures were fabricated at various locations across the sample to evaluate the process uniformity and the material quality. The pads were shaped in squares with a width of 150μm with designed gaps between the contacts of 2.5, 3.5, 4.5, 5.5, 10.5, 15.5 and 20.5 μm. As shown in **Figure 3.10** illustrates the layout configuration of the LTLM that was used to extract the parameters of the ohmic contacts.

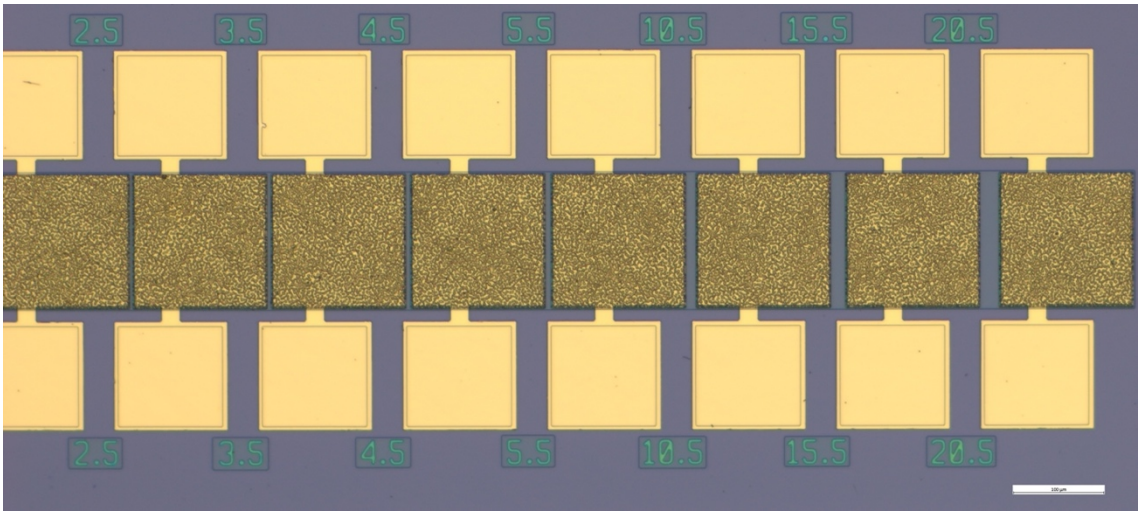


Figure 3.10. Conventional LTLM

A 4-point probe method was applied to acquire the value of R_C, two probes passed the injected current between the adjacent pads while the other two probes measured the voltage drop across them. From Ohm's law (R=V/I), the total evaluated resistance was plotted as a function of gap size with a linear fit line of the data. The intercept with the vertical axis reads $2R_C$ while the horizontal intercept is equal to $2L_T$. Furthermore, the slope of the plotted fit line represents the sheet resistance (R_{sh}) per the width of the pads. The typical TLM measurement is illustrated in **Figure 3.11**.

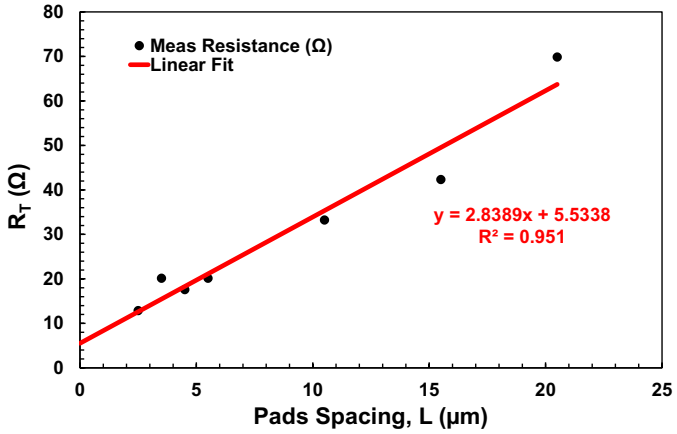


Figure 3.11. Ohmic contact measurement

To put the contact resistance into prospective, and for simplicity of comparison, it is commonly multiplied by the width of the pads and quoted in Ω·mm unit. The transfer length represents the distance from the gap through which the current is transferred via the pads. The results of the TLM measurements for all wafers fabricated during this project are summarised in **Table 3.2**.

Table 3.2. TLM structure contact resistance and length transfer

	Conventional LTLM	
Wafer	**R_C (Ω·mm)**	**L_T (μm)**
A	0.42	0.97

3.8.3. Device Isolation

Device isolation is a standard process applied for the purpose of limiting or minimising the electrical effects of the devices on adjacent ones and thereby influencing the overall operating parameters leading to false characterisation and an overestimation of their performance. This is accomplished by having a minimum separation distance between devices and the alteration or the complete physical removal of the conductive layers between them. In this work, the minimum separation distance was set to 300μm and 200μm for RF and DC devices, respectively. Additionally, the other component of the isolation effort is achieved by physically removing the conductive layer well below the 2DEG distance or by damaging the layer to deplete the 2DEG resulting in an increase

of the resistance of the layer between devices, i.e., ion implantation. The former, known as a mesa isolation, is commonly used due to simplicity of process and cost-effective purposes.

Mesa Isolation:

Mesa isolation is the most common method used currently to remove layers of semiconductor between adjacent devices. In this project, a typical etch target depth is in the range of 100-200nm, which ensures the entire removal of the barrier and the channel layers down to the buffer layer. Since GaN has a strong ionic bond, wet etching is ineffective. Therefore, dry plasma etching technique is applied. Although dry etching is relatively a simple process, the etch depth is critical for reproducible, optimised device and performance, where under-etching results in current leakage and poor pinch-off of HEMT devices, alter transmission lines impedance and affects bias levels in circuitry. In contrast, over-etching can lead to low yield devices attributable to a discontinuity of the gate metal at the gate feed area where the gate strip crosses the mesa sidewall as demonstrated in **Figure 3.12**. A new approach will be discussed later in section **5** to overcome the gate metallisation discontinuity drawback imposed by the conventional method of mesa isolation.

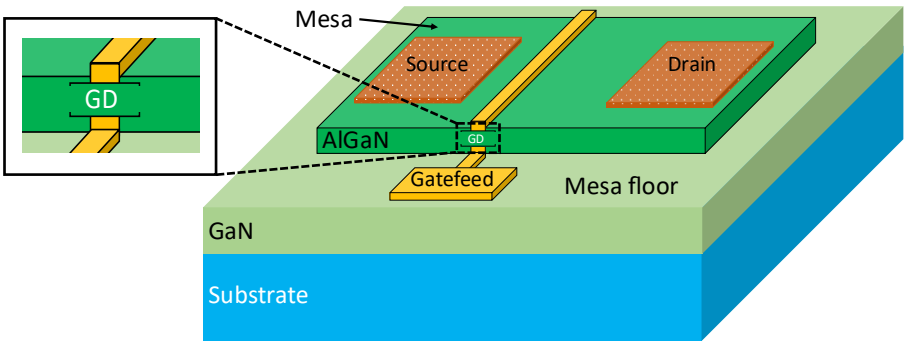


Figure 3.12. Over-etched mesa with gate discontinuity (GD)

The process of mesa isolation begins with spinning S1813, and baking in oven for one hour at a 90°C. Then, the sample is exposed and developed in MF319 for 13 and 75 secs, respectively. After that, a plasma ahing is performed to remove resist residue followed by deoxidisation to remove the oxide layer to prevent it from becoming a mask on the surface which can potentially jeopardies the GaN

etch or considerably slow the etching process. Finally, the sample is plasma etched using **$SiCl_4$**. **Figure 3.13** shows the device post mesa etch has been performed and the etch depth obtained (≈200nm).

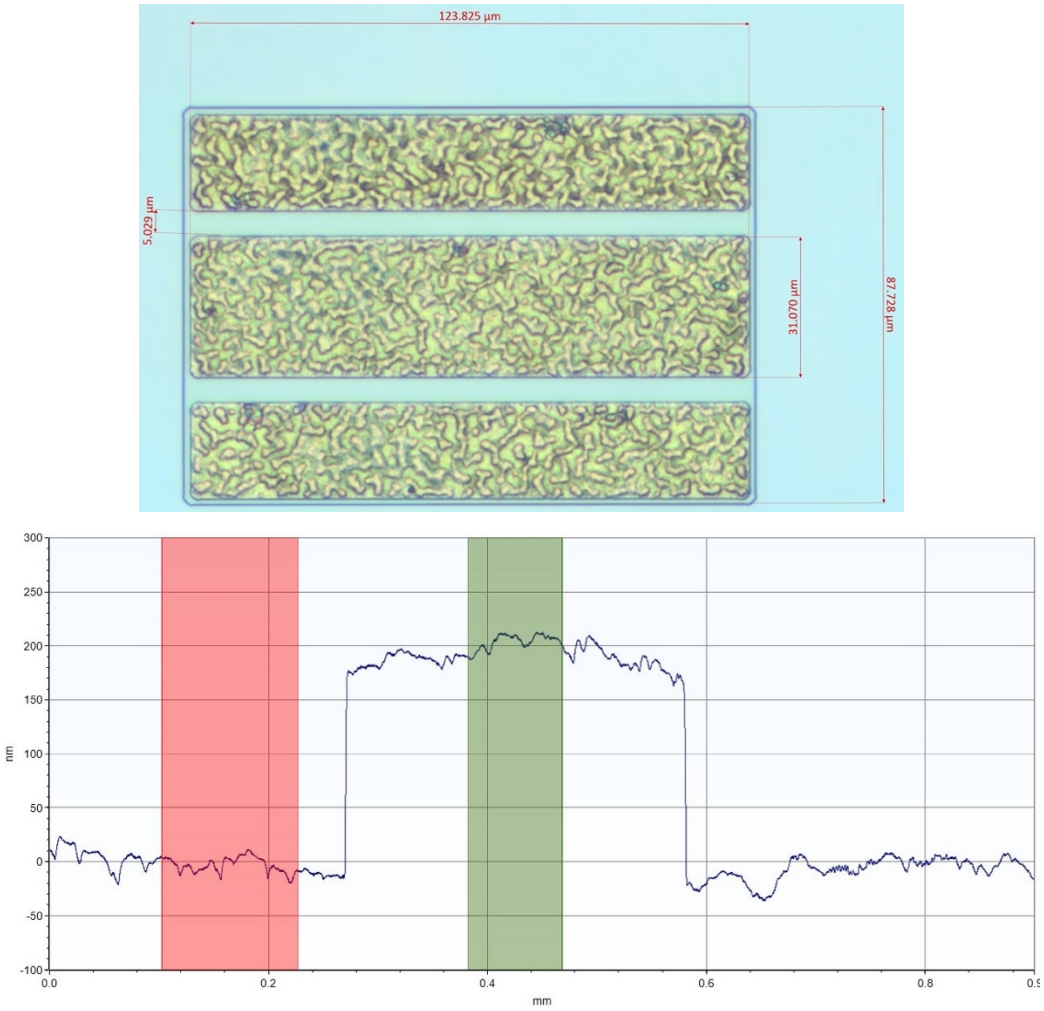


Figure 3.13. HEMT device after 200nm mesa etch

3.8.4. Dielectric Passivation and Insulation

In our process Silicon Nitride (Si_3N_4) was deposited by plasma enhanced chemical vapor deposition (PECVD) in an Oxford Plasma Technology microP80 Plus. Silane (SiH_4), Ammonia (NH_3) and Nitrogen gases were used in the SiN deposition. The substrate was placed on a stage maintained at 300°C during the Si_3N_4 deposition process. The thickness of the silicon nitride used in this work, for passivation, was nominally 150nm. The variation in thickness (run-to-run) of the deposited silicon nitride layer was less than 10%. Since this layer of silicon nitride film is used for passivation as well as a MIM capacitor dielectric and in

addition to the fact that silicon nitride films less than 150nm in thickness resulted in a poor capacitor yield due to pinholes where charges leak through, 150-250nm was the optimal thickness for the silicon nitride film throughout this project for either passivation or dielectrics. However, thicker dielectric, up to 400nm, for capacitors is often applied as an alternative for capacitance value control parameter instead of area and to increase the breakdown voltage of the capacitor as well.

To etch silicon nitride, a positive photoresist was spun on top of the silicon nitride then exposed and developed. The resist was exposed on ohmic contacts including VdP and the bottom plate MIM capacitor CPW interconnect. The unexposed resist acts as a mask during the silicon nitride dry etching process. The Si_3N_4 was etched only on the exposed area of the wafer. A damage free Si_3N_4 etching process was implemented using SF_6 reactive ion etch (RIE) in a Plasma Technology RIE80. This process is a damage free, as determined by depositing Si_3N_4 on a VdP structure, and then removing nitride using the etching process. The measured values of sheet resistance, mobility, and sheet carrier concentration were unaffected, either by silicon nitride deposition or the subsequent etching process. The time required to etch the 150-200nm layer of nitride is about 2-3min. Subsequently, a Dektak was utilised to verify the etch depth of the silicon nitride across the wafer, which was found to be approximately around 170±10nm.

Similarly, the etching process of silicon nitride for the optical lithography gate trench (1μm) applied during this project is identical to process outlined above in this section.

3.8.5. Schottky Contact Formation

Schottky contact is applied in this project to be the gate of a transistor or the anode of a diode. In this project, three methods were employed to fabricate the Schottky contact, fully photolithographic process for both footprint/trenches and head, a mix of both lithography namely e-beam writer and optical lithography for the footprint and head of the gate respectively. Lastly, a complete e-beam lithography for both for features set to less than 1μm in size is employed. Constrained by gate capacitance and resistance patristics T-shaped gate (anode in diodes) is suitable to accomplish two objectives: lowering the gate capacitance

via the reduction of the length of the gate trench, which results in reducing the time delay for higher speed operation. The other objective is to increase the gate head length to offset the increase of gate resistance emanating from the gate foot length reduction. Consequently, a T-shaped gate configuration is necessary to attain these conflicting aims and to overcome the given tradeoff between gate capacitance and resistance. This is the only level of the device process that included the use of e-beam writer. Since photolithography can only offer a minimum feature size of 1μm, the utilisation of an e-beam writer becomes an essential tool for the fabrication of the gate footprint in the size of submicron/nanometer features whereas the gate head is fabricated using photolithography with a fixed length of 1.5μm for all devices.

3.8.6. Probing Bond-Pads, Field Plates and Transmission Lines

The probing pads were designed to be used with on-wafer microwave probes measuring RF signal response up to 110 GHz. The tips of the used RF probes have a coplanar waveguide (CPW) configuration with a characteristic impedance of 50Ω. In use the tips of the probes were aligned to pad markers. Probe pad markers were essential to maintain a known distance from the probe tips to the measured device, known as the skating distance.

Table 3.3. Bond pads and CPW lines process

Lithography	Metal/lift-off
• Spin LOR 10A at 6k for 60 sec. • Bake on HP at 170 °C for 2 min or oven at 160 °C for 30 min. • Spin S1813 at 6k for 60 sec. • Bake on HP at 120 °C for 2 min or oven at 90 °C for 30 min. • Expose with MA6: G-line, dose 98 μJ/cm^2, hard contact. • Develop in MF319 for 90 sec (agitate gently). • Clean with DI water for 2 min, then blow dry with N_2. • O_2 ash at 50 Watt for 2 min. • Soak in HCL:H_2O 1:4 for 10 sec. ***(should be done just before metal deposition)*** • Clean with DI water for 30 sec and blow dry with N_2.	Evaporate: • Metal stack **Ti/Au** (**50/400 nm**). • Soak in 1165 at 50 °C for 30 min, use pipette for 20 sec. • Dip in IPA, then clean with DI water for 2 min, and blow dry with N_2.

Variations in distance from the device under measurement to the probe tips alters the values of the extracted equivalent circuit elements obtained from the RF measurements. The tapered coplanar configuration probe pads were designed to give a 50Ω characteristic impedance using the design equations outlined in CPW section. The fabrication process is outlined in **Table 3.3**.

A thick bi-layer resists were used to lift-off the metallisation consisting of 50nm Ni followed by 500nm gold. The 50nm Ni layer at the bottom provides good adhesion whilst the thick 500nm gold on the top reduces the series resistance from the probe tips to the ohmic contact and provide an adequate interaction with atmosphere owning to its low tendency of oxidising when exposed to air as shown in **Figure 3.14**. The same metallisation is used to produce filters, calibration standards, meander inductors, the top plate of MIM capacitors and various PCMs such as substrate RF leakage, top barrier leakage and CPW transmission lines behavior on GaN wafers with different substrate for coupling analysis.

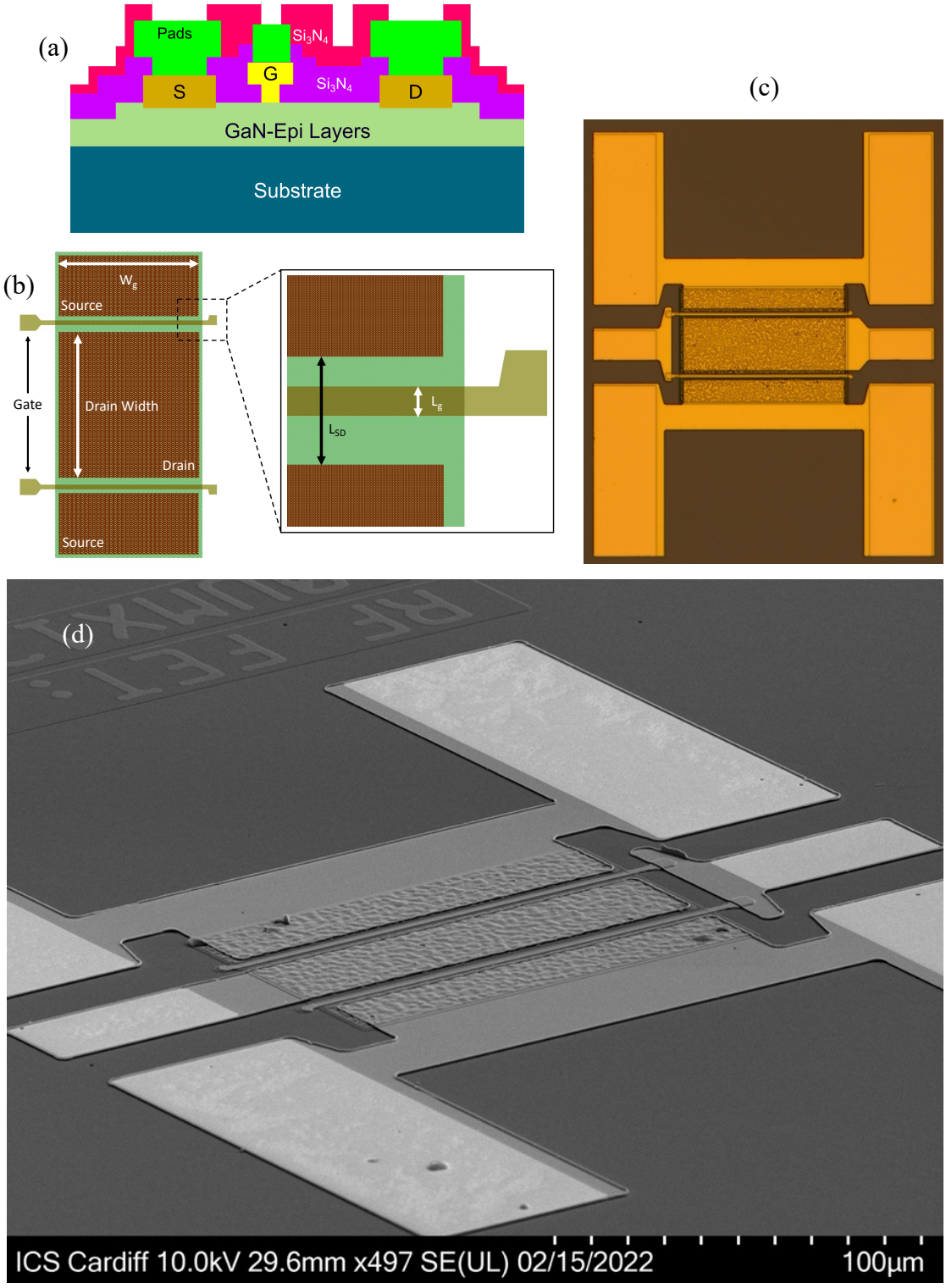


Figure 3.14. HEMT cross-section view (a), layout geometry definitions (b), microscopic image of HEMT with bond pads in a CPW environment (c) and a SEM image (d)

4. PASSIVE AND ACTIVE DEVICES FOR GAN ON SI

Passive elements such as transmission lines, inductors and capacitors are necessary for MMIC realisation on the system level. Accurate modelling of their properties is required to enable design and forecast the conditions of the operating environment, where heat for example generated by the surrounding devices has an immense impact on their performance. In this chapter, various passives on GaN wafers have been developed. The chapter begins with a comparison between Si and SiC to examine the essence of RF losses and coupling issues of GaN wafers. Novel passive structures and a proposed process will be provided to overcome these difficulties concerning the substrate losses.

4.1. Coplanar Transmission Lines

4.1.1. Coplanar Transmission Lines Theory and Design

The coplanar waveguide (CPW) introduced by Wen and is shown in **Figure 4.1**, which consists of three metal conductors separated by two slots each of width (S) printed on a dielectric substrate. The width of the central conductor between the slots is denoted by (W). The ground planes are assumed to have an infinite width.

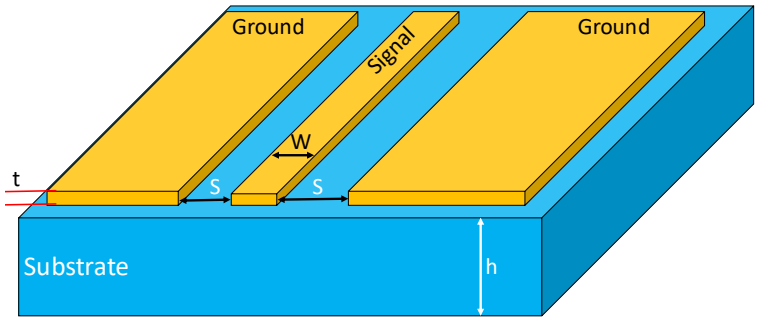


Figure 4.1. Coplanar transmission line geometry

CPW is generally more attractive as the transmission line media for the microwave monolithic integrated circuits (MMICs) because of the following

advantages over microstrip (MS). Coplanar interconnect topologies (Coplanar waveguide, Slotline) avoid parasitic via hole inductance effects in MMICs and have become increasingly desirable in MMICs to avoid the use of ultra-thin substrates and backside wafer processing. There are some disadvantages of the CPW structure such as parasitic modes, lower power-handling capability, and poorer field confinement than microstrip since half of the electric field is in air. CPW may be considered as a pair of coupled slotline which support both even and odd modes. By convention, the odd mode (unbalance mode) is referred to as the CPW mode, the even mode (balanced mode) is known as the slot- line mode as demonstrated in **Figure 4.2**.

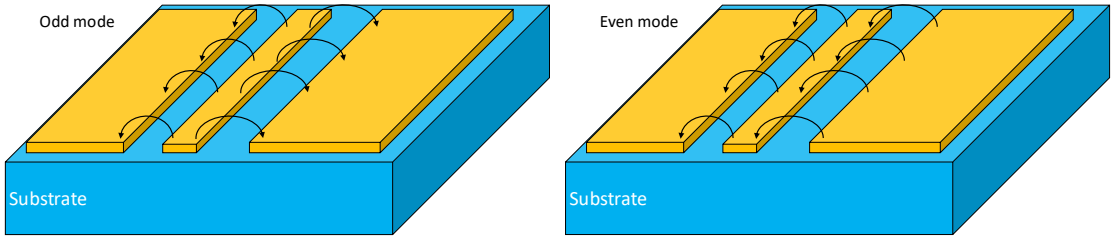


Figure 4.2. Odd and even modes are supported by CPW

Generally, the slot-line mode is undesirable and is suppressed using airbridges shorting the two ground planes at intervals of a quarter wavelength ($\lambda_g/4$).

$$\lambda_g = \frac{\lambda_o}{\sqrt{\varepsilon_{eff}}} = \frac{c}{f\sqrt{\varepsilon_{eff}}}, \ where\ \varepsilon_{eff} = \frac{\varepsilon_{r1} + \varepsilon_{r2}}{2} \tag{4.1}$$

ε_{eff} is the effective relative permittivity used to accurately deduce the dielectric constant of mixed dielectrics such as air and substrate, λ_o is the wavelength of free space, c is the speed of light in vacuum, f is the operating frequency, $\varepsilon_{r1}\ and\ \varepsilon_{r2}$ is the relative permittivity of the CPW substrate (9.5 for GaN/Si) and air (unity), respectively.

The characteristic impedance (Z_o) of the CPW and effective dielectric constant (ε_{eff}) were obtained using the following expressions:

$$Z_o = \frac{30\pi}{\sqrt{\varepsilon_{eff}}}\left[\frac{K(k^*)}{K(k)}\right] \tag{4.2}$$

where $\left[\frac{K(k^*)}{K(k)}\right]$ is the ratio between the complement $K(k^*)$ and the complete elliptic integral of the first kind $K(k)$ respectively obtained from the following equation:

$$\frac{K(k^*)}{K(k)} = \pi^{-1}\log\left(2\frac{1+\sqrt{k^*}}{1-\sqrt{k^*}}\right), \qquad where\ k^* = \sqrt{1-\left(\frac{W}{W+2S}\right)^2} \tag{4.3}$$

The approximations above are only valid under these conditions:

1- $0 \le \left(\frac{W}{W+2S}\right) \le \frac{\sqrt{2}}{2}$
2- Substrate thickness $h > \frac{W+2S}{2}$
3- An assumption of an infinite ground planes is made, where their losses are neglected

The accuracy of these expressions has been shown to be comparable with fabrication tolerances. The CPW lines used for this project were designed with 55μm ground-to-ground spacing (2S+W), and a centrally positioned conductor 25μm wide (W), to give a 50Ω impedance line. These dimensions result in a 15μm conductor-to-ground plane gap (S) dimension for the CPW. The 25gm gap (S) allows the CPW to be extended to form the slot-line required for the mixer MMIC circuit without the requirement for impedance tapers. The minimum separation required between adjacent CPW lines is three times the ground-to-ground spacing (2S+W) to reduce coupling to lower than 30dB. Several CPW lines with different lengths were designed and fabricated on a 675 μm-thick p-type LR (ρ < 40 Ω.cm) and HR (ρ > 5K Ω.cm) Si (111) substrate. Two types of metallisation technique were used, electron beam evaporation and gold plating. Airbridges were fabricated to connect the ground planes at 400μm intervals to suppress the excitation of the slot-line mode. CPW transmission lines were characterised by on-wafer S-parameter measurements from 240MHz to 40GHz using Agilent PNA network analyser (E8361A). A propagation loss of 0.3dB/mm for novel CPW transmission lines at 40GHz was achieved using a 550nm Au layer evaporated by electron beam. Normally a metal thickness (t) of about three times the skin

depth is desired to minimise conductor loss caused by the resistive nature of the conducting medium. At microwave frequencies the signal flow is concentrated in the surface layer of the conductor and decreases exponentially with depth into the conductor. The penetration of the current flow is defined by the skin depth (δ). (The thickness of the layer of the conductor at which the current density fallen to l/e (or 30%) of its surface value.)

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_o \mu_r}} \tag{4.4}$$

where is the ρ resistivity of the metal in Ω·m, f is the frequency in Hz, μ_o is the permeability in vacuum (4πE-7 Hm^{-1}), μ_r the conductor relative permeability (unity for gold metal).

An attempt to minimise the propagation loss by increasing the gold thickness to 2μm using gold plating (less costly process) gave no reduction in propagation loss of the transmission lines. This could be due to the rough surface, large grain size, and impurities inherent in the gold plating method.

4.1.2. CPW Transmission Lines on Si and SiC Substrates

To understand the RF losses obtained when using GaN-on-HR Si substrates, 300 μm-length CPW lines were realised. 3-D full-wave electromagnetic simulation tool was used for device design and simulation, whereas microwave-circuit software was used for device modelling. The measured and simulated RF performance of CPW on GaN-on-HR Si and GaN-on-SiC, with an identical epi-structure, up to 40 GHz frequency is shown in **Figure 4.3**. Simulations were validated by the close agreement between measured and simulated S-parameters results. The obtained results clearly show that the CPW on GaN-on-HR Si introduced much more loss than the CPW on GaN-on-SiC benchmark (0.6 dB compared to 0.2 dB at 40 GHz). This is obviously an indication of substrate coupling effects presented by the GaN-on-HR Si substrate. Furthermore, both CPW lines showed good matching to 50 Ω, where a reflection coefficient of below -20 dB was obtained.

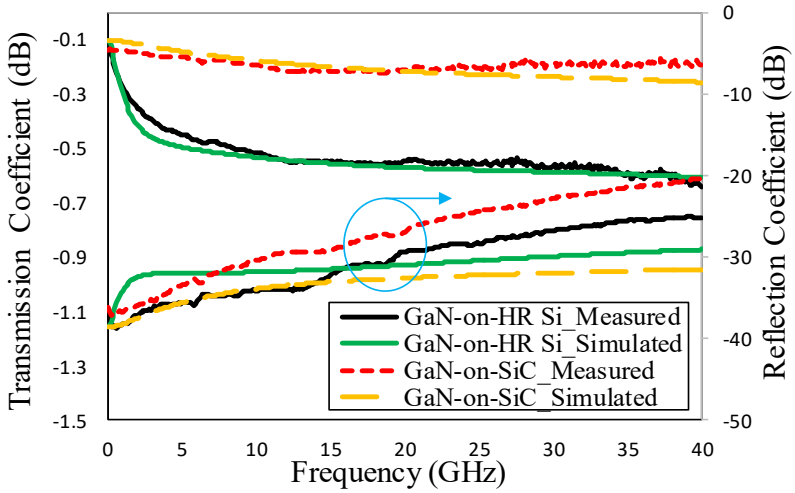


Figure 4.3. Measured and simulated S-parameters of the fabricated CPW lines and simulated transmission coefficient for CPW on GaN-on-HR Si and SiC

4.1.3. RF Behavior on GaN-on-LR Si Substrate

In this section, a comprehensive study of the RF losses originating from GaN-on-LR-Si substrate is conducted. First a CPW transmission line will be simulated, fabricated, and modelled to observe the propagation within the transmission lines and the effects of LR-Si substrate. Secondly and similarly, an RF leakage PCM using an open-circuited stubs will be examined to observe the leakage of the injected signal into the substrate.

4.1.3.1. CPW Lines S-Parameters

To understand loss mechanism for GaN-on-HR Si substrates, 300 µm-length CPW lines were realised. 3-D full-wave electromagnetic simulation tool was used for device design and simulation, whereas microwave-circuit software was used for device modelling. The CPW transmission line is designed to exhibit a 50Ω characteristic impedance. The EM simulation, demonstrated in **Figure 4.4**, shows the electric field strength distribution within the substrate. Most of the electric field is confined between the signal path and the ground indicating a CPW behavior. A leakage of the field is observed at up to 6µm into the substrate with an electric field strength of more than 30 V/m. Lower leakage at a shallower distance, less than 50µm, from the surface was observed from GaN-SiC, for example. This shows that LR silicon substrate are more prone to electric coupling than SiC.

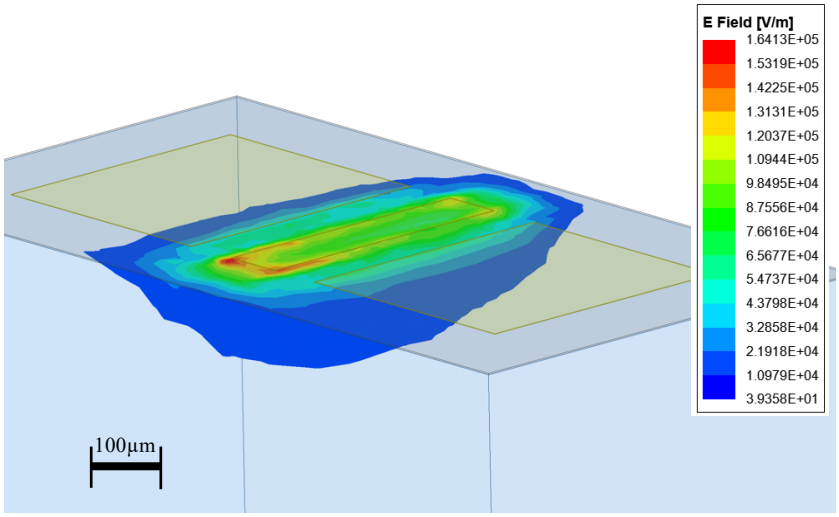


Figure 4.4. CPW electromagnetic simulation with electric field distribution within the substrate

AlGaN/GaN HEMT layers were grown on a 675 µm-thick p-type LR ($\rho < 40\ \Omega.cm$) Si (111) substrate for the experiment. An AlN transition layer, a Fe-doped GaN buffer, 25 nm AlGaN top barrier, and 2 nm GaN cap layer which make up the epi-layer structure. The CPW transmission line, shown in **Figure 4.5**, is fabricated using a photolithography means. The process started after mesa etch of around 200nm depth and after the deposition of the first layer of Si_3N_4. Next, a bilayer resist technique was applied to realise the CPW transmission line. This was followed by a final deposition of silicon nitride to protect the metals.

The final fabrication step was a silicon nitride etch to open windows in the pads for measurements. Using an Agilent PNA network analyser (N5227A) and a short-open-load-thru (SOLT) calibration technique, on-wafer S-parameter measurements were done up to 50 GHz. In this research, CPW structures constructed at W = 25µm and S = 15µm for Si substrate, all CPWs were designed with a characteristic impedance of 50Ω.

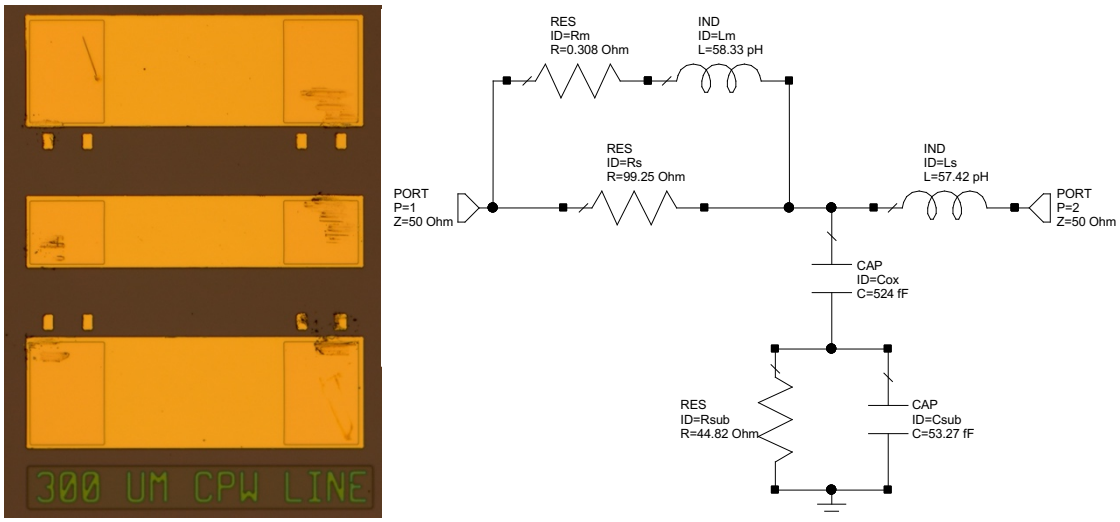


Figure 4.5. CPW equivalent circuit model and microscopic image of the CPW transmission line

Figure 4.5 also shows a small signal circuit model using lumped elements to represent the various RF performance and losses within the fabricated and simulated CPW transmission line. R_s and L_s represent the series resistance and inductance, respectively, of the transmission line contributed directly to the conductor loss. R_m and L_m represent the resistance and inductance due to skin losses of the metal. C_{ox} represents the capacitance between the metal and the substrate. Finally, R_{sub} and C_{sub} model the substrate conduction and electric coupling capacitance, respectively.

Figure 4.6 and **Figure 4.7** demonstrate the S-parameters on Smith chart for the EM simulation CPW, the fabricated CPW measurement, and the RF small signal model. Both figures exhibit identical behavior, which indicates that the fabricated transmission line and the wafer are displaying a passive functioning in symmetrical pattern across the wafer to a considerable degree. At lower frequency up to 10GHz, the CPW transmission line is controlled by the series inductive branch of the small signal model and that most of the signal is propagated from the input to the output port of the circuit. However, as the frequency increases, the capacitive element between the metal and the substrate is activated and it begins to absorb the injected signal into the substrate. This leads to an increase in the coupling between the signal and the substrate and hence it becomes conductive, and the lossy behavior of the LR-Si substrate is clearly apparent.

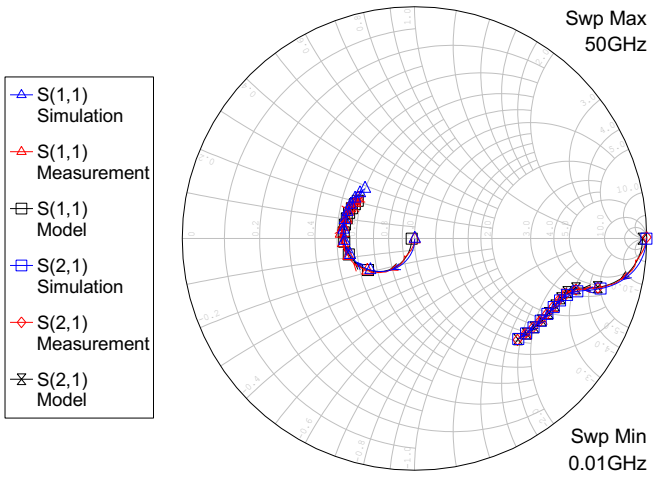


Figure 4.6. S11 and S21 smith chart plot of the simulated, measured, and modelled 300μm CPW line.

Figure 4.6 shows both the transmission and the reflection coefficients of the CPW transmission line in all three forms, i.e., EM simulation, fabrication, and small signal model. **Figure 4.7**, on the other hand, exhibits both the reverse transmission and the reflection coefficients of the CPW transmission line in all three forms, i.e., EM simulation, fabrication, and small signal model.

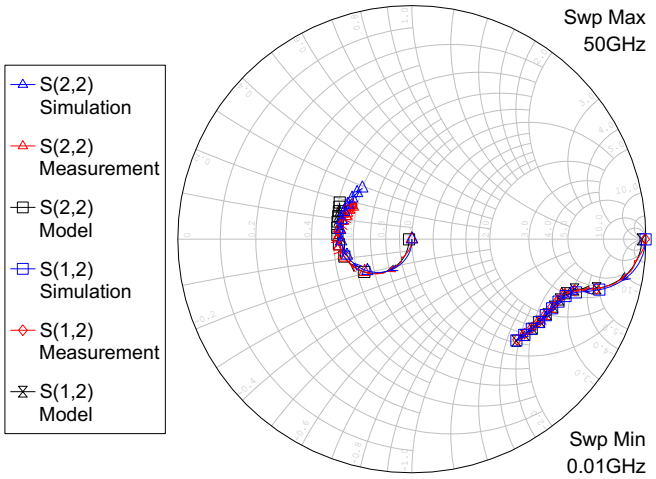


Figure 4.7. S22 and S12 smith chart plot of the simulated, measured, and modelled 300μm CPW line.

Figure 4.8 shows both the reflection and transmission coefficients. The graph demonstrates a good agreement between the EM simulation, the measured and

the model of the CPW transmission line. It is evident that the transmission line is exhibiting a reflection of less than -10dB for the entire frequency bandwidth. The transmission coefficient, on the other hand, is showing a cutoff attenuation of -3dB at 10GHz with a maximum attenuation of approximately -4dB occurring at 50GHz point.

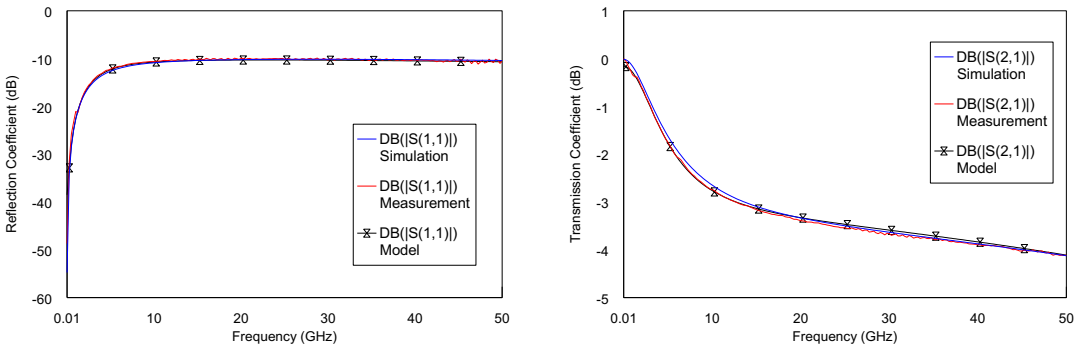


Figure 4.8. Reflection and transmission coefficients of CPW

To characterise the behavior of the CPW transmission lines with regard to its frequency alteration, the S-Parameter is converted to the corresponding Z and Y Parameters to observe the capacitive and inductive nature of the CPW line. This is especially significant at higher frequency operation which may considerably affect the characteristic impedance evaluation of the transmission lines. **Figure 4.9** illustrates the real and imaginary of both the complex impedance and admittance. Both the resistance and the reactance of the CPW transmission lines are exhibiting a slightly higher slope at higher frequency (above 5GHz) than the conductance and the susceptance. This slightly higher slope inclination indicates that the simulated, fabricated, and modelled CPW transmission lines are more inductive in nature than they are capacitive. Consequently, this inductive behavior exhibited by the CPW transmission lines manifested by the impedance slope and the lower admittance slope or lack thereof, the transmission lines are ineffective in operation at higher frequency which further asserts the point illustrated by the forward transmission coefficient, in **Figure 4.8**, where attenuation reaches -4dB at maximum frequency.

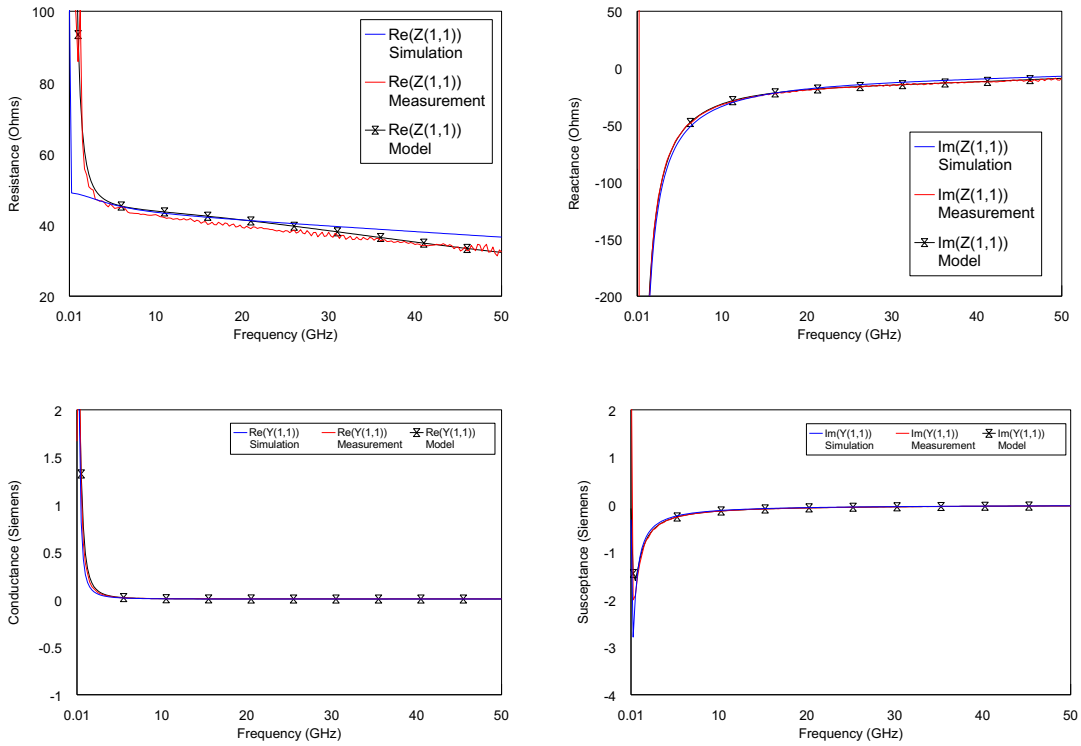


Figure 4.9. Resistance, reactance, conductance, and susceptance of the CPW line on LR-Si substrate

4.1.3.2. CPW Lines Propagation Analysis

The propagation constant is split into two parts, each of which has a distinct influence on signals. The attenuation constant, which is indicated by the Greek lowercase letter, is the real component of the propagation constant (α). It reduces the amplitude of a signal as it travels through a transmission line. The native units of the attenuation constant are Nepers/meter. However, in microwave engineering, the value is frequently converted to dB/meter by multiplying the magnitude given in Nepers/length by 8.686 dB to get the loss value in dB/length. The phase constant adds the imaginary component to the propagation constant and is indicated by a Greek lowercase letter (β). At a constant time, it determines the sinusoidal amplitude/phase of a signal through a transmission line. The "natural" units of the phase constant are radians/meter, and it is usually converted to degrees/meter by the multiplication of $180/\pi$. In this thesis, the complex propagation constant is extracted from the measurements/simulation S-parameters. Hence, its standard formula and the S-parameters-based calculation formula are given by:

$$\gamma = \sqrt{Z \cdot Y} = \alpha + j\beta \tag{4.5}$$

$$e^{-\gamma L} = \frac{1 - {S_{11}}^2 + {S_{21}}^2}{2S_{21}} + \sqrt{\frac{(1 + {S_{11}}^2 - {S_{21}}^2)^2 - 4{S_{11}}^2}{4{S_{21}}^2}} \tag{4.6}$$

where γ is the propagation constant, Z and Y are the impedance and admittance, respectively, L is the actual length of the given transmission line. Furthermore, the transmission line characteristic impedance is also studied in this work, and it is evaluated using the following:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = Z_s \sqrt{\frac{(1 + S_{11})^2 - {S_{21}}^2}{(1 - S_{11})^2 - {S_{21}}^2}} \tag{4.7}$$

where R, L, G and C are the transmission line resistance, inductance, conductance, and capacitance respectively, which are all given per unit length,Z_S is the simulation or measurement system impedance, and it is often equal to 50Ω.

From the S-parameters, the dissipation loss can be directly calculated using Eq.(4.8). Also, the effective dielectric constant can be extrapolated using Eq.(4.9). Finally, the quality factor of the transmission lines, which is basically half the ratio between the phase and the attenuation coefficients of the propagation constant, calculated using Eq.(4.10).

$$D_{Loss} = 10 \log\left[\frac{1 - |S_{11}|^2}{|S_{21}|^2}\right] \tag{4.8}$$

$$\varepsilon_{eff} = \left[\frac{c\beta}{\omega}\right]^2 \tag{4.9}$$

$$Q = \frac{\beta}{2\alpha} \tag{4.10}$$

where D_{Loss} is the dissipation loss, ε_{eff} is the effective dielectric constant, c is the speed of light in vacuum (≈ $3 \times 10^8\ meter/second$), and Q is the quality factor of the transmission line. **Figure 4.10** illustrates the magnitude of the propagation constant and its real component i.e., the attenuation constant for the fabricated CPW line in conjunction with the simulation and the small signal model for validation. The CPW is clearly exhibiting a lossy behavior with an attenuation of

approximately 5dB/mm at 10GHz and it increases to a little less than 15dB/mm at the maximum frequency. This further shows the inefficiency of the transmission lines using LR-Si substrate as the frequency increases particularly beyond the 10GHz mark as the signal amplitude is degraded immensely.

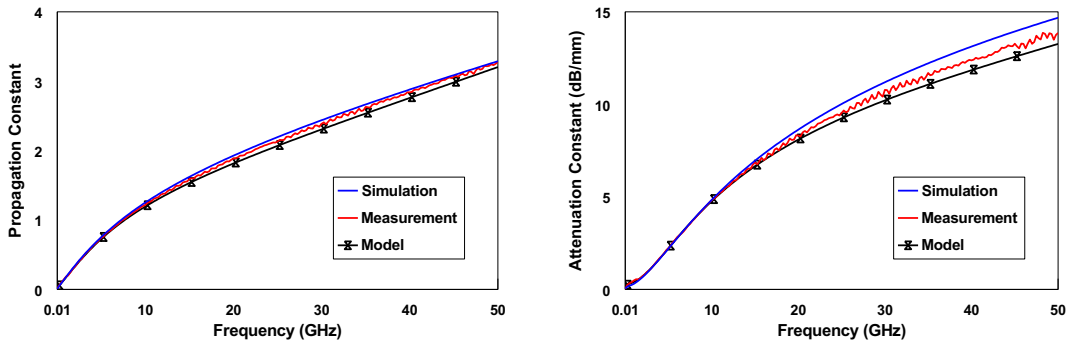


Figure 4.10. Propagation constant and attenuation of CPW

Characteristic impedance and the dissipation loss are shown in **Figure 4.11**. The characteristic impedance of the CPW lines is showing a nonlinear performance with a minimum value of 15Ω at low frequency and increases to more than 45Ω at the higher end of the operation frequency. This is attributed to the increase of the inductance of the transmission line as the frequency raises, which is most likely stemming from the skin effect. The dissipation loss, on the other hand, is further demonstrating the effect of the lossy silicon substrate on the transmission line performance. The losses reach a value of about 7dB/mm at 10GHz with a linear rise from lower frequency.

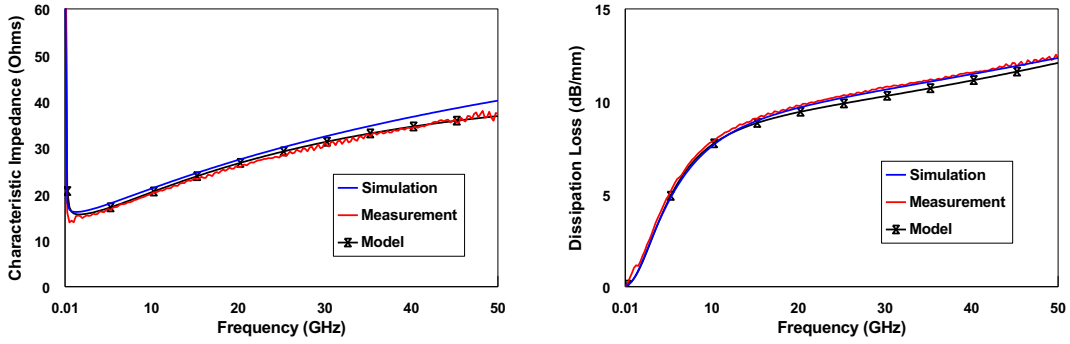


Figure 4.11. Characteristic impedance and dissipation losses of CPW transmission line

The effective dielectric constant and the quality factor of the transmission line are illustrated in **Figure 4.12**. It is evident that, at lower frequency, the effective dielectric constant is mainly determined by the silicon permittivity in conjunction with the corresponding value of the static GaN 11.9 and 8.9 respectively. However, as the frequency increases, the effect of GaN is more apparent where the GaN dielectric constant value at high frequency (≈ 5.3) is more dominant in the calculation of the effective dielectric constant. Moreover, the effective dielectric constant keeps diminishing to a value of less than 2.5 obtained at the maximum frequency.

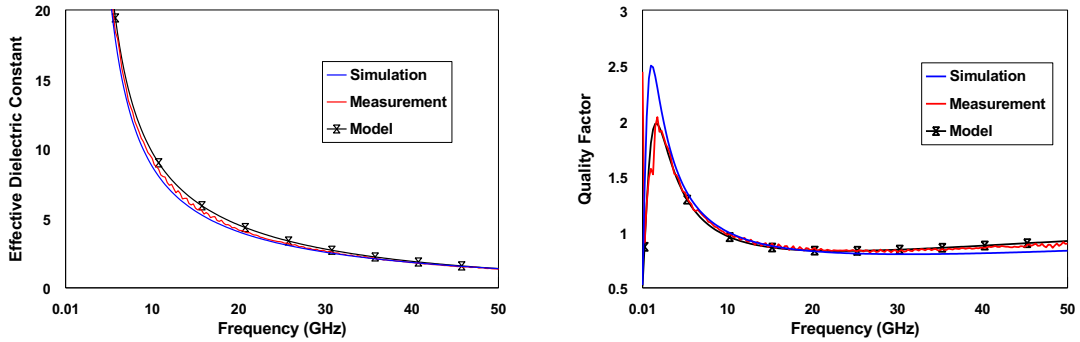


Figure 4.12. Effective dielectric constant and quality factor of CPW lines

This is mostly due to the reduction of the total capacitance of the transmission line as the frequency rises. The transmission line factor has a maximum of 2 to 2.5 and it falls to unity at exactly 10GHz and it levels off at unity up to the maximum frequency. This further shows that the fabricated CPW transmission lines are useable at frequency below 10GHz point when placed on a LR-Si substrate.

4.1.3.3. Telegrapher's Equation and RLGC Model

A transmission line is a series of conductors in a nonconducting environment that forms a means of transmitting an electrical signal with the least amount of loss and interference possible. The conductor and insulating portions are expected to be homogeneous and uniformly shaped over their length. As a result, the electrical characteristics in the conductor and insulating materials are uniform as the electrical signal travels along the transmission line. A simple electrical circuit

model can then be used to depict a transmission line. For Example, a single conductor forms the transmission line as illustrated in **Figure 4.13**, which is asymmetrical in nature. The signal is passed down the line with the voltage on the conductor in anti-phase with respect to the ground, and the current on the conductor having the same magnitude but travelling in the opposite direction to the current in the ground path.

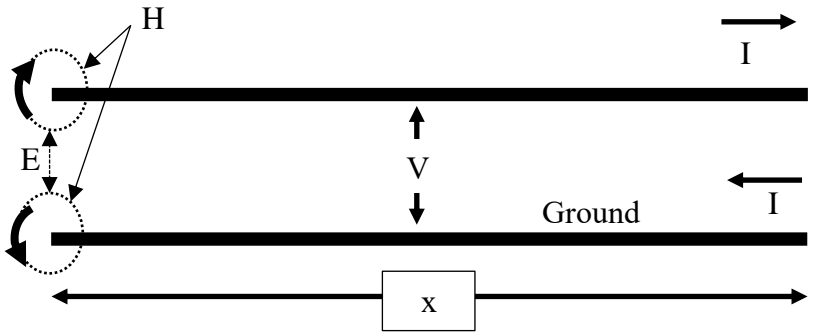


Figure 4.13. Single conductor with current flows and magnetic (H) and electric (E) fields patterns

The current in the conductor and the ground create a magnetic field, and the potential difference between them produces an electric field as depicted by the patterns. Considering a small section of the conductor (transmission line), the magnetic field and the electric can be represented by an inductive and capacitive circuit model respectively. The inductance and capacitance are evenly distributed across the line. The conductor and the ground have some series resistance and a shunt conductance is present between them due to the loss of dielectric within transmission medium. These are, once again, uniformly scattered down the line. The following are the definitions for the parameters **L**, **C**, **R**, and **G**:

- **L** represents the magnetic field around the transmission line as an inductance distributed all r along its length (in units of inductance-per-unit length, H/m),
- **C** represents electric field in the dielectric material (in units of capacitance-per-unit-length, r F/m),
- **R** represents resistive loss in the conductor (in units of resistance-per-unit-length, Ω/m)

- **G** represents dielectric loss in the insulating material (in units of conductance-per-unit- length: Ω−1/m or S/m).

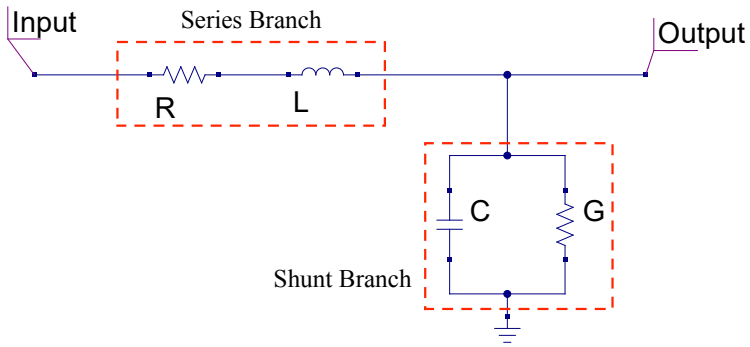


Figure 4.14. Telegrapher's equation representation of a short section of the conductor interconnect

As a result, for a short transmission line section of length x, the resistance, inductance, conductance, and capacitance are Rx, Lx, Gx, and Cx, that is the 'per unit length' value times the length x. The electrical circuit depicted in **Figure 4.14** may be used to simulate the small segment with length x using these values. This model is valid for a segment of line if the phase of the currents and voltages does not change dramatically throughout its length, which relies on the rule of thumb that the length, x, should be less than one-twentieth of a wavelength. Hence, the approximation for a 300μm transmission line is considerably accurate up to a frequency of 50GHz (obtained using the equation, $f = \frac{c}{20L}$, where c is the speed of light in a vacuum and L is the actual length of the line). To represent the whole transmission line of length L, the line must be subdivided into various of these extremely short subsection portions by a factor of 20. The value of these quantities can be calculated using the following set of equations as given by:

$$\begin{aligned} R &= Re\{\gamma \cdot Z\} \quad L = \frac{Im\{\gamma \cdot Z\}}{\omega} \\ G &= Re\{\gamma \cdot Y\} \quad C = \frac{Im\{\gamma \cdot Y\}}{\omega} \end{aligned} \tag{4.11}$$

Figure 4.15 depicts the frequency-dependent distribution characteristics of the circuit model depicted in **Figure 4.14**. The power loss in the conductor and the energy storage in the magnetic field are represented by the series resistance *R*

and inductance *L*, respectively. On the other hand, the shunt capacitance *C* and the conductance *G* reflect the energy storage in the electrical field and the power loss within the dielectric, respectively, which both account for substrate coupling effects. It is evident that the series components (*R* and *L*) are exhibiting a strong and linear frequency-dependency behavior across the entire frequency spectrum. In contrast, , the shunt conductance and capacitance displayed a constant evaluation across the frequency spectrum explicitly beyond 10 and 5 GHz, respectively.

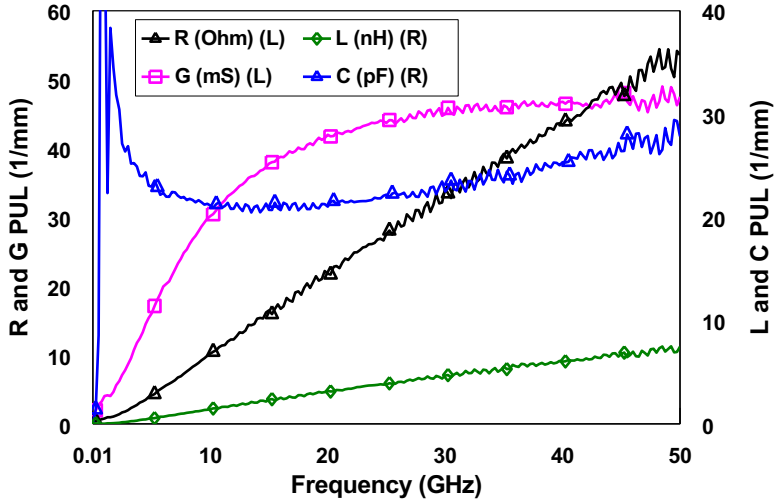


Figure 4.15. LR-Si RLGC model as a function of frequency

The error percentage between the model and the fabricated CPW line measurement is shown in **Figure 4.16**, which is based on the S-parameters difference between them divided by the measured data which can be calculated using the following expression:

$$Error\ (\%) = 100 \times \frac{S_{\text{Measured}} - \left(S_{\text{Modelled/Simulated}}\right)}{S_{\text{Measured}}} \tag{4.12}$$

A good agreement is obtained where the error remains below 5% across the entire frequency band. Similarly, the error percentage between the simulation and the fabricated CPW line measurement is also demonstrated in **Figure 4.16**. The error between the simulation and the fabricated CPW line shows a steady increase particularly beyond 20GHz where the error percentage reaches a value of 10% at 40GHz. This is mainly attributed to the expected effects of the

nonuniformity of the substrate across the wafer which may have acquired within the growth phase. On the other hand, the substrate stack-up used within the EM simulation lacks the inclusion of the growth defects. Hence, a uniform characteristic is assumed across the wafer.

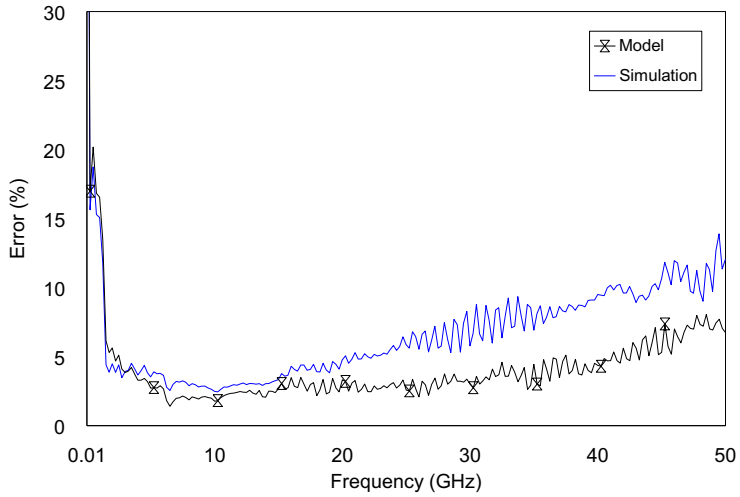


Figure 4.16. Error between simulation/model and the fabricated CPW transmission line

4.1.3.4. CPW Lines Substrate Comparison

Figure 4.17 illustrates the magnitude of the propagation constant and its real component i.e., the attenuation constant for the fabricated CPW line with GaN on different substrates such as HR-Si and SiC beside LR-Si for comparison. The CPW using GaN-on-LR-Si is by far the most lossy of the three substrates with a maximum value of attenuation at the higher end of the frequency spectrum. GaN-on-HR-Si is exhibiting a value of 2.4dB/mm of attenuation, whereas GaN-on-SiC attenuation does not reach unity dB/mm. This is due to the low loss within the substrates. On the other hand, characteristic impedance and the dissipation loss are also shown in **Figure 4.17**. The characteristic impedance of the CPW lines on low conductive substrates (HR-Si and SiC) are showing a more linear performance because of the stability offered by the transmission medium since it is less prone to loss and temperature increase in comparison with LR-Si substrate. The dissipation loss, on the other hand, is further demonstrating the effect of the lossy silicon substrate on the transmission line performance. The losses reach a value of about 7dB/mm at 10GHz with a linear rise from lower

frequency. However, for HR-Si and SiC, the dissipation loss remains below 2.5 and 0.3dB/mm, respectively, over the entire frequency band.

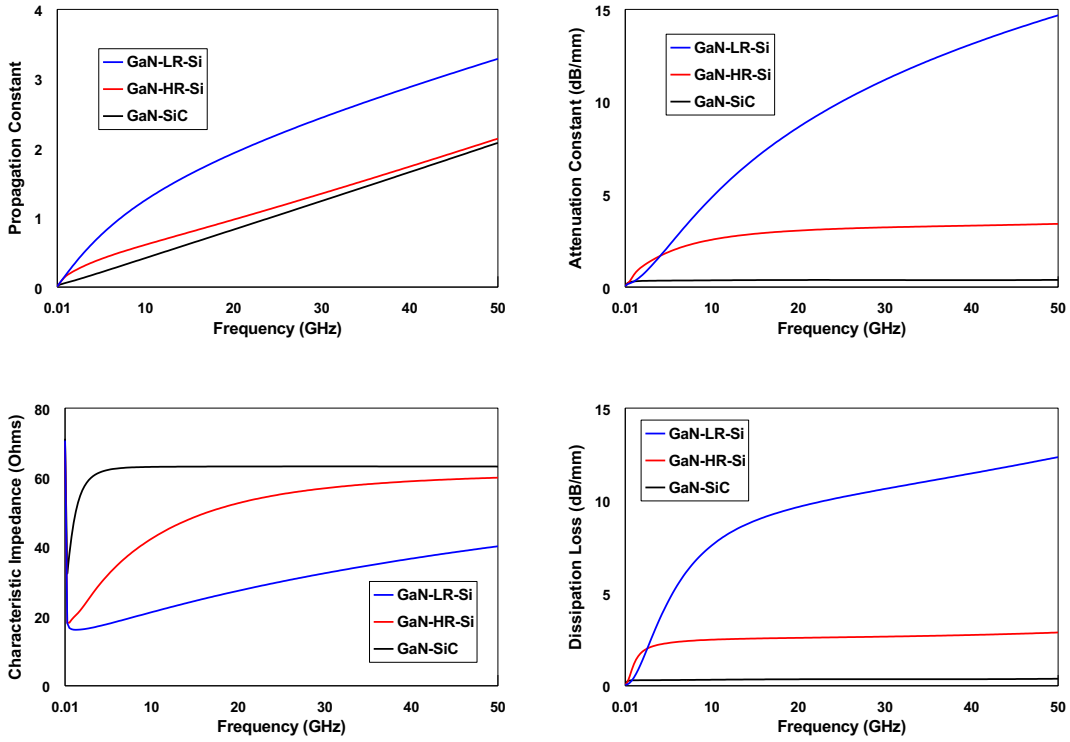


Figure 4.17. Various transmission line propagation parameters for different substrates

Figure 4.18 depicts the frequency-dependent distribution characteristics of the circuit model depicted in **Figure 4.14**. The power loss in the conductor and the energy storage in the magnetic field are represented by the series resistance *R* and inductance *L*, respectively. On the other hand, the shunt capacitance *C* and the conductance *G* reflect the energy storage in the electrical field and the power loss within the dielectric, respectively, which both account for substrate coupling effects as mentioned before. As the dielectric resistivity of the substrate increases, lower series resistance and inductance are attained. For example, GaN-on-SiC show the least quantity of resistance and inductance per mm. This is attributed to the constant characteristic impedance leading to a considerably better matching on the transmission line. Furthermore, the shunt conductance is also reduced thus increasing the quality of the transmission line in general as the substrate resistivity is enhanced. The capacitance, on the other hand, shows a considerable increase especially with SiC substrate which makes the

transmission line exhibit a more stable characteristic impedance across the frequency spectrum and indeed this the case for SiC as depicted in **Figure 4.17**.

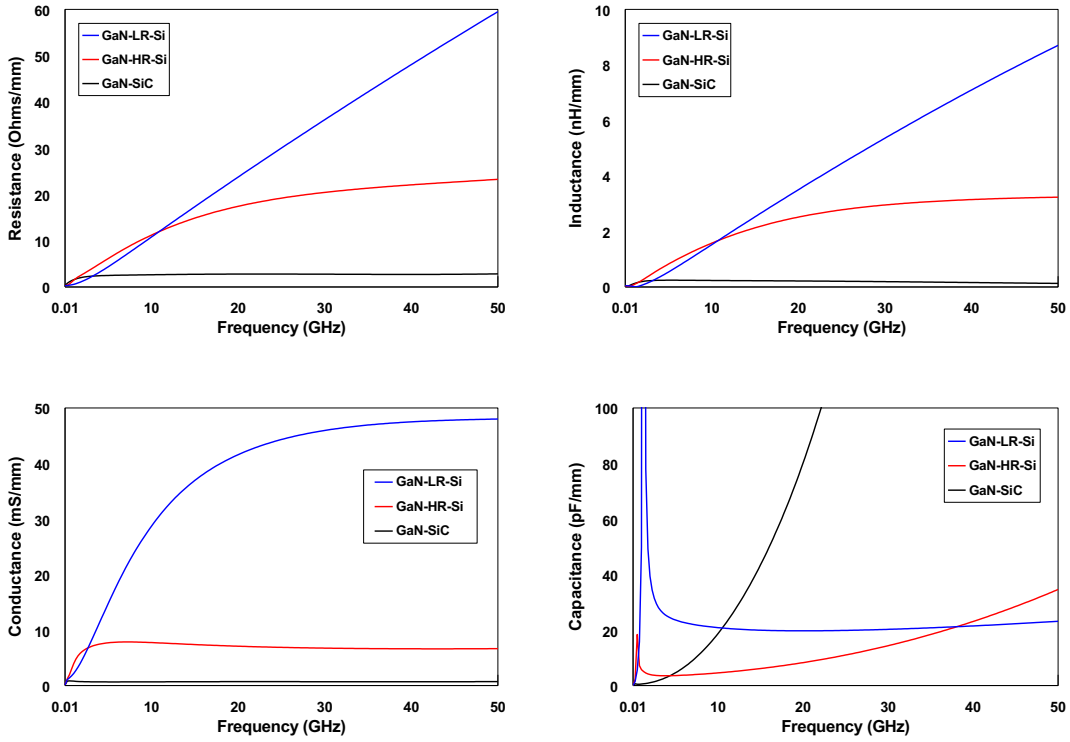


Figure 4.18. RLGC model evaluation as a function of frequency for various substrates

4.1.3.5. RF Leakage PCM

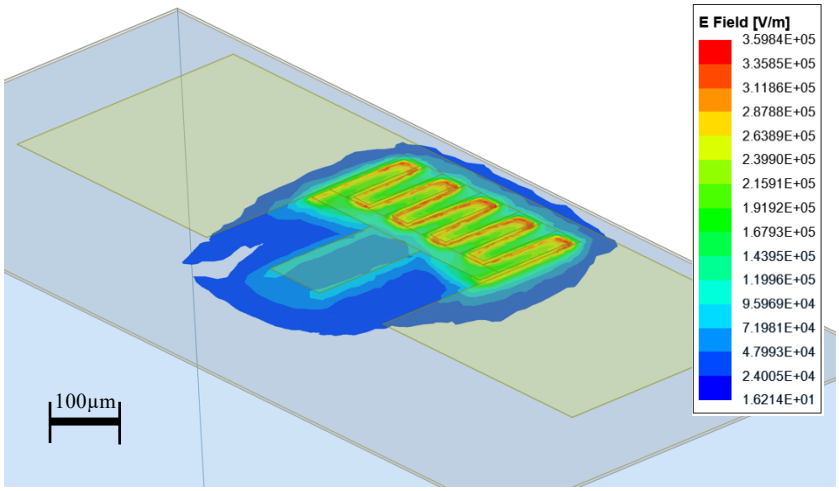


Figure 4.19. RF leakage PCM electromagnetic simulation with electric field distribution within the substrate

To further analyse the RF loss caused by the GaN-on-LR Si substrate, RF-leakage CPW structure were simulated, measured, and modelled as shown in **Figure 4.19** and **Figure 4.20**. **Figure 4.19** demonstrates the electric field between the fingers of the signal and the ground plane.

Figure 4.20 shows the small-signal equivalent circuit model for multi-finger open-circuited CPW lines on GaN-on-LR Si substrate. The RF leakage is shown to be significant for the GaN-on-LR Si, where R_S = 7.4 Ω, L_S = 44 pH, C_L = 294 fF, C_{CC} = 238 fF, and R_L = 143 Ω. These values indicate a strong leakage from the signal line-to-ground of the CPW, which basically represents substate parasitic.

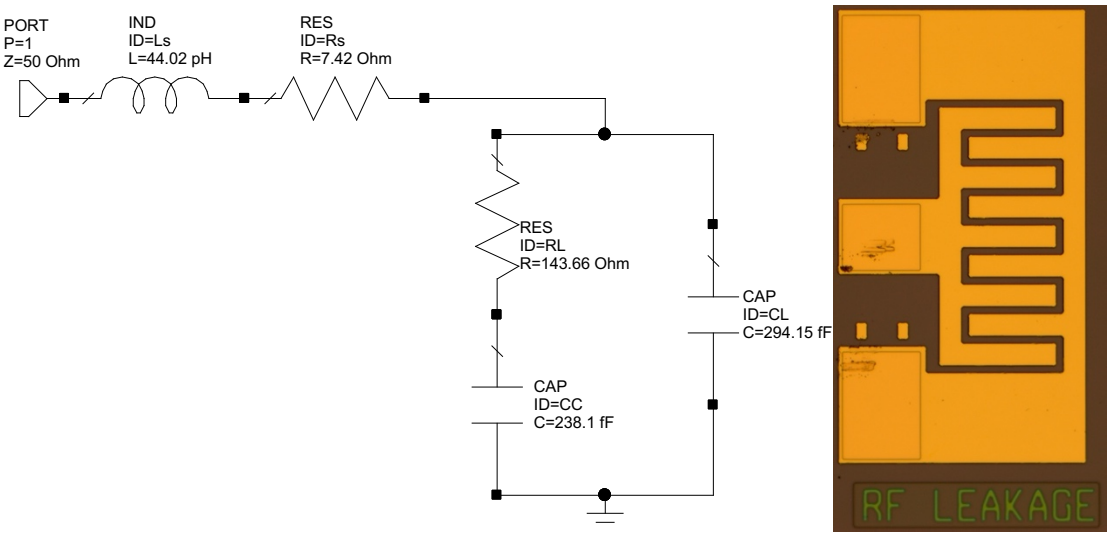


Figure 4.20. RF leakage PCM circuit model for GaN-on-LR Si and the microscopic image

Figure 4.21 shows the modelled and measured results of open-circuited CPW lines up to 50 GHz for GaN-on-LR Si substrate. A capacitively coupled parasitic resistance was observed for the lines on GaN-on-LR Si. Measured and modelled *S*-parameters are in a good agreement, indicating the circuit model validation.

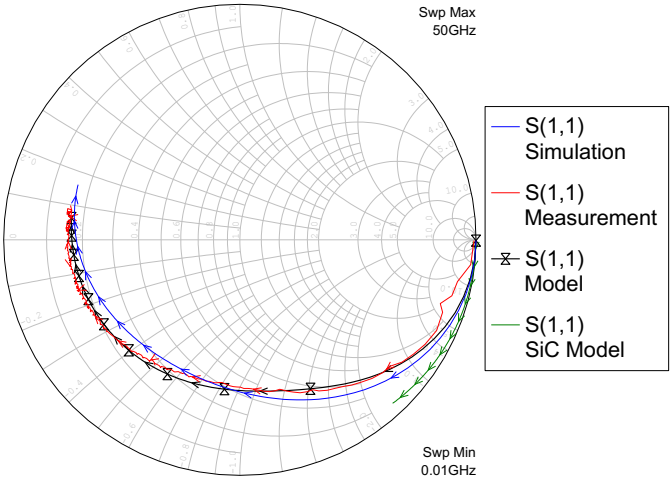


Figure 4.21. S11 for RF leakage PCM

Figure 4.22 illustrates the reflection coefficient magnitude and phase which determines the amount of energy being absorbed by the ground plane and vice versa. A good agreement is obtained for the EM simulation, fabrication, and the small signal model for the designed PCM on GaN-on-LR Si, where a maximum of reflection is attained at 10GHz with a value of -4dB. As the frequency increases, the reflection reduces to -3dB at 50GHz stemmed from the fact that beyond the 10GHz point, the effective dielectric constant is controlled by the GaN epilayers rather than the Silicon substrate as shown in **Figure 4.12**. For comparison, the reflection coefficient magnitude of the PCM on SiC substrate is also included, which reveals the low loss nature of the wafer with almost 0dB reflection across the frequency spectrum for GaN-on-SiC substrate.

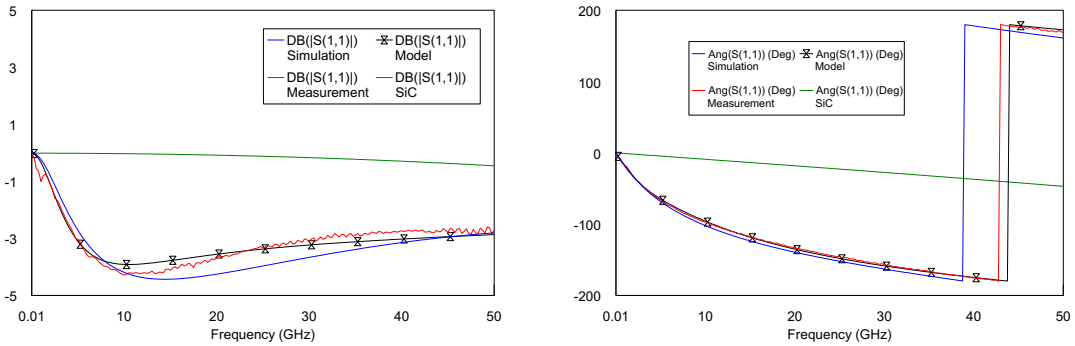


Figure 4.22. Magnitude and phase of the RF Leakage PCM reflection coefficient

The error percentage between the model and the fabricated RF leakage structure measurement is shown in **Figure 4.23**, which is based on the S-parameters difference between them divided by the measured data which can be calculated using Eq.(4.12). A good agreement is obtained where the error remains below 5% across the entire frequency band. Similarly, the error percentage between the simulation and the fabricated RF leakage structure measurement is also demonstrated in **Figure 4.16**. The error between the simulation the fabricated RF leakage structure shows a steady increase particularly beyond 20GHz where the error percentage reaches a value of 15% at 40GHz. As mentioned before, this is mainly attributed to the expected effects of the nonuniformity of the substrate across the wafer which may have acquired within the growth phase.

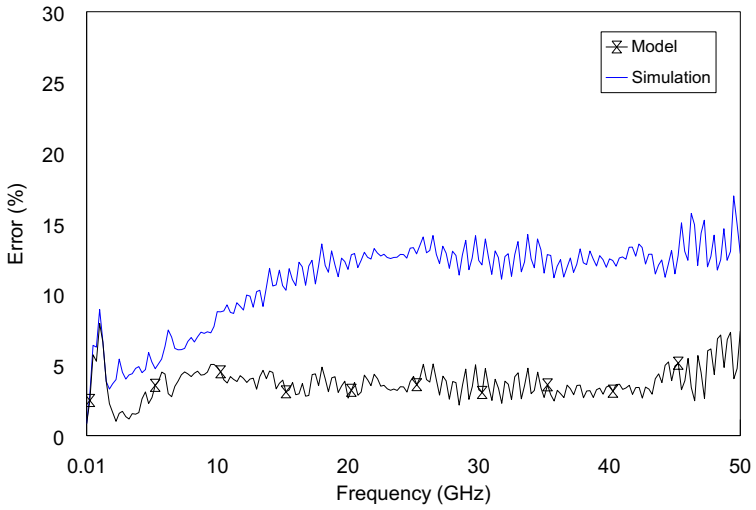


Figure 4.23. Error between simulation/model and the fabricated RF leakage PCM structure

On the other hand, the substrate stack-up used within the EM simulation lacks the inclusion of the growth defects, hence, a uniform characteristic is assumed across the wafer.

The overall RF leakage calculated and given in dB/mm for both GaN on LR-Si and SiC are depicted in **Figure 4.24**. The graph shows the leakage as a function of frequency. It is manifested that higher leakage is acquired when using a LR-Si substrate in comparison with SiC, where the latter exhibits a maximum leakage less than 2dB/mm and the former displays more than 10dB/mm of RF leakage.

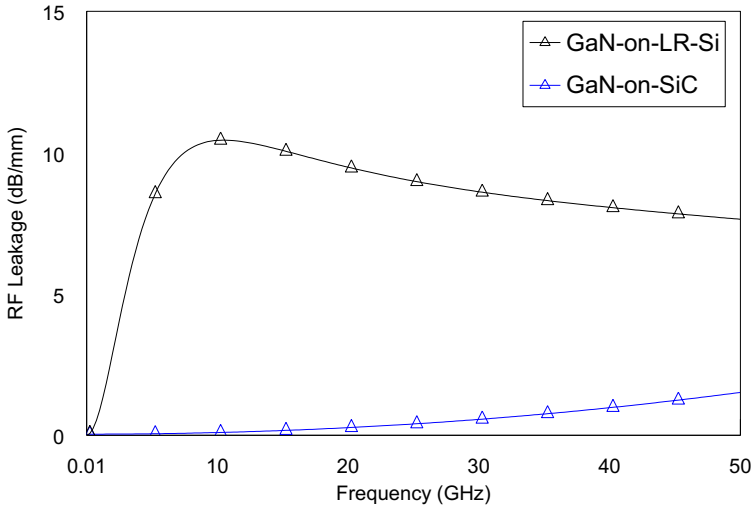


Figure 4.24. RF leakage in (dB/mm) for GaN on Si and SiC

4.2. MIM Capacitors

Beside MMIC inductors, Metal-insulator-metal (MIM) capacitors are among the most widely used passives within RF circuit designs. High quality MIM capacitors are usually characterised by the following criteria:

- High capacitance density per area
- Low leakage current
- High breakdown voltage
- Low series resistance and inductance

4.2.1. MIM Capacitors Theory and Design

Metal-insulator-metal (MIM) capacitors is a form of an electrical discontinuity, though which a signal is passed by an alternating current. This is conducted by collecting an electronic charge in the form of an electric energy with electric fields between the plates of capacitors. This behavior defines the main function of a capacitor, in general, which is a high frequency pass filter if configured in series, where a DC current is blocked determined by the cutoff frequency of the capacitor. These MIM capacitors are a rectangular parallelepiped of dielectric with metallised lower and upper faces as shown in **Figure 4.25**. MIM capacitors are commonly employed in analog/RF circuits because of their advantageous characteristics:

- High-capacitive density due to the minimum width and spacing of metals
- Good matching characteristics due to lateral coupling
- Symmetric plate engineering and fabrication
- Ease of optimisation
- Relatively low leakage current
- Excellent frequency characteristics and quality factor
- Low cost, due to lack of additional mask or process steps, can be integrated into GaN HEMT standard fabrication process

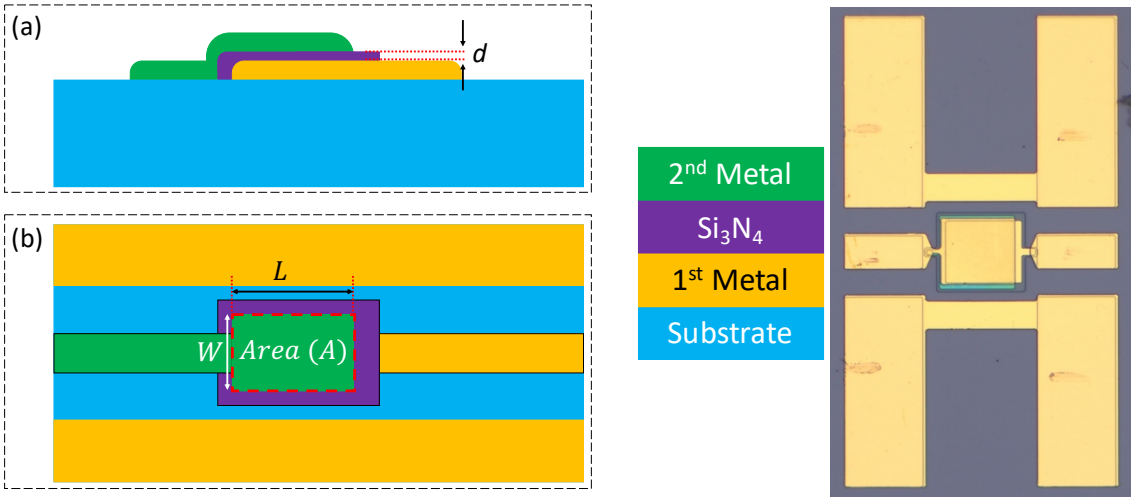


Figure 4.25. Cross-section side view (a), top view layout (b) of a MIM series capacitor and a microscopic image

For a dielectric area (A), thickness (d), and relative permittivity (ε_r), the structure is, to first order, a parallel plate configuration of capacitance (C) is defined by:

$$C(pF) = \frac{\varepsilon_o \varepsilon_r A}{d}, \qquad where\ A = WL\ \&\ \varepsilon_o = 8.854\ (pF/m) \tag{4.13}$$

The thickness and the relative permittivity of the Si_3N_4 used during this project are 150-400nm and 6.5 respectively.

In general, and at high frequency of operation, MIM capacitors exhibit a considerable number of losses generated from the parasitic elements and the nonideality factor of the materials. These losses can be represented by an equivalent circuit model as illustrated in **Figure 4.26**, where L_S and R_S imitate the

series inductance and resistance losses attained from the metallic interconnects respectively. R_L is the capacitor resistance between its plates representing the capacitor leakage, ideally it should be very large to suppress current flow between the plates. C_{prime} is the effective capacitance the MIM capacitor indicating the amount of charge and electric energy the capacitor can store per voltage.

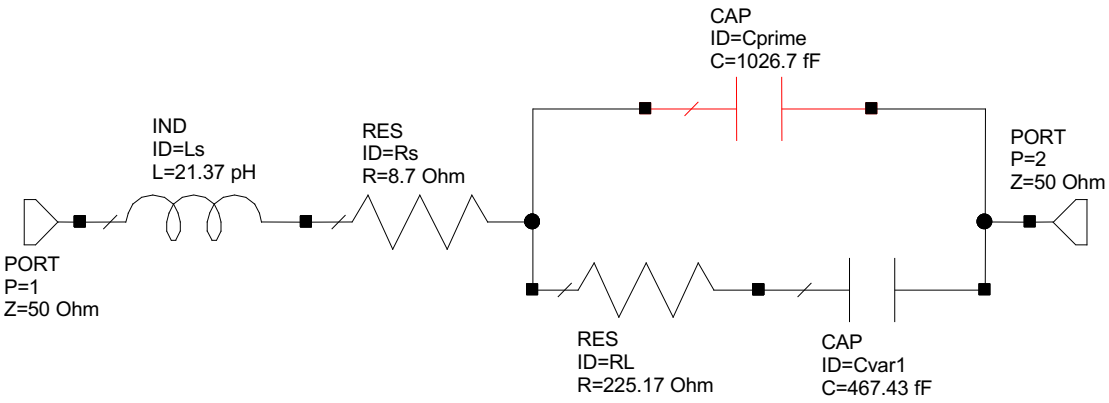


Figure 4.26. Small-signal circuit model of the fabricated series MIM capacitors

In this work, each of the capacitor pattern-development steps were defined using photolithography and fully integrated within the HEMT fabrication steps. The MIM capacitors were fabricated on the mesa floor where the top conductive layers were removed using dry etching process (as in standard MMIC technology). The capacitors were realised with a 200 nm PECVD Si_3N_4 deposited at 300°C. The MIM capacitor fabrication process is visually represented in **Figure 4.27**.

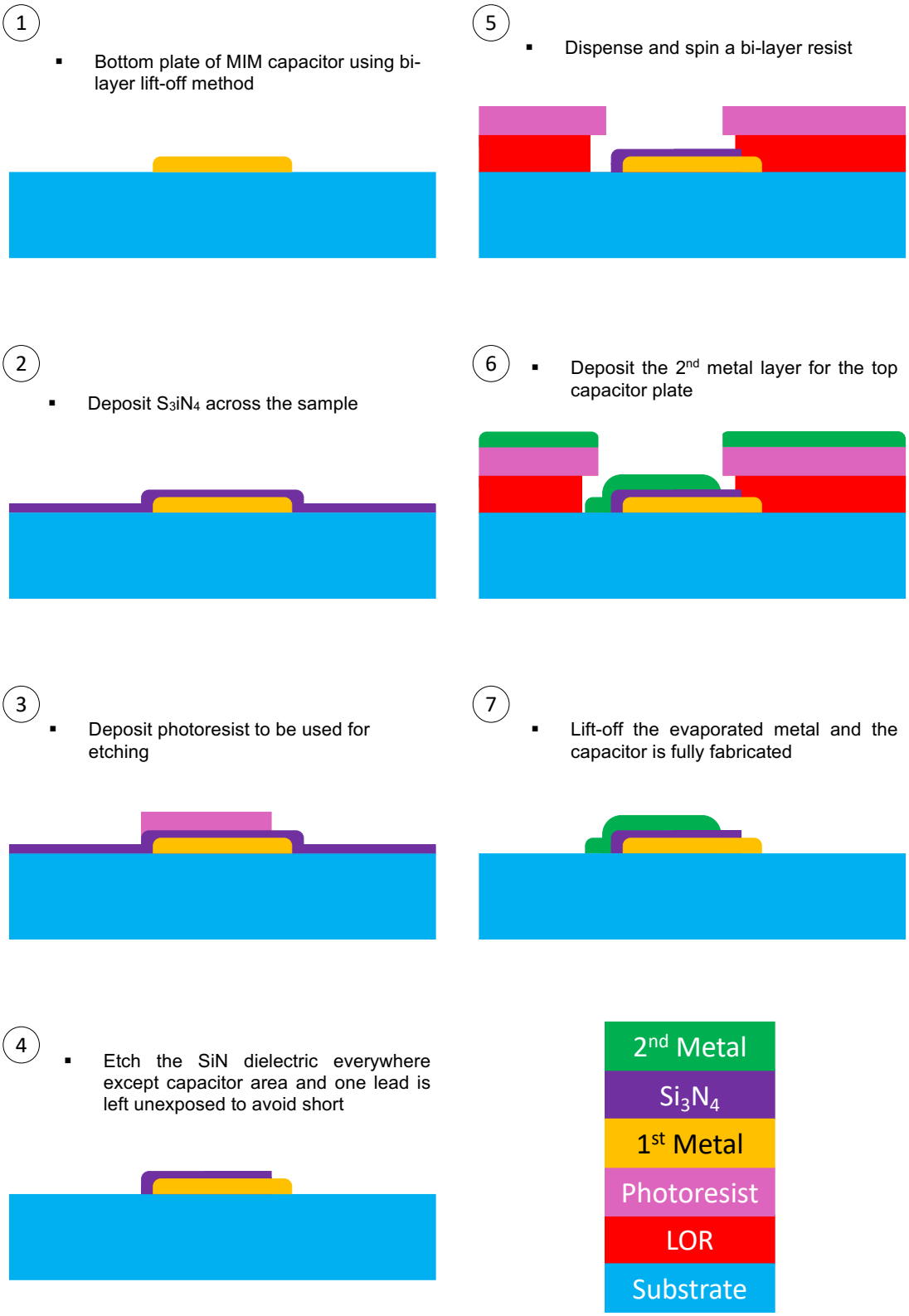


Figure 4.27. MIM capacitor fabrication process

Figure 4.28 illustrates the capacitance of a series MIM capacitor (A = 50×50μm^2) along with the capacitance obtained from the small signal model. The graph shows a decreasing capacitance as a function of the signal frequency because of the substrate conductance which have shown earlier. The capacitance is at its maximum at the lowest end of frequency spectrum with a value of 1.5pF.

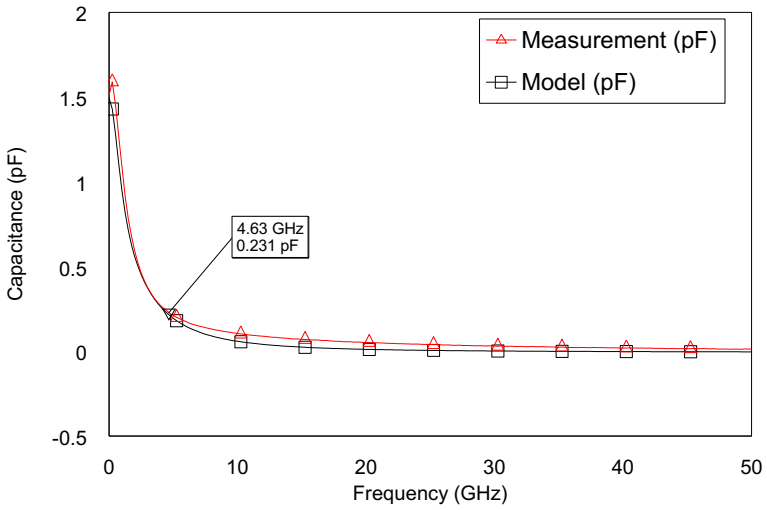


Figure 4.28. Capacitance of a 50×50μm^2 series-MIM-capacitor

The input/output reflection and transmission coefficients plotted on smith chart are shown in **Figure 4.29** with a sweep up to 50GHz. A self-resonance is observed at the point where the transmission coefficient moves from one side of the smith chart to another, and it is situated precisely at the real axis on smith chart as demonstrated in **Figure 4.29** with a plotted mark (4.64GHz). This can be considered a cutoff frequency, beyond which, the capacitor becomes considerably leaky where the signal couples though the dielectric and between the metallic plates effortlessly. From **Figure 4.28**, it is manifest that the capacitance value falls to 0.231pF at the self-resonance point.

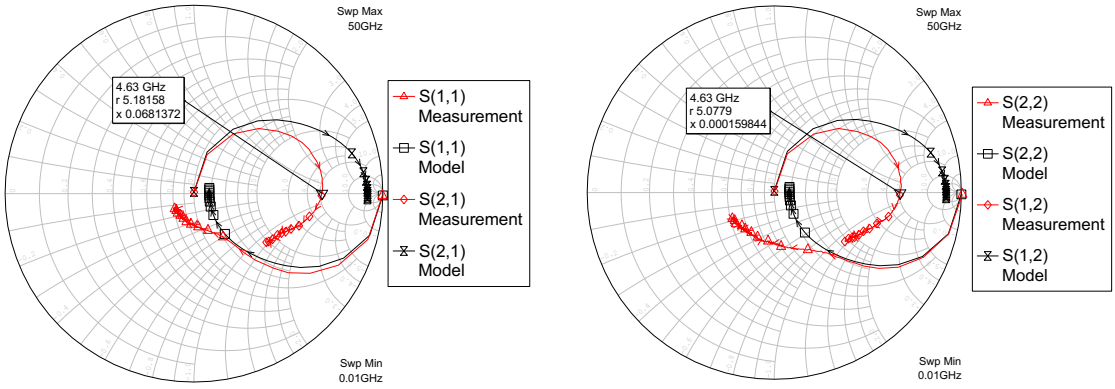


Figure 4.29. Smith chart for 50×50μm^2 series-capacitor

4.3. MMIC Planar Meander Inductor

4.3.1. MMIC Inductor Theory and Design

In its most basic form, a meander inductor as depicted in **Figure 4.30**, is composed of straight conducting sections meandered across the plane. The meander inductor's total inductance is therefore equivalent to the summation of all sections' self-inductances and the negative and positive mutual inductances arising between all combinations of straight sections. Grover marks a significant contribution to the inductance calculation which can be found in [129]. He scrutinised partial inductance, or the contribution of individual sections to total inductance, as well as the geometric mean distance, or GMD.

Generally, meander inductor is a planar and single layer where both leads are situated on the same plane at the top of the substrate. The inductance of a meander inductor, given in nH, is given by the following expression:

$$L(nH) = 2.6[A^{0.0603}H^{0.4429}N^{0.954}D^{0.606}W^{-0.173}] \quad (4.14)$$

where, as illustrated in **Figure 4.30**, *A* is the distance between the input and output pads on one side and the meander inductor turns (60μm), *H* is the height of the inductor (180μm), *N* is the number of turns (3), *D* is the width of meander (45μm) and *W* is width of the transmission line (20μm). These input parameters are plugged into the equation in mm unit length.

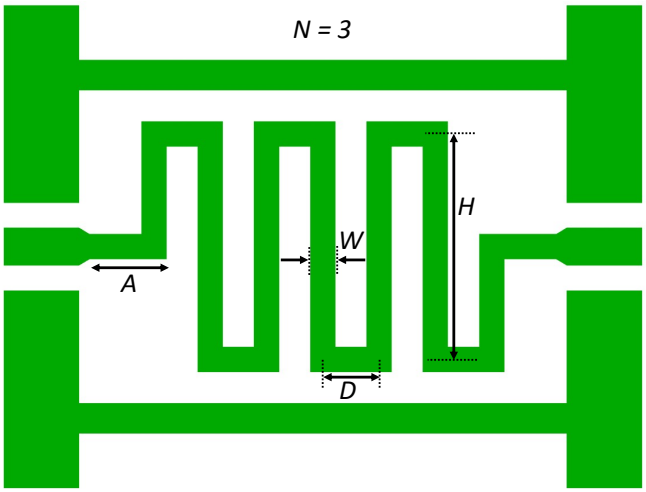


Figure 4.30. Top view of a meander inductor layout

4.3.2. Meander Inductor RF Performance

Beside the microscopic image of the inductor, **Figure 4.31** also shows the EM simulation with the electric current density superimposed on the meander inductor. The maximum current density, occurring at 18GHz, is obtained at the corners of the inductor section, which can be attributed to the current-crowding effect stemmed from the increase resistance at the deep bends. The inductor is then fabricated using bi-layer resists with Ti/Au (40/700 nm).

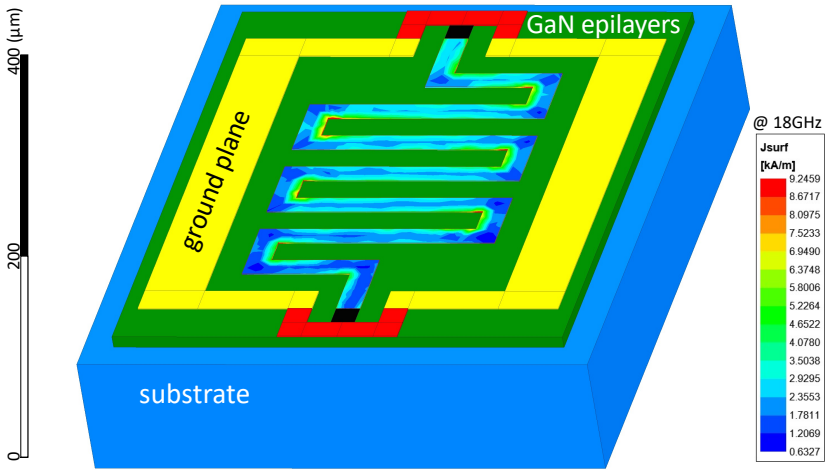


Figure 4.31. Meander inductor 3D electromagnetic simulation

Figure 4.32 illustrates the fabricated inductor small signal model with twelve elements included to understand the RF behavior of the inductor using LR-Si substrate as the wafer on which it is built on. R_S represents the series resistance

of the conducting metal. R_m and L_m represent the resistance and inductance, respectively, due to skin effect at high frequency. L_{prime} is the main inductance value of the fabricated inductor. The reset of the elements denotes the losses introduced by the substrate.

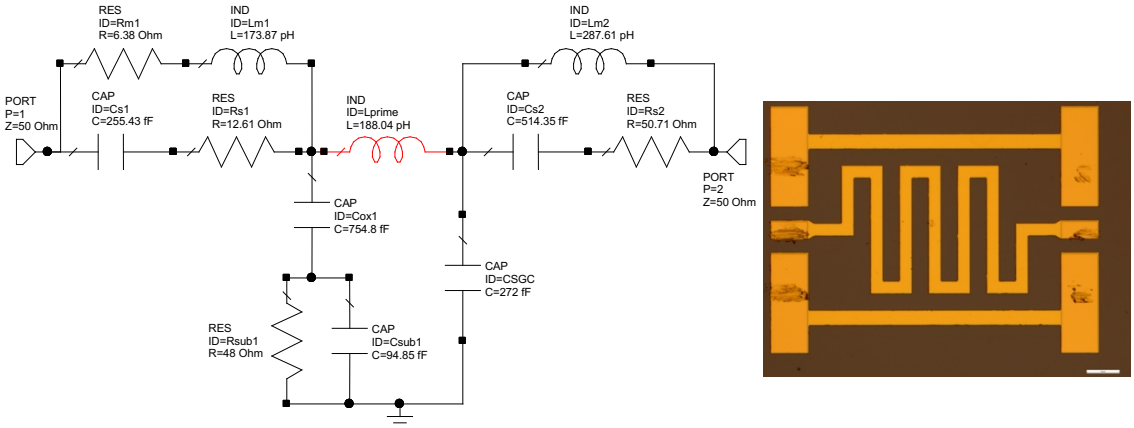


Figure 4.32. Planar MMIC inductor circuit model and a microscopic image of the inductor

Figure 4.33 shows the input/output reflection and transmission coefficients plotted on smith chart charts. A good agreement between the measurement and the small signal model S-parameters. The graph shows all the four S-parameters of a two-port network swept from 10MHz up to 50GHz. In general, the inductor is demonstrating a comparable RF behavior to a transmission line due to its simplicity. In fact, it can be described as a strongly inductive transmission line. Furthermore, the substrate is similarly exhibiting a resistance of less than 50Ω, indicating a very lossy substrate. Therefore, a prime inductance is degraded, and the total prime inductance is less than 200pH.

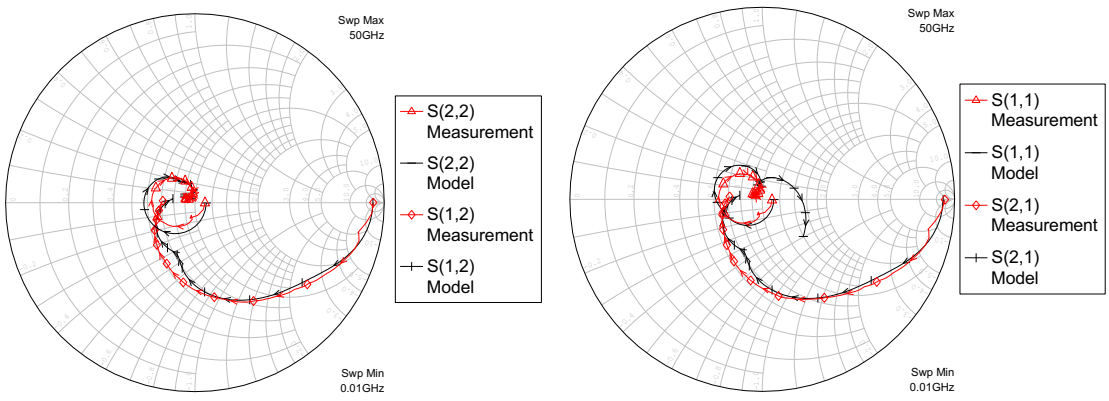


Figure 4.33. Smith chart of the fabricated and model meander

Figure 4.34 shows both the total inductance and the quality factor of the meander inductor. The quality factor is the ratio between the reactance and the resistance of the device. The inductor has a maximum inductance of a little less than 800pH at 6GHz. The inductance is then falls to less than 200pH at approximately 15GHz mark. On the other hand, the quality factor is only reaching a maximum of more than 2 at 6GHz and falls below unity at about 10GHz, which indicates higher resistance, is being acquired than inductive reactance meaning more power is being dissipated due to heat than the power stored as a magnetic field. This further shows the lossy RF performance of the inductor, and it is mostly originating from the LR-Si substrate that has an immense conducing capacity leading to a further loss enhancement in the RF performance.

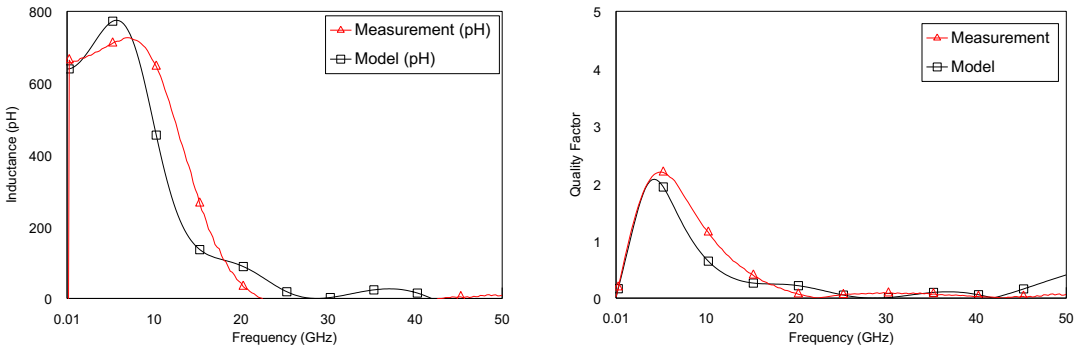


Figure 4.34. Inductance and quality factor

4.4. GaN HEMT Device Dimensions Analysis

4.4.1. Growth of the Material

The devices, in this work, were fabricated using AlGaN/AlN/GaN epitaxy grown on 6-inch p-type low resistivity silicon (LR-Si) substrate by metal organic chemical vapor deposition (MOCVD). The GaN epilayer consists of a 200nm AlN nucleation, 750nm graded buffer of AlGaN, both of which are applied to accommodate the lattice mismatch between the LR-Si substrate and GaN epitaxy to reduce the bow condition on the surface. Subsequently, the active layer of GaN comprises of a 1400nm GaN buffer and channel, 1nm AlN spacer, 25nm $Al_xGa_{1-x}N$ barrier with Al composition of 25% and finally capped with a 2nm GaN to

further manage the tensile strain on the barrier. The wafer from end-to-end is crackfree with a maximum concave bow of only 20µm after exposure to high temperature, around 1050°C, during growth followed by a cooling process. This illustrates that the lattice and thermal mismatch strains are well managed in the buffer layers and the wafer bow is compatible with processing through a commercial Silicon fab. The GaN (002) and (102) X-ray rocking curve FWHMs were 620 and 900 arcsecs respectively, indicating a reasonable crystal quality of the buffer layer. Hall measurement was conducted on the layer using VdP test structure and the following were obtained, a 1.1×10^{13} cm^{-2} carrier density in the channel, a 1700 $cm^2/V\cdot sec$ electron mobility and a 412 Ω/□ sheet resistivity.

4.4.2. Device Process and Layout Definitions

In this work, all levels of device definition were realised using photolithography. **Figure 4.35** illustrates the cross-section of the HEMT devices in this project. **Figure 5.2** shows the various fabrication steps required to realise a fully functioning GaN HEMT. The process commences with the fabrication of alignment markers. After that, the ohmic contacts (source/drain) were realised using standard AlGaN/GaN HEMT metal scheme (Ti/Al/Ni/Au) and annealed at 790°C for 30s. Next, mesa isolation was applied to remove the active layers between devices using a chlorine-based mixture of gases in an ICP-RIE tool. After that, a 100nm S_3iN_4 passivation was deposited by method of plasma enhanced chemical vapor deposition (PECVD) at room temperature.

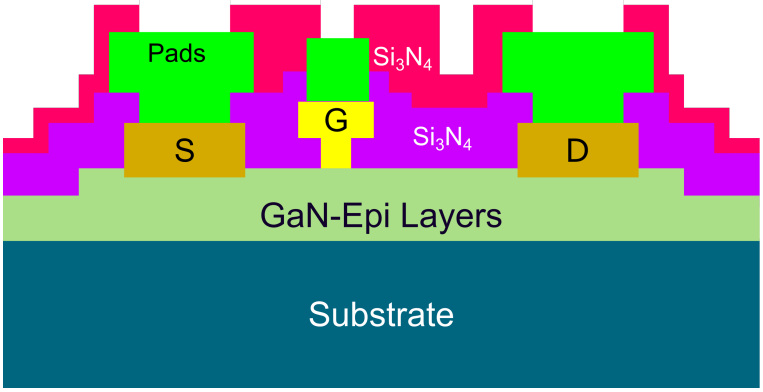


Figure 4.35. Cross-section view of the HEMT fabricated in this project including field plates and 3 layers of Si_3N_4 passivation

Subsequently, gate footprints were realised using low damage SF_6/N_2 plasma etch. The metal (Ni/Au) of the gate and its feed were then evaporated to form the Schottky contact of the device. Finally, after a second S_3iN_4 passivation, the bond pad metal was deposited for measurement using Ti/Au metal-stack as shown in **Figure 5.2**.

Figure 4.36 illustrates the RF HEMT device different dimensions. W_g is defined as the gate width or device width as well. L_g and L_{SD} are the gate length (1μm) and the distance between the source and the drain (5μm) respectively. Drain width (DW) is the length of the drain mid ohmic contact between the dual sources. The study here will focus on both the gate width and the drain width and how it effects the device performance in RF and DC working environments. It is worth noting that the nominal values of the gate length and drain width are 125 and 32μm respectively. The gate to source separation (L_{GS}) is 1.5μm and the gate to drain separation (L_{GD}) is kept at 2.5μm.

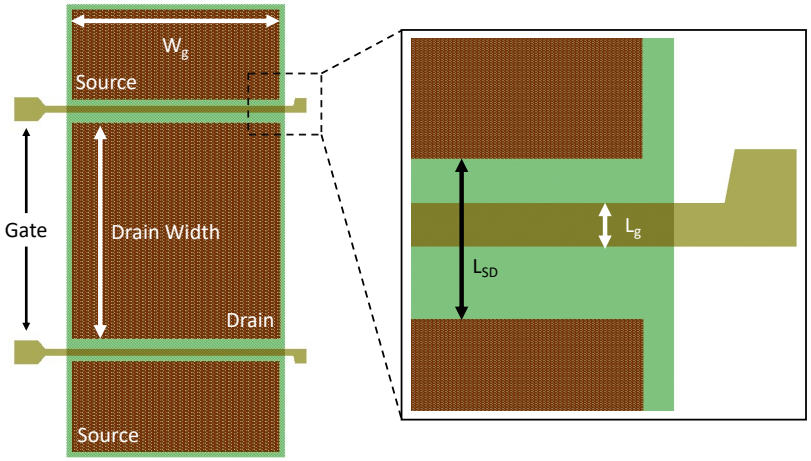


Figure 4.36. GaN HEMT layout and device geometry definitions

4.4.3. Measurements and Discussion

On-wafer DC and RF measurements were performed using a semiconductor parameter analyser (B1500A) and a PNA microwave network analyser (N5227A), respectively. The latter was calibrated from 100 MHz up to 50 GHz with an off-wafer impedance standard substrate (ISS) calibration kit for a 100μm pitch RF-probe utilising a Short-Open-Load-Through (SOLT) calibration procedure at a small signal RF excitation (-20dBm).

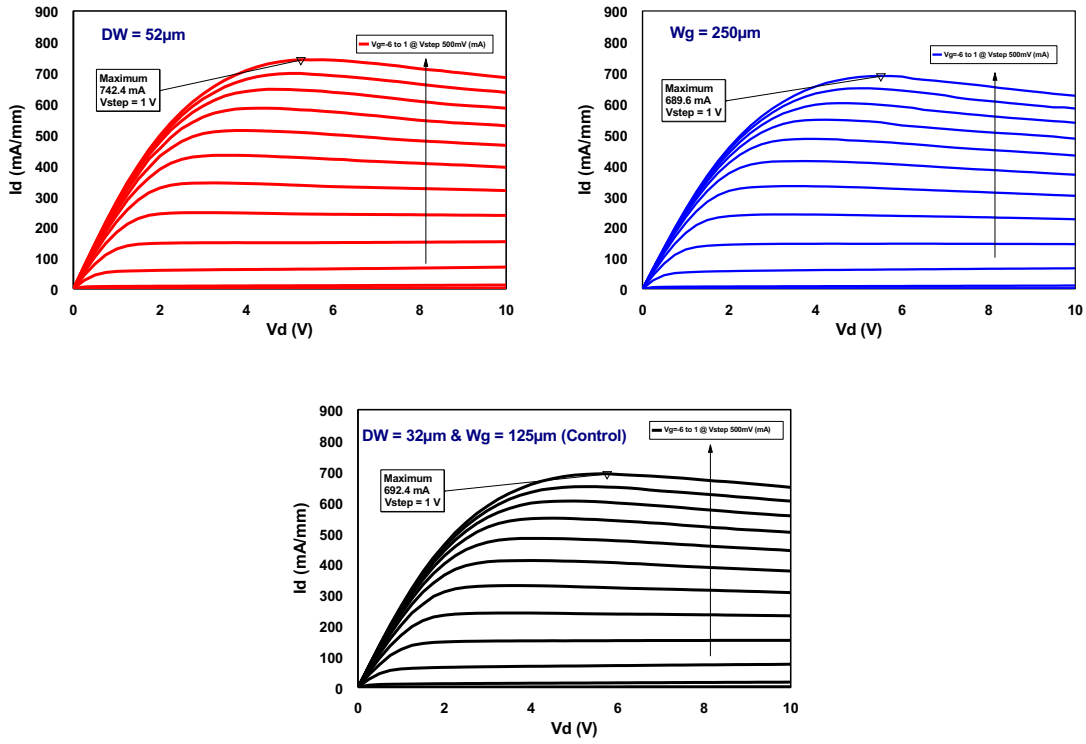


Figure 4.37. I-V family curves of 2-finger with different W_g and DW

Figure 4.37 illustrates the typical DC output characteristics and GaN *I-V* relation for a 2-finger × 1.0µm × 125µm wide device and 32µm drain width, which is the nominal values used for the control device throughout the project. Additional devices are fabricated at a different device width (W_g = 2-finger x 250 µm) and drain width (DW = 52 µm) as well to observe the effects on the device performance as function of dimensions. The voltage applied at the gate and drain terminals varies from -6 to 1.0V at a step of 0.5V and 0 to 10V at a step of 1.0V, respectively, for all devices. Maximum current and power handling obtained as the drain width increases, possibly, due to a higher saturation velocity. Nonetheless, enhancing the device width (gate width) degrades the power capability slightly, which can be attributed to the increase of self-heating effect manifested by the steep fall of current seen above 6V in comparison to the other devices.

An excellent pinch-off behavior is exhibited especially in smaller DW devices acquired at -4V gate voltage. As depicted in **Figure 4.38**, at a bias of V_{ds} = 4.5V

and V_{gs} = -3V, a maximum DC transconductance was obtained with the device of a 52 μm DW having the highest G_m, which is also directly caused by the increase of saturation velocity due to larger area for electrons to tunnel across between the source and the drain. However, the area increase is limited by the transfer length phenomena occurring between metals and semiconductors. This will be discussed in the subsequent section.

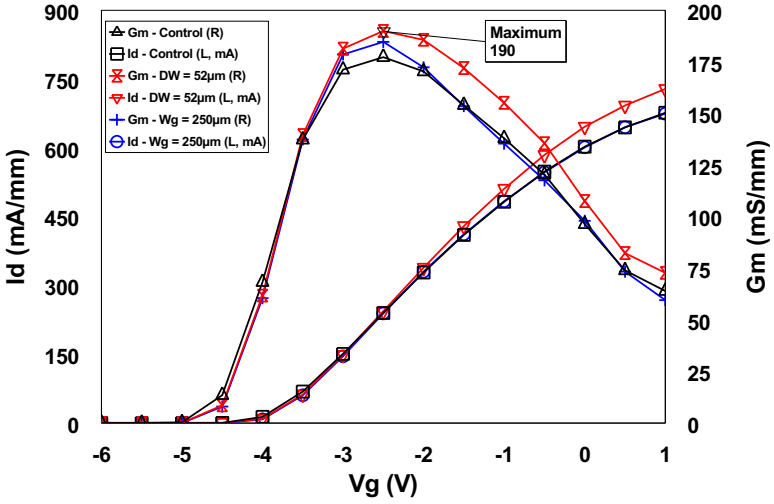


Figure 4.38. The transfer characteristics and the DC transconductance at V_{ds} = 4.5V and V_{gs} = -3V

Figure 4.39 shows both the drain current below pinch-off and the gate leakage at a drain bias of 4.5V. The latter shows a considerable leakage current reaching as high as 1mA/mm when the 52μm DW device is strongly pinched off. The gate leakage, then falls steadily to the same level as the other two devices, less than a μA, as a function of the gate bias positively increasing, which causes the gate diode to breakdown and loses the control over the source-drain channel.

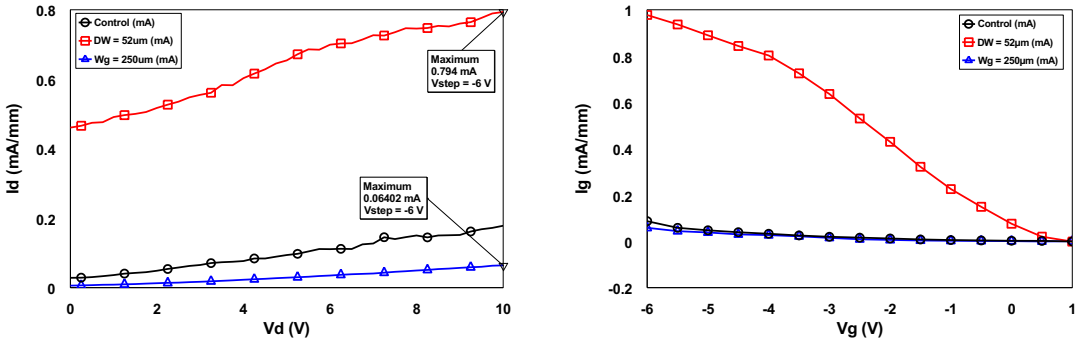


Figure 4.39. Drain current (I_d) and gate leakage (I_g) at V_g = -6V V_d = 4.5V, respectively

On the other hand, the drain current also shows a poor pinch-off for the wide drain device with a range between 0.5 to 0.8mA/mm of drain leakage across the entire span of the drain bias from 0 to 10V.

To further analyse the effects of dimensions, gate current is measured as a function of applied drain bias below and above the device pinch-off point as shown in **Figure 4.40**. The results further demonstrate that the increase of drain width is the main source of gate and drain leakage increase. However, increasing the device width show little effects with respect to leakages within the GaN HEMT devices fabricated on LR-Si substrate. This indicates that the HEMT devices are well insulated from being in a direct contact with lossy substrate and that the GaN epi-layers offer an excellent performance due to high quality of wafer design and growth.

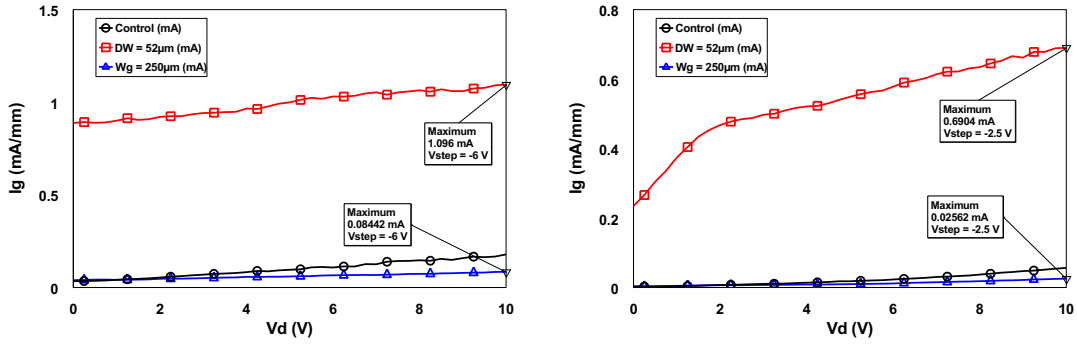


Figure 4.40. Gate leakage as a function of drain bias with a gate voltage of -6V (left) and -2.5V (right)

Next, a comparison of the power density attained by the devices is analysed to observe the effects of dimension scaling on the performance of the transistors. **Figure 4.41** depicts the devices' power maximum output capability as a function of the applied drain voltages achieved at a unity gate voltage. Furthermore, **Figure 4.41** depicts the difference in power between the examined devices and the control, demonstrating a maximum delta at high drain voltages. With more than 60% increase in the device drain width from 32 to 52μm, only 5.5% enhancement of power density (Watt per mm) was observed as summarised in **Table 4.1**. This is due to the limitations imposed by maximum transfer length, through which the current can flow between the ohmic contacts (source/drain), and the semiconductor [130] as demonstrated in **Figure 4.42**. In this project, the maximum transfer length (L_T) was in the order of a unity micrometer or less. Hence, most of the current transport is occurring in within this section of the device.

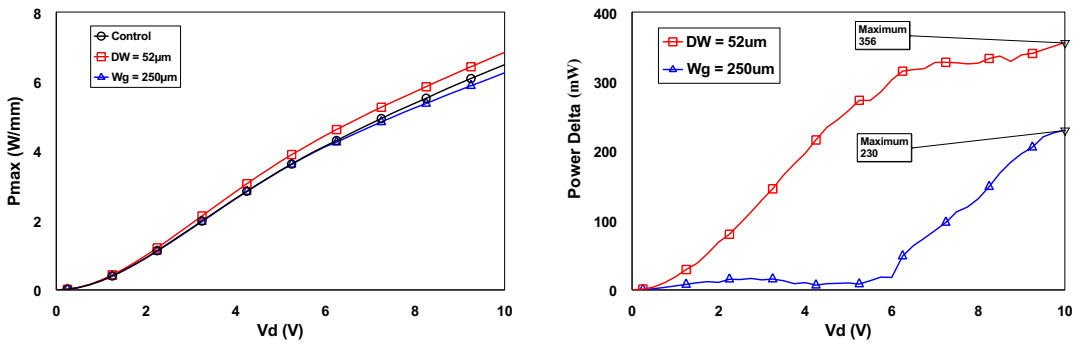


Figure 4.41. Power exhibited by the devices at V_g = 1.0V

Scaling the device width from 125 to 250μm, however, exhibited almost no change to the power density nor to the maximum normlised current per mm.

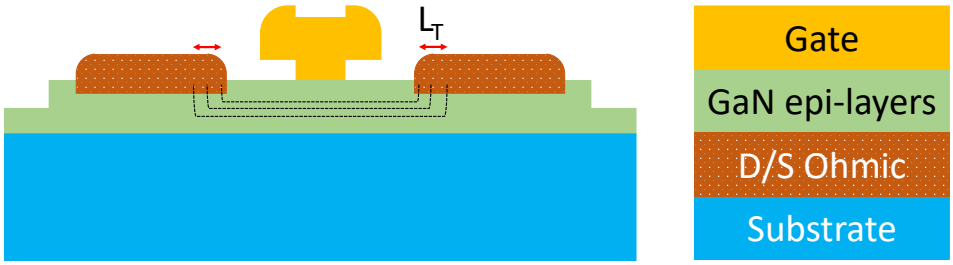


Figure 4.42. Current transport (dotted lines) between ohmic contacts and semiconductors in GaN HEMTs

Figure 4.43 illustrates the de-embedded small-signal gain characteristics of 1.0μm 2-finger GaN- based HEMTs on LR-Si. The devices were biased at their best RF performance where the highest current gain (H21) and Maximum Available Gain (MAG)/power gain existed. Since the intersection of both H21 and MAG with frequency, at which H21 (f) = MAG (f) = zero dB, occurs within the measurement frequency range (100 MHz – 50 GHz), extrapolation of H21 and MAG using a -20 dB/decade slope is not required. The results show negligible variation observed between the devices f_T parameter when a gate and drain width scaling is performed. Further, the results also reveal a 20% reduction in f_{max} as the device width is enhanced from 125 to 250μm. This is attributed to the increase of gate parasitic and gate-drain capacitance. These findings agree with Eq. (2.50), where is f_{max} is inversely proportional to the gate resistance (R_g) and C_{gd}. This was verified by the development of a small signal model as given in **Table 4.2**. Considering Eq. (2.41), it is evident that R_g is directly proportional to the device width. Hence, an increase in R_g is acquired due to the device width enhancement. Likewise, C_{gd} is also increased due to the increase of the overall device area. Similarly, the enchantment of drain width causes a reduction approximately 13% in f_{max}.

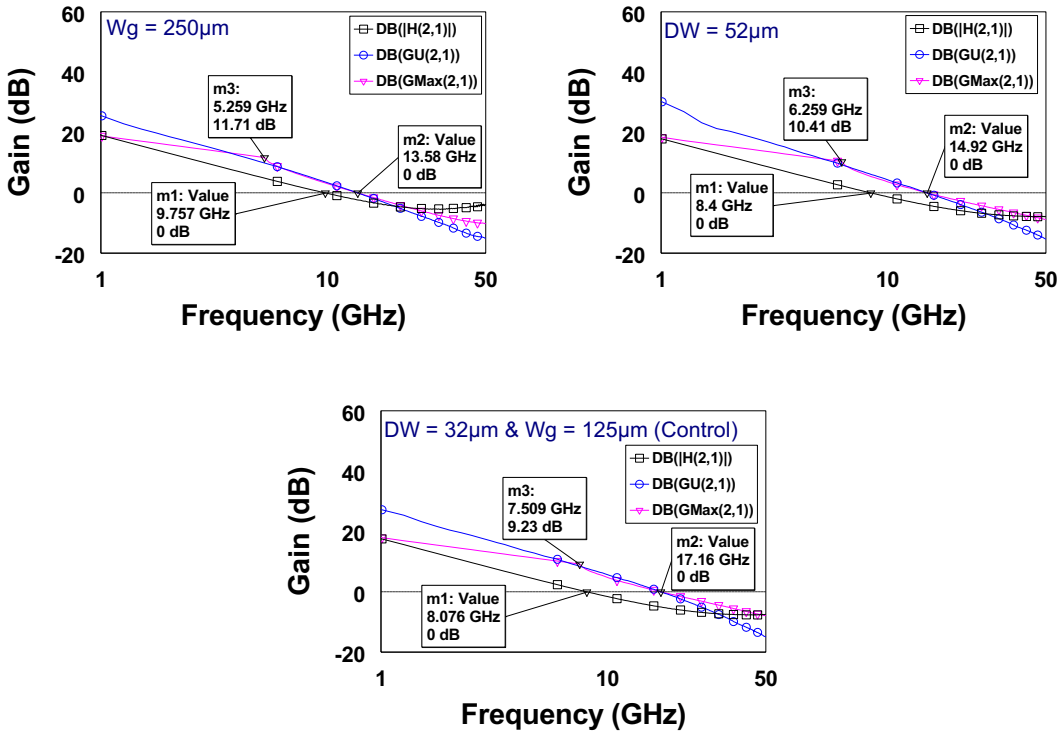


Figure 4.43. GU, H21 and G_{MAX} gains as a function of log frequency in GHz after pads de-embedding

The complete DC and RF results for the fabricated devices are summarised in **Table 4.1**. Although the enhancement of the drain width increases the power density of the device and slightly lowers the on-resistance, limited RF effects was acquired expect for the maximum oscillation frequency as explained above. This can be attributed to the quality of growth and the excellent insulation of the substrate which led to the minimisation of electrical coupling between the substrate and the fabricated devices. Additionally, the high performance of these GaN-on-Si devices is due to well-engineered material growth, device layout, and manufacturing process quality, as well as suitable passivation methods employed in this project.

Table 4.1. Summary of DC and RF parameters of HEMT with different device dimensions

	Parameter	W_g = 125µm & DW = 32µm (Control)	W_g = 250µm & DW = 32µm	W_g = 125µm & DW = 52µm
DC	I_{DSS} (mA/mm)	692	690	742
	Max $P_{density}$ (W/mm)	6.48	6.25	6.84
	V_P (V)	-4.0	-4.0	-4.0
	R_{ON} (Ω·mm)	3.57	3.68	3.32
	G_m (mS/mm)	177	184	190
RF	f_T (GHz)	8.08	9.76	8.4
	f_{max} (GHz)	17.16	13.58	14.92

Table 4.2. Dimension scaled HEMT devices small-signal model parameters biased at V_d =4.5 V and V_g = -2.5V with an RF power injection level at -20dBm

Device	Control Device	W_g = 250µm	DW = 52µm
f_T (GHz)	**8.08**	**9.76**	**8.4**
f_{max} (GHz)	**17.16**	**13.58**	**14.92**
C_{pg} (fF)	**153**	199	264
C_{pgd} (fF)	**115**	111	105
C_{pd} (fF)	**190**	164	261
L_g (pH)	**24**	34	26
L_d (pH)	**30**	30	46
L_s (pH)	**0.51**	0.01	5.7
R_g (Ω)	**6.0**	9.2	6.4
R_d (Ω)	**6.6**	3.9	8.1
R_s (Ω)	**4.7**	4.1	6.5
R_{in} (Ω)	**3.5**	1.42	4.8
R_{ds} (Ω)	**321**	177	246
g_m (mS)	**60**	81	79
C_{gs} (fF)	**985**	949	1,105
C_{gd} (fF)	**24.8**	34.9	22.6
C_{ds} (fF)	**34.6**	10.1	18.3
τ (ps)	**4.9**	1.2	4.5

4.5. Conclusion

In this chapter, various devices, passive and active, were simulated fabricated and modelled to understand the behavior of the wafers and the effects of the lossy silicon substrates. Loss mechanism analysis was performed for GaN grown

on various substrates based on the CPW distributed element circuit model to compare their performance. A CPW transmission line, RF PCM, MIM capacitor, meander inductor and HEMTs were fabricated using GaN-on-LR-Si and the results confirm the lossy behavior of the substrate and the maximum operation frequency limits the substrate exhibited only beyond 10GHz.

5. THE EFFECT OF MINIATURE MESA EXTENSION FOR A PLANAR SUBMICRON GATE FORMATION

In this chapter, a new approach is presented to overcome issues in AlGaN/GaN HEMTs such as, metal discontinuity of the gate stemmed from conventional mesa isolation. As a result, this usually requires a careful mesa etch process to procure an anisotropic mesa-wall profile. An alternative technique is the use of ion implantation for device isolation instead of conventional mesa for a planar device formation. However, ion implantation is a costly process and not always easily accessible. In this work, the proposed method is to simply extend the mesa, merely below the gate, just enough to accommodate the gatefeed, thereby ensuring the entire gate is planar in structure up to the gatefeed.

The newly developed device exhibited no compromise to the DC and RF performance. Conversely, it produced a planar gate configuration with an enhanced transconductance and a lower gate leakage while the etch process is considerably simplified. However, a small (< an order of magnitude) drain leakage increase was observed. The proposed structure can be employed to lower the gate leakage current in AlGaN/GaN HEMTs typically arising from conventional mesa etch due to a direct contact between the gate and two-dimensional electron gas (2DEG) at the mesa sidewall. Finally, a deeper etch is feasible, down to the substrate for further device-to-device isolation or heat sink formation, without any concern about gate discontinuity since its critical portion is elevated above the mesa extension.

5.1. Review of Isolation Approaches

GaN is the most attractive semiconductor due to its inherent characteristics such as electron mobility and saturation velocity enabling higher the feasibility of high power devices at microwave frequency with a considerably enhanced power density [131]–[135]. Currently, HEMT fabrication includes a device isolation step

performed by a conventional mesa etch or ion implantation to suppress the two-dimensional-electron-gas (2DEG) and electrically insulate devices. Although a 3D-structure device is obtained due to physical removal of material, the former (mesa) is widely used for cost purposes. However, the introduction of a nonplanar structure in HEMTs results in high gate leakage current, which degrades noise performance in RF amplifiers and can drive the device into breakdown prematurely [136], [137]. Also, possible metallic discontinuity of the gate at the mesa edge especially at small gate length $L_g \leq 1.0\mu m$ as shown in **Figure 5.1**.(a). Besides, in a mesa isolation, etch depth is critical for reproducible, optimized device and circuit performance. Under-etching causes current leakage and poor pinch-off of HEMTs, affects bias levels in circuits, and alters transmission line impedances [138].

In contrast, ion implantation isolation, as presented in **Figure 5.1**.(b), preserves the planar structure of the device but at the expense of a considerably higher cost [139]. Additionally, at near-surface ion implants greatly degraded the resistivity of the damaged GaN. The considerable decrease in resistivity of the implant-damaged GaN after annealing at relatively low temperatures would most likely limit the use of ion implantation to lower temperature applications [140], [141]. Furthermore, the primary drawback of the ion implantation isolation process in semiconductors, in general, is predominantly associated with the lattice disorder triggered by the implanted ions. The ion implantation with high-level concentrations of acceptors is commonly required to offset the existing electron background in GaN and to achieve the transition to p-type because of the high background electron concentration present within the as-growth GaN material. Nevertheless, the quality of the crystalline structure of the GaN material is considerably degraded by the implantation induced damage resulted from the implantation process with high dopant concentrations [142].

Other researchers have examined alternative methods such as thermal oxidization as reported in [143], [144]. However, this process can affect the 2DEG beneath the actual device due to high temperature sample exposure for long duration, up to 900°C and 30min, respectively. Finally, air bridging the gate has also been investigated as reported in [145]–[147]. Nevertheless, air bridging the

gate is a complex process to be implemented [139] and can reduce device reproducibility and yield.

In this chapter, a novel approach is provided to overcome the existing tradeoff between cost and 3D-structure concerns. A miniature extension from the mesa is employed to accommodate the gate-feed, which is the interconnect between the gate itself and the measurement bond pads (or transmission lines in integrated circuits). As a result, this ensures a gate continuity and reduces the gate leakage current since the critical section of the gate metal is positioned planarly on the mesa/extension in its entirety as illustrated in **Figure 5.1**.(c) thus, preventing a direct contact between the gate and the 2DEG. Moreover, the bond pads or transmission lines are large features with a Si_3N_4 passivation underneath hence a metal discontinuity and a direct 2DEG contact, respectively, are implausible to be present.

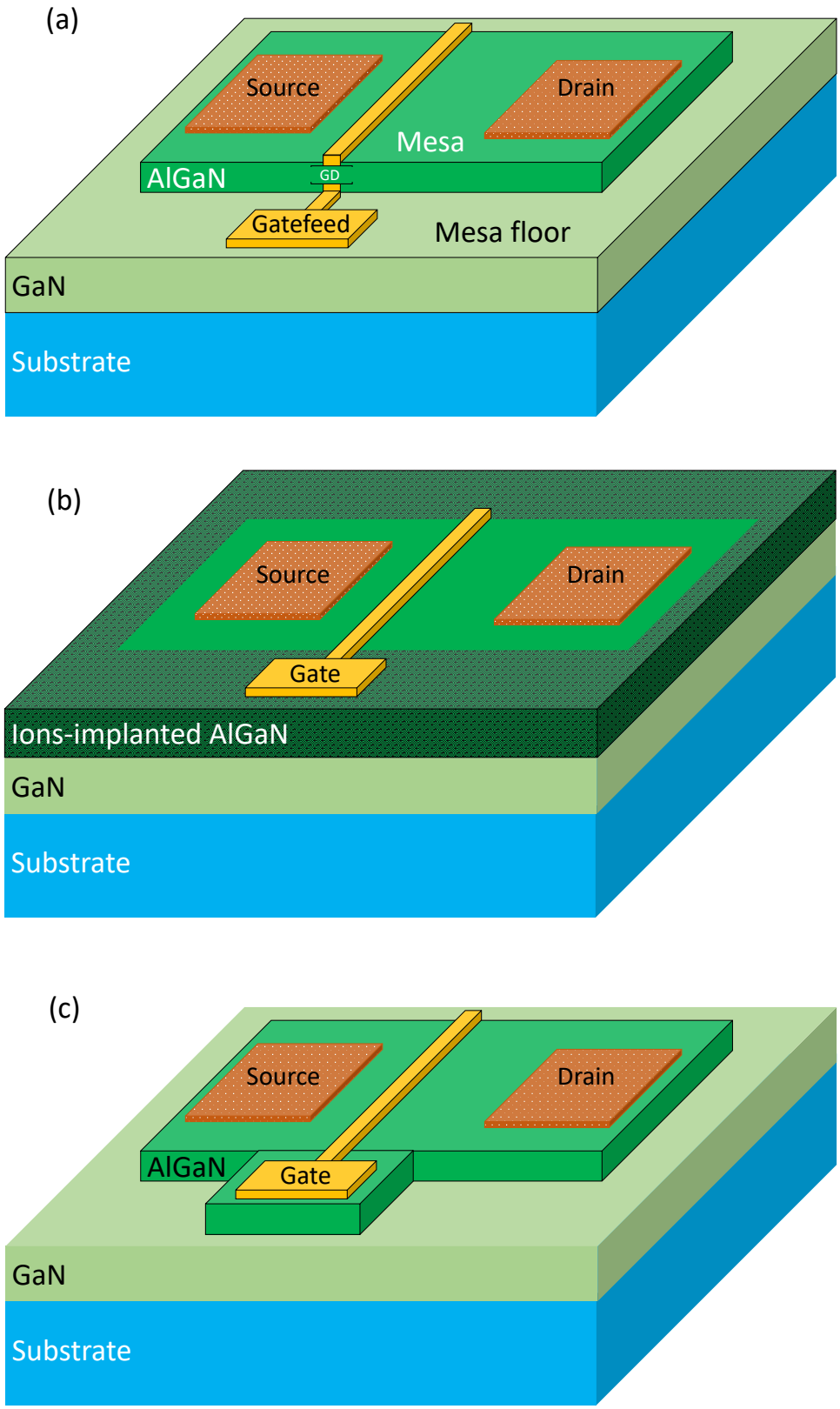


Figure 5.1. Device isolation, (a) conventional mesa, (b) ion implantation، and (c) proposed planar device with a gate-feed on a miniature mesa-extension

5.2. Gate-feed on a Miniature Mesa-Extension for a Planar Structure

5.2.1. Growth of the Material

The devices, in this work, were fabricated using AlGaN/AlN/GaN epitaxy grown on 6-inch p-type low resistivity silicon (LR-Si) substrate by metal organic chemical vapor deposition (MOCVD). The GaN epilayer consists of a 200nm AlN nucleation, 750nm graded buffer of AlGaN, both of which are applied to accommodate the lattice mismatch between the LR-Si substrate and GaN epitaxy to reduce the bow condition on the surface. Subsequently, the active layer of GaN comprises of a 1400nm GaN buffer and channel, 1nm AlN spacer, 25nm $Al_xGa_{1-x}N$ barrier with Al composition of 25% and finally capped with a 2nm GaN to further manage the tensile strain on the barrier. The wafer from end-to-end is crackfree with a maximum concave bow of only 20µm after exposure to high temperature, around 1050°C, during growth followed by a cooling process. This illustrates that the lattice and thermal mismatch strains are well managed in the buffer layers and the wafer bow is compatible with processing through a commercial Silicon fab. The GaN (002) and (102) X-ray rocking curve FWHMs were 620 and 900 arcsecs respectively, indicating a reasonable crystal quality of the buffer layer. Hall measurement was conducted on the layer using VdP test structure and the following were obtained, a 1.1×10^{13} cm^{-2} carrier density in the channel, a 1700 $cm^2/V\cdot sec$ electron mobility and a 412 Ω/□ sheet resistivity.

5.2.2. Device Process

In this work, all levels of device definition were realised using photolithography. The process commences with the fabrication of alignment markers. After that, the ohmic contacts (source/drain) were realised using standard AlGaN/GaN HEMT metal scheme (Ti/Al/Ni/Au) and annealed at 790°C for 30s. Next, mesa isolation was applied to remove the active layers between devices using a chlorine-based mixture of gases in an ICP-RIE tool. After that, a 100nm S_3iN_4 passivation was deposited by method of plasma enhanced chemical vapor deposition (PECVD) at room temperature.

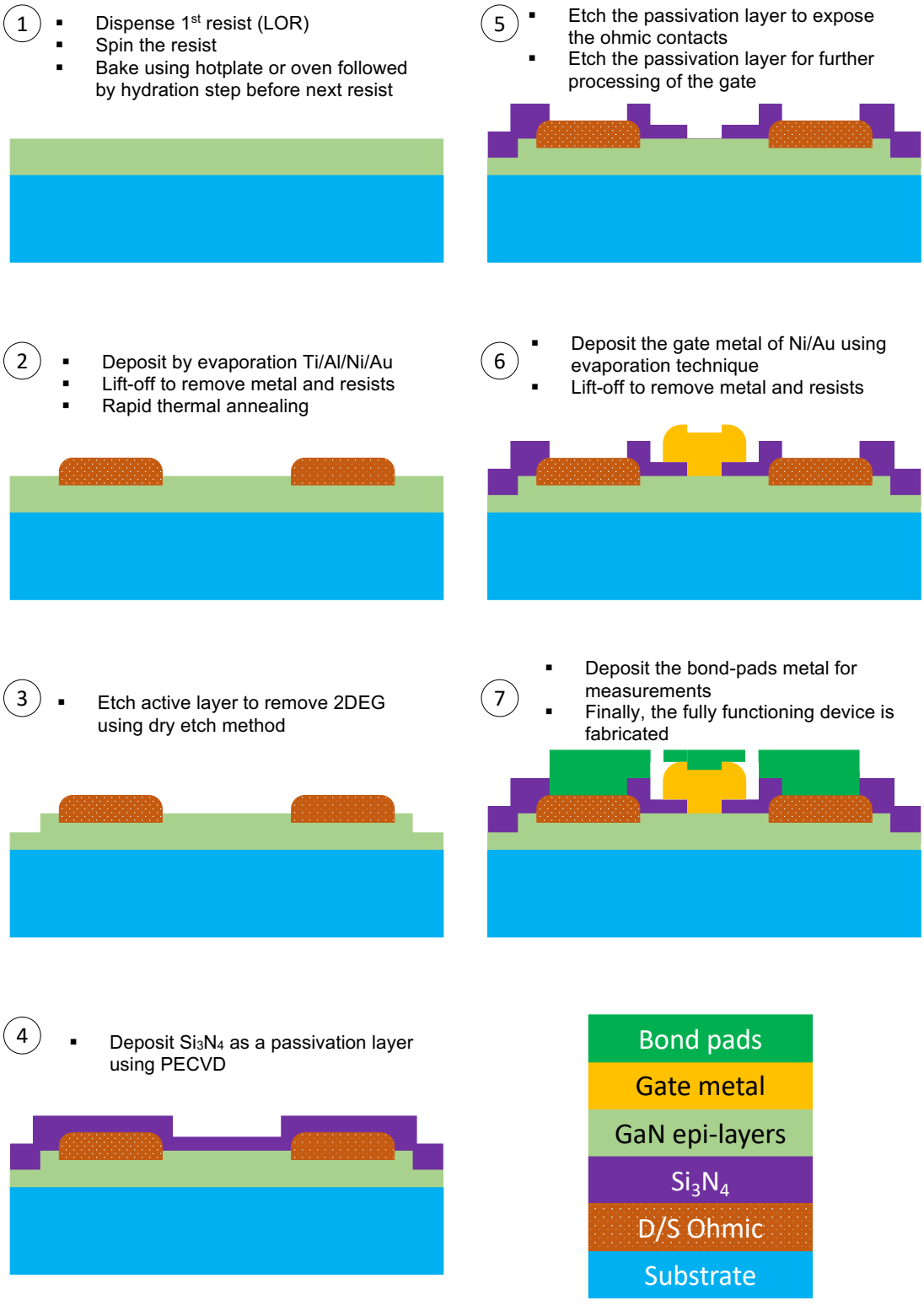


Figure 5.2. AlGaN/GaN heterostructure HEMT's main features fabrication steps

Subsequently, gate footprints were realised using low damage SF_6/N_2 plasma etch. The metal (Ni/Au) of the gate and its feed were then evaporated to form the Schottky contact of the device. Finally, after a second S_3iN_4 passivation, the bond pad metal was deposited for measurement using Ti/Au metal-stack. The complete GaN HEMT fabrication process flowchart is demonstrated in **Figure 5.2**.

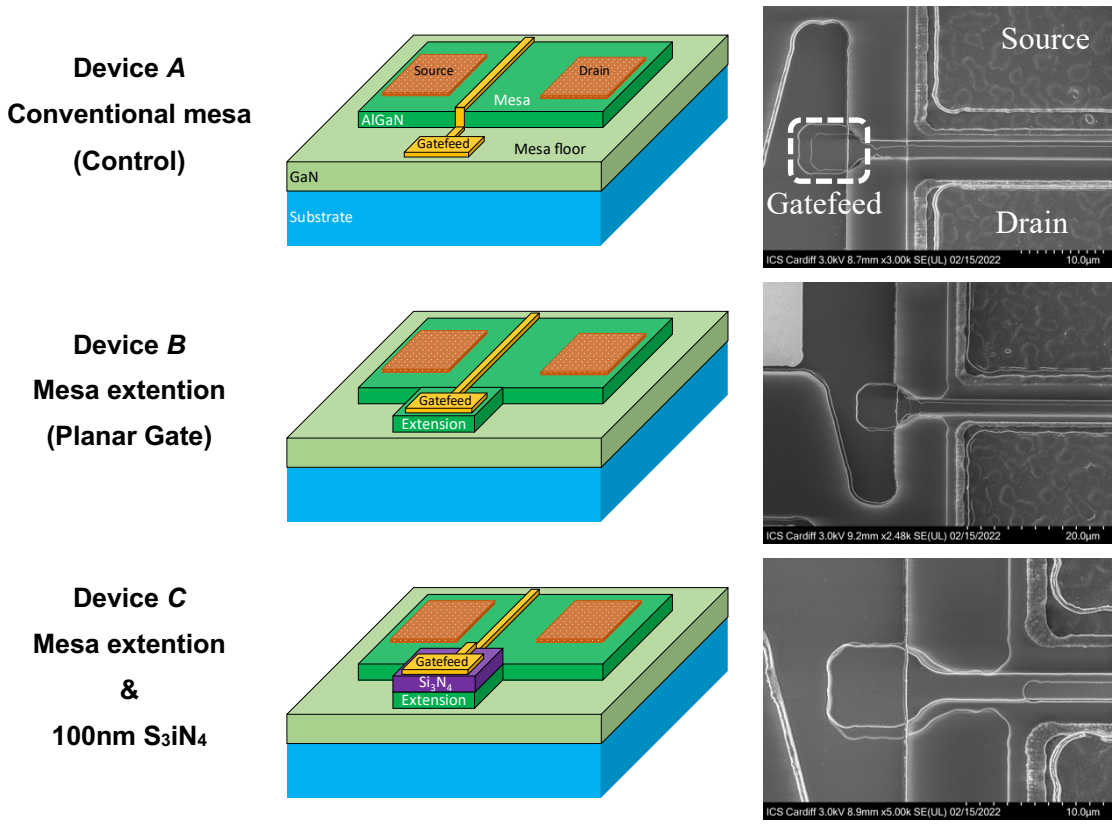


Figure 5.3. 3D cross-section view and bird's-eye view SEM images of the proposed and control devices, all devices are passivated with Si_3N_4 but only the gate of device *C* is affected by its presence hence it is shown in the demo graphs

5.2.3. Design of the Proposed Devices

In this work, the proposed device is fabricated into two different structures, beside the conventional HEMT (device *A*), with respect to the location of the gate-feed, directly on the miniature mesa extension and elevated above the extension by a 100nm of Si_3N_4, annotated by device *B* and *C*, respectively. The mesa extension, as shown in **Figure 5.3**, is designed to accommodate the gate-feed. Hence, it is larger than gate-feed by at least 0.5-1.0μm from the outward three sides (farthest

from the device) to account for any potential misalignment due to limited resolution of optical lithography. Both proposed structures are compatible with the conventional GaN HEMTs process, therefore realisable without any additional fabrication requirements.

5.2.4. Leakage Current & Device Isolation

As depicted in **Figure 5.4**, three factors were applied to alter the leakage currents, at the gate and the drain electrodes, in this experiment, gatefeed location with respect to mesa/mesa floor, gatefeed dielectric and the direct contact with 2DEG confinement at the mesa sidewall. The latter is present only in device *A*, which results in an increase in gate leakage below the pinch-off point where electrons can tunnel through the gate to the 2DEG as the gate voltage is negatively increasing. On the other hand, device *B* and *C* exhibited a considerable reduction in gate leakage at strong pinch-off due to lack of direct contact between the gate and the 2DEG channel as shown in **Figure 5.5**.(a).

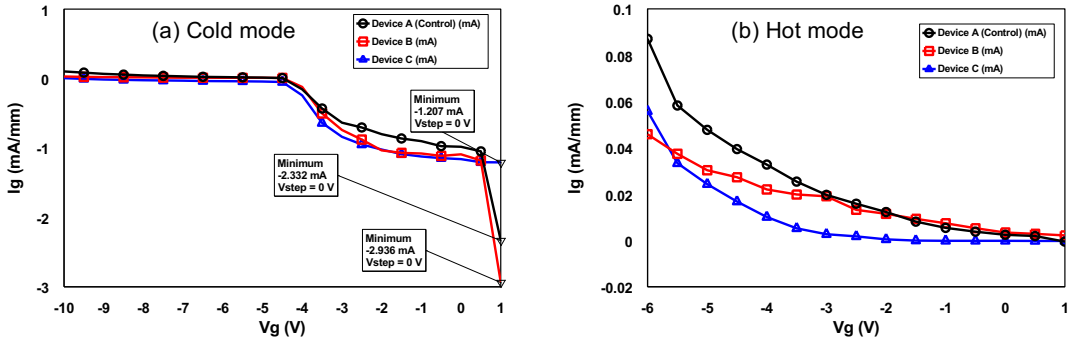


Figure 5.4. Gate leakage in (a) cold mode where biasing is applied only to the gate contact and (b) hot mode where biasing is applied to both the gate and the drain contacts

Further reduction in gate current is especially observed for device *C* emanating from the existence of Si_3N_4 dielectric below the gate-feed. However, when the devices are conducting, a slightly higher gate leakage is apparent in device *B* in comparison with device *A* due to the presence of an active layer below the gate-feed, which was suppressed in device *C* owing to the dielectric deposition beneath the gate-feed as depicted in **Figure 5.5**.(b). The 2DEG in the active area below the gate-feed can be substantially depleted using O_2 treatment as

demonstrated in [148]. Additionally, all of the devices exhibited a saturation in the gate current below pinch-off, which can be attributed to the electric field at the gate edge of the AlGaN that equally saturates at the pinch-off (V_g = -4V in this case) [149].

Additionally, **Figure 5.4**.(b) demonstrates approximately one order of magnitude of gate leakage reduction between planar and non-planar gate-feed at various gate bias points, which is comparable to the decrease obtained by using $^{131}Xe^+$ and O^+ ion-implantation process as given in [150] and [151], respectively. **Figure 5.5** illustrates the gate leakage as a function of the applied drain voltage. Below pinch-off, where the gate bias is set at -6V, device exhibited the lowest leakage as shown in **Figure 5.5**.(a).

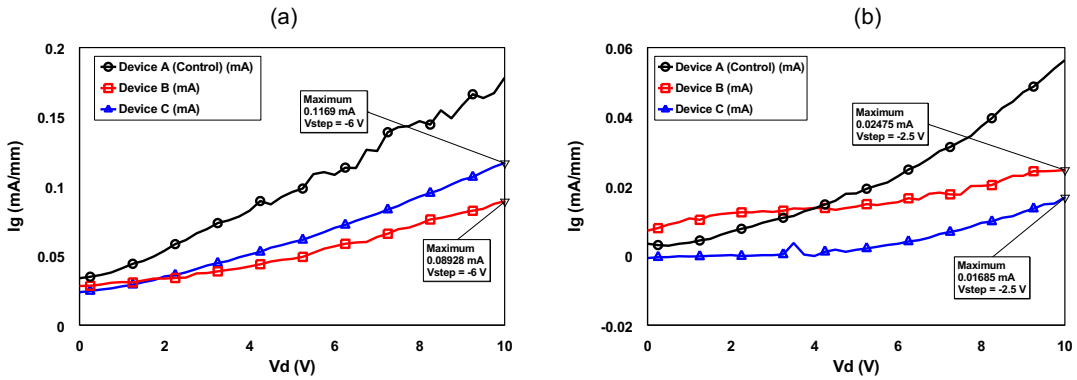


Figure 5.5. Gate leakage as a function of drain bias, below and above pinch-off (a) and (b) respectively

Moreover, when the device is turned-off, the gate controllability over the device pinch-off is degraded as the distance is increased between the gate-feed and the 2DEG, from a direct contact as in the case of device *A* and approximately 28nm for device *B*, to more than 100nm of separation for device *C*, which translates into 0.09, 1.13 and 34.2 mA of drain leakage respectively, at V_{ds} = 10V and V_{gs} = -6V as shown in **Figure 5.6**.

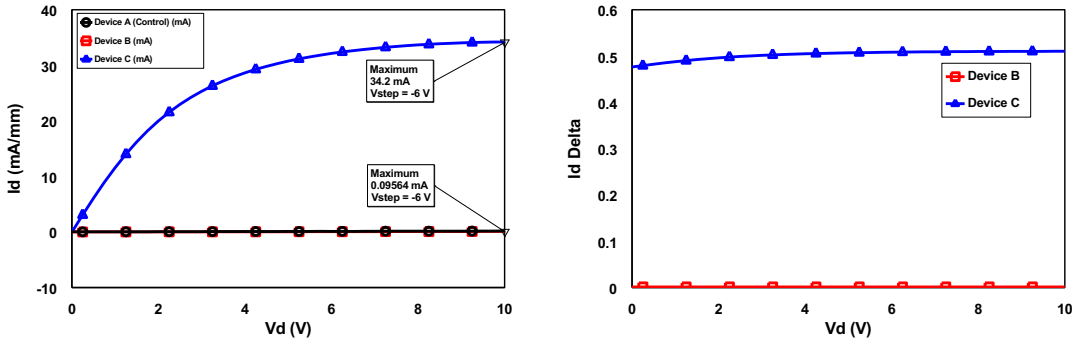
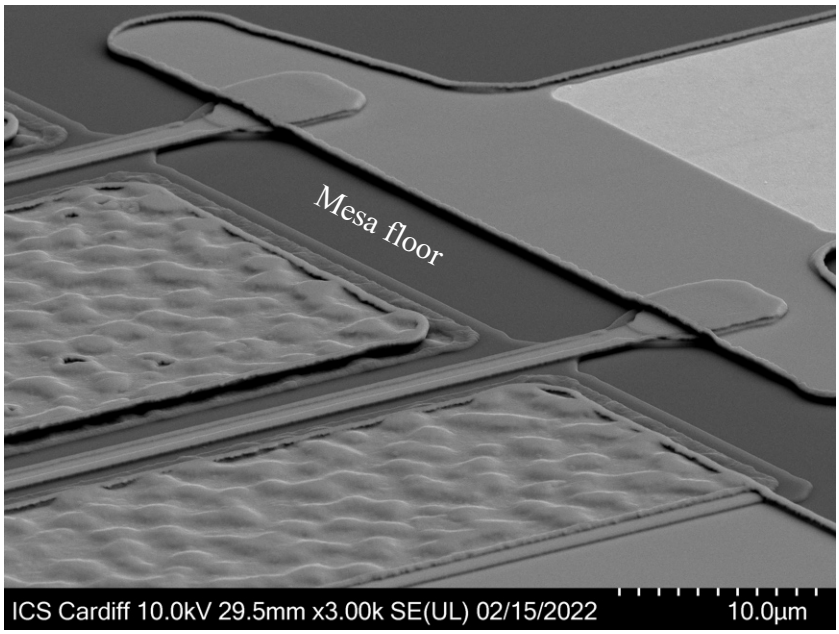


Figure 5.6. Drain leakage below pinch-off gate bias

Device-to-device current is found to be in the order of unity μA/mm at 10V for the three different-structure devices (*A*, *B* and *C*) where device-to-device separation is kept uniformly at 300μm. Furthermore, all devices which included the proposed mesa extension clearly yielded no GD issues across the sample since the entire gate and its feed are formed planarly, whereas devices without the mesa extension, suffer from GD phenomena, which was manifested by the device failure to pinch-off for more than fifth of the devices (*A* and *C*) across the sample. This number of failed devices is likely to be higher at submicron gate lengths or if a deeper etch is required. Also, the mesa sidewall profile consideration, in the sense of etch steepness and anisotropy, becomes critical, which can be mitigated by using the proposed mesa extension as illustrated in **Figure 5.7**.

Device *B*



Device *C*

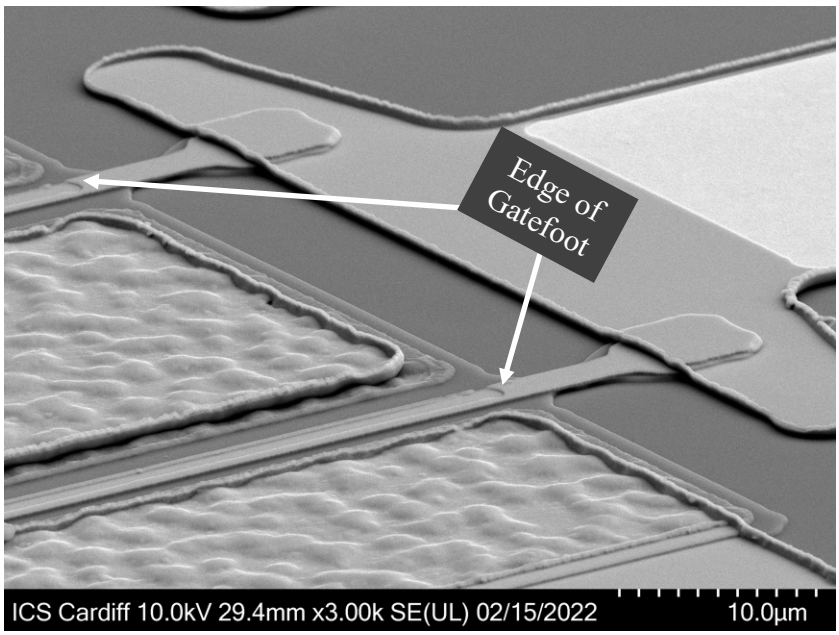


Figure 5.7. SEM images of device *B* (planar, mesa extension) and *C* (+100nm Si_3N_4 elevation)

5.2.5. DC and RF Performance

On-wafer DC and RF measurements were performed using a semiconductor parameter analyser (B1500A) and a PNA microwave network analyser (N5227A), respectively. The latter was calibrated from 100 MHz up to 50 GHz with an off-wafer impedance standard substrate (ISS) calibration kit for a 100µm pitch RF-probe 128tilizing a Short-Open-Load-Through (SOLT) calibration procedure at a small signal RF excitation (-20dBm).

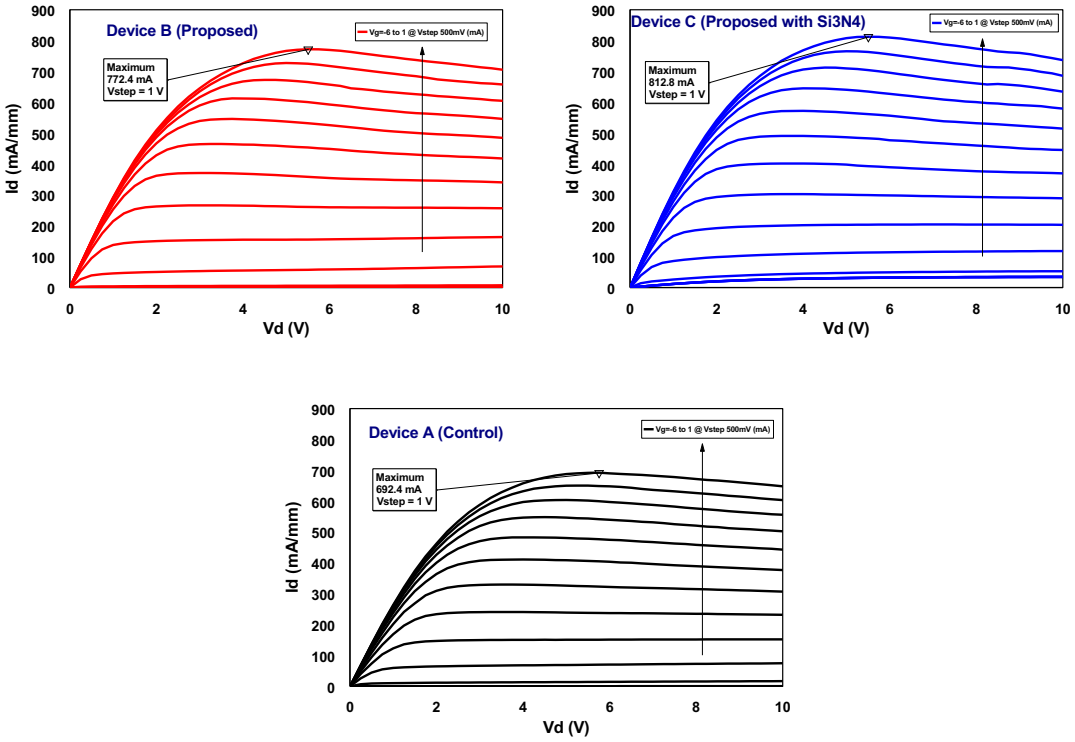


Figure 5.8. I-V family curves of 2-finger 125μm wide device

An assessment of IV characteristics on all three devices was performed to validate the influence of mesa extension on device performance in terms of output current, as shown in **Figure 5.8**. The maximum drain current, I_{DSS}, of three devices is 692, 772 and 813 mA/mm for device A, B and C, respectively. The increase of maximum current in the proposed devices is stemming from the reduction in the On-resistance (R_{ON}) as listed in **Table 5.1**. Further, a well pinch-off behavior is exhibited in all devices at -4V as depicted in **Figure 5.9**. Additionally, At V_{ds} = 4.5V and V_{gs} = -3V, a maximum DC transconductance (G_m) was obtained for the three devices. However, the proposed devices exhibited an increase of G_m, which can be mainly attributed to the expansion of gate width (W_g) due to the mesa extension as predicted from the saturation region DC transconductance formula given in Eq.(2.29).

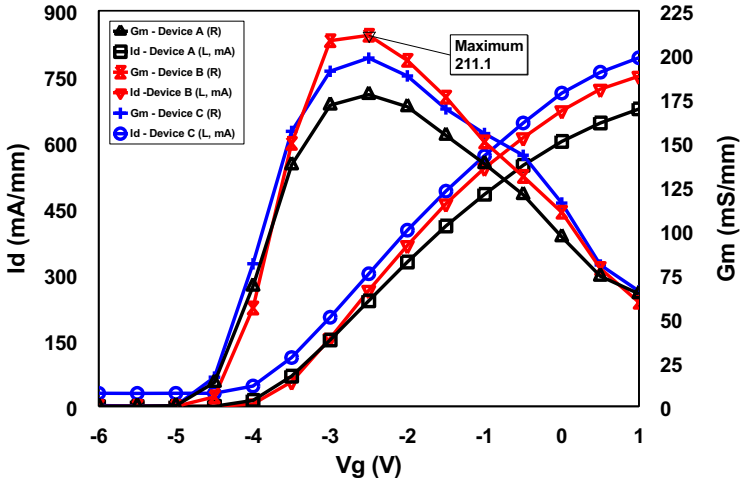


Figure 5.9. The transfer characteristics and the DC transconductance

Figure 5.10 illustrates the power handling of the devices as a function of the applied drain voltages obtained at a unity gate voltage. Moreover, the difference between the power of the studied devices with respect to the control is also shown in **Figure 5.10**, which demonstrates a maximum delta occurring at maximum drain voltages. It is evident that as the distance between the 2DEG channel and the gate is increased, more power can be achieved, mainly due to the reduction of gate leakage within the device. Hence, device *C* exhibited the maximum power density where the gate-feed, which is the lowest resistance portion of the gate, is situated above the mesa followed by the dielectric deposition of Si_3N_4 which resulted in largest distance between the gate-feed and the 2DEG channel. On the other hand, the control device (A) demonstrated the lowest power density caused by the direct contact between the gate and the 2DEG channel which leads to the increase of gate conduction resulting in a relatively lower power handling capabilities in comparison with the corresponding devices.

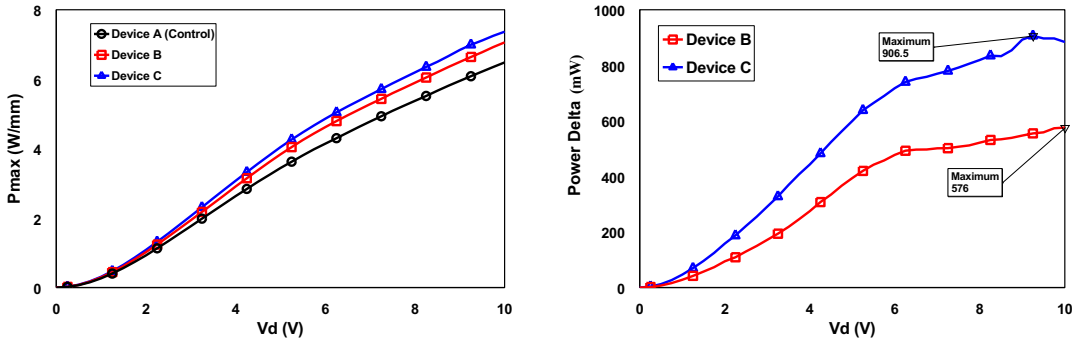


Figure 5.10. Power exhibited by the devices at V_g = 1.0V

Figure 5.11 shows the de-embedded small-signal gain characteristics of 1.0μm 2-finger GaN- based HEMTs on LR-Si. The devices were biased at their best RF performance where the highest current gain (H21) and Maximum Available Gain (MAG)/power gain existed. Since the intersection of both H21 and MAG with frequency, at which H21 (f) = MAG (f) = zero dB, occurs within the measurement frequency range (100 MHz – 50 GHz), extrapolation of H21 and MAG using a -20 dB/decade slope is unnecessary. The results validate that the mesa extension exhibited no compromises to the RF performance of the proposed devices.

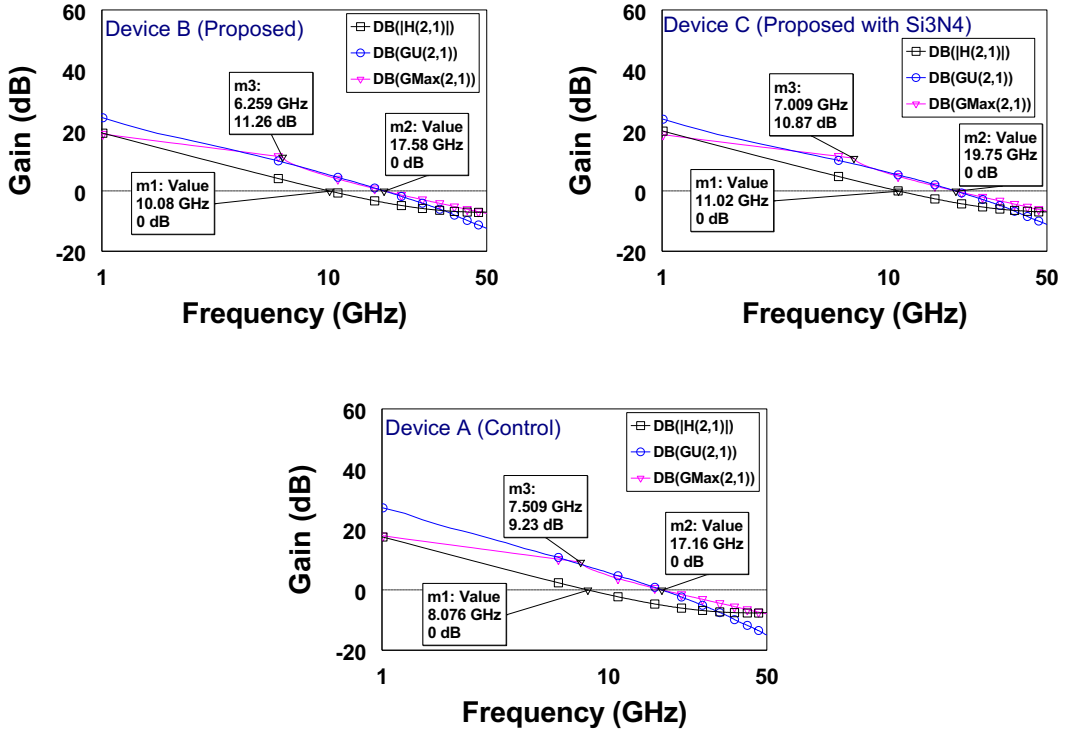


Figure 5.11. GU, H21 and G_{MAX} gains as a function of log frequency in GHz after pads de-embedding

As 132tilizing132 in **Table 5.1**, the results reveal a slight increase in f_T and f_{max} as the gate-feed location is furthest away from the 2DEG channel triggered by the increase of g_m and the reduction in gate-source capacitance for device *B* and *C*, respectively. Generally, device *B* exhibited the 132tilizing performance regarding DC and RF output parameters. Similarly, device *C* also demonstrated an excellent and far superior performance in all characteristics except for the drain leakage occurring below pinch-off.

Table 5.1. Parameters of HEMT with different gate formations

	Parameter	Device (A) (Control)	Device (B) Mesa Planar Gatefeed	Device © Mesa and Si_3N_4 Gatefeed
DC	I_{DSS} (mA/mm)	692	772	813
	Max $P_{density}$ (W/mm)	6.48	7.1	7.4
	V_P (V)	-4.0	-4.0	-4.0
	R_{ON} (Ω·mm)	3.57	3.23	3.05
	G_m (mS/mm)	177	211	198
RF	f_T (GHz)	8.08	10.08	11.02
	f_{max} (GHz)	17.16	17.58	19.75

RF small-signal model for all the three devices under study was developed for the measurements obtained at V_d =4.5 V and V_g = -2.5V with an RF power injection level at -20dBm and the entire 16-elements of extrinsic and intrinsic parameters are included in **Table 5.2**. In general, the developed devices showed similar performance at high frequency with respect to the small signal model parameters except for C_{gs}, g_m, C_{ds} and R_{ds}. The latter, which is the finite output resistance of the device, was reduced in both proposed devices. The observed reduction in R_{ds} was more than 40% and 50% for device B and C, respectively. This can be mostly attributed to the charge exchange with deep levels located at the interface of the device channel and buffer [138]. Due to the mesa extension, the distance between the gate and the states is relatively enhanced. This results into the failure of states to follow the applied voltage, hence the output resistance decreased. This is more evident for device C where the reduction is 10% higher than the decrease obtained by device B.

Table 5.2. HEMT small-signal model parameters biased at V_d =4.5 V and V_g = -2.5V with an RF power injection level at -20dBm

Device	Device (A) (Control)	Device (B) Mesa Planar Gatefeed	Devi©(C) Mesa and Si_3N_4 Gatefeed
f_T (GHz)	8.08	10.08	11.02
f_{max} (GHz)	17.16	17.58	19.75
C_{pg} (fF)	153	291	171
C_{pgd} (fF)	115	93	117
C_{pd} (fF)	190	199	205
L_g (pH)	24	32	15.8
L_d (pH)	30	46	51
L_s (pH)	0.51	0.03	1.4
R_g (Ω)	6.0	8.8	7.4
R_d (Ω)	6.6	3.7	3.5
R_s (Ω)	4.7	8.1	3.8
R_{in} (Ω)	3.5	6.0	10
R_{ds} (Ω)	321	189	158
g_m (mS)	60	108	75
C_{gs} (fF)	985	1,199	890
C_{gd} (fF)	24.8	31.9	30.7
C_{ds} (fF)	34.6	15.1	10.2
τ (ps)	4.9	4.4	4.9

5.3. Summary

In this chapter, a novel structure is proposed to overcome mesa etch concerns such as sidewall profile, common gate discontinuity and gate leakage originated from a gate direct contact with 2DEG. The proposed structure required a miniature extension of the mesa to deposit the gate-feed, thereby ensuring a fully planar gate formation. This, as result, reduced the gate leakage by an order of magnitude. However, since the gate-feed is situated on an active layer with a very low resistance due to a relatively larger length in comparison with the actual gate, the gate became conductive above pinch-off point and gate leakage increased. Consequently, a dielectric is deposited below the gate-feed to counter the arising problem, which led to an increase in the drain leakage at the off-state due to a substantial dielectric thickness. This can be prevented using methods such as atomic layer deposition for a denser yet a shallower (a few nm) dielectric deposition below the gate-feed. Finally, the proposed structure will allow a deeper etch of the active layer for heat management purposes while keeping the integrity of the gate metal intact.

6. GaN HEMT Small Signal Modelling

The small-signal equivalent circuit model values for constructed AlGaN/GaN HEMTs are discussed in this chapter. To estimate comparable circuit components of fabricated AlGaN/GaN HEMTs, it relies on in-depth process information and device geometry. By providing useful input for pr134tilizing134134nsation, an accurate small-signal modelling approach will be critical to the further developmen134tilizing134134nsation of the AlGaN/GaN HEMT technolo'y. It's also required for a reliable circuit design at the system level. Moreover, to offer a comparison data, the small-signal equivalent circuit model values for various AlGaN/GaN HEMTs are also provided. In general, the extraction is divided into two segments with respect to bias dependency, namely extrinsic and intrinsic parameters. The former, which is a bias-independent, is obtained followed by the intrinsic part. The full mathematical manipulation proce134tilizing134arised in the flowchart given in **Figure 6.1**, which were detailed in the forthcoming sections.

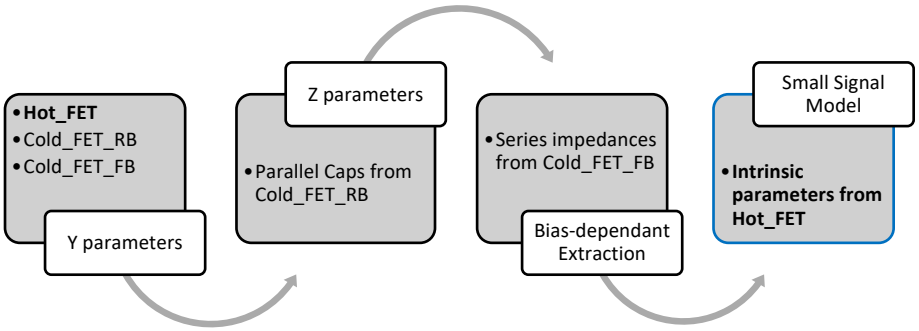


Figure 6.1. Small-signal-model parameters extraction process

6.1. HEMT 16-Element Model

The small signal model 134tilizinilised in this work is illustrated in **Figure 2.20**, which contains 16-elements as explained in Section **(2.8)**. It is the most basic and simplified representation of GaN HEMT operation at high frequency. However, it includes the most effective parameters and parasitic to explain the device RF behavior.

6.2. Extrinsic Parameters Extraction

Extrinsic parameters extraction is comprised of three different parasitic sections: parallel capacitances, series inductances and resistances. Generally, the parallel capacitances are extracted first followed by inductances and concluded by the extraction of the parasitic resistances. In the next few sections, details of the extraction method were presented.

6.2.1. Parallel Capacitances

Parallel capacitances which are the CPW measurement pads introduced parasitic effects. Parasitic capacitances can be estimated using either of the following procedure:

1- Open test fixture, which can be either simulated using EM simulator or integrated within the fabrication process flow.
2- Reverse-bias cold-FET, where the gate terminal of the device is biased well below the pinch-off and the drain is left at zero without an external voltage.

Both methods were employed, and the results were given after that. It should be noted that parallel capacitances are usually represented by a Pi circuit model and hence, the measured S-parameters of the device or the open test fixture have to be converted to Y-parameters for accurate estimation and calculations. Also, capacitances are estimated at the lower side of the frequency spectrum where the reactance are highest according, to capacitive reactance ($X_C = 1/i\omega C$) and vice versa, for the parasitic inductance, where their reactance is lowest at lower frequency ($X_L = i\omega L$).

6.2.1.1. Open Structure

On-wafer RF measurements were performed using a PNA microwave network analyser (N5227A). The network analyse was calibrated from 100 MHz up to 50 GHz with an off-wafer impedance standard substrate (ISS) calibration kit for a 100µm pitch RF-135tilizinglising a Short-Open-Load-Through (SOLT) calibration

procedure at a small signal RF excitation (-20dBm). The following set of equations were used to extract the parasitic capacitances:

$$C_{pgd} = Im\left(\frac{-Y_{12}}{\omega}\right) = Im\left(\frac{-Y_{21}}{\omega}\right)$$
$$C_{pg} = Im\left(\frac{Y_{11}}{\omega}\right) + Im\left(\frac{Y_{12}}{\omega}\right) \quad (6.1)$$
$$C_{pd} = Im\left(\frac{Y_{22}}{\omega}\right) + Im\left(\frac{Y_{12}}{\omega}\right)$$

Figure 6.2 illustrates the extracted parasitic capacitances, its small signal model and the error between the model and the measurements. The results show that the capacitances are nearly constant as a function of frequency with C_{pgd} = 7.5fF, C_{pg} = 82fF and C_{pd} = 198fF. The minimum error percentage is found to be more than 10%, which is rather high, and it is possibly emanating from the unreasonably low series capacitance (C_{pgd}).

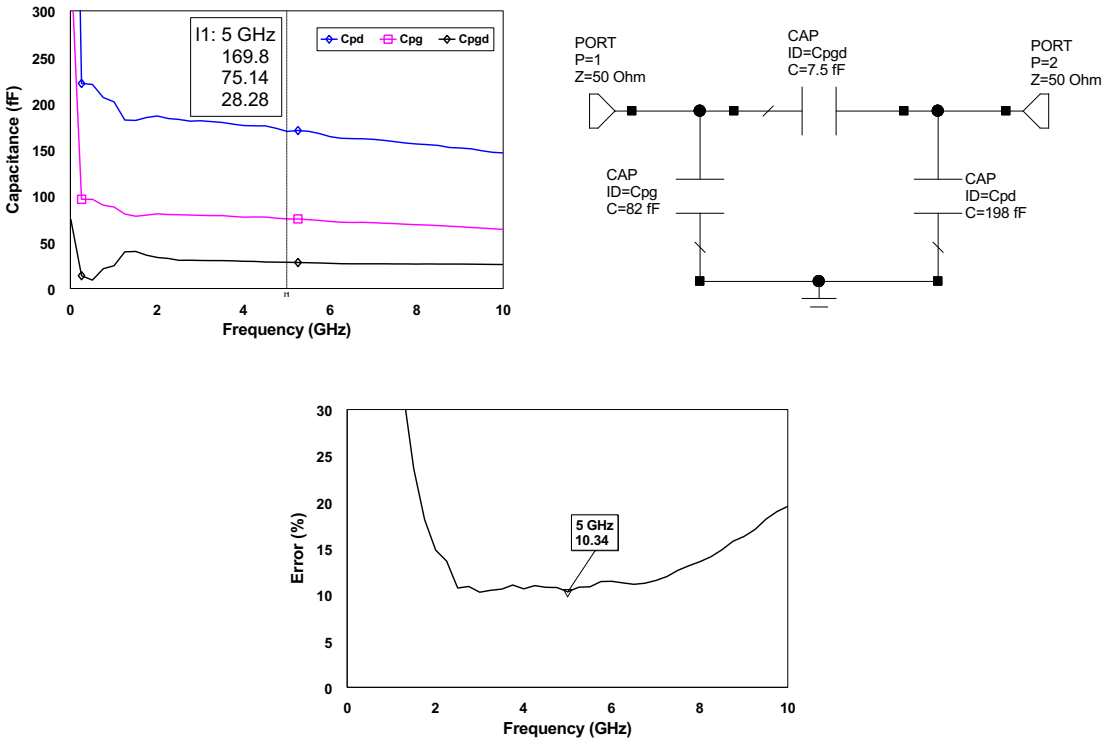


Figure 6.2. Calculated parallel capacitance, small signal model and the error percentage between them

Figure 6.3 further shows the divergence obtained between the model and the measured data. The figure demonstrates the S-parameters for the

measurements and the model plotted on smith chart. As a result of this deviation between the model and the measurement data, it was opted out from any further use within the small signal model extraction.

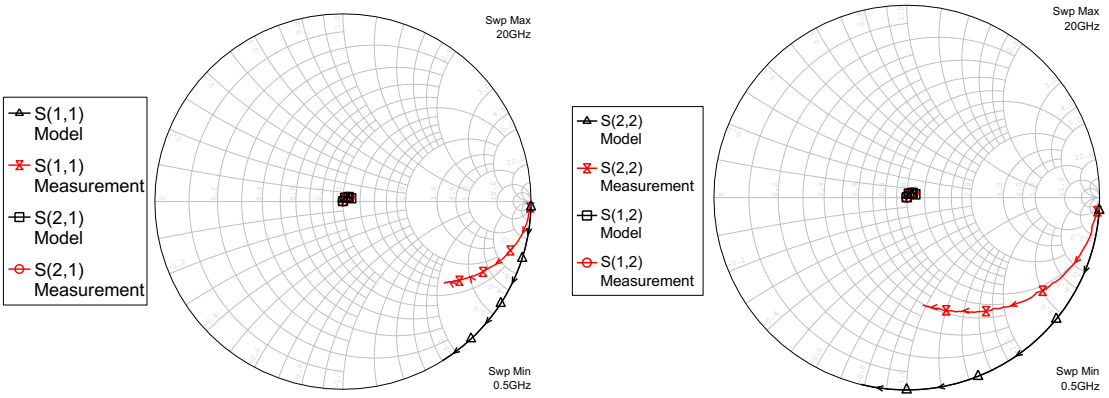


Figure 6.3. Smith chart of the fabricated and model of the open

6.2.1.2. Cold-FET below Pinch-off

By setting the drain and source to zero volts and adding a negative voltage to the gate, the device is reversed biased. The intrinsic device small-signal low frequency behavior may be described as an open circuit when the device is reversed biased. Therefore, the HEMT device is in a reverse biased mode in this scenario. The circuit then becomes a three-terminal system connected by shunt capacitors.

The following is the process for estimating parasitic capacitances:

- To pinch off the gate and drain, apply a suitably negative bias to the device.
- Measure and obtain the S-parameters of the HEMT device.
- Take the S-parameters and convert them to admittance parameters.
- Using the admittance parameters, calculate the parasitic capacitances using Eq.(6.1).

Figure 6.4 demonstrates the extracted parasitic capacitances, its small signal model and the error percentage between the model and the measurements. The results show that the capacitances are nearly constant as a function of frequency with C_{pgd} = 98fF, C_{pg} = 181fF and C_{pd} = 183fF. The error percentage is found to be less than 5% for the entire frequency of interest.

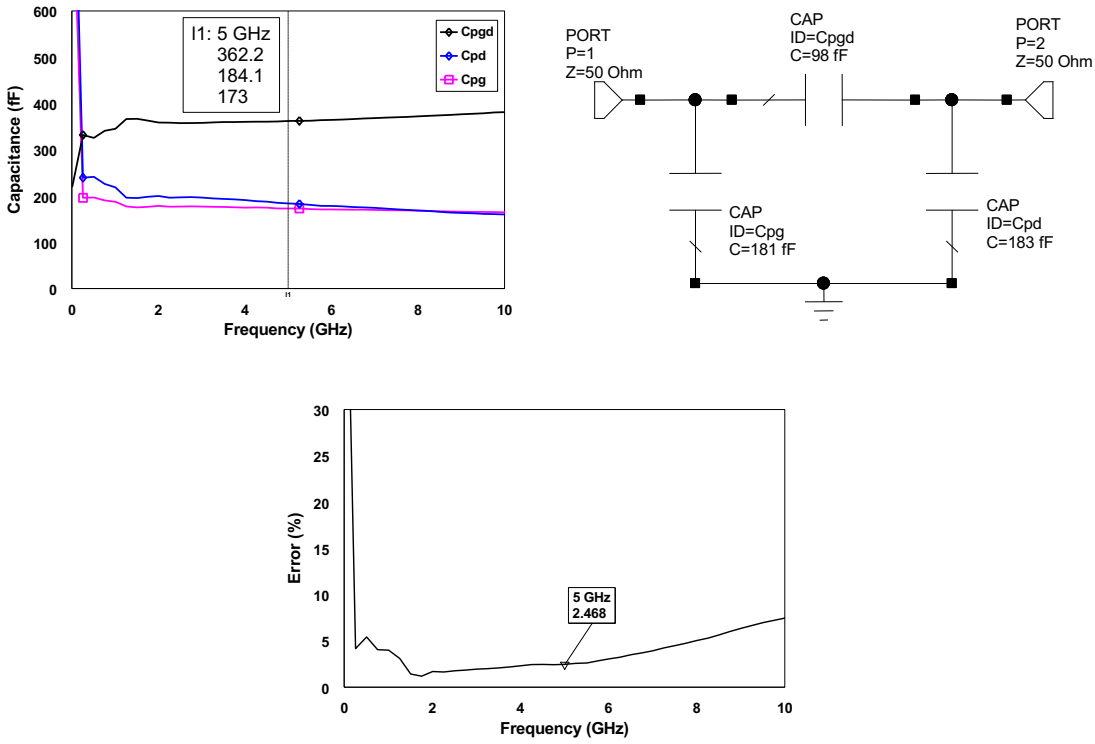


Figure 6.4. Parallel capacitance measured at -8Vg and 0Vd, small signal model and the error percentage between them

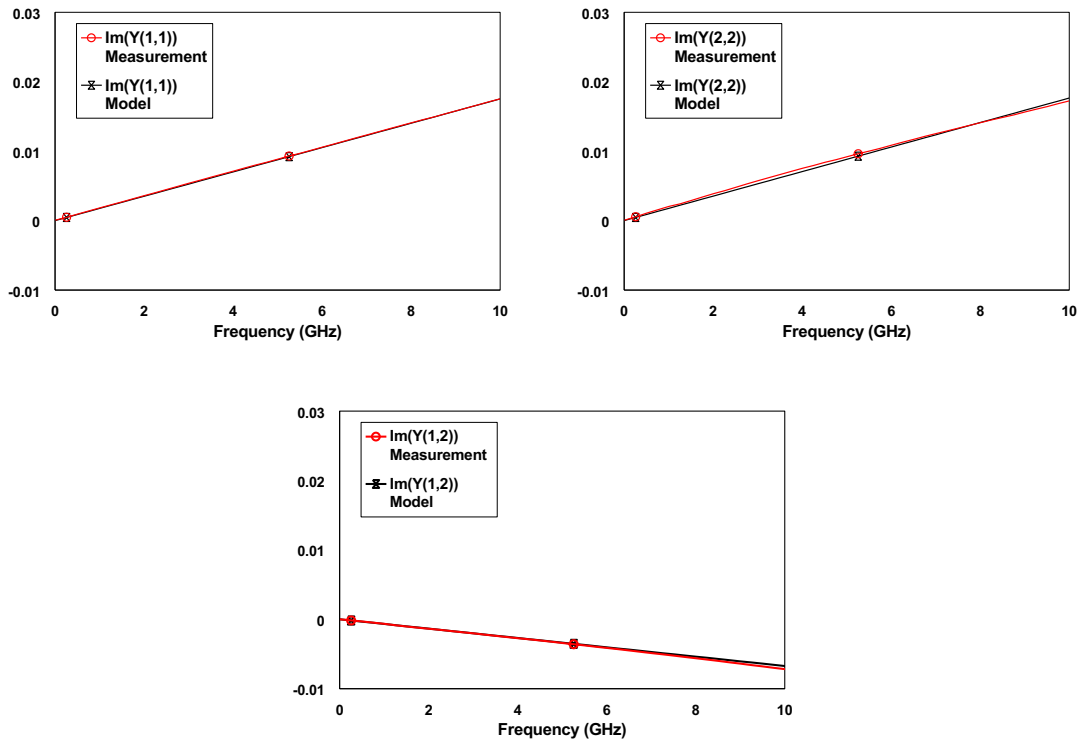


Figure 6.5. Imaginary admittance (in Ω^{-1}) of the HEMT in a reverse-bias and a cold-FET mode

Figure 6.5 shows the imaginary part of the Y-parameters obtained from the measurements and small signal circuit model for the HEMT device while biased in a reverse-bias in a cold-FET mode. It clearly exhibits a capacitive behavior, where parallel admittance is obtained at the input and output and steadily increasing as a function of frequency. Both the measurements and the model data show a good agreement without any discrepancy between them.

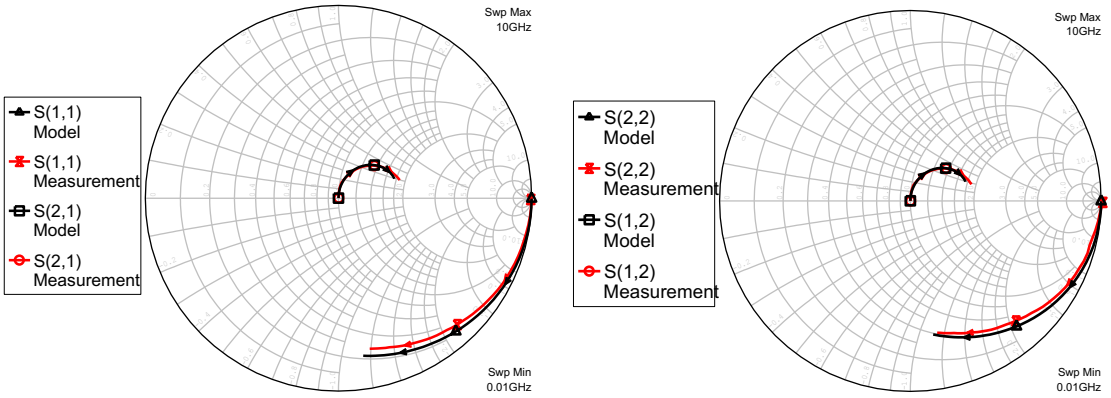


Figure 6.6. Smith chart of the fabricated and model of the HEMT in a reverse-bias and a cold-FET mode

Figure 6.6 and **Figure 6.7** further demonstrate the agreement between the measurement S-parameters and the small signal model, which are plotted in smith chart and rectangular magnitude/phase format. As a result of the agreement between the measurement S-parameters and the small signal model, the use of these extracted capacitances, in the next step of the extraction procedure of the series inductance and resistances, is clearly justified.

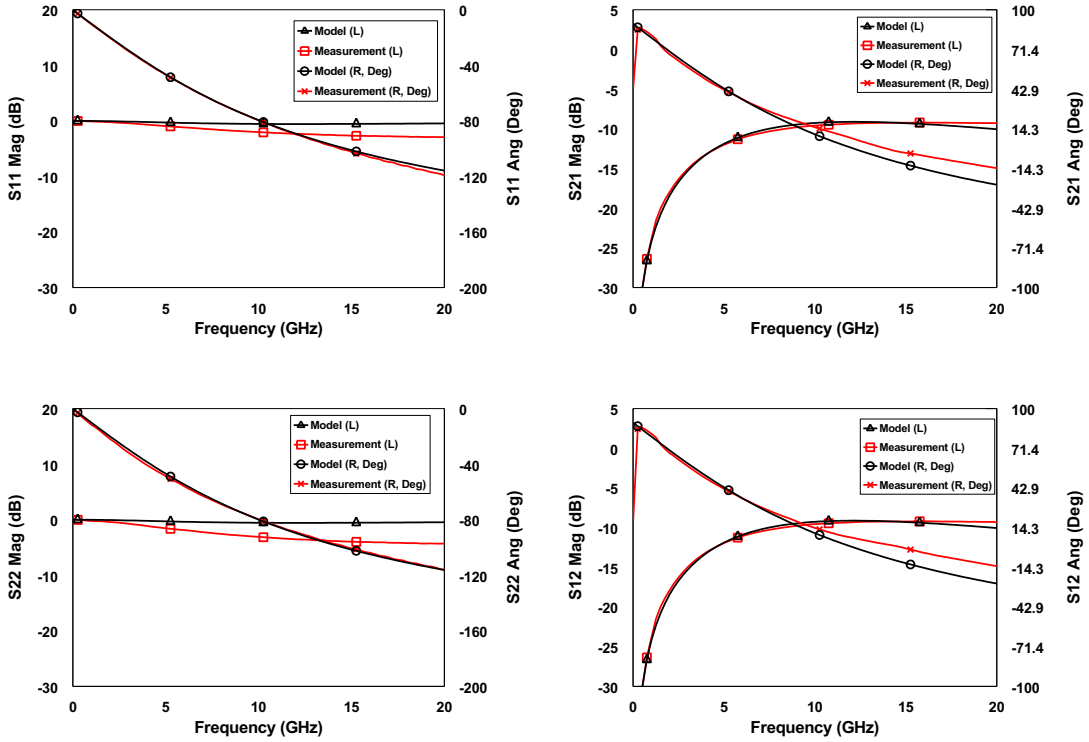


Figure 6.7. S-parameters of the fabricated and model of the HEMT in a reverse-bias and a cold-FET mode

6.2.2. Series Inductances and Resistances

Series inductances and resistance, which are the CPW measurement pads introduced parasitic effects. Parasitic inductances and resistance can be estimated using either of the following procedure:

1- Short test fixture, which can be either simulated using EM simulator or integrated within the fabrication process flow.

2- Forward-bias cold-FET, where the gate terminal of the device is biased well above the pinch-off and the drain is left at zero without an external voltage.

It should be noted that series inductances and resistance are usually represented by a T-circuit model and hence, the measured S-parameters of the device or the short test fixture have to be converted to impedance Z-parameters for accurate estimation and calculations after converting to Y-parameters and subtracting the parallel capacitances obtained earlier. Also, inductances are estimated at the higher side of the frequency spectrum where the reactance are highest according to inductive reactance ($X_L = i\omega L$) and vice versa for the parasitic capacitances,

where their reactance is lowest at higher frequency ($X_C = 1/i\omega C$). In this work, the short fixture is the only method used to calculate the parasitic inductances since the other method produces a nonlinear inductance as a function of frequency.

6.2.2.1. Short Structure

On-wafer RF measurements were performed using a PNA microwave network analyser (N5227A). The network analysis was calibrated from 100 MHz up to 50 GHz with an off-wafer impedance standard substrate (ISS) calibration kit for a 100µm pitch RF-probe utilising a Short-Open-Load-Through (SOLT) calibration procedure at a small signal RF excitation (-20dBm). The following set of equations were used to extract the parasitic inductances:

$$\begin{aligned} L_S &= \frac{Im(Z_{12})}{\omega} = \frac{Im(Z_{21})}{\omega} \\ L_g &= \frac{Im(Z_{11})}{\omega} - L_S \\ L_d &= \frac{Im(Z_{22})}{\omega} - L_S \end{aligned} \tag{6.2}$$

Figure 6.8 illustrates the extracted parasitic inductances. The results show that the inductances are approximately constant as a function of frequency with L_s = 5.4pH, L_g = 31.3pH and L_d = 25.7pH.

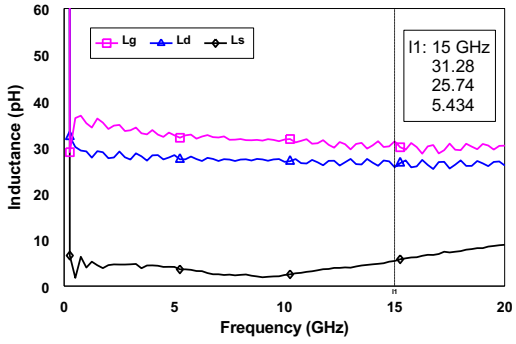


Figure 6.8. Series inductances from short circuit structure

Figure 6.9 shows the imaginary part of the Z-parameters obtained from the measurements and small signal circuit model for the HEMT device while biased in a forward-bias in a cold-FET mode. It clearly exhibits an inductive behavior,

where series impedance is obtained at the input and output and steadily increasing as a function of frequency. Both the measurements and the model data show a good agreement without any discrepancy between them.

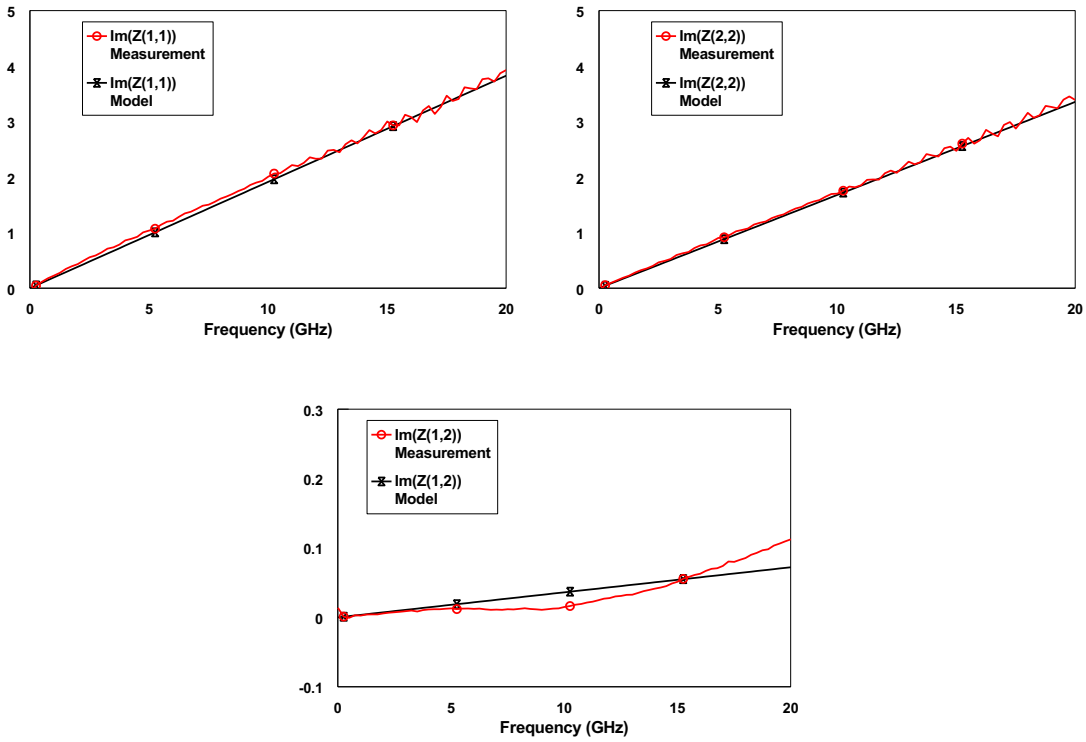


Figure 6.9. Imaginary impedance (in Ω) of the short test fixture

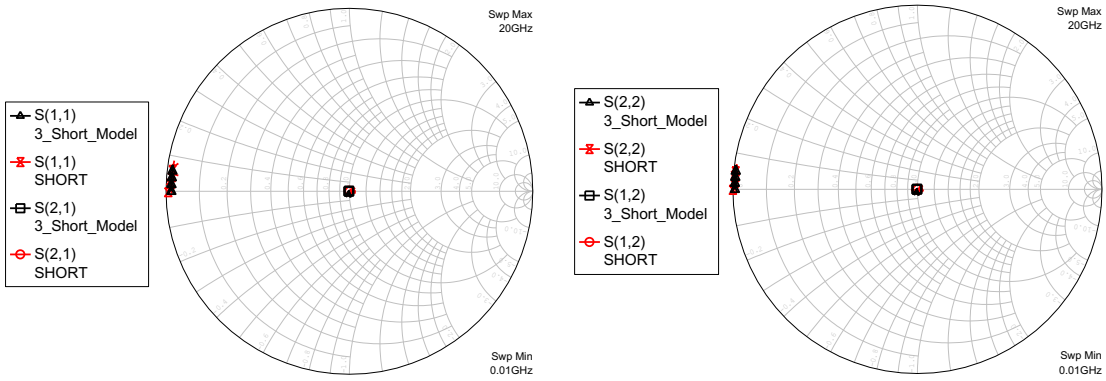


Figure 6.10. Smith chart S-parameters of the short test fixture

Figure 6.10 further demonstrates the agreement between the measurement S-parameters and the small signal model, which are plotted on a smith chart. As a result of the agreement between the measurement S-parameters and the small

signal model, the use of these extracted inductances, in the next step of the extraction procedure of the series resistances, is similarly justified.

6.2.2.2. Cold-FET above Pinch-off

The processes for extracting the series resistive parasitic component values from a forward-biased device are like those for a reversed-biased device, but they are more involved and contain a few added considerations. When the intrinsic device is forward biased, it behaves as a short circuit.

The following is the process for estimating parasitic resistances:

- Apply a positive voltage to the gate to send enough current through the device to turn the diode "on," but not enough to destroy the device.
- Measure and acquire the S-parameters of the device.
- Subtract the shunt capacitances and series inductances using the de-embedding technique as depicted in **Figure 6.11**.
- Calculate the series resistances using the following set of equations:

$$\begin{aligned} R_S &= Re(Z_{12}) = Re(Z_{21}) \\ R_g &= Re(Z_{11}) - R_S \\ R_d &= Re(Z_{22}) - R_S \end{aligned} \tag{6.3}$$

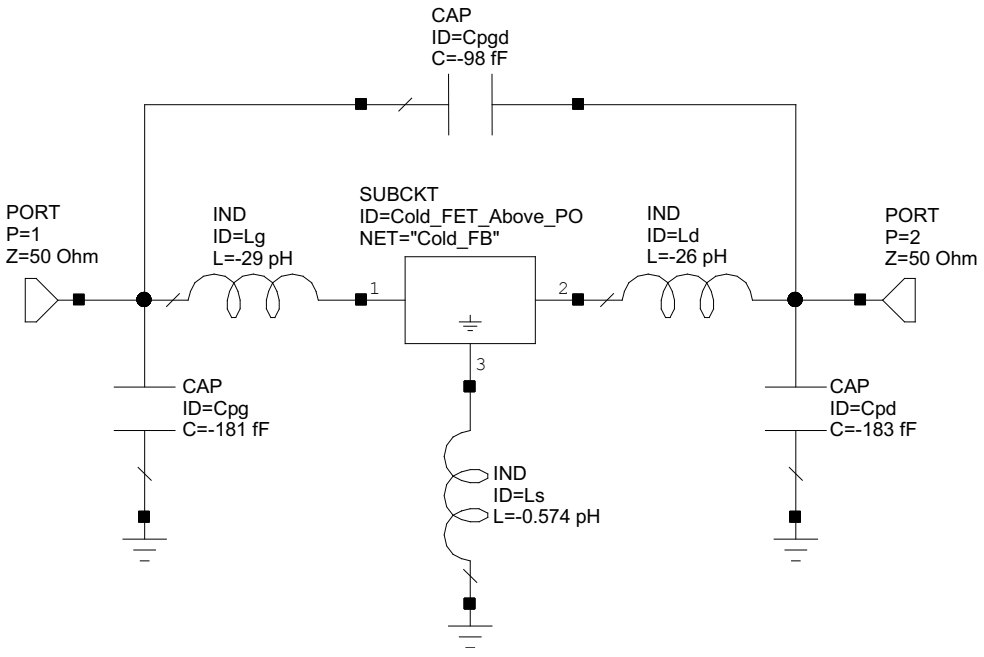


Figure 6.11. De-embedding the extrinsic reactive impedances

Figure 6.12 illustrates the extracted parasitic resistances. The results show that the series resistances are approximately constant as a function of frequency with R_s = 4.3Ω, R_g = 3.7Ω and R_d = 6.1Ω.

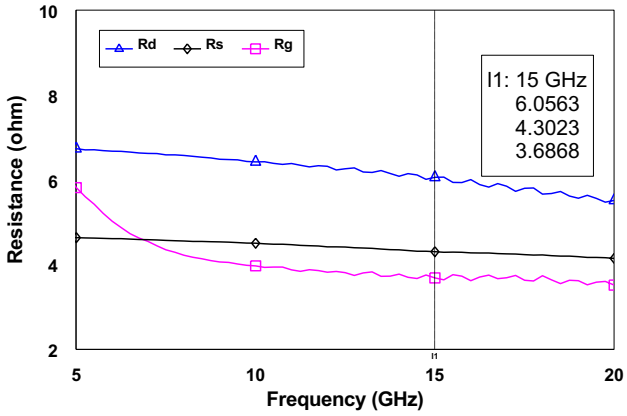


Figure 6.12. Series resistances from cold-FET in a forward-bias

6.3. Intrinsic Parameters Extraction (Hot-FET)

The process for extracting the intrinsic element values is conducted by applying a variable bias point on the drain terminal with respect to the source, which is fixed at zero volts, i.e., the device in a hot-FET mode since current flows from drain to source. After that, on-wafer RF measurements were performed using a PNA microwave network analyser (N5227A). The network analysis was calibrated from 100 MHz up to 50 GHz with an off-wafer impedance standard substrate (ISS) calibration kit for a 100μm pitch RF-probe utilising a Short-Open-Load-Through (SOLT) calibration procedure at a small signal RF excitation (-20dBm).

The following is the process for estimating the intrinsic element values:

- Apply a positive voltage to the drain from zero to 10V with an incremental increase.
- Apply a negative voltage at the gate where the maximum DC transconductance occurs and some other points nearby for validation.
- Measure and acquire the S-parameters of the device.
- Subtract the shunt capacitances and series inductances and resistances using the de-embedding technique as illustrated in **Figure 6.13**.

- Calculate the intrinsic 7-element values using the following set of equations:

$$C_{gd} = \frac{-Im(Y_{12})}{\omega} = \frac{-Im(Y_{21})}{\omega}$$

$$C_{gs} = \frac{Im(Y_{11}) - \omega C_{gd}}{\omega}\left[1 + \frac{(Re(Y_{11}))^2}{(Im(Y_{11}) - \omega C_{gd})^2}\right]$$

$$C_{ds} = \frac{Im(Y_{22}) - \omega C_{gd}}{\omega}$$

$$R_{in} = \frac{Re(Y_{11})}{(Im(Y_{11}) - \omega C_{gd})^2 + (Re(Y_{11}))^2} \tag{6.4}$$

$$g_m = \sqrt{(Re(Y_{21}))^2 + \left[(Im(Y_{21}) + \omega C_{gd})^2\right] \cdot \left[1 + (\omega C_{gs} R_{in})^2\right]}$$

$$\tau = \frac{1}{\omega}\sin^{-1}\left[\frac{-(g_m C_{gd} + Im(Y_{21}) + \omega C_{gs} R_{in} Re(Y_{21}))}{g_m}\right]$$

$$R_{ds} = \frac{1}{Re(Y_{22})}$$

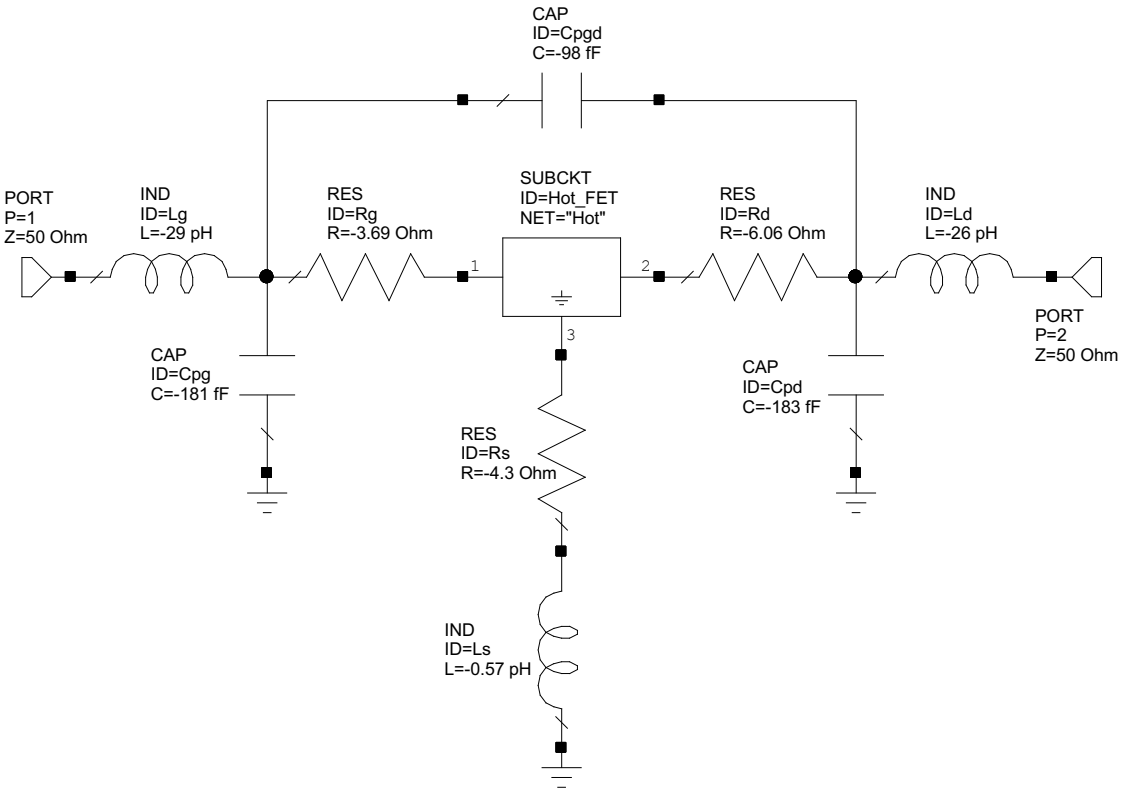


Figure 6.13. De-embedding the extrinsic components

Figure 6.14 illustrates the intrinsic capacitances as a function of frequency that model the three different electric-coupling occurring between the three terminals of the HEMT device i.e., gate, source and drain. Each element has been defined earlier. C_{gs} and C_{gd} are the capacitance between the gate on one side and the source and drain on the other. Both capacitive elements are inversely proportional to the cutoff frequency and the maximum oscillation frequency. Higher capacitance means longer times and more energy required for charging and discharging the gate which translates to lower operational frequency and vice versa. Both quantities are exhibiting a constant behavior as a function of frequency, whereas C_{ds}, capacitance between drain and source, shows a non-linear behavior as a function of the operational frequency.

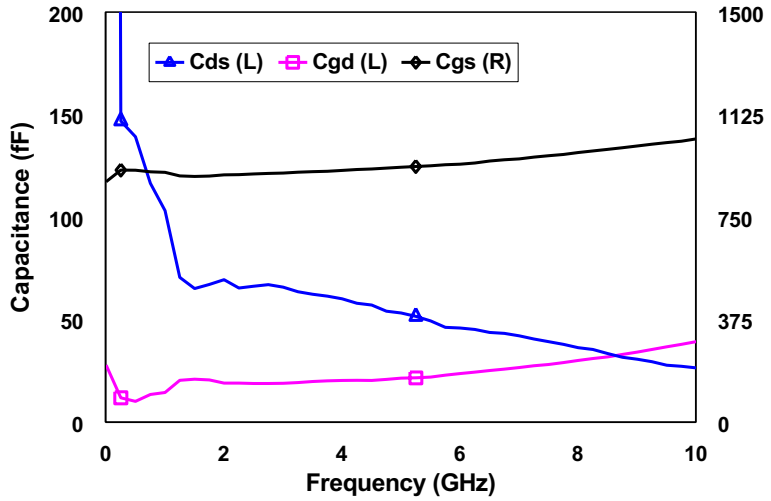


Figure 6.14. Intrinsic parallel capacitances between the device three terminals at obtained at V_d =4.5 V and V_g = -2.5V

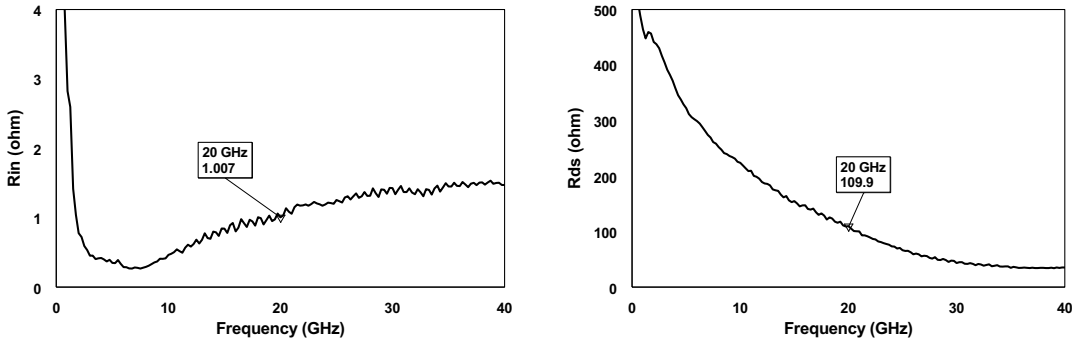


Figure 6.15. Input and output resistances

Figure 6.15 shows the device intrinsic input resistance (R_{in}) and the output resistance (R_{ds}). The former is inversely proportional to the oscillation maximum frequency and vice versa for the R_{ds}.

The device small signal model RF transconductance is depicted in **Figure 6.16**. This determines the current modulation and the gate control over the drain current. As shown in **Figure 6.16**, the RF transconductance obtained for the small signal model exhibits a clear DC to RF dispersion which is manifested in the larger value of the DC transconductance in comparison to the one obtained for small signal RF. There are several factors that can cause the issue of DC to RF dispersion, such as the surface state trapping, distance between the gate and the 2DEG channel. More discussion was given when comparing the various devices side-by-side at the end of this chapter to identify where this phenomenon is originating from.

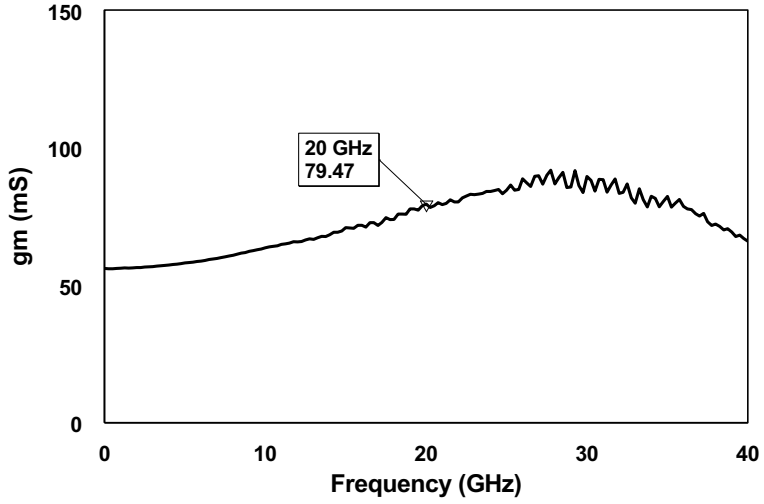


Figure 6.16. RF transconductance of 2-finger HEMT DW = 32μm and Wg = 125μm

The complete small signal model, following an optimisation process to lower the error margin between the model and the measurements with respect to S-parameters, is demonstrated in **Figure 6.17**. The given measurements are for a 2-finger HEMT DW = 32μm and Wg = 125μm obtained at drain and gate bias of V_d =4.5 V and V_g = -2.5V, respectively.

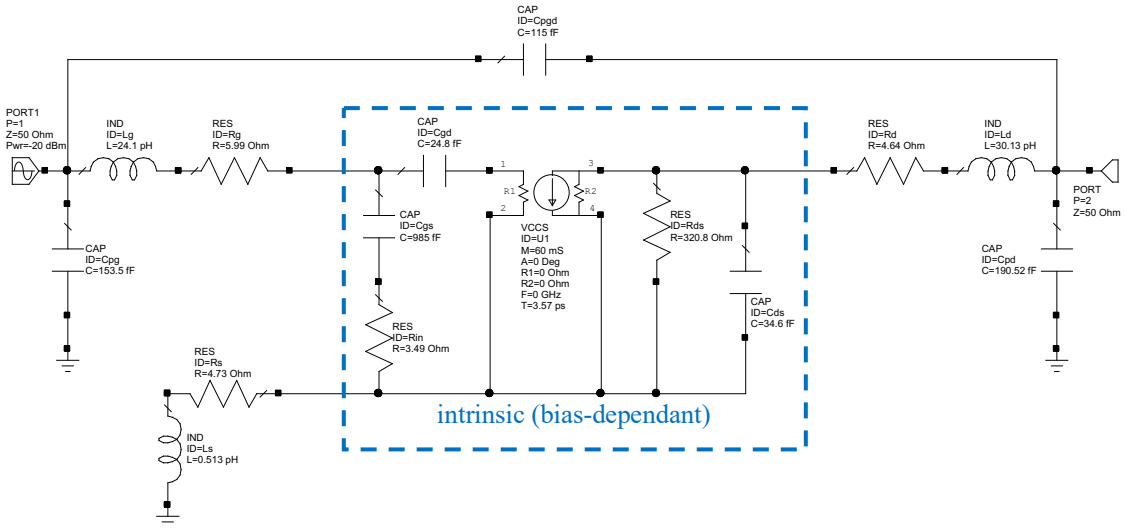


Figure 6.17. Fabricated 2-finger HEMT small signal model obtained at V_d =4.5 V and V_g = -2.5V post-optimisation

Figure 6.18 demonstrates the forward and backward transmission and reflection coefficients of the fabricated GaN HEMT device along with the small signal model for comparison in a rectangular format. The data shows both the magnitude and the phase of a 2-finger HEMT biased at V_d =4.5 V and V_g = -2.5V with a small signal RF excitation (-20dBm) and the small signal model results are shown post-optimisation process for minimum error between the measurement and model S-parameters. The graph shows an excellent agreement between the fabricated RF 2-finger HEMT device and the developed small signal model. The parameter S_{21}, which is related to the gain presented by the fabricated device, is exhibiting a maximum gain at low frequency of more than 13dB without any matching networks presented at its two terminals.

Figure 6.19, on the other hand, exhibits the same data on a smith chart in a phasor format. Similarly, the agreement between the fabricated device and the developed small signal model is clearly displayed. It should be noted that juxtaposition of **Figure 6.18** and **Figure 6.19** is for the control device which was utilised as a reference throughout this project, where the device and drain width set at 125μm and 32μm, respectively, and the gate-feed of the device is situated on the mesa floor with a sidewall 2DEG direct contact.

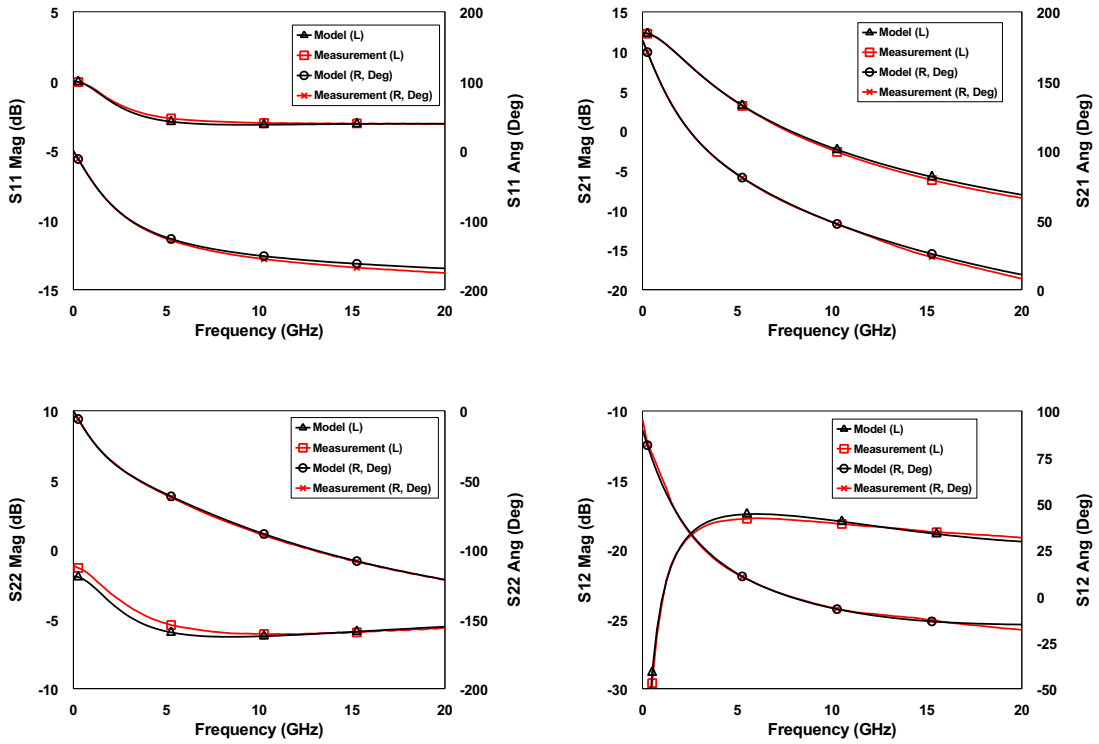


Figure 6.18. S-parameters of a HEMT small signal model vs measurement in magnitude and phase

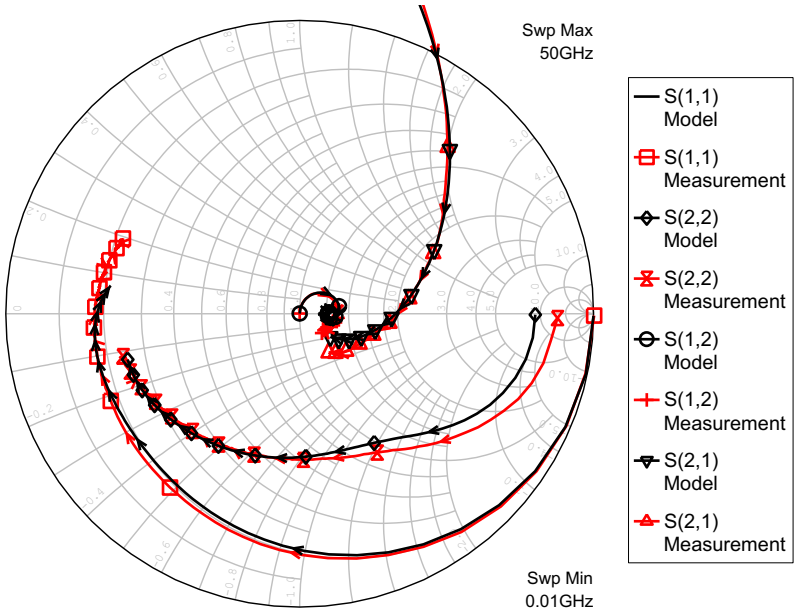


Figure 6.19. HEMT small signal model vs measurement S-parameters

The error percentage between the model and the fabricated RF GaN HEMT device measurement is shown in **Figure 6.20**, which is based on the S-

parameters difference between them divided by the measured data which can be calculated using the following expression:

$$Error\ (\%) = 100 \times \frac{S_{\text{Measured}} - \left(S_{\text{Modelled/Simulated}}\right)}{S_{\text{Measured}}} \tag{6.5}$$

A good agreement is obtained where the error remains lower than 5% across the entire frequency band and up to the maximum oscillation frequency with a minimum error, which is less than 2%, occurring at 7.5GHz in a proximity to the cutoff frequency where the current gain falls to unity.

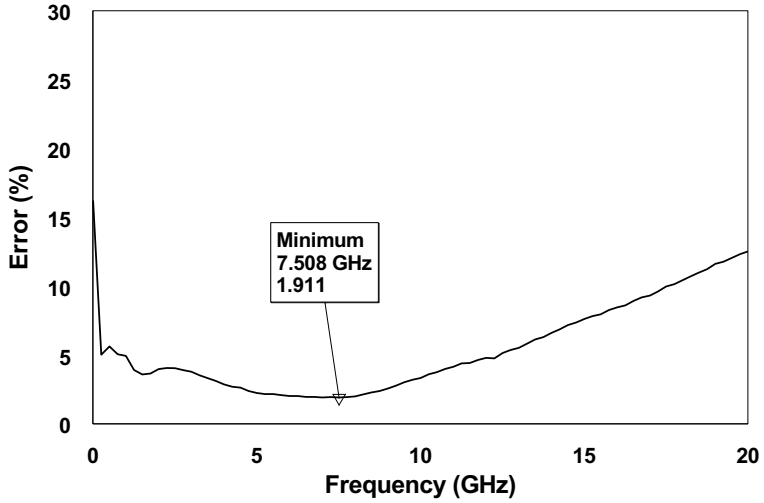


Figure 6.20. Error percentage between the model and measurement data

In addition to the high frequency extracted parameters i.e., f_T and f_{max}, **Table 6.1** summarises the small-signal-model parameters of various GaN HEMT devices with two T-shaped gates and a 1μm of L_g. The control device, which is considered as a reference and a benchmark with its dimensions being the nominal values utilised for comparison with the other fabricated devices. After small-signal-model development, a few issues arose to the surface as follows:

- The first and most concerning issue is the presence of a DC-to-RF dispersion for all the fabricated devices, to different extents, despite the measurements taken to ensure the elimination of this phenomenon such as the deposition of

a Si_3N_4 dialectic as a passivation layer to suppress the occurrence of trap states at the surface level beside the GaN cap layer already existing in the epi-layer to further resolve the problem. It was found that the device with a planar gate exhibited the lowest DC-to-RF dispersion, i.e., highest RF transconductance, as shown in **Table 6.1**. This can be explained by the uniformity of the metallic deposition of the gate electrode thereby eliminating any sharp edges or corners which improves the electric fields distribution and suppress any undesired spikes in the fields. However, this structure produces higher capacitance between the gate and the source because of the existence of an active area below the gate-feed with a slightly larger area relative to the gate length.

Table 6.1. HEMT small-signal model parameters biased at V_d =4.5 V and V_g = -2.5V with an RF power injection level at -20dBm

Device	Mesa Planar Gatefeed	Mesa and Si_3N_4 Gatefeed	Control Device	DW = 52µm	W_g = 250µm
f_T (GHz)	11.02	10.08	8.08	8.4	9.76
f_{max} (GHz)	19.75	17.58	17.16	14.92	13.58
C_{pg} (fF)	291	171	153	264	199
C_{pgd} (fF)	93	117	115	105	111
C_{pd} (fF)	199	205	190	261	164
L_g (pH)	32	15.8	24	26	34
L_d (pH)	46	51	30	46	30
L_s (pH)	0.03	1.4	0.51	5.7	0.01
R_g (Ω)	8.8	7.4	6.0	6.4	9.2
R_d (Ω)	3.7	3.5	6.6	8.1	3.9
R_s (Ω)	8.1	3.8	4.7	6.5	4.1
R_{in} (Ω)	6.0	10	3.5	4.8	1.42
R_{ds} (Ω)	189	158	321	246	177
g_m (mS)	108	75	60	79	81
C_{gs} (fF)	1,199	890	985	1,105	949
C_{gd} (fF)	31.9	30.7	24.8	22.6	34.9
C_{ds} (fF)	15.1	10.2	34.6	18.3	10.1
τ (ps)	4.4	4.9	4.9	4.5	1.2

- Secondly, f_T and f_{max} show a positive increase with respect to the gate being in a non-direct contact with the 2DEG channel. This is evident in the two devices with the innovative gate structures, which leads to both devices

having the highest f_{max} of the other devices where the gate is directly connected by the sidewall to the 2DEG.

- Thirdly, the increase of the device gate width demonstrated a better device stability, which is influenced by the gate series parasitic, namely inductance and resistance, and the higher current gain cutoff frequency. This is manifested by the increase of the gate width from 125 to 250μm, which resulted in the improvement of f_T from 8.08 to 9.76GHz. However, the maximum oscillation frequency is degraded by more than 20%, where f_{max} falls from 17.16 for a 125μm wide device to 13.58GHz for the 250μm one. This can be attributed to the increase of the gate series parasitic, aka, the gate inductance and resistance, both of which demonstrates a directly proportional increase as the device width is enhanced.
- Finally, it is unclear why the different device structures have exhibited different pads capacitances. However, since the capacitance values that were obtained are in femtofarad, any small variation in the fabrication or the measurement setup may have been magnified at the small-signal-modelling process and optimization phase.

6.4. Summary

In this chapter, a small-signal-model was developed to evaluate the behavior of the GaN HEMT devices with respect to high frequency operation and the parasitic associated with it. The process began with the extraction of the extrinsic elements using various methods followed by the extraction of the intrinsic parameters. It was found that the parallel capacitances are estimated accurately using the cold-FET with a reverse bias rather than using an open structure. Furthermore, the series inductances were extracted using the short structure, which gave the most accurate data and a minimum error. Subsequently, the series resistances were estimated using the cold-FET in a forward bias causing the current to flow within the device to initiate a voltage drop across the resistances. Finally, the intrinsic elements were calculated after de-embedding the extrinsic parameters. A good agreement was obtained for the developed model specifically within the desired range of frequency spectrum.

7. NOVEL GAN SCHOTTKY BARRIER DIODES

Diode based MMICs are used widely to perform tasks such as mixing of two signals of different frequencies. Mixing of two signals could also be performed by FET circuits, but diodes are often preferred to FETs for the following reasons:

- The RF performance (bandwidth) of diode circuits is superior to that of FET circuits due to lower RC product.
- Less demand for fabrication control and smaller plan area than for a FET, thus giving better yield and cost advantage.
- In some circuits, no external DC bias is required and therefore, fewer on-chip components are needed which results in less fabrication steps and smaller chip size.

The purpose of the work on Schottky contact diodes for frequency conversion application presented in this chapter are:

1) To identify process conditions
2) To evaluate diode quality
3) To identify suitable diode geometry
4) To reduce the diode barrier height for better performance
5) To extract equivalent circuits for diodes

This chapter begins with a brief outline of basic Schottky-contact diode operation. A series resistance analysis of the diode studied in this project is discussed. The small signal equivalent circuit of the Schottky -contact diode is presented. The layout of the diodes studied is described, and their fabrication techniques are briefly mentioned. DC, RF, and low frequency *C-V* measurement techniques and measurements to characterise the diodes are outlined. Finally, results and discussions on the effects of recess under the Schottky-contact (anode) obtained from the *I-V* diode characteristics and *C-V* measurements, and the small signal equivalent circuit deduced from RF measurements for different diode configurations are presented.

7.1. SBD Theory

GaN-based Schottky barrier diode (SBD) is commonly constructed in three different structures, vertical, quasi-vertical and lateral as illustrated in **Figure 7.1**. The latter has both contacts, namely cathode and anode, on the same surface level [152]. Although lateral SBDs are easier to fabricate and test, they suffer from larger barrier height in comparison with vertical ones [153]. However, lateral diodes tend to have a smaller on-resistance and turn-on voltage since current only flows in the drift region and no substrate loading effects are observed in comparison to vertical diodes. Beside the low on-resistance, lateral SBDs also have smaller junction capacitance which allow them to be an excellent candidate for high frequency applications.

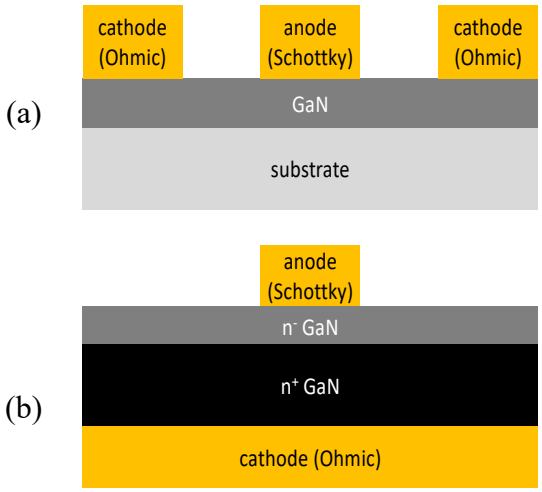


Figure 7.1. Lateral (a) and vertical (b) structures GaN-based SBDs

In this project, the ohmic and Schottky contacts are fabricated laterally on the same surface using the wafer demonstrated in **Figure 7.2** to form the AlGaN/GaN heterostructure Schottky diode. The wafer consists of GaN epi-layers placed on a foreign substrate such as Si, sapphire or SiC. The diode fabrication process starts by forming the isolation, either by mesa or ion implantation using Argon, to remove or damage the active layers between devices in order to self-isolate them for accurate measurements purposes. After that, the ohmic metallic stack-up is deposited and annealed to diffuse the metal into the semiconductor to eliminate the barrier between them and to lower the contact resistance. Next, a passivation

layer (SiN) is deposited then selectively etched for anode and bond-pads metal deposition. Finally, a second passivation layer is deposited and selectively etched to expose the measurement pads.

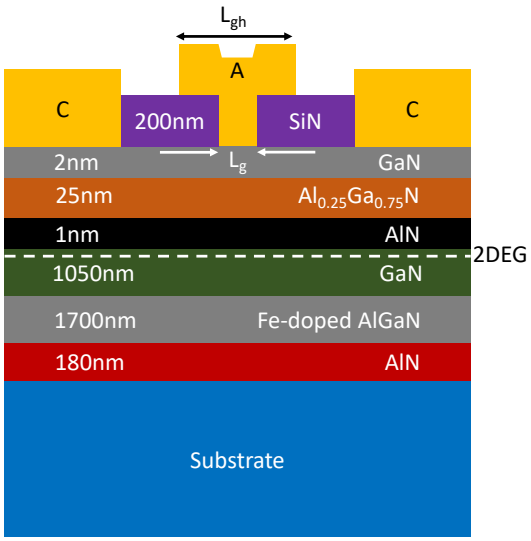


Figure 7.2. Cross-section view of the fabricated SBDs and the GaN epilayers

Unlike p-n junction diode, where the current transport is conveyed through the minority carriers, Schottky diode is a majority-carrier device, which as a result offers a faster switching capability and do not suffer from charge storage delay resulting in a lower transition time with an instantaneous voltage change across its terminals [154], [155]. Schottky diode is based on a metal-semiconductor contact that forms its anode and ohmic, respectively. The latter (ohmic contacts), such as gallium arsenide, Silicon, or gallium nitride, emits a linear current-voltage (*I-V*) relation, where the current is a non-rectified one with a constant conductance value. Schottky (metal such as aluminum, titanium, copper, or gold) on the other hand, is a rectifying-contact formed when the metal (anode) is placed on a semiconductor (cathode) with different work function, which as a result, creates a barrier height between them producing a nonlinear *I-V* curve. Ideally, Schottky barrier should pass current only under forward bias conditions and block the current flow otherwise (reversed bias). Generally, due to higher mobility, Schottky diode utilises an n-type semiconductor (electrons majority-carriers) rather than p-type (holes majority-carriers), which results in higher cutoff frequency and lower series resistance. **Figure 7.3** illustrates the characteristic

energy band diagram of a Schottky diode formed between a metal and semiconductor before and after the point of contact, where Φ_m and Φ_s are the energy differences (known as the work function) between the free-space level and fermi levels of the metal and the semiconductor, respectively. When a Schottky contact is generated between the metal and semiconductor, carriers will begin to flow from semiconductor to the metal to reach a thermodynamic equilibrium condition at which both fermi levels are coincident, and a barrier height is situated between the metal and the semiconductor. This resultant junction potential is called the built-in potential across the diode junction, and it is expressed as:

$$V_{bi} = |\Phi_m - \Phi_s| \tag{7.1}$$

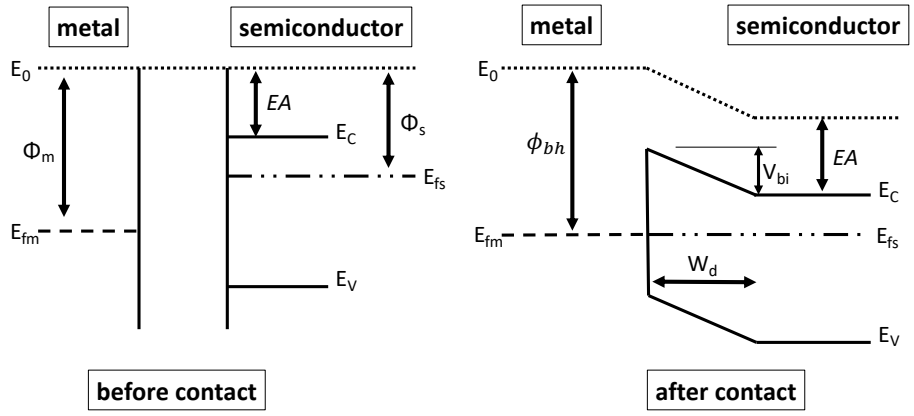


Figure 7.3. Energy band diagram of a Schottky barrier before and after contact

The formed depletion region between the metal and the semiconductor is positively charged neutralising the negatively charged metal and it imitates the behavior of a capacitor's dielectric. Assuming that electrons are completely ionised, n_s, which is the sheet density in the active channel, can be considered as the electron concentration and the width of the depletion region is obtained using Eq. (7.2).

$$W_d = \left[\frac{2\varepsilon_s(V_{bi} - V_a)}{qn_s}\right]^{1/2} \tag{7.2}$$

where ε_s = $\varepsilon_0\varepsilon_r$ GaN dielectric permittivity (GaN ≈ 7.88e-11 F/m)

V_{bi} = junction built-in potential

V_a = applied voltage

n_s = sheet density

q = charge of electron (≈ 1.6e-19 $Coulombs$)

The charge per unit area ($Coulombs.cm^{-2}$) is given by:

$$Q_d = qN_dW_d = [2\varepsilon_s(V_{bi} - V_a)]^{1/2} \tag{7.3}$$

By taking the derivative of charge with respect of the junction voltage, the capacitance of the depletion layer per unit area ($F.cm^{-2}$) can be obtained as shown:

$$C(V) = \frac{\partial Q_d}{\partial V} = \left[\frac{\varepsilon_s q n_s}{2(V_{bi} - V_a)}\right]^{\frac{1}{2}} = \frac{\varepsilon_s}{W_d} \tag{7.4}$$

Knowing the junction capacitance at zero bias (C_{j0}) and the barrier height (ϕ_{bh}), from measurements, Eq. (7.4) can become:

$$C(V) = \frac{C_{j0}}{\left[1 - \frac{V_a}{V_{bi}}\right]^m} = S^{-1} \tag{7.5}$$

where m = a grading coefficient used as a reflect of the abruptness of the diode junction [156] and its value is usually 0.5 < m < 1, depending on the type of device [157].

In general, Schottky diode, under biasing, operates in two modes forward and reverse depending on the applied voltage and its current is calculated using Eq. (7.6). The applied voltage is utilised to alter the potential barrier magnitude with regard to the desired applications. If a forward operation is required, the potential barrier (V_{bi}) is decreased and vice versa for a reverse-operational mode as depicted in **Figure 7.4**. On the other hand, at zero-bias, the majority carriers in

Schottky diode require thermal activation to overcome the barrier that resulted from the unequal work function between the metal and semiconductor materials. This type of current transport is known as the thermionic emission, in which the currents flowing from metal to semiconductor and vice versa are equal in magnitude and as a result they cancel each other.

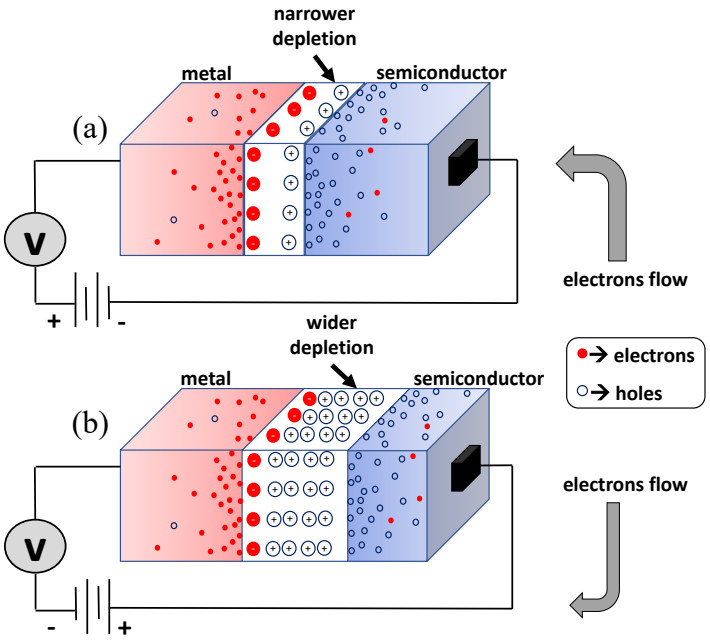


Figure 7.4. Schottky diode mode of operation as a function of the applied potential, (a) forward (varistor) and (b) reverse (varactor)

$$I_D = I_S\left[exp\left(\frac{qV_a}{\eta_n kT}\right) - 1\right] \tag{7.6}$$

where $I_S = the\ saturation\ current = A_j A^* T^2 exp\left(\frac{-q\phi_{bh}}{kT}\right)$

and

A_j = area of the junction

A^* = Richardson's constant (GaN ≈ 26 A.cm ^{2}. K^{-2})

T = absolute temperature

k = Boltzmann's constant (≈ 1.38e-23 J.K^{-1})

ϕ_{bh} = barrier height, which is defined as the difference between the metal work function and the electron affinity (*EA* = the energy

required to move an electron from the conduction band to vacuum) of the semiconductor

η_n = ideality factor, this is a mathematical correction factor added to rectify the diode current nonidealities arise from practical defects, such as imperfections in the active layer caused by crystal structure damage during the growth process or a contamination within the various fabrication steps effecting the Schottky behavior of the anode. Ideally, its value should be a unity, however for GaN material, ideality factor ranges between 1.5-2.5 and higher in some cases [158]–[161].

7.2. Nonlinearities and Harmonics in SBD

As aforementioned, Schottky diodes are majority-carriers-based devices, which in consequence translates into a negligible delay in their switching-time due to a minimal charge storage or lack thereof. Therefore, the DC transfer function, in Eq. (7.6), of the Schottky diode is also applicable for its AC transfer characteristics. Now, in order to identify the origin of harmonics in diodes, rewriting Eq. (7.6) after an RF signal with a DC component (V_{dc}) is inserted to the diode equation [$V_a = V_{dc} + V_{RF}\cos t\omega_{RF}$]. The RF signal has an amplitude V_{RF} and an angular frequency of ω_{RF} the diode current expression becomes:

$$I_D = I_S\left[exp\left(\frac{V_{dc} + V_{RF}\cos t\omega_{RF}}{V_t}\right) - 1\right] \tag{7.7}$$

where $V_t = \eta_n kTq^{-1} \approx$ 25mV at room temperature

By applying Taylor's series expansion followed by trigonometric double-angle identities [162], [163] only to the exponential term that contains the AC component (RF signal) up to the fifth-order term to observe the mathematical basis by which the harmonics are generated, the diode current expression (7.7) can be rearranged as:

$$I_D = I_S\left[exp\left(\frac{V_{dc}}{V_t}\right) exp\left(\frac{V_{RF}\cos t\omega_{RF}}{V_t}\right) - 1\right] \tag{7.8}$$

$$= I_S\left[exp\left(\frac{V_{dc}}{V_t}\right) - 1\right]$$
$$+I_S exp\left(\frac{V_{dc}}{V_t}\right)\left[\frac{V_{RF}\cos t\omega_{RF}}{V_t} + \frac{{V_{RF}}^2\cos^2 t\omega_{RF}}{2{V_t}^2} + \frac{{V_{RF}}^3\cos^3 t\omega_{RF}}{6{V_t}^3}\right.$$
$$\left. + \frac{{V_{RF}}^4\cos^4 t\omega_{RF}}{24{V_t}^4} + \frac{{V_{RF}}^5\cos^5 t\omega_{RF}}{120{V_t}^5} + \ldots\right]$$

$= I_S\left[exp\left(\frac{V_{dc}}{V_t}\right) - 1\right]$ → dc current arose from the DC bias

$+I_S exp\left(\frac{V_{dc}}{V_t}\right)\frac{V_{RF}\cos t\omega_{RF}}{V_t}$ → fundmental RF signal

$+I_S exp\left(\frac{V_{dc}}{V_t}\right)\left[\frac{{V_{RF}}^2}{4{V_t}^2} + \frac{{V_{RF}}^2\cos 2t\omega_{RF}}{4{V_t}^2}\right]$ → DC and 2^{nd} harmonic

$$+I_S exp\left(\frac{V_{dc}}{V_t}\right)\left[\frac{{V_{RF}}^3\cos t\omega_{RF}}{8{V_t}^3} + \frac{{V_{RF}}^3\cos 3t\omega_{RF}}{24{V_t}^3}\right]$$
→ fundmental and 3^{rd} harmonics

$$+I_S exp\left(\frac{V_{dc}}{V_t}\right)\left[\frac{{V_{RF}}^4}{64{V_t}^4} + \frac{{V_{RF}}^4\cos 2t\omega_{RF}}{48{V_t}^4} + \frac{{V_{RF}}^4\cos 4t\omega_{RF}}{192{V_t}^4}\right]$$
→ DC, 2^{nd} and 4^{th} harmonics

$$+I_S exp\left(\frac{V_{dc}}{V_t}\right)\left[\frac{{V_{RF}}^5\cos t\omega_{RF}}{192{V_t}^5} + \frac{{V_{RF}}^5\cos 3t\omega_{RF}}{384{V_t}^5} + \frac{{V_{RF}}^5\cos 5t\omega_{RF}}{1920{V_t}^5}\right]$$
→ fundmental, 3^{rd} and 5^{th} harmonics

$+ \ldots$

From the expression (7.8), it is apparent that the even-terms nonlinearities in the diode produce an additional rectified dc component beside the preceding even harmonics. The odd terms of nonlinearities, on the other hand, only generate odd harmonics. Furthermore, the dc component is usually utilised in power detection circuitry and the generated harmonics are exploited in electronic circuits such as mixers and frequency multipliers.

7.3. Series Resistance and Capacitance

To enhance the diode's performance, it is crucial to have a low series resistance. **Figure 7.5** illustrates the physical origin of the various components that contribute to the total series resistance of the diode. The diode current expression, which includes the series resistance effect is given as:

$$I_D = I_s\left[exp\left(\frac{qV_a - IR_s}{\eta_n kT}\right) - 1\right] \tag{7.9}$$

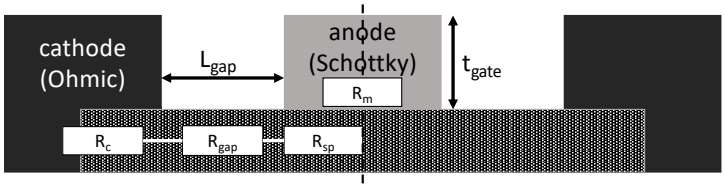


Figure 7.5. Physical representation of the resistive origin in SBD

In general, diode series resistance is comprised of four components: the ohmic contact resistance (R_c), the resistance of the metallic anode (R_m), the anode-cathode gap resistance (R_{gap}) and the spreading resistance beneath the anode (R_{sp}). that includes the aforementioned components that can be expressed as:

$$R_s = \frac{R_m}{3} + \frac{R_c}{2} + R_{gap} + \frac{R_{sp}}{2 * 3} \tag{7.10}$$

where R_m = anode resistance = $W_g\left[N_{anode}t_{gate}L_g\sigma_m\right]^{-1}$

R_c = ohmic contact resistance = $\left[N_{anode}W_g\sigma_c\right]^{-1}$

R_{gap} = resistance under the anode-cathode gap = $L_{gap}\left[N_{anode}W_g\sigma_{gap}\right]^{-1}$

R_{sp} = spreading resistance below the anode = $L_g\left[2N_{anode}W_g\sigma_{gap}\right]^{-1}$

N_{anode} = number of anode fingers

σ_m = conductivity of anode metal

σ_c = contact conductivity

σ_{gap} = conductivity of gap between anode and cathode

t_{gate} = thickness of anode metal

W_g, L_g and L_{gap} are the anode width, anode length and anode-cathode distance, respectively. The factor 2, is used due to ohmic contact being on both sides of the Schottky. Furthermore, the other factor, 3, is added to make up for the anode metal and the spreading resistances being effective and distrusted by three metal contacts (2 ohmic and the anode itself) [164].

However, due to depletion region being so thin, the Schottky/2DEG diode series resistance, which can be calculated using Eq. (7.11), is largely composed of ohmic contact resistance (R_C) and the sheet resistance of the semiconductor (R_{2DEG}) [165]. The latter is inversely proportional to the electron mobility (μ_n) and the electron concentration (N_d) in the 2DEG. Since the contact resistance arises from the ohmic cathodes on both sides of the anode, a factor of 2 is added to R_C [165].

$$\begin{gathered} R_s = 2R_c + R_{2DEG} \\ R_s = 2\left[N_{anode} W_g \sigma_c\right]^{-1} + \left[L_{gap} - W_d\right]\left[q N_d \mu_n W_g N_{anode}\right]^{-1} \end{gathered} \tag{7.11}$$

Knowing the contact specific resistivity from TLM and the sheet resistance value of the semiconductor from wafer characterisation using Hall measurements, Eq. (7.12) can be rewritten and further simplified to:

$$R_s = \frac{2\rho_C + L_{gap} R_{GaN\_sheet}}{N_{anode} W_g} \tag{7.12}$$

The total SBD junction capacitance may be calculated using the expression:

$$C_{j0} = \frac{W_g L_g \varepsilon_s N_{anode}}{W_d} \tag{7.13}$$

Furthermore, in order to predict the diode capacitance accurately, the capacitance per anode finger maybe calculated using this expression [164]:

$$C_{j0}(per\ anode) = \frac{W_g L_g \varepsilon_s}{W_d}\left[1 + \frac{2W_d}{L_g} - \frac{4W_d}{L_g + 2W_d}\right] \tag{7.14}$$

However, to consider the effect of the distance between the cathode and anode, L_{gap}, and the Schottky metallic thickness, t_{gate}, the capacitance per anode can be given as:

$$C_{j0}(per\ anode) = 2\left(\frac{W_g (t_{gate} + W_d)\varepsilon_s}{L_{gap}}\right) \tag{7.15}$$

It is manifested from **Figure 7.6** that the zero-bias junction capacitance of the diode is directly and linearly proportional to the width of the anode. On the other hand, the series resistance is decreasing exponentially with the anode width increase. Therefore, a trade-off is evident between the anode width on one side and the junction capacitance and series resistance on the other side. However, since the anode with and the series resistance have an exponential relation, 10-25 μm is a good trade-off range between the junction capacitance and the series resistance. Although, lowering both components have a positive effect on the cutoff frequency of the diode, series resistance is more important to be lowered as it is responsible for the power dissipation in circuits such as frequency multipliers.

Figure 7.6, **Figure 7.7**, **Figure 7.8** and **Figure 7.9** show the calculated series resistance, junction capacitance and the cut-off frequency as a function of different width, length and number of fingers.

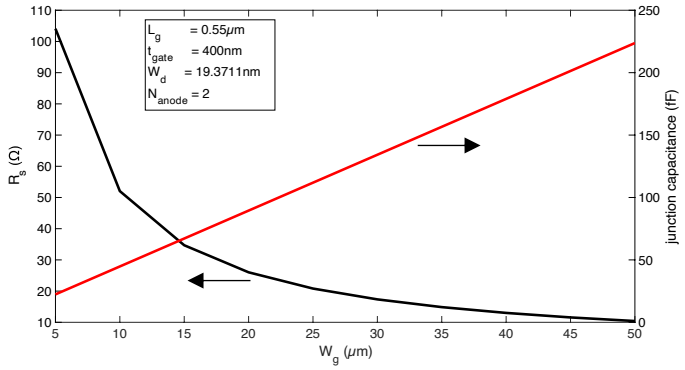


Figure 7.6. The SBD series resistance and cutoff frequency as a function of its width

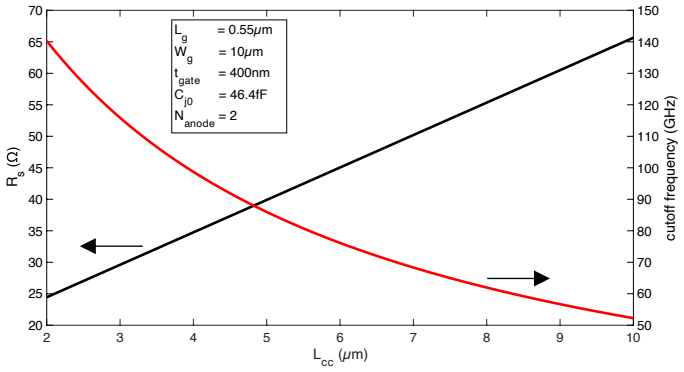


Figure 7.7. The SBD series resistance and cutoff frequency as a function of the cathode-cathode distance

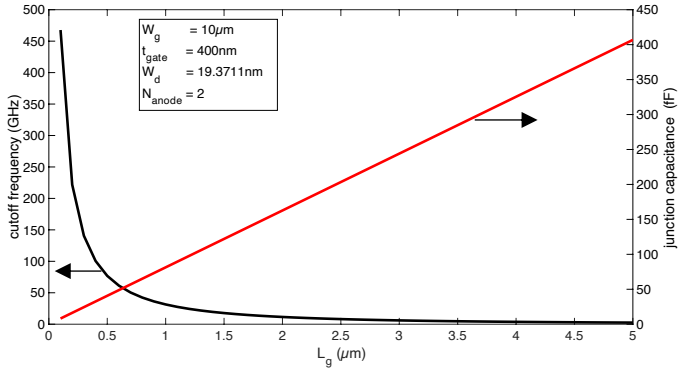


Figure 7.8. The SBD junction capacitance and cutoff frequency as a function of its length

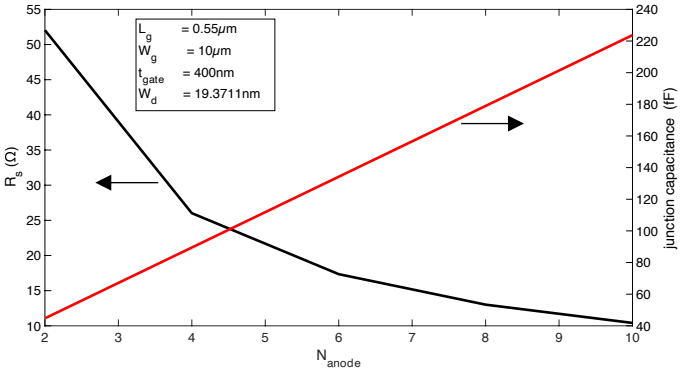


Figure 7.9. The SBD series resistance and capacitance as a function of the number of anode fingers

7.4. SBD Characterization

The most used figure of merit (FOM) to characterise varactor diode is the dynamic cutoff frequency, which is a detriment of the maximum operational frequency before the diode is unusable. Practically, the diode actual operational frequency

range is usually less than the cutoff frequency and it can be obtained using the given equation:

$$f_c = \frac{S_{max} - S_{min}}{2\pi R_s} \approx \frac{S_{max}}{2\pi R_s} \rightarrow \text{assuming } S_{min} \; is \text{ negligible} \tag{7.16}$$

where $S_{max} = \frac{1}{C_{min}}$ maximum elastance near breakdown voltage

$S_{min} = \frac{1}{C_{max}}$ minimum elastance at zero-bias

Another FOM to characterise varactor diode (which is simply a diode in a reverse-bias mode) is by analysing its dynamics (F_C) at the desired operational frequency (output frequency in case of a multiplier) and it is computed using the expression:

$$F_C = \frac{S_{max}}{2\pi f_0 R_s} = \frac{f_c}{f_0} \tag{7.17}$$

where f_0 = the frequency at which the varactor's dynamic value is assessed. High F_C translates into higher efficiency when designing frequency multiplier as to be shown in later section.

Additionally, an important FOM is the capacitance or elastance modulation ratio between the maximum and minimum capacitance, or elastance, at zero and near-breakdown voltages, respectively. In order for the diode to exhibit a high cutoff frequency, the C_{mr} FOM must be relatively large (> 10), which can be calculated using the expression [166]:

$$C_{mr} = \frac{C_{max}}{C_{min}} = \frac{S_{max}}{S_{min}} \tag{7.18}$$

This can be achieved by increasing the number of anodes, which would result in a wider gap between the minimum and maximum capacitance and lower the series resistance. Nevertheless, increasing the number of anodes may have a negative impact on the breakdown voltage and the saturation current.

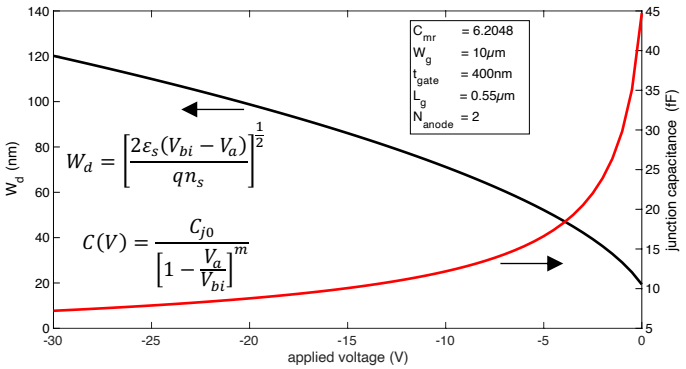


Figure 7.10. Junction capacitance and depletion width as a function of the reversed applied voltage

Figure 7.10 and **Figure 7.11** depict the dynamics of the SBD as function of the applied reversed voltage.

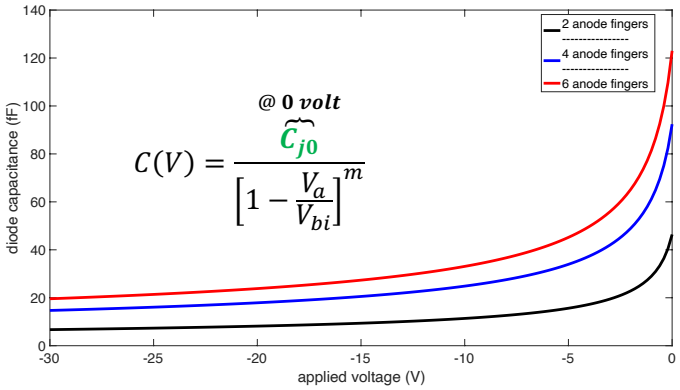


Figure 7.11. The SBD capacitance as a function of the applied reversed voltage for a different finger-number

7.5. Reverse Breakdown Voltage

Breakdown voltage is critical in application such as frequency multipliers when used in varactor reverse-bias mode. Higher breakdown voltage contributes to increased output power and conversion efficiency because of a higher ratio between the minimum and maximum elastance of the diode. The breakdown voltage can be calculated using Eq. (7.19) and it can be observed that its value is directly proportional to the critical electric field and inversely proportional to the doping or charge density in the 2DEG [167], [168].

$$V_{BV} = \frac{\varepsilon_s (E_c)^2}{2qn_s} - V_{bi} \tag{7.19}$$

where E_c = the critical electric field (GaN ≈ 3300 kV/cm)

From **Figure 7.12**, GaN material exhibited higher breakdown capability compared to GaAs and Si. Therefore, GaN is clearly superior to other materials regarding its dynamics, computed from (7.17) , as an effect of the breakdown voltage.

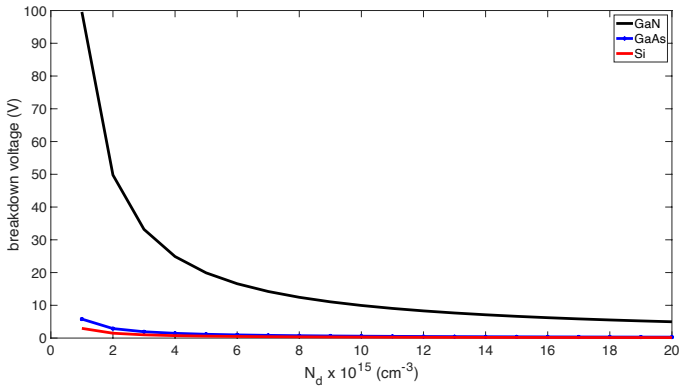


Figure 7.12. The SBD breakdown voltage as a function of the doping density or electron concentration

7.6. Varactors in Frequency Convertors

A diode-based frequency multiplier is dependent on the nonlinearities of the device. The nonlinearities can be either resistive current-voltage (*I*-*V*) or reactive charge-voltage (*Q*-*V*) relations, varistor and varactor, respectively. In this project, the *Q*-*V* nonlinearities is opted to maximise the efficiency at the expense of operable bandwidth. Theoretically, the available efficiency for varactor-based multiplier is 100%, whereas the varistor multipliers are limited by a factor of $1/n^2$ where n is the multiplication factor of the frequency multiplier (25% maximum efficiency for a double, for example) [169]. Since a varactor diode topology is chosen, recalling eq. (7.5), the elastance (S) which is the reciprocal of the capacitance can be expressed as [170]:

$$S = S_0[1 + m_1 e^{j\omega t} + m_1^* e^{-j\omega t} + m_2 e^{j2\omega t} + m_2^* e^{-j2\omega t} + \cdots] \qquad (7.20)$$

where m_1 and m_2, known as the elastance modulation factors, = 0.502 and 0.166, respectively, and S_0 = the elastance at the bias.

Eq. (7.20) assumes that the frequency doubler is ideal and only the fundamental and the second harmonic are present in the system. The relation between S_0 and the bias voltage can be displayed as:

$$V_{bias} = V_{bi} - V_{bi}\left[C_{j0}S_0\right]^2[1 + 2|m_1|^2 + 2|m_2|^2] \tag{7.21}$$

Now, the power in the system that is generated by such capacitance nonlinearities which satisfies the aforementioned assumptions can be written as:

$$\begin{cases} P_{system} = 4{V_{bi}}^2 C_{j0}\left[C_{j0}S_0\right]^3 \omega|m_1|^2|m_2| \\ P_{loss\_f_0} = 4{V_{bi}}^2 {C_{j0}}^2\left[C_{j0}S_0\right]^2 \omega^2|m_1|^2 R_s \\ P_{loss\_2f_0} = 16{V_{bi}}^2 {C_{j0}}^2\left[C_{j0}S_0\right]^2 \omega^2|m_2|^2 R_s \end{cases} \tag{7.22}$$

As a result, the input power at the fundamental (f_0), the output power at the second harmonic ($2f_0$) and the conversion efficiency (η) can be obtained from eq. (7.23).

$$\begin{cases} P_{in} = P_{system} + P_{loss\_f_0} + P_{loss\_2f_0} \\ P_{out} = P_{system} \\ \eta\ (\%) = \left[\dfrac{P_{out}}{P_{in}}\right] \times 100. \end{cases} \tag{7.23}$$

Figure 7.13, **Figure 7.14** and **Figure 7.15** demonstrate the effects of series resistance, junction capacitance and the applied voltage on the input and output power and the acquired conversion efficiency.

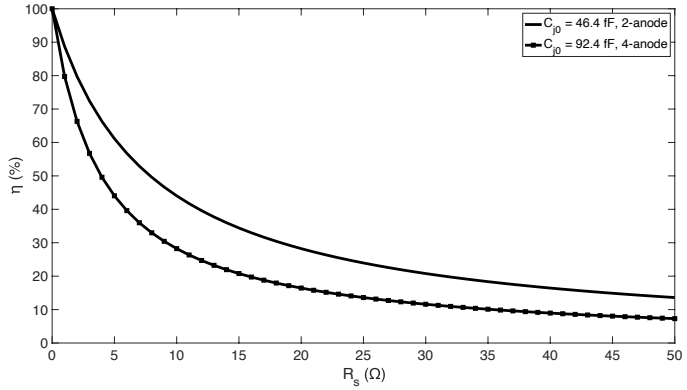


Figure 7.13. The SBD conversion efficiency as a function of its series resistance

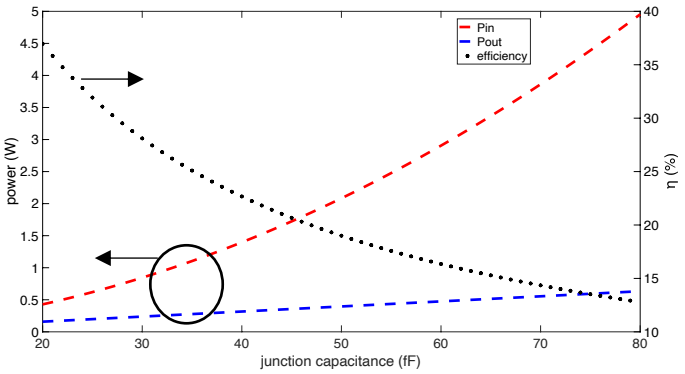


Figure 7.14. The SBD conversion efficiency and input/output power as a function of its junction capacitance

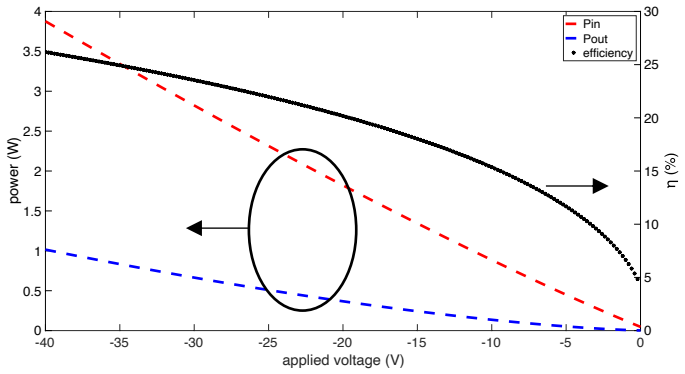


Figure 7.15. The SBD conversion efficiency and input/output power as a function of the applied voltage

7.7. Layout and Design

Two different physical layouts of Schottky contact diodes were designed and fabricated during this project. The first type of Schottky contact diode is embedded in a coplanar waveguide structure as shown in **Figure 7.16**.(a). This was used for RF measurements to obtain the small signal equivalent circuit and RF behavior of the diode. The layout of this diode consisted of Schottky finger (anode) length of 500nm embedded in a coplanar waveguide structure. In this work, a T-shaped cross section structure devices were used with six and four finger devices with total anode width of 5 and 10 μm were realised. The cross-sectional geometry of various structures is shown in **Figure 7.2**. Changing the Schottky contact area by changing the Schottky finger length (L_g) and width (W_g) will affect the junction capacitance (C_j). Increasing the number of Schottky contact

fingers (n) for a constant anode width reduces the series resistance. The separation between ohmic and Schottky contacts was to be 2.0μm to minimise the series resistance and metal-to-metal capacitance whilst maximising process reliability and yield. The second type is a large area circular diode (180μm diameter) Schottky-contact with a 20μm anode-cathode gap as shown in **Figure 7.16**.(b). This diode structure was used to obtain the *I-V* and *C-V* characteristics.

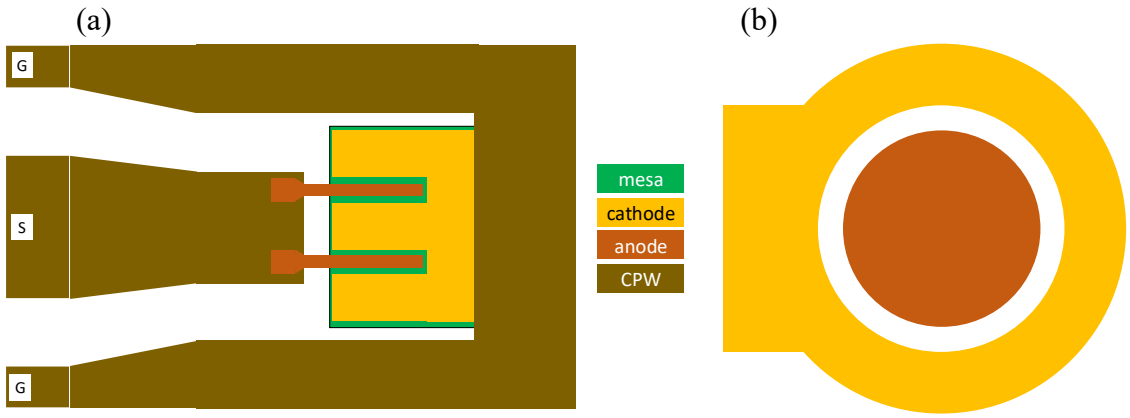


Figure 7.16. The actual layouts for (a) the embedded 2-anode (2-finger) RF SBD in CPW environment and (b) large area circular DC diode

7.8. Novel Trenched-Anode SBDs

GaN-based SBDs with low onset voltage (V_{ON}), high reverse-breakdown (V_{BV}) voltage, and low reverse-current leakage (I_R), high-switching speed (R_{ON}) and high cutoff frequency (f_c) are essentially required to compete with current III-V technologies. Conventional GaN based SBD DC and RF performance is still limited to their large V_{ON}, switching loss and RF leakage when utilising LR Si substrates. Several researchers have recently proposed low V_{ON} along with low I_R and high V_{BV} technologies, including recessed anode, dual-field plates, regrowth cathodes, and dual channel field-effect rectifier. However, these approaches require accurate control of anode etching to the 2DEG and a complicated fabrication process, which incorporates reliability issues and extra processing cost. Nevertheless, a 3-D SBDs integrated with a tri-gate MOS structure has shown outstanding DC characteristics at the expense of RF performance owing to the inherently large junction capacitance (C_j) and series resistance (R_S) [171]. Therefore, these techniques are only limited to low-

frequency applications. To date, most of the research effort into GaN-based SBDs on silicon is predominantly focused on power electronics, with limited literature targeting RF operation. However, achieving high fc while maintaining low IR and superior V_{BV} remains a challenge. In this work, an optimised multi-channel RF AlGaN/GaN SBDs on LR Si structure is demonstrated using a cost-effective (GaN on LR Si) which is fully compatible with III-V THz monolithic integrated circuit (THz-MIC) technology. In contrast, to conventional SBDs, the newly developed devices significantly enhanced the turn-on characteristics, switching loss, ideality factor (η_n) and f_c, where a V_{ON} = 0.84 V, R_{ON} = 0.97 Ω·mm, V_{BV} > 30 V, η_n = 1.69 and f_c = 0.6 THz were achieved. This is attributed to the direct contact of Schottky anode to 2DEG at the sidewalls of the multi-mesa trenches along with proper design geometries to suppress substrate coupling effects.

Figure 7.17 indicates a cross-section of the fabricated AlGaN/GaN SBDs on LR Si using a multi-channel structure, which was simultaneously fabricated with conventional SBDs on the same substrate to allow precise comparison. A combination of multi-mesa and T-shaped structures was adopted to form the anode to reduce Schottky barrier height and anode resistivity, respectively. The height (H_F), width (W_F), spacing (S_F) and length (L_F) of the nanowires were ~50, 41, 89 nm and 2 μm, respectively. The Anode length (L_A) and anode head length (L_{AH}) were 0.550 μm and 1.1 μm, respectively, whereas the junction length (L_j) was 4.28 μm. The total physical anode width was 2 × 10 μm, while the effective anode width for the fin-like anode structure was 2×5.83μm.

The epitaxy material used in this work was grown on LR Si (111) (ρ < 40 Ω.cm) provided by Nexperia. The epilayer consists of 4.65 μm buffer, 20 nm $Al_{0.2}Ga_{0.8}N$ barrier and 3 nm GaN cap layer. A sheet carrier density of 5.9 × 10^{12} cm^{-2} and electron mobility of 1713 cm^2/Vs are determined by using Hall measurements.

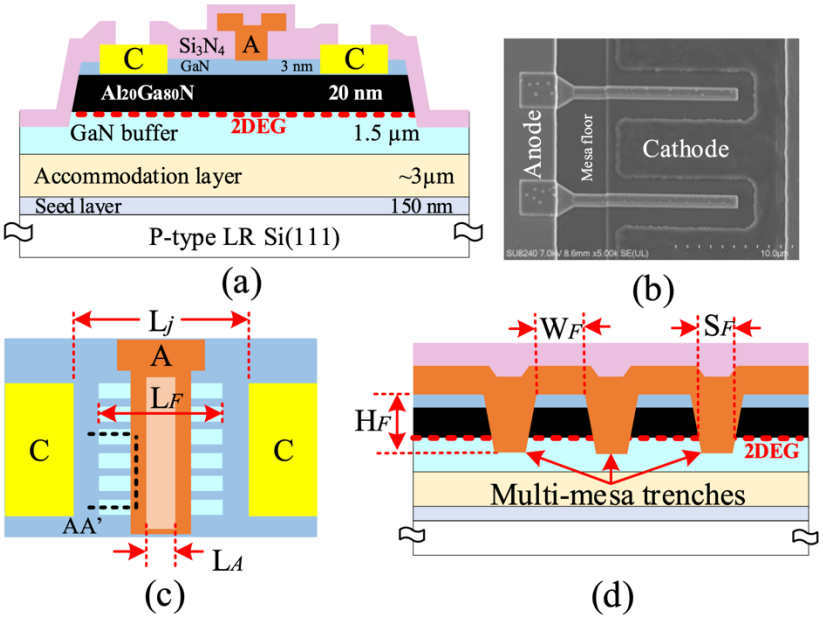


Figure 7.17. (a) Cross-sectional view, (b) scanned-electron microscope (SEM) image, and (c) top-view of the multi-channel SBDs, and (d) Cross-sectional representation of the tri-anode along line AA'

The device fabrication started with defining the Ti/Pt markers, followed by the deposition of Ti/Al/Ni/Au ohmic contacts and rapid thermal annealing at 790 °C in N_2 environment to form the cathode. Next, a ~150 nm depth mesa isolation was performed through Cl_2/Ar-based inductively coupled plasma (ICP). Then, multi-mesa trenches were defined by e-beam lithography and subsequently etched using Cl_2/Ar-based ICP with an etch depth of ~50 nm. A 100 nm Si_3N_4 passivation layer was then deposited using a low-stress inductively coupled plasma chemical vapor deposition (ICP-CVD) at room temperature. To form the T-shaped anode, E-beam lithography was used to define anode foot trenches through the Si_3N_4 passivation layer using a low damage SF_6/N_2 gas mixture reactive-ion etching (RIE), which was followed by Ni/Au metal stack evaporation to finish the T-shaped anode. Windows in the Si_3N_4 at the cathode areas were etched prior to the deposition of Ti/Au bond pads and 160 nm Si_3N_4 layer as a final passivation layer. Device fabrication was finalised by Si_3N_4 etching in the measurement pad regions. The dimensions of the fabricated devices are outlined in **Table 7.1**.

Table 7.1. Dimensions of the fabricated devices

Dimensions (nm) →	L_A	L_{AH}	L_j	W_g	H_F	W_F	S_F	L_F
Conventional	1.1k	550	4.28k	10k				
Multi-channel	1.1k	550	4.28k	*10k	50	41	89	2k

*Due to trenches, the effective width of the multi-channel (W_g) is 5.83μm

7.8.1. DC Characteristics

Figure 7.18 indicates the typical *I-V* characteristics of the fabricated conventional and multi-channel structures at room temperature using a linear scale. The diode current (A/mm) and resistance (Ω·mm) of conventional and multi-channel structures are normalised by the total physical anode width (2×10μm) and effective anode width (2×5.83μm), respectively. **Figure 7.18** reveals that incorporating a multi-channel anode structure reduced V_{ON} from 1.246 to 0.84V together with improved R_{ON} from 1.52 to 0.97 to Ω·mm. This is attributed to the direct anode contact to the 2DEG, where the anode is wrapped around the narrow AlGaN/GaN bodies.

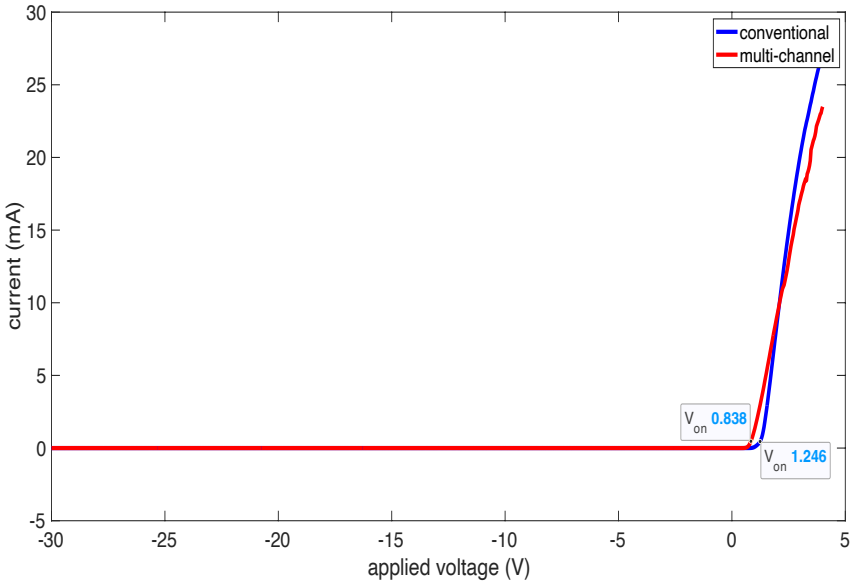


Figure 7.18. Conventional and multi-channel SBDs *I-V* curves

To further analyse these findings, the semilog I-V plot (shown in **Figure 7.19**) is used, which allows the extraction of η_n, and Φ_{bh}. Based on the analytical equations indicated in [8]. Both device structures exhibited η_n between 1 and 2, indicates the presence of conduction mechanism besides a thermionic emission

mechanism. An improvement of 14.28 % in η_n (from 1.97 to 1.69) was obtained by the developed multi-channel structure as compared to conventional SBDs. Furthermore, the observed reduction in V_{ON} when using the new structure corresponds to a reduction of 17.5 % in n (from 0.78 to 0.64 eV). However, I_R was slightly increased with the multi-channel structure, where I_R < 38 μA/mm was performed at a reverse voltage of up to 30 V. This is attributed to the additional anode length where the anode is in direct contact to the GaN buffer in the multi-mesa floor regions. The achieved results are comparable to that of SBDs on semi-insulating (SI) SiC with recessed anode and regrowth cathode technologies, with better V_{BV} and I_R [172]. This enhancement is mainly attributed to the scale of anode-to-cathode spacing and the use of T-shaped anode, owing to the reduction in peak electric field of Schottky junction.

The following set of equations are used to extract the DC parameters:

$$I_D = I_S\left[exp\left(\frac{qV}{\eta_n kT}\right)\right] \tag{7.24}$$

rearrangement of the above equation,

$$\frac{I_1}{I_2} = \left[exp\left(\frac{q(V_1 - V_2)}{\eta_n kT}\right)\right] \tag{7.25}$$

then,

$$\Delta V = (V_1 - V_2) = \left[\frac{\eta_n kT}{q}\right](\log_{10}(e)) \tag{7.26}$$

where e = 2.718

ΔV = the change of voltage which corresponds to the change in current per decade.

Now, the ideality factor is calculated as:

$$\eta_n = \left[\frac{q\Delta V}{kT}\right](\log_{10}(e)) \tag{7.27}$$

And the barrier height is deduced using the expression:

$$\phi_{bh} = \left[\frac{kT}{q}\right] \ln\left[\frac{T^2 A^*}{I_s}\right] \tag{7.28}$$

where I_s = the extracted current value from the *I-V* semilog plot at the zero-voltage point, k is Boltzmann constant T is the diode temperature and A^* is Richardson constant.

Finally, the series resistance is obtained using equation:

$$R_s = \frac{\Delta V}{I_{fd}} \tag{7.29}$$

where I_{fd} = the first higher current at the point where the voltage, due to slope decrease caused by the voltage drop across the series resistance, is deviated from the straight fit line of the semilog curve.

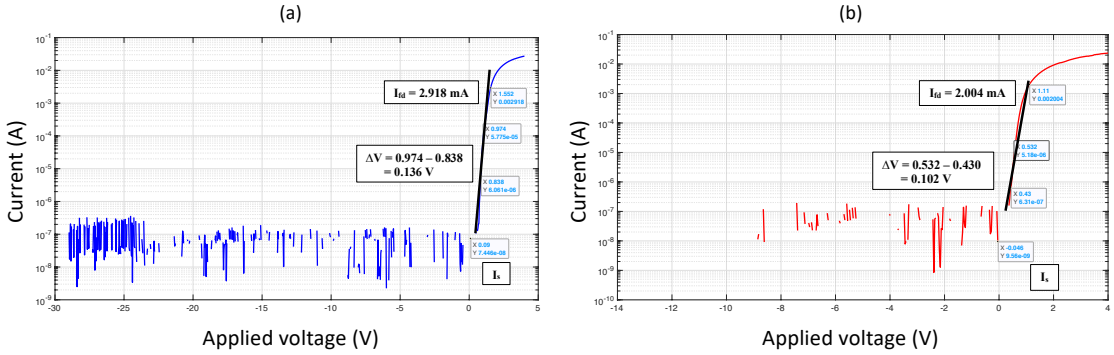


Figure 7.19. SBDs *I-V* semilog, (a) conventional and (b) multi-channel

The extracted values of C_j as a function of the applied voltage of the fabricated devices are shown in **Figure 7.20**.(a). Cj was inversely proportional to the applied reverse voltage, where a sharp drop in C_j was obtained when changing the voltage form 0 to −2 V. Furthermore, owing to the direct anode contact to 2DEG for multi-channel SBDs, C_j was significantly reduced at reverse biases beyond −2 V, as compared to conventional SBDs. This reflected a dramatic enhancement in f_c which can be calculated from R_S and C_j. Therefore, f_c was improved by 32.7

% (from 457 to 607 GHz), as shown in **Figure 7.20**.(b). However, the achieved f_c of the fabricated lateral SBDs on LR Si is still limited to their larger R_S, which mainly depends on material growth quality and cathode contact resistivity, as compared to SBDs realised on GaN on a semi-insulating SiC substrates.

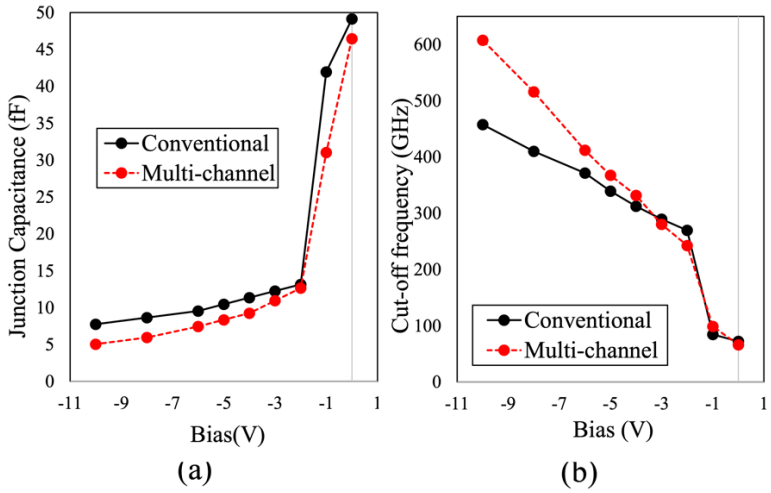


Figure 7.20. *C-V* measurement of the 90 µm diameter circular Schottky diode, (a) capacitance and (b) corresponding cutoff frequency

7.8.2. RF Behavior and Small Signal Model

On-wafer small-signal S-parameters measurements were performed in the frequency range 0.1 to 110 GHz using an Agilent PNA network analyser (E8361A) and frequency extenders (N5260A). The system was calibrated with an off-wafer calibration impedance standard substrate (ISS), using a Short-Open-Load-Thru (SOLT) calibration technique.

Figure 7.21 shows the extracted small-signal circuit model of the devices, which was validated by the good agreement between modeled and measured S-parameters up to 110 GHz, as shown in **Figure 7.22**. This allows the extraction of SBD intrinsic elements, junction resistance (R_j), C_j and Rs, which used to determine fc of the fabricated devices. As indicated in **Figure 7.21**, unlike SI-substrates, substrate parasitic elements (S_{sub} and R_{sub}) are incorporated into the standard SBD circuit model when considering lossy Si as a substrate. Furthermore, C_p and L_P represents pad parasitic components. However, the

external parasitic elements have a significant influence on the model at frequencies beyond 20 GHz.

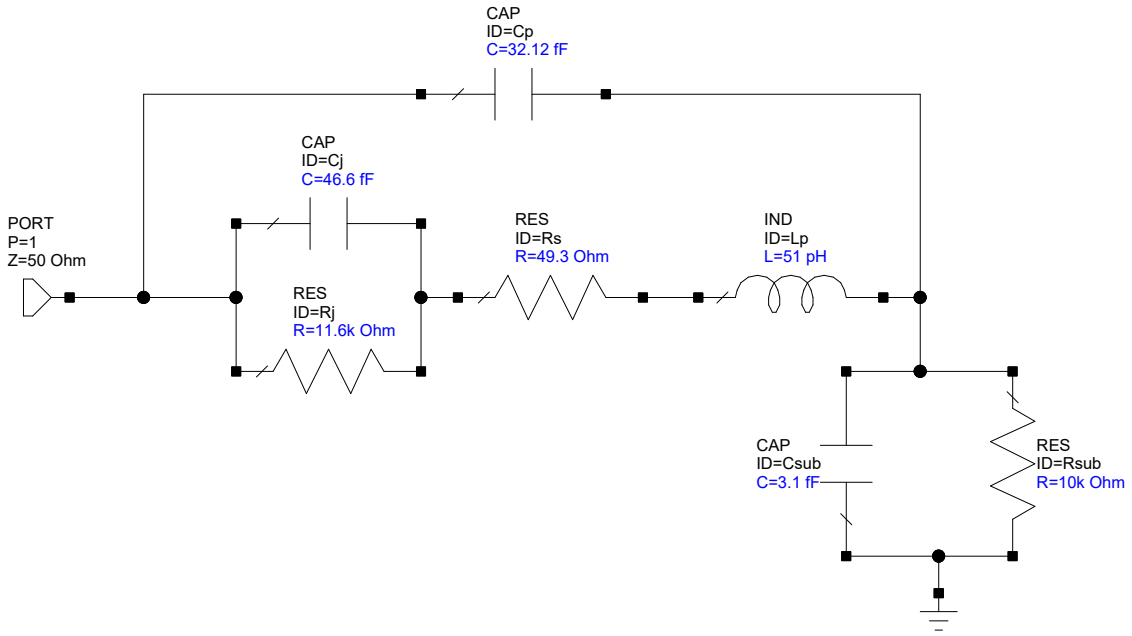


Figure 7.21. Multi-channel SBD small signal model

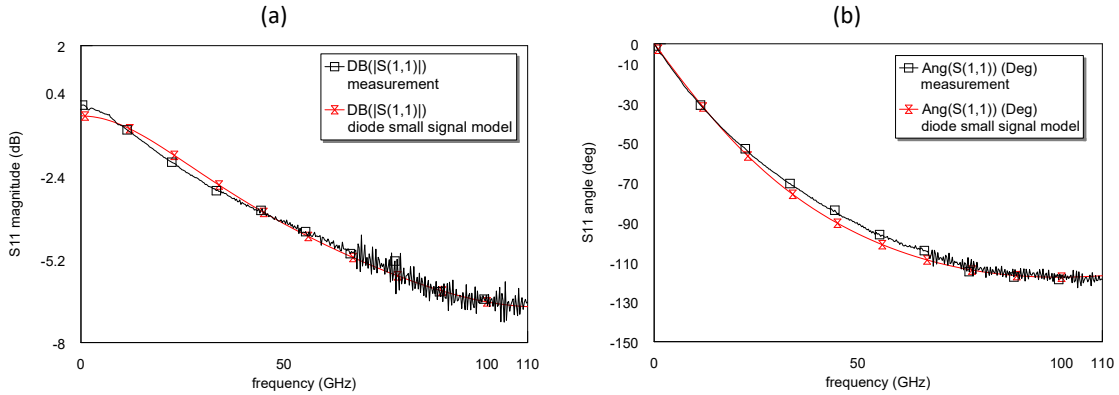


Figure 7.22. Magnitude (a) and phase (b) of the return loss, measurement vs model

Table 7.2 shows the extracted circuit element values of conventional and multi-channel structures at no bias (0V). In contrast to conventional SBDs, an increase in R_S by 15.6 % (44.9 to 51.9) and a slight reduction in C_j by 5.5 % (from 49.1 to 46.4 fF) were observed for the newly developed fin-type technology. This is attributed to the additional anode length in the multi-mesa trenches and reduction

in n, respectively. In addition, the low capacitance value of C_{sub} and high resistance value of R_{sub} (3.1 fF and 10kΩ, respectively) indicates that substrate coupling effect could be neglected in both design structures. This was a result of the proper design geometries where the anode-to-cathode separation (2.42 µm) is less than the buffer thickness (4.65 µm).

Table 7.2. The SBD small signal model and *I-V* extracted key parameters

Parameters →	**C_j (fF)**	**R_s (Ω)**	**I_s (A)**	**η_n**	**Φ_{bh} (eV)**	**V_{BV} (V)**
Conventional (2-anode)	48.3	44.6	7.45e-8	1.97	0.78	-30
Multi-channel (2-anode)	46.4	49.3	9.56e-9	1.69	0.64	-30

The developed multi-channel RF lateral AlGaN/GaN SBD on LR Si technology has been realised in this work. A V_{ON} of 0.84 V along with R_{ON} of 0.97 Ω·mm and η_n of 1.69 were achieved because of the direct Schottky anode contact to the 2DEG resulting in a Φ_{bh} of 0.64 eV. The fabricated devices exhibited V_{BV} of greater than 30 V along with I_R of less than 38 µm/mm. In addition, a newly proposed small-signal circuit model was introduced up to 110 GHz. The models are exhibiting a similar *I-V* characteristics, as shown in **Figure 7.23**, which are comparable to the measured results of the devices. An f_c of 0.6 THz at a reverse bias of -10 V was achieved because of the optimised SBD design structure and geometries. These findings enable an effective methodology for the realisation of high-performance sub-THz-MIC topologies.

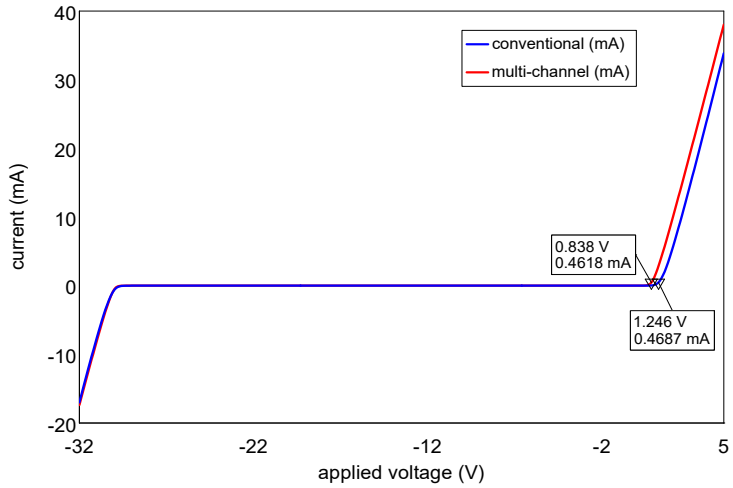


Figure 7.23. *I-V* curves of the conventional and multi-channel SBDs models

7.9. Summary

In this chapter, a novel diode structure was proposed to reduce the barrier height by having a direct contact between the anode and the 2DEG channel. This was achieved by etching trenches below the anode across the channel. This has resulted in a clear reduction of the Schottky barrier height from 0.78 to 0.64 initiated by the implantation of the channel trenches. Therefore, the reduction in barrier height led to a decrease in the turn-on voltage and resistance as well. In addition, a newly proposed small-signal circuit model was introduced up to 110 GHz. And an f_c of 0.6 THz at a reverse bias of -10 V was achieved because of the optimised SBD design structure and geometries. These outcomes can be capitalised on to enable an effective approach for the realisation of high-performance sub-THz-MIC topologies.

8. CONCLUSIONS AND FUTURE WORK

GaN HEMTs are particularly promising for future RF and power applications because of their excellent features such as high 2DEG sheet carrier density and mobility, as well as high breakdown fields. GaN is emerging as the future of semiconductors because of its intrinsic features such as electron mobility and saturation velocity, which make high-power devices at microwave frequencies with a significantly increased power density possible. To suppress the 2DEG and electrically insulate devices, HEMT manufacturing nowadays comprises an isolation method conducted by standard mesa etch or ion implantation. Even though a 3D-structure device is created by physically removing material, the former, mesa, is extensively employed for cost reasons. The inclusion of a nonplanar structure in HEMTs, on the other hand, leads in a large gate leakage current, which reduces noise performance in RF amplifiers and can cause the device to prematurely collapse. There's also the possibility of a metallic breakage in the gate near the mesa's edge. In addition, several passive and active devices were simulated, constructed, and modelled to better understand the behavior of the wafers and the implications of the lossy silicon substrates. To compare the performance of GaN produced on various substrates, a loss mechanism study was conducted using the CPW distributed element circuit model. Using GaN-on-LR-Si, a CPW transmission line, RF PCM, MIM capacitor, meander inductor, and HEMTs were built, and the findings indicated that the substrate's lossy behavior, and the upper operation frequency limit is around 10GHz.

8.1. Novel Planar Gate Formation

8.1.1. Summary and Key Findings

A unique and novel structure is presented to address mesa etch problems such as sidewall profile, the common gate discontinuity, and gate leakage caused by a gate direct contact with 2DEG. The suggested construction requires a small expansion of the mesa to deposit the gate-feed, ensuring a totally planar gate creation. Therefore, the gate leakage was decreased by an order of magnitude. However, because the gate-feed is located on an active layer with a very low resistance owing to a substantially longer length in contrast to the real gate, the

gate became conductive above the pinch-off point, and gate leakage increased. As a result, a dielectric is deposited below the gate-feed to address the developing issue, resulting in an increase in drain leakage at the off-state due to the large dielectric thickness. No compromise to the RF performance was observed for the proposed devices.

8.1.2. Future Research

This can be avoided by employing techniques such as atomic layer deposition for a denser yet shallower (a few nm) dielectric coating below the gate-feed. Finally, the suggested structure will allow for a deeper etch of the active layer for heat control while maintaining the gate metal's integrity.

Also, more investigation is needed to increase the current transport limitations between the metallic contacts and the semiconductors. Conventionally and at the device level, this is performed by scaling the device width or increasing the number of gate fingers [173]. Although, these approaches offer an increase to the total current flowing between the contacts, the devices will occupy larger area to accommodate the required dimension scaling. Hence, the current or the power density will not be improved as was shown in this work. Furthermore, the reduction of distance between the source and the drain can lower the access resistance but will cause the device to be more prone to the short-channel effect.

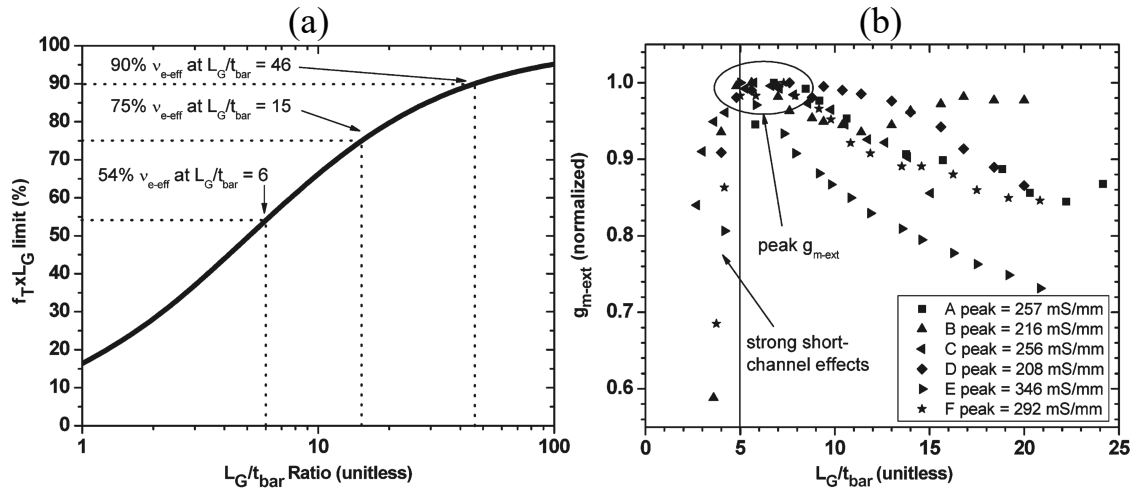


Figure 8.1. Aspect ratio limitations effects on (a) v_{eff} and (b) g_m [174]

Another technique, at the material level, is to increase the 2DEG charge density of the materials. This can be achieved by increasing the barrier thickness or the

Al composition in the barrier as explained in Chapter (**2**). Nonetheless, other factors must be taken into considerations such as the device aspect ratio (AR) and lattice mismatch accommodation. The former can alter the device RF performance (namely, f_T and f_{max}), effective electron velocity (v_{eff}) and the current modulation efficiency (g_m), as presented in **Figure 8.1**. With respect to material mismatch as a factor of consideration, designing a well-matched lattice epitaxy is complex and not cost-effective. Hence, the charge density enhancement approach is not recommended in comparison with a device-level engineering.

Now, a less-complex solution can be realised with the introduction of slots at the edges between ohmic contacts as shown in **Figure 8.2**. This may cause the resistance at the transfer length region (shown by the dotted line in **Figure 8.2**) to be increased. Thus, as the resistance is enhanced within the L_T region, the electrons (current) are forced to push further into the ohmic contacts to look for a lower resistance path. This as a result, may improve the electron velocity of the device and increase the acquired maximum current density.

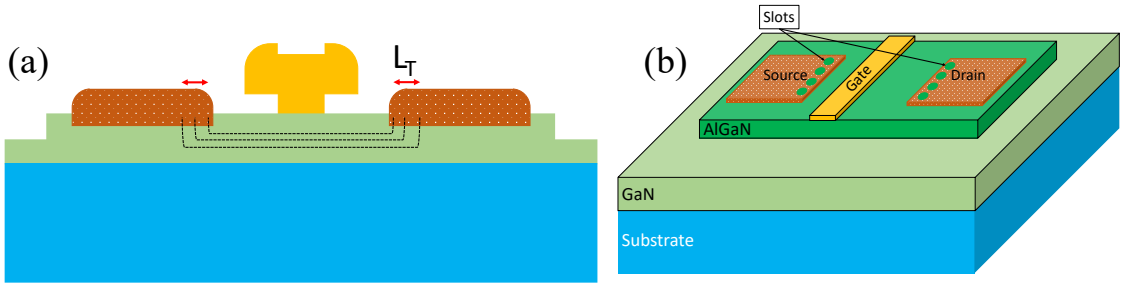


Figure 8.2. (a) transfer length region and (b) the proposed future work

8.2. Novel Multi-trenched Diodes

8.2.1. Summary and Key Findings

A novel diode structure was proposed to reduce the barrier height by having a direct contact between the anode and the 2DEG channel. This was achieved by etching trenches below the anode across the channel. This has resulted in a clear reduction of the Schottky barrier height from 0.78 to 0.64 initiated by the implantation of the channel trenches. Therefore, the reduction in barrier height led to a decrease in the turn-on voltage and resistance as well. In addition, a

newly proposed small-signal circuit model was introduced up to 110 GHz. And an f_c of 0.6 THz at a reverse bias of -10 V was achieved because of the optimised SBD design structure and geometries. These outcomes can be capitalised on to enable an effective approach for the realisation of high-performance sub-THz-MIC topologies.

8.2.2. Future Research

The newly developed diode can be further implemented in actual electronic circuity to demonstrate the potential of the proposed fabricated diodes and observe the effect of the enchantment achieved due to the reduction of the Schottky barrier height. The diodes will be employed in frequency multipliers, RF passive mixers, and power detectors as a next step. **Figure 8.3** shows a simulation comparison between the fabricated SBDs utilized in a frequency doubler. The diodes were negatively biased (varactor mode) to produce their capacitance/voltage nonlinearities for better efficiency at the expense of a narrower bandwidth. The circuit simulation results demonstrate a better efficiency is acquired when using the multi-channel diode with more than 8% improvement, indicating a potential use in millimetre wave and THz applications.

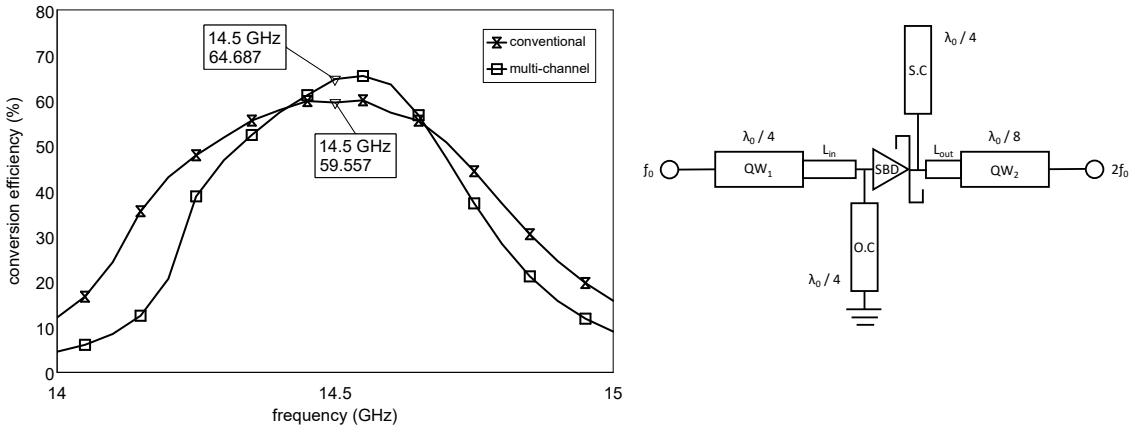


Figure 8.3. A conventional/multi-channel SBDs-based frequency multiplier simulation conversion efficiency comparison (left) and the circuit block diagram (right).

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