Bypass arm based DC fault isolation scheme for MMC-HVDC systems

Yaoqiang Wang[1,2] · Ruyin Sun[1,2] · Yanxun Guo[1,2*] · Kewen Wang[1,2] · Jun Liang[1,3]

Abstract

High voltage direct current transmission based on a modular multilevel converter (MMC-HVDC) is an effective method to solve the grid connection of the new energy. A DC fault is an issue that must be solved for MMC-HVDC. This paper proposes a protection scheme for HVDC converters to quickly suppress DC fault current without increasing the operation loss. By employing a bypass arm in conjunction with a switch-type zero-loss current limiter (SZCL), most of the DC current in the bridge arm flows through the bypass arm so the fault current of the power devices is reduced. There are a number of main advantages of this scheme. The fault isolation time can be greatly shortened, the cost of the system is effectively reduced, the steady-state operation loss of the system does not increase, the operation of the AC-grid can be maintained stably when a DC fault occurs, and the overcurrent impulse to the AC-grid is reduced. The proposed scheme is applicable to two-terminal systems and the DC grid, especially for faults at the converter outlet of the DC grid. Simulation results using PSCAD/EMTDC show the superiority of the proposed scheme when compared with other schemes and a comparison of the costs shows the feasibility of the proposed scheme in practical applications.

Keywords MMC-HVDC · Bypass arm · DC fault · Fault isolation

1 Introduction

With the scarcity of the traditional energy, high voltage direct current transmission based on a modular multilevel converter (MMC-HVDC) is an effective method to solve the problems associated with the grid connection of new energy [1, 2]. The MMC has advantages when compared to the two-level voltage source converter (VSC). These advantages include no commutation failure, scalability (scalable to different power and voltage levels), and low harmonic distortion [3]. Therefore, the MMC-HVDC has become a power transmission with broad application prospects [4, 5].

However, DC faults are inevitable during the long-term operation of MMC-HVDC systems [6]. When a DC fault occurs, MMCs based on half-bridge submodules (HBSMs) are seriously threatened by the freewheeling diodes, especially for pole-to-pole DC faults [7]. Short-circuit fault current does not naturally decay due to the freewheeling effect of diodes [8]. If there is no protection scheme, the power devices of the half-bridge MMC (HB-MMC) may be severely damaged. Therefore, it is necessary to take measures to quickly isolate DC faults [9].

For two-terminal systems, a DC fault can be cleared by tripping an AC circuit breaker (ACCB). However, ACCBs take a long time to isolate DC faults [10, 11]. Another scheme for the DC fault isolation uses modified MMC topologies, such as the full-bridge sub-module (FBSM), the clamp double sub-module (CDSM), etc. [12, 13]. However, the FBSM requires twice as many power devices, which results in a very high initial investment. Although the CDSM and the hybrid MMC reduce the number of power devices when compared to the FBSM, this topology increases the control complexity [14-15]. Although the control in [16] is not complicated, its cost is high due to the use of expensive IGBTs. In [17], a double-thyristor switch scheme (DTSS) eliminates the uncontrolled rectification effect of the freewheeling diodes, which causes the fault current to attenuate naturally. However, the freewheeling diodes share the fault current with the thyristors so that the diode is easily damaged. In addition, the process of embedding a double-thyristor into each sub-module is a complex project. There is a scheme that is equivalent to the isolation of the AC and DC side current paths after the protection action, and the isolation time of the DC fault current is related to the fault conditions [18]. Under extreme conditions, the isolation time can take hundreds of milliseconds, which is extremely unfavorable to the power devices of the sub-modules and the AC side. Based on the pros and cons of the above two schemes, a centralized configuration of back-to-back thyristors on the AC side

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(BBTS) scheme was proposed in [19]. However, the fault isolation time is still not ideal.

The above methods are all for two-terminal systems, and they are not considered for DC grids. In the DC grid, the DCCBs on both sides of the DC line are usually used to isolate DC line faults [20]. In [21], a DC fault isolation scheme combining the DCCB and the MMC was proposed. The fault current in the DC circuit can be quickly cut off by the DCCB. Therefore, the DC circuit breaker (DCCB) is ideal for DC protection [22]. However, there is no DCCB at the outlet of the converter due to cost considerations, as is the case with the Zhangbei DC grid. However, the converter still needs to isolate DC faults to deal with a number of conditions [23]. 1) When DC line1 fails, as shown in Fig. 1(a), DCCB1 and DCCB3 should operate together, but DCCB1 of DC line1 cannot operate normally. At this time, DCCB3 cooperates with the backup protection composed of DCCB2 and the converter. 2) When a fault occurs at the outlet of the converter, as shown in Fig. 1(b), DCCB1 and DCCB2 operate together, and the converter should provide protection. Therefore, the fault isolation capability of the converter is essential bot for the two-terminal systems and for DC grids [24]. A bypass arm protection scheme can provide protection for the converter, and it uses a few power devices to rapidly achieve the DC faults isolation. This protection is suitable for MMC-HVDC based overhead lines [25, 26].

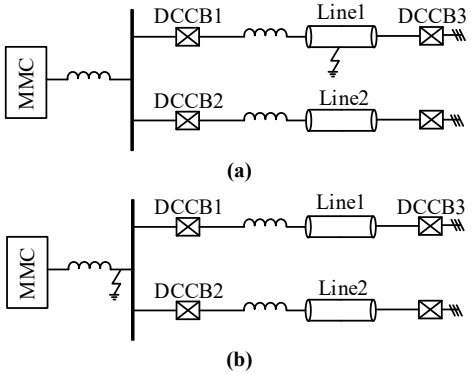


Fig. 1 Two DC faults conditions of a DC grid: **a** the DCCB of a DC line cannot operate normally when that DC line fails; **b** a fault occurs at the outlet of the converter

A bypass arm based DC fault isolation scheme for MMC-HVDC systems is proposed in this paper. The main contributions of this paper are as follows.

1) This scheme can quickly achieve DC fault isolation, which improves the capability of the system and does not increase the steady-state operation loss of the system.

2) This scheme greatly reduces the long-term impact of DC faults on the AC-side, and it is conducive to maintaining the stable operation of the AC-side during DC faults. The advantages in reducing the impact on the AC-side is more significant, which reduces the requirement in terms of the action time of the DCCB.

3) In terms of cost, this scheme reduces the control complexity and is easy to implement. Users can easily modify existing MMC-HVDC projects based on HBSMs.

4) Many of the existing schemes are for two-terminal systems. However, this scheme is suitable for both two-terminal systems and the DC grid, especially for faults at the converter outlet of the DC grid. The fault isolation capability of the converter is critical to the DC grid.

The remainder of this paper is organized as follows. Section II introduces the principles of the proposed scheme, including how to designs the reactance of the SZCL and how to isolate DC fault current. Section III deduces the expressions of the DC current and the AC current with equivalent circuits. In Section IV, simulation results using PSCAD/EMTDC show the superiority of the proposed scheme when compared with other schemes, and a cost comparison shows the feasibility of the proposed scheme in practical application. Finally, Section V presents the conclusion of this paper.

2 Bypass arm protection scheme

2.1 Bypass arm protection principle

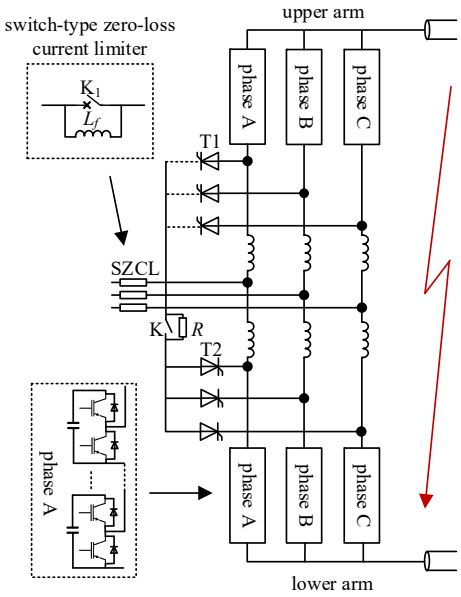


Fig. 2 MMC structure with a bypass arm.

When a DC fault occurs on the MMC-HVDC system based on HBSM, the protection must quickly isolate the DC fault, especially pole-to-pole DC faults. Therefore, this paper takes the pole-to-pole DC fault as an example for DC fault isolation. A bypass arm composed of bypass thyristors in series is arranged between the upper and lower arms on each phase of the converter, as depicted in Fig. 2, where K_1

is a vacuum circuit breaker (VCB), L_f is the reactance of the SZCL, K is a mechanical switch and R is a current limiting resistor. The SZCL has been successfully tested at the Ningxia grid. Under normal operation, the bypass thyristors are kept in an off-state condition; K is closed and the bypass arm is inoperative; and K_1 is closed and L_f is bypassed. As soon as fault current is detected, the bypass thyristors are switched on to force the fault current to flow through them, and K_1 is tripped to divert the current to L_f. K is turned on after the DC fault current is cleared for a while, and the current flows through the current limiting resistor. The current flowing through the thyristor is less than the holding current (R can be set to a larger value within the allowable range).

2.2 L_f design

L_f is selected so that the steady-state short-circuit current after current limiting is equal to or close to the steady-state rated current of the system. L_f prevents the AC system from excessive disturbances during fault clearing. It should be noted that a larger L_f causes a faster current attenuation. However, if L_f is too large, the cost increases too much, so the value of L_f needs to be reasonably designed. Since L_f does not affect the start-up of the transformer, the SZCL is placed on the valve side of the transformer.

It is assumed that the AC side line voltage is U_1, and the active and reactive power of the AC side are P and Q, respectively. To reduce the reactive power loss during normal operation of the system, the MMC generally requires that $P \neq 0$ and $Q \approx 0$. The effective value of the steady-state rated current of the system I_r is as follows:

$$I_r = \frac{P}{\sqrt{3}U_1} \tag{1}$$

After K_1 is tripped to divert the current to L_f, the steady-state short-circuit current I_f can be calculated as:

$$I_f = \frac{U_1}{\sqrt{3}\sqrt{R_s^2 + \omega^2(L_s + L_T + k^2 L_f)^2}} \tag{2}$$

where R_s +jL_s is the equivalent impedance of the AC side, L_T is the transformer leakage reactance, and k is the three-phase transformer ratio.

Through (1) and (2), the short-circuit current index ρ is:

$$\rho = \frac{I_f}{I_r} \tag{3}$$

By the above equations, L_f can be expressed as:

$$L_f = \frac{\sqrt{\left(\frac{U_1^2}{\rho P}\right)^2 - R_s^2}}{\omega k^2} - \frac{L_s + L_T}{k^2} \tag{4}$$

By specifying the short-circuit current index ρ (its value is approximately 1) and consulting Table 1, L_f=0.3H can be obtained.

Fig. 3 shows the AC-grid current at different values of L_f. It can be seen that L_f =0.3H is the most economical and effective value.

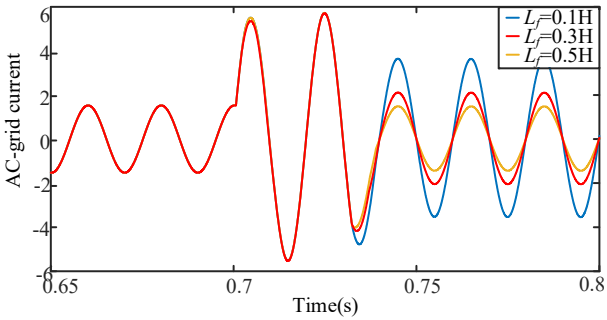


Fig. 3 AC-grid current under different values of L_f

2.3 DC fault isolation steps

Fig. 4 illustrates the current flow path of one phase after a DC fault occurs. The bridge arm inductance of each phase has two discharge paths. One is to discharge through the sub-module diode and the short circuit point on the DC side, as shown in the dotted line of Fig. 4, and the other is to discharge through the bypass thyristors, as shown in the solid line of Fig. 4.

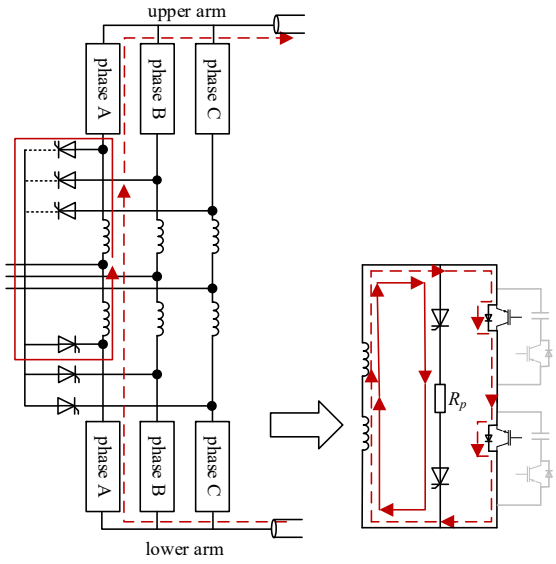


Fig. 4 Equivalent discharge path of a single-phase bridge arm after a DC fault occurs

Using the bypass arm topology to isolate a DC fault can be divided into 4 steps, and the corresponding actions at each moment are as follows.

t_0: DC fault occurs. The interval t_0~t_1 is the time for DC fault detection and recognition.

t_1: The DC fault is detected. Within about 1ms, the MMC is blocked and the bypass arm is turned on. Most of the current of the bridge arm inductance flows through the bypass bridge arm, and the fault current flowing through the sub-module devices is reduced.

t_2 (for the DC gird only, this step can be ignored if it is a two-terminal systems): The DCCB is tripped. When a fault like the one in Fig. 1(a) occurs, DCCB1 cannot act normally. At this time, DCCB2 cooperates with the converter to operate normally. When a fault of Fig. 1(b) occurs, DCCB1 and DCCB2 cooperate with the converter to operate normally.

t_3: K_1 is tripped and the current flows through L_f. K_1 is a mechanical switch and the bypass bridge thyristors are the power electronic devices. Thus, their action times are different. K_1 is considered according to the time of a traditional circuit breaker, and the action time is T_{trip}=30ms. The bridge arm inductance continues to discharge through the bypass arm and the sub-module.

t_4: The fault current at the DC side decays to 0. After the DC fault current is cleared for a while, K is turned on and the current flows through the current limiting resistor. The current flowing through the thyristor is less than the maintenance current.

A DC fault isolation flowchart is shown in Fig. 5.

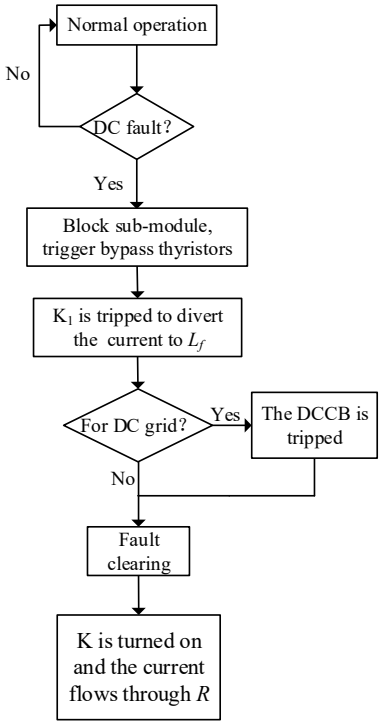
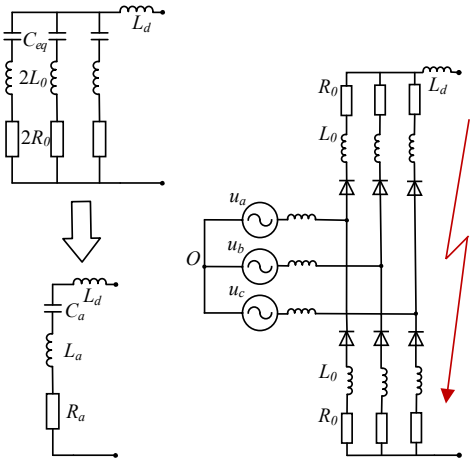


Fig. 5 DC fault isolation flowchart

3 Characteristics analysis

3.1 DC fault transient characteristics

When a DC fault occurs in a bipolar MMC-HVDC, the fault transient process can be divided into the capacitance discharge stage and the uncontrolled rectifier stage. In the first stage, the equivalent circuit of the MMC is shown in Fig. 6(a). The MMC can be equivalent to an RLC series circuit. The DC fault current provided by the submodule capacitor rises rapidly and the MMC can block it in about 1ms. When this stage is completed, the freewheeling diodes in the converter act as an uncontrolled rectifier even if all the IGBTs are turned off, which allows the AC side power supply to provide current to the DC circuit. The equivalent circuit is shown in Fig. 6(b). Therefore, if there is no protection scheme at this time, the DC fault cannot be automatically cleared. In these figures, L_d is the sum of the DC line smoothing reactor and the outlet of the converter smoothing reactor. In addition, R_0 and L_0 are the bridge arm resistance and inductance, respectively. R_a =$2R_0/3$, L_a =$2L_0/3$, and C_a =$6C_{eq}/N$. Furthermore, C_{eq} is the capacitance of the MMC submodule, and N is the number of sub-modules of each phase of the MMC.



(a) (b)

Fig. 6 Equivalent circuit diagrams of a MMC after a DC fault: **a** capacitor discharging stage, **b** uncontrolled rectifier stage

3.2 Equivalent circuit current expressions

Through the above analysis, an equivalent circuit diagram of the DC side when the protection is put into operation after a fault occurs can be obtained. In addition, the direction of each current flow is marked, as shown in Fig. 7. Here R_p=0.012 Ω represents the equivalent internal resistance of all upper and lower bypass arm thyristors (it is known that the internal resistance of all the bridge arm thyristors is 0.01 Ω). R_c and L_c are the resistance and inductance of the DC fault current path, respectively. R_d is used to denote the DC-link resistance of the DC fault current path and R_{sc} is used to denote the DC-link short-circuit resistance. Then, R_c is the sum of R_d and R_{sc}.

In Fig. 7, the impedance of the bypass bridge arm is far less than that of the MMC loop. Therefore, the current almost flows into the bypass arm and the AC side feeds power to the bypass arm. Therefore, the DC side current decays to 0.

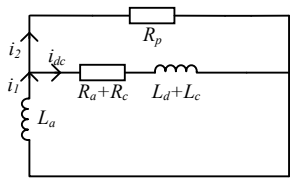


Fig. 7 DC equivalent circuit diagram

For the DC side, the mathematical model can be described by the following equations:

$$i_2(t)=\frac{1}{R_p}[(L_d+L_c)\frac{di_{dc}(t)}{dt}+(R_a+R_c)i_{dc}(t)] \quad (5)$$

$$i_1(t)=i_2(t)+i_{dc}(t) \quad (6)$$

Substituting (5) into (6), $i_1(t)$ can be expressed as:

$$i_1(t)=\frac{L_d+L_c}{R_p}\cdot\frac{di_{dc}(t)}{dt}+\frac{R_a+R_c+R_p}{R_p}i_{dc}(t) \quad (7)$$

The voltage relationship can be obtained by:

$$L_a\frac{di_1(t)}{dt}=-[(R_a+R_c)i_{dc}(t)+(L_d+L_c)\frac{di_{dc}(t)}{dt}] \quad (8)$$

Substituting (7) into (8), the equation can be obtained as:

$$\frac{L_a(L_d+L_c)}{R_p}\cdot\frac{d^2i_{dc}(t)}{dt^2}+\frac{(R_a+R_c+R_p)L_a+(L_d+L_c)R_p}{R_p}\cdot\frac{di_{dc}(t)}{dt} \quad (9)$$
$$+(R_a+R_c)i_{dc}(t)=0$$

Equation (9) can be expressed as:

$$\frac{d^2i_{dc}(t)}{dt^2}+\frac{(R_a+R_c+R_p)L_a+(L_d+L_c)R_p}{L_a(L_d+L_c)}\cdot\frac{di_{dc}(t)}{dt} \quad (10)$$
$$+\frac{(R_a+R_c)R_p}{L_a(L_d+L_c)}i_{dc}(t)=0$$

Similarly, assuming $i_{dc}(t_1)=I_0$, $i_{dc}(t)$ can be expressed as

$$i_{dc}(t)=I_0e^{-(t-t_1/\tau)} \quad (11)$$

where the time constant $\tau=L_a(L_d+L_c)/[(R_a+R_c+R_p)L_a+(L_d+L_c)R_p]$.

Consulting Table 1, R_a=2 Ω, L_a=0.057 H, L_c=0.055 H and L_d=0.02 H. When a pole-to-pole metal DC fault occurs at 50 km of the DC line, the DC-link resistance of the DC fault current path R_d is 1.603Ω and the DC-link short-circuit resistance R_{sc} is 10 Ω. Then, R_c is 11.603 Ω. A comparison between the calculated and simulation values in this case is shown in Fig. 8(a).

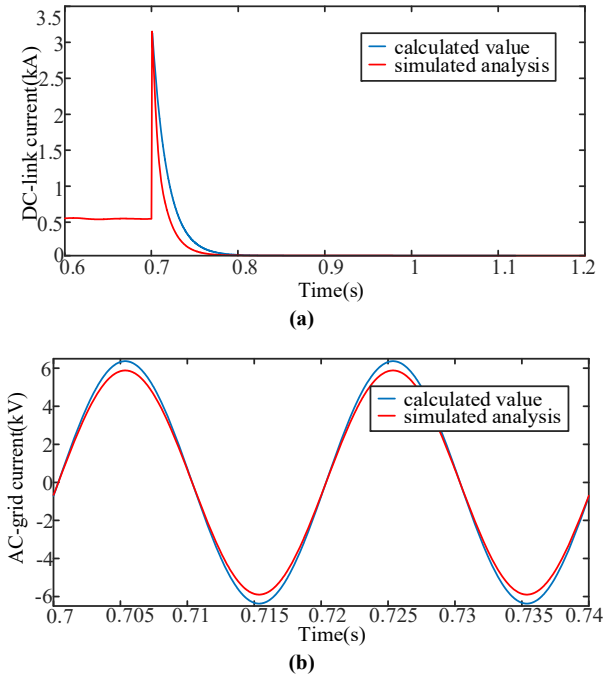


Fig. 8 Comparison between the calculated and simulation values **a** DC-link current; **b** AC-grid current

For the AC side, the current of the AC side almost flows into the bypass arm (so only the bypass arm is considered). The three-phase bridge arm is equivalent to forming a three-phase short circuit, as shown in Fig. 9.

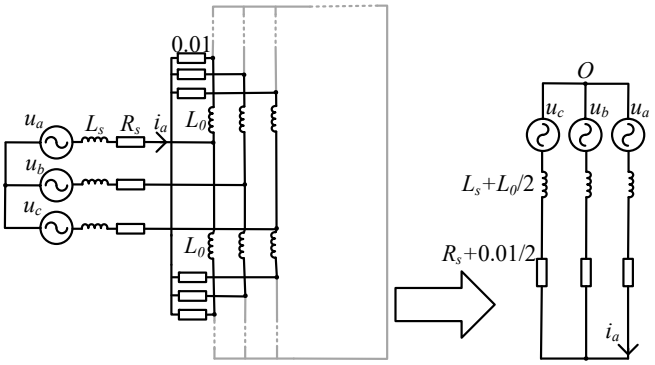


Fig. 9 AC equivalent circuit diagram

The equivalent circuit can be described by the following equations:

$$\dot{U}_a-\dot{U}_b=212\angle0°-212\angle-120°=366.73\angle30° \quad (12)$$

$$\dot{U}_a-\dot{U}_c=212\angle0°-212\angle-240°=366.73\angle-30° \quad (13)$$

$$\dot{I}_a=\frac{\dot{U}_a-\dot{U}_b}{(R_s+0.01/2)+j\omega(L_s+L_f+1/2L_0)}$$
$$+\frac{\dot{U}_a-\dot{U}_c}{(R_s+0.01/2)+j\omega(L_s+L_f+1/2L_0)}=I\angle\theta \quad (14)$$

where L_f=0.3 H, R_s +jL_s is the equivalent impedance of the AC side, and L_0 is the inductance of the bridge arm.

Substituting (12) and (13) into (14), I and θ can be obtained as I=4.5 and θ=-90°.

Then i_a can be obtained as:

$$i_a=\sqrt{2}I\cos(\omega t+\theta)$$
$$=\sqrt{2}\times4.5\cos(314t-90°) \quad (15)$$

Consulting Table 1, a comparison between the calculated and simulation values is shown in Fig. 8(b).

The reasons for some of the differences between Fig. 8(a) and Fig. 8(b) are given below.

1) The impedance of the bypass bridge arm is far less than that in the MMC loop, which causes the current of the AC side to almost flow into the bypass bridge arm. However, there is still little current flowing into the DC side, and it is ignored in mathematical analysis.

2) There is the difference between the actual value and the calculated value of the time constant τ.

3) For the simulation model, the set sampling frequency leads to a difference between the mathematical calculation and the simulation.

4 Comparation analysis

4.1 Simulation results

This section compares the proposed scheme to other schemes in terms of the DC current isolation rate, the impact of the AC-grid, and the thyristor current. A two-terminal MMC-HVDC system and a DC grid were constructed in PSCAD/EMTDC as shown in Fig. 10. For the DC grid, fault 1 represents a pole-to-pole DC fault on the line; fault 2 represents a pole-to-pole DC fault at the

outlet of the converter. The relevant parameters are shown in Table 1.

Table 1 Simulation system parameters

Parameters	Value
AC side phase voltage	212kV
Equivalent impedance of AC side	1.771+j0.107Ω
Rated capacity of the MMC-HVDC system	900MVA
Three-phase transformer ratio	1:1
Transformer leakage reactance	0.15 pu
Active power of the AC side	700 MW
Number of submodules in the bridge arm	400pc
Voltage at DC side	640kV(±320kV)
Total submodule capacitance	29.3μF
Inductance of bridge arm	84.79mH
Outlet of the converter smoothing reactor	0.02H
DC line smoothing reactor smoothing reactor	0.2H
Overhead line length	100km
Overhead link resistance	0.03206ohm/km
Overhead link inductance	1.1mH/km
Current limiting resistor	50Ω

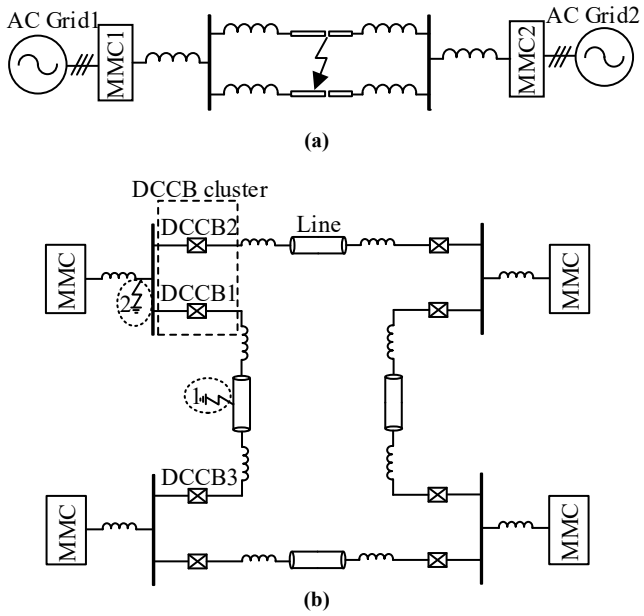


Fig. 10 Simulation models: **a** two-terminal MMC-HVDC system, **b** DC grid

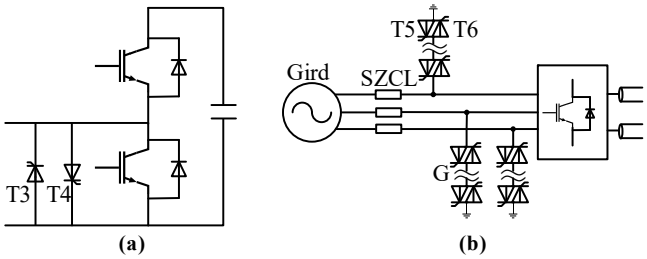


Fig. 11 Existing schemes: **a** DTSS; **b** BBTS

To eliminate the uncontrolled rectification effect of diodes, scholars proposed a double-thyristor switch scheme (DTSS), as shown in Fig. 11(a) [17]. Another group of scholars proposed a scheme of a centralized configuration of back-to-back thyristors on the AC side (BBTS) to solve the adverse effect of the slow DC current attenuation of the DTSS on a system under severe fault conditions, as shown in Fig. 11(b), where SZCL is the switch-type zero-loss current limiter, and G is a series of double thyristors [19].

The three different protection schemes (DTSS, BBTS, proposed scheme) are tested on three occasions. For the two-terminal MMC-HVDC system, a pole-to-pole DC fault occurs at t=0.7 s. The MMC is blocked at t=0.70065 s, and the bypass thyristors are switched on at the same time. K_1 is tripped and the current flows through L_f at t=0.73 s. The DC-link short-circuit resistance R_{sc} is set to 10Ω. Fig. 13(a) shows a comparison of DC current waveforms from the three schemes when a fault occurs at 50km of the DC line. It can be seen that the proposed scheme isolates the DC fault faster than the other two schemes. Pole-to-pole metal DC faults located 25, 50, and 100 km away from the rectifier station are simulated at t = 0.7 s. Fig. 13(b) shows that when the distance to the rectifier is closer, the peak value of the fault current is larger and the fault isolation time is shorter. If the system is restarted after the fault is cleared, K_1 is closed to cut off the current limiting reactor L_f. K_1 is still considered to be the traditional circuit breaker. Thus, T_{close}=50ms. The latency time before the converter is unlocked should be greater than T_{close}. The special control strategy can be used to improve the dynamic performance of the MMC during system restart. However, this is not the focus of this paper. However, it will be considered in a future study. Waveforms of the DC current and AC current are shown in Fig.12.

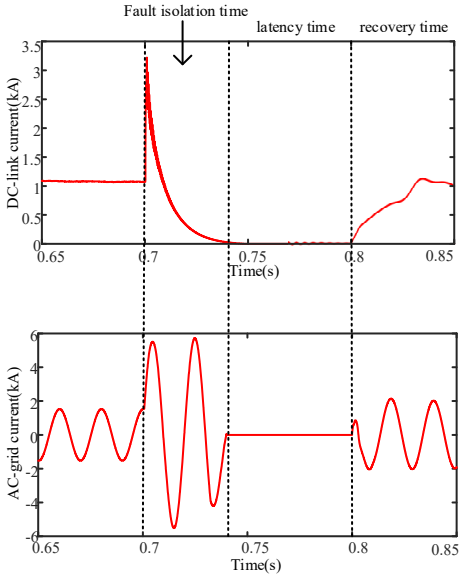


Fig. 12 Simulation results of fault isolation and system restart

For the DC grid, pole-to-pole DC faults located 0, 25, 50, and 100 km away from the rectifier station are simulated at t = 0.7 s. The MMC is blocked at t=0.70065 s, and the bypass thyristors are switched on at the same time. When fault 1 occurs, as shown in Fig. 10(b), the DC-link short-circuit resistance R_{sc} is set to 10 Ω. DCCB1 and DCCB3

should work together, but DCCB1 of DC line1 cannot work normally. At this time, DCCB3 cooperates with the backup protection composed of DCCB2 and the converter. DCCB2 and DCCB3 are tripped at t=0.705 s. K_1 is tripped, and the current flows through L_f at t=0.73 s. Fig.13(e) shows a comparison of DC current waveforms from the three schemes when a fault occurs at 50km of the DC line. It can be seen that the proposed scheme isolates the DC fault faster than the other two schemes. Pole-to-pole DC faults located 25, 50, and 100 km away from the rectifier station are simulated at t = 0.7 s. Fig. 13(f) illustrate that when the distance to the rectifier is closer, the peak value of the fault current is larger and the fault isolation time is shorter.

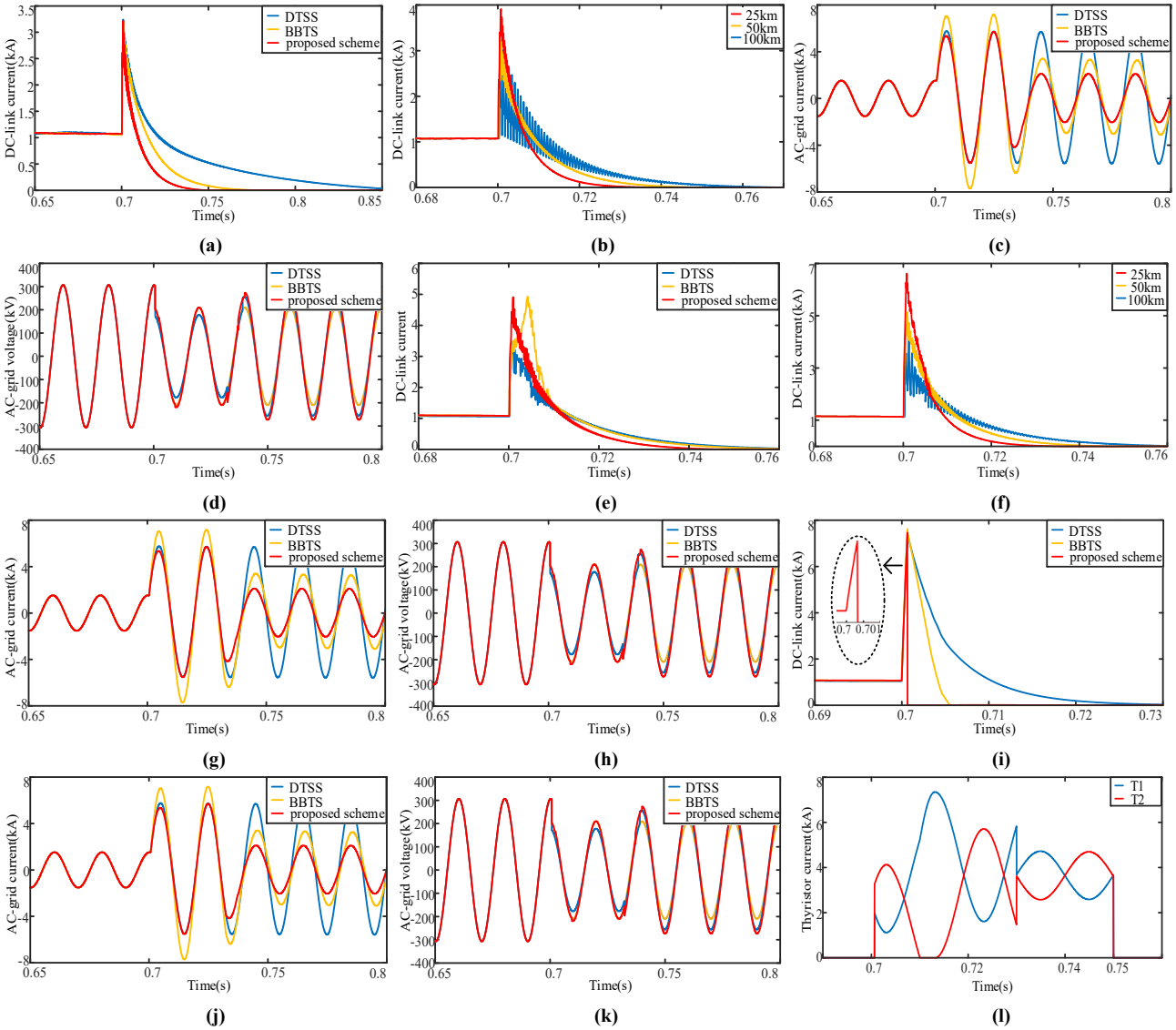


Fig. 13 Simulation results for different schemes: **a** DC-link current of a two-terminal system; **b** two-terminal system DC-link current at different distances; **c** and **d** AC-grid current and voltage of a two-terminal system; **e** DC-link current of a DC grid under fault 1; **f** DC grid under fault 1 DC-link current at different distances; **g** and **h** AC-grid current and voltage of a DC grid under fault 1; **i** DC-link current of a DC grid under fault 2; **j** and **k** AC-grid current and voltage of a DC grid under fault 2; **l** thyristor current for a DC grid under fault 2.

When fault 2 occurs, as shown in Fig. 10(b), the DC-link short-circuit resistance R_{sc} is set to 0 Ω. DCCB1 and DCCB2 cooperate with the converter to operate normally. The MMC is blocked at t=0.70065 s, and the bypass thyristors are switched on at the same time. The DCCB1 and DCCB2 are tripped at t=0.705 s. K_1 is tripped, and the current flows through L_f at t=0.73 s. Fig. 13(i) shows a comparison of DC current waveforms of the three schemes when a fault occurs at the outlet of the converter. The thyristor currents for DC grid fault 2 are as shown in Fig. 13(l). As expected, the thyristor current of the proposed scheme is higher than that of DTSS because the proposed

scheme carries almost the full current and does not share current with diodes as in the DTSS. After K is turned on and the current limiting resistor is connected to the bypass arm, the thyristors are turned off after the thyristor current drops below the maintenance current to prepare the system to resume normal operation.

Fig. 13(c), Fig. 13(g) and Fig. 13(j) show that the AC-grid current of the proposed scheme and the BBTS decrease, and that the DTSS maintains a larger AC-gird current. Fig. 13(d), Fig. 13(h) and Fig. 13(k) show that the proposed scheme and the BBTS can return to a normal AC-gird voltage but the DTSS maintains a lower voltage. Due to the design of a reasonable current-limiting reactor L_f, the AC-grid only needs to withstand the voltage reduction and three-phase short-circuit current in T_{trip}. The advantages of the proposed scheme in reducing the impact on the AC-grid is more significant, which also reduces the requirement for the action time of the DCCB.

4.2 Cost analysis

The cost of a converter station includes both the construction cost and the operation cost. The bypass bridge arm barely flows current under steady state conditions. Therefore, the operating loss of the proposed scheme is the same as that of the classic HB-MMC. Thus, this part only considers the construction cost.

To verify the engineering feasibility of this isolation scheme, its additional costs are compared with the DTSS and the BBTS under the same voltage levels. Because the voltage of the bridge arm inductance U_{L0} is very small when compared to the AC voltage U and the DC voltage U_{dc}, U_{L0} can be ignored in this part. Here, U=212kV and U_{dc}=640kV(±320kV).

For the DTSS, the number of upper and lower bridge arm sub-modules of each phase is N. Since each sub-module is added with double thyristors, the number of thyristors for each phase is $2N$. The voltage that each of the phase thyristors need to withstand is U_{dc}.

It is assumed that the number of thyristors required for each phase of the proposed scheme is x, and the number of thyristors required for each phase of scheme 2 is y.

For the proposed scheme, the upper and lower thyristors of phase A are connected to a node. The upper thyristors of phase A withstand the negative value of the phase voltage of phase A $-U$ and the lower thyristors of phase A withstand the phase voltage of phase A U. For the BBTS, the back-to-back thyristors of phase A withstand the phase voltage of phase A U. Because DC voltage and AC voltage cannot be directly compared, the modulation ratio m is introduced and the modulation amplitude is U_m=320m. Usually, the modulation ratio m < 1 and between 0.7~0.9.

The ratios of the voltage levels and the numbers are:

$$\frac{2U_m}{U_{dc}} = \frac{x}{2N} \tag{16}$$

$$\frac{U_m}{U_{dc}} = \frac{y/2}{2N} \tag{17}$$

Solving the above formulas yields:

$$x=(1.4N\sim1.8N) \tag{18}$$

$$y=(1.4N\sim1.8N) \tag{19}$$

Actually, the bridge arm reactance shares a small voltage with the thyristor in the proposed scheme, which causes the voltage of the thyristors to be less than the calculated value. Therefore, the actual number of thyristors is < (1.4N~1.8N).

Comparison results are listed in Table 2. The cost of the thyristor in the proposed scheme is less than that in the DTSS and the BBTS. Although a SZCL is not used in the DTSS, greater losses are caused if the AC side devices are damaged due to overcurrent. In addition, the fault clearing speed of the proposed scheme is obviously better than that of the other two schemes. Therefore, the proposed scheme is an ideal fault isolation scheme.

Table 2 Cost comparison

Type	Numbers of SZCL	Numbers of thyristor
DTSS	/	2N
BBTS	3	1.4N~1.8N
Proposed scheme	3	<(1.4N~1.8N)

5 Conclusion

For DC grids, DCCBs are not added at the outlet of the converter due to cost considerations, as is the case with the Zhangbei DC grid. When a fault occurs on the line, the proposed scheme and the adjacent DCCB can be used as backup protection in case the DCCB on the line cannot operate normally. When a fault occurs at the outlet of the converter, the proposed scheme can cooperate with the line DCCBs to isolate the DC fault together. For a simple two-terminal system, the proposed scheme is also applicable. A theoretical analysis and simulation results show that the proposed scheme has a number of advantages.

1) A comparation analysis confirms that this scheme can quickly achieve DC fault isolation with less cost in terms of the system and does not increase the steady-state operation loss of the system. Users can easily modify existing MMC-HVDC projects based on HBSM.

2) The proposed scheme greatly reduces the long-term impact of DC faults on the AC-side, and it is conducive to maintaining the stable operation of the AC-side after the a DC fault. The advantages in reducing the impact on the AC-side is more significant, since it also reduces the requirement for the action time of the DCCB.

3) The proposed scheme is suitable for two-terminal systems and for DC grids, especially for faults at the converter outlet of the DC grid. The fault isolation capability of the converter is critical to DC grids.

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