A Fault Protection Strategy Based on Z-Source Solid State Circuit Breaker for More Electric Aircraft

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***Abstract*—High-voltage direct-current (HVDC) rated at 270 Vdc is one of the main power supply technologies expected for future more electric aircraft (MEA). However, dc protection is still one major challenge preventing the wide deployment of HVDC. To overcome this, Z-source solid-state circuit breakers (Z-SSCBs) could be employed due to their simple structure and fast speed of response. However, Z-SSCBs alone cannot effectively isolate a short-circuit fault when a large fault resistance and a small fault current ramp rate are present, which would greatly damage MEA. In this paper, an auxiliary protection strategy based on Z-SSCBs is presented to address this problem. The strategy combines inverse-time overcurrent and voltage protection to force the opening of the Z-SSCB when its automatic triggering fails. The principle of operation of a Z-SSCB is discussed, and the design process of the protection strategy is presented in detail. Software simulations using Saber and experimental tests have been carried out to validate the protection strategy. Both sets of results match well, offering a good performance and meeting IEEE protection (Std C37.112-2018) and aircraft electrical standards (MIL-STD-704F). It is shown that with the auxiliary protection strategy, the Z-SSCB successfully isolates faults against overcurrent, overvoltage and undervoltage operating conditions.**

***Index Terms*—Z-source solid-state circuit breaker, protection, more electric aircraft, power supply system of aircraft.**

I. INTRODUCTION

WITHIN the context of global warming, green aviation is an important development trend. More electric aircraft (MEA) and all electric aircraft are recognized as key solutions supporting this goal. To optimize the secondary energy design of an aircraft, its power supply system will be electrified to replace traditional pneumatic, hydraulic, and mechanical systems. This will significantly reduce the fuel consumption, weight, and volume of the aircraft, while at the same time will improve its reliability, maintainability, and ground support capability [1]-[2].

With the development of MEA technology and the wider use of airborne power electronics devices, it becomes more achievable to satisfy the increased requirements of overall power capacity and power quality of aircraft power supply systems. These systems have gradually evolved from constant to variable frequency ac and to HVDC [3]. Compared to an ac system, a dc system can further improve system efficiency and reduce its volume and weight.

An HVDC power supply system for MEA uses several power components, and the network impedance is small. For a low impedance short-circuit fault, the rate of current rise is large and the amplitude of fault current significant. This could cause catastrophic damage to the aircraft if the fault is not removed quickly. Therefore, dc protection is one of the main challenges faced by an HVDC power supply system.

The basic process of dc protection is to detect, assess, and classify a dc fault and then transmit a signal to protective equipment to block it (e.g. circuit breakers, CBs). Research mainly focuses on three aspects: fault detection and location, fault current limiting devices, and fault isolation devices [4]. Fault detection is required for successfully isolating the fault [5]. Various fault detection and location algorithms based on current, voltage or current variation have been proposed to isolate faults [6]-[9]. Most algorithms achieve this by detecting undervoltage, overcurrent or high rate of change of current. Fault current limiting devices may limit the ramp rate of a fault current before the fault is fully isolated. They are often used alongside CBs and mainly include a reactor, a resistive current limiter, and a superconducting current limiter [10].

The first security measure for aircraft was in the form of fuses. However, fuses only offered temporary protection when the rated current was exceeded [11], and they would take seconds to minutes to disconnect depending on the magnitude of the fault current. Since the nineteenth century, mechanical CBs have been in operation. They can be reset manually or automatically. Nonetheless, while cutting off the fault current, mechanical CBs are prone to arcing, which can reduce their lifespan [12]. SSCBs that use power electronic components (such as thyristors and IGBTs) have recently received significant attention. These devices exhibit quicker response times and provide the ability to achieve arc-free interruption. Particularly, thyristor-based Z-SSCB have gained an increased popularity. In general, Z-SSCBs can achieve automatic interruption and isolation of short-circuit fault currents without the need for additional fault detection circuitry due to the fast-rising characteristics of dc short-circuit fault currents and the semi-controlled characteristics of thyristors. Therefore, it may be possible to protect the dc power systems in MEA using Z-SSCBs [13]. Unidirectional [14]-[16] and bidirectional [17]-[19] Z-SSCB topologies have been proposed to this end.

The main components of a mechanical CB are the

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mechanical switch and the arc extinguishing systems. A hybrid CB mainly consists of a bypass branch based on a load commutation switch and a mechanical switch, an energy absorption branch, as well as the main breaker (composed of a string of power electronics switches). In comparison, a Z-SSCB consists mainly of power electronic components such as thyristors and diodes without incorporating mechanical switches. As the weight and volume of the mechanical and hybrid CBs are mainly determined by the weight and size of the mechanical switches and inductors [20], the Z-SSCB will be much smaller and lighter at a similar voltage level than a mechanical or a hybrid CB containing mechanical switches.

The main disadvantage of a Z-SSCB is that it can interrupt and isolate a short-circuit fault only when conditions for a minimum fault current ramp rate and maximum fault resistance are met [16]—in other words, automatic triggering of the Z-SSCB does not occur for high impedance faults, potentially leaving an MEA exposed. Despite this, existing research mainly focuses on specific topologies [21], while strategies to address the main disadvantage of a Z-SSCB have yet to be developed.

To address this shortcoming, an auxiliary protection strategy specifically designed for Z-SSCBs is presented in this paper. For completeness, software simulation tests using Saber and experimental validation using a scaled-down experimental testbed have been conducted to verify it. Three major contributions are made in this paper. Firstly, a newly developed protection strategy that fully considers the topology and parameters of the presented Z-SSCBs to integrate the protecting actions is proposed. This results in a protection scheme against faults with a significantly wider range of fault impedance and current ramp rate compared to conventional Z-SSCBs. Secondly, the working principle of the protection strategy was developed to fully consider practical application scenarios of Z-SSCBs in the field of MEA. Thirdly, extra functions including the protection against pre-commissioning faults and current blocking at the load side with a power supply have been added, resulting in four different versions of Z-SSCB devices (which have their own advantages in cost, efficiency and reliability). This provides additional flexibility in availability for practical applications. At the same time, it leads to system restoration after the fault is removed to ensure the normal operation of the system. Moreover, the strategy still has the characteristics of a fast response, small size and light weight.

II. Working Principle of the Z-SSCB

Despite the different available topologies, most Z-SSCBs share a similar working principle [22]. To facilitate the discussion, the bidirectional topology in [23] is used to explain it. The topology is shown in Fig. 1, which uses two transformers and two thyristors to ensure bidirectional protection of the system. This is a simple structure with low conduction loss. The coupled inductor L_1 and the thyristor SCR_1 constitute the main circuit when power in the bidirectional CB flows forward, and L_2 and SCR_2 when power flows backwards.

As shown in Fig. 1(a), in the no-fault condition, the power supply transmits power to the load through the primary coil of

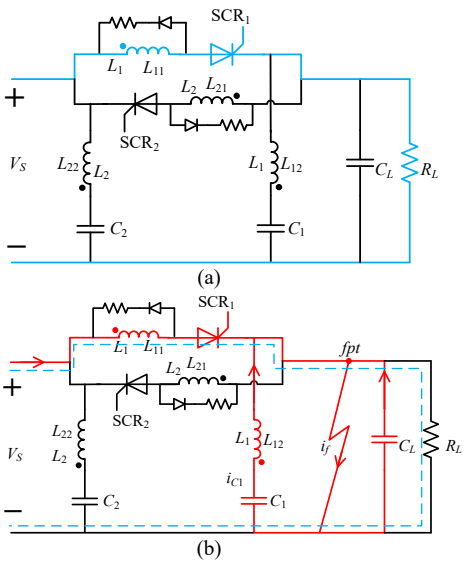


Fig. 1. Working principle of the Z-SSCB [23]: (a) no-fault condition, (b) occurrence of a short-circuit fault.

L_{11} and SCR_1. When a short-circuit fault occurs at the load side, the load capacitor C_L and capacitor C_1 of the Z-SSCB discharge at the same time to feed the fault current (see Fig. 1(b)). The discharge current i_{C1} flows to the fault point *fpt* through the secondary coil L_{12} of L_1. The induced current is opposite to the forward current of SCR_1, as shown in Fig. 1(b). Finally, the current of SCR_1 gradually drops to zero. As such, SCR_1 is turned off to interrupt and isolate the short-circuit fault automatically without the need for any relays or protection algorithms. However, as discussed earlier, automatic triggering of a Z-SSCB is only possible when the fault resistance is not greater than a maximum permissible value and the rate of rise of fault current is not less than a minimum threshold.

A. Maximum fault resistance

The fault resistance must not be greater than the maximum fault resistance $R_{f\ max}$, as given by

$$R_{f\max} \le \frac{C_1}{n(C_1+C_L)} R_L \qquad (1)$$

where n is the turns ratio of the coupled inductor, R_L is the load resistance, C_1 is the capacitance of the Z-SSCB and C_L is the capacitance of the load.

B. Minimum fault current ramp rate

Similarly, the current ramp rate shall not be less than the minimum fault current rise rate. In the event of a short-circuit fault, assuming the fault resistance changes linearly [24], the minimum fault current ramp rate K is obtained as:

$$K \ge n^2 \frac{1}{(R_L C_1)^2} e(C_1+C_L) \qquad (2)$$

where e is Euler's number (a mathematical constant). Since n remains unchanged, the value of K decreases with an increase of R_L and C_1 but it increases with an increase of C_L.

At the design stage, by knowing the required K and $R_{f\ max}$, the sizing of capacitances in the Z-SSCB may be achieved to meet the protection requirements defined by (1) and (2). However, when relevant parameters in the power supply

system of the MEA change (e.g. loads), K and $R_{f\,max}$ may change too, which may lead to the failure in triggering the Z-SSCB. This imposes a huge risk to the safety of the aircraft and, thus, a bespoke protection strategy is required to provide a much wider range of protection when short-circuit faults with larger resistance and lower current ramp rate occur.

C. Design considerations of the Z-SSCB

The main components of the Z-SSCB studied in this paper include a coupled inductor and a capacitor. The detailed design process for Z-SSCB component sizing is available in [23], but key calculations are here provided for completeness. The relationships between the coupled inductor and capacitor, as well as the turn ratio, are given as,

$$L_{11} \gg \frac{8}{81n} R_L^2 C_1 \tag{3}$$

$$L = \frac{0.4\pi N^2 A_c \times 10^{-8}}{l_g + \frac{MPL}{\mu_m}} \tag{4}$$

$$n > \frac{R_L}{R_{step}} - 1 \tag{5}$$

The weight of the inductor should be considered and an appropriate margin should be reserved in the inductor design to prevent saturation. However, the high-power rating of the thyristors can compensate for the adverse effect caused by the coupled inductor's weight on the power density of the CB. Z-SSCBs with coupled inductors have already been identified to be suitable for aircraft applications with higher power levels [13]. Thus, the Z-SSCB investigated in this paper may contribute to increasing the power density even further. Moreover, as solid-state transformers become more common in the near future, the weight and size of coupled inductors in CBs are expected to be reduced further [25].

D. Power loss analysis of Z-SSCBs

The on-state losses of MOSFETs increase with an increased current magnitude and, in general, silicon-based thyristors may exhibit lower on-state losses than MOSFETs at the same current level [13]. Thyristors are available in voltage ratings ranging from tens of volts to several thousand volts. For example, the voltage rating of the 2N6400 series thyristors manufactured by ON Semiconductor ranges from 50 V to 800 V [26]-[27]. At the same time, as HVDC power systems for MEA are developed, the capacity of aircraft power systems is expected to increase, raising the voltage levels up to 1 kV to 3 kV [28]. This can effectively increase the overall power transfer efficiency of the system while reducing the size and weight of the equipment. Thyristors are thus deemed appropriate for future HVDC systems of MEA.

The high on-state losses exhibited by SSCBs are still a main disadvantage, but as the voltage levels of MEA rise, CBs with an increased power rating will be used to withstand higher voltages and currents than unipolar devices [29]. The development of components such as wide-bandgap semiconductor devices will also reduce the on-state losses of the CBs.

In Z-SSCBs, on-state losses are primarily generated by inductors, thyristors, and diodes. Winding losses (copper losses) and core losses make up most of the inductive losses, while thyristor losses consider switching losses and conduction losses. However, switching losses are negligible. Diodes exhibit mainly power losses, which are primarily dissipated in the form of thermal energy.

TABLE I
ON-STATE LOSSES AND EFFICIENCY OF THE Z-SSCB

Current [A]	V_{source} [V]	V_{load} [V]	$V_{inductor}$ [V]	V_{semi} [V]	P_{loss} [W]	Efficiency [%]
1	6.37	4.75	0.055	1.476	1.62	74.568
2	11.95	9.59	0.110	1.541	4.72	82.744
3	16.80	14.47	0.165	1.548	7.23	85.723
4	21.79	19.29	0.211	1.535	10.0	88.527
5	26.58	23.98	0.237	1.584	13.0	90.218

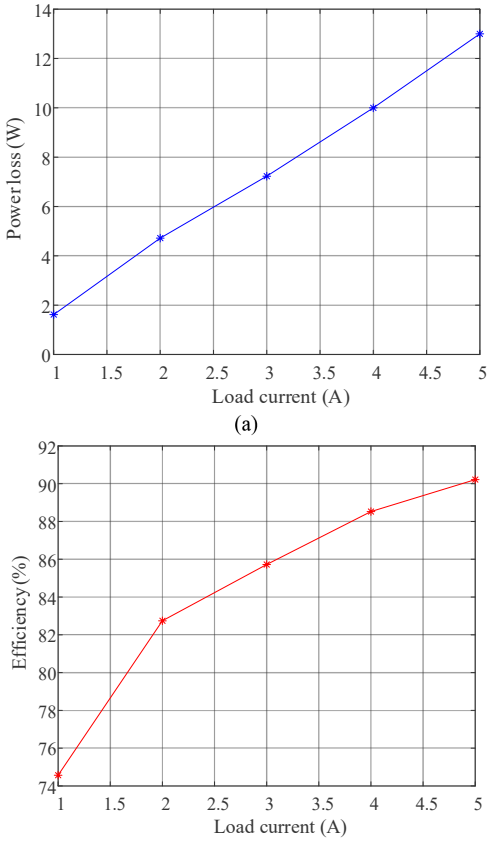


Fig. 2. (a) Power loss and (b) efficiency of the Z-SSCB at different current levels

The on-state losses of the Z-SSCB presented in this paper (see Fig. 1) have been quantified by measuring and calculating the energy losses and efficiency. This was done varying the current from 1 A to 5 A. To conduct this exercise, the parameters from Table VII in Section IV have been adopted. The results are shown in Table I and Fig. 2. In the table, V_{source} is the source voltage, V_{load} is the voltage across the load, $V_{inductor}$ is the voltage across the primary coil of the coupled inductor, and V_{semi} is the sum of the voltages across the thyristor and diode.

It can be seen from Fig. 2 that the power losses increase with an increasing load current. Similarly, the efficiency increases as the current increases. Thus, as the voltage levels of aircraft power systems continue to rise and capacity

requirements increase, thyristors can contribute to a higher power density of the power system.

E. Effect of the cable on the performance of the Z-SSCB

To further investigate the effect of the cable's impedance on the performance of the Z-SSCB, simulations have been conducted when the cable's inductance and resistance vary while the maximum fault resistance and minimum fault current ramp rate of the CB are maintained constant. A schematic diagram of the simulated system is shown in Fig. 3. The tested cable inductances and resistances are shown in Table II. Simulation results are presented in Fig. 4.

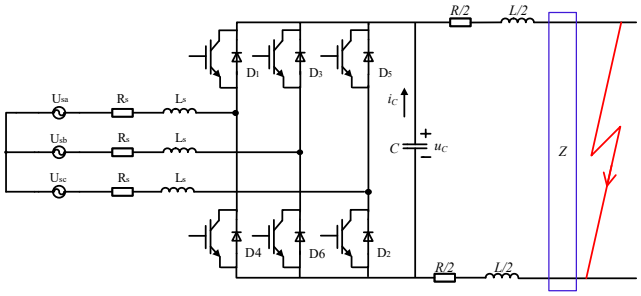


Fig. 3. The simulation schematic with a short cable

TABLE II
LINE'S INDUCTANCE AND RESISTANCE

L (mH)	0	0.2	0.4	0.6
R (Ω)	0	0.5	1	2

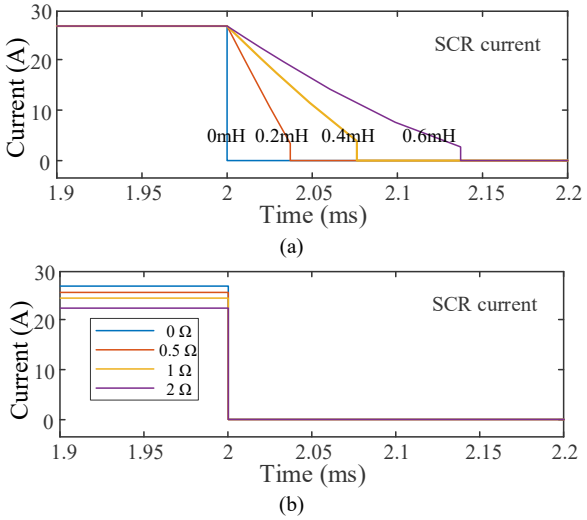


Fig. 4. Simulation results for varying line (a) inductance and (b) resistance.

From the simulation results shown in Fig. 4, the time it takes for the thyristor current to drop to zero increases as the inductance of the line increases. In contrast, increasing the resistance of the cable affects the current magnitude in the line but has no influence on the circuit thyristor's turn-off speed.

III. PRINCIPLE AND DESIGN OF THE PROTECTION STRATEGY

To ensure the effective triggering of the Z-SSCB, an auxiliary protection function containing sensors and an auxiliary branch is considered. This is highlighted by the green dashed box in Fig. 5. Sensors are used to measure the current or voltage at the load side.

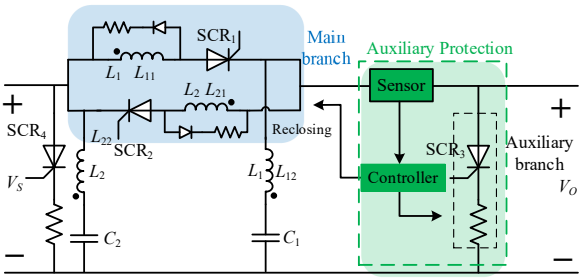


Fig. 5. A Z-SSCB with an auxiliary protection function (CB-1).

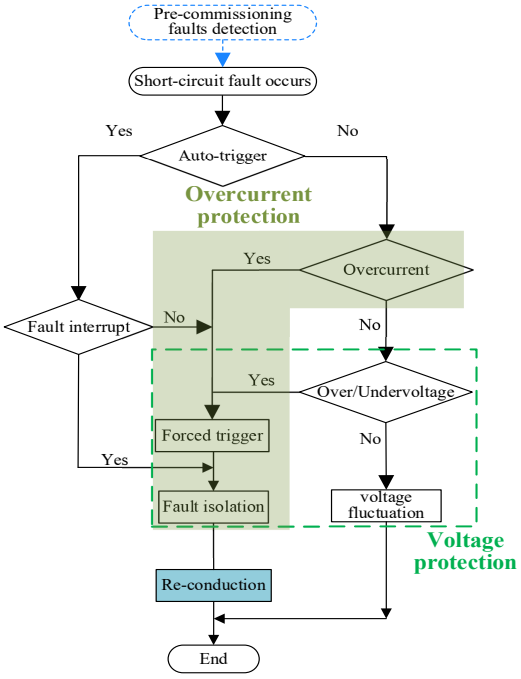


Fig. 6. Flowchart of the protection strategy based on Z-SSCBs.

A flowchart of the protection strategy is shown in Fig. 6. It includes three main parts: overcurrent protection, overvoltage protection, and re-conduction. Once a short-circuit fault occurs, if a large rate of rise of fault current is exhibited, the Z-SSCB would be triggered and the fault current interrupted, followed by fault isolation. In this case, the auxiliary protection does not act. However, if the rate of rise of current is smaller than K, SCR_1 or SCR_2 cannot be automatically triggered, leading to a continuous increase in current magnitude. The current sensor within the auxiliary protection will detect this overcurrent, enabling the controller to send a turn-on signal to SCR_3. This allows a fast discharging of C_1, producing a counter-current to draw currents of SCR_1 or SCR_2 to zero. SCR_1 or SCR_2 will then turn off to interrupt the fault current and isolate the fault. After the fault is fully isolated and cleared, the controller will send signals to SCR_1 or SCR_2 to restore the Z-SSCB to the pre-fault status (i.e. SCR_1 or SCR_2 are on, and SCR_3 is off).

Similarly, when the voltage sensor detects an overvoltage or an undervoltage, the working principle of the auxiliary protection and restoration is similar to that of overcurrent. SCR_3 will be turned on to discharge C_1 or C_2, forcing SCR_1 or SCR_2 to be turned off.

A. Inverse-time overcurrent protection

Overcurrent and over/undervoltage detection is critical to guarantee the absolute safety required in MEA applications. Thus, the detection algorithm presented in this paper is adapted from proven algorithms to effectively ensure the reliable triggering of the Z-SSCB. When the Z-SSCB does not trigger automatically, the fault current will continue to rise until reaching a threshold, which activates the auxiliary protection function. The threshold current is preset to meet industry standards, including IEEE regulations of inverse-time overcurrent protection [30] and the aircraft electrical standard MIL-STD-704F [31].

Inverse-time overcurrent protection is widely used for the protection of power systems, line backup and transformers. The basic operation principle is to determine the length of the delay time for triggering the CB according to the magnitude of the fault current. The larger the value of the fault current is, the shorter the delay time, and vice versa.

The characteristic of a general inverse-time overcurrent protection curve is defined by

$$t(I)=\left(\frac{A}{M^{p}-1}+B\right) \quad M>1 \qquad (6)$$

where A, B and p are constants, M is the current expressed in multiples of the pickup current (I_{input}/I_{pickup}, where I_{pickup} is the relay current set point) and $t(I)$ is the operating time in seconds.

By changing the values of A, B and p in (6), different curves are obtained. Typical curves are summarized in Table III [30]. The moderately inverse characteristic, shown in Fig. 7, is selected in this paper to meet the requirements of MEA protection according to [31]. It ensures to effectively trigger the Z-SSCB when it fails to be automatically turned off during a short-circuit fault.

TABLE III
PARAMETERS OF IEEE INVERSE-TIME CHARACTERISTIC [30]

Characteristic	*A*	*B*	*p*
Moderately inverse	0.0515	0.1140	0.02
Very inverse	19.61	0.491	2
Extremely inverse	28.2	0.1217	2

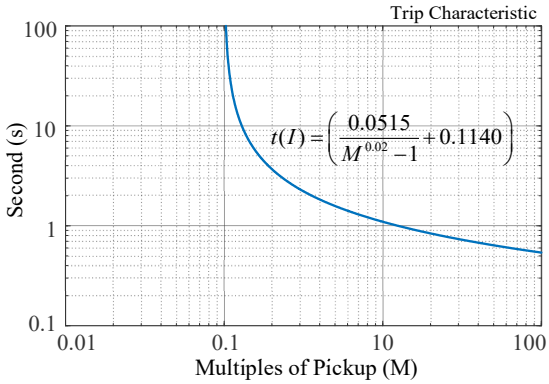


Fig. 7. Standard moderately inverse-time current characteristic [30].

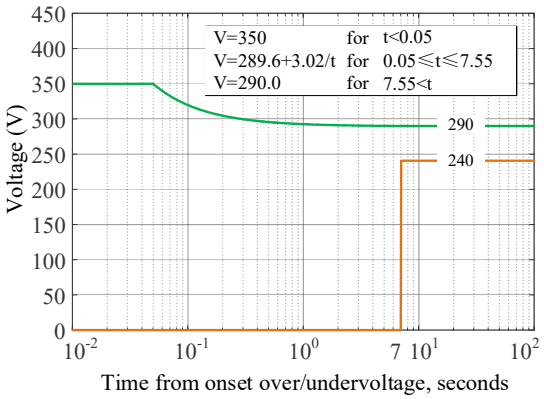


Fig. 8. Limits for overvoltage and undervoltage for a 270 V dc system [31].

B. Voltage protection

Voltage variation of the aircraft power supply system is divided into overvoltage and undervoltage. These adverse conditions may be caused by converter failures, abnormal switching of aircraft power modes, and sudden loading and unloading of loads [34]. When any of these events leads to an overvoltage or undervoltage, if protection measures are not taken quickly, damage to the whole MEA power supply system would be sustained.

When a short-circuit fault occurs in the system, the most direct manifestation is a rapid change in current. Voltage may also change, but not that significantly. Therefore, protection strategies based on voltage variations are often used as a backup protection instead.

According to standard MIL-STD-704F [31], the limits for dc overvoltage and undervoltage for a 270 V dc system are shown in Fig. 8 and are adopted in this paper. For instance, this implies that the system should be able to maintain a voltage of 350 V for 0.05 s.

To summarize, the auxiliary protection circuit is mainly used to enable the Z-SSCB to have the functions of inverse-time overcurrent and overvoltage/undervoltage protection. When conditions (1) and (2) are met, the automatic triggering of the Z-SSCB quickly isolates the fault and the auxiliary protection does not act. Otherwise, it ensures the triggering function of the Z-SSCB to ensure the isolation of the fault.

C. Application considerations of the protection strategy

Load-side current blocking. To ensure the effective triggering of the Z-SSCB and automatic turning off of thyristors in the auxiliary branches when there is a power supply at the load side, diodes D_1 and D_2 are added to the main circuit. Taking SCR_3 as an example, when it is triggered, D_1 will prevent the fault current from flowing to SCR_3. Hence only the discharging current from C_1 will flow into SCR_3, which then allows SCR_1 to be turned off (i.e. CB tripped), as shown in Fig. 9. SCR_3 will turn off naturally once C_1 is fully discharged.

Safe start of a Z-SSCB. The safe start is one of the main challenges for Z-SSCBs [32]. To address this problem, a separate capacitor charging branch may be required. This way, the capacitor would be charged before the thyristor in the main circuit of the CB is turned on. The subsequent discharge of the capacitor would help to determine the presence of a short-circuit fault. The capacitor charging branch is illustrated with a green dashed line in Fig. 10. This includes both an extra *SCR* (S_1) and a mechanical switch (S_2). To avoid using both, an alternative approach is to use two *SCR*s (SCR_5 and SCR_6) to replace the diodes (D_1 and D_2) in the design shown in Fig. 9. The new topology is shown in Fig. 11. This topology has the same number of components compared to the one in Fig.

9. The topology has both the functionalities of pre-commissioning protection and current blocking at the load side with a power supply.

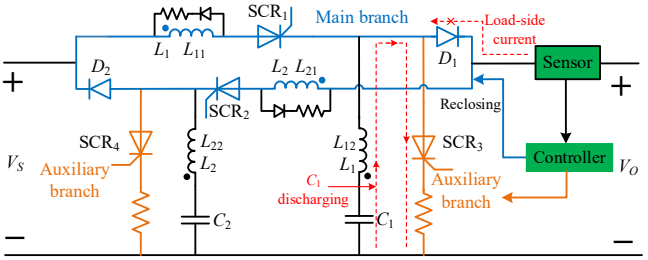


Fig. 9. Configuration of the Z-SSCB with an auxiliary protection function when there is a power supply at the load side (CB-2).

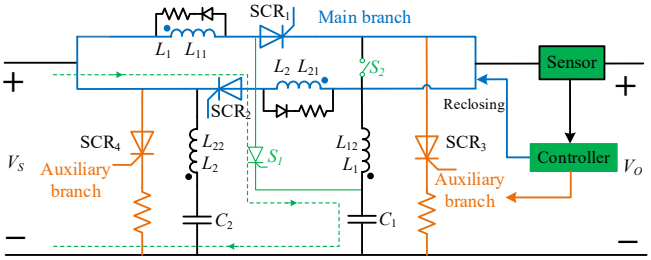


Fig. 10. Z-SSCB with a capacitor charging branch including an *SCR* and a switch (CB-3).

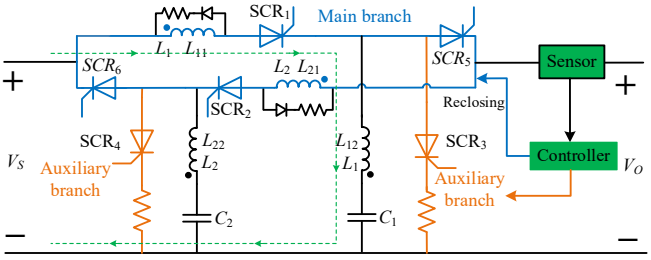


Fig. 11. Z-SSCB with diodes replaced by *SCR*s (CB-4).

To add the functionalities of load-side current blocking or pre-commissioning fault protection, diodes or thyristors are included in the main circuit for the topologies in Fig. 9 and Fig. 11, resulting in two semiconductors in the main circuit. This is similar as in methods adopted in the existing literature. Hence, the power loss for the topologies in Fig. 9 and Fig. 11 will be similar to those from existing methods, but higher than those in Fig. 5 and Fig. 10.

Unidirectional protection. A Z-SSCB plays a protective role when connected in series with loads. Regarding unidirectional applications, when SCR_3 is turned on (see Fig. 10), the main circuit's thyristor of the Z-SSCB (SCR_1 or SCR_2) will be turned off provided an adequate reverse voltage is created. Consequently, SCR_3 will also be turned off once its current reaches zero.

Bidirectional protection. Regarding bidirectional applications, the load could be supplied in both directions by a double-bus, double-breaker system [36]. The protection would require additional block diodes in the circuit to limit the direction of current flow, in addition to the series CBs between both sources and the load.

On the cost implications for bidirectional protection. For bidirectional protection, the auxiliary branch should be present at both the output and the input, and this will increase cost and weight. However, this approach may be still advantageous compared to using two unidirectional CBs with two auxiliary branches for bidirectional protection. Since the thyristor in the auxiliary branch will have a rated voltage significantly lower than the thyristor in the main circuit, it will be significantly lighter and, thus, less expensive. The auxiliary branch will make up for a very small portion of the weight and cost of the Z-SSCB topology.

On the configuration of the dc grid. When the Z-SSCB is used to protect a dc load, the Z-SSCB will remain unaffected by the system configuration mode (e.g. radial, ring or interconnected [35]) as long as the input and output of the Z-SSCB coincide with the input and output of the dc load to be protected.

Discrimination. To correctly discriminate between sudden load variations and overcurrent faults, a reasonable fault current threshold should be set according to the range of load changes for the load being protected. For instance, if an output current greater than the threshold is detected, this implies an overcurrent fault has taken place.

Pulsating loads. The longer a transmission line is, the greater the probability of a fault occurring is too. As an additional consideration, when a pulsating load (exhibited when deploying a buck converter) is closer to the bus than to the load, faults are more likely to occur at the output [36]. Simultaneously, Z-SSCBs require a constant current to operate properly, so they should be connected in series with the output side of the buck converter to provide protection.

Device malfunction. The Z-SSCB will malfunction if the fault detection unit fails to detect a continuous overcurrent or overvoltage fault in time, or if the auxiliary branch cannot be opened in time. Having said that, these scenarios are unlikely to happen. In the presence of small impedance short-circuit faults, the Z-SSCB investigated in this paper provides automatic interruption and isolation of the fault currents. Moreover, its auxiliary protection can isolate the short-circuit fault for large impedance faults or persistent overcurrent/overvoltage faults.

D. A comparative study

A) Comparison between the proposed topology and those in [37] and [38].

To provide a clearer understanding of the contributions of this paper and highlight the differences of the presented Z-SSCB configurations from existing published work, a comparison with the topologies presented in [37] and [38] was conducted. A summary of this comparative exercise is presented in Table IV.

The topology in [37] incorporates one auxiliary branch for unidirectional protection and an additional diode in the main circuit to block current from the load side. However, this topology cannot be utilized for bidirectional protection or protection against pre-commissioning faults. In the proposed topology in this paper and in the one presented in [38], the topologies feature two auxiliary branches for bidirectional protection and two semiconductors in the main circuit during normal operation. Nevertheless, the two diodes incorporated to the original design were used to address load-side current blocking, which is not a feature discussed in [38], resulting in two semiconductors in the main circuit.

TABLE IV
COMPARISON WITH THE TOPOLOGIES PRESENTED IN [37] AND [38]

Characteristics	**Proposed in this paper**	[37]	[38]
Auxiliary branch	**2**	1	2
Bidirectional protection	**Yes**	No	Yes
Pre-commissioning protection	**Yes**	No	No
Load-side current blocking	**Yes**	Yes	No
Time-inverse protection	**Yes**	No	No
Reliability	**High**	Low	Low
Complete protection strategy	**High**	No	Low
Number of semiconductors in the main circuit breaker	**1 to 2**	2	2
Power loss	**Low to Medium**	Medium	Medium

Furthermore, neither the topologies in [37] nor [38] introduce any protection algorithms or establish a comprehensive protection strategy for dc protection in MEA. Also, the proposed protection strategy considers multiple variations evolved from the original Z-SSCB configuration to selectively cover all functions and application scenarios, resulting in different numbers of semiconductors to be used in the main circuits. However, the number of devices is no greater than for the topologies in [37] and [38], so arguably the power losses are either lower or similar. The presented protection strategy also has the highest reliability due to the functions of pre-commissioning protection, load-side current blocking and time-inverse protection.

Overall, an auxiliary branch based on the proposed topology combining inverse-time delay protection was developed in this paper to form a robust protection strategy for MEA using Z-SSCB. Furthermore, innovative solutions for various application scenarios in MEA are presented, such as pre-commissioning protection, bidirectional protection, and protection in the presence of a power supply at the load side. It is an innovative and comprehensive method for the practical control of the Z-SSCB, and thus, it has the potential for practical deployment in MEA applications.

B) Comparison among the proposed four topologies.

Four different CB topologies have been presented in the paper to consider additional protection functionalities. A comparative study is conducted to further discuss their advantages and disadvantages. To facilitate the discussion, the CB in Fig. 5 is named CB-1, the one in Fig. 9 CB-2, the one in Fig. 10 CB-3, and the one in Fig. 11 CB-4. Table V compares the number of components and functionality of the four topologies.

CB-1 has the lowest on-state loss and cost as it has the fewest total number of components and semiconductors in the main circuit, while it does not have the function of pre-commissioning faults protection and load-side current blocking with an extra power source at the load side. In contrast, CB-2 deploys two diodes in the main circuit to achieve load-side current blocking function, but this increases the on-state losses. Nevertheless, the cost increase is expected to be minimal since diodes are generally inexpensive (e.g. 1.28 GBP [42]). CB-3 includes an extra thyristor and a mechanical switch to form a capacitor charging branch, offering protection against pre-commissioning faults. It maintains the lowest power loss as the number of *SCR*s in the main circuit stays the same as in CB-1. The added capacitor charging branch would still slightly increase the cost of the CBs, and the function of load-side current blocking is not included. Alternatively, CB-4 includes both functions with the same number of components as in CB-2. However, the disadvantage of CB-4 is its higher cost due to the more expensive thyristors compared to the diodes used in CB-2.

TABLE V
COMPARISON AMONG THE PROPOSED FOUR TOPOLOGIES IN THE PAPER

Topology	CB-1	CB-2	CB-3	CB-4
Number of Thyristors	4	4	5	6
Number of didoes	0	2	0	0
Number of semiconductors in the main circuit	1	2	1	2
Mechanical switch	0	0	1	0
Power loss	Low	Medium	Low	Medium
Load-side current blocking	No	Yes	No	Yes
Pre-commissioning faults protection	No	No	Yes	Yes
Cost	★	★★	★★	★★★

E. Weight and cost analysis of thyristors

Additional thyristors are utilized to perform the functions of the proposed strategy, but their weight and cost are not significant. Several thyristors which can satisfy the application requirements of MEA have been obtained from a component manufacturer [43], as shown below in Table VI. It can be seen that the cost of a single thyristor is only between £1.92 to £8 and weighs no more than 6 g, which is negligible. For a practical implementation, purchasing large quantities of thyristors will result in even more economic unit prices, which makes the additional cost very limited.

TABLE VI
INFORMATION OF THE THYRISTORS SUITABLE FOR MEA [43]

Type	Voltage/Current (AV)	Cost		Weight
		Single	large quantities (1000)	
TN5015H-6G-TR	600 V/30 A	£1.92	£0.94	1.5 g
CLB40I1200PZ-TUB	1200 V/40 A	£3.54	£2.21	1.5 g
TM8050H-8W	800 V/50 A	£5.42	£2.89	4.43 g
VS-70TPS16PBF	1600 V/70 A	£7.3	£5.05	6 g
CLA80E1200HF	1200 V/80 A	£8	£4.76	6 g

IV. SIMULATION VERIFICATION

The protection strategy is verified via software simulation conducted with Saber. It is assumed the Z-SSCB works with a 270 V_{dc} power supply system, with a load resistor R_L = 10 Ω and a load capacitor C_L = 220 μF. The Z-SSCB is designed not to act when the load-side current variation is less than 5 times the rated current. Thus, the turns ratio n of the coupled inductor, which is related to the response characteristics of the CB to a step change of the load [33], is selected as 5. Other relevant parameters of the Z-SSCB are obtained based on the analysis presented in Section III and are summarized in Table VII.

TABLE VII
Simulation PARAMETERS

Components	Parameters
Capacitor	$C_1 = C_2 = 230$ μF
Coupled inductor	$L_{11} = L_{21} = 2500$ μH $L_{12} = L_{22} = 100$ μH $n_1 = n_2 = 5$
Load resistor	$R_L = 10$ Ω
Load Capacitor	$C_L = 220$ μF

TABLE VIII
Delay Time of the Auxiliary Protection Scheme

Voltage	Theoretical action time [31]	Current	Theoretical action time [30]
330 V	0.075 s	81 A	0.187 s
310 V	0.15 s	67.5 A	0.222 s
290 V	4.55 s	54 A	0.292 s
240 V	4 s	40.5 A	0.494 s

The maximum fault resistance of the Z-SSCB is chosen as $R_{f\ max} = 1.022$ Ω, and the minimum fault ramp rate is set to $K = 5781$ $(\Omega{\cdot}s)^{-1}$. These values have been selected to ensure that the Z-SSCB fails to trigger automatically and, hence, to test the performance of the designed auxiliary protection algorithm.

The inverse-time overcurrent protection and voltage protection schemes discussed in Section III are adopted. In the simulation, the action delay of the Z-SSCB is determined according to Table III [30]. The designed values of voltage/ currents against action time are shown in Table VIII. However, due to limitations of the experimental equipment (presented in Section V), it is not possible to capture high-bandwidth elements of a waveform accurately for a long time. For a consistent comparison between simulation and experimental results, the delay time for voltage was adjusted to 4.55 s for 290 V and to 4 s for 240 V. These adjustments do not affect the verification of the presented protection strategy.

A. Inverse-time overcurrent protection

To prevent voltage protection preceding current protection, the detection and control procedures related to voltage are temporally disabled in this first simulation.

Simulation results when inverse-time overcurrent protection is active only are shown in Fig. 12. It can be seen from Fig. 12(a) that when $t(s) = 0.6024$ s, an overcurrent of 81 A is applied, which is three times larger than the rated current. When the overcurrent lasts for 0.1876 s until $t(s) = 0.79$ s, the CB starts to operate by turning on SCR_3. The load voltage rapidly drops to zero, and the voltage of SCR_1 is then reverse-biased to interrupt the fault current, which stabilizes at 0 A. This shows that the auxiliary protection enables the Z-SSCB to interrupt the current with the designed relay time duration of 0.187 s (see Table VIII).

Fig. 12(b) shows the results when an overcurrent of 67.5 A, 2.5 times the rated current, is applied. The Z-SSCB interrupts the fault current in 0.2205 s, which agrees on well with the designed relay time duration of 0.222 s. Tests are repeated for overcurrents of 54 A and 40.5 A, with interruption time delays of 0.292 s and 0.494 s, as shown in Fig. 12(c) and Fig. 12(d) respectively. These are in line with the values in Table VIII.

The results shown in this section demonstrate that the reliability of inverse-time overcurrent protection enables a dual protection facilitated by the automatic and auxiliary

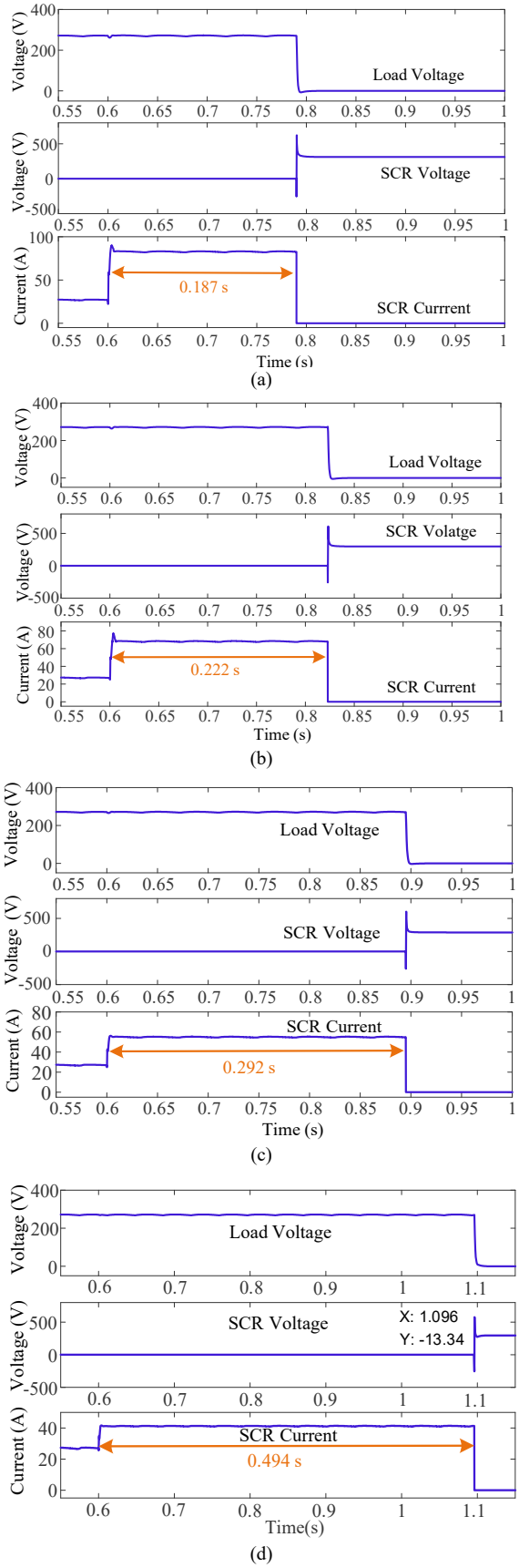


Fig. 12. Simulation results of inverse-time overcurrent protection. Overcurrent of (a) 3 times the rated current (81 A), (b) 2.5 times the rated current (67.5 A), (c) 2 times the rated current (54 A), (d) 1.5 times the rated current (40.5 A).

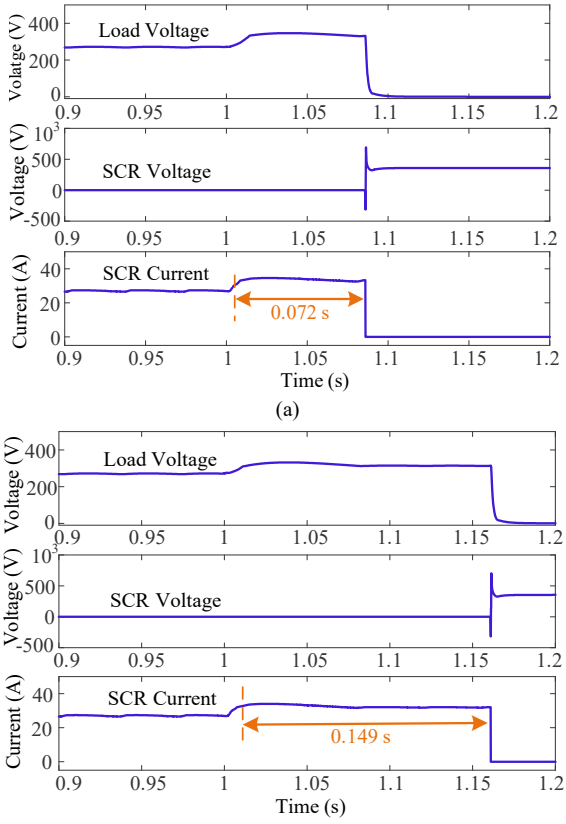
triggering of the Z-SSCB. This can not only expand its application range, but also enhance the reliability of the protection scheme itself.

B. Over/Undervoltage protection

Fig. 13 shows the simulation results when the voltage protection of the Z-SSCB is activated. It can be seen in Fig. 13(a) that an overvoltage of 330 V is applied at $t(s)$ = 1.014 s. This lasts for 0.072 s until the Z-SSCB starts opening at $t(s)$ = 1.086 s. The load voltage then drops rapidly to zero, the thyristor voltage is reverse-biased, and the current drops and stabilizes at 0 A. This indicates that the Z-SSCB has completely opened and the fault has been removed. The action time of Z-SSCB is thus 0.072 s, which differs only by 0.003 s from the designed duration of 0.075 s and, hence, the protection standard is met.

When an overvoltage of 310 V is applied instead, it lasts for 0.149 s (see Fig. 13(b)) and the Z-SSCB is disconnected to meet the protection requirements summarized in Table III. Similarly, Fig. 13(c) and Fig. 13(d) show results for an overvoltage of 290 V and an undervoltage of 240 V, with corresponding delay action times of 4.552 s and 3.976 s—agreeing on well with Table VIII.

From the simulation results, it is observed that the voltage protection function successfully acts according to the action time requirements. It is also shown that the action time is slower than that for inverse-time overcurrent protection. However, as an auxiliary protection method, it contributes to guaranteeing the reliable triggering of the Z-SSCB.



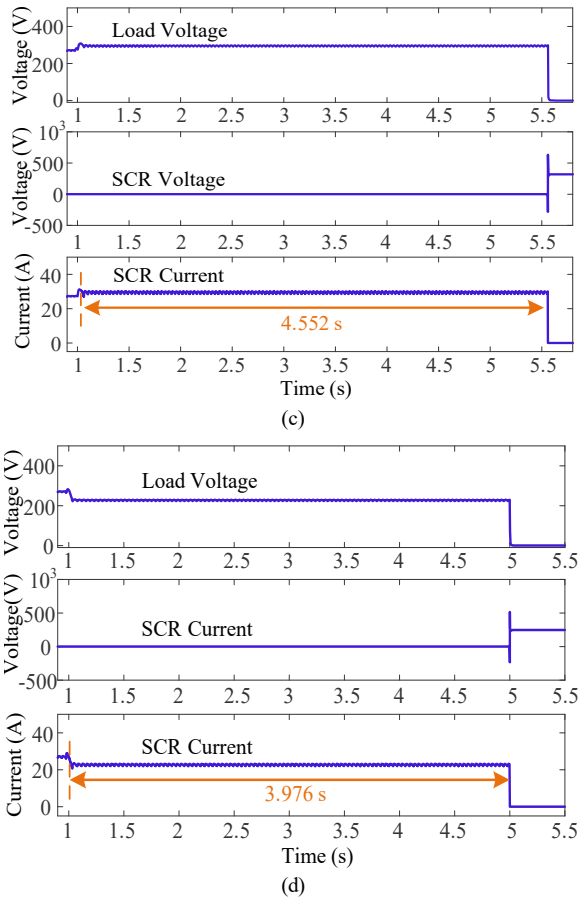


Fig. 13. Simulation results of voltage protection, (a) overvoltage of 330 V, (b) overvoltage of 310 V, (c) overvoltage of 290 V, (d) undervoltage of 240 V.

C. Re-conduction function

The purpose of this function is to restore to normal system operation after fault clearance. The measured current and voltage during this function are shown in Fig. 14. When the fault occurs, the Z-SSCB is triggered and the thyristor current becomes 0 A, which shows that the fault has been removed. Assuming a fault clearance within the specified delay time (2.5 ms), a signal is sent to trigger SCR_1 to reconnect the circuit. As shown, the capacitor is charged to the voltage source (270 V).

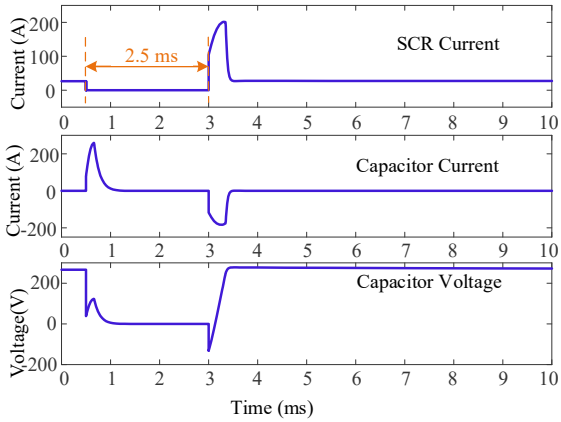


Fig. 14. Simulation results of the re-conduction function.

V. Experimental Validation

To further verify the protection strategy, an experimental prototype of a Z-SSCB with auxiliary protection units was built (see Fig. 15). The nominal voltage of the prototype is 50 V. The Z-SSCB includes capacitors C_1 and C_2, coupled inductors L_1 and L_2, thyristors SCR_1 and SCR_2, and freewheeling circuits. The auxiliary protection circuit includes five parts: a sampling circuit, an analog signal conditioning circuit, a control circuit based on the DSP28335 control unit, a digital signal output circuit, and a power supply circuit for each circuit.

The working voltage of the Z-SSCB investigated in Section IV is scaled down to 50 V and the rated current to 1.67 A. The experimental verification of inverse-time overcurrent and voltage protection and re-conduction for a purely resistive load (R_L = 30 Ω) is carried out next. The selected operating times of the Z-SSCB are shown in Table IX.

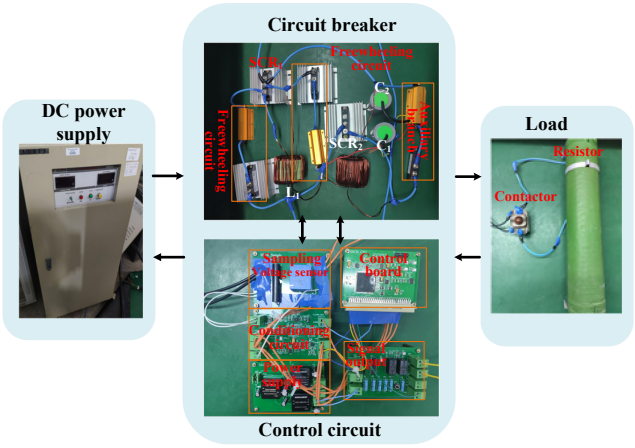


Fig. 15. Prototype for experimental validation of the protection scheme.

TABLE IX
Action Time of the Auxiliary Protection Scheme

Voltage	Theoretical action time [31]	Current	Theoretical action time [30]
61 V	0.075 s	5 A	0.187 s
57 V	0.15 s	4.17 A	0.222 s
54 V	4.55 s	3.3 A	0.292 s
44 V	4 s	2.5 A	0.494 s

A. Inverse-time overcurrent protection

An overcurrent is emulated by closing the load contactor (see Fig. 15) to create a fault with a fault resistance R_{step} in parallel with the load. Fig. 16 show the experimental results.

Fig. 16(a) shows results for an overcurrent of 5 A (three times the rated current). This is created by connecting a fault with a resistance of 15 Ω at $t(s) = t_1$. During $t_0 \sim t_1$ prior to the fault, the load voltage is 50 V (see blue trace), the thyristor current is 1.67 A (yellow trace), and the overcurrent signal (red trace) and auxiliary control signal (green trace) outputs by the DSP are at low levels. At t_1, the thyristor current changes from 1.67 A to 5 A, but the load voltage remains unchanged. The current sensor detects the overcurrent and the overcurrent signal becomes high. However, the auxiliary control signal remains low until the protection action time is reached at t_2. At t_2, the DSP outputs a high level signal which requests the relay on the signal output board to pull in. Given the relay is

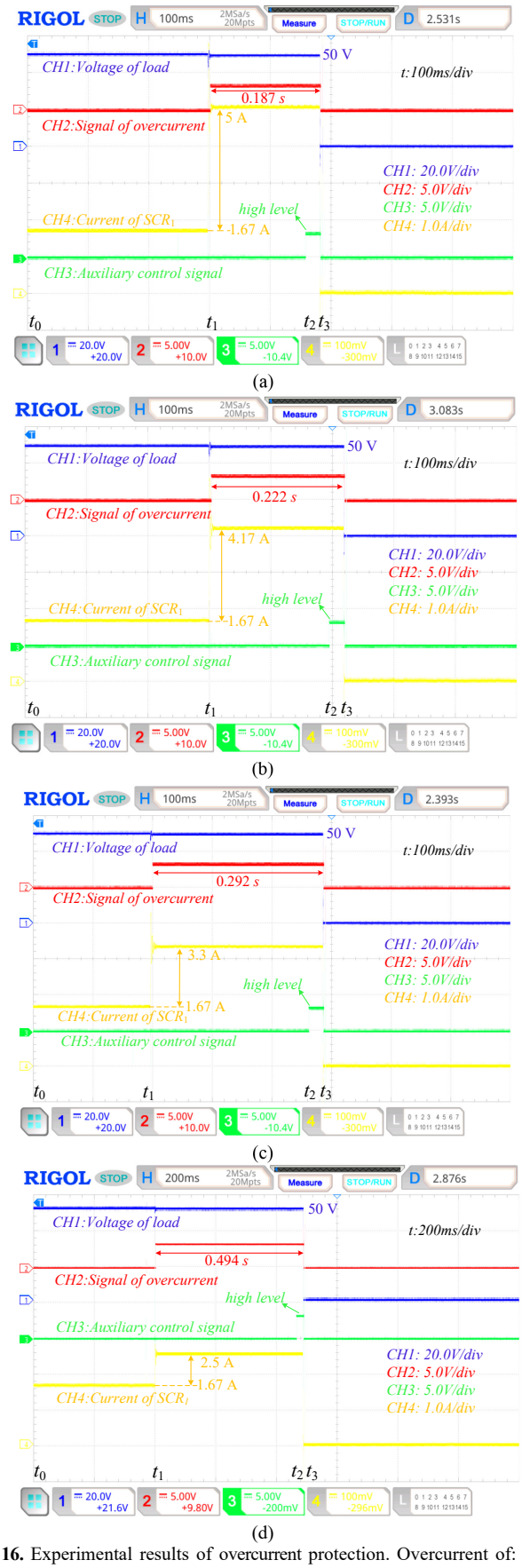


Fig. 16. Experimental results of overcurrent protection. Overcurrent of: (a) 3 times the rated current (5 A), (b) 2.5 times the rated current (4.17 A), (c) 2 times the rated current (3.3 A), (d) 1.5 times the rated current (2.5 A).

mechanical, this occurs after 30 ms at t_3. At this point, the thyristor of the auxiliary control circuit receives the drive signal and closes, the Z-SSCB is triggered, and the current of SCR_1 drops rapidly and stabilizes at 0 A. After the Z-SSCB is turned off, the load voltage also decreases from 50 V to 0 V, the overcurrent and auxiliary signals change to a low level, and the Z-SSCB protection ends.

In summary, for an overcurrent fault of three times the rated current (5 A), the Z-SSCB detects the fault at t_1 and turns off at t_3 after a delay of ~180 ms, which, according to the protection action time standard, meets the protection requirements.

Different values of R_{Step} are used to investigate other values of overcurrent (i.e. 2.5 times the rated current, 4.17 A; 2 times the rated current, 3.3 A; and 1.5 times the rated current, 2.5 A). Experimental results for these fault conditions are shown in Fig. 16(b) to Fig. 16(d). The colors used in the traces are similar as for Fig. 10(a). In general, when the current ramp is detected, the DSP outputs the control and protection signal to the auxiliary branch after the set delay time to trigger the Z-SSCB.

The experimental results presented in this section verify the inverse-time overcurrent protection function of the Z-SSCB, which successfully interrupts and isolates short-circuit faults while strictly abiding by current protection action standards.

B. Voltage protection

In the voltage protection experiment, overvoltages and an undervoltage were emulated by changing the power supply voltage directly. Experimental results are shown in Fig. 17.

Fig. 17(a) shows results for an overvoltage of 61 V. Before t_1, the DSP overvoltage signal is at a low level (red trace). At t_1, the voltage is higher than the specified protection value (blue trace) and the DSP signal becomes high. When the overvoltage exceeds the protection action time, the DSP outputs a high level auxiliary control signal at t_2 (green trace), the relay is pulled in within 30 ms, the thyristor of the auxiliary circuit receives the driving signal, and the Z-SSCB is turned off at t_3. When the load voltage and the current of SCR_1 (yellow trace) drop to zero, the protection process is completed. As the voltage signal directly collects the power supply voltage, this will change when the Z-SSCB is turned off, and the output overvoltage and auxiliary control signals of the DSP remain high. The time interval between t_1 and t_3 is ~78 ms; i.e. when the system voltage is 61 V and lasts for more than 78 ms, the Z-SSCB judges that an overvoltage fault occurs and disconnects appropriately.

Experiments for other voltage fault conditions have been also conducted. Fig. 17(b) shows results when the overvoltage is 57 V. In this case, the overvoltage duration is ~150 ms and the Z-SSCB is turned off. Fig. 17(c) and Fig. 17(d) show results for an overvoltage of 54 V and an undervoltage of 44 V. In these two experiments, the Z-SSCB outputs a high auxiliary control signal when the duration of the overvoltage exceeds 4.5 s and when the duration of the undervoltage exceeds 4 s, respectively. Then, the Z-SSCB is turned off.

The voltage protection experiments show that the Z-SSCB can accurately identify and reliably isolate the faults according to the set voltage fault protection standard.

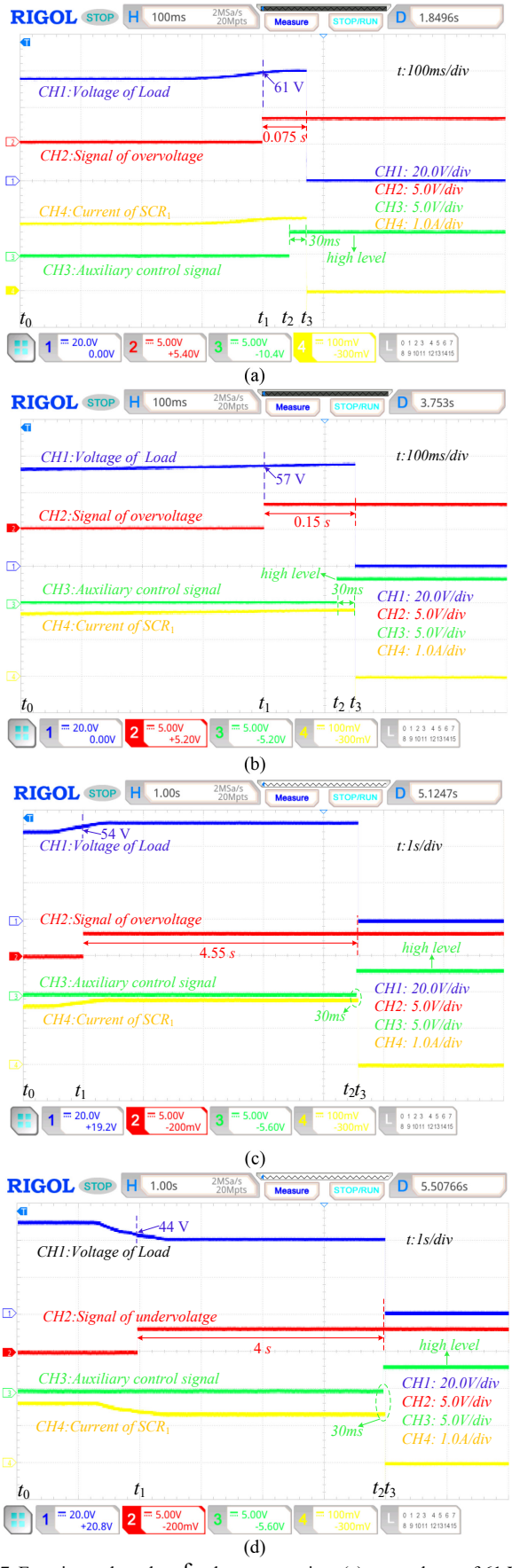


Fig. 17. Experimental results of voltage protection: (a) overvoltage of 61 V, (b) overvoltage of 57 V, (c) overvoltage of 54 V, (d) undervoltage of 44 V.

C. Re-conduction function

The results for the re-conduction experiment are shown in Fig. 18. The system operates normally during t_0~t_1. When $t(s) = t_1$, an overcurrent occurs in the system, the thyristor current rises to about 5 A (yellow trace), and the DSP outputs a high level overcurrent signal (red trace). When the current delay time reaches the protection action time, the Z-SSCB operates. The load voltage and thyristor current rapidly drop to zero, and the overcurrent signal shifts to a low level. After the Z-SSCB is turned off, the overcurrent fault is eliminated, and the DSP outputs a high thyristor closing control signal (green trace) at t_3, after ~4 s, to turn on the thyristor SCR_1. The Z-SSCB returns to its rated operation at 50 V (blue trace) and the current changes to 1.67 A. To ensure the Z-SSCB can be turned off for a hypothetical subsequent fault, the driving signal of the thyristor should be reset quickly after it is turned on. Therefore, the DSP output closing signal is set to last ~50 ms, it is then driven to a low level at t_4 (green trace), and the Z-SSCB is ready for the next fault.

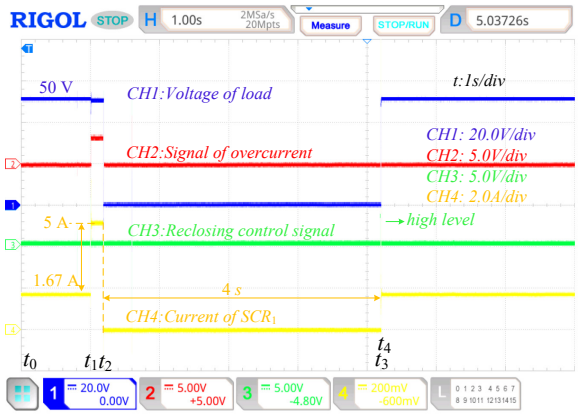
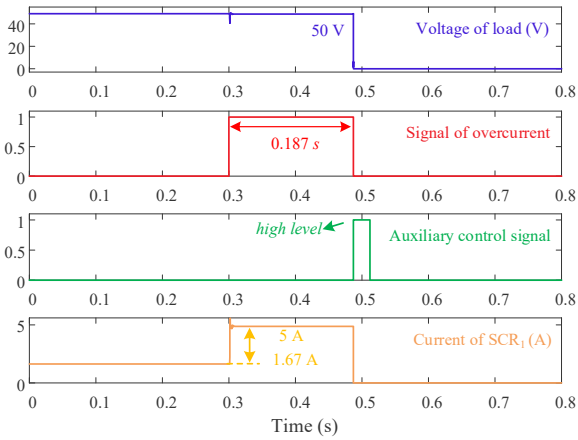
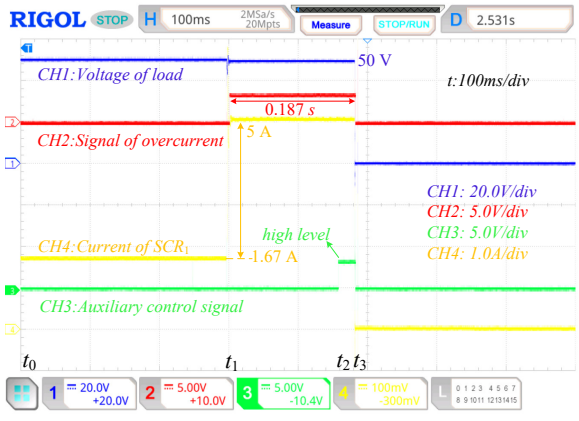


Fig18. Experimental results of the re-conduction function.



(a)



(b)

Fig. 19. Comparison between the simulation and experiment results of overcurrent protection at 5 A: (a) simulation results, (b) experimental results.

D. Reliability analysis of the experiment

In this paper, the proposed protection strategy was verified by conducting scaled-down experiments, which is similar to the approach adopted in [29], [39] and [40] to conduct experimental work. The scalability of the protection strategy across different voltage levels was verified using both computational simulations and mathematical analysis, which provides important insight for high voltage level design.

The value for the system's overcurrent was scaled down linearly using a base of 16.2 A. In contrast, for the system undervoltage and overvoltage, the values were scaled down using a base of 5.4 V. To further verify the validity of the low voltage experimental facilities, the same parameters for overcurrent protection (5 A) were used in simulations and compared to the experimental results. The comparison of the simulation and experimental results is shown in Fig. 19. When an overcurrent fault occurs, the fluctuation of the load voltage and the delay time (0.187 s) are consistent both in the simulation and experiment. Thus, in both cases, it is possible to send an auxiliary control signal after the set delay time, resulting in the rapid removal of the fault.

VI. Conclusion

The power supply systems for MEA have been recently shifting from ac to HVDC, but protection has been still recognized as a major challenge. The Z-SSCB, by exhibiting a simple structure and a fast-breaking speed, is a prime candidate to facilitate deployment of HVDC-based power supply systems. To contribute to this end, an auxiliary protection strategy based on Z-SSCBs was presented in this paper. The strategy forces the opening of a Z-SSCB when overcurrent, overvoltage or undervoltage faults do not meet the designed automatic triggering conditions of the Z-SSCB. This is of importance as the protective scheme may effectively expand the range of applications for Z-SSCBs.

The presented strategy combines inverse-time overcurrent and voltage protection, and the corresponding parameters have been designed according to industrial standards. This enables the protection scheme to meet the stringent requirements of aircraft power supply systems.

The presented protection strategy has been verified through simulation tests conducted in Saber. For completeness, this has been complemented with experimental validation using a down-scaled laboratory prototype. It has been shown that by applying the protection strategy, the Z-SSCB is capable of isolating faults exhibiting large fault resistance and small fault current ramp rate, which makes up for the shortcomings of the Z-SSCB and, thus, improves its reliability.

The sets of simulation and experimental results agree on well, demonstrating that the reliability of inverse-time overcurrent protection facilitates a dual protection by enabling both automatic and auxiliary triggering (if needed) of the Z-

SSCB. Given that the action time of voltage protection is faster than that of overcurrent protection, voltage protection can be used as a backup to fully guarantee a reliable triggering of the Z-SSCB should this be required. The protection scheme enables system restoration to ensure the system is ready both to resume normal operation and to be protected against subsequent faults should they occur.

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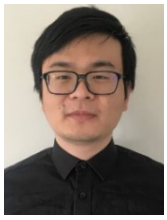

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