Motor Overvoltage Mitigation Using SiC-Based Zero-Voltage Switching Inverter

Suleman Yunus, Wenlong Ming, *Member, IEEE,* and Carlos E. Ugalde-Loo, *Senior Member, IEEE*

***Abstract*—The motor overvoltage phenomenon is an issue that may arise from the high voltage slew rates ($\mathrm{d}v/\mathrm{d}t$) of silicon carbide MOSFETs in cable-fed drives. This can lead to substantial strain on cable and motor insulation, resulting from partial discharges and uneven voltage distribution. In line with this, this paper presents a novel method to select inductor and capacitor parameters for a zero-voltage switching (ZVS) inverter to mitigate motor overvoltage. The ZVS inverter employs only one additional active switch on the positive dc terminal compared to two-level inverters. This prevents the need for bulky LCR and RC passive filters or multilevel inverters in conventional solutions which may lead to increased volume and losses. The presented approach suppresses overvoltage oscillations by profiling the $\mathrm{d}v/\mathrm{d}t$ of both resonant and natural commutations whilst minimizing the switching losses. A comparison with alternative techniques for mitigating motor overvoltage was conducted to demonstrate the method's efficacy, including two-level passive filter strategies and three-level inverters. The presented technique was validated through simulations in PLECS and MATLAB/Simulink, demonstrating a 1% increase in efficiency and a 30% reduction in volume. Furthermore, the method was experimentally verified, showing the measured overvoltage being reduced from 2 p.u. to 1.06 p.u.**

***Index Terms*—Cable-fed motor drives, motor overvoltage, reflected wave phenomenon, silicon carbide MOSFET, zero-voltage switching.**

I. INTRODUCTION

THE fast increase in voltage rise time observed in silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) holds great potential for improving operational efficiency and performance under arduous conditions such as mining, oil exploration, remote-operated vehicles and aerospace applications [1], [2]. However, the high voltage slew rate ($\mathrm{d}v/\mathrm{d}t$) associated with switching transitions in SiC MOSFETs can result in technical challenges, such as motor overvoltage oscillations, which have been documented in [3], [4]. The overvoltage phenomenon, also known as the reflective wave phenomenon, occurs due to an impedance mismatch between the cable and motor, leading to the reflection of voltage pulses generated by the inverter [5], [6]. The severity of this phenomenon is influenced by the rise time of voltage pulses, cable characteristics, and cable length [7], [8].

This work was supported by the Engineering and Physical Sciences Research Council (EPSRC) through a Doctoral Training Partnership (DTP) [under grant EP/R513003/1] and by the project "Multi-energy Control of Cyber-Physical Urban Energy Systems (MC2)" [under grant EP/T021969/1].

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Incorporating long cables to connect a SiC MOSFET inverter with a motor has the potential to generate a motor terminal voltage twice the magnitude of the inverter voltage, resulting in recurring partial discharges and rapid insulation breakdown [9], [10]. This predicament is particularly evident at high switching frequencies [11], [12]. Based on standard IEC 60034-18-41 [13], the first two coils of a motor encounter 40% of the voltage when the rise time is approximately 200 ns. Thus, it is critical to comprehend the relationship between voltage rise time and cable length and to formulate countermeasures for high-speed, high-power-density motors with low insulation thickness [14], [15].

The conventional approach to mitigate overvoltage is to use LCR filters at the inverter terminal to limit the $\mathrm{d}v/\mathrm{d}t$ of pulse-width modulation (PWM) pulses or RC filters at the motor terminals to match the impedance of the cable and motor [16]–[19]. This approach is simple and effective, but it has some drawbacks, such as the need for bulky LCR passive components, which occupy a large volume and subsequently increase the power loss and cost [11]. Moreover, there is an increased difficulty in adjusting the filter parameters when there are changes in the drive system voltage and power requirements [20]. Additionally, the high $\mathrm{d}v/\mathrm{d}t$ of SiC MOSFETs may interact with the filter parasitic elements, resulting in a high-frequency impedance mismatch, increasing, in turn, the motor overvoltage [17].

Filter-less strategies for addressing the issue of motor overvoltage have been proposed in the literature [20], [21], such as utilizing a three-level neutral point clamped (NPC) inverter to decrease voltage fluctuations or a quasi-three-level (Q3L) T-type inverter to cancel and mitigate voltage reflections. However, an overvoltage of 1.2 p.u. remains despite introducing such topologies [22]. An alternative approach that aims to fully mitigate overvoltage is the implementation of a soft-switching inverter and profiling the $\mathrm{d}v/\mathrm{d}t$. This technique actively determines the $\mathrm{d}v/\mathrm{d}t$ of voltage transients. An example of this approach is the soft-switching auxiliary resonant commutated pole inverter presented in [23]. Regardless, these three-level topologies may not be practical for three-phase systems due to the high number of switching devices required, volume constraints, and initial capital costs. Using active gate drivers may also be an effective technique, but they are costly and add complexity to the system. Furthermore, their application may be limited in specific systems due to design constraints, such as the need for high current drive capability [24].

Generally, cable-fed motor drive systems are required in inhospitable and inaccessible environments where the inverter and motor are connected at different locations [25]. The

challenge of effectively mitigating motor overvoltage in these extreme conditions whilst maintaining high efficiency and minimizing volume and cost remains an ongoing research topic. To this end, this paper presents a novel approach to addressing this issue by utilizing a zero-voltage switching (ZVS) inverter. Most ZVS topologies presented in the literature require several additional active switches for three-phase systems, which may not be suitable for cable-fed systems due to volume constraints in these conditions. For this reason, the topology presented in [26] is utilized in this paper since only one additional active switch is required. To realize ZVS without requiring multiple active switches, two types of commutation are devised, namely resonant and natural commutations. Moreover, by incorporating ZVS and a modified space vector PWM (SVPWM) scheme, the switching losses, electromagnetic interference, and power density are improved without significantly compromising the general structure of the two-level topology [27].

Prior research on the adopted ZVS topology has focused on grid-connected and photovoltaic inverters [27], [28]. Additionally, the changes in $\mathrm{d}v/\mathrm{d}t$ that occur during resonance and natural commutations are not uniform [29]. Thus, any attempt to characterize $\mathrm{d}v/\mathrm{d}t$ for resonant commutations may lead to discrepancies in the value of $\mathrm{d}v/\mathrm{d}t$ observed during natural commutations. Hence, it is necessary to take extra timing considerations into account to prevent motor overvoltage at each switching transition consistently. Furthermore, failure to address this issue adequately may still result in repetitive partial discharges at either resonant or natural commutations and prompt motor insulation failure. Further research is therefore necessary to explore the implementation and design parameters of the ZVS inverter for motor drives and overvoltage mitigation, specifically in the context of cable-fed systems.

The work presented in this paper makes three critical contributions to the field of motor drive systems. Firstly, it adapts the ZVS inverter topology presented originally in [26] to eliminate motor overvoltage in cable-fed drive systems while only requiring one auxiliary circuit. Secondly, an in-depth analysis of the inverter parameters based on different cable lengths and characteristics is conducted, which is crucial for the scalability and applicability of the ZVS topology for overvoltage mitigation. Finally, a comprehensive comparison of the volume and efficiency of the ZVS inverter with existing solutions is presented, including LCR and RC passive filter methods and three-level inverters, highlighting the advantages of the ZVS topology.

The effectiveness of the proposed approach was evaluated using the simulation tools MATLAB/Simulink and PLECS (Plexim) and experimentally validated with a 1.23 kW ac permanent magnet brushless servo motor drive system. It is shown that the presented method can improve the adaptability of the ZVS inverter for motor drive systems as follows:

1) To achieve full overvoltage mitigation, guidelines are shown for selecting the values of resonant capacitors and inductors based on the cable characteristics, length and $\mathrm{d}v/\mathrm{d}t$ requirements. By suitably designing the resonant parameters, the rise time of both resonant and natural commutations can be profiled—thereby, mitigating motor overvoltage.
2) In order to reduce the switching turn-off losses in the ZVS inverter, the duration of the voltage rise time has been prolonged. Ordinarily, increasing the voltage rise time in hard-switching inverters leads to larger switching losses. Nonetheless, as detailed in this paper, it is feasible to curtail the turn-off losses in the ZVS inverter. Given that ZVS already provides negligible switching turn-on losses, the presented approach enhances the efficiency of the entire motor drive system.

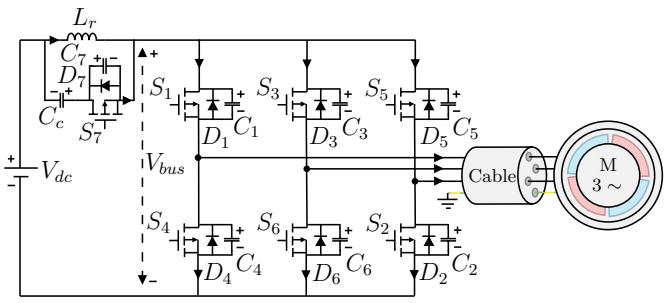


Fig. 1. Three-phase ZVS inverter cable-fed motor drive system.

The previous factors make the solution promising for addressing the issues of the reflective wave phenomenon in cable-fed drive systems and mitigating motor overvoltage whilst having minimum impact on the volume and efficiency of the whole drive system.

II. Review of ZVS Topologies

The three-phase ZVS inverter and the cable-fed motor are illustrated in Fig. 1. The auxiliary circuit is connected in series with the positive terminal of the inverter. A brief introduction to the control of the ZVS inverter is presented in this section.

A. Topology and Principle of Operation

Fig. 2 illustrates two types of current commutation in the legs of the ZVS inverter at a positive phase current i_m. In Case I, when switch S_+ is turned-off, i_m transitions from S_+ to the lower anti-parallel diode with the assistance of the paralleled capacitor C_r. During this transition, the ZVS is achieved, and $\mathrm{d}v/\mathrm{d}t$ is controlled by varying C_r. Conversely, Case II shows that the current transitions from the lower anti-parallel diode D_- to S_+, bypassing C_r, before S_+ is activated. This results in hard-switching and an increase in switching losses.

To enable ZVS during switching transitions in Case II, an auxiliary switch, S_7, and clamping capacitor C_c are utilized. S_7 predominantly conducts during the operating cycle, thereby accumulating energy in C_c. In anticipation of the occurrence of Case II transitions, it is necessary for the bus voltage V_{bus} subsequent to the auxiliary branch to resonate towards zero via the deactivation of S_7. Hence, in a conventional modulation scheme the switching frequency of S_7 will be high since Case II commutations will occur multiple times within each switching cycle.

In three-phase systems, the switching losses and complexity of the inverter control can be reduced by synchronizing the

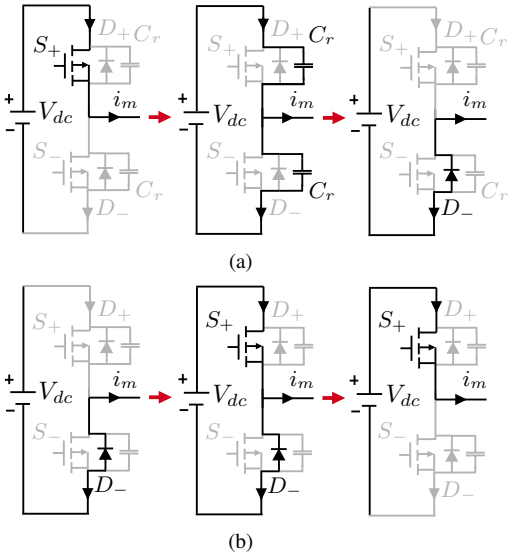


Fig. 2. Switching current commutation for ZVS legs at positive phase current: (a) Case I, (b) Case II.

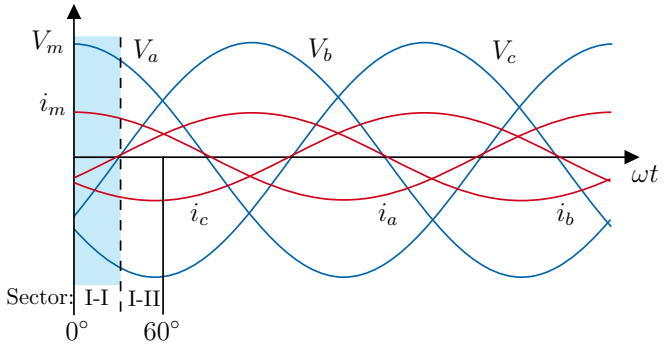


Fig. 3. Space vector sector definition based on current polarity.

switching of S_7 with the main switches in each phase leg. If SVPWM is used as the modulation technique [30], this can be accomplished by modifying the vector states based on current polarity. Sector I can be subdivided into two subsectors, Sectors I-I and I-II, as shown in Fig. 3. Each sector has a designated vector sequence of the switching states 000, 111, 100, 110. For instance, in Sector I-I, the arranged vector sequence is 111-100-110-111, where S_1 is always conducting and S_3 and S_5 are synchronized from the zero vector to the first vector. This method requires only one transition of S_7 per PWM cycle to achieve ZVS in Case II.

B. Analysis of Operation Modes

The steady-state operation of the inverter is summarized in Fig. 4 and is divided into six distinct stages of operation for Sector I-I [27]. These are described next.

Stage 1 ($t_0 - t_1$): Initial Stage.

The circuit is in state vector V7 (111) with S_1, D_3 and D_5 in conducting state. In the auxiliary circuit, S_7 is in conducting state and the resonant inductor (L_r) is charged by C_c. The size of C_c is large enough that the voltage across it is constant

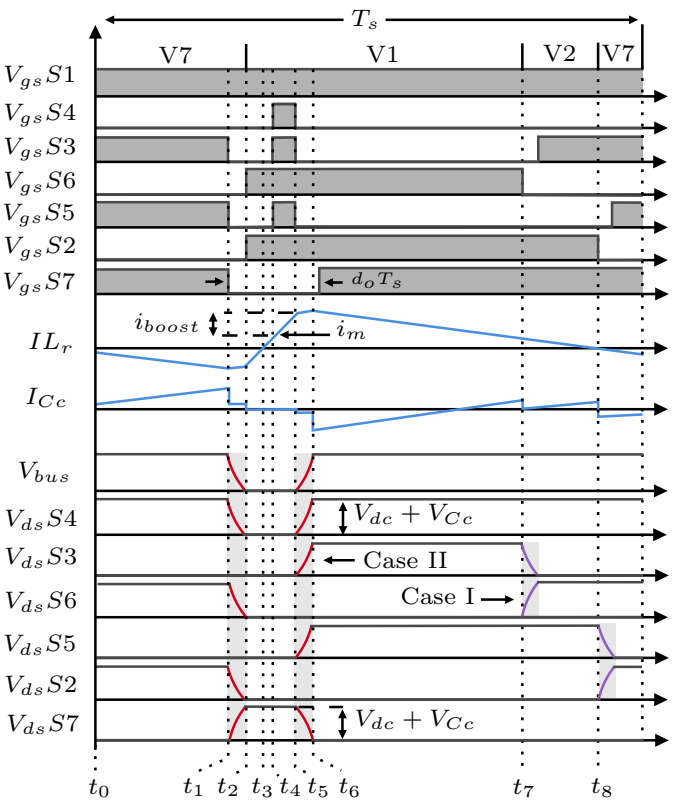


Fig. 4. Switching patterns and theoretical waveforms of gate-source voltage V_{gs}, resonant inductor current I_{Lr}, clamping capacitor current I_{Cc} and drain-source voltage V_{ds} in Sector I-I. Case I commutation is shown in purple, while Case II commutation is shown in red.

during a switching cycle. The current across the auxiliary switch is $i_{S7} = -I_{Lr}$ and $V_{bus} = V_{dc} + V_{Cc}$. The equivalent circuit of the initial stage is shown in Fig. 5(a).

Stage 2 ($t_1 - t_2$): First Resonance.

When S_7 is turned-off, L_r discharges the parallel capacitors C_4, C_6, C_2 and resonates V_{bus} to zero. The time duration for this resonance corresponds to the resonant fall time t_{fr}. As the circuit is no longer in state vector V7 (111), L_r resonates the voltage across S_7 to $V_{dc} + V_{Cc}$ with I_{Lr} remaining negative. The equivalent circuit of this stage is shown in Fig. 5(b).

Stage 3 ($t_2 - t_4$): Freewheeling Diodes.

After the first resonance, L_r still has residual energy to keep I_{Lr} negative. Freewheeling body diodes D_4, D_6 and D_2 begin to conduct and ZVS is realized for S_6 and S_2. The resonant inductor current I_{Lr} reaches zero at t_3 and the freewheeling diodes are turned-off. The motor currents at phase b (i_b) and phase c (i_c) now commutate the diodes D_3 and D_5 to S_6 and S_2. I_{Lr} is now equivalent to $i_b + i_c$ at t_4. The equivalent circuit for this scenario is depicted in Fig. 5(c).

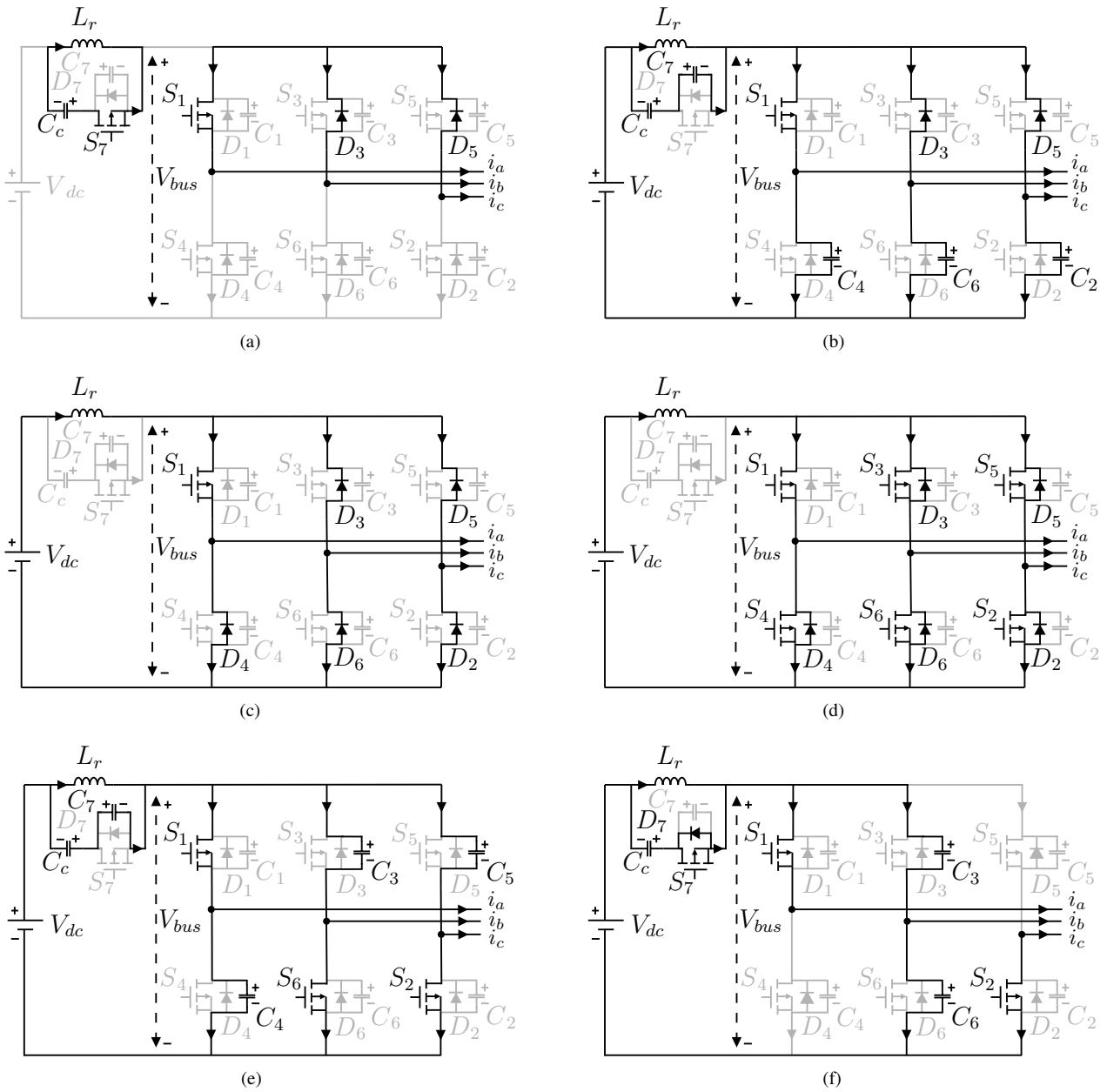


Fig. 5. Equivalent circuits of all main stages. (a) Stage 1 - initial stage ($t_0 - t_1$) (b) Stage 2 - first resonance ($t_1 - t_2$). (c) Stage 3 - freewheeling diode ($t_2 - t_4$). (d) Stage 4 - short-circuit ($t_4 - t_5$). (e) Stage 5 - second resonance ($t_5 - t_6$). (f) Stage 6 - Case I commutation (t_7).

Stage 4 ($t_4 - t_5$): Short Circuit.

At t_4, all six main switches are turned-on, entering the short-circuit mode. During this stage, L_r stores energy for the ZVS turn-on of S_7. This results in I_{Lr} increasing linearly by the boost current i_{boost}, whereas the voltage V_{Lr} across the inductor is clamped to V_{dc}, which is necessary for achieving ZVS. The equivalent circuit for this scenario is depicted in Fig. 5(d).

Stage 5 ($t_5 - t_6$): Second Resonance.

At t_5, S_4, S_3 and S_5 are turned-off, and the energy stored in L_r discharges V_{Cc}, resonating C_4, C_3, C_5 and C_7. The time duration for this resonance corresponds to the resonant rise time t_{rr}. This stage ends when S_7 is turned-on under ZVS conditions. The equivalent circuit for this scenario is depicted in Fig. 5(e).

Stage 6 (t_7/t_8): Case I Commutation.

At t_7, S_6 is turned-off and i_b initiates the charging of C_6. Subsequently, C_3 is discharged as S_3 is turned-on. Following the buffer of the resonant capacitor, ZVS is achieved. Similarly at time t_8, S_2 is turned-off and S_5 is turned-on through the parallel capacitors, as shown in Fig. 2(a). The time required for charging and discharging of parallel capacitors is given by the natural rise and fall time t_n. The equivalent circuit corresponding to this process at time t_7 is shown in Fig. 5(f). Following this stage, the inverter returns to Stage 1 of a new vector switching cycle.

III. Resonant Parameter Design

Following an overview into the control of the inverter, it has been established that ZVS is possible through the resonant action of L_r and C_r. The selection of these parameters has been discussed in the literature [29]. Also, the principle of actively profiling $\mathrm{d}v/\mathrm{d}t$ to not excite cable antiresonance has been extensively discussed [23]. However, in the ZVS inverter, the rise and fall times of the resonant stages (Stages 2 and 5) and natural commutation (Stage 6) are not the same value, i.e., $t_{rr} \neq t_{fr} \neq t_n$. To address this, the selection of L_r and C_r to profile $\mathrm{d}v/\mathrm{d}t$ at each type of commutation of the ZVS inverter so as to mitigate motor overvoltage is discussed next.

A. Selection of the Resonant Inductor L_r

The resonant inductor is designed to charge and discharge the resonant capacitors in the resonant stages by storing energy. From this viewpoint, the inductance should be as large as possible. However, it is preferable to limit its value to reduce capital costs, inverter losses and volume. During the resonant stages, the maximum $\mathrm{d}v/\mathrm{d}t$ of the main switches is analyzed using Kirchhoff's voltage law [29] as follows:

$$\frac{\mathrm{d}}{\mathrm{d}t}v_{fr\_\max} = \frac{V_{dc}}{\sqrt{L_r C_{rt}}} \tag{1}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}v_{rr\_\max} = \frac{V_{dc}}{\sqrt{L_r C_{rt}}} - \left[\frac{\sqrt{3} i_{m\_\max}}{2C_{rt}} + \frac{3 m_i i_{m\_\max}}{2C_{rt}}\right] \tag{2}$$

whereby m_i is the modulation index and $i_{m\_\max}$ is the maximum motor phase current. The resonant fall voltage is denoted as v_{fr} and the resonant rise voltage as v_{rr}. Assuming that all the parallel resonant capacitors have the same capacitance value, i.e. $C_r = C_1 = C_3 = C_5 = C_4 = C_6 = C_2 = C_7$, the total resonance capacitance is $C_{rt} = 4(C_r + C_{oss})$, where C_{oss} is the output capacitance (for this paper, the value for the SiC MOSFET Wolfspeed C2M0080120D is used, with a value of 92 pF [31]).

Since the maximum voltage across the main switches is $V_{dc} + V_{Cc}$, and assuming the rise times of both resonant commutations are not the same value, using (1), L_r based off the falling commutations is designed using

$$L_r = \frac{1}{C_{rt}}\left(\frac{V_{dc} t_{fr}}{V_{dc} + V_{cc}}\right)^2 \tag{3}$$

The resonant inductance can also be determined by the rising commutations; however, as later described in Section III-C, only the falling commutations are required for this.

B. Selection of the Resonant Capacitor C_r

During natural commutation in Case I, the appropriate configuration of the corresponding voltage slew rate $\mathrm{d}v_n/\mathrm{d}t$ is dependent on the charging and discharging characteristics of C_r at each main switch. Fig. 4 illustrates that the drain-source voltage V_{ds} fluctuates in response to the charging and discharging rate of C_r. Evaluation of $\mathrm{d}v_n/\mathrm{d}t$ across each main switch is conducted using Kirchhoff's first law:

$$\frac{\mathrm{d}}{\mathrm{d}t}v_n = \pm\frac{i_m}{2(C_r + C_{oss})} \tag{4}$$

whereby the sign changes represent the charging and discharging of the resonant capacitors. Since the SVPWM has been modified to allow for two concurrent commutations, the maximum motor current is $\frac{\sqrt{3}}{2} i_{m\_\max}$ with respect to the conventional SVPWM [29]. The natural commutation voltage slew rates using $i_{m\_\max}$ are found as

$$\frac{\mathrm{d}}{\mathrm{d}t}v_n = \pm\frac{\sqrt{3} i_{m\_\max}}{C_{rt}} \tag{5}$$

With the specified rising times t_n and the maximum phase current of the modified space vector, C_r is determined from (5) as

$$C_r = \frac{\sqrt{3} t_n i_{m\_\max}}{4(V_{dc} + V_{Cc})} - C_{oss} \tag{6}$$

C. Design Procedure for Overvoltage Mitigation

The relationship between motor overvoltage and the propagation delay t_p is depicted in Fig. 6 with t_p given as a function of cable length l [32]:

$$t_p = l\sqrt{L_{cab} C_{cab}} \tag{7}$$

whereby L_{cab} is the cable inductance and C_{cab} is the cable capacitance. These parameters are experimentally determined using a precision LCR meter [33] or measured directly as shown in Section V. It is important to note that (7) assumes a lossless cable and factors such as cable resistance can have a slight indirect effect on t_p, particularly at high frequencies. Therefore, accurate simulation modeling of the cable, as mentioned in Section IV, is crucial.

It is observed from Fig. 6 that the overvoltage oscillations can effectively be suppressed by designing the rise times to $4t_p$, with t_p being determined by the specific cable length and its inherent characteristics. As shown in Fig. 6(d), the motor voltages V_m no longer fully neutralize one another at $5t_p$, resulting in an overvoltage despite the longer rise time. Thus, complete suppression of V_m occurs when the inverter voltage V_i does not excite the cable antiresonance, and

$$t_r = 4at_p \tag{8}$$

where $a \in \mathbb{Z}^+$. This phenomenon is explained by the superposition principle, where V_i is divided into two equal pulses with a temporal time displacement of $2t_p$. Given the assumption of unity reflection coefficients [18], both inverter voltages are reflected at twice the magnitude at the motor terminals. Due to the time displacement, the resultant motor voltages cancel each other at $4at_p$ [23].

To ensure consistent suppression of overvoltage in the ZVS inverter, the rise and fall times at each resonant and natural commutation must be carefully selected. As noticed from

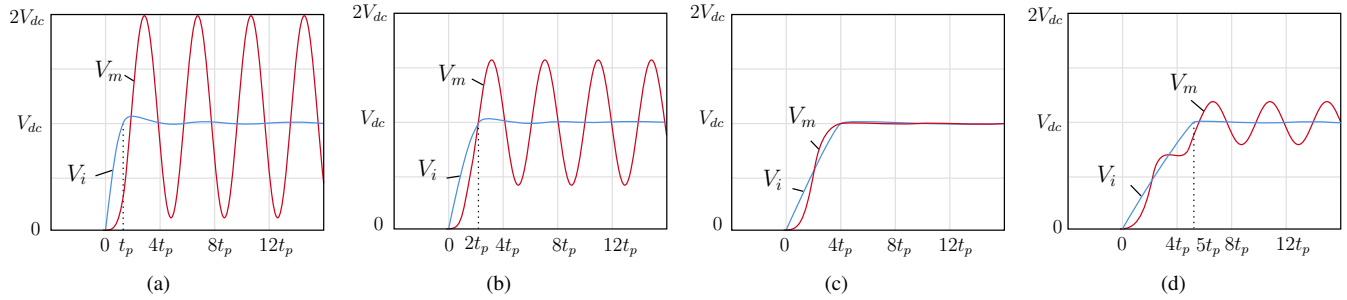


Fig. 6. Drive system inverter voltage V_i and motor voltage V_m at increasing rise times for cable propagation time t_p = 65 ns. (a) t_p. (b) $2t_p$. (c) $4t_p$. (d) $5t_p$. (Simulation study representing PWM source of varying rise times feeding into 15 m ac cable with the motor-side represented as an open circuit.)

(1) and (2), the values of $\mathrm{d}v/\mathrm{d}t$ can not be equal without restricting V_{dc} or $i_{m\_\max}$, such that:

$$\left|\frac{\mathrm{d}}{\mathrm{d}t}v_{fr\_\max}\right| > \left|\frac{\mathrm{d}}{\mathrm{d}t}v_{rr\_\max}\right| \tag{9}$$

To this extent, the resonant rise $\mathrm{d}v_{rr\_\max}/\mathrm{d}t$ from (2) is denoted as a function of the resonant fall $\mathrm{d}v_{fr\_\max}/\mathrm{d}t$ from (1) and the natural $\mathrm{d}v_n/\mathrm{d}t$ from (5) with a modulation index $0.4 \leq m_i \leq 0.8$ as follows:

$$\begin{aligned}\frac{\mathrm{d}}{\mathrm{d}t}v_{rr\_\max} =& \frac{V_{dc}}{\sqrt{L_r C_{rt}}} - \left[\frac{\sqrt{3}i_{m\_\max}}{2C_{rt}} + \frac{3m_i i_{m\_\max}}{2C_{rt}}\right] \\ =& \frac{\mathrm{d}}{\mathrm{d}t}v_{fr\_\max} - \frac{\mathrm{d}}{\mathrm{d}t}v_n\left[\frac{1}{2}\left(1+\sqrt{3}m_i\right)\right] \\ \approx& \frac{\mathrm{d}}{\mathrm{d}t}v_{fr\_\max} - \frac{\mathrm{d}}{\mathrm{d}t}v_n\end{aligned} \tag{10}$$

From (10), it is observed that the $\mathrm{d}v/\mathrm{d}t$ can be profiled by carefully selecting the rise time at each commutation. This is possible since the change in PWM voltage magnitude at each commutation has the same value (i.e., $V_{dc} + V_{Cc}$). The rise time selection for each $\mathrm{d}v/\mathrm{d}t$ is mathematically expressed as follows:

$$\underbrace{\frac{\mathrm{d}}{\mathrm{d}t}v_{rr\_\max}}_{t_{rr}=8t_p} \approx \underbrace{\frac{\mathrm{d}}{\mathrm{d}t}v_{fr\_\max}}_{t_{fr}=4t_p} - \underbrace{\frac{\mathrm{d}}{\mathrm{d}t}v_n}_{t_n=8t_p} \tag{11}$$

To ensure effective overvoltage suppression, it is imperative first to establish C_r as given in (6) utilizing $t_n = 8t_p$. Subsequently, L_r can be calculated using the established capacitance and inductance from (3). Finally, t_{fr} should be set to $4t_p$. As per (1), by setting a constraint on the maximum rise time, this will enable t_{rr} to be equal to $8t_p$. By following this methodology, complete overvoltage suppression can be achieved at both the resonant and natural rise times. A diagram outlining this process is illustrated in Fig. 7.

D. Voltage and Current Stress on Main Switches

Assuming that all the parallel resonant capacitors are of the same value, the minimum i_{boost} is expressed as [34]

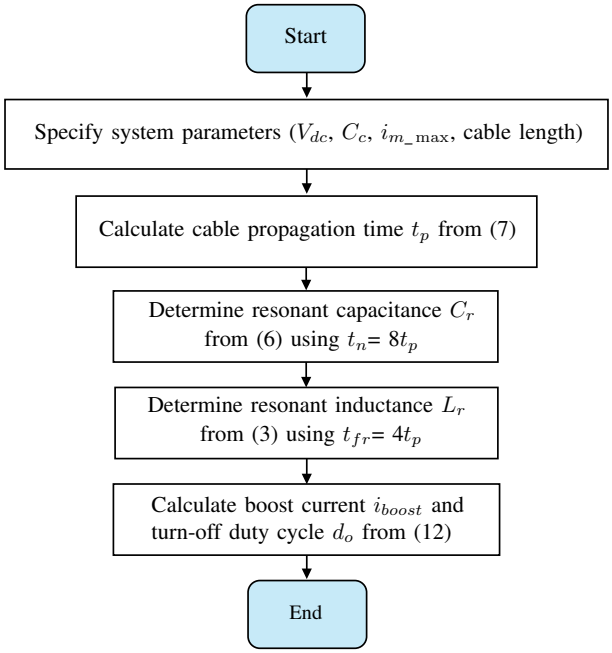


Fig. 7. Guideline procedure for determining the resonant parameters of the ZVS inverter.

$$i_{boost} \geq \sqrt{\left(\frac{V_{dc}^2 - V_{Cc}^2}{Z_r^2} - 2i_{m\_\max}\right)^2 - \frac{V_{dc}^2 - V_{Cc}^2}{Z_r^2}} \tag{12}$$

where the resonant impedance is defined as $Z_r = \sqrt{L_r/C_{rt}}$. When the inverter is operating at steady state, the clamping capacitor voltage V_{Cc} is defined by the volt-second balance principle of the resonant inductor as follows:

$$V_{Cc} = \frac{d_o}{1-d_o}V_{dc} \tag{13}$$

whereby d_o is the turn-off duty cycle of S_7.

Since the voltage across the main switches is $V_{dc} + V_{Cc}$, to avoid high voltage stress, d_o should be less than 0.1 [34].

The current I_{Lr} of the resonant inductor [27] is given by

$$I_{Lr}(t_3) = \sqrt{\frac{V_{dc}^2 - V_{Cc}^2}{Z_r^2} + i_{boost}^2} + i_m \approx \frac{V_{dc}}{Z_r} + \sqrt{3}i_m m_i \tag{14}$$

When calculating the resonant parameters for a system, it is essential to consider the value of Z_r to prevent excessive current stress on the power switches. The current stress at the auxiliary switch ($i_m + I_{L_r}$) and main switches ($i_m + i_{boost}/3$) is calculated using (12) and (14). Since the current stress can be limited by increasing the value of Z_r [27], the design for overvoltage mitigation must consider Z_r or increase the current rating of the auxiliary and main switches. One way to accomplish this is to increase the value of L_r with respect to C_r. Specifically, a different set of resonant rise and fall time requirements can be chosen as long as t_r in (8) is met for all natural and resonant commutations. Adherence to this condition ensures that the voltage does not cause excitation of the cable antiresonance. Neglecting the influence of Z_r may give rise to MOSFET malfunctioning, particularly in extended utilization periods, potentially incurring higher expenses in maintenance and replacement.

E. Volume Considerations

The volume of the primary components in the ZVS inverter is depicted in Fig. 8. A comparison between a conventional two-level inverter with a passive LCR filter, RC filter and a conventional three-level inverter is also shown. The selection of passive components was based on the system specifications, which included the $\mathrm{d}v/\mathrm{d}t$ requirements for a 1.23 kW AC permanent magnet brushless servo motor operating at a switching frequency of 20 kHz and a dc voltage of 300 V.

The sizing of the heat sink, influenced by natural air convection, relies on calculating the thermal resistance of the heat sink. This calculation incorporates the simulated power losses, as computed in Section IV-B, along with the heat sink temperature obtained from PLECS simulations. For these computations, an ambient temperature of 40°C was considered [35]. Subsequently, the heat sink volume can be determined, as discussed in [36]. This process involves employing curve fitting techniques to establish a correlation between the volume of various extruded heat sinks and their corresponding heat sink thermal resistances. Additionally, for all active switches, the packaged DYNATRON heat sink and cooling fan (Part No. G199) [37] are employed to ensure effective heat dissipation.

The ZVS inverter and two-level with LCR filter utilizes ferrite leaded inductors from Würth Elektronik [38], whereas the two-level filter inverters uses low-inductive 100 Ω resistors from Ohmite [39]. Additionally, 10 nF polypropylene film capacitors from Panasonic [40] are utilized in both the ZVS inverter and passive filters. The volume of each component was determined based on the dimensions specified in their respective datasheets. Only basic LCR and RC passive filter were implemented in this study; however, comprehensive information on more advanced filters is available in the literature [16].

The ZVS inverter exhibits a volumetric reduction of ≈30% compared to the three-level inverter and ≈40% reduction compared to the two-level inverter with an LCR and RC filter. It is also worth reminding that the LCR passive filter is typically installed at the inverter terminal, where the RC passive filter is installed at the motor terminal. Moreover, determining the size

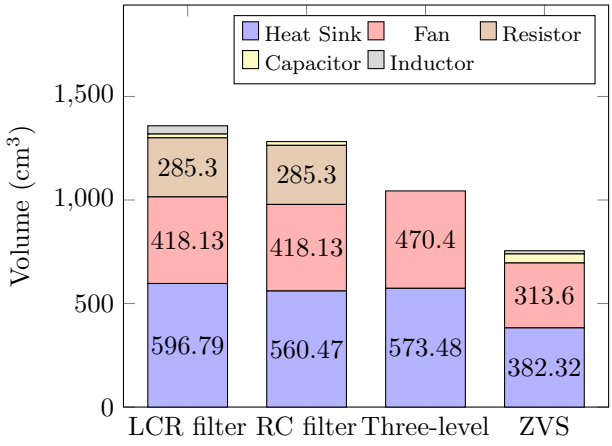


Fig. 8. Volume comparison of main components of conventional two-level inverter with a passive LCR and RC filter, Q3L T-type inverter and ZVS inverter. The total volumes of the inverter (including the resonant inductor and capacitance) are correspondingly 1358.45, 1282.13, 1043.88 and 742.54 cm^3. These values increase to 1359.7, 1283.4, 1046.4 and 743.8 cm^3 when the gate drivers (Texas Instruments ISO5452-Q1) are accounted for.

TABLE I
SYSTEM PARAMETERS

Parameter	Value	Parameter	Value
V_{dc}	300 V	R_{g-in}	3.9 Ω
C_c	10 μF	R_{g-ex}	2.5 Ω
f	50 Hz	$R_{ds(on)}$	80 mΩ
f_{sw}	20 kHz	V_{ggh}	20 V
m_i	0.8	V_{ggl}	-5 V

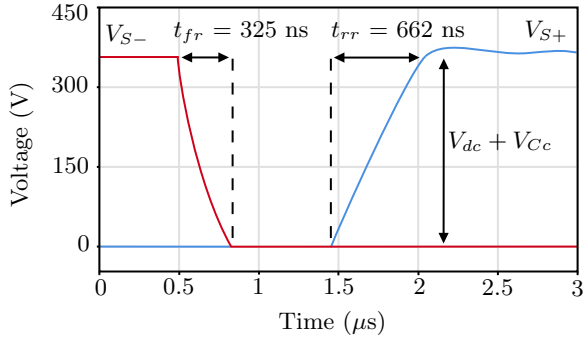
of C_c in the ZVS inverter is contingent upon the dc voltage stipulations to provide a constant voltage across its terminals in a switching period. Therefore, its practicality can be impacted by the availability of suitable constituent elements.

IV. SIMULATION RESULTS

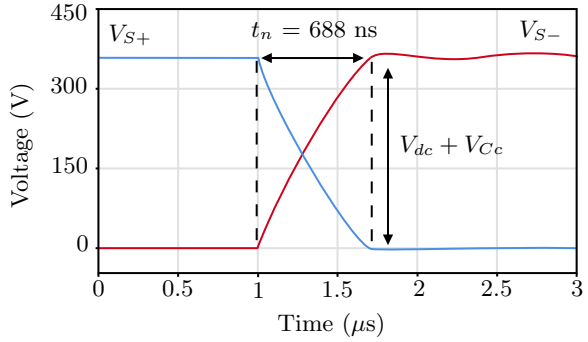
A simulation was carried out in MATLAB/Simulink to verify the effectiveness of the ZVS topology for overvoltage mitigation. A high-frequency ac cable and motor model was implemented from [33] to accurately model and predict the transient overvoltage oscillations. This cable model includes the impact of both the skin and proximity effects and the dielectric losses at high frequency range. A breakdown of the system parameters is given in Table I, which have been adopted for both software simulation and experimental testing. Experimental results are reported in Section V.

A. Overvoltage Mitigation Comparison

As shown in Section III-C, it is necessary to ascertain the optimal resonant and natural time t_r for every cable length employed to address the issue of overvoltage. The propagation time t_p for each cable length is presented in Table II, alongside the calculated values of C_r, L_r, and Z_r, which were obtained using the prescribed guidelines in Fig. 7. The values for C_r and L_r have been rounded to the nearest component commercially available. It is noticed that Z_r remains approximately the same value despite increasing the cable length. This is due to the ratio of C_r and L_r being the same since only t_p is varying. It



(a)



(b)

Fig. 9. ZVS commutation comparison of inverter voltages V_s with active $\mathrm{d}v/\mathrm{d}t$ profiling. (a) Resonant fall and resonant rise commutations. (b) Natural fall and natural rise commutations. (Simulation parameters: L_r = 9.10 μH, C_r = 2.64 nF, cable length = 20 m and t_p = 86.7 ns.)

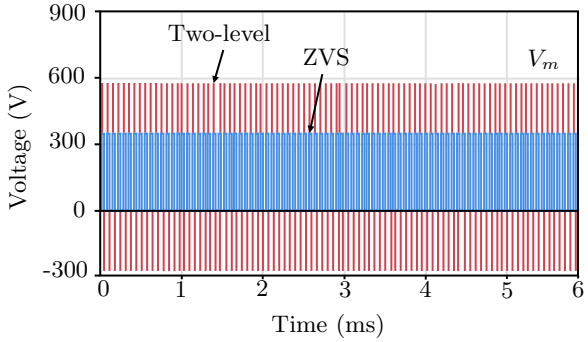
TABLE II
CABLE LENGTH AND RESONANT PARAMETERS

Cable length (m)	t_p (ns)	C_r (nF)	L_r (μH)	Z_r (Ω)
5	21.6	0.59	2.27	28.88
10	43.3	1.27	4.55	28.90
15	65.0	1.96	6.82	28.87
20	86.7	2.64	9.10	28.86

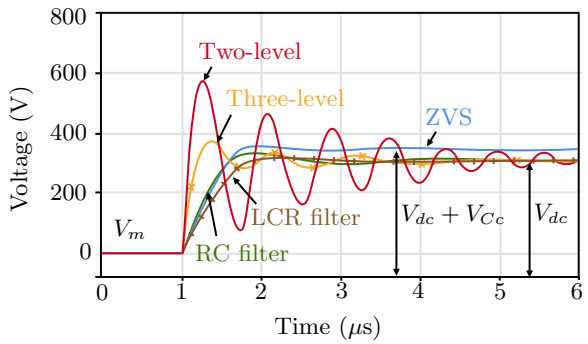
is worth highlighting that these parameters were determined based on the experimental dc voltage V_{dc} = 300 V and $i_{m\_\max}$ = 3 A. Changing these system parameters (i.e. load current) may slightly impact the motor overvoltage mitigation, as later shown in Section V-C.

The resonant rise and fall times for a single switching commutation are displayed in Fig. 9(a). As outlined in (9), it is imperative that the fall rate of voltage be greater than the rising rate of voltage. Hence, the rise time t_{rr} is chosen as $8t_p$, and the fall time t_{fr} is chosen as $4t_p$. Utilizing a measured value of t_p of 86.7 ns for a 20 m cable, the calculated resonant rise time and resonant fall time are 693.6 ns and 346.8 ns. Comparing these values with the simulated results reveals a disparity of $\approx 5\%$. Likewise, the natural commutations in Fig. 9(b) are designed to $8t_p$. Compared with the calculated rise times, a deviation of 1% results with regard to the simulated outcomes. These commutations are structured not to stimulate cable antiresonance, thereby mitigating overvoltage.

The performance of the ZVS topology was compared against the conventional two-level inverter with no passive $\mathrm{d}v/\mathrm{d}t$ filters and the same system parameters. As shown in



(a)



(b)

Fig. 10. Simulated motor voltage V_m comparisons. (a) Motor voltage comparing two-level inverter with no passive filter with the ZVS topology. (b) Extended view comparing two-level inverter with no passive filter, two-level with LCR and RC filter, Q3L T-type inverter and ZVS inverter. (Simulation parameters: L_r = 9.10 μH, C_r = 2.64 nF, cable length = 20 m and t_p = 86.7 ns.)

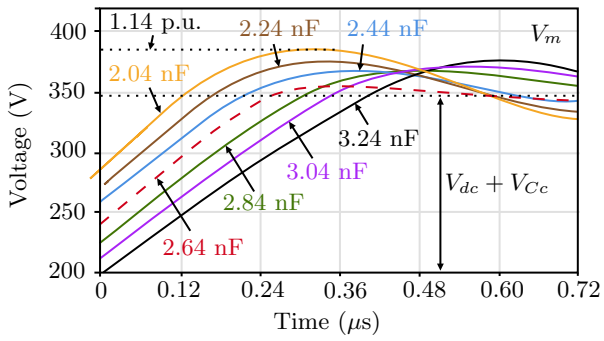


Fig. 11. Motor voltage V_m with variations in resonant capacitance C_r during natural rise commutation. (Simulation parameters: L_r = 9.10 μH, cable length = 20 m and t_p = 86.7 ns.)

Fig. 10(a), the phase voltage V_m of the two-level inverter has almost twice the value of the dc voltage V_{dc} at 560 V. This would result in rapid insulation failure impacting the long-term reliability of the motor. An extended view in Fig. 10(b) shows that by using the ZVS topology with active $\mathrm{d}v/\mathrm{d}t$ profiling, the motor overvoltage is fully mitigated to the inverter bus voltage $V_{dc} + V_{Cc}$ at 345 V. Significantly, the voltage $V_{i,ab}$ between phases a and b of the ZVS inverter is equivalent to $V_{dc} + V_{Cc}$ due to the presence of the clamping capacitor, thus enabling the motor overvoltage to subside to this increased voltage level.

It is worth noting that extended exposure to high temperatures or mechanical stress can lead to slight fluctuations in the values of C_r, which can influence the pre-determined rise and fall times, ultimately affecting overvoltage mitigation. Fig. 11 illustrates the simulated relationship between C_r and V_m for a 20 m cable, revealing that V_m increases up to 1.14 p.u. when C_r deviates from the optimal value of 2.64 nF. While variations in L_r can also impact V_m, its effect is less significant, particularly if L_r does not deviate considerably from its ideal value. Moreover, these variations in L_r only affect resonant commutations and not natural commutations.

Furthermore, passive components may undergo gradual aging effects over extended periods, contingent on factors such as component quality, construction, and operating conditions. To mitigate the risks associated with aging phenomena, it is advisable to opt for components with appropriate tolerances and perform regular inspections and replacements.

B. Efficiency Comparison

The switching and conduction losses of the inverter were determined using PLECS based on parameters in the Wolfspeed C2M0080120D datasheet [31]. This includes the internal gate resistance (R_{g-in}), external gate resistance (R_{g-ext}) and normally on-state resistance ($R_{ds(on)}$). The gate drive voltage is set as -5/20 V during turn-off (V_{ggl}) and turn-on (V_{ggh}). The critical parameters are extracted from the datasheet and further detailed in Table I. By using manufacturer data, multi-dimensional look-up tables were employed to accurately estimate and average the losses with case temperature T_c = 40°C. The system efficiency η_{sys} was also calculated through software simulation using

$$\eta_{sys} = \frac{P_{in} - \left(P_{inv} + P_{mot} + P_{cable}\right)}{P_{in}} \times 100 \qquad (15)$$

where P_{in} is the dc input power, P_{inv} is the total inverter losses, P_{mot} is the total motor losses and P_{cable} is the total cable losses.

The efficiency of a drive system utilizing a Q3L T-type inverter and a two-level inverter with passive LCR and RC filters are compared in Fig. 12. The results show that the ZVS topology exhibits a higher system efficiency for all power ratings. The improved efficiency is primarily attributed to the reduced number of active switches compared to the three-level inverter, resulting in lower switching and conduction losses for the SiC MOSFET inverter. However, the two-level inverter experiences substantial power losses due to the bulky LCR and RC filters and the hard-switching technique required, as demonstrated at rated conditions in Fig. 13. Specifically, the switching turn-on losses are evident in the hard-switching inverters, whereas in the ZVS inverter, these losses are absent.

Although the inverter analyzed in this study operates at a switching frequency of 20 kHz, at higher frequencies up to 300 kHz, the turn-on losses would become the dominant source of loss in the system, as reported by previous literature [27]. Furthermore, it should be noted that while the simulated comparison is performed at a dc link voltage of 300 V, the results can be extended to higher voltages with a similar

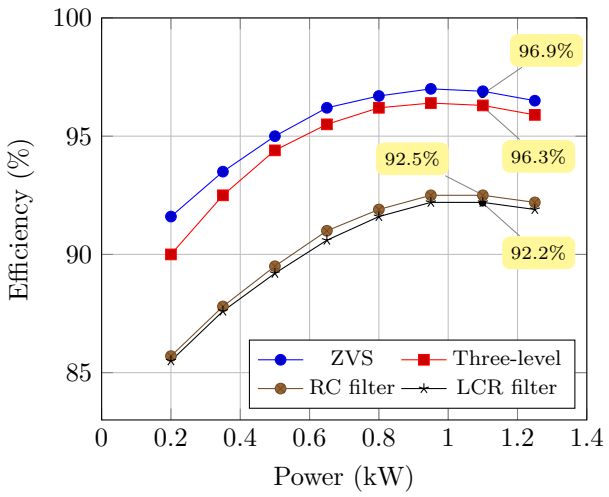


Fig. 12. Simulated system efficiency of ZVS motor drive system compared with Q3L T-type inverter, two-level inverter with passive LCR and RC filter. (t_p = 86.7 ns, f_{sw} = 20 kHz, m_i = 0.8.)

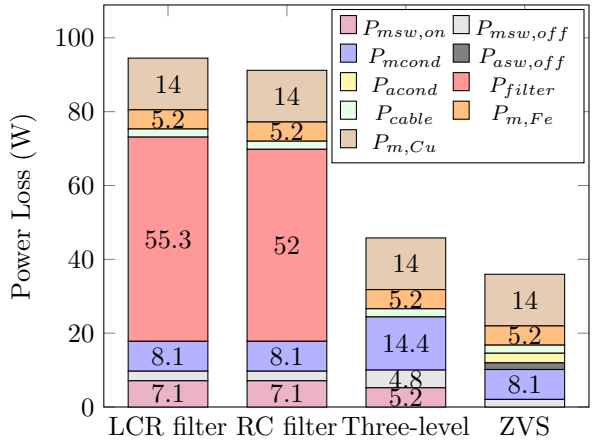


Fig. 13. Power loss distribution comparison of two-level inverter with passive LCR and RC filter, Q3L T-type inverter and ZVS inverter. $P_{msw,on}$, $P_{msw,off}$ and P_{mcond} are the turn-on, turn-off switching losses and conduction loss of the main switches. $P_{asw,off}$ and P_{acond} are the switching turn-off and conduction power loss of the auxiliary switch. P_{filter} is the filter power loss. $P_{m,Fe}$ and $P_{m,Cu}$ are the motor iron and copper losses. The total power losses of the motor drive system are correspondingly 91.5 W, 88.2 W, 45.8 W and 36.0 W. (Simulation parameters: load torque T_L = 4 Nm, rotor speed ω_r = 3000 rpm, f_{sw} = 20 kHz and t_p = 86.7 ns.)

outcome. When operating at higher voltages, the load currents are expected to increase, which, in turn, leads to higher losses in both the inverter topologies and passive filters. A relevant study in [26] conducted a comparable loss analysis between a hard switching two-level inverter and the ZVS inverter at 600 V. The findings from the study reaffirmed the superior efficiency of the ZVS inverter at higher voltages.

During a ZVS turn-off transition, the voltage gradually increases from zero whilst the current quickly drops. This results in the switching losses being reduced when compared with a hard-switching inverter. In the ZVS inverter, C_r can systematically control the voltage slew rate. Therefore, by reducing the $\mathrm{d}v/\mathrm{d}t$, the switching turn-off losses $P_{sw,off}$ can be reduced [41]. This is shown in Fig. 14, where $P_{sw,off}$ was

TABLE III
TOTAL ZVS TURN-OFF POWER LOSS AT 20 KHZ

Cable ($8t_p$)	1 m (34.4 ns)	5 m (172.8 ns)	10 m (346.4 ns)	15 m (520 ns)	20 m (693.6 ns)
Power loss (W)	3.88	3.85	3.63	2.75	2.50
Efficiency	96.89%	96.89%	96.91%	96.98%	97.00%

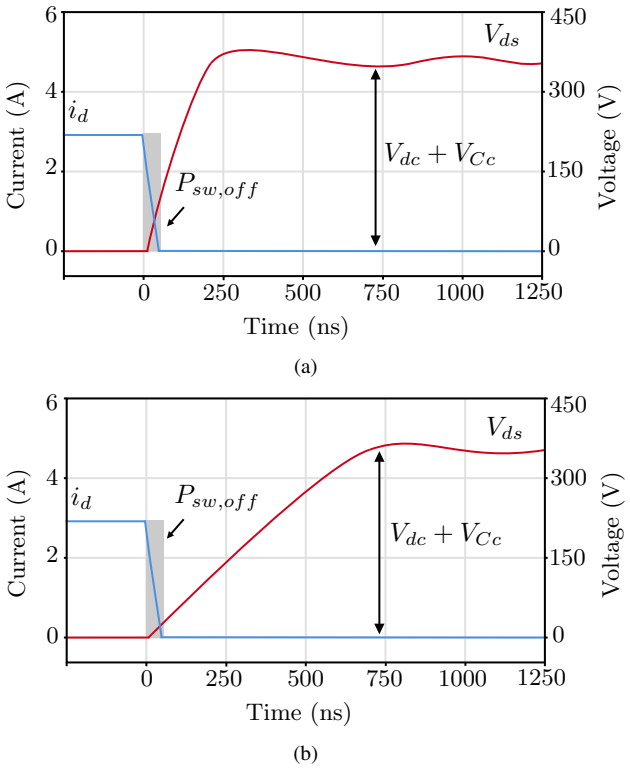


Fig. 14. Simulated ZVS switching turn-off waveforms at different rise times showing the turn-off losses $P_{sw,off}$. (a) Switching waveforms with actively profiled natural fall times for a 5 m cable. (b) Switching waveforms with actively profiled natural fall times for a 20 m cable.

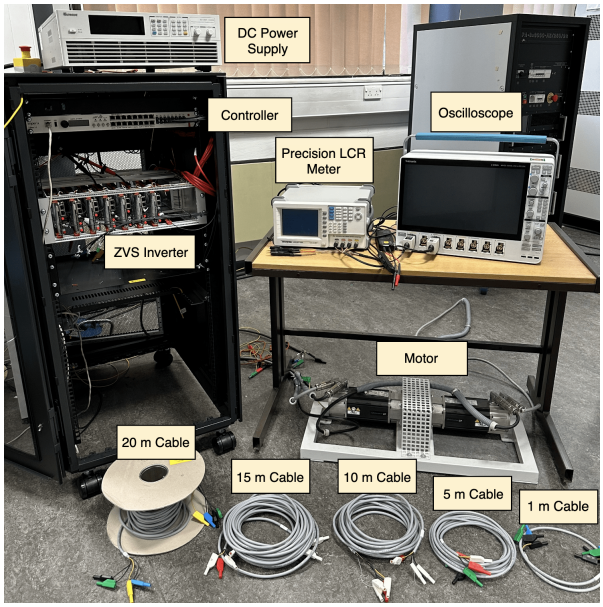


Fig. 15. Experimental test bench of ZVS inverter and cable-fed motor.

calculated as the product of the MOSFET drain current i_d and V_{ds}. However, it is imperative to meticulously weigh the benefits and drawbacks of the preferred performance metrics at a high-switching frequency and the ideal efficiency to ascertain the most favourable voltage rise time for the ZVS inverter.

Although the ZVS inverter exhibits negligible switching turn-on losses, an additional turn-off loss results from adding the short-circuit stage. Thus, comprehending the significance of $P_{sw,off}$ for slower $\mathrm{d}v/\mathrm{d}t$ is crucial. By employing the propagation times associated with cable length, the correlation between voltage rise time $8t_p$, $P_{sw,off}$ and η_{sys} is listed at rated motor conditions in Table III. The 1 m cable was only used as a base comparison with no $\mathrm{d}v/\mathrm{d}t$ profiling, as the overvoltage phenomenon does not occur at this cable length.

The primary factors contributing to power loss in ac cables are attributable to the dielectric and resistive phenomena, specifically the skin and proximity effects. It is important to note that as the system operates at higher switching frequencies and longer cable lengths, these losses become more significant and can greatly impact the overall system efficiency [42]. Additionally, copper and iron losses of L_r have been accounted for; however, they are considered negligible at the current inverter ratings in this study.

V. EXPERIMENTAL RESULTS

To confirm the suitability of the presented ZVS parameter selection for mitigating motor overvoltage, a three-phase ZVS inverter is employed to deliver power to a motor via a range of long cables; 5 m, 10 m, 15 m and 20 m, as shown in Fig. 15. In line with this configuration, a four-core unscreened 16 AWG cable from Lapp [43] was employed with the earth core grounded. This provides a return path for common-mode currents, reducing the EMI within the cable and minimizing interference with surrounding equipment and circuits. The motor rotor angle is measured by an incremental encoder and processed by the DSP (Xilinx Zynq 7030 SoC). The driving signals are generated from the DSP and sent to the gate drive circuit (Texas Instruments ISO5452-Q1). The gate driver controls the rise and fall times for the active SiC MOSFET power switches (C2M0080120D) with SiC Schottky diodes (C4D20120D).

A. Impact of Cable Length

By selectively adjusting the resonant parameters, it is possible to achieve the desired $\mathrm{d}v/\mathrm{d}t$ for natural and resonant commutations as a function of cable length whilst conforming to (8), thereby mitigating motor overvoltage at each switching transition. The controlled $\mathrm{d}v/\mathrm{d}t$ through the ZVS inverter is illustrated in Fig. 16 by utilizing the parameters outlined in

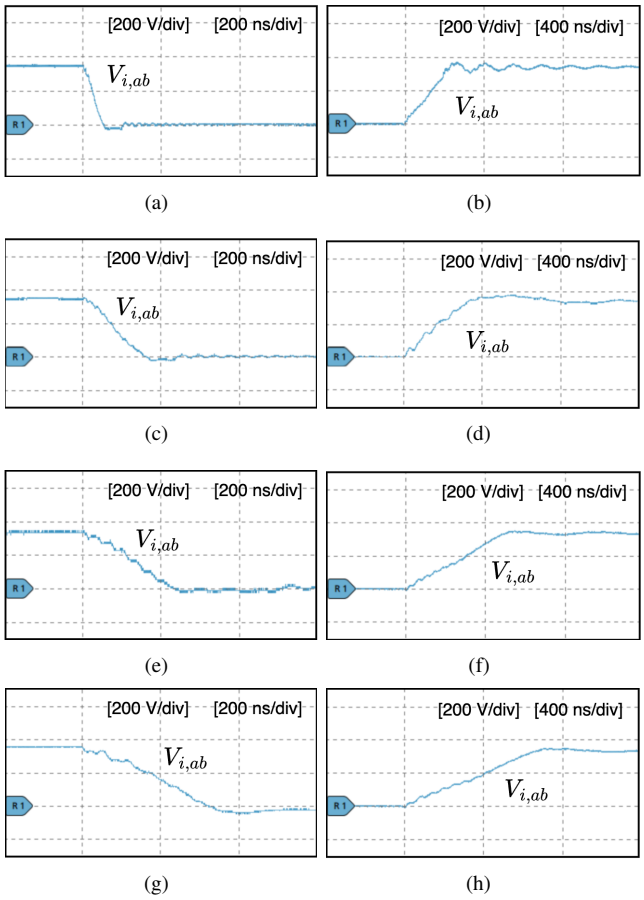


Fig. 16. Experimental inverter switching waveforms of resonant fall ($4t_p$) and resonant rise ($8t_p$) showing the actively profiled $\mathrm{d}v/\mathrm{d}t$ for each cable length. (a)-(b) Cable length = 5 m. (c)-(d) Cable length = 10 m. (e)-(f) Cable length = 15 m. (g)-(h) Cable length = 20 m.

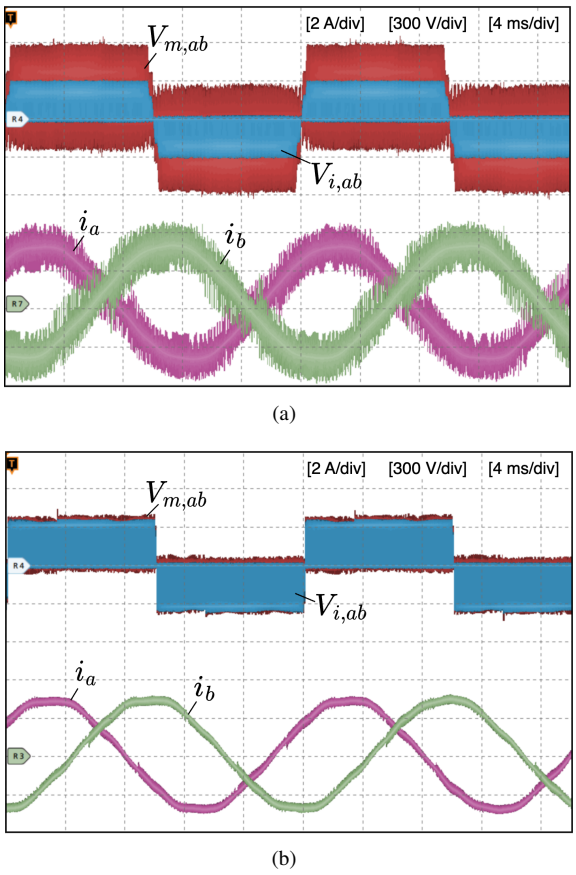


Fig. 17. Differential-mode motor-side voltage $V_{m,ab}$, inverter-side voltage $V_{i,ab}$ and two motor phase currents with a cable length of 20 m. (a) Hard-switching two-level inverter. (b) ZVS inverter.

Table II. As shown in Fig. 16(a) and Fig. 16(g), an increase in cable length results in a proportional increase in both natural commutation and resonant rise commutations, with a rise time of $\approx 8t_p$ and resonant fall times of $4t_p$ for each cable length. Upon comparison of the measured resonant fall times at a cable length of 20 m with the simulated value of 325 ns, a discrepancy of 7% is observed. Similarly, the simulated resonant rise times are 662 ns, which exhibits a deviation of 4% when compared to the measured values.

Fig. 17 compares the differential-mode inverter voltage $V_{i,ab}$ between phases a and b with the motor overvoltage $V_{m,ab}$ when a 20 m cable is adopted. A hard-switching two-level inverter without a filter is used as a baseline for comparison by short-circuiting the auxiliary branch and removing C_r. The measured rise and fall times for the two-level inverter with no filter are 52 ns and 31 ns correspondingly. As shown in Fig. 17(a), $V_{m,ab}$ can increase up to 2 p.u. If the motor and cable are not designed to withstand this voltage magnitude, the resulting overvoltage can exceed the partial discharge inception voltage of the rotor winding, leading to partial discharges that may significantly decrease the motor's operational lifespan. Thus, the motor voltage reflections persist until fully damped to the inverter PWM voltage. This effect depends on the ac skin resistance, proximity effects, and dielectric losses of the ac cable [33]. Additionally, the occurrence of high-frequency ac current ripple during switching transients is due to the charging and discharging of the cable's parasitic capacitance, caused by the high $\mathrm{d}v/\mathrm{d}t$ of the PWM voltage pulses.

Conversely, as illustrated in Fig. 17(b), utilizing the ZVS inverter and adopting appropriate parameter selection can almost alleviate the motor overvoltage. Moreover, the motor phase current exhibits reduced current ripple compared to the hard-switching two-level inverter, which can be attributed to the regulated $\mathrm{d}v/\mathrm{d}t$ and increased rise time of the ZVS inverter. It is also seen that the overvoltage frequency of the reflected wave is 143.6 kHz, which agrees with the calculated reflected wave frequency for a 20 m cable [44]:

$$f_{rw} = \frac{1}{4lt_p} = 144.2 \text{ kHz} \tag{16}$$

The mitigation of motor overvoltage is further assessed with Fig. 18, which shows an extended view for a 20 m cable. Upon analyzing the hard-switching two-level motor drive system in Fig. 18(a), it is evident that the maximum motor overvoltage during the rising edge is 1.9 p.u., while during the falling edge it is 1.8 p.u. These results are consistent with the simulated outcomes, which exhibit a peak overvoltage of 1.9 p.u., as shown in Fig. 10(b). In contrast, as seen in Fig. 18(b), the ZVS inverter technique effectively mitigates motor overvoltage.

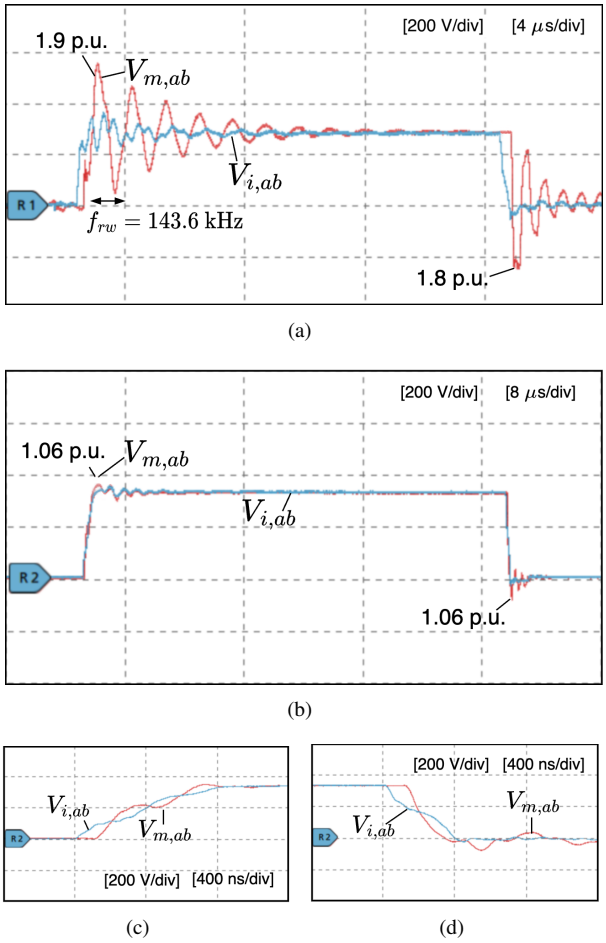


Fig. 18. Differential-mode motor-side voltage $V_{m,ab}$ and inverter-side voltage $V_{i,ab}$ with a cable length of 20 m. (a) Hard-switching two-level inverter. (b) ZVS Inverter. (c) Extended view of ZVS inverter showing natural rise ($8t_p$). (d) Extended view of ZVS inverter showing resonant fall ($4t_p$).

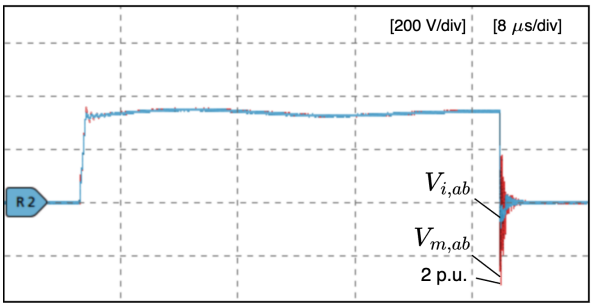


Fig. 19. Motor voltage $V_{m,ab}$ when only resonant rise commutation ($8t_p$) is actively profiled using 20 m cable.

This behavior can be explained further in Figs. 18(c)-(d), where the motor voltage closely follows the analytical results presented in Fig. 6. The natural rise commutation design, set at $8t_p$, leads to three intersections between $V_{m,ab}$ and $V_{i,ab}$. On the other hand, the resonant fall commutation, selected as $4t_p$, results in a single intersection between $V_{m,ab}$ and $V_{i,ab}$, as depicted in Fig. 6(c). To note, the time difference between $V_{m,ab}$ and $V_{i,ab}$ is the propagation time t_p. This is measured at 87 ns, which is in agreement with the calculated value of 86.7 ns for a 20 m cable using (7).

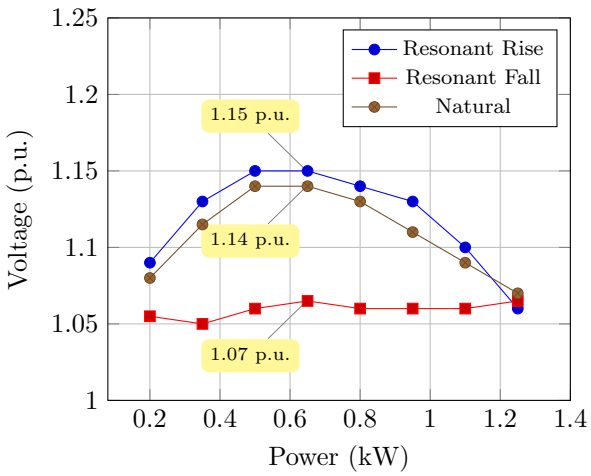


Fig. 20. Measured motor overvoltage for the different types of commutations when output power deviates from rated power using a cable length of 20 m.

B. Actively Profiling One Type of Commutation

Drawing on previous literature on the ZVS topology [29], regulating the $\mathrm{d}v/\mathrm{d}t$ of switching transitions can enable active profiling of a specific type of commutation. However, this method is limited to a single type of commutation, and actively profiling one type does not guarantee the profiling of the other two commutations. This limitation is shown in Fig. 19, where only the rising resonant commutations have been actively profiled to $8t_p$. This results in a motor overvoltage of 2 p.u.

Despite active profiling of one type of commutation, as in the shown example, long-term motor winding damage may still occur since the other two commutations still need to be profiled. The presented motor overvoltage mitigation approach addresses this problem by profiling all three types of commutations.

C. Variations in Load Conditions

It is crucial to consider the effects of motor overvoltage when the rise and fall times deviate from their optimal values. This can occur when there is a substantial reduction in output capacity from rated conditions including variations in load current. Fig. 20 illustrates the change in motor overvoltage for a 20 m cable when compared to deviations in output power from rated conditions. The results show that variations from optimal rise times can increase motor overvoltage more significantly at an output power of 0.6 kW than at 0.2 kW. This is because the rise time increases from $8t_p$ as the output power decreases from rated power. Specifically, at 0.6 kW, the rise time deviates from the optimal rise time, and no $\mathrm{d}v/\mathrm{d}t$ profiling occurs. At 0.2 kW, the rise time is around $12t_p$, and thus $\mathrm{d}v/\mathrm{d}t$ profiling occurs when (8) is met. In contrast, changes in loading conditions have minimal impact on falling resonant commutations, as evidenced by (1).

Despite their influence, alterations in load conditions have a negligible effect on overvoltage, as the maximum overvoltage with the presented method is limited to 1.15 p.u.

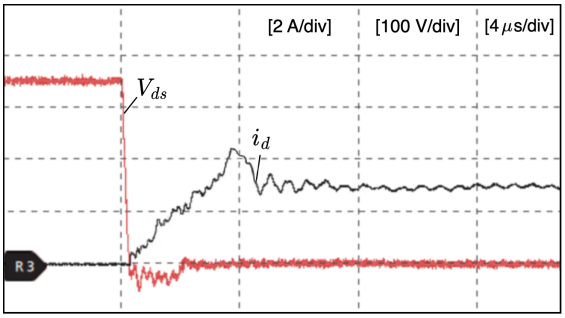


Fig. 21. MOSFET V_{ds} and i_d during turn-on switching transients.

D. Zero-Voltage Switching

The waveforms of V_{ds} and i_d during a switching transition in Sector I-I are shown in Fig. 21. It becomes apparent that ZVS is initiated, and the main switch is activated as i_d increases, following the clamping of V_{ds} to zero. The decrease in V_{ds} occurs at a rate actively controlled by both the resonant parameters and cable propagation time. This ZVS switching technique results in negligible switching turn-on losses compared to those incurred by a two-level hard-switching inverter.

VI. Conclusion

In SiC MOSFET cable-fed drives, motor overvoltage may arise as a result of high $\mathrm{d}v/\mathrm{d}t$. This can lead to substantial strain on cable and motor insulation, resulting from partial discharges and uneven voltage distribution. To alleviate this issue, this paper presented a parameter selection strategy of a ZVS SiC-based inverter.

The proposed strategy involves regulating the $\mathrm{d}v/\mathrm{d}t$ of each resonant and natural commutation to prevent the activation of cable antiresonance and mitigate overvoltage. The method requires carefully selecting resonant parameters based on the length of the cable and cable propagation time.

The performance of the inverter was assessed through theoretical analysis, software simulations, and experiments. In addition, the ZVS inverter was compared to conventional solutions, such as the three-level and two-level inverter with a passive RC filter. The results indicate that the ZVS inverter has lower losses and exhibits volume advantages. Furthermore, the ZVS inverter can effectively mitigate motor overvoltage, with limited impact when varying motor load conditions due to prolonged rise/fall times.

VII. Acknowledgement

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