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Quick VCSELs and Wafer Assessment for Volume MOVPE Production

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Abstract

This thesis details material and device characterisation in the volume MOVPE production of VCSELs, with a focus on understanding and minimising variation in the manufacturing process as the wafer diameter is increased.

The development of a Quick VCSEL (QuickSEL) process as a fast, efficient, and reliable quality control method in production settings is presented. Devices are fabricated within 24 hours and produce output characteristics which are comparable to that of standard planarised structures, intended for use in rapid prototyping of epitaxial designs and for the assessment of epi-wafer quality and uniformity in volume settings.

From post-growth material characterisation and wafer-scale device-level testing, the quality and uniformity of generic MOVPE-grown 6-inch GaAs substrate VCSEL wafers is assessed. Variation of the oxide aperture across wafers processed whole is shown to have a significant effect on the uniformity of device performance. Even when accounted for, some residual variation in device performance remains, which is attributed to the variation in the properties of the epi-layers, specifically, a spatially varying detuning of the gain peak and cavity resonance wavelengths, and mirror reflectivity.

The first in-depth comparative experimental study on the performance of 940 nm VCSELs on GaAs and Ge substrates is also presented. Parity in performance between GaAs and Ge substrate VCSELs in terms of key figures of merit is demonstrated. The thermal resistance is measured to be within error despite a smaller oxide aperture and thicker substrate of the Ge VCSELs under test. It is concluded that potential enhancements are to be found in the thermal performance of VCSELs on Ge.

The advantage of improved oxidation uniformity associated with the reduced wafer bow of large diameter Ge wafers is demonstrated. The variation of the material properties represented by the photoluminescence and Fabry-Perot cavity resonance wavelengths are found to be equivalent, showing that radial variations which are generally observed are not driven by wafer curvature. This study demonstrates that high-performance epitaxial structures can be grown on Ge substrates with wafer-scale uniformities equivalent to that of structures grown on GaAs.

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To my parents, Deborah and Tony Baker.

..But something stirs and something tries
And starts to climb towards the light..

– from *Echoes* by Pink Floyd

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List of Acronyms

AR/VR	Augmented Reality/Virtual Reality
BCB	Benzocyclobutene
C-TLM	Circular Transfer Length Method
CW	Continuous Wave
DBR	Distributed Bragg Reflector
DOE	Design of Experiment
EEL	Edge-Emitting Laser
FP	Fabry–Pérot
FWHM	Full-Width Half-Maximum
ICP	Inductively-Coupled Plasma
LED	Light Emitting Diode
LiDAR	Light Detection and Ranging
MBE	Molecular Beam Epitaxy
MOVPE	Metal-Organic Vapour Phase Epitaxy
MQW	Multiple Quantum Well
PECVD	Plasma-Enhanced Chemical Vapour Deposition
PIV	Power-Current-Voltage

PL	Photoluminescence
PVD	Physical Vapour Deposition
QW	Quantum Well
RF	Radio Frequency
RIE	Reactive Ion Etch
SCH	Separate Confinement Heterostructure
SEM	Scanning Electron Microscope
SPVS	Surface Photovoltage Spectroscopy
SWIR	Short-Wave Infrared
VCSEL	Vertical Cavity Surface Emitting Laser
VQF	VCSEL Quick Fabrication

Chapter 1

Introduction

1.1 Motivation

In recent years, the increase in demand for VCSELs in consumer applications has driven manufacturers to scale-up production with growth on larger diameter substrates. For VCSELs, production on 150 mm (6-inch) wafers is still relatively new, whilst work is already being done to facilitate the move to 200 mm (8-inch) production. VCSELs are complex optoelectronic devices and performance is highly sensitive to both the properties of the constituent epitaxial stack and the specific application-dependent wafer processing. This makes the scale-up to high-volume production challenging, and the trade-off between performance and yield must be fine-tuned. Today, VCSEL development is a very often a market driven endeavour and much of the cutting-edge research involves heavy involvement from the private sector. Yield, reproducibility, and reliability are hugely important at every stage of the production cycle, from early R&D to product qualification, and the understanding and minimisation of variation in the manufacturing process is imperative. Further, the timescale of the product design cycle, from design readiness to final release, is typically on the order of months and, as a result, quality control methods which are fast, efficient, and reliable at every stage of the development cycle are paramount.

Table 1.1: Timeline of VCSEL commercialisation.

Year	λ (nm)	Market	Who?	Ref.	Production
1996	850	Datacom	Honeywell	[2]	2-inch
2001	850	Computer Mouse	Hewlett Packard	[3]	2/3-inch
2003	780 8x4 array	Laser Printer	Fuji Xerox	[4]	2-inch
2003	850	Datacom	Honeywell	[3]	3-inch
2005	850	Computer Mouse	Emcore	[5]	3-inch
2007	980 Array	Industrial/Fibre Pump	Princeton Optronics	[6]	3/4-inch
2007	850 10G	Datacom	Emcore	[7]	3-inch
2013	850 25G	Datacom	Chalmers	[8]	4-inch
2017	940	3D Sensing	Lumentum	[9]	6-inch
2021	940 on Ge	3D Sensing & LiDAR	IQE	[10]	6-inch
2021	13xx on GaAs	LiDAR	IQE	[11]	3/4-inch
2022	940 on GaAs & Ge	3D Sensing & LiDAR	IQE	[12]	8-inch
2023	SWIR on InP	3D Sensing & LiDAR	Trumpf	[13]	$\leq$ 4-inch

1.2 Historical Context and Future Outlook

Research on VCSELs stems from the first demonstration of the surface emitting laser in 1979 at the Tokyo Institute of Technology [1] after its conception by Iga in 1977. Since then, there have been thousands of research articles, dozens of review articles and several books dedicated to the subject. Compared with the initial demonstrations where cryogenic temperatures were required, VCSEL technology today is mature. Devices which reliably offer sub-mA threshold currents, narrow beam divergence, low power consumption, as well as stable single-mode operation, modulation bandwidths beyond 25 GHz, and array-fabrication capability are readily available. For these reasons, VCSELs are the de facto laser source for many applications including short-reach datacom, facial recognition and other 3D sensing technology, LiDAR, miniature atomic clocks and magnetometers, computer mice, and laser printers. A timeline of VCSEL commercialisation is shown in Table 1.1.

Commercialisation began in the 1990s with Honeywell's 850 nm emission wavelength VCSELs designed for datacom applications [2], [14]. Whilst that work sought to produce high-performance lasers which met all requirements for short-reach data communication, there was also a critical focus on yield, reproducibility, and reliability. It was this aspect that made the work stand out from previous research and which marked a seminal moment for the VCSEL industry. Uniformity, both wafer-scale and run-to-run, was a critical concern early on, with efforts over a three-year period to reduce the wavelength non-uniformity by an order of magnitude [2]. In the paper, Tatum explains the importance of "rapid and continuous feedback of production information" to foster the continual improvement needed – this was the catalyst for commercialisation.

Since the early 2000s, VCSELs have been employed in computer mice [3] due to their advantages over LED illumination [15]. This constituted the first application of VCSELs in consumer markets. Around the same time, Fuji Xerox, introduced VCSEL arrays to their laser printers [4], [16], [17]. Meanwhile, the increase in internet traffic in the early 2000s and the inclusion of a multimode fibre solution utilising short wavelength lasers in the Gigabit Ethernet standard (IEEE802.3z) [18] drove demand for 850 nm VCSELs for local area networks. Significant advances were made in this period, including the development of the oxide-confined VCSEL [19] and so the dynamic properties of the devices produced were able to keep step with fibre channel data rates. The standards were defined for 10 Gbit/s (IEEE802.3ae) in 2002 and 100G (IEEE802.3ba) in 2011 and VCSEL capability improved in turn [20]–[22].

Around 2007, researchers at Princeton Optronics developed VSCEL arrays operating at 980 nm for fibre laser pumping applications [6], [23]. Before this, VCSELs were only employed in low-power applications, and this signified a different approach which utilised the array-capability of VCSELs to boost the optical power. Up until 2013, VCSEL production was confined to 3-inch wafers, however, the market of VCSELs for datacom saw an expansion. Highly reliable devices with 25 GHz 3 dB bandwidths were produced, and manufacture was scaled to 4-inch wafers [11].

The use of VCSELs in optical sensing applications accelerated towards the end of the

2010s, with 2017 marking the scale-up to 6-inch wafer production [11] to meet the demand for 940 nm VCSELs for face ID in the Apple iPhone X. This demand was maintained as Apple released new iPhone and iPad models in 2020 which included world-facing scanning-LiDAR chips [3].

To provide context for this thesis, a quote from the seminal work on VCSEL commercialisation [2]: "the future for VCSEL technology is bright, with [new] volume applications emerging... Each new market will have its own set of design criteria, its own performance trade-offs, its own statistical requirements. But every new introduction will face similar challenges, and each will build on the history of the millions of VCSELs that came before." This still rings true today. The future for VCSEL technology is now centred on applications in 3D sensing, automotive LiDAR, and AR/VR, where the volumes are much higher. Work has already begun, such as growth on germanium [10], [24]–[26], to facilitate the scale-up to 8-inch wafer production [12], [27]. These markets are driving innovation in the production of higher power VCSELs utilising multi-junction active regions [28]–[30], array addressability [31], and the move to longer wavelength emission with SWIR emitting VCSELs ($>$ 1300 nm) developed for high-power eye-safe use [32]. In 1996, VCSELs were grown on 2-inch diameter substrates. Today, hundreds of millions of VCSELs have already been produced on 6-inch diameter wafers to meet the demand in 3D sensing. If, as some have predicted, VCSELs have a strong presence in automotive LiDAR solutions, the global volume will step up further [33]. Many VCSEL players still operate at lower volumes on 4-inch wafers or smaller, and it is likely that some of these markets will also move to larger wafer production. The question of wafer size is a matter of economics, which relates to chip footprint, cost of scaling up growth/processing capability, and market demand. There are benefits to be found in scaling up production, and the desire to push towards 8-inch stems from the potential access to silicon and LED foundry tools [34], just as the scale-up to 6-inch provided access to more advanced systems in the established 6-inch RF GaAs fabs [35]. The scale-up itself creates new research questions and challenges for producing reproducible, highly uniform wafers and ultimately a high device yield. The experimental studies and development of processing and characterisation

techniques in this thesis are intended to assist in enabling the future scale-up of VCSEL production, be that transitioning to 6-inch production or beyond.

1.3 Thesis Scope

The importance of a rapid and continuous flow of production information has already been emphasised in this chapter, and the first section of this thesis seeks to facilitate this in product development cycles and in volume production. A typical timeline for a VCSEL product development cycle is given in [36]. The total lead time is made up of 1) epitaxial growth, 2) device architecture and photomask design, 3) front- and back-end processing, 4) on-wafer testing, 5) packaging, 6) chip-level testing, and 7) reliability testing. The total development cycle is on the order of months, with the first four stages taking at least 8-10 weeks. In a production setting, one of the main concerns is optimising these cycle times to reduce cost. DOE studies are usually carried out for the development of epi-structures but often vital information on the material quality is only ascertained down the line via on-wafer testing at the device level. If the time taken for the subsequent stages of wafer processing and on-wafer testing are minimised, this cycle can be performed in-house at epi-foundries to more quickly optimise epi-design and growth recipes. This enables rapid feedback to epitaxy which minimises development time. The challenge for today's characterisation is that the current processes do not provide adequate information. Therefore, what wafer manufacturers require is a process for rapid VCSEL fabrication, but which also preserves device performance to provide representative information on both material quality and final chip-level device performance. The development of a QuickSEL process is intended to be of use in studies in the early stages of VCSEL product development and also as a method of continuous feedback during production campaigns.

This technique has utility as an ongoing quality control method for assessing on-wafer, wafer-to-wafer, and run-to-run variation, which is of vital concern for manufacturers as the wafer diameter is increased. As such, the fabrication and characterisation of VCSEL

devices during these cycles can be used to assess the propagation of non-uniformities from the properties of the constituent epi-layers through to the resulting VCSEL performance, and this is the focus of the second section of this thesis. To do this effectively, the variation of the material properties, fabrication parameters, and device performance are each assessed. The properties of the epitaxial layers arising from growth and the properties of the processed device structures arising from fabrication can both have a significant impact on device performance. By careful choice of experiments and analysis, the effects of each are disentangled from the measured device performance. A comprehensive analysis of on-wafer variation in 6-inch MOVPE VCSEL production is given.

Finally, with the scale-up to 6-inch VCSEL production, growth on alternative substrates, such as germanium (Ge), has received attention and been shown to offer some advantages over gallium arsenide (GaAs). However, a detailed experimental comparison of device performance is still needed. Rapid VCSEL fabrication and characterisation is used to also compare the performance of GaAs and Ge substrate VCSELs and to assess the advantages of growth on Ge in terms of uniformity and yield. One of the key focusses is the potential enhancement in thermal performance resulting from the higher thermal conductivity of Ge. This experimental work carried out on GaAs and Ge substrate structures forms the first in-depth study into the performance of VCSELs grown on Ge, adding to the recent work which showed the potential advantages of Ge in large diameter wafer production.

In summary, this thesis seeks to address three research questions pertaining to yield, reproducibility, and variation in MOVPE VCSEL production which arise from the scale-up to large diameter wafers:

1. Can a method of rapid VCSEL fabrication be designed to streamline feedback in manufacturing, such that processing time is sufficiently reduced but device performance is preserved?
2. What wafer-scale non-uniformities arise in VCSEL production by MOVPE as the wafer size is increased?

3. Does growth on alternative substrates, such as Ge, provide any net advantages over growth on GaAs?

It is not within the scope of this thesis to produce state-of-the-art VCSEL devices, nor to explicitly modify the designs of epitaxial structures for improvement of device performance or yield. Likewise, there are no explicit recommendations of modifications to growth reactor conditions. Instead, typical wafers with generic epitaxial structures are considered and the conclusions drawn are predicted to apply generally to MOVPE VCSEL growth on large diameter substrates.

1.4 Thesis Structure

Chapter 2 provides a review of the background information which underpins the methodology, results, and discussion presented in this thesis. Firstly, the background theory and principles of VCSEL operation are presented, then attention is given to the typical output characteristics of VCSELs. Chapter 3 firstly provides an overview of VCSEL production, with focus on MOVPE growth and standard processing techniques. A description of the sources of variation in the production process and critical tolerances is given. Then, the methodology used for the studies performed is discussed, with descriptions of the experimental setups and of the physics underpinning the material and device characterisation methods provided. Chapter 4 focusses on the development of a Quick VCSEL (QuickSEL) process. Specific fabrication methods are presented for QuickSELs and standard planarised devices and the experimental qualification of the QuickSEL is presented. Chapter 5 focusses on characterising the on-wafer non-uniformities which arise from the scale-up of VCSEL production to 6-inch diameter substrates and beyond. Post-growth material characterisation is considered alongside assessment of fabrication parameter non-uniformity and the wafer-scale measurement of VCSEL performance. Chapter 6 provides the first detailed experimental comparison of GaAs and Ge substrate VCSELs. Addition-

ally, the advantages of growth on Ge to mitigate variations are shown from the assessment of on-wafer device performance. Finally, a summary and conclusion is given in Chapter 7, along with avenues for future investigations.

1.5 Publications

The material in this thesis is based mostly on work reported in the following journal articles and conference presentations:
Journal Articles:

- J. Baker, C. P. Allford, S. Gillgrass, R.Forrest, D. G. Hayes, J. Nabialek, C. Hentschel, J. I. Davies, S. Shutts, and P. M. Smowton. "Quick fabrication VCSELs for characterisation of epitaxial material," Applied Sciences 2021, Vol. 11, Page 9369

- J. Baker, S. Gillgrass, C. P. Allford, T. Peach, C. Hentschel, T. Sweet, J. I. Davies, S. Shutts, and P. M. Smowton. "VCSEL Quick Fabrication for assessment of large diameter epitaxial wafers," IEEE Photonics Journal 2022, Vol 14, Issue 3, Page 1-10

- S. Gillgrass, C. P. Allford, T. Peach, A. D. Johnson, J. Baker, J. I. Davies, A. M. Joel, S. Shutts, P. M. Smowton, "Impact of thermal oxidation uniformity on 150 mm GaAs- and Ge-substrate VCSELs," Journal of Physics D: Applied Physics, Focus on Future Compound Semiconductor Manufacturing 2023, Vol 56, Number 15

- J. Baker, C. P. Allford, S. Gillgrass, T. Peach, J. Meiklejohn, C. Hentschel, W. Meredith, D. Powell, T. Sweet, M. Haji, J. I. Davies, S. Shutts, P. M. Smowton, "VCSEL quick fabrication of 894.6 nm wavelength epi-material for miniature atomic clock applications," IET Optoelectronics 2022, Vol 17, Issue 1, Page 24-31

Conference Presentations:

- J. Baker, D. G. Hayes, T. Peach, J. I. Davies, S. Shutts, and P. M. Smowton, et. al. "Quick fabrication of 940nm emitting VCSEL arrays for commercial wafer characterization," SPIE Photonics West, Vertical-Cavity Surface-Emitting Lasers XXV (2021)

- D. G. Hayes, T. Peach, J. Baker, S. Gillgrass, C. P. Allford, J. I. Davies, S. Shutts, P. M. Smowton, et. al. "150mm full wafer fabrication and characterization of 940nm emitting VCSELs for high-volume manufacture," Vertical-Cavity Surface-Emitting Lasers XXV (2021)

- J. Baker, S. Gillgrass, C. P. Allford, C. Hentschel, J. I. Davies, S. Shutts, and P. M. Smowton. "Sub-mA Threshold Current Vertical Cavity Surface Emitting Lasers with a Simple Fabrication Process," IEEE Photonics Conference (2021)

- J. Baker, C. P. Allford, S. Gillgrass, T. Peach, J. I. Davies, S. Shutts, and P. M. Smowton. "Sub-mA threshold current quick fabrication VCSELs for characterisation of epitaxial material over 150 mm wafers," SPIE Photonics West, Vertical-Cavity Surface-Emitting Lasers XXVI (2022)

- J. Baker, S. Gillgrass, T. Peach, C. P. Allford, A. D. Johnson, A. M. Joel, S. W. Lim, J. I. Davies, S. Shutts, P. M. Smowton. "Impact of strain-induced wafer-bow on the performance of VCSELs grown on 150 mm GaAs and Ge substrates," SPIE Photonics Europe, Semiconductor Lasers and Laser Dynamics X (2022)

- J. Baker, S. Gillgrass, T. Peach, C. P. Allford, A. D. Johnson, A. M. Joel, S. W. Lim, M. Geen, J. I. Davies, S. Shutts, P. M. Smowton. "Impact of strain-induced wafer-bow on the manufacture of VCSELs grown on 150 mm GaAs and Ge substrates," International Conference on Compound Semiconductor Manufacturing Technology (2022)

- S. Gillgrass, C. P. Allford, T. Peach, J. Baker, J. I. Davies, T. Sweet, A. D. Johnson, A. M. Joel, S. W. Lim, S. Shutts, P. M. Smowton. "Manufacture of 940 nm VCSELs on 150 mm GaAs and Ge substrates," Semiconductor and Integrated Optoelectronics Conference (2022)

- J. Baker, S. Gillgrass, T. Peach, C. P. Allford, A. D. Johnson, A. M. Joel, S. W. Lim, M. Geen, T. Sweet, J. I. Davies, S. Shutts, P. M. Smowton. "VCSEL Quick Fabrication for substrate optimisation in high-volume manufacture" UK Semiconductors (2022)

- J. Baker, S. Gillgrass, T. Peach, C. P. Allford, A. D. Johnson, A. M. Joel, S. W. Lim, M. Geen, J. I. Davies, S. Shutts, P. M. Smowton. "Comparative study of 940 nm VCSELs grown on GaAs and Ge substrates," IEEE Photonics Conference (2022)

- S. Gillgrass, C. P. Allford, A. D. Johnson, J. Baker, J. I. Davies, S. Shutts, P. M. Smowton, "Characterisation of 200 mm GaAs and Ge substrate VCSELs for high-volume manufacturing," SPIE Photonics West, Vertical Cavity Surface Emitting Lasers XVII (2023)

- C. P. Allford, J. Baker, S. Gillgrass, J. Meiklejohn, D. Powell, Wyn Meredith, T. Sweet, J. I. Davies, Samuel Shutts, Peter M. Smowton, "Quick Fabrication VCSEL characterisation for rapid assessment of epitaxy design and growth," SPIE Photonics West, Vertical Cavity Surface Emitting Lasers XVII (2023)

- J. Baker, C. Hentschel, C. P. Allford, S. Gillgrass, J. Iwan Davies, S. Shutts, P. M. Smowton, Characterisation Techniques for On-Wafer Testing of VCSELs in Volume Manufacture, International Conference on Compound Semiconductor Manufacturing Technology (2023)

Finally, listed here are related publications, the content of which is not explicitly included in the thesis:

Journal Articles:

- C. Hentschel, C.P. Allford, S-J. Gillgrass, J. Nabialek, R. Forrest, J. Baker, J. Meiklejohn, D. Powell, W. Meredith, M. Haji, J.I. Davies, S. Shutts and P.M. Smowton. "Gain Measurements on VCSEL Material Using Segmented Contact Technique," Journal of Physics D: Applied Physics, Focus on Future Compound Semiconductor Manufacturing 2023, Vol 56, Number 7

Conference Presentations:

- J. Baker, D. G. Hayes, T. Peach, J. I. Davies, S. Shutts, and P. M. Smowton. "Performance-mapping for characterisation of 150mm VCSEL wafers in industry," Semiconductor and Integrated Optoelectronics Conference (2021) (Poster Presentation)

- C. Hentschel, C. P. Allford, S. Gillgrass, Z. Li, J. Nabialek, R. Forrest, J.Baker, D. G. Hayes, W. Meredith, J. I. Davies, S. Shutts, and P. M. Smowton. "Gain Measurements on Vertical Cavity Surface Emitting Laser Material Using Segmented Contact Technique," IEEE Photonics Conference (2021)

- J. Baker, S. Gillgrass, T. Peach, C. P. Allford, C. Hentschel, J. I. Davies, S. Shutts, and P. M. Smowton. "VCSEL quick fabrication for characterisation of epitaxial material designed for atomic sensing applications," Semiconductor and Integrated Optoelectronics Conference (2022)

- S. Shutts, C. Hentschel, S. Gillgrass, J. Meiklejohn, C. P. Allford, J. Baker, J. Nabialek, D. Powell, W. Chalupczak, M. Haji, W. Meredith, P. M. Smowton. "Design and characterisation of VCSELs for atomic sensor applications," SPIE Photonics West, Vertical Cavity Surface Emitting Lasers XVII (2023)

Chapter 2

VCSEL Fundamentals

2.1 Semiconductor Laser Principles

2.1.1 Radiative Transitions in Semiconductors

In a direct bandgap semiconductor, like that shown in Figure 2.1, there are three basic radiative transitions: (a) stimulated absorption, (b) spontaneous emission, and (c) stimulated emission. When a photon of energy $E_{h\nu} \geq E_g = E_c - E_v$, where E_g is the bandgap energy, impinges on the system, a valence electron can be promoted to the conduction band by stimulated absorption. Conversely, an electron in the conduction band may undergo a downward transition at any time, emitting a photon of energy $h\nu \geq E_c - E_v$ by spontaneous emission. Spontaneous emission events are characterised by a radiative lifetime which accounts for the average time taken for an electron in the conduction band to recombine with a hole in the valence band, which is typically on the order of nanoseconds. The third process, stimulated emission, is fundamental to the operation of lasers and occurs when an incident photon perturbs a conduction band electron to emit a photon of the same frequency, phase, and direction as the original photon. It is then possible for the coherent photons generated to produce further stimulated emission events, thus amplifying

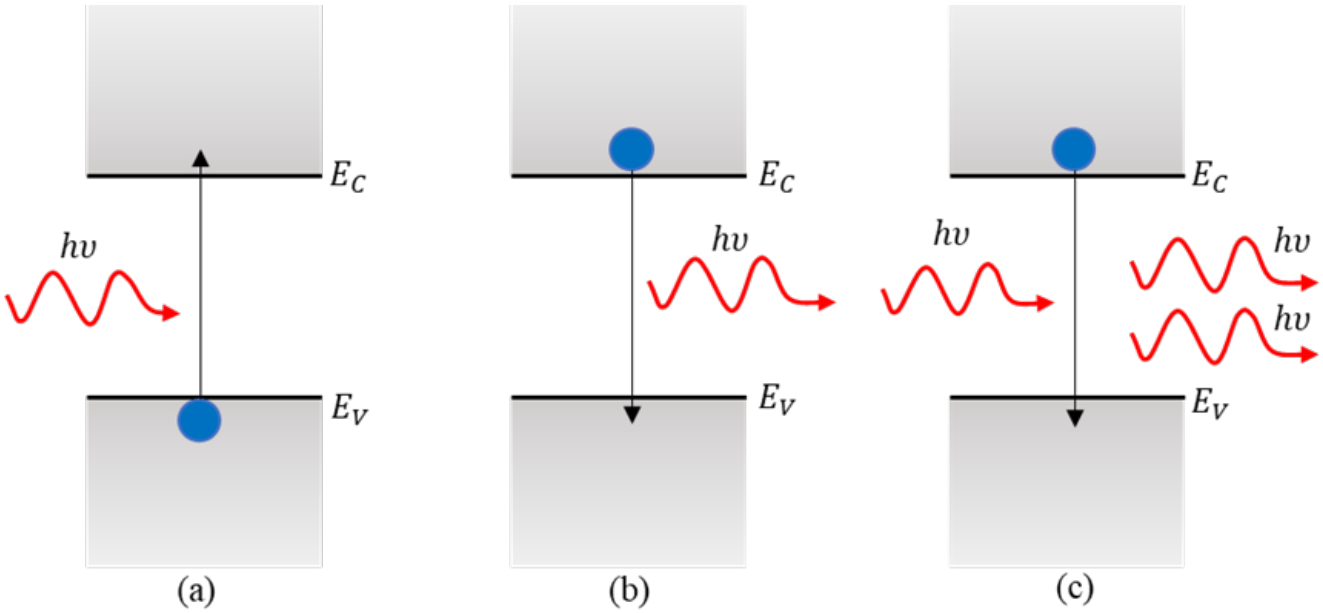

Figure 2.1: Radiative transitions occurring in a semiconductor material; (a) stimulated absorption, (b) spontaneous emission, and (c) stimulated emission.

the incident optical intensity. The timescale for stimulated emission events is dependent on the electron and photon populations, however, under the correct conditions, stimulated emission events occur near instantaneously in comparison to spontaneous emission. These conditions must be met for the rate of stimulated emission to dominate and for laser action to occur.

2.1.2 Laser Action

The amplification of light by stimulated emission is fundamental to laser action. For the rate of stimulated emission to dominate, a population inversion of carriers is needed, such that the number of electrons in the excited energy state is greater than the number in the ground state. However, once a conduction band electron is stimulated to emit a photon, the electron subsequently transitions to the valence band, thus depleting the degree of inversion. To achieve steady-state lasing, the population inversion must be maintained, and, in a diode laser, this is most often achieved by electrical pumping. Charge carriers are injected into the gain medium, ensuring a sufficient supply of electrons in the conduction

band and holes in the valence band. Furthermore, to create a sufficiently high photon density, feedback is required and this is achieved by placing reflective mirrors at the ends of the gain medium, forming an optical cavity.

The light inside the cavity is subject to loss, a component of which is internal (relating to the material) and a component of which is external (relating to the reflectivity of the cavity mirrors). For laser action to occur, the gain (amplification) in the cavity must balance the total loss. The single-pass intensity variation of light propagating through a medium with gain, g, and internal optical loss, α_i, can described by

$$I = I_0 exp[(g - \alpha_i)L], \tag{2.1}$$

where I_0 is the initial intensity and L is the cavity length. Both g and α_i are usually expressed in units of cm^{-1}. As the light of intensity, I_0, propagates along the cavity and, after being partially reflected by one end mirror, completes a round trip to the second mirror, the intensity is described by

$$I = I_0 R_1 R_2 exp[2(g - \alpha_i)L], \tag{2.2}$$

where R_1 and R_2 are the reflectivity of the mirrors. For a steady state solution, the intensity after a round-trip must equal the initial intensity, therefore

$$g_{th} = \alpha_i + \frac{1}{2L} ln\left(\frac{1}{R_1 R_2}\right), \tag{2.3}$$

where g_{th} is the threshold gain of the laser, that is, the gain required to balance the total loss. The first term on the right-hand side of Equation 2.3 represents the internal loss of the gain medium and the second term represents the mirror loss. From Equation 2.3, a relation between the cavity length and the mirror reflectivity can be obtained which, for typical values of g_{th} and α_i demands that to reduce the cavity length to the order of 1 µm the product $R_1 R_2$ must exceed 0.99. This is important for vertical cavities which are necessarily produced by epitaxy and, due to the practical limitations of the technol-

ogy, cannot be very large (total thickness of whole epi-structure is several micrometres). Hence, for a vertical-cavity laser, the mirror reflectivity is required to exceed 99%. The short cavity length thus leads to a photon lifetime in the cavity on the order of ps for VCSELs. Conversely, the reflectivity of the cavity mirrors in an EEL is approximately 30%, determined by the refractive index contrast at the semiconductor-air interface. As such, cavity lengths range from 10s to 100s of micrometres and photon lifetime is often longer, ranging up to nanoseconds.

The feedback provided by the mirrors causes the light to travel back and forth along the cavity, constructively interfering to form standing waves, and optical modes corresponding to the fundamental and higher order harmonic frequencies of the standing waves are formed. For a mode to be supported, the round-trip distance must equal an integer number of wavelengths:

$$2L = \frac{m\lambda}{n}, \tag{2.4}$$

where n is the refractive index of the material in the cavity and $m = 0,\ 1,\ 2...$ etc. Equation 2.4 can be used to find the spacing of allowed longitudinal modes. Assuming that dispersion in the material can be ignored, this is written as

$$\Delta\lambda = \frac{\lambda^2}{2nL}, \tag{2.5}$$

which for a typical VCSEL operating at ~ 900 nm with a λ-thick inner cavity is approximately 120 nm. For this reason, higher order longitudinal modes are not amplified by the quantum wells as they lie outside the bandwidth of the gain spectrum and as a result VCSELs are inherently single longitudinal mode lasers.

2.2 VCSEL Structure

The focus of this thesis is on commercialised VCSEL technology, which generally utilises the InAlGaAs material system. Within this material system the laser emission is between

$\sim$ 800 and 1000 nm with a GaAs or InGaAs gain medium. Most VCSELs take the form of a PIN-diode structure with an undoped multiple quantum well (MQW) active region embedded in a separate confinement heterostructure (SCH). The cavity mirrors are formed by two distributed Bragg reflector (DBR) mirrors one of which is p-doped with the other n-doped. A cross-sectional diagram showing a typical oxide-confined VCSEL is shown in Figure 2.2. Epitaxial growth of AlGaAs is used to form DBR mirrors for VCSELs emitting from the red to the short-wave infrared [32], [37], [38]. The composition of the constituent layers determines the number of mirror pairs needed to achieve the high reflectivity required for laser action, as discussed in section 2.1.2, usually resulting in a structure in excess of 100 layers. Given the large number of layers, the resistance at each heterointerface is an important design consideration. Several approaches for limiting the resistance have been demonstrated and these are described in more detail in section 2.5. Furthermore, although, the binary compounds GaAs and AlAs are generally considered to be lattice matched, there is a slight mismatch of approximately 0.16%, the strain of which is non-negligible for AlGaAs-based VCSELs grown on GaAs. The effect of the small lattice mismatch can compound and result in a bowing/warping of the epitaxial wafer. This becomes particularly important as the diameter of the growth substrate is increased. The significance of the GaAs-AlAs lattice mismatch in volume VCSEL production is discussed in more detail in Chapter 3.

For the remainder of section 2.2 the key structural features of VCSELs are described in more detail and the theory underpinning the design of epitaxial structures and device architecture is discussed.

2.2.1 Distributed Bragg Reflector Mirrors

Distributed Bragg reflector mirrors are structures that consist of layers of alternating high and low refractive index material. When the layers are formed such that they are each a quarter material-wavelength thick, constructive interference of the partial reflections occurring at each boundary results in a high reflectivity of light at the Bragg wavelength.

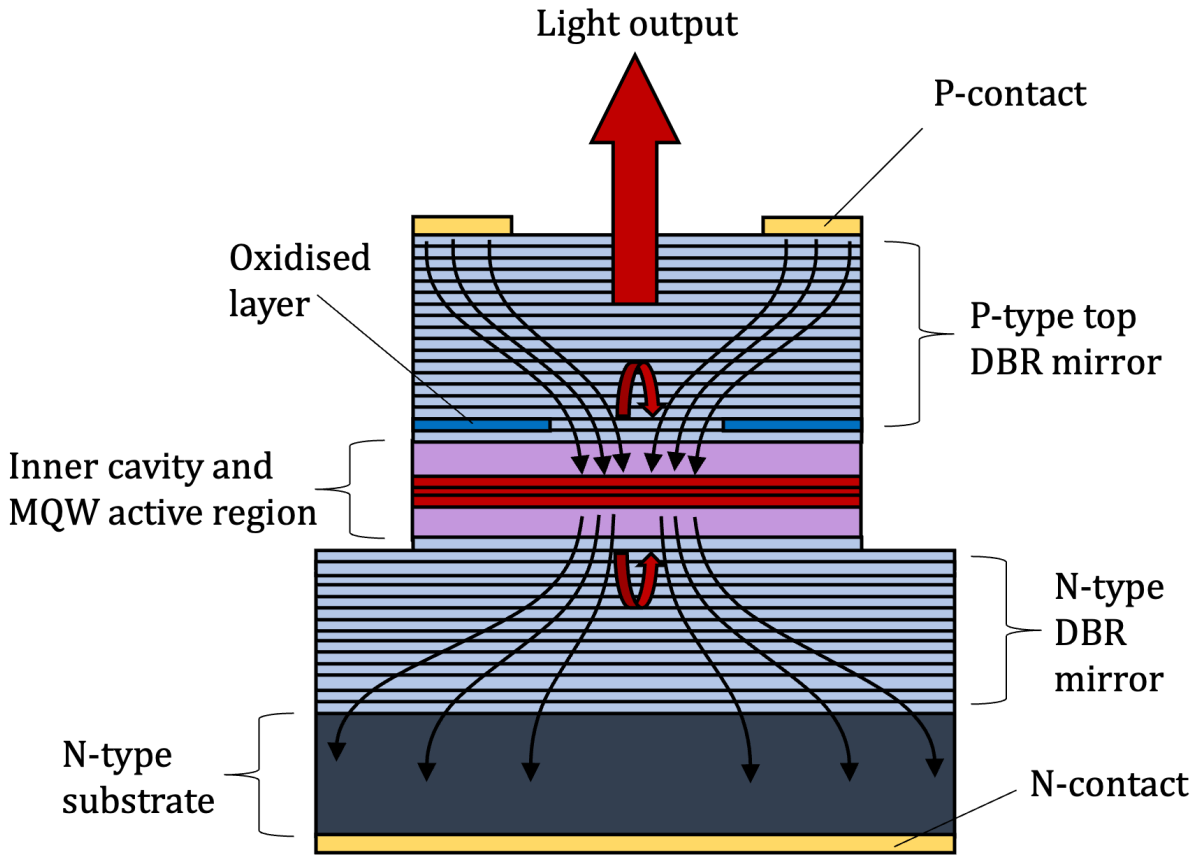

Figure 2.2: Typical structure of a top-emitting VCSEL device consisting of an MQW active region sandwiched between upper (p-type) and lower (n-type) DBR mirrors. Current is injected though an Ohmic ring contact and is confined to the centre of the active region by a selectively oxidised highly resistive layer above the inner cavity. Carriers take a path through the device shown by the curved black arrows.

From [39], the Bragg wavelength can be expressed as

$$\lambda_B = 2\bar{n}\Lambda, \tag{2.6}$$

where $\bar{n}$ is equal to the sum of the refractive indices within a DBR pair, $n_1 + n_2$, and Λ is the period of the grating, equivalent to the sum of the thicknesses of the pair. The stacking of many DBR pairs leads to the formation of a high-reflectivity stopband, the width of which relative to the Bragg wavelength can be approximated by [39]

$$\Delta\lambda \approx \frac{2\lambda_B}{\pi}\frac{\Delta n}{\bar{n}}. \tag{2.7}$$

The power reflectivity of the mirror is dependent on the refractive index contrast of the constituent layers and the total number of periods. For a Bragg stack consisting of N pairs of low and high index layers, n_1 and n_2, the reflectivity, R, is

$$R = \left(\frac{1 - \left(\frac{n_1}{n_2}\right)^{2N}}{1 + \left(\frac{n_1}{n_2}\right)^{2N}}\right)^2. \tag{2.8}$$

Under this approximation it is assumed that the stack is clad on each end by air. To illustrate the dependence on material composition, the power reflectivity as a function of the number of mirror pairs is shown in Figure 2.3 for different refractive index contrasts based on Equation 2.8. The cases considered are for $Al_xGa_{1-x}As/Al_yGa_{1-y}As$ DBR layers, where x and y are the the Al mole fractions in each layer of the DBR pair. As the refractive index contrast is reduced, the number of mirrors pairs required to achieve a given reflectivity increases. This is equivalent to decreasing the Al mole fraction of the low index layer (thus increasing the refractive index) whilst increasing the Al mole fraction of the high index layer (thus decreasing the refractive index). This is detailed in the legend of Figure 2.3. Figure 2.4 displays a measured reflectivity spectrum for a VCSEL showing a 103.4 nm wide stopband, centred at 942.0 nm, resulting from the Bragg mirrors. The Fabry–Pérot dip occurs at 942.6 nm, which indicates the presence of a cavity resonance.

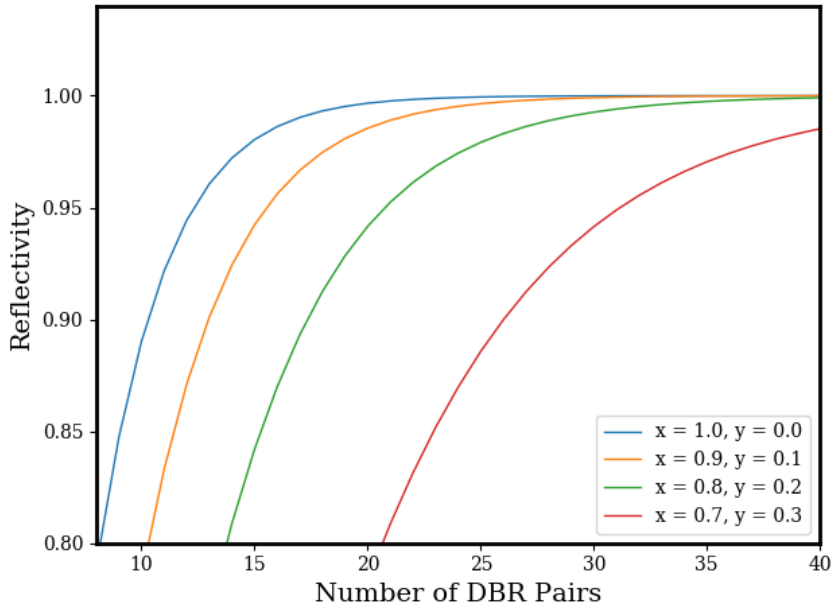

Figure 2.3: Power reflectivity as a function of the number of DBR pairs for different refractive index contrasts. The terms x and y refer to the Al mole fraction in the high and low refractive index layers of the constituent DBR pairs, respectively.

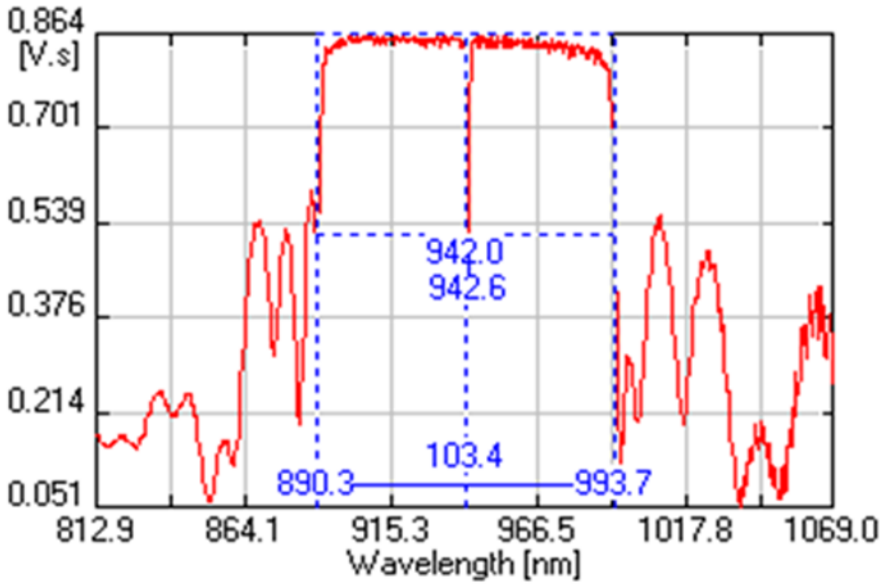

Figure 2.4: VCSEL reflectivity spectrum measured from post-growth reflectometry characterisation. Here a 103.4 nm wide stopband is formed which is centred at 942.0 nm. The dip in the spectrum corresponding to the Fabry–Pérot (FP) cavity resonance wavelength occurs at 924.6 nm.

The reflectivity spectrum of the full VCSEL structure is the cumulative result of the separate DBR stopbands and the inner cavity. The materials used in the top and bottom DBRs may be different, for example, AlAs is often employed in the bottom DBR due to its high thermal conductivity [40], but most often cannot be used in the top DBR due to the need for the mirror stack to have a different Al content to the selective oxidation layer (see section 3.3.3). Therefore, it is common for the mirrors of a given VCSEL structure to be made up of different compositions despite being designed to produce equivalent reflectivity characteristics. This is managed by tuning the layer thicknesses for a given composition to produce the same stopband characteristics, as per Equations 2.6 and 2.5. To achieve the very high reflectivity required due to the short amplification length (Equation 2.3), there are typically in excess of 20 Bragg pairs in each DBR mirror for VCSELs emitting in the 800-1000 nm range. As the wavelength range shifts towards the red, low Al content AlGaAs becomes absorbing and $Al_{0.95}Ga_{0.05}As/Al_{0.5}Ga_{0.5}As$ layers must be used. This decrease in index contrast necessitates a larger number of DBR pairs, typically in excess of 45.

2.2.2 Active Region and Cavity Design

As stated above, the standard configuration for VCSELs is to employ a multiple quantum well (MQW) active region, with GaAs or InGaAs the material of choice for the QW layers. When grown with AlGaAs barriers, the strain present in an InGaAs quantum well must be considered. This limits the thickness of the layer which can be grown without misfit locations for a given In composition to roughly 100 Å per 1% of strain [41]. This translates to critical thickness of approximately 70 Å for $In_{0.2}Ga_{0.8}As$ grown on GaAs which has a strain of 1.4%. A lower In mole fraction in the QW reduces the strain which in turn increases the critical layer thickness, although this also affects the range of wavelengths available. The compressive strain for layers below the critical thickness has been shown to boost the differential gain in VCSELs, and this is utilised in the design of high-modulation bandwidth VCSELs emitting at 850 nm [42]. The thickness and composition of the QW

layers determine the optical transition energies and, therefore, the spectral dependence of the gain. The energy corresponding to ground state electron-hole recombination in the QW layer is given by

$$E_{ph} = E_{e1} + E_g + E_{h1} \tag{2.9}$$

where E_{e1} is the electron confined state energy, E_g is the semiconductor bandgap energy, and E_{h1} is the hole confined state energy. This is illustrated in Figure 2.5. The properties of the QW layers can be probed by measuring the emission spectrum resulting from the recombination of optically excited carriers (see Chapter 3), however, some assumptions must be made when relating the observed wavelength to the layer thickness or composition.

Most VCSELs employ a λ-thick inner cavity, and to maximise the amount of stimulated emission, the overlap between the active layers and the intensity of light should be maximised. For this, the QWs are placed at an antinode of the electric field. From Equation 2.4, in the resonant condition the cavity length is an integer number of half-wavelengths and typically electric field antinodes are positioned at both ends of the inner cavity. Therefore, in this configuration, the shortest cavity length which centres the active region in a field antinode is one wavelength thick, equivalent to m = 2 [43].

To account for the overlap of the gain layers with the electric field profile, the relative confinement factor can be introduced:

$$\Gamma_r = \frac{L_a}{d_a} \frac{\int_{d_a} |E(z)|^2 dz}{\int_{\infty} |E(z)|^2 dz} \tag{2.10}$$

which represents the average intensity in the QW layers, normalised to the total intensity in the inner cavity. Approximating the field profile in the in the centre of a λ-thick cavity by

$$E = E_0 cos\left(\frac{2\pi \bar{n} d_a}{\lambda}\right) \tag{2.11}$$

where d_a is the total thickness of the active layers, the result is $\Gamma_r = 2$, demonstrating that the gain provided can be enhanced by exploiting the overlap of the standing-wave

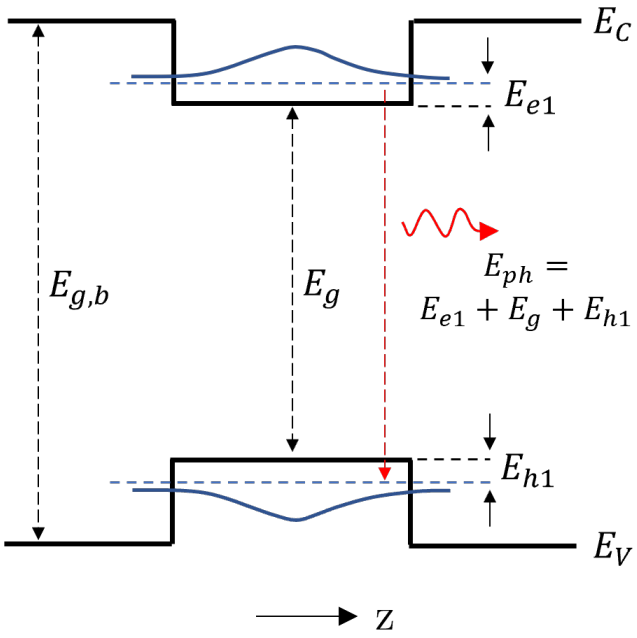

Figure 2.5: Conduction and valence band edge profiles (E_c and E_v) of a quantum well. The narrow bandgap (E_g) quantum well layer is clad by wider bandgap ($E_{g,b}$) barrier layers. The confined state energies for electrons and holes are E_{e1} and E_{h1}, respectively. Recombination between the electron and hole confined states results in emission of a photon with energy $E_{ph} = E_{e1} + E_g + E_{h1}$.

pattern with the active material. Historically, this has also been achieved with resonant periodic gain [44], [45], where each QW of the active region is placed at a field antinode, spaced by $\lambda/2$, however it was found to be inferior to a simple MQW arrangement with thin barriers like that described here. It should be noted that a λ-thick inner cavity is not always optimum. For some designs, it is advantageous to minimise the photon lifetime [46], [47] and this is often done by reducing the cavity length to $\lambda/2$. In this case, nodes of the electric field are placed at the ends of the cavity.

2.2.3 Optical and Electrical Confinement

The realisation of low threshold (sub-mA) VCSELs can be attributed to the advances in selective oxidation of AlGaAs (see section 3.3.3), and the electrical and optical confinement that was afforded by the oxidised layers buried in the epitaxial structure. For an etched mesa, the oxidation of the buried layer (or layers) produces a low effective index

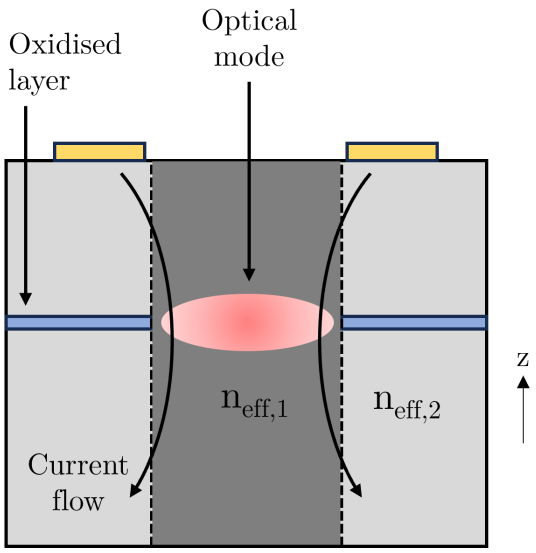

Figure 2.6: Electrical and optical confinement in an etched-mesa VCSEL. The oxidation of a high-Al content AlGaAs layer creates a low-effective-index high-resistivity outer cladding layer which funnels current through the central high-effective-index low-resistivity core region and confines the optical mode.

region defined by the oxidation front which results in the confinement of the optical mode to the central high-index region [48]. The central region is commonly referred to as the VCSEL aperture. Further, the oxidised layer is highly resistive which has the simultaneous effect of funnelling current through the aperture thereby also providing electrical confinement. This is shown in the diagram of Figure 2.6. The advances in selective oxidation of AlGaAs enabled the production of microcavities with small active volumes which, in turn, lowered threshold currents and enhanced output characteristics [49]–[51]. On the other hand, reduction of the aperture diameter to less than approximately 4 µm, scattering and diffraction effects at the aperture interface result in an increased optical loss, which leads to an sharp increase in threshold current density. [52], [53]. For larger device diameters, oxide-related scattering and diffraction is negligible.

2.3 VCSEL Threshold

2.3.1 Threshold Current

At threshold, the gain and the losses of the laser are equally balanced. The loss coefficients of the laser can be divided into that of the passive and active layers, α_i and α_a and that due to partial transmission through the mirrors α_m. Differentiating between the loss in the active and passive regions is a result of the of contrast in the rate of free carrier absorption transitions occurring. From [43], by considering the round-trip condition, Equation 2.3 is modified to give the VCSEL threshold gain as

$$g_{th} = \alpha_a + \frac{1}{\Gamma_r d_a}\left(\alpha_i(L_{eff} - d_a) + ln\left(\frac{1}{\sqrt{R_t R_b}}\right)\right) \tag{2.12}$$

where R_t R_b is the product of the top and bottom Bragg mirror reflectivity and L_{eff} is the effective cavity length which accounts for the penetration depth into the DBRs [43], [54]. The loss coefficient α_i is made up of scattering and diffraction losses in addition to absorption via free carriers. To achieve the required gain threshold the laser needs to be electrically pumped to reach threshold carrier density, which is dependent on the active material. The threshold current density can be expressed as

$$j_{th} = \frac{q d_a}{\eta_i \tau_{sp}} n_{th}^2 \tag{2.13}$$

where η_i is the internal quantum efficiency, q the elementary charge, τ_{sp} is the carrier spontaneous recombination lifetime, and n_{th} is the threshold carrier density. Often, the internal quantum efficiency exceeds 90% [43] and the reduction of η_i is found to be one of the limiting factors for high current VCSEL operation, due to thermal leakage of carriers. The spontaneous recombination lifetime characterises the rate of carrier loss to spontaneous radiative and non-radiative recombination events, and is itself carrier density

dependent and given by

$$\frac{1}{\tau_{sp}} = \frac{1}{\tau_{sp,n}} + \frac{1}{\tau_{sp,r}} = An + Bn^2 + Cn^3. \tag{2.14}$$

The terms A, B, and C represent the contribution of non-radiative (surface and interface, as well as via trap states resulting from impurities and defects), radiative, and Auger recombination, respectively. Assuming a uniform distribution of j_{th} over the active area, the threshold current can be expressed as

$$I_{th} = j_{th}A = \frac{qV_a}{\eta_i \tau_{sp}} n_{th}^2 \tag{2.15}$$

hence the threshold current increases linearly with the device active volume.

2.3.2 Gain Peak - Cavity Resonance Detuning

The threshold current of a VCSEL is also dependent on the alignment of the gain spectrum with the Fabry–Pérot cavity resonance wavelength. This is because, unlike EELs, VCSELs do not necessarily lase at the gain peak as they intrinsically operate with a single longitudinal mode [39], [43], [55]. As such, the available gain at the cavity resonance wavelength is strongly dependent on the alignment with the gain spectrum, which results in a wavelength dependence of the threshold carrier density. This is illustrated in Figure 2.7, where gain spectra corresponding to different carrier densities are shown for a fixed gain threshold. Sweeping through the wavelength range, it is evident that the minimum threshold carrier density occurs when the cavity resonance wavelength coincides with the gain peak.

This property of VCSELs has important implications for the temperature dependence of threshold current. The shift with temperature of the gain peak and cavity resonance wavelengths differs significantly. The gain peak shift, $\Delta\lambda_{pk}$, is $\sim$ 0.3 nm/K, driven by the temperature coefficient of the bandgap [56]–[58], whereas the cavity resonance shift,

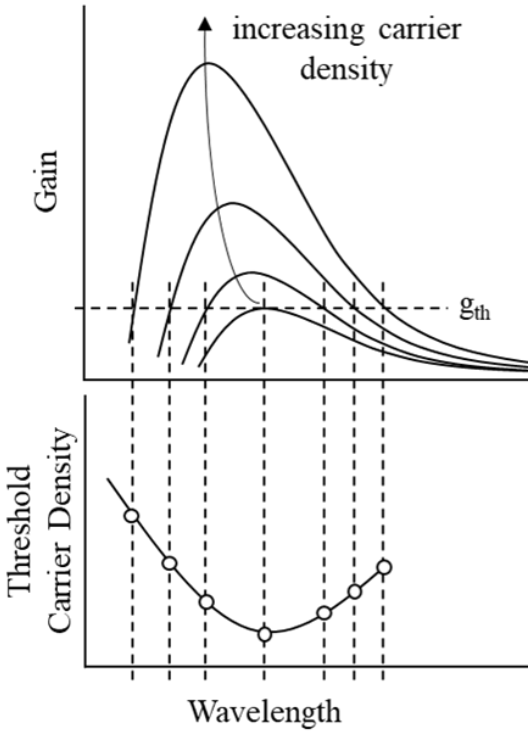

Figure 2.7: (top) typical gain spectra of a VCSEL and the change with increasing carrier density - the horizontal dashed line corresponds to the fixed gain threshold; and (bottom) spectral dependence of threshold carrier density for a fixed gain threshold. The vertical dashed lines correspond to different cavity resonance wavelengths.

$\Delta\lambda_{cav}$, is typically ~ 0.07 nm/K, resulting from change in refractive index [57], [59], [60]. This difference means that the available gain at the longitudinal cavity resonance wavelength also varies non-linearly with temperature. This is illustrated in Figure 2.8. As the temperature is increased, the gain spectrum shifts to longer wavelength and simultaneously, for a fixed carrier density, the peak gain also decreases. The resonance wavelength is relatively stable in comparison to the gain spectrum, therefore, if beginning on the long wavelength side of the gain spectrum, the available gain at the cavity mode wavelength increases with temperature, is maximum when coinciding with the gain peak, and finally decreases with further increases in temperature [61], [62]. Assuming the optical losses are constant throughout the temperature sweep, the threshold carrier density, and hence threshold current, tracks the available gain, and is minimised when the cavity mode coincides with the gain peak. This is shown in Figure 2.9 from experimentally determined threshold currents as a function of temperature, where the alignment of the cavity

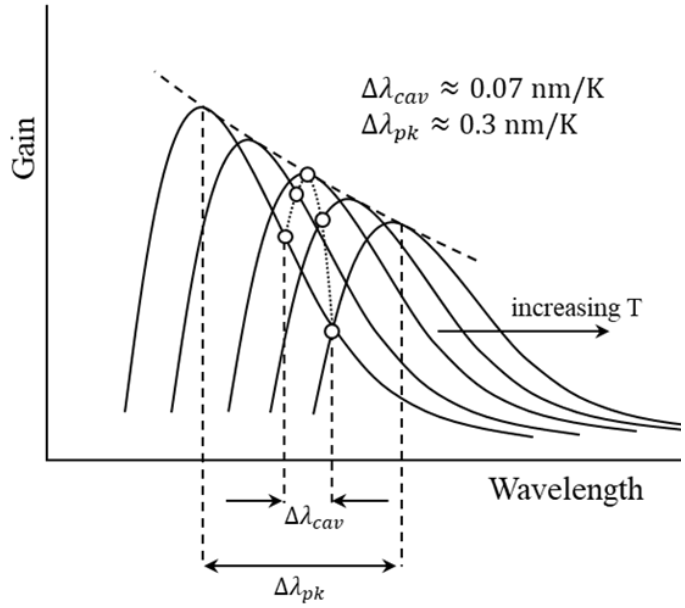

Figure 2.8: Gain spectrum shift with temperature. The gain spectrum shifts according to the temperature coefficient of the bandgap ($\sim$ 0.3 nm/K), whereas the cavity mode shifts according to the refractive index shift of the constituent layers ($\sim$ 0.07 nm/K). The solid circles indicate the available gain at the cavity mode wavelength throughout the temperature sweep.

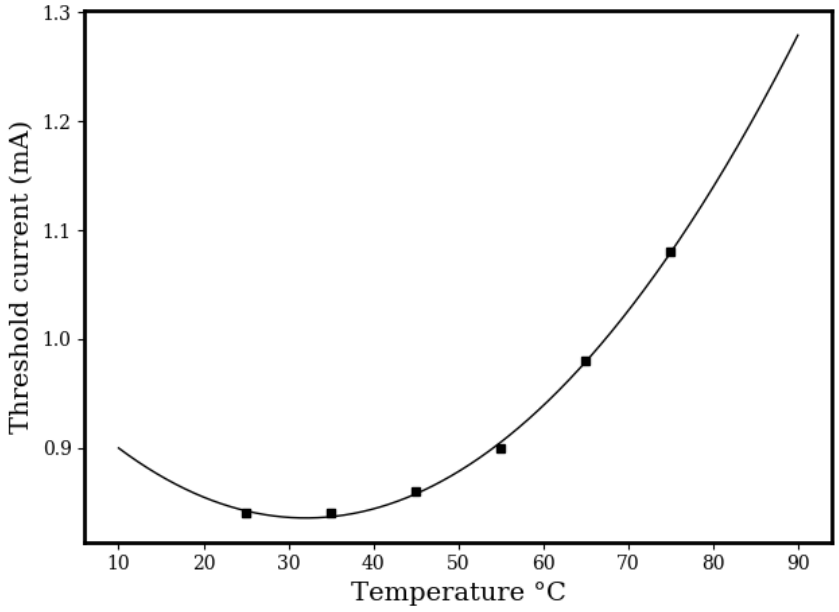

Figure 2.9: Experimentally measured VCSEL threshold current as a function of temperature. A minimum occurs at $\sim$ 30°C which corresponds to the alignment of the gain peak and cavity resonance wavelengths.

mode and the gain peak occurs at ~ 30°C. Therefore, by designing the room temperature gain peak wavelength to be blue-shifted relative to the cavity resonance wavelength, the VCSEL threshold current can be optimised for high temperature performance. The temperature dependence of threshold current can provide valuable information on the VCSEL epitaxial structure. From [63], the change in threshold current with temperature can be fit with

$$I_{th}(T) = \alpha + \beta(T - T_{min})^2, \tag{2.16}$$

where α is the minimum achievable threshold current, β is a term which characterises the rate of change with temperature, and T_{min} is the temperature at which the threshold current minimum occurs. If there are no significant differences in the gain spectrum, the quantity α is representative of the total optical loss of the particular VCSEL and can also be indicative of epitaxial layer variations when considering equivalent device architectures. The term β is not determined by the specific VCSEL design, rather it is driven by the shape of the gain spectrum and the cavity mode wavelength, hence it can offer information on the quantum well layers and the inner cavity length.

2.4 Power-Current Characteristic

A typical CW VCSEL power-current (P-I) characteristic is shown in Figure 2.10. Much can be ascertained from the P-I curve and labelled in Figure 2.10 is the threshold current, I_{th}, external differential efficiency, η_d, peak optical power, P_{max}, and the corresponding current, I_{max}. The point (I_{max},P_{max}) is referred to as the thermal rollover and this represents the current at which a further increase results in a drop in optical power. In this section, these features of the P-I curve will be described.

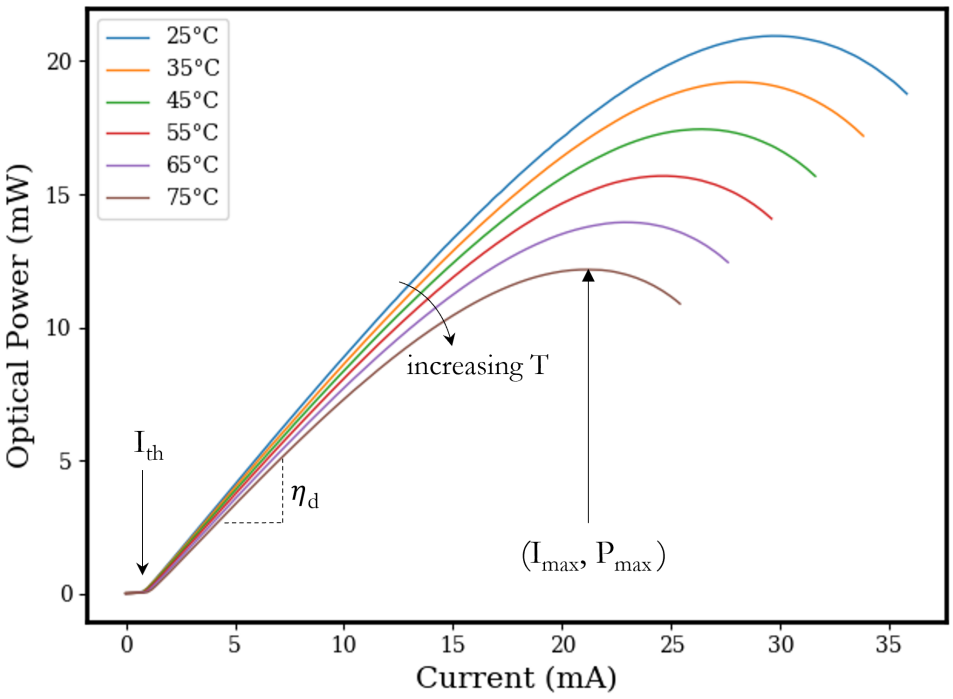

Figure 2.10: Typical VCSEL power-current (P-I) characteristic between 25 and 75°C. Labelled is the threshold current (I_{th}), external differential efficiency (η_d), and thermal rollover point (I_{max},P_{max}).

2.4.1 External Differential Efficiency

The external differential efficiency, sometimes referred to as the slope efficiency, η_d, is a measurable quantity given by the ratio of the optical output power of the VCSEL to the total injected current and is calculated as the gradient of the P-I curve. Multiplication of η_d by $(q/h\nu)$, where $h\nu$ is the photon energy and q is the elementary charge, gives the external differential quantum efficiency, that is, the ratio of the number of photons produced by stimulated emission which are coupled out of the VCSEL to the number of carriers injected above threshold. The external differential efficiency is defined as [39], [64], [65]

$$\eta_{d,ext} = \eta_i \left(\frac{h\nu}{q}\right) \frac{\alpha_m}{\alpha_i + \alpha_m}, \tag{2.17}$$

where η_i is the internal quantum efficiency from Equation 2.13, α_i is the internal optical loss, and α_m is the mirror loss. Here α_i accounts for loss in both the active and passive layers. From this, and assuming the internal quantum efficiency and internal loss are

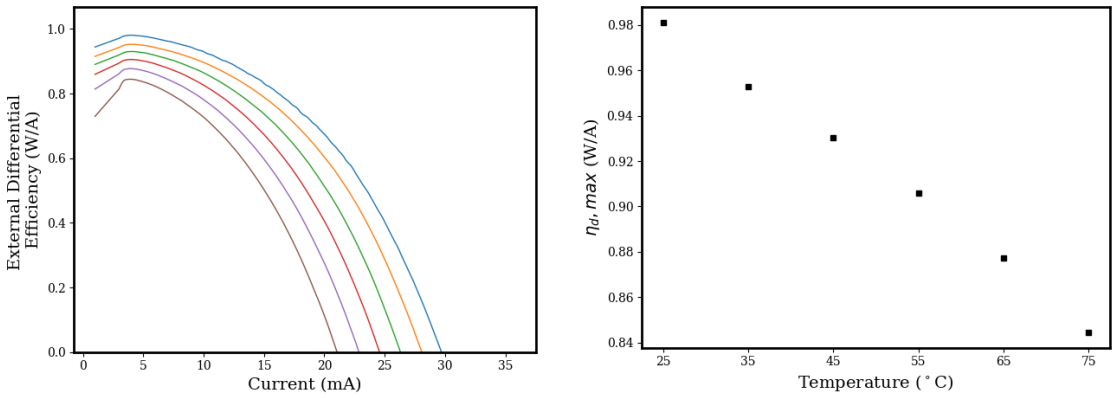

Figure 2.11: External differential efficiency as a function of bias current in in the range 25 to 75 °C (left) and dependence of the peak external differential efficiency on ambient temperature (right).

constant, it can be seen the differential efficiency increases as the mirror loss increases, that is, when the DBR reflectivity is reduced. Hence, one method to improve the differential efficiency is to remove some mirror pairs from the VCSEL stack, however, there is of course a trade off with the resulting increase in the threshold gain.

With Equation 2.17 the optical power above threshold can be written as

$$P_{opt} = \eta_d(I - I_{th}) = \eta_{d,q}\frac{h\nu}{q}(I - I_{th}), \tag{2.18}$$

where $\eta_{d,q}$ is the external differential quantum efficiency, which quantifies the number of photons emitted to the number of carriers injected above threshold. It is evident from Figure 2.10 that the differential efficiency varies with current, and this is shown explicitly in Figure 2.11 (left). The point at which η_d is maximum occurs in the linear region of the P-I curve above threshold, with further increases yielding a drop in efficiency. As the VCSEL approaches thermal rollover, η_d drops rapidly. This is understood as a decrease in η_i due to increased carrier thermalisation and leakage associated with the increasing internal temperature [66], as well as an increase in the optical loss. The effect of increasing temperature can be seen explicitly in Figure 2.11 (right).

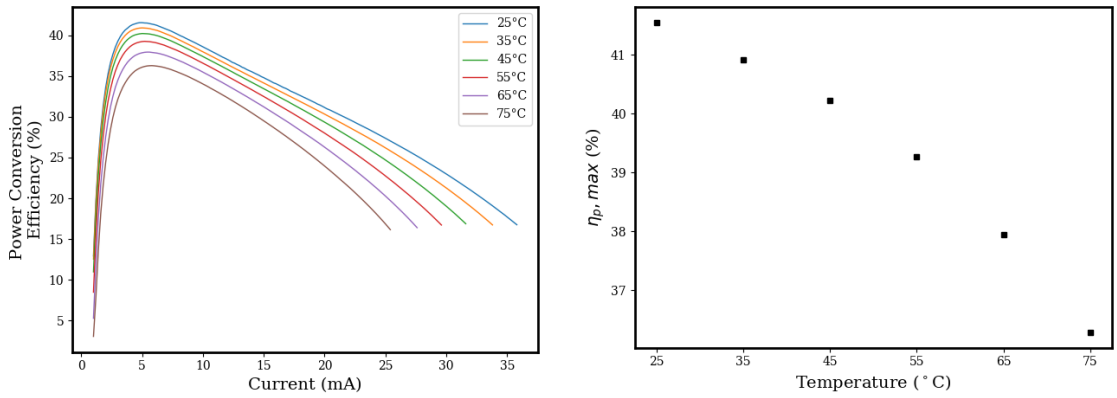

Figure 2.12: Power conversion efficiency as a function of bias current in the range 25 to 75 °C (left) and dependence of the peak power conversion efficiency on ambient temperature (right).

2.4.2 Power Conversion Efficiency

The fraction of total electrical power which is converted into optical power is quantified by the power conversion efficiency, η_p, which can be expressed as

$$\eta_p = \frac{P_{opt}}{IV} = \frac{\eta_d(I - I_{th})}{IV_k + I^2 R_d}, \tag{2.19}$$

where V_k is the kink (turn-on) voltage and R_d is the differential resistance. The differential efficiency has a significant impact on the conversion efficiency which necessitates an appropriate epitaxial design which balances a low absorption loss with a high transmission through the outcoupling mirror. Figure 2.12 shows the dependence of η_p on the bias current for a typical VCSEL, where the shape of the plot is determined by the change in η_d. On the other hand, assuming an equivalent epitaxial structure and a constant η_d, the maximum achievable conversion efficiency is achieved when the ratio $V_k/I_{th}R_d$ is maximised [67]. The kink voltage is principally determined by the junction material and so can be assumed to be constant. Therefore, η_p is maximised when threshold current and electrical resistance are minimised. These quantities are determined by the specific device architecture of the VCSEL.

2.4.3 Thermal Rollover

Self-heating in VCSELs in CW operation leads to a saturation of the optical power at high bias currents which is referred to as thermal rollover. This is shown for the P-I curves in Figure 2.10. The mechanisms of thermal rollover on the microscopic scale are numerous and complex. Baveja, et al., [66] combine an empirical model with experimental measurements to understand the origins from a viewpoint of macroscopic VCSEL parameters and find that, for an AlGaAs-based 850 nm VCSEL, at any ambient temperature, the linear power dissipation exceeds the quadratic power dissipation as the bias current is increased. That is, the effects of carrier leakage, carrier thermalisation, spontaneous recombination, and internal optical loss contribute more to the total power dissipation than the effects of the electrical resistance (Joule heating). They find that the saturation of the optical power is driven by a rapid decrease in the internal quantum efficiency (η_i) driving a sharp increase in the power dissipation associated with carrier leakage. Joule heating nonetheless makes a significant contribution to the internal temperature increase with bias current and its reduction can help delay the onset of carrier leakage-induced power dissipation. Summers, et al, [68] also showed that thermally-activated leakage and carrier broadening is the dominant factor in the power saturation of VCSELs.

The current at which rollover occurs, I_{max}, is strongly dependent on the thermal resistance, and hence the specific device architecture. The internal temperature of small devices increases more rapidly with increasing current, and therefore power saturation occurs at a lower current density. As such, I_{max} scales with the aperture diameter. Further, the optical power at rollover, P_{max}, increases with device size due to the reduced thermal resistance (internal temperature) at a given current density, and this can be seen in the linear relation of peak optical power and corresponding current density of Figure 2.13.

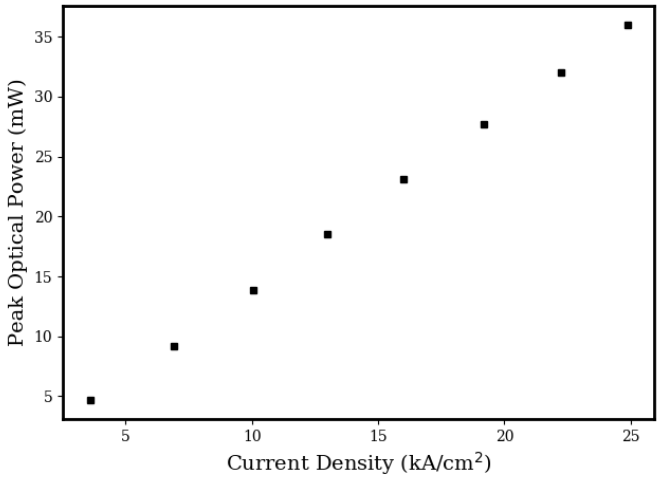

Figure 2.13: Peak optical power and the corresponding current density for devices of increasing aperture diameter.

2.5 Current-Voltage Characteristic

The current-voltage (I-V) characteristic of a VCSEL reveals important information on the electrical performance, related to the diode junction and the series resistance. A typical VCSEL I-V characteristic is displayed in Figure 2.14 (left), with the kink voltage, V_k, and differential resistance, R_{diff}, labelled. The kink voltage is determined by the bandgap at the junction, which is $\sim$ 1.4 V for GaAs. The differential resistance is given by the gradient of the I-V curve (dV/dI). Figure 2.14 (right), shows the corresponding change in R_{diff} with bias current for the I-V curves. As the bias is increased beyond V_k, the differential resistance begins to plateau, although, as the device approaches thermal rollover, R_d drops off due to the high junction temperature as the device is operated CW. Above V_k, the voltage can be approximated by

$$V = V_d + R_s I \tag{2.20}$$

where R_s is the series resistance, and V_d is the junction voltage given by the Shockley ideal diode equation [69]. The series resistance is both voltage and temperature dependent and, in this thesis, is characterised by the differential resistance at a fixed voltage.

Given that current is injected through the DBR layers, VCSELs can have considerable

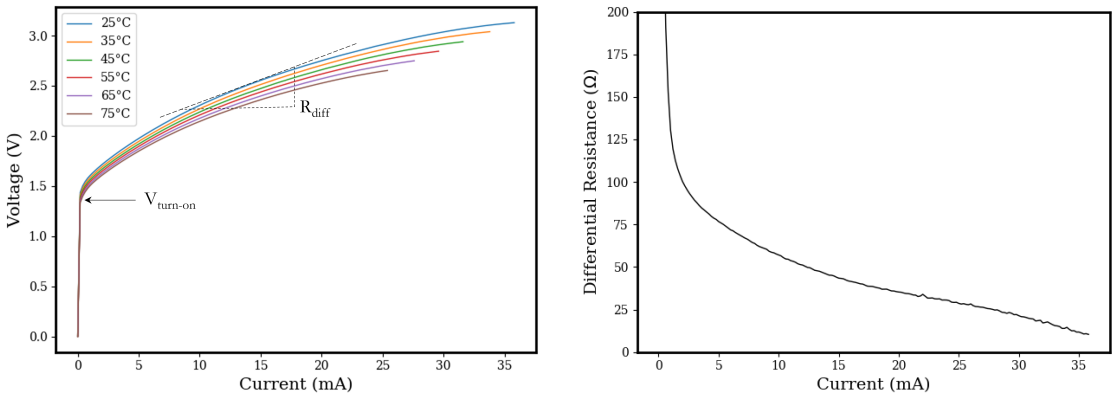

Figure 2.14: VCSEL I-V characteristics between 25 and 75 °C (left) and differential resistance as a function of current (right). Labelled on the I-V characteristic is the kink (turn-on) voltage and the differential resistance derived from the slope of the curve. The differential resistance decreases with increasing ambient temperature resistance is also seen to decrease above approximately 25 mA which corresponds to the thermal rollover current.

series resistances due to the large number of heterointerfaces. Additionally, the layers cannot be too highly doped as this increases the rate of free carrier absorption, which is most significant in the p-type layers due to high rates of inter-valence band absorption. Therefore, there is a trade-off between absorption loss and series resistance in the mirror layers. To combat this, the interfaces of the DBR layers are usually graded in composition which reduces the voltage offset [70], [71] and thus the interface resistance. Additionally, delta-doping schemes may also be employed whereby the doped regions are placed at electric field nodes, thus minimising the absorption loss [72]. The resistance is also sensitive to the specific device geometry and processing. The contact resistance resulting from the formation of Ohmic contacts to the mesa/substrate will also contribute to the total measured resistance. In general, the p-type metallisation will have a higher specific contact resistance, related to the alloying process (discussed further in 3.3.5). Most often the resistance contributions from the metal contacts are negligible in comparison to the contribution from the DBRs. There is a strong dependence on the device size which, from the simplest approximation, arises due to the proportionality of the resistance to the inverse of the active area. As such, R_s is high for small oxide aperture devices and plateaus for large devices, tending to a value determined by the mirror stack.

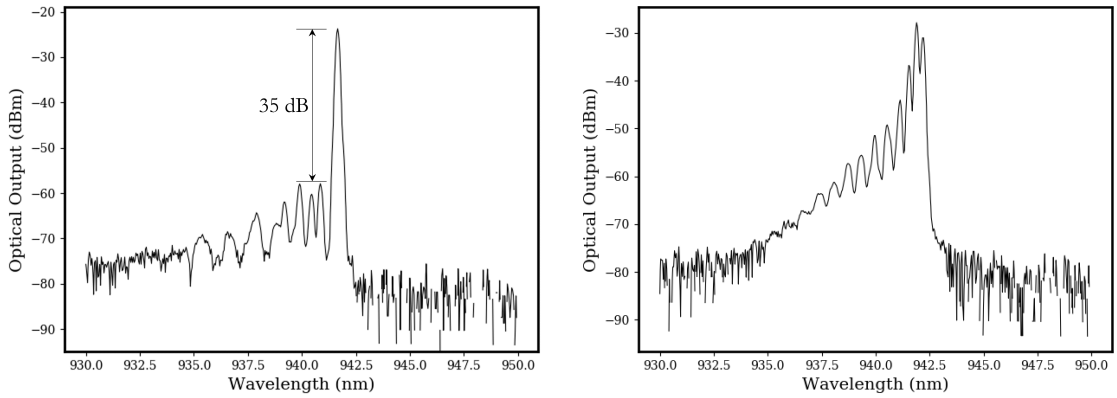

Figure 2.15: VCSEL single-mode (left) and multi-mode (right) emission spectra. The side-modes are suppressed by 35 dB for the single-mode VCSEL. The peaks on the short wavelength side of the multi-mode spectrum correspond to supported transverse modes.

2.6 Emission Spectra

2.6.1 Transverse Modes

Although VCSELs operate intrinsically with a single longitudinal mode, there can be many modes supported in the lateral plane, which can result in a large number of peaks seen in the emission spectra, as in Figure 2.15. The transverse modes of an oxide-confined VCSEL can be described by the linearly-polarised cylindrical waveguide approximation with the low-index (oxidised) cladding region and the high-index (un-oxidised) core. In the simplest case, the VCSEL operates with a single fundamental mode where the intensity profile is approximately Gaussian. Higher-order modes are then supported when the lateral dimensions of the VCSEL is increased. In Figure 2.15 (left) the spectrum of a 3 µm aperture VCSEL just above threshold is shown. Although higher-order modes are present, they are heavily suppressed with a side-mode suppression ratio of $\sim$ 35 dB. Therefore, this VCSEL is considered to be single-mode. Higher-order modes suffer from increased losses for small apertures due to the lack of guiding, which results in the mode suppression seen in the spectrum. When the aperture diameter is increased, this loss reduces and number of side modes increases, along with the optical intensity of the modes, which is evident in the multi-mode spectrum in Figure 2.15 (right).

2.6.2 Wavelength Tuning

2.6.2.1 Wavelength Shift with Temperature

In contrast to EELs, the lasing wavelength of a VCSEL is relatively stable with changes in temperature. The difference is due to the fact that the VCSEL emission wavelength is determined solely by the longitudinal cavity resonance wavelength, as opposed to the wavelength corresponding to the peak gain as in EELs. Hence, the shift in wavelength is driven by the change in optical path length of the cavity with temperature. In this respect, both the refractive index and thickness of the cavity layers change with temperature, although the effect of thermal expansion is negligible [73]. Therefore, the wavelength shift is principally driven by the refractive index change, which for GaAs/AlGaAs in the 300-400 K range varies linearly by ~ 0.07 nm/°C [73].

The emission spectra of a VCSEL measured at 4 mA between 25 and 70 °C is shown in the Figure 2.16 (left). The spectra can be seen to shift to longer wavelengths as the temperature is increased. Additionally, the light output firstly increases and then decreases with increasing temperature and this is due to the change in threshold current as the gain peak detuning changes. The extracted lasing wavelengths are plotted as a function of temperature in Figure 2.16 (right) with the slope is measured as 0.069 nm/°C.

2.6.2.2 Wavelength Shift with Current

The shift of the emission wavelength is determined by the temperature change in the VCSEL stack and, as such, varies for different devices depending on the thermal resistance. Small aperture VCSELs have a high thermal resistance, R_{Th}, thus, for a given increase in current, the wavelength shift is greater than that of a large aperture (lower thermal resistance) device. Differences in the epitaxial structure can also contribute to different rates of self-heating for equivalent geometry VCSEL devices. For instance, a VCSEL produced from an AlAs-based epi-stack will have a lower thermal resistance than that

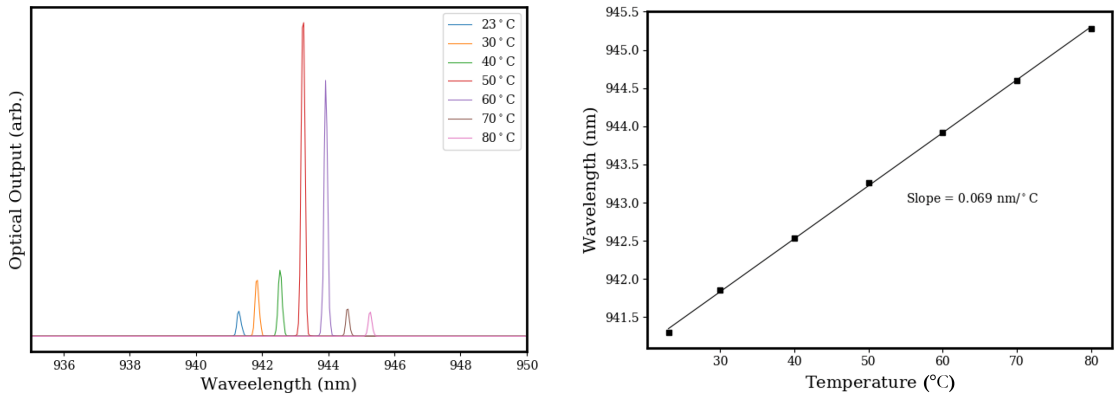

Figure 2.16: Single-mode emission spectra in the range 23 to 80 °C (left) and extracted fundamental mode wavelength as a function of ambient temperature (right). The slope of the linear fit is $\sim$ 0.07 nm/°C and corresponds to the refractive index shift of the constituent epitaxial layers.

of an AlGaAs-based stack due to the higher thermal conductivity of AlAs. Further, the electrical resistance is important. Epi-structures with doping configurations designed to minimise resistance at the heterointerfaces will suffer less from Joule heating than a device with abrupt interfaces. However, for devices produced from equivalent epi-structures, it is the specific device geometry which determines the electrical resistance. To enable representative comparisons, it is useful to extract R_{Th} which can be determined from measurements of the emission spectrum as a function of temperature and consideration of the dissipated power.

2.6.2.3 Thermal Resistance

The thermal resistance represents the temperature change for a given heat flux and can be expressed as

$$R_{Th} = \frac{\Delta T}{\Delta P_{diss}} \tag{2.21}$$

where ΔT is the temperature shift and ΔP_{diss} is the change in dissipated power. As mentioned, the redshift of the fundamental mode wavelength depends solely on the internal temperature of the VCSEL and as such can be used to quantify ΔT. From the technique used in [74], it is possible to determine the VCSEL thermal resistance from CW measure-

ments of the wavelength shift with temperature and dissipated power. The dissipated power is taken as the total power supplied minus the optical power, $P_{diss} = IV - P_{opt}$, therefore, Equation 2.21 can be rewritten as

$$R_{Th} = \frac{\Delta T}{\Delta P_{diss}} = \frac{\Delta\lambda/\Delta P_{diss}}{\Delta\lambda/\Delta T} \tag{2.22}$$

From section 2.6.2.1, the wavelength shift of the fundamental mode is determined by the refractive index shift of the constituent layers of the stack and is ~ 0.07 nm/°C. In [75], a method for calculation of the thermal resistance of VCSELs from CW laser measurements is presented. By measuring the wavelength shift as a function of dissipated power at a range of ambient temperatures, the temperature-dependence of R_{Th} is accounted for. From this, a component of R_{Th} which is determined by the device structure only can be extracted which allows comparison between different device designs. By determination of the wavelength shift as a function of CW dissipated power, the thermal resistance can be extracted. Therefore, it is also possible to calculate and estimated a temperature increase per unit current, which can be used to compare the thermal performance of different device architectures and epitaxial structures.

2.7 Summary

The key details from this chapter are summarised here. There are three fundamental features of a laser: a pump source, a gain medium, and optical feedback. VCSELs are most often electrically pumped, and the optical feedback is typically provided by epitaxially grown distributed Bragg reflector mirrors. The thickness and composition of these layers, as well as the total number of Bragg pairs, determine the spectral-dependence of the mirror reflectivity. The VCSEL gain medium is buried epitaxially between two Bragg mirrors to form a resonant cavity. The thickness of the cavity is typically an integer multiple of half the material wavelength and this determines the VCSEL emission wavelength. Due to the short cavity length, VCSELs are inherently single longitudinal mode. Shifts

in the optical path length of the cavity (driven by changes in the thickness or composition of the constituent epi-layers) result in shifts of the lasing wavelength. The active medium for a VCSEL is typically a multiple-quantum well, the thickness and composition of which determines the photon energy resulting from electron-hole recombination in the well. This determines the spontaneous emission spectrum of the VCSEL and ultimately the spectral dependence of gain. The quality of the active layers can be probed by PL, however, the link between the PL peak and gain spectrum peak is non-trivial and, as such, the PL wavelength is most often used as a growth calibration parameter. Both optical and electrical confinement in VCSELs are realised by the selective oxidation of high-Al composition layers buried in the DBR mirrors. By oxidising these layers, a low index region forms, confining the optical mode to the central, high-index region of the VCSELs. Further, the oxidised region is also highly resistive, which funnels current through the centre of the device. The employment of this processing strategy has led to the reduction of the active volume of VCSELs, facilitating sub-mA threshold currents. The threshold carrier density of a VCSEL is dependent on the alignment of the gain spectrum with the cavity resonance wavelength. This leads to a temperature-dependent threshold current, with a minima occurring when the resonance wavelength aligns with the spectral peak of the gain.

A VCSEL can be well-characterised by measurement of the power-current-voltage curves and the emission spectra. The differential resistance is determined from the slope of the I-V curve above turn-on and decreases with increasing bias current and temperature. The threshold current is the current that flows at threshold gain, and this is extracted form the P-I curve as the turn-on point at which the optical power increases dramatically. If there is low self-heating, the optical power above threshold depends linearly on the bias current. The external differential quantum efficiency is derived from the slope of the P-I relation and this characterises the ratio of the number of photons coupled out of the device to the number of carriers injected in above threshold. This depends on the internal quantum efficiency, the internal optical loss, and the transmission through the mirrors. The power conversion efficiency is the ratio of the optical power (P) to the total electrical

power (I*V) and this is dependent on both the differential quantum efficiency and the electrical resistance. VCSELs are generally operated CW, which results in a 'thermal rollover' whereby the optical power saturates due to self-heating. The current (density) at which this occurs can be used to assess the thermal performance of devices. Although operating with a single longitudinal mode, many modes can be supported in the lateral plane. Often the emission spectra of a VCSEL will contain many peaks corresponding to the separate transverse modes. The lasing wavelength shifts by ~ 0.07 nm/°C which is determined by the refractive index shift of the constituent layers. The thermal resistance can be evaluated from measurement of the wavelength shift with dissipated power, using the known shift with temperature to calibrate the internal temperature increase for a given increase in power dissipation.

In summary, this chapter presented the fundamentals of VCSELs, including laser principles, the typical structure of VCSELs and their output characteristics from power-current-voltage and spectral measurements.

Chapter 3

VCSEL Wafer Production & Characterisation Techniques

3.1 Introduction

In this chapter, the background and underlying principles of volume VCSEL wafer production including epitaxial growth and wafer processing is presented. The first section provides information on the MOVPE growth of VCSELs, including an overview of the MOVPE process, reactor conditions, and sources of variation, as well as a description of the epitaxial structures produced for this thesis. The next section describes the fundamentals of wafer processing, including photolithography, dry etch, selective oxidation, dielectric planarisation, and metallisation, as well as a description of the specific processing used to fabricate devices for this thesis. Finally, descriptions of experimental methods are given.

3.2 MOVPE Growth of VCSEL Wafers

3.2.1 Why MOVPE?

Metal-organic vapour-phase epitaxy (MOVPE) is the commercial-standard growth technique used for the production of VCSEL wafers. MOVPE as a technology has been greatly refined since the early research [76], [77] and the work carried out in the late 1970s demonstrated that MOVPE could be used to produce the high-quality epitaxial layers required for the growth of diode laser structures [78]–[80]. The time of this work coincided with the conceptualisation and realisation of surface emitting lasers, but it was not until the late 1980s that MOVPE was used to produce a VCSEL [81], [82]. As of today, commercial MOVPE reactors are mature, with the capacity of growing 8×6-inch or 5×8-inch VCSEL wafers with a high-degree of layer uniformity. The attraction of MOVPE, and the reason for it being the growth technology of choice for VCSEL production is its suitability to volume production. For a market-driven technology like VCSELs, large-scale production is more economical, and the high growth rates and material yields afforded by MOVPE offer comparatively lower production costs.

3.2.2 The MOVPE Process

3.2.2.1 Overview

The process of MOVPE involves the injection of organometallic precursor gases into a reactor chamber at moderate pressures. As opposed to physical deposition techniques like MBE, the growth of epitaxial layers in MOVPE occurs by chemical reaction at the semiconductor substrate surface. For the growth of InAlGaAs alloys, the precursor gases used are most often trimethylindium (TMI), trimethylaluminium (TMA), trimethylgallium (TMG), and arsine. As the precursor gases approach the substrate surface, pyrolysis occurs, and the subspecies adsorb onto the semiconductor surface. Subsequent surface

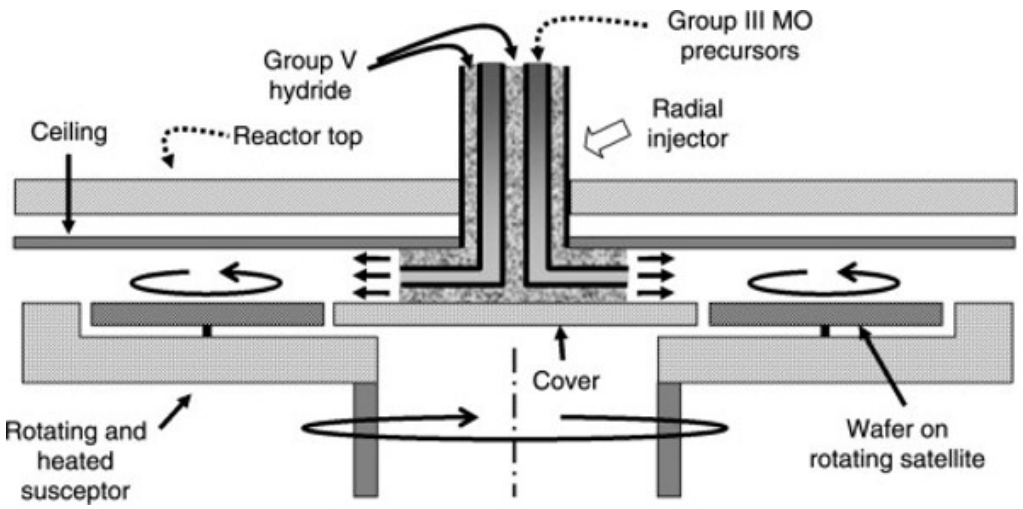

Figure 3.1: Diagram of a Planetary Reactor MOVPE mass production system. Metalorganic precursors are injected through the centre of the reactor, creating a horizontal radial gas flow over rotating substrates. Reproduced with permission from [85].

kinetics result in the formation of crystalline epitaxial layers, whilst by-products are desorbed and evacuated from the chamber. The temperatures required for MOVPE growth are usually between 550 and 750°C [83], with the chemical bond of the precursor gas determining the required temperature.

3.2.2.2 Reactor Design

Historically, there have been several approaches to MOVPE reactor design [83], but the focus here will be the Planetary Reactor marketed by Aixtron [84]. These reactors rely on horizontal laminar flow, with the metal-organic precursor gases entering the chamber through a gas inlet in the centre of the reactor, with the group III and V precursors injected through separate flow channels to prevent premature reactions. The gas flows radially from centre to edge, passing over the heated semiconductor substrates which are seated in a graphite susceptor. Both the susceptor and each individual wafer rotates during growth to ensure a uniform gas flow rate over the wafers. The reactor temperature is controlled by an RF inductive heater. A simple schematic for the reactor described is given in Figure 3.1.

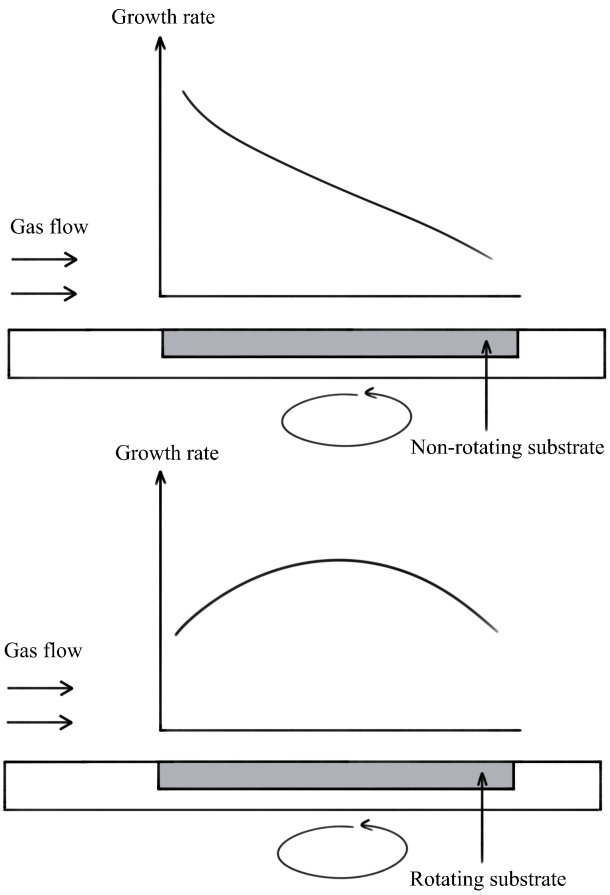

Figure 3.2: Growth rate variation across a rotating and non-rotating substrate.

3.2.3 Growth Conditions

The MOVPE process is complex and high-quality growth relies on the precise control of many conditions within the reactor; growth temperature, reactor pressure, gas flow rate, V-III precursor ratio. These conditions determine the properties of the deposited material (layer thickness, composition, doping concentration, defect density), some of which are monitored in-situ. A high growth rate (between 4 and 20 Å/s) can introduce defects and dislocations [36], which will degrade the performance of laser devices. Several experimental and modelling studies into MOVPE growth reactor conditions for VCSEL production have been performed. From [86] and [87], the importance of substrate rotation is evident. There is a significant non-uniformity in growth rate across the wafer resulting from the gas inlet at the centre of the reactor, however, rotation of the individual wafers in the satellites results in an averaging of the growth rate, as first described in [88]. In

[89], the temperature of wafers during growth in an Aixtron 8×6 Planetary Reactor is measured and shown to vary radially. Also measured is the curvature for each wafer in the reactor and some correlation with the temperature distribution is seen, with the lowest curvature wafer resulting in the highest average temperature, although some high curvature wafers are still seen to have uniform temperature distributions. The subject of wafer bow/curvature will be covered in the next section. Even with a uniform temperature distribution across the wafer, a horizontal variation of growth rate within the reactor can still result in a radial variation of the properties of the wafer, and this is illustrated in Figure 3.2.

3.2.4 Wafer Bow

The lattice constants of GaAs and AlAs are shown in Figure 3.3. There is a finite mismatch of $\sim 0.14\%$ which, for a VCSEL structure with > 100 layers, results in a large compressive strain. This is particularly an issue for structures containing AlAs layers (which is common in the bottom DBR for improved thermal performance). The compressive strain translates into a significant wafer bow which increases as the wafer diameter is increased. Growth on Ge has received attention recently due to its favourable properties [90], including a lattice constant closer to AlAs, and the growth of VCSEL epi-structures on Ge have been shown to result in negligible wafer bow [10], [91]. A comparison of the height variation of a 6-inch GaAs and Ge substrate VCSEL wafer is reproduced from [91] and shown in Figure 3.4. The maximum height variation of a Ge wafer is ~ 25 µm, compared to ~ 130 µm for the GaAs wafer. The GaAs wafer displays a convex bow relative to the $z = 0$ plane with the maximum height at the centre of the wafer. As a rule of thumb, the bow of a GaAs VCSEL wafer is approximately 0.1% of the wafer diameter; that is, ~ 100 µm for a 4-inch (100 mm) wafer and ~ 200 µm for 8-inch (200 mm). The Ge wafer shows a slight concave warp which is an artifact of the surface height variation of the Ge substrate. The impact of the strain-induced bow of GaAs VCSEL wafers adds complexity and time to the processing of wafers which worsens as the wafer diameter increases. As such, growth

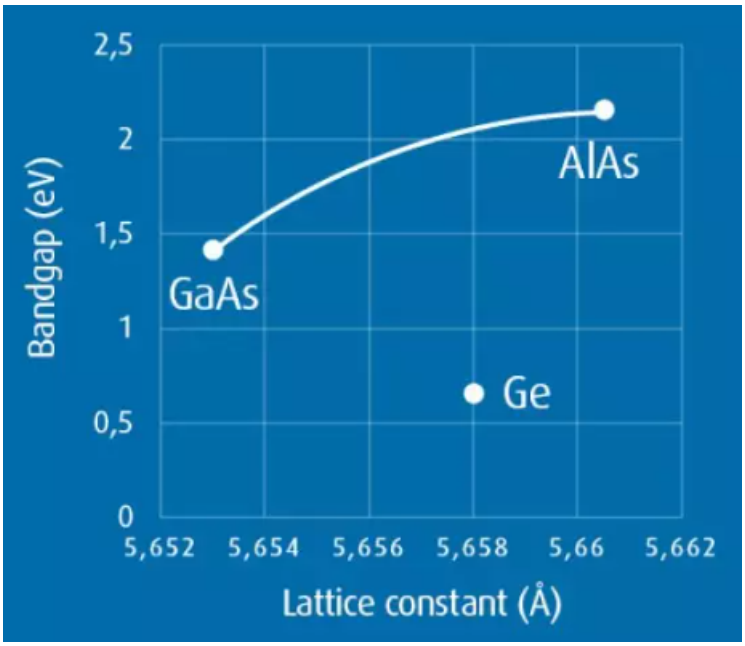

Figure 3.3: Lattice constant of GaAs, AlAs, and Ge. Courtesy of Umicore ©. Growth of AlAs and high-Al AlGaAs on GaAs results in a compressive strain due to the small lattice mismatch. The lattice match with Ge is advantageous for reducing this strain.

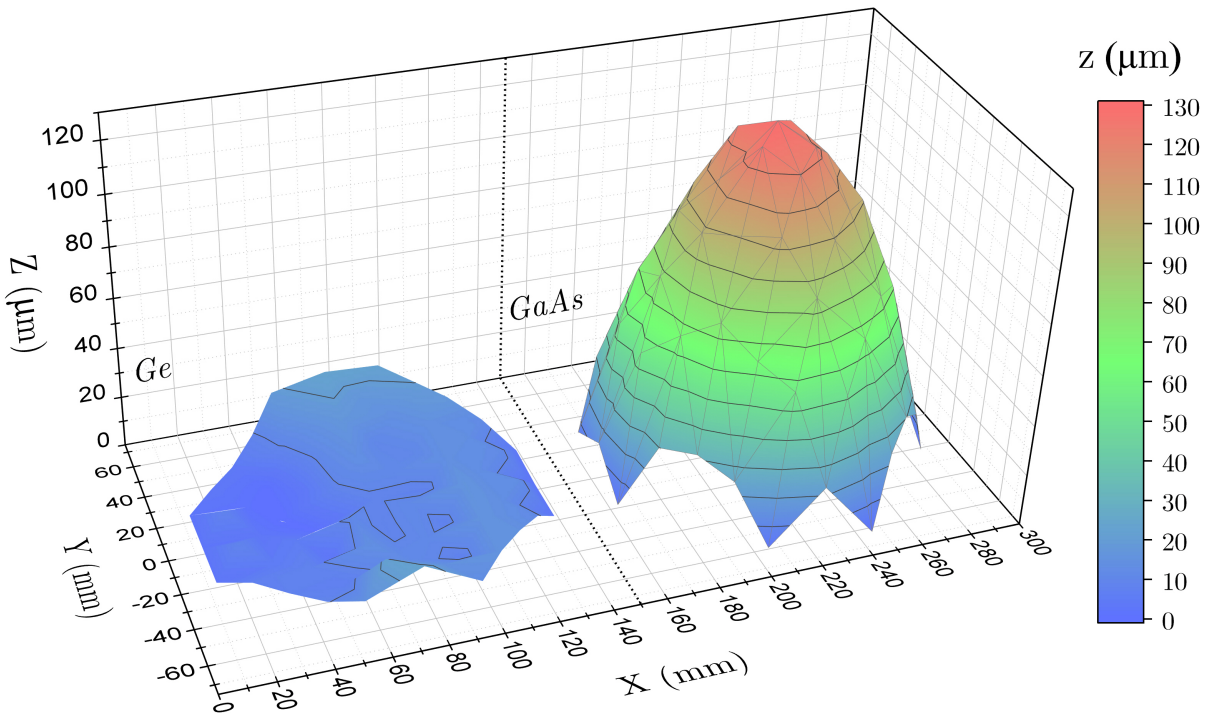

Figure 3.4: The height variation of a 6-inch Ge and GaAs substrate VCSEL wafer. The radial bow for the GaAs wafer is the result of the compressive strain resulting from the growth of AlAs DBR layers on GaAs. The height variation of the Ge wafer is thought to be related only to the height variation of the substrate. Reproduced from [91].

on Ge provides a potential route to facilitate the scale-up of VCSEL production to 200 mm. A detailed description of the advantages of Ge is given in [91]. All epitaxial wafers used in this thesis were designed and grown by IQE.

3.2.5 Epitaxial Structures for this Study

The epitaxial structures used in this thesis are grown with a generic p-i-n layout, designed for 940 nm emission wavelength. This consists of an InGaAs MQW active region sandwiched between an upper p-doped $Al_xGa_{1-x}As/Al_yGa_{1-y}As$ DBR mirror and lower n-doped AlGaAs/AlAs DBR mirror, grown on a 6-inch n-type GaAs substrate. A λ-thick inner-cavity is formed between the DBR mirrors, consisting of the MQW layers and AlGaAs SCH layers. A buried $Al_{0.98}Ga_{0.02}As$ layer is included between the active region and the upper DBR mirror stack, which is used to provide electrical confinement and optical guiding following selective wet oxidation (section 3.3.3). Nominally equivalent epitaxial structures are also grown on 6-inch Ge substrates.

3.3 Wafer Processing

Processing of VCSEL epitaxial material varies greatly depending on the intended application. In the most general case, VCSEL fabrication includes the definition of a cylindrical mesa, formation of the lateral geometry of the optical cavity, passivation and planarisation of the mesa sidewalls, and definition of electrical contacts to the p and n sides of the epitaxial structure. The devices produced for this work were fabricated using standard techniques at the Institute for Compound Semiconductors (ICS) cleanroom at Cardiff University. The tools in the ICS cleanroom were acquired to match industry standards and, as such, the processing techniques used are similar to those employed in commercial settings. Acknowledgement for wafer processing and development work is gratefully given to my colleagues Dr Sara Gillgrass of Cardiff University and Dr Tomas Peach of the

Institute for Compound Semiconductors.

3.3.1 Optical Lithography

For all the devices characterised in this thesis, optical lithography is used to transfer a mask pattern to the epitaxial material for definition of the individual VCSEL structures via dry-etching (described below in section 3.3.2). A single layer coating consisting of the positive-tone resist AZ10XT is spin-coated on the wafer at 3000 rpm for 45s to achieve a thickness of ~ 7 µm. The mask pattern is then transferred to the resist by exposure to UV light and subsequent development in AZ400K and this is used as the etch mask. Lift-off processes are used for patterning metals. In this case, a single layer coating of the negative-tone resist AZ2070 is spin-coated at 4000 rpm for 45s resulting in a thickness of ~ 5 µm. The pattern is exposed onto the sample and the resist is baked at 110°C before development in AZ726 to open up the regions for metal deposition. When the remaining un-developed resist is removed, the unwanted metal is removed with it, leaving the intended metal pattern deposited on the semiconductor surface.

3.3.2 Mesa Etch

The formation of vertical mesa sidewalls is an important consideration which requires a highly anisotropic and directional etch. The simplest and fastest method - 'wet' etching (submerging the sample in a chemical etchant) - is inherently isotropic with an etch rate dependent on the crystal orientation. This results in an undercut of the etch mask by a distance comparable to the depth of the etch when a deep etch (several microns) is required [45]. As such, dry etch techniques, which utilise mechanisms of both chemical reaction and physical bombardment, are favoured. For this thesis, an Oxford Instruments PlasmaPro 100 Cobra Plasma Etch Tool is used for mesa isolation by ICP-RIE etching with a Cl-based gas chemistry. The ICP tool is equipped with a laser interferometer for in-situ monitoring of the etch into the VCSEL epi-structure, enabling depth control to

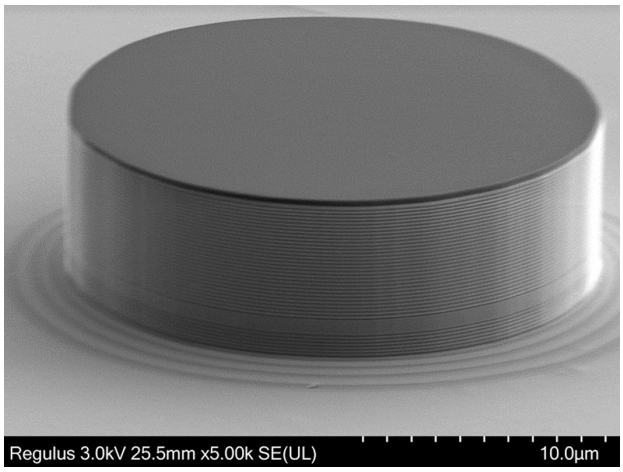

Figure 3.5: A SEM image of a VCSEL mesa. The deep etch and vertical sidewalls are achieved by ICP-RIE etch with a Cl-based gas chemistry.

individual layers in the stack. The etch is typically 3-5 µm, depending on the particular structure, deep enough to expose the high-Al oxidation layer (section 3.3.3) and the active region. For a typical top-emitting 940 nm VCSEL, there is a tolerance of ± 0.2 µm beyond which the AlAs layers in the bottom DBR are exposed. These layers oxidise rapidly during the selective oxidation process which can severely limit yield. Under-etching of the mesa can be detrimental to device performance if either the active region or oxidation layer are not exposed. The etch depth uniformity for the 6-inch VCSEL wafers processed by the Institute for Compound Semiconductors for this thesis is $\sim$ 2% and which results in a 100% device yield. An etched VCSEL mesa is shown in Figure 3.5.

3.3.3 Selective Oxidation of AlGaAs

One of the major advances in the performance of VCSELs came from the electrical and optical confinement afforded by the incorporation of selectively oxidised AlGaAs layers in the epitaxial stack [19], [51], [74], [92], [93]. The lateral formation of Al-oxide funnels carriers through the centre of the VCSEL mesa [50], whilst the low refractive index [94] provides index-guiding, thus also confining the optical mode to the centre of the VCSEL mesa [49]. The principle of selective oxidation of AlGaAs is based on the exposure of high Al composition layers to a water vapour saturated inert gas environment (N2/H2)

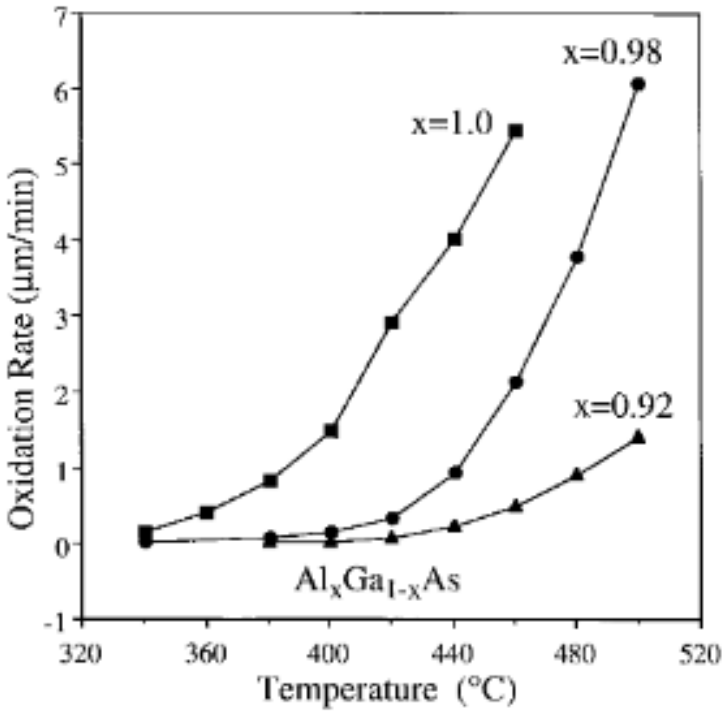

Figure 3.6: The dependence of AlGaAs oxidation rate on temperature. Reproduced with permissions from Choquette, et al. (1997) [95] IEEE ©

at an elevated temperature. To achieve reproducible results requires tight control of the variables which affect the oxidation rate. This includes the gas composition, flow rate, ambient and substrate temperature, as well as the Al mole fraction of the AlGaAs layer and its thickness - the latter variables being determined by the epitaxial growth. Much work has been done to characterise the impact of these variables on the oxidation rate, some of which is reproduced here from [96]. Figure 3.6 shows the exponential dependence of the oxidation rate on temperature for different Al mole fractions. As such, a relatively small temperature variation of the substrate in the oxidation furnace (a few °C) can lead to significant variations in the oxidation rate across the wafer. The wafer-scale variation of the oxidation extent is examined in detail in Chapter 5. Furthermore, from the same plot, it is evident that the oxidation rate is also highly sensitive to the layer composition, with a higher Al mole fraction yielding a faster oxidation. This can be understood from Figure 3.7 where the oxidation activation energies and resulting oxidation rates of different AlGaAs compositions are shown. The oxidation rate at 420 °C is demonstrated to change by three orders of magnitude as the Al mole fraction is changed from 0.82 to 1.00. This sensitivity

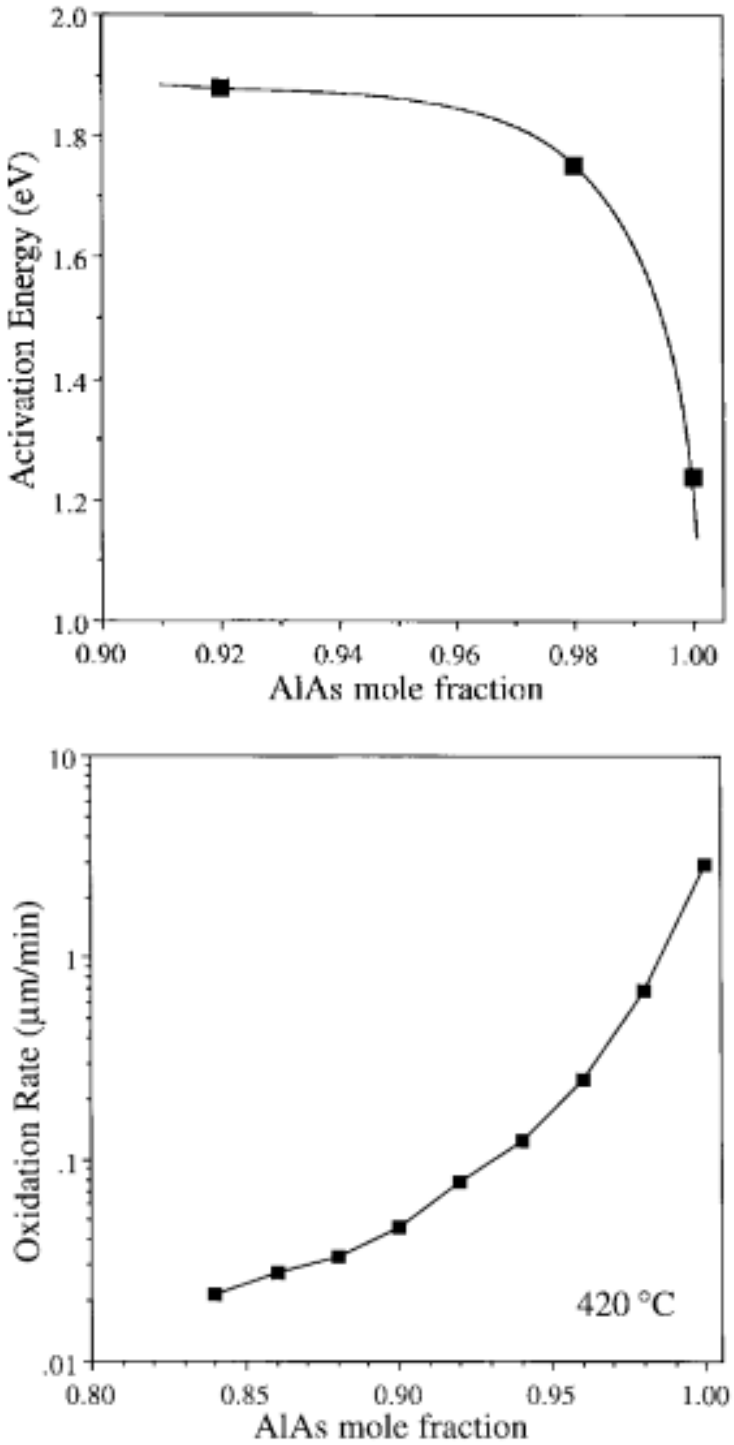

Figure 3.7: The dependence of AlGaAs oxidation rate on Al mole fraction. The dependence of the oxidation rate on Al mole fraction is the result of the change in activation energy (top). For a fixed temperature, the oxidation rate varies exponentially with Al mole fraction (bottom). Reproduced with permissions from Choquette, et al. (1997) [95] IEEE ©

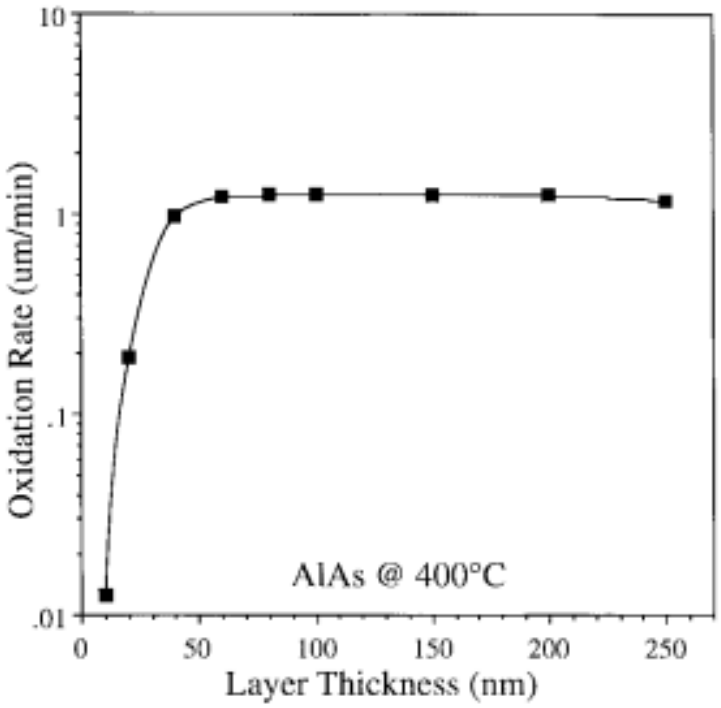

Figure 3.8: The dependence of AlGaAs oxidation rate on layer thickness. For layer thicknesses less than 60 nm, the oxidation rate is sensitive to fluctuations in layer thickness. Reproduced with permissions from Choquette, et al. (1997) [95] IEEE ©

to compositional change is what makes the process highly selective and perfectly suited for VCSELs where the oxidation layer is buried in the epitaxial structure. The thickness of the layer also impacts the oxidation rate, as shown in Figure 3.8 for an AlAs layer clad by GaAs. The rate is greatly reduced for thin layers and is stable for thicknesses greater than $\sim$ 60 nm – it should also be noted that the composition of the surrounding layers also affects the oxidation rate. Therefore, in conjunction with the furnace conditions, any compositional and layer thickness variations across the epitaxial-wafer will, therefore, also result in variation in the oxidation rate (hence VCSEL oxide aperture). For this thesis, oxidation was performed on both an Aloxtec (conduction-based) Wet Oxidation Furnace and a Tystar (convection-based) High Temperature Oxidation Furnace. The former handles individual wafers up to 6-inch diameter with the substrate temperature controlled by thermal contact with a heated chuck. The Aloxtec furnace is equipped with an infrared camera for in-situ monitoring allowing real-time measurement of the oxidation extent with an error of $\pm$ 0.5 µm and, as such, is well suited for research &

development. The Tystar furnace has capacity for multiple wafers up to 8-inch diameter with the substrate temperature determined by the furnace ambient temperature. This furnace requires a calibration run on sacrificial material and is most often used for volume production. These furnaces will be subsequently referred to as conduction-based (Aloxtec) and convection-based (Tystar), respectively.

3.3.4 Planarisation

One drawback of the buried nature of the oxidation layers in a VCSEL is the non-planarity that results from the mesa etch. Early on, this challenge was overcome by subsequently planarising the VCSEL mesa using polyimide [70], [97], and, since then, benzocyclobutene (BCB) [98], [99] or SiN_x. For this thesis, the focus is on devices planarised with BCB due to its relatively simple processing, that is, in comparison to PECVD-based SiN_x (despite Nitride deposition being more highly favoured for volume applications [100]). A description of the advantages of BCB for VCSELs is given in [101]. It has also been reported that BCB works to passivate the mesa sidewalls [102] by reducing the number of dangling bond surface states [103], and hence the rate of non-radiative surface recombination.

In this work, the planarisation is carried out by first spin-coating BCB at 4000 rpm for 45s resulting in a layer of 6-7 µm on the wafer surface after curing at 210°C for 40 mins. A second layer of BCB is spin-coated at 2000 rpm to result in a 10 µm thick covering on the surface after curing. The BCB is subsequently etched-back to the height of the mesa by RIE at a rate of $\sim$ 0.25 µm/min. Across a 6-inch wafer, a significant variation of either the mesa etch depth or the BCB etch-back can limit device yield. A step height greater than the thickness of the metal between the mesa height and BCB (in this case 0.3 µm) results in discontinuity between the ring contact and metal feed.

Reproducing from [104]; the need for planarity in VCSEL fabrication adds complexity to the processing and the planarisation process itself can be quite time consuming. There have been attempts to produce planar VCSELs by utilising the electrical isolation provided by the selective oxidation process. One approach, used in [105], produces an array

of individually addressable oxide confined VCSELs. The performance of these devices is both electrically and optically uniform, although a deep oxidation is required for simultaneous definition of the laser aperture and electrical isolation of the contact pad. In [106] and [107], via holes are etched to expose the high Al-content oxidation layer for definition of the VCSEL aperture/isolation of the contact pad, however, in both cases ion-implantation is also required. A high-density VCSEL array is produced in [108] by selective oxidation, with the apertures defined by a hexagonal grid of etched via holes, although this process requires a transparent p-metal. Definition of the VCSEL mesa by continuous and non-continuous ring trench etching is studied in [109] and it is shown that favourable thermal properties can be achieved. However, with this design there is still the need for deposition of a dielectric layer to electrically isolate the interconnect and contact pad. In Chapter 4, the development of a method to rapidly produce VCSELs without the need for planarisation is described, whereby the device architecture is designed to minimise the processing time at all stages.

3.3.5 Ohmic Contact Formation

To facilitate electrical pumping of the VCSEL it is necessary to form electrical contacts to the highly p-doped and n-doped layers. In the simplest case, one contact is deposited on the top surface of the mesa and a global contact is deposited on the substrate side. This ceases to apply for structures grown on semi-insulating substrates, in which case both contacts are deposited on the emission side and, as such, the contact configuration is referred to as 'co-planar.' For most of the purposes of this thesis, devices employ an emission side (p-type) ring contact deposited on the p^+ doped GaAs cap of the mesa and a global (n-type) contact deposited on a n^+ doped GaAs substrate.

Two key considerations are taken for the formation of electrical contacts to GaAs: the contacts must be Ohmic (non-rectifying) and there must be adequate adhesion to the surface. For an Ohmic contact to p-type GaAs, the deposited metal most often consists of a thin-layer deposition of Ti and Pt or Cr followed by a thick layer of Au. After

thermal annealing, the alloying of the Ti/Pt or Cr atoms into the doped GaAs reduces the potential barrier at the interface and facilitates an Ohmic semiconductor-metal junction. For a contact to n-type GaAs, the deposited metal is usually a three-layer deposition of AuGe, Ni, and Au and, similarly, after annealing the Ga and Ge inter-diffuse. Ni is included to aid this process and to improve surface morphology [110]. For efficient injection of carriers into the VCSEL, the contact resistance must be minimised (typically $< 10^{-5}$ Ωcm^2 [34]).

For this work, deposition of p- and n-type metal contacts is performed using a Kurt J Lesker PVD tool, equipped with both thermal and e-beam sources for evaporation of the source material. Some device designs (detailed in Chapter 4) require a dielectric layer for electrical isolation and for this SiO_2 is deposited by e-beam evaporation. Contacts to p-type GaAs are made by deposition of Ti/Au or Cr/Au to a thickness of 10/300 nm. Contacts to n-type GaAs are made with AuGe/Ni/Au to a thickness of 100/28/300 nm. Patterning of the metal contacts is done via a lift-off process described in section 3.3.1. Figure 3.9 shows the contact resistance variation for emission-side p-contact metal across a 6-inch wafer processed at the Institute for Compound Semiconductors. These measurements are derived from wafer-scale mapping of C-TLM [111] structures. A low contact resistance is achieved across the the entirety of the wafer, with values kept below 2×10^{-6} Ω/cm^2.

3.4 Epi-Wafer and Device Characterisation

The measurements performed for this thesis can be divided into two groups: post-growth material characterisation and VCSEL device characterisation. Material characterisation refers to measurement of un-processed epitaxial material and this constitutes the standard metrology carried out by the wafer manufacturer in line with the production process. Credit for post-growth characterisation (PL and reflectivity) is gratefully given to colleagues at IQE. Device characterisation refers to measurement of processed VCSELs

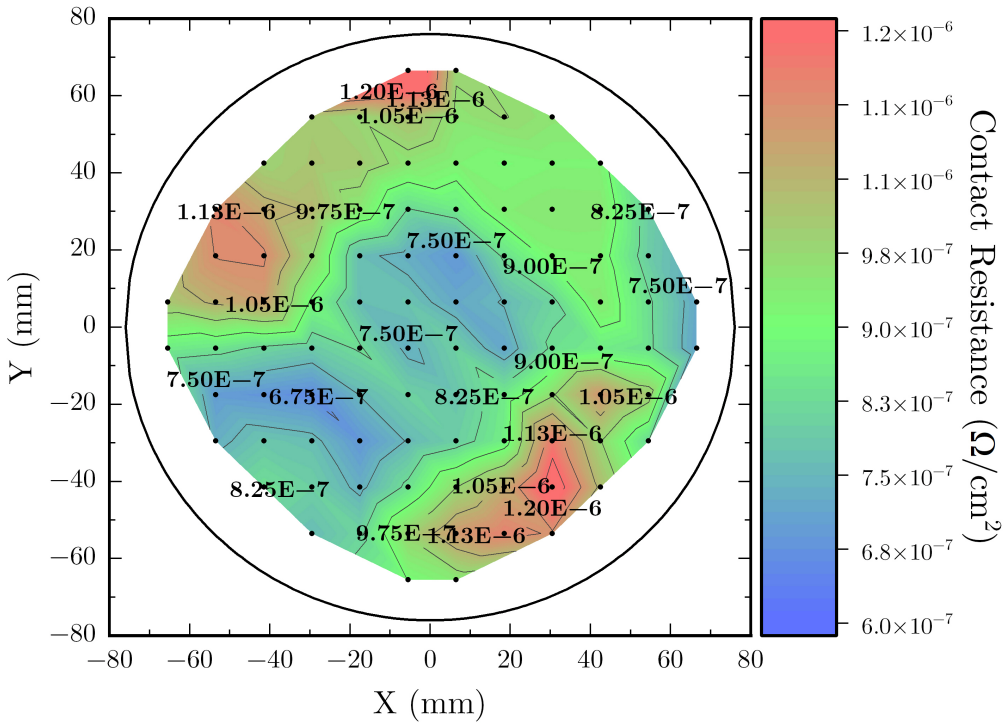

Figure 3.9: Contact resistance variation on a 6-inch VCSEL wafer measured by C-TLM. The contact resistance of the p-contact metallisation is below $1 \times 10^{-6}\Omega/\text{cm}^2$ across the entire wafer.

(see Chapter 4 for device structures), which, in the context of this thesis, are standard characterisation practises, so as to be compatible with commercial settings. As such, the principal measurements carried out are of the power-current-voltage characteristics and of the emission spectra. The experimental setups and procedures for each are described in the remainder of this chapter.

3.4.1 Reflectometry

One of the most powerful characterisation techniques for VCSELs is the measurement of the reflectivity spectrum, which provides information on the FP cavity resonance and characteristics of the DBR stopband. One of the main advantages is that this technique is non-destructive and can be performed on as-grown epi-structures [45], [112]. Hence, in a VCSEL wafer foundry setting, these measurements can be carried out at thousands of locations on every wafer produced to form detailed wafer-maps. This is routinely used

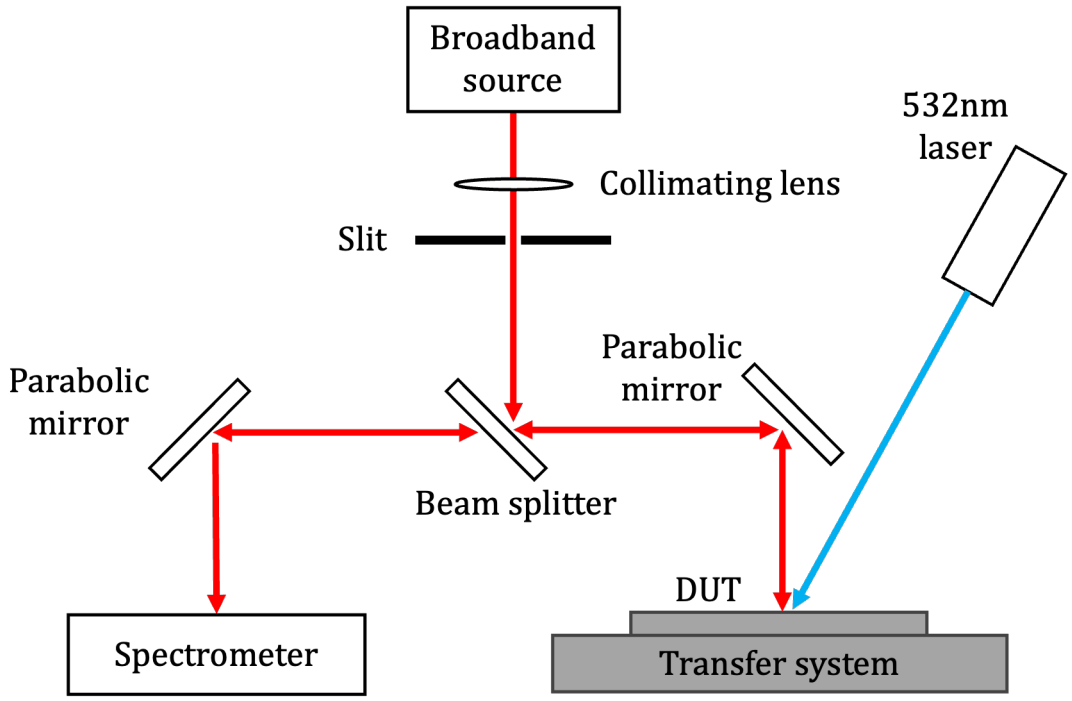

Figure 3.10: Simplified schematic of the mapping setup used for measurement of VCSEL photoluminescence and reflectivity spectra.

as a method of assessing material quality and uniformity, tracking drift from run-to-run, and evaluating epi-structure designs and growth recipes.

The stopband shape, width, and centre wavelength can be compared to pre-growth simulations to assess the quality of the growth, with deviations from the simulated reflectivity spectra indicating mismatches between the top and bottom $\lambda/4$ layers and the cap/sub-cap layer thickness which affects the phase condition.

For this study, measurements are carried out on whole unprocessed wafers on a Nanometrics RPM PL Wafer Mapping System equipped with an integrated broadband light source. The measurements for this work were performed by IQE as part of standard material characterisation methods, in-line with the foundry-process. A simplified schematic of the reflectance mapping system is shown in Figure 3.10. There are some drawbacks to the measurement system, for example, the use of a parabolic mirror to focus the beam at the wafer introduces angular incidence which limits the information provided by the depth and linewidth of the FP resonance.

3.4.2 Photoluminescence

Photoluminescence (PL) is a technique widely employed to measure the properties of QWs and, for VCSELs, is used to assess the quality of the growth of the active region. The PL spectrum provides information on the transition energies of the QW confined states, as well as the radiative efficiency in the well [45]. Spatial mapping of the PL intensity can inform on the defect density, with defect states producing lower intensity responses due to the increase in non-radiative recombination centres. Under the correct conditions, information about the impurity density can also be extracted from the PL linewidth (modifications to the crystal potential (hence transition energies) resulting from charge capture at defect states). The downside of PL is that it cannot be performed on as-grown VCSEL structures. The PL spectra from QWs sandwiched within a full VCSEL structure is significantly influenced by the effects of the DBRs and, as such, light only exits the structure at wavelengths corresponding to the FP cavity resonance or regions of reduced reflectivity outside the stopband [41]. Therefore, for a representative assessment of the QW layers, PL measurements are performed on calibration structures grown without the top DBR, and this is the case for the wafers characterised in this thesis.

Similar to measurement of the reflectivity spectra, the PL is carried out on whole (calibration structure) wafers on a Nanometrics RPM PL Wafer Mapping System with 532 nm wavelength laser source used to excite electrons into high energy states in the conduction band. The emitted light from the subsequent recombination events is guided with the same optics as for the reflectance measurements and directed to a spectrometer. Unlike the information extracted from the reflectivity spectrum, the characteristics of the PL spectrum are not angular dependent, hence the excitation laser beam can be angled towards the wafer, as shown by the blue ray in Figure 3.10. The measurements for this work were performed by IQE as part of standard material characterisation methods, in-line with the foundry-process.

3.4.3 VCSEL Characterisation

The characterisation of VCSEL devices for this thesis was performed both on-wafer and on optical-bench setups, both of which are described here.

Measurements on an optical bench were performed on cleaved samples mounted on a TO-8 header. Up to 15 devices were wire-bonded and electrical contact with a Keithley 2401 current source was made via the header pins. The headers were fixed in place by a copper mount, thermally isolated from the translation stage. A Thorlabs PID temperature controller was used to heat the device from room temperature up to 80°C. The VCSEL optical output power was measured with a Thorlabs integrating sphere connected to a Thorlabs PM100USB power and energy meter, with the sample in close-proximity to the aperture of the sphere to ensure maximum light collection. This is shown in Figure 3.11. Devices were mounted in an equivalent way for the measurement of the emission spectra, with a lens used to collect the diverging beam into a multi-mode fibre, as shown in Figure 3.12. The spectrum was measured by an ANDO optical spectrum analyser with a resolution of 0.1 nm. On-wafer measurements were performed using an MPI semi-automated wafer prober, an image of which is shown in Figure 3.13. Both cleaved samples and whole wafers were mounted on a thermal chuck facilitating temperature control from room temperature up to 200 °C (measurements were only carried out up to 80°C). Samples were fixed in position by vacuum. The chuck also forms the ground for samples with a substrate-side Ohmic contact. Electrical contact to the VCSEL devices was made via tungsten needle probes with a footprint of 2 or 5 µm, as shown in Figure 3.14. Acknowledgement for the production of an in-house LabView automation software is gratefully given to Dr. Richard Forrest and Dr. Craig Allford. The current source was a Keysight B2910BL precision source/measure unit which enabled 4-wire voltage measurements. The light output is collected by an Ophir integrating sphere mounted above the sample and connected to a Newport 1936-R calibrated power meter for optical power measurements. An optical fibre tap from the sphere coupled some light into an Ocean Insight HR4000 CCD spectrometer for measurement of the VCSEL spectra. The

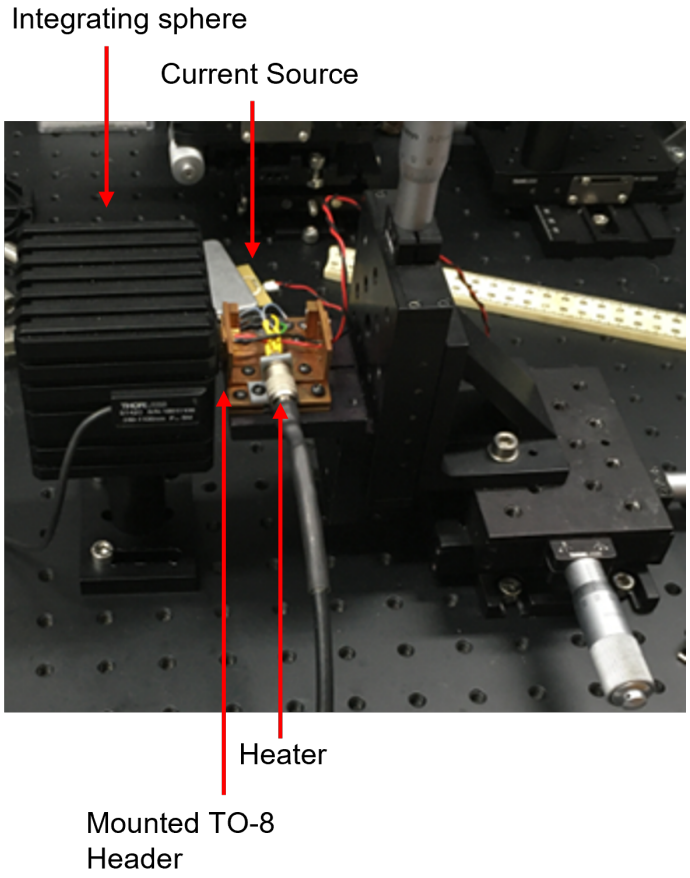

Figure 3.11: Image of optical-bench setup for measurement of VCSEL optical power. Light is directly coupled to a calibrated integrating sphere. A heater controls the temperature up to 80 ^{c}ircC.

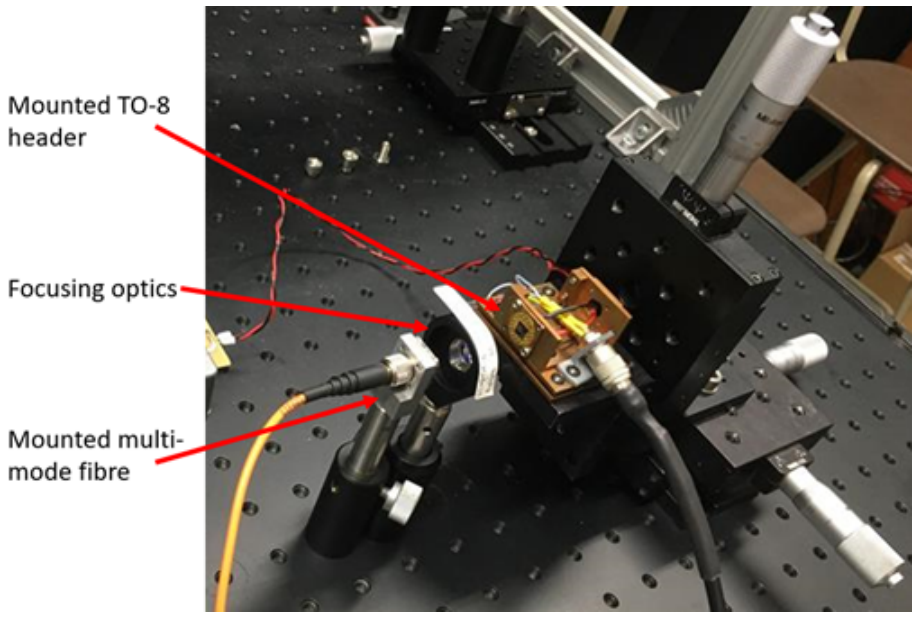

Figure 3.12: Image of optical-bench setup for measurement of VCSEL emission spectra. Light is coupled into a multi-mode fibre via a focussing lens which is connected to an optical spectrum analyser.

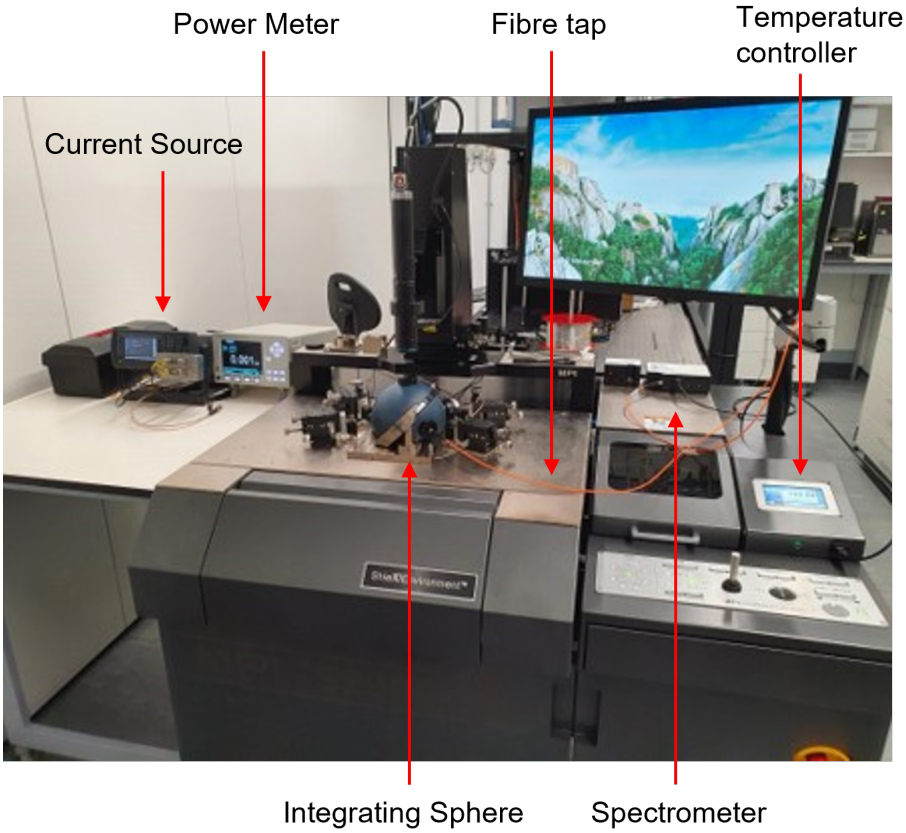

Figure 3.13: Image of wafer-mapping setup. Wafers are mounted on a temperature-controlled chuck which also forms the ground contact for substrate-side contact. Optical power is measured with a calibrated integrating sphere with a fibre-tap connected to a spectrometer for spectral measurements.

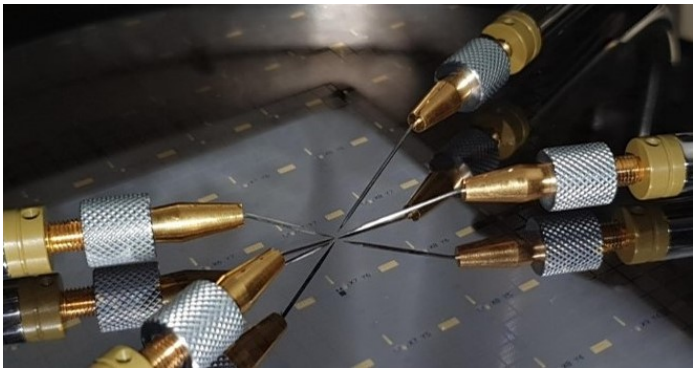

Figure 3.14: Image of a loaded VCSEL wafer. Needle probes with a footprint of 2 or 5 µm are used to contact devices for electrical pumping and 4-wire voltage measurements.

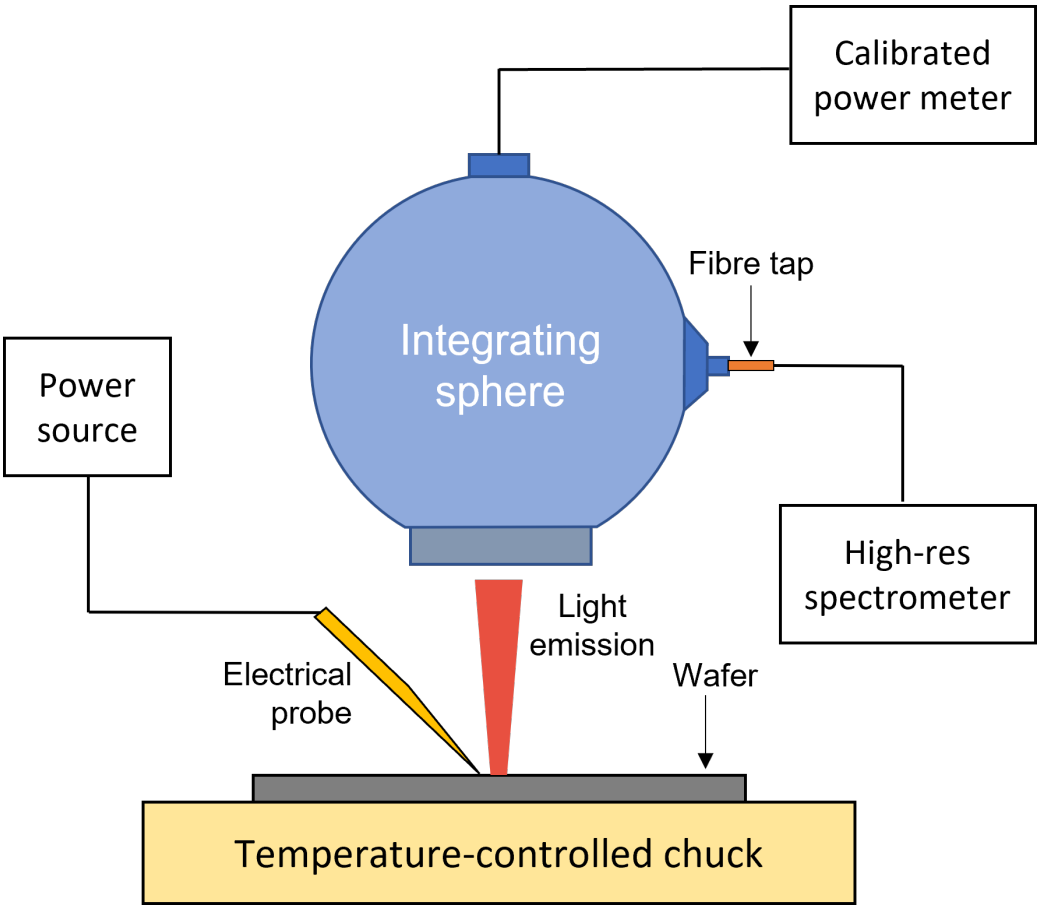

Figure 3.15: Schematic of the on-wafer VCSEL power and wavelength measurement setup. From [113].

fibre core used was 550 µm to provide sufficient signal to noise. The spectrometer had a fixed slit width of 10 µm which set the resolution to 0.3 nm. A schematic of the setup used for on-wafer P-I-V-λ measurements is given in Figure 3.15.

3.5 Summary

This chapter provided background on the MOVPE growth of VCSEL epi-structures including the reactor design and growth conditions affecting wafer uniformity. Attention was given to the strain-induced bow of VCSELs grown on large diameter GaAs substrates and the potential advantages of growth on Ge. The specific epitaxial structures grown for this study were described in section 3.2.5. Additionally, the processing techniques used for the production of VCSEL devices in this thesis was described and the standard processing techniques used for the realisation of VCSEL devices were outlined. A description of the sensitivity of the selective oxidation process to temperature (as well as layer thickness and composition) was given, which has important ramifications relating to uniformity, which is further explored in Chapter 5. The procedures used for the characterisation of wafer material quality and uniformity was presented. Further, the experimental setups for the characterisation of VCSEL devices, both on an optical bench and on-wafer, were described. The key details from this chapter are summarised here. Metal-organic vapour-phase epitaxy (MOVPE) is the commercial-standard growth technique used for the volume production of VCSEL epitaxial wafers. The epitaxial layers are adsorbed onto the semiconductor substrate due to pyrolysis occurring in the precursor gases typically between 550 and 750 °C. Control of the growth rate is non-trivial and depends on the composition of the precursor (V/III ratio), injection mechanism, gas flow rate, substrate temperature, and pressure, among other factors relating to the reactor design. Rotation of the substrate during epitaxy is crucial, and has resulted in dramatic improvements in wafer uniformity, however, lateral variation in the growth rate may still result in a radial on-wafer variation.

The growth of AlAs and high-Al composition AlGaAs DBR layers on GaAs substrates results in a compressive strain which translates into a significant wafer bow ($\sim$ 150 µm for a 150 (6-inch) mm wafer. This needs be accounted for in the both the growth conditions and in wafer processing, which adds complexity to the manufacturing process. Due to its mechanical robustness, zero-defect crystal quality, and favourable lattice constant, germanium has received attention as a potential route to 8-inch+ VCSEL production. The maximum height variation across a 6-inch Ge-substrate VCSEL wafer is measured to be around only 20 µm, related to the surface height variations of the Ge substrate. That is, the bow resulting from growth of high-Al layers on GaAs is becomes negligible with growth on Ge.

The epitaxial structures of the wafers produced for this work are grown with a generic p-i-n layout, designed for 940 nm emission wavelength. This consists of a bottom n-doped AlAs/AlGaAs DBR and upper AlGaAs/AlGaAs p-doped DBR. The active region is an InGaAs MQW structure embedded in a material-wavelength thick SCH, forming the optical cavity. A buried 98% Al composition layer is included in the top DBR for definition of the oxide aperture. This structure is grown on both GaAs and Ge substrates.

All wafer processing for this thesis was carried out at the Institute for Compound Semiconductors cleanroom at Cardiff University. For this study, optical lithography is used to transfer the mesa and contact geometry from the mask to the samples, with an alignment tolerance of $\sim$ 1 µm across a 6-inch wafer. ICP-RIE etching is used for the definition of the mesa. The etch must be deep enough to expose high-Al oxidation layer and the active region, with a tolerance of $\pm$ 0.2 µm. The uniformity of the etch depth for the 6-inch wafers processed for this study is within 2%. The selective oxidation of the buried high-Al composition layer has an exponential dependence on temperature. As such, temperature gradients across a 6-inch wafer can lead to a large variation in oxide apertures. The process is also highly dependent on the thickness and composition of the AlGaAs layer, which can also drive variation in the oxidation rate. The definition of the VCSEL mesa results in a non-planarity which typically requires extra processing steps to overcome. Often a dielectric (BCB) is deposited on the sample to the height of the mesa before the depo-

sition of the contacts. It has also been reported that BCB works to passivate the mesa sidewalls, reducing the rate of non-radiative surface recombination. To facilitate electrical pumping, Ohmic contacts must be made to the p+ and n+ layers of the VCSEL. In the simplest case, one contact is made on the top surface (emission-side) of the mesa and a global contact is deposited on the substrate side. An exception comes when structures are grown on semi-insulating substrates, in which case both contacts must be deposited on the emission side. The contact metals are typically Ti/Au or Cr/Au for p-contacts and AuGe/Ni/Au for n-contacts. Through measurement of C-TLM structures, it is found that low contact resistance ($< 1.2\times10^{-6}$ Ω) metallisation is achieved across an entire 6-inch wafer with high uniformity.

Characterisation of VCSEL epi-wafers is divided into two categories; post-growth material characterisation and device-level testing. Measurement of the reflectivity spectrum is performed to provide information on the FP cavity resonance and characteristics of the stopband. This is carried out at thousands on locations across a 6-inch wafer on a Nanometrics RPM PL wafer mapping system using a broadband optical source. Further, wafer-scale mapping of the photoluminescence spectrum is performed on the same system, using a 532 nm wavelength laser source. This is performed on calibration structures grown without a top-DBR and provides information on the active region quality. Reflectometry and PL measurements were carried out by IQE in-lin with the foundry process.

The characterisation of VCSEL devices was performed on both an optical bench and semi-automated wafer-mapping setup. In both cases, the optical power is measured via a calibrated integrating sphere. For the bench setup, spectral measurements are performed by coupling light into an optical fibre to an optical spectrum analyser. For the wafer-mapping setup the optical fibre is tapped off the integrating sphere and light is coupled to a CCD spectrometer. The temperature is controlled from room temperature up to 80 °C.

In summary, this chapter provided information on the practical realisation of VCSELs, from MOVPE growth to device fabrication. The epitaxial structures produced for this work were described and the standard wafer processing techniques which were used were

introduced. Details on the characterisation techniques and experimental setups for measurement of the VCSEL output characteristics were also given.

Chapter 4

Quick VCSELs (QuickSELs)

4.1 Introduction

The importance of rapid and continuous feedback of production information in the commercial manufacture of VCSELs was detailed in Chapter 1. Here, the development of a Quick VCSEL (QuickSEL) fabrication process which minimises processing time whilst preserving device performance is presented. The motivation being to facilitate efficient and reliable feedback from on-wafer VCSEL testing within both product development and volume production settings. As detailed in section 1.3, the VCSEL product development cycle is on the order of months and reduction of this cycle time can provide sizeable cost reductions. The QuickSEL has the potential to significantly reduce the time taken in the development of VCSEL epitaxial structures. Further, in already-established volume production, the QuickSEL also finds use in routine quality control methods for assessing material variation, tracking drift throughout a growth campaign, and quantifying impact on device performance. The QuickSEL has since become a process that has been industrially adopted, in use by commercial entities in the early stages of VCSEL product development.

In section 4.2, a description of the architecture and processing steps is first given for

dielectric-planarised standard VCSELs. These devices are used as a performance benchmark against which QuickSEL device performance is qualified. In sections 4.3 and 4.4, work is reproduced from [114] and [104] which focusses on the design, processing, and characterisation of two different approaches to Quick VCSEL fabrication. In both cases, the performance of QuickSEL devices are compared to that of standard device architectures. In section 4.5, the different approaches are compared in terms of processing complexity and device performance, and the optimised QuickSEL device design is presented.

4.2 Standard VCSEL

Firstly, a description of the processing steps for standard BCB-planarised VCSELs is given. Standard VCSELs are used as a benchmark of device performance for the qualification of the QuickSEL design. Any deviations in performance from standard device performance are then accounted for when using the QuickSEL process to assess epitaxial quality. Fabrication followed standard processing techniques which were introduced in section 3.3. For the standard VCSEL structures the process was as follows: definition of the mesa by inductively coupled plasma (ICP) etch through the oxidation layer and active layers, a depth of ~ 3 µm. Wet thermal oxidation of the samples at 400 °C to form the oxide apertures with an oxidation depth of 5.5 ± 0.5 µm. The samples were spin-coated with benzocyclcobutane (BCB) and subsequently etched-back to planarise the material to the height of the mesas. Ti/Au (10/300 nm) p-metal ring contacts and were deposited on the mesa surface before the etch to improve alignment tolerance. The deposition of a Ti/Au (10/500 nm) feed metal is then performed after the planarisation step, followed by a standard AuGe/Ni/Au deposition for the global substrate-side n-metal contact. Figure 4.1 is a SEM image of a processed standard VCSEL; labelled is the surface of the mesa, p-contact ring, feed metal, and the planarising BCB.

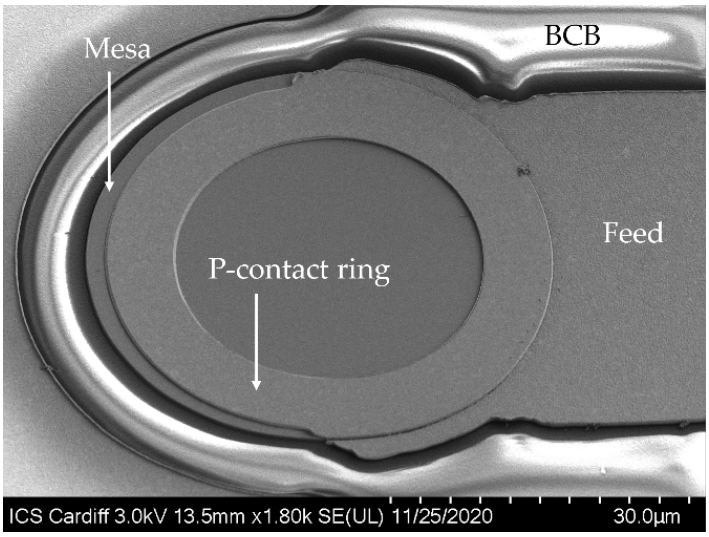

Figure 4.1: SEM image of BCB-planarised standard VCSEL device. The mesa is fully isolated by an open-area etch. BCB is used to facilitate a planar deposition of the ring-contact and feed metal.

4.3 Bridge-Mesa Approach

The initial QuickSEL approach was based on an etched-trench bridge-mesa design, whereby the central cylindrical VCSEL cavity is only partially isolated from the surrounding planar material. The remaining material is referred to as the bridge and this facilitates deposition of a bond pad in the same plane as the p-metal ring contact without the need for a planarisation process step. However, deposition of a dielectric is needed to electrically isolate the contact pad. A SEM image of a bridge-mesa VCSEL is shown in Figure 4.2. Labelled is the partially isolated mesa, p-contact ring and feed metal, and the insulating SiN layer. The region referred to as the bridge is also indicated.

This device design resulted in a significant reduction in processing time but this was also at the expense of device performance. Other variations on this design which further reduced the processing time (with/without substrate thinning and with/without oxidation) were also produced to assess the impact on device performance. These device suffered from leakage along the bridge which resulted in high threshold currents. A near-field image of light emission along the bridge due to the leakage path is reproduced here and shown in Figure 4.3. The resulting impact on threshold current for the different processing variations is reproduced in Figure 4.4. As seen in the same figure, the issue was exacerbated

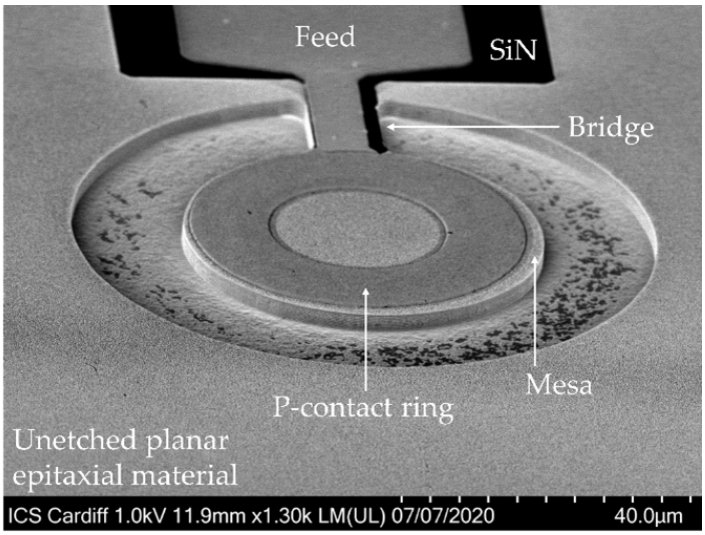

Figure 4.2: SEM image of bridge-mesa VCSEL. The mesa is partially isolated from the surrounding planar material by a trench etch. The bridge facilitates a planar p-contact, with a SiN layer deposited to isolate the feed metal.

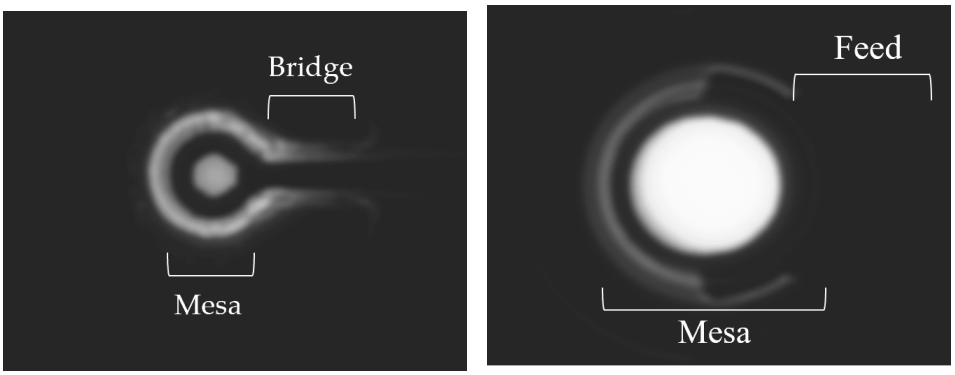

Figure 4.3: Near-field images of (left) oxidised QuickSEL bridge mesa device, showing light emission along the bridge due to leakage current, and (right) a standard-BCB planarised VCSEL. The light emission along the bridge of the QuickSEL is the result of the partial mesa isolation.

for devices which were not oxidised. The emission wavelength was mostly unaffected and found to be determined principally by the material cavity resonance, with some redshift related to self-heating. The thinning of the substrate was observed to produce improved thermal performance, measured as a reduced wavelength redshift and improved mode stability. This work was reported in [114].

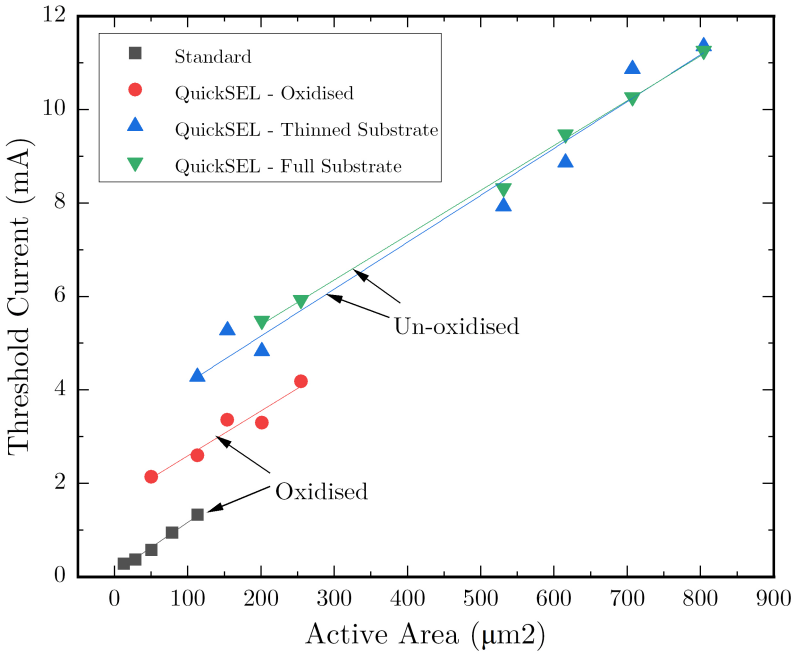

Figure 4.4: Best (lowest) measured threshold currents as a function of active area for QuickSEL and standard device types. For bridge-mesa VCSELs, the active area is calculated from the nominal aperture diameter. Oxidised and un-oxidised devices are labelled.

4.4 Oxide-Via VCSEL

In efforts to further reduce the fabrication time and improve QuickSEL device performance, another approach was developed and tested. With the oxide-via VCSEL design, the complete removal of the current leakage path was achieved, whilst the need for deposition of any dielectric was also circumvented (unlike for the bridge-mesa or standard VCSEL design).

4.4.1 Oxide-Via Processing

For these devices, the entire fabrication can be broken down concisely into 7 steps: two lithography; two metallisation; single etch; oxidation and one annealing step. Initially, optical lithography is used to define the geometry of the structures which includes, in a departure from the full process, both the mesa and the contact pad regions. The structure is then etched to expose the high Al-content oxidation layers. Upon wet thermal

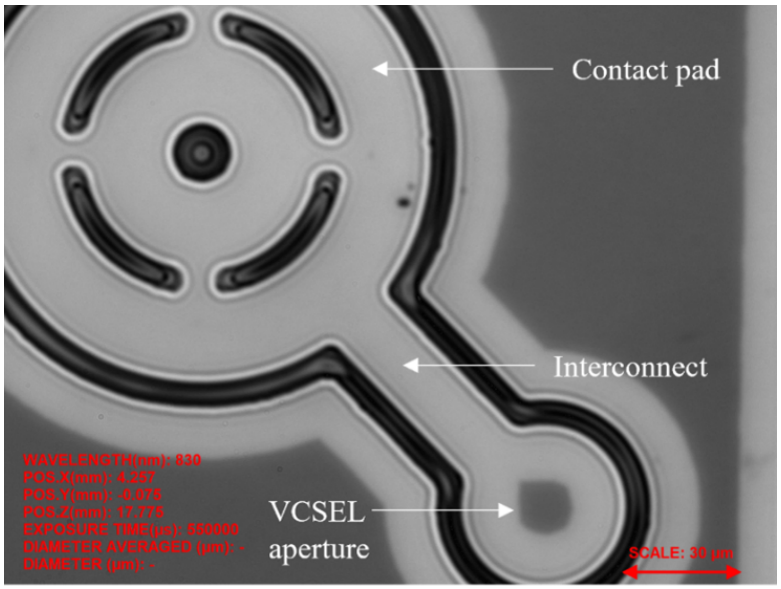

Figure 4.5: Infrared camera image of an oxide-via QuickSEL structure taken in-situ during selective-oxidation. A quasi-circular aperture is formed due to the geometry of the mesa and interconnect.

oxidation, in addition to the aperture formation in the VCSEL mesa, via-holes are utilised to provide complete electrical isolation under the contact pads, ensuring that current flows only through the aperture region. An oxidation length of 13.5 ± 0.5 µm is sufficient to fully isolate the contact pad and generate the desired VCSEL apertures. This length is intrinsically linked to the dimensions of the device design and therefore can be further reduced but this is at the expense of alignment tolerance. The second lithography step is used to define the p-contact which is then deposited using Ti/Pt/Au PVD. The final two steps are a blanket backside AuGe/Ni/Au metallisation for a global n-contact and annealing of the metal contacts. The significant departures of the QuickSEL process from the previously described standard VCSEL are the elimination of the requirement for BCB planarisation and the utilisation of only a single top-side metallisation step. Thus, the total fabrication time reduces by $\sim 60\%$. A top-view image of a QuickSEL after thermal oxidation is shown in Figure 4.5. The quasi-circularity of the VCSEL aperture (resulting from the mesa-interconnect geometry) can also be seen in Figure 4.5.

4.4.2 Comparison with Standard Structure

Next, the performance of the oxide-via VCSELs is compared to that of standard structures. The devices were produced on 12.5 × 12.5 mm tiles of equivalent epitaxial material taken from the centre of the same 6-inch wafer. To achieve the same oxide aperture diameter, a deeper oxidation extent is required for the QuickSELs due to the geometry of the mesa. As such, these samples were oxidised in different runs and definition of precisely equivalent aperture devices was not achieved. When comparing typical performance for each device type, the behaviour of larger aperture diameter devices (7 – 9 µm) is assessed to minimise the effects of scattering and diffraction associated with small apertures, as well as the higher uncertainty of the aperture diameter resulting from the increasing oxidation rate [115].

4.4.2.1 Series Resistance

A comparison of the dependence of series resistance on oxide aperture diameter, extracted from the slope of the I-V curve at 2.5 V, is shown in 4.6, for both QuickSEL and standard devices. The mean series resistance of the standard VCSELs is found to be approximately 25 Ω higher than that of the QuickSELs in the range 7 – 9 µm and is likely associated with the p-contact metallisation. For the standard VCSELs, there is a contact resistance related to the deposition of the feed metal onto the p-contact ring which is not present for the QuickSEL devices given that the contact pad and feed metal are deposited simultaneously and directly onto the semiconductor surface. Further, the metal thickness and width of the p-contact ring is also reduced for the standard structures. Although there is a slight difference in active area for nominally equal oxide apertures (due to the quasi-circularity of the QuickSELs) the effect on series resistance should be small given that the active area is only ∼ 7% larger. This higher series resistance in the standard VCSELs thus contributes to increased Joule heating in those devices and hence a higher internal temperature.

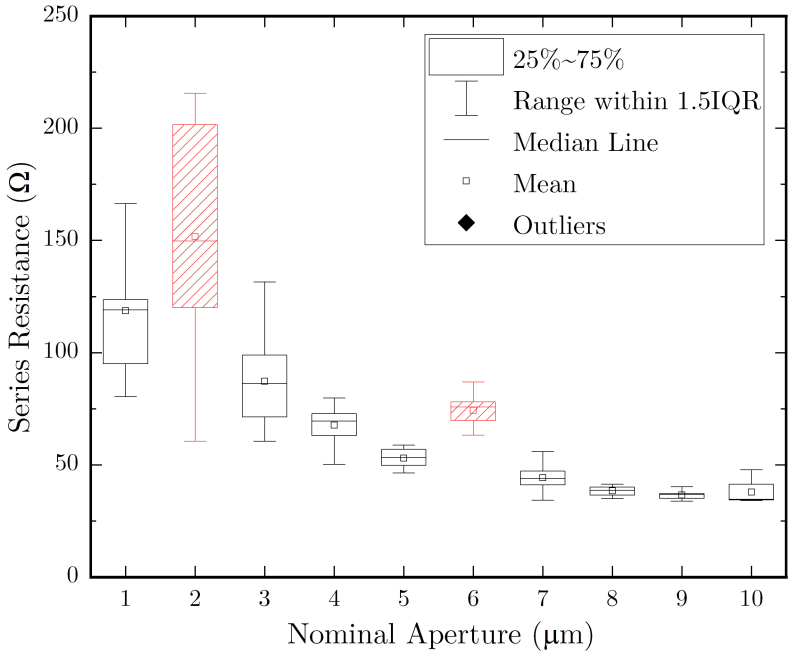

Figure 4.6: Box plots of series resistance as a function of oxide aperture for QuickSEL devices (plain black boxes) and standard VCSEL devices (red striped boxes). Resistance is extracted from the I-V characteristic as the slope at $2.4 - 2.5$V.

4.4.2.2 Power-Current Characteristic and Threshold Requirement

In Figure 4.7, the dependence of threshold current on aperture diameter for both device types is shown. It can be seen that the QuickSEL design approaches the performance of a standard VCSEL, producing values of I_{th}, which closely match that of standard structures. However, there is a small increase of approximately 0.3 mA in the mean threshold current for the $7 - 9$ μm QuickSEL devices relative to the standard devices. This difference is shown to be partly the result of temperature effects associated with a difference in thermal mass of the QuickSEL and standard structures, amongst other contributing factors which are also discussed below. The temperature dependence of I_{th} for standard and QuickSEL devices is shown in Figure 4.8 (top). Based on the analysis of [63] (as discussed in section 2.3.2), the threshold current minimum, α, and the temperature at which the threshold current minimum occurs, T_{min}, are extracted. This minimum is observed to occur at approximately 45 °C within a range of ±5 °C for all the devices measured, whether standard or QuickSEL designs. Therefore, the gain peak-to-cavity resonance detuning is taken to be equivalent for both device types. The standard VCSELs have increased

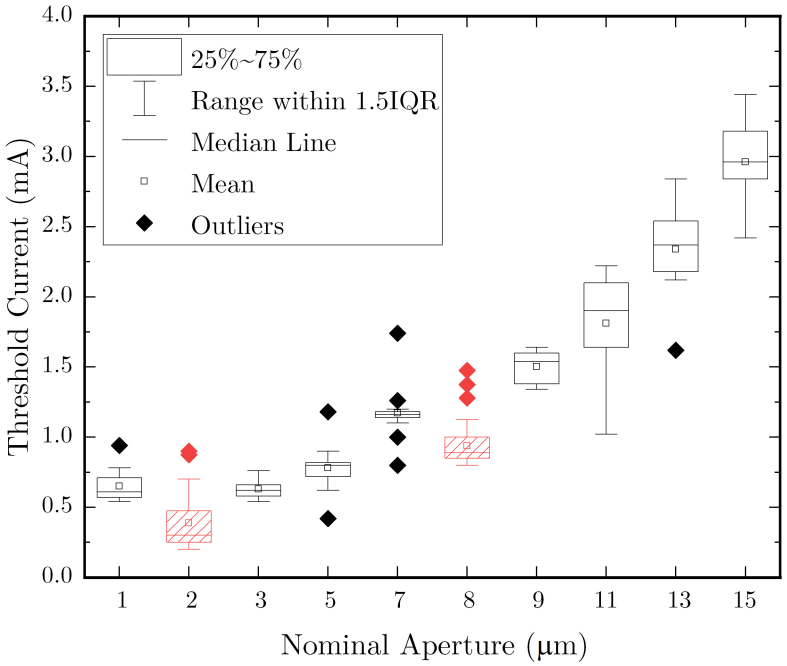

Figure 4.7: Box plots of measured threshold currents for a range of oxide aperture diameters for both QuickSEL (plain black boxes) and standard (red striped boxes) VCSEL devices.

thermal resistances due to the shorter oxidation lengths used (smaller thermal mass). Hence, for equivalent active areas, the thermal impedance of a standard VCSEL is higher than that of a QuickSEL. Additionally, the series resistance is higher which leads to a greater degree of Joule-heating. Thus, for any given bias current, a standard VCSEL operates at higher internal temperature than a QuickSEL device. Therefore, from Figure 4.8 (top), at room temperature the standard VCSELs operate closer to T_{min} due to the higher rate of internal heating. This results in a decrease in threshold current relative to the QuickSELs. Additionally, it is also likely that there is an increased rate of surface recombination at the exposed mesa sidewalls of the QuickSEL devices relative to the BCB-passivated standard devices, which contributes to a higher threshold current [102], [116], [117]. Also, as already mentioned, the QucikSEL design results in quasi-circular aperture shapes, owing to the interconnect region of the device, which increases the active area by $\sim 7\%$ relative to the circular aperture of a standard device. Given that the threshold current of a VCSEL scales with active volume, this also contributes to increase in threshold current for QuickSELs relative to a standard device. Although devices are processed from

similar regions of the wafer, some spatial variation in the DBR layers may also contribute to a difference in threshold gain [103], [118]. The typical output optical power-current (P-I) characteristics of the standard and QuickSEL device types, measured up to thermal rollover are shown in Figure 4.8 (bottom). In general, the maximum output power is higher for the standard VCSELs, with some 8 µm aperture devices reaching up to 27.5 mW. However, the onset of thermal rollover occurs at significantly lower currents than for the QuickSEL devices (up to 10 mA for a given aperture diameter). Again, this is a result of the difference in electrical and thermal impedance. The power conversion efficiency, η_p, is extracted at a fixed current of 6 mA and is found to be highest for the standard devices, although there is good agreement for the maximum power conversion efficiency at $\sim 30\%$ but occurring at lower currents for standard devices. The mean η_p for a 7 and 8 µm QuickSEL and standard VCSEL is measured as 30.2 ± 4.2 and 32.5 ± 5.9 %, respectively, with the error given by the standard deviation across all devices measured. The mean current corresponding to $\eta_{p,max}$ is then measured as 3.5 ± 0.7 and 5.0 ± 0.4 mA for a 7 and 8 µm aperture standard and QuickSEL device. The slope efficiency, η_d, measured between 5 and 10 mA is consistently higher for the standard VCSELs, with a value of 0.89 W/A for an 8 µm aperture standard device, compared to 0.65 and 0.77 W/A for a 7 and 9 µm aperture QuickSEL, respectively. The reduction in η_d of the QuickSEL device could be related to the lack of sidewall passivation leading to a higher rate of non-radiative recombination at locations away from the lasing mode if the carrier density is not pinned. However, given that the stimulated recombination process is much faster than the surface recombination processes, it is likely that the decrease in η_d is driven by a difference in optical loss related to the epi-layers.

4.4.2.3 Emission Spectra

The emission spectra for devices produced by QuickSEL processing are comparable to that of standard device structures. Single mode emission for oxide aperture diameters $<$ 3 µm up to 2 mA injection current is achieved in QuickSEL devices, the spectra for which

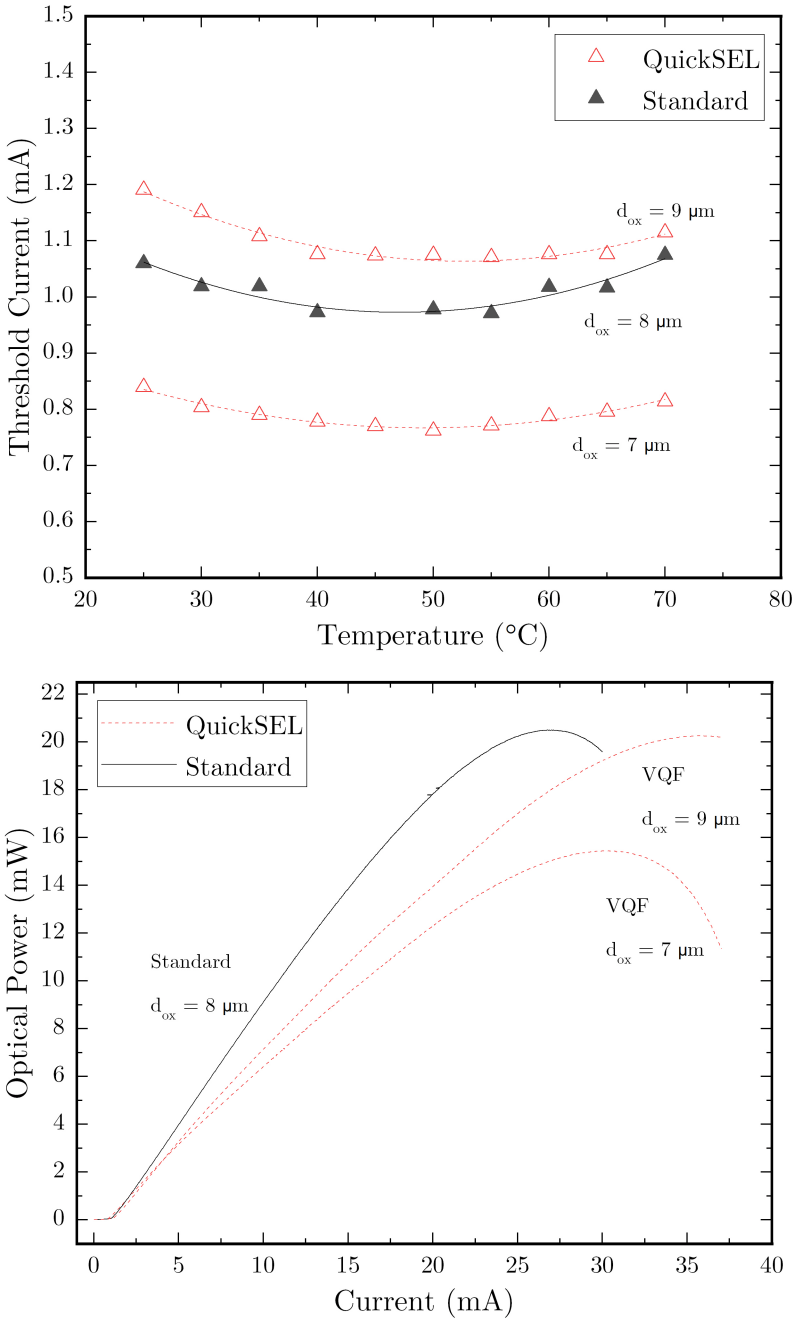

Figure 4.8: Temperature dependence of the threshold current fitted with a second order polynomial (top) and L-I characteristic at room temperature up to thermal rollover (bottom) for QuickSEL and Standard VCSEL devices. The gain-peak detuning is found to be equivalent for both device types, with the threshold current minima occurring at $\sim$ 45 °C. The onset of thermal rollover occurs at a lower current for the standard structure due to the reduced thermal mass.

are shown in Figure 4.9. The number of lasing modes in larger aperture devices is also comparable, shown in the multi-mode spectra in Figure 4.10. However, the wavelength of the fundamental mode is longer in the standard VCSELs. This is seen more clearly for the 8 µm aperture devices in Figure 4.11, where the extracted wavelengths for all devices are plotted. The cavity resonance wavelength extracted from post-growth reflectometry measurements is shown by the dashed line corresponding to a value of 941.4 nm for both device types. Comparing the mean values to the resonance wavelength, the standard devices are found to be more redshifted, again indicative of greater self-heating.

Assessing the effects of self-heating on the wavelength further, the shift with current above threshold for an 8 µm aperture standard and 9 µm aperture QuickSEL device is measured as 0.5 and 0.1 nm/mA, respectively. A temperature shift per unit current, ΔT, is then calculated as 7.2 and 1.1 °C/mA for the standard and QuickSEL devices, respectively. Here, it has been demonstrated that the performance of oxide-via QuickSEL devices is representative of standard devices and that the observed disparities can be explained by consideration of device thermal properties, the limitations imposed by the un-passivated mesa sidewalls, and the quasi-circular aperture shape. The difference in room temperature threshold current is understood by considering the temperature dependent detuning of the gain peak and cavity resonance wavelength. Further, the difference in threshold lasing wavelength is understood by comparing the difference in operating temperatures at a given current which is driven by the difference in thermal resistance. An enhanced rate of surface recombination likely limits the best achievable threshold current, but this effect is small and does not significantly hinder the utility of the information provided by characterisation of QuickSELs. The key quantities discussed and used to compare QuickSEL and standard device performance are summarised in Table 4.1.

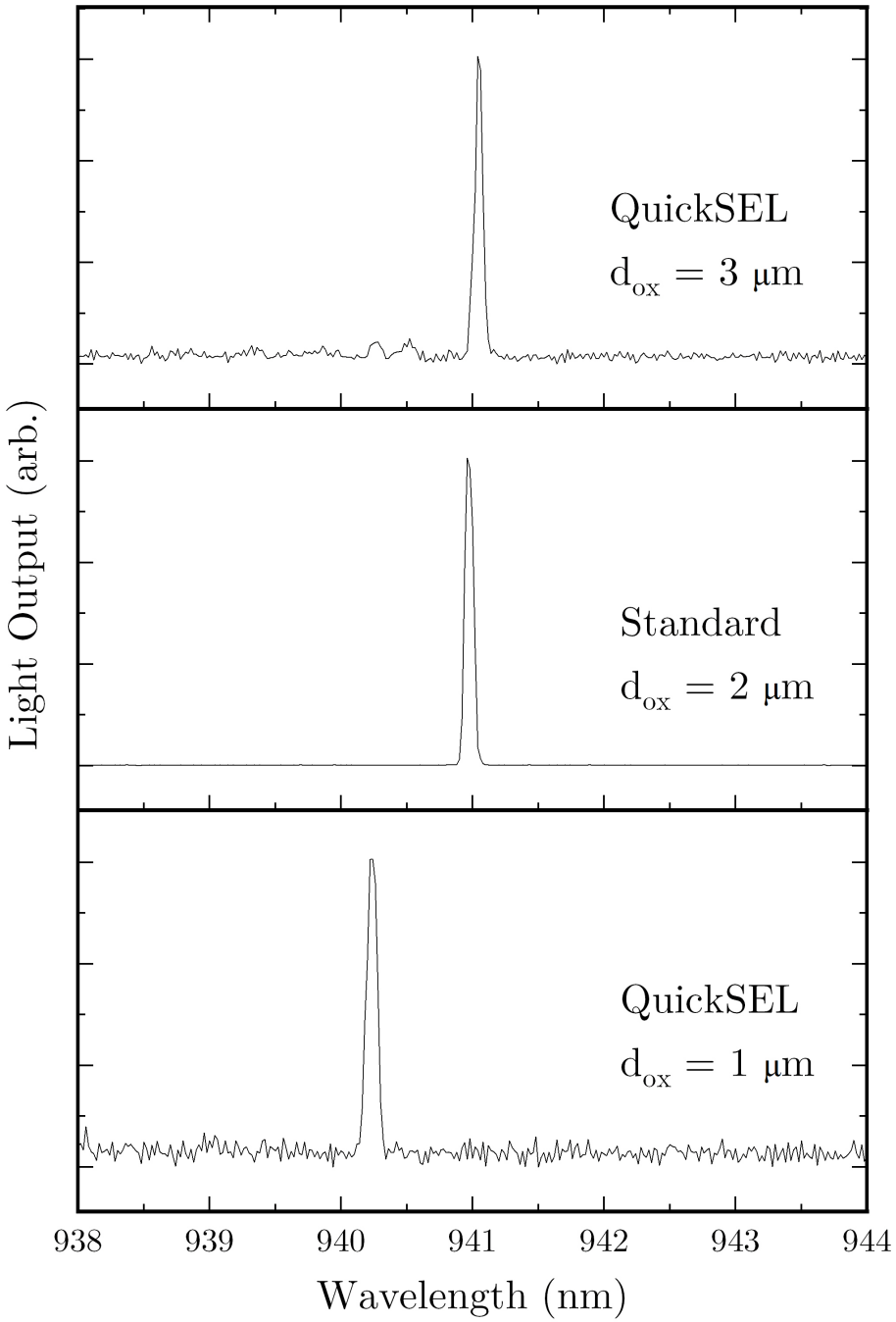

Figure 4.9: Single-mode emission spectra at 2 mA for 1-3 um aperture QuickSEL and standard devices (labelled). The blueshift observed for the 1 μm aperture device is associated with confinement effects of the oxide layers.

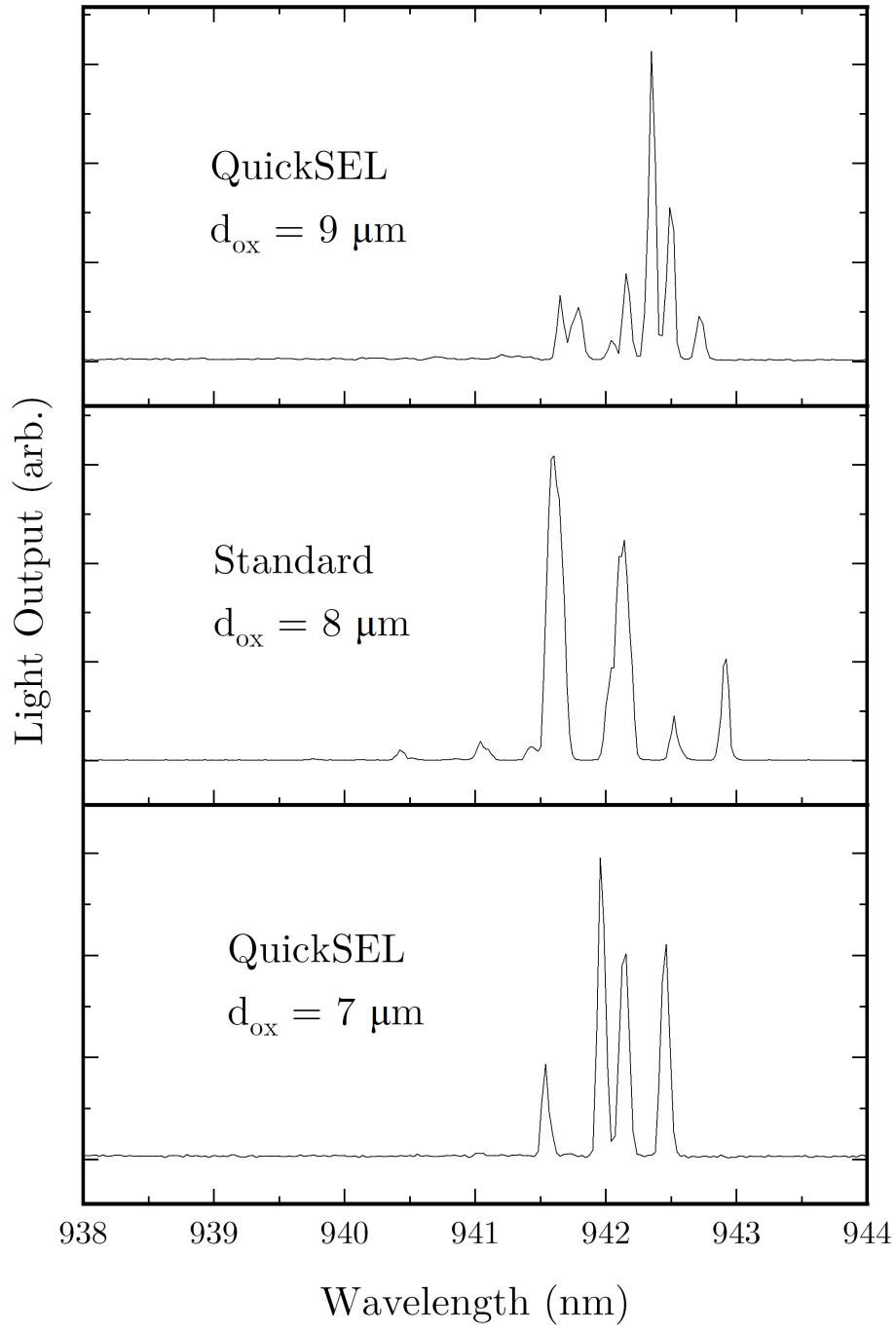

Figure 4.10: Multi-mode (right) emission spectra for 7-9 um aperture QuickSEL and standard devices. The redshift in the fundamental mode wavelength of the 8 um aperture standard device is associated with a higher power dissipated resulting from the reduced thermal mass.

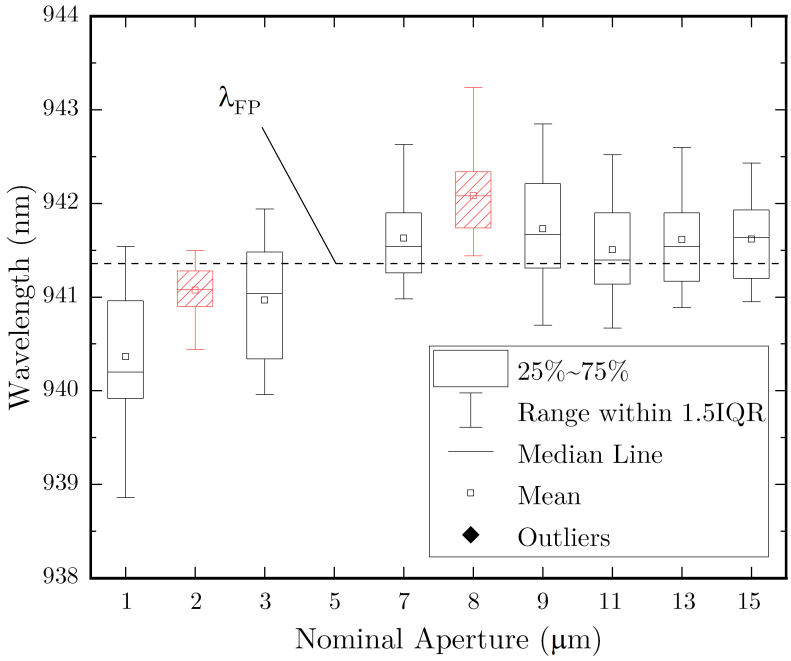

Figure 4.11: Box plots for the measured fundamental mode wavelengths of QuickSELs (plain boxes) and standard VCSELs (striped boxes). The FP cavity resonance wavelength is indicated by the horizontal dashed line. A redshift in the mean emission wavelength of the 8 um standard VCSELs is related to the reduced thermal mass.

Table 4.1: Comparison of key figures of merit for standard and oxide-via QuickSEL devices. The quantities provided are the mesa diameter (d_m), the oxide aperture diameter (d_{ox}), series resistance (R), threshold current (I_{th}), threshold current density (J_{th}, internal temperature increase (ΔT), threshold current minima (α), power conversion efficiency (η_p), and external differential efficiency (η_d).

Device	d_m (µm)	d_{ox} (µm)	R (Ω)	I_{th} (mA)	J_{th} (kA/cm^2)	ΔT (°C/mA)	α (mA)	η_p (%)	η_d (W/A)
QuickSEL	34	7	56	1.0	2.2	1.1	0.7	28.2	0.65
Standard	26	8	77.2	0.8	1.8	7.2	1.0	36.4	0.89
QuickSEL	36	9	45.0	1.2	2.0	1.1	1.4	32.7	0.77

4.5 Optimised QuickSEL Design

4.5.1 Comparison of Approaches

In sections 4.3 and 4.4, the performance of bridge-mesa and oxide-via VCSELs relative to standard devices structures was assessed. For bridge-mesa devices, the leakage current resulting from the partial mesa isolation limited performance. With the oxide-via design, the VCSEL mesa is fully isolated whilst also not requiring planarisation, which greatly improves performance with respect to the bridge-mesa design, with some limitations arising from the aperture quasi-circularity and surface recombination at the un-passivated mesa sidewalls. From the experimental comparison it is clear that the oxide-via device produces the most representative device performance. However, another important consideration is the fabrication complexity and processing time. Figure 4.12 compares the process flow for each processing method, with standard processing on the left, bridge-mesa in the middle, and oxide-via to the right. Not only is the performance of oxide-via devices closer to standard structures, but the fabrication complexity is also reduced relative to bridge-mesa devices. The reduction in fabrication complexity is accompanied by a reduction in processing time, which is shown in Table 4.2.

The oxide-via device achieves the greatest reduction in fabrication complexity and processing time, whilst resulting in only slight differences in performance relative to standard VCSELs. Therefore, it is found that this is the optimum approach for producing QuickSELs. Hereafter, any reference to a QuickSEL device will be a reference to an oxide-via device.

4.5.2 Design Variants and Optimisation

Some variations and modifications to the QuickSEL design are employed to accommodate different epitaxial structures and to maximise the tolerance of the alignment and oxidation extent over large diameter wafers. For 940 nm high-power applications, the epitaxial

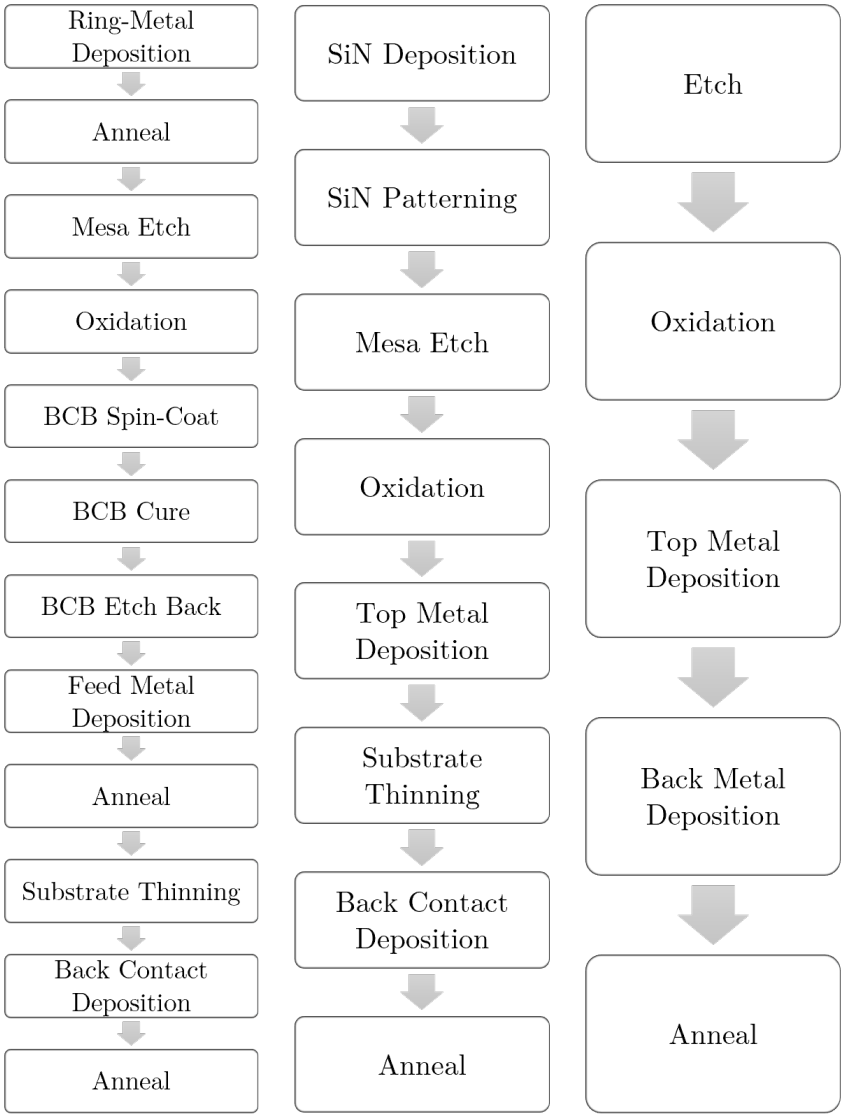

Figure 4.12: Comparison of process flow for standard VCSELs (left), bridge-mesa VCSELs (middle) and oxide-via VCSELs (right).

Table 4.2: Comparison of QuickSEL approaches relative to a standard VCSEL process. Dielectric refers to the requirement for any dielectric deposition in the process. Confinement refers to the electrical and optical confinement afforded by the oxide aperture in standard VCSELs.

Device	Dielectric	Confinement	Fab Time (Hours)	Performance
Standard	Yes	Full	60	Optimum Performance
Bridge Mesa	No	Partial	38	Significant deterioration
oxide-via	No	Full	< 24	Minor deterioration

structures are grown on doped substrates which allows a global substrate-side n-contact. However, for 850 nm high-speed applications, the structures are grown on semi-insulating substrates and a global n-contact is not possible. In this case, the n-contact must be deposited on a highly n-doped layer which is only exposed after etching. This design variation is referred to as a co-planar QuickSEL to keep with the nomenclature used for standard VCSELs and refers to both the p-contact and n-contact being on the emission side of the wafer. A microscope image of a co-planar QuickSEL is presented in Figure 4.13. The QuickSEL design was modified such that, after an extra etch step, a AuGe/Ni/Au deposition forms a contact to the n-DBR on the emission-side of the device. The P-I-V performance of the co-planar QuickSEL structure is shown to be equivalent to QuickSEL devices with a substrate-side n-contact in Figure 4.14. The sample has both substrate- and emission-side contacts, meaning that the comparison is made for the same device. The P-I and I-V characteristics are within error for both contact arrangements. Key figures of merit extracted from the P-I-V data are presented in Table 4.3. These quantities are all within error, thus demonstrating that the co-planar design provides representative information, and therefore is a viable solution for semi-insulating substrate wafers.

Additionally, as is evident in Figure 4.13, small modifications to the original QuickSEL design are made, with the aim of relaxing the fabrication tolerance over large areas. Each etch pattern is designed such that the oxide-via widths are equal. This removes differences related to aspect-ratio-dependent etching and improves the overall etch depth uniformity across a full wafer. Also seen in Figure 4.13 are notches added to the contact pad geometry. These are added to relax the oxidation extent tolerance and prevent under-oxidation.

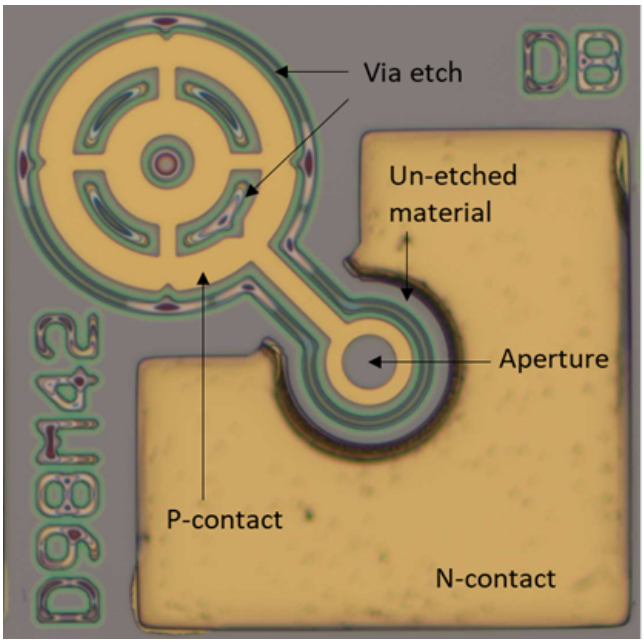

Figure 4.13: Microscope image of a co-planar QuickSEL. The via etch, p-contact and aperture (labelled) are all equivalent as for the oxide-via devices discussed in this chapter. An extra etch step is made after which the n-contact is deposited on the emission-side of the wafer. The isolation un-etched material is also labelled.

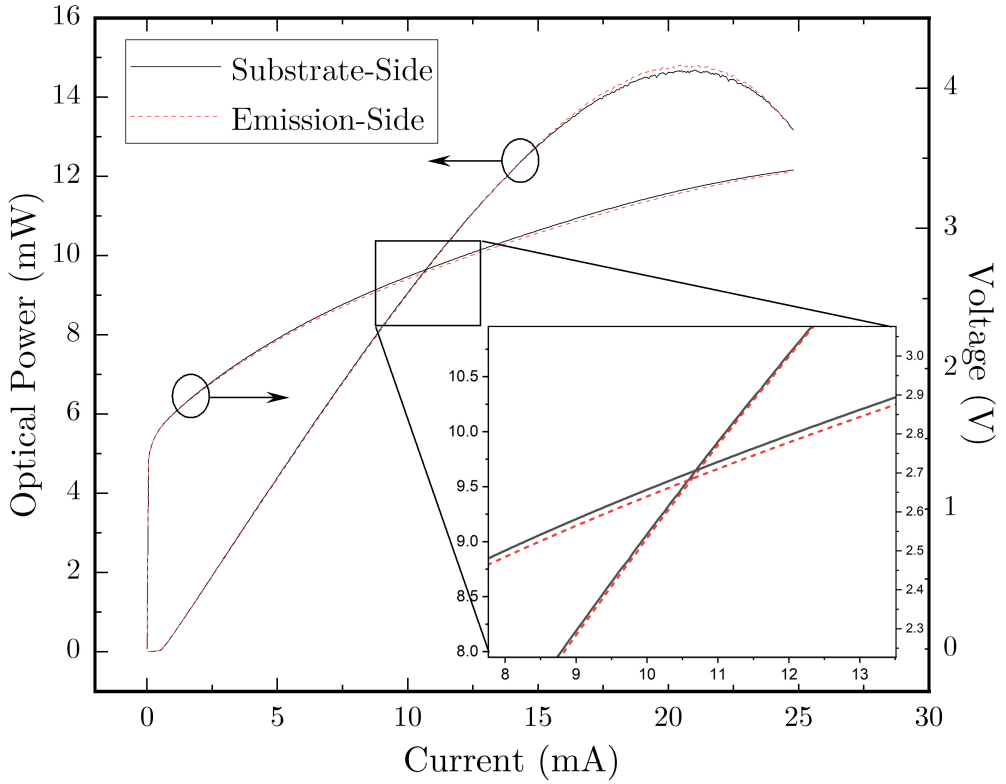

Figure 4.14: Comparison of substrate-side and emission-side QuickSEL contact arrangements. Devices were patterned with both types of n-contacts, enabling the comparison of performance for the same device.

Table 4.3: Comparison of key figures of merit for a 38 µm co-planar and standard substrate-side n-contact QuickSEL device. The quantities included are the threshold current (I_{th}), series resistance (R), peak optical power (P_{max}), thermal rollover current (I_{max}), peak differential efficiency ($\eta_{d,peak}$), and peak power conversion efficiency ($\eta_{p,peak}$).

Contact	I_{th} (mA)	R (Ω)	P_{max} (mW)	I_{max} (mA)	$\eta_{d,peak}$ (W/A)	$\eta_{p,peak}$ (%)
Substrate-Side	0.54	74.0	14.68	21.0	1.01	40.97
Emission-Side	0.54	72.8	14.81	21.05	1.00	40.82

4.6 Summary

In this chapter, approaches for producing Quick VCSELs (QuickSELs) were presented. These devices were designed to minimise the processing time such that VCSELs can be rapidly produced for use as feedback within product development cycles, epi-structure DOEs, and in quality control in volume settings. The performance of devices fabricated by each approach was compared to that of standard BCB-planarised VCSELs.

The initial QuickSEL approach was a bridge-mesa, whereby the VCSEL is partially isolated from the surrounding planar material. This design did not require the time-consuming step of BCB-planarisation by allowing deposition of the contact pad and interconnect along the bridge. However, deposition of a dielectric was needed to electrically isolate the contact pad. These devices suffered from a leakage current along the bridge which resulted in high threshold currents, which was exacerbated for devices which were not oxidised.

In efforts to further reduce the fabrication time and improve QuickSEL device performance, another approach was developed and tested. The oxide-via VCSEL design, whereby etched vias expose the buried high-Al content oxidation layer, made it possible to circumvent the need for deposition of any dielectric (unlike for the bridge-mesa or standard VCSEL design). Atypical mesa geometries were patterned such that the contact pad and interconnect regions are electrically isolated by the selective oxidation process due to the exposed high-Al layers in the vias. This resulted in planar, electrically-isolated, and

optically-confined VCSEL devices without the need for any dielectric. These QuickSEL devices closely approach the performance of standard BCB-planarised VCSELs. The series resistance was found to be slightly lower for the QuickSELs, which was related to the definition of the top contact. Higher threshold currents were observed for the QuickSEL devices which was attributed to surface-recombination at the un-passivated mesa sidewalls, the quasi-circular aperture, and larger thermal mass (coupled with the effect of gain-peak detuning). The emission wavelength was shown to be principally determined by the cavity resonance. Comparable differential and power conversion efficiencies were observed. The calculated internal temperature increase per unit current was shown to be lower for a QuickSEL due to the larger thermal mass.

Comparing the approaches, the oxide-via VCSEL structure was shown to be superior in terms fabrication simplicity, processing time, and device performance. QuickSELs can be produced in under 24 hours and provide representative information on epitaxial material quality and of standard device performance. Hence, this approach was chosen to be carried forward for the subsequent work described in this thesis.

Furthermore, modifications and optimisations to the QuickSEL structure were presented. To accommodate growth on semi-insulating substrates, a co-planar QuickSEL design was developed. This involved a second etch step and the deposition of the n-contact on the emission-side of the wafer. Devices were produced with both a substrate-side and emission-side n-contact and P-I-V measurements showed no deviation in the device performance. Additionally, to improve tolerance when processing whole wafers, features of the mesa pattern were modified. Notches were included on the contact pad to prevent under-oxidation, and the thickness of the contact was reduced to provide an improved alignment tolerance. The QuickSEL has since become a process that has been industrially adopted and is used by commercial entities for optimisation of epitaxial designs in early stages of VCSEL product development.

In conclusion, a design and fabrication process was developed such that VCSEL devices with performance close to that of standard BCB-planarised structures can be produced within 24 hours. In the following chapters, the utility QuickSELs in product development

cycles for both the assessment of material quality and uniformity and for the prediction of standard device performance is demonstrated.

Chapter 5

Assessment of Wafer Quality and Uniformity

5.1 Introduction

As described in Chapter 1, VCSEL performance is highly sensitive to both the properties of the constituent epitaxial material and the specific application-dependent wafer processing. In volume production, target yields are of critical concern and are usually expected to exceed 90%, hence it is important to understand the sources of on-wafer and wafer-to-wafer variation. Conversely, this is not necessarily the case in small-scale settings where it is understood that yields will be low. As described in section 3.2, the simultaneous control of many conditions are needed to achieve a uniform deposition throughout the reactor chamber. Comprehensive characterisation techniques are thus required to assess material uniformity relative to target specifications and critical tolerances. This is crucial for both the development of reproducible growth recipes and as ongoing quality control in volume manufacture, especially as the wafer diameter is increased.

In this chapter, the material and device characterisation methods previously described are applied to full 6-inch VCSEL wafers for the assessment of material quality and unifor-

mity. In section 5.2, the characterisation of wafer quality via standard industry methods is shown. Data from reflectometry measurements are presented, from which the material cavity resonance wavelength, as well as other important parameters relating to the reflectivity of the DBR mirrors, are extracted. Further, measurements of photoluminescence spectra on calibration material are shown, from which information on the active region is derived. Then, in section 5.3, the impact of oxidation length non-uniformity on QuickSEL device performance is assessed. This oxide variation is shown to be temperature-driven, associated with both furnace temperature gradients and the bow of large diameter GaAs substrate wafers. Finally, in section 5.4, the wafer-scale variation of QuickSEL device performance on 6-inch diameter GaAs substrate wafers is characterised. The threshold current, threshold current density, lasing wavelength, series resistance, optical power, and device efficiencies are all spatially mapped. Performance at elevated temperature is measured to assess the variation of the gain-peak and cavity resonance wavelengths. The variation in QuickSEL performance is assessed against the non-uniformities arising from both growth and processing.

5.2 Post-Growth Material Characterisation

5.2.1 Reflectometry

Measurement of the VCSEL reflectivity spectrum provides many useful insights into material quality and has the benefit of being able to be performed rapidly on as-grown epi-material. The Fabry–Pérot (FP) cavity resonance wavelength – the dip in the stopband caused by the resonance of the cavity – can be directly extracted from the reflectivity spectrum, and this provides the expected lasing wavelength of processed devices. The height of the stopband provides an indication of the relative reflectivity. However, for the measurements performed here, the magnitude is un-calibrated and so cannot be used to

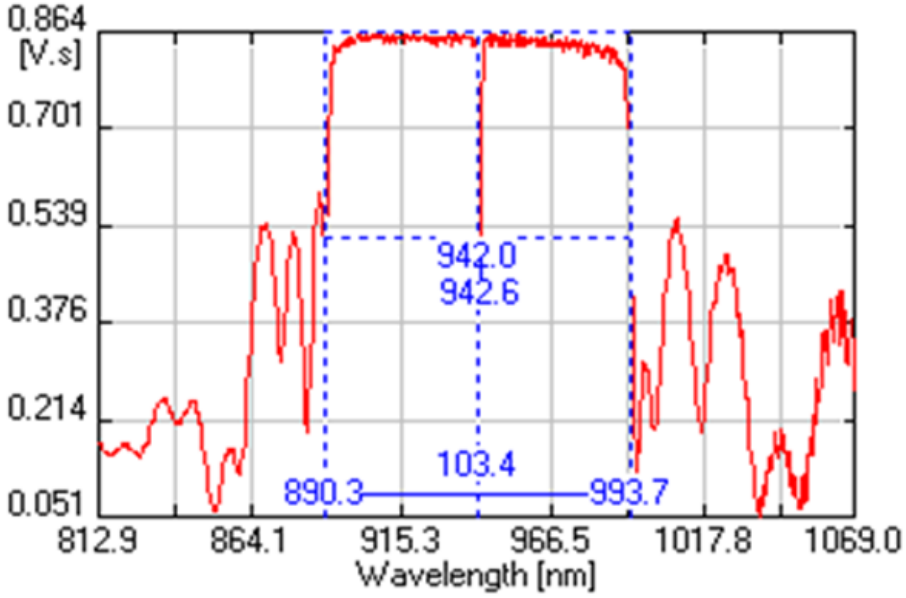

Figure 5.1: VCSEL reflectivity spectrum measured at the centre of a 6-inch wafer. A 103.4 nm wide stopband is formed which is centred at 942.0 nm. The dip in the spectrum corresponding to the FP cavity resonance occurs at 942.6 nm.

compare absolute power reflectivity. The centre-wavelength and width of the stopband can also provide information on deviations in layer thickness and composition from the target structure. An example VCSEL reflectivity spectrum is shown in Figure 5.1, with some of the values of the quantities mentioned labelled in the plot. The reflectivity spectrum of Figure 5.1 is taken from the centre of a 6-inch wafer designed for 940 nm emission wavelength. As seen in the plot, there is good alignment of the FP dip and stopband centre (942.0 and 942.6 nm). The stopband width is found to be $\sim$ 100 nm which is typical for a 940 nm emitting AlGaAs-based VCSEL, as discussed in section 2.2.1. The mirror reflectivity, representative of the refractive index contrast of the DBR layers (Equation 2.8), is extracted as the height of the stopband. In the following sections, contour plots resulting from the wafer-scale mapping of each of these characteristics are presented.

5.2.1.1 Fabry–Pérot Cavity Resonance

For a VCSEL, the material cavity resonance wavelength is one of the most critical parameters for device performance as this determines the lasing wavelength. Wavelength

tolerance varies between applications depending on the target specification. In some cases, very tight control of wavelength (< 0.1 nm accuracy) is needed [113], [119], [120], whereas for others a ± 5 - 10 nm range is acceptable [121], [122]. In either case, assessing the variation in emission wavelength across a wafer is a critical part of the manufacturing process. This is initially done by mapping the FP dip wavelength from the reflectivity spectra as shown in Figure 5.2. The variation in the cavity resonance wavelength is radial, with longer wavelengths in the centre and shorter wavelengths at the edge. The wavelengths range from ∼ 935 nm at the edge to ∼ 945 nm at the centre, with a standard deviation of 1.9 nm. The variation of the cavity resonance wavelength is determined by changes in the optical path length of the inner cavity layers, which comprise the QW active layers and the SCH. Therefore, the combined effect of the shift in layer thickness and composition across the wafer is to reduce the optical path length towards the edge by ∼ 0.5 %. This is consistent with a decrease in refractive index and thickness. The former would be the result of a decreasing Al mole fraction and the latter a reduction in layer thickness. A relative shift of 1% in the Al incorporation results in only a 0.4 nm shift in the FP wavelength. Conversely, a 1% variation in the layer thickness results in ∼ 10 nm shift. Hence, it is likely that the observed decrease of the FP cavity resonance results from a layer thickness variation across the wafer.

5.2.1.2 Characteristics of the Stopband

Properties of the DBR stopband are primarily determined by the thickness and composition of the constituent DBR layers. From Equation 2.8, the number of pairs and the refractive index contrast of the high and low index layers determines the peak reflectivity of the mirror. Figure 5.3 shows the variation of the stopband height (combined DBR reflectivity) which is mostly uniform over the wafer with some regions of lower reflectivity towards the edge and a range of < 5% from the maximum. Assuming no substrate side transmission ($R_b = 1$), the stopband height is taken to represent the top DBR reflectivity. Since the number of DBR pairs is constant at all locations on the wafer, the variation

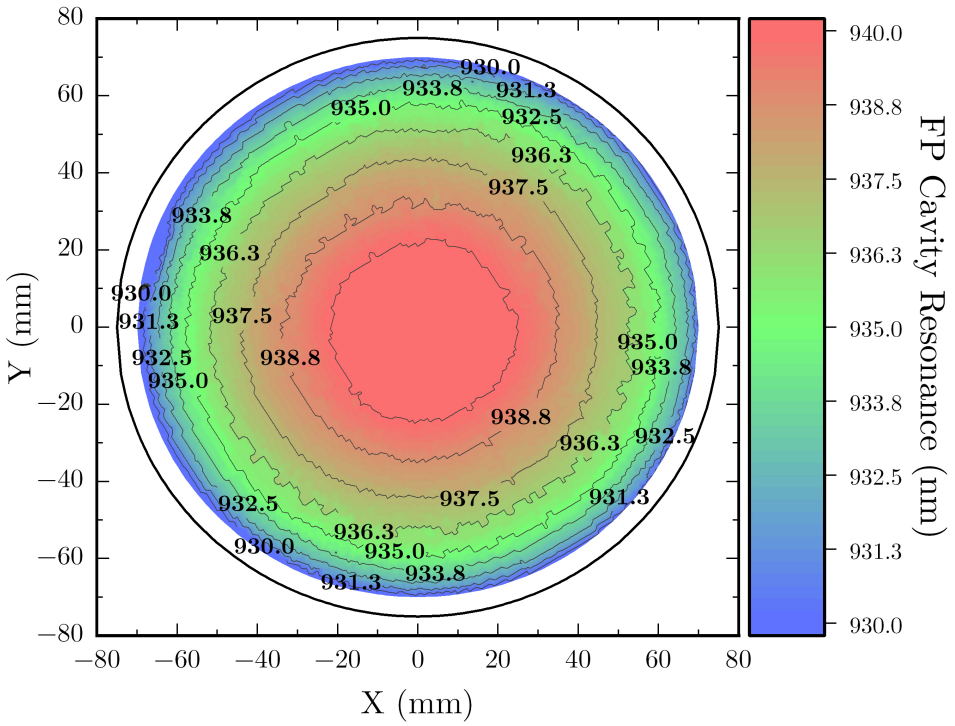

Figure 5.2: Wafer-scale variation of the FP cavity resonance wavelength across a 6-inch wafer. A radial decrease towards the edge is observed, which is consistent with a decreasing optical path length of the cavity layers.

in reflectivity is indicative of changes in refractive index contrast, that is, changes in the Al mole fraction in the AlGaAs layers. The combined thicknesses and refractive indices of the DBR pairs determine the Bragg wavelength, that is, the stopband centre, as detailed in section 2.2.1. For the full VCSEL structure, the overall stopband is a result of the combined reflectivity spectra of the top and bottom DBRs. In Figure 5.4, the stopband centre is shown to vary radially with a centre-to-edge range of $\sim$ 14 nm. The formation of a high finesse VCSEL cavity relies on the alignment of the stopband centre with the FP cavity resonance [45] and in Figure 5.5 (bottom) this variation is presented. A deviation from FP-stopband centre alignment indicates a drift between the separate reflectivity spectra of each DBR. Over the majority of the wafer, the alignment is within 5 nm, which results in the cavity resonance being located centrally within the $\sim$ 100 nm stopband. For these characteristics of the stopband, there is a radial variation with an abrupt shift around 20 mm from the wafer edge which forms a radially symmetric band. This an artifact of the measurement system and data acquisition and does not represent

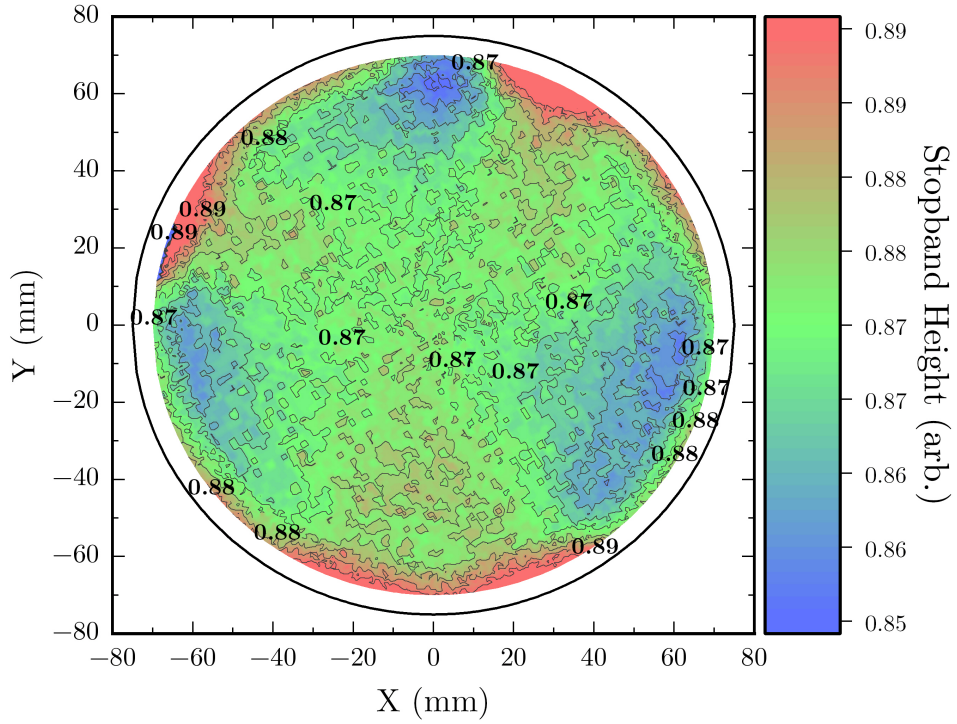

Figure 5.3: Stopband height variation across 6-inch wafer. The stopband height is representative of the DBR mirror reflectivity.

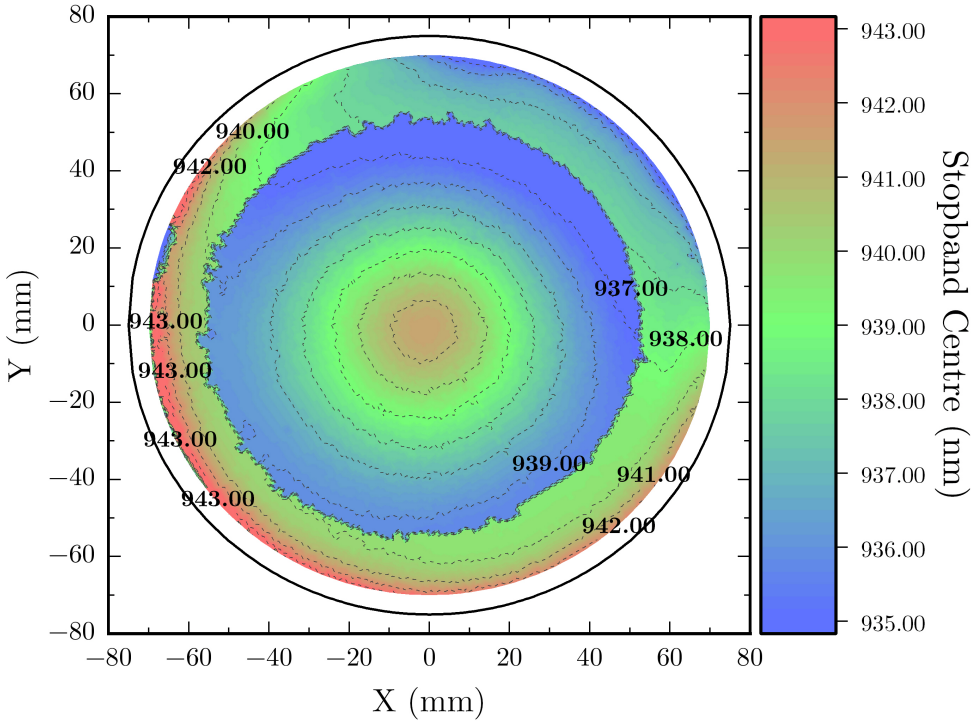

Figure 5.4: Wafer-scale variation of the stopband centre wavelength, $\lambda_{\mathrm{SB,Centre}}$. The abrupt shift 20 mm from the wafer edge is related to the appearance of high-reflectivity sidebands in the measured spectra.

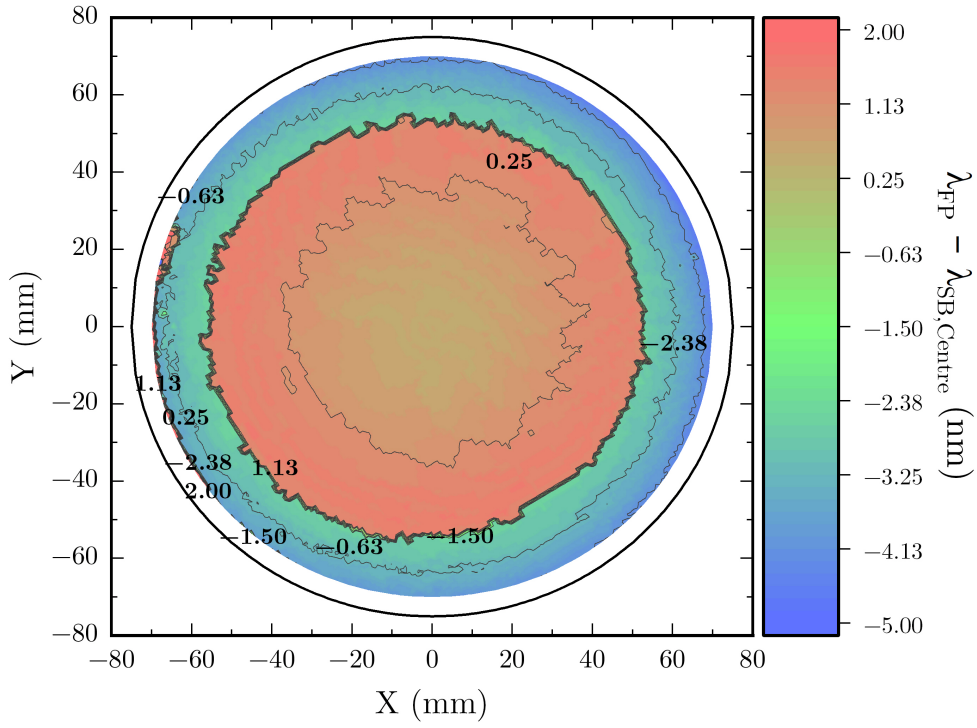

Figure 5.5: Wafer-scale variation of the alignment of the FP wavelength with the stopband centre, $\lambda_{FP} - \lambda_{SB,Centre}$ (bottom). The abrupt shift 20 mm from the wafer edge is related to the appearance of high-reflectivity sidebands in the measured spectra.

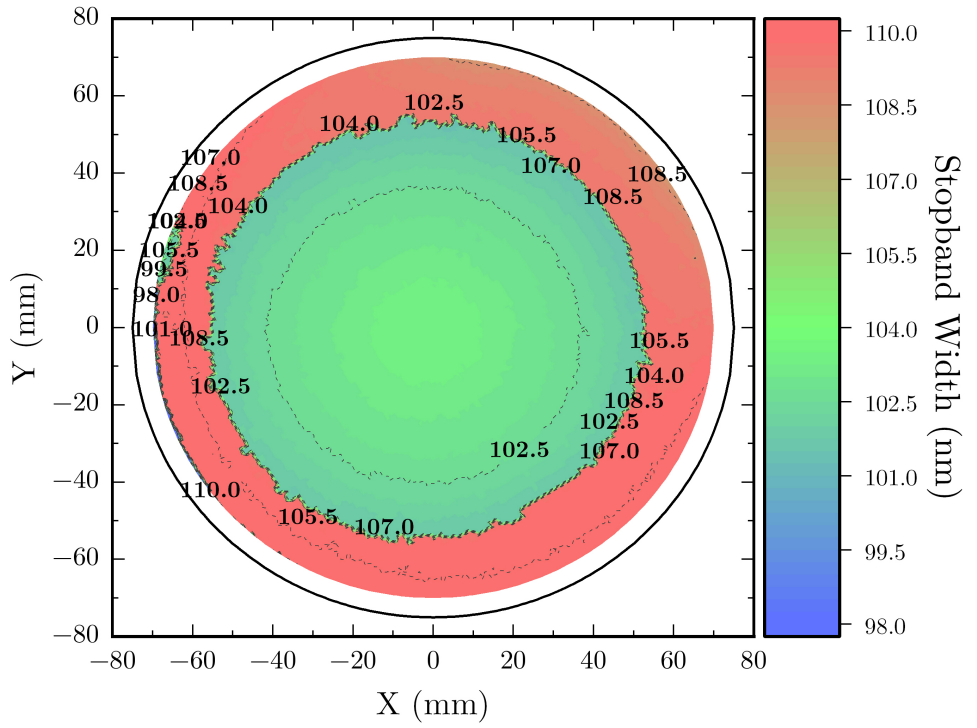

Figure 5.6: Wafer-scale variation of the stopband width. Similar to the stopband centre, the abrupt shift 20 mm from the wafer edge is related to the appearance of high-reflectivity sidebands in the measured spectra.

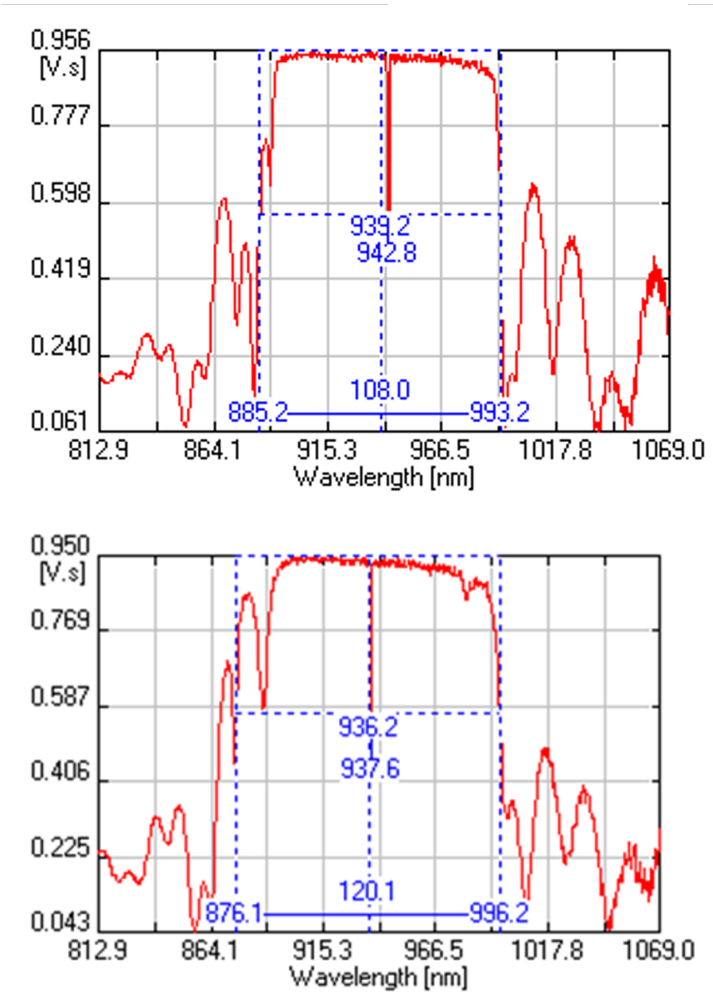

Figure 5.7: Reflectivity spectra measured at the centre (top) and edge (bottom) of a 6-inch wafer. A high-reflectivity sideband is observed on the short wavelength side of the edge spectrum, which results in a 10 nm increase in the stopband width and reduces the stopband centre wavelength.

an abrupt shift in the properties of the epitaxial layers, as explained below. The growth and decay of high reflectivity side bands outside the stopband can occur even with the gradually-varying layer thickness and composition across the wafer. Figure 5.7 shows two reflectivity spectra, measured at the wafer centre and edge. A side band is seen to form on the short wavelength side of the stopband of the edge spectrum, and this results in a 12 nm larger stopband width compared to the centre spectrum. The abrupt shifts seen in Figures 5.4, 5.5, and 5.6 occur at the locations at which the sideband reflectivity exceeds the threshold specified in the automated analysis. The sideband in Figure 5.7 (bottom) also results in the shift of the stopband centre to shorter wavelengths seen in Figure 5.4.

5.2.2 Photoluminescence

Measurement of the photoluminescence spectrum is a valuable method for characterisation of the active layers. If performed on a full VCSEL stack, light would only be emitted at the wavelengths corresponding to low reflectivity (the FP resonance wavelength and regions outside the stopband). As such, PL characterisation is performed on calibration wafers grown without the top DBR. The PL peak wavelength is an important parameter specified in the design of the epitaxial structure and its wafer-scale measurement provides information on the properties of the QWs. A PL spectrum measured at the centre of a 6-inch wafer is shown in Figure 5.8. From the spectrum, the PL wavelength, intensity, and linewidth (FWHM) can be extracted. In this case, the PL wavelength is 923.3 nm and the linewidth is 20.3 nm. Similar to the stopband height, the intensity of the PL spectrum is un-calibrated so can only be used to assess relative changes across a wafer. The integrated signal quantifies the area under the curve of the spectrum which thus accounts for both the intensity and linewidth (as well as other features present). The PL wavelength is representative of the photon energy corresponding to recombination in the QW layers, which is given by Equation 2.9. Assuming the QW width is known, the material composition can be estimated from the PL wavelength. For this structure, the QW layers are $In_xGa_{1-x}As$ and, from the spectrum in Figure 5.8, the indium mole fraction, x, is calculated to be approximately 0.12 at the centre of the wafer. This epi-structure is designed for 940 nm emission wavelength, however, the QW layers must be grown to ensure that the PL wavelength is significantly shorter than this to account for pumping-related self-heating effects, as well as bandgap renormalisation and the quantum-confined Stark effect. Furthermore, the relation between the PL wavelength and the peak gain wavelength is non-trivial and, for a given VCSEL, is influenced by the specific device design and processing. As a result, the gain peak wavelength is not easily ascertained from the PL wavelength. The spatial variation is again found to follow a radial distribution with a range of < 1.5 nm centre-to-edge and a standard deviation of ~ 0.4 nm. The uniformity of the PL wavelength is much better than that of the FP resonance due to

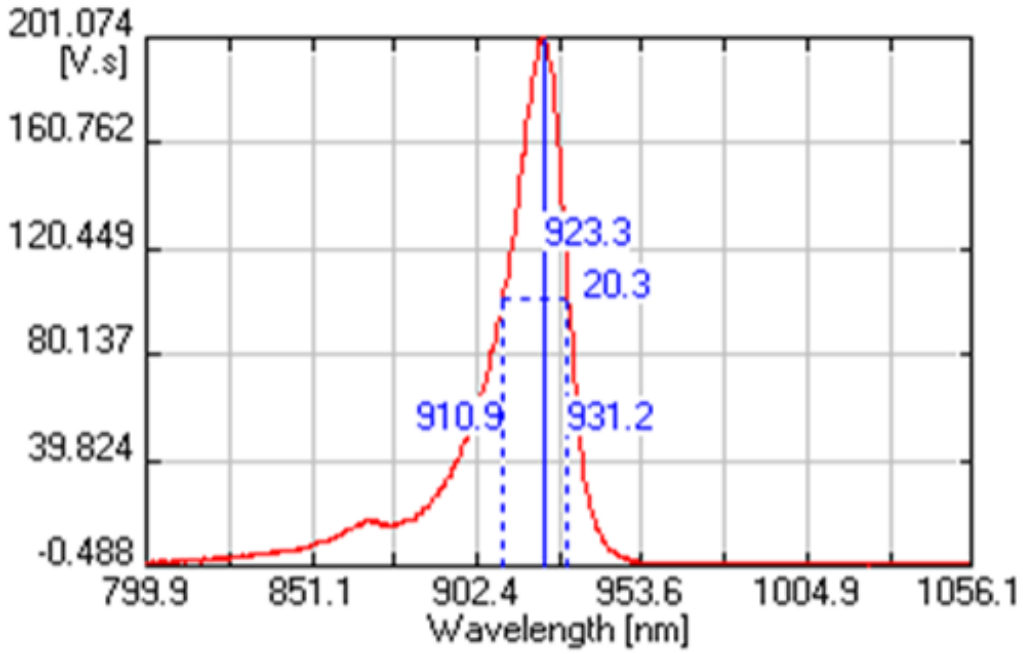

Figure 5.8: Photoluminescence spectrum for VCSEL active region calibration structure measured at the centre of a 6-inch wafer. The PL wavelength is a 923.3 nm and the linewidth (FWHM) is 20.3 nm, corresponding to $\sim$ 30 meV.

the sensitivity of the cavity resonance to layer thickness variation. As an example, a 5% variation in layer thickness for a 6 nm $In_{0.12}Ga_{0.88}As$ QW with $Al_{0.3}Ga_{0.7}As$ barriers results in just a 3 nm ($< 0.5\%$) shift in the e1-h1 transition wavelength. Conversely, the same % thickness variation for a cavity designed for 1000 nm emission wavelength results in a 50 nm shift in the resonance wavelength. As such, when subject to typical changes in layer properties, the PL wavelength is significantly more uniform across the wafer, and this is shown in Figure 5.9. The layer thickness can be controlled to within approximately 0.5% for modern commercial reactors and this has a negligible impact on the QW transition energy. From simple calculations of the ground state QW transition energy, a decrease of 0.2% in the In content would result in the observed wavelength shift ($x_{centre} = 0.12, x_{edge} = 0.010$). Therefore, the observed shift in PL wavelength is likely mainly driven by an increasing bandgap energy associated with a decreasing indium mole fraction towards the wafer edge with the thickness variation having only a small impact.

In addition to the PL wavelength, the integrated signal can also provide relative information on the quality of the QWs if it is assumed the alignment and collection is the

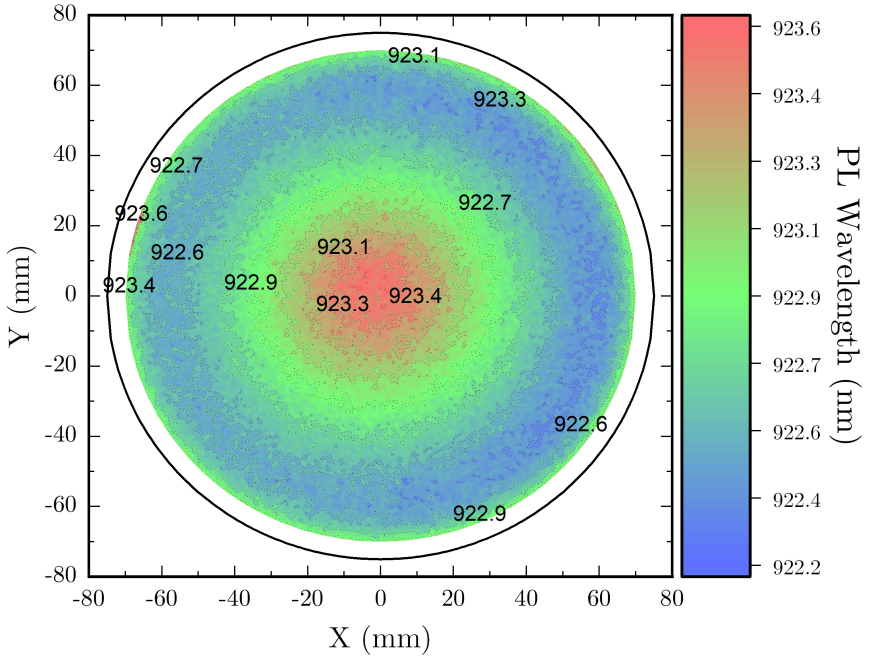

Figure 5.9: Wafer-scale variation of PL peak wavelength. A radial decrease towards the edge is observed, with a centre-to-edge difference < 1.5 nm.

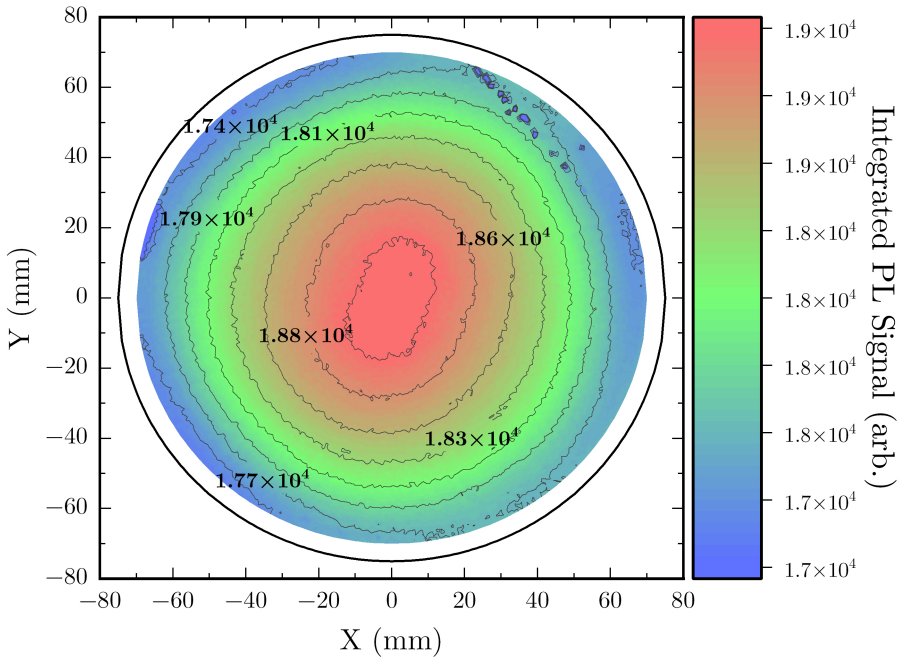

Figure 5.10: Wafer-scale variation of the integrated PL signal. The integrated signal accounts for both the intensity and linewidth of the peak.

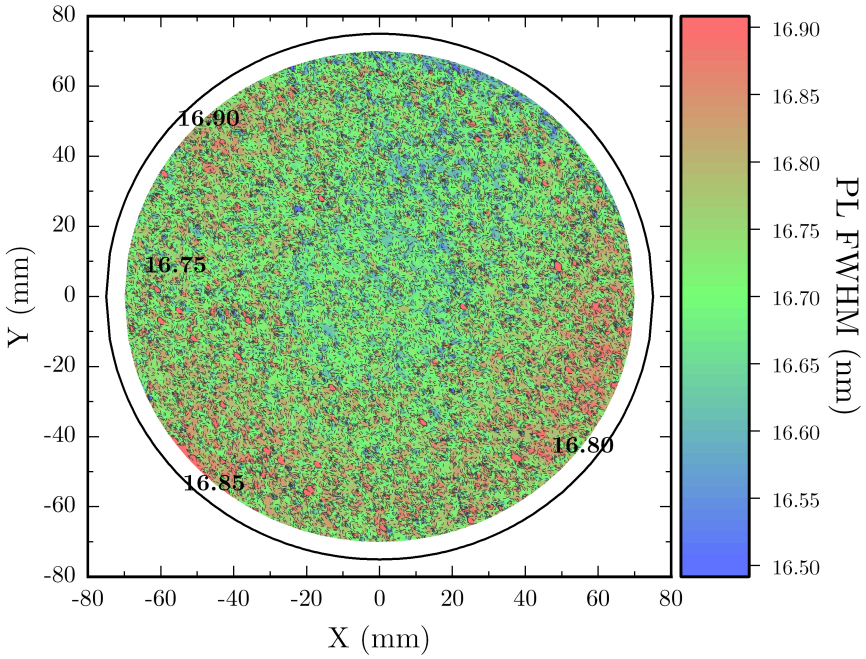

Figure 5.11: Wafer-scale variation of PL peak linewidth (FWHM). No discernible variation across a 6-inch wafer is observed.

same for each case. The integrated signal accounts for both the intensity and linewidth of the peak, and so can highlight regions with a high density of defect states. As discussed in section 3.4.2, a strong PL peak indicates a high QW radiative efficiency. Further, the linewidth of the PL peak, given by the FWHM, can also provide qualitative information on the defect density, with a narrow linewidth indicative of a low density of recombination centres. Here, the measured linewidths are $\sim$ 30.0 meV across the whole wafer, which is slightly larger than that expected thermal broadening from at $\sim$ 300K ($\sim$ 26.0 meV). This suggests no unintended effects arising from growth. Note: for quantitative information on the defect density, most often surface scanning and/or x-ray diffraction techniques are employed, but this is beyond the scope of this thesis.

5.2.3 Sheet Resistance

From from C-TLM measurements of the p-contact metallisation, a radial variation of the sheet resistance, R_{sheet}, is observed. The sheet resistance is representative of the conductivity in the uppermost layers of the top DBR, and is dominated by the p+ doped

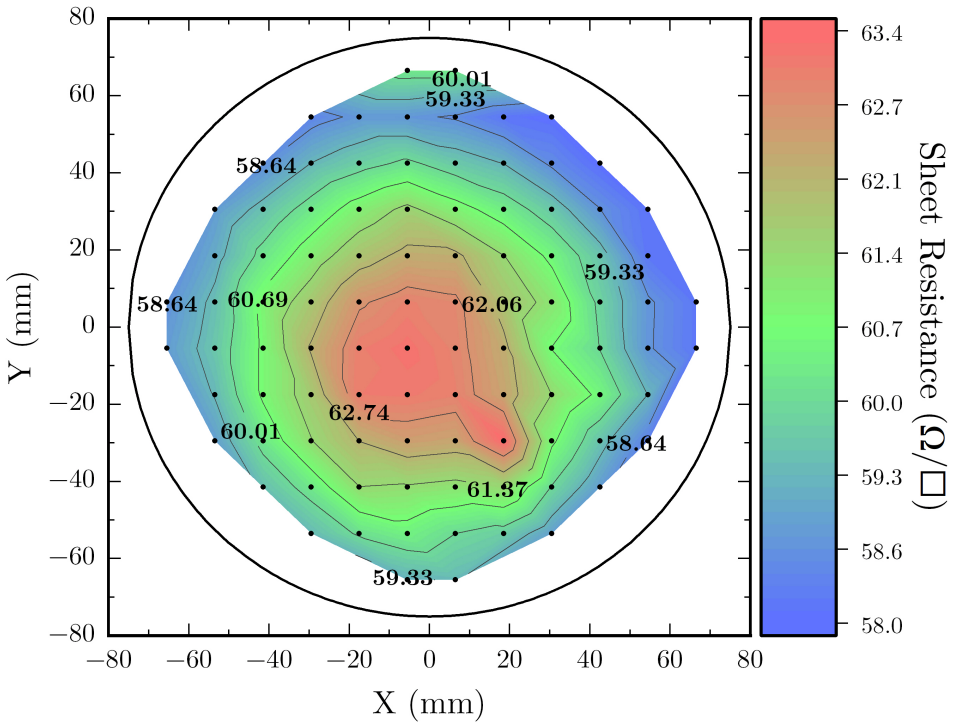

Figure 5.12: Wafer-scale variation of the sheet resistance measured by C-TLM. The radial decrease indicates a spatial variation in the doping concentration in the p+ GaAs cap layer.

GaAs cap and sub-cap layers. R_{sheet} decreases from $\sim$ 63 to 58 Ω (12%) towards the wafer edge, which suggests a lower doping concentration at the wafer centre. The acceptor concentration in GaAs has been shown to be strongly dependent on temperature [123], hence it is possible that this is indicative of a slight growth temperature gradient across the wafer - lower at the centre. If so, then the spatial variation of the doping concentration is likely to be systematic through the layers of the top DBR. In which case, it would be expected that the rate of free carrier absorption would vary according to the doping profile. Further investigation would be needed to calibrate the variation of the sheet resistance with the doping profile and to study the effect on the internal optical loss, but this is beyond the scope of the investigation here.

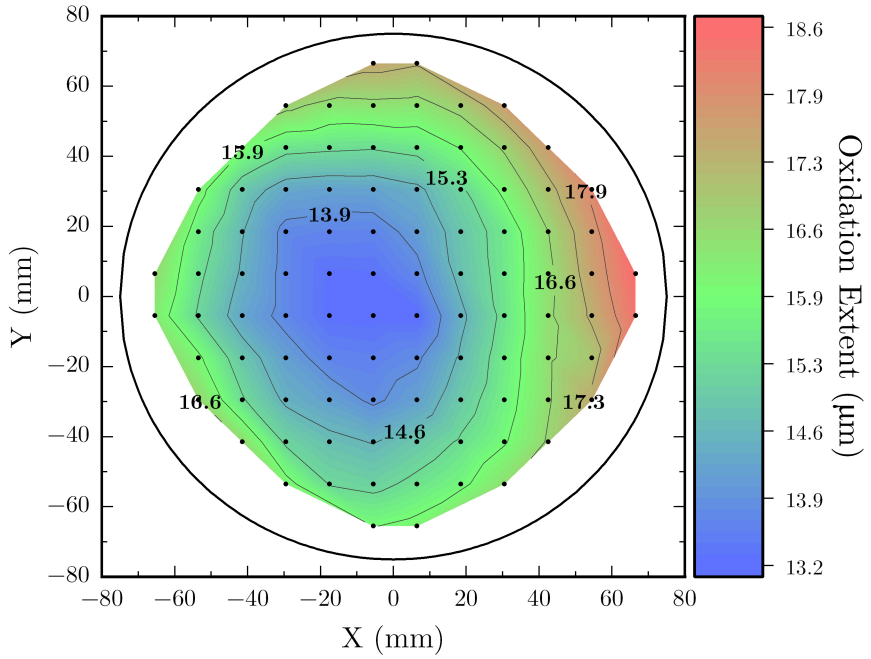

Figure 5.13: oxidation extent variation of a 6-inch GaAs substrate wafer oxidised in a conduction-based furnace. The radial variation is the result of temperature gradients driven by the bow of the wafer.

5.3 Oxidation Non-Uniformity

One of the most critical parameters in the processing of VCSELs is the oxide aperture diameter. Variation in the device active volume, determined by the oxidation extent, can result in a significant variation in performance characteristics, particularly the threshold current, series resistance, and optical power, although the beam quality and lasing spectra can also be affected. As such, maximising the wafer-scale uniformity of the oxide aperture is an important concern. The variation in oxidation extent on a 6-inch GaAs wafer is shown in Figure 5.13. The oxidation extent increases approximately radially from the centre to the edge, with a linear component from the furnace (see below). The total range across the wafer is ~ 6 µm, which results in a variation of up to ~ 12 µm in oxide aperture. As described in section 3.3.3, the oxidation rate is highly sensitive to temperature therefore any temperature non-uniformity drives oxidation non-uniformity. The furnace and wafer temperatures are measured in-situ and the resulting contour plots are shown in Figure 5.14. From Figure 5.14, the origins of the oxidation variation can be

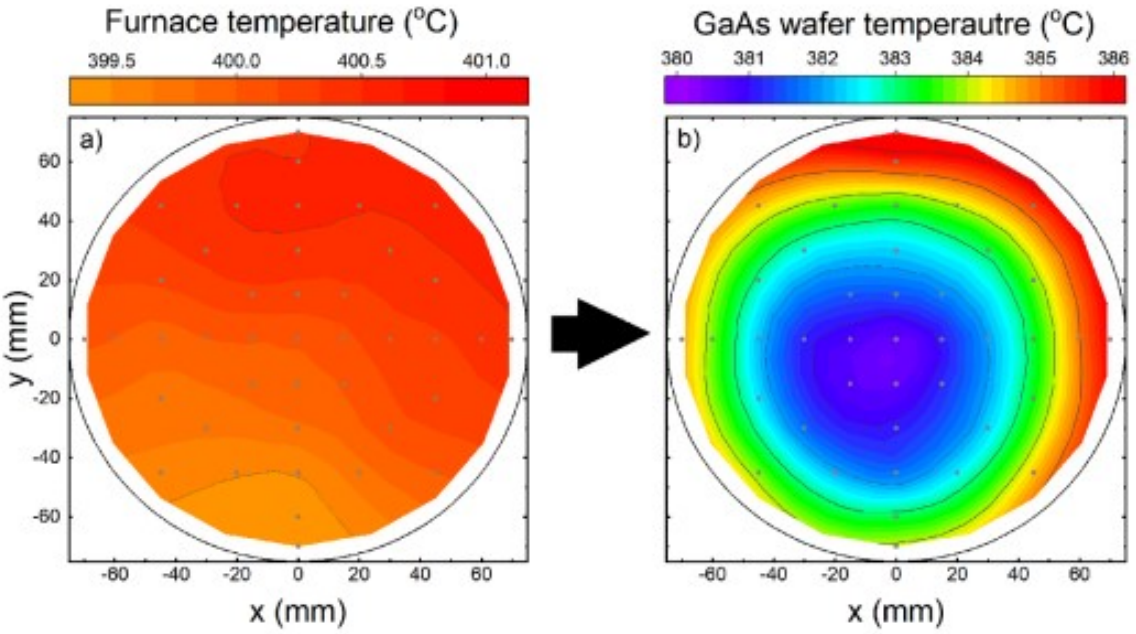

Figure 5.14: Furnace and wafer temperature measured in-situ during thermal oxidation. The furnace temperature varies linearly by ~ 2 °C. The radial temperature variation is driven by the strain-induced bow of a 6-inch wafer.

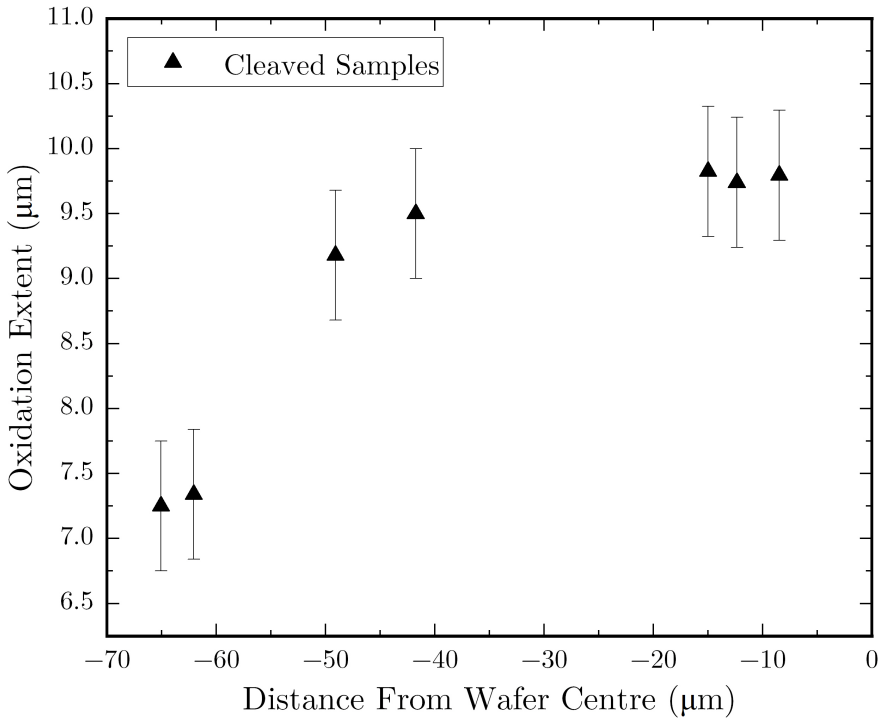

Figure 5.15: oxidation extent of cleaved samples as a function of distance from the centre of a 6-inch wafer. The effects of wafer bow are removed where fabrication is done on small cleaved samples. A decrease in oxidation rate towards the wafer edge is observed, the opposite effect of when processed as a whole wafer.

clearly seen. The furnace temperature varies linearly by 2 °C. However, more significantly, the wafer temperature is seen to vary radially with a maximum centre-to-edge difference of 6°C, and this is attributed to the strain-induced bow which results from the growth of the bottom (AlAs-containing) DBR mirror on a GaAs substrate (as described in section 3.2.4) and the resulting varying contact with the heat source in the furnace. Given that the relationship between oxidation rate and temperature is exponential, the wafer bow drives the radial variation of oxidation extent that is seen in Figure 5.13.

When the effects of wafer bow and temperature variation are removed by fabrication on small cleaved samples from the edge and centre of a 6-inch wafer, the opposite result is observed. The material cleaved from the edge of the wafer is found to oxidise more slowly than that of the centre. This is shown in Figure 5.15. From the information presented in section 3.3.3, this is indicative of a decrease in Al mole fraction and thickness in the oxidation layer towards the wafer edge. These layers are thin (< 50 nm), and therefore the oxidation rate is also sensitive to layer thickness shifts. For an assumed 0.2% variation in the Al fraction (based on the analysis in section 5.2.2), the effect on the oxidation rate is likely not sufficient to produce the observed centre-to-edge difference in oxidation extent alone.

5.4 Device Performance

5.4.1 Lasing Wavelength

In section 5.2.1.1, the material cavity resonance wavelength was shown to vary radially across the wafer, indicative of a radial variation in thickness/composition of the inner cavity layers. In Figure 5.16, the peak lasing wavelength is shown to follow the same trend. When confinement effects are negligible, that is, when the oxide aperture is larger than ~ 4 µm, the lasing wavelength is principally determined by the material cavity resonance. However, as the QuickSEL devices are driven CW, there can also be a com-

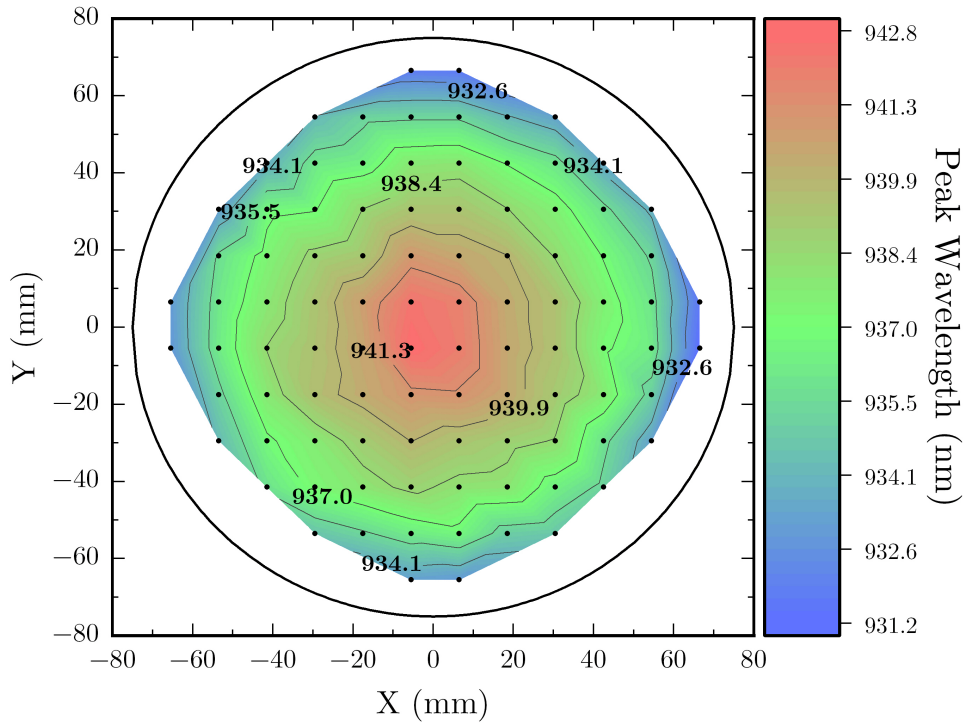

Figure 5.16: Wafer-scale variation of the peak wavelength measured for 38 µm mesa devices (8-9 µm aperture at centre) at 2mA.

ponent of the measured wavelength that is driven by self-heating. A variation in oxide aperture complicates matters further, as this results in different internal temperatures for a given bias current. To account for this, large aperture devices are mapped, and spectral measurements are performed at currents close to threshold. The result of these considerations is seen in Figure 5.17 with the comparison of the measured peak wavelength of 38 µm mesa (8-9 µm aperture at the centre) devices at 2mA and the cavity resonance wavelength along a central horizontal line profile. Clearly, the values closely match the FP resonance wavelength and are thus representative of the properties of the epi-layers.

5.4.2 Threshold Requirement

VCSEL threshold current, I_{th}, is highly sensitive to the oxide aperture diameter. As such, if there is a significant on-wafer variation of oxidation extent, the measured threshold currents track with this variation. This can be seen in Figure 5.18 for a wafer oxidised in a conduction-based furnace with a 3-4 µm oxidation extent variation, which translates to

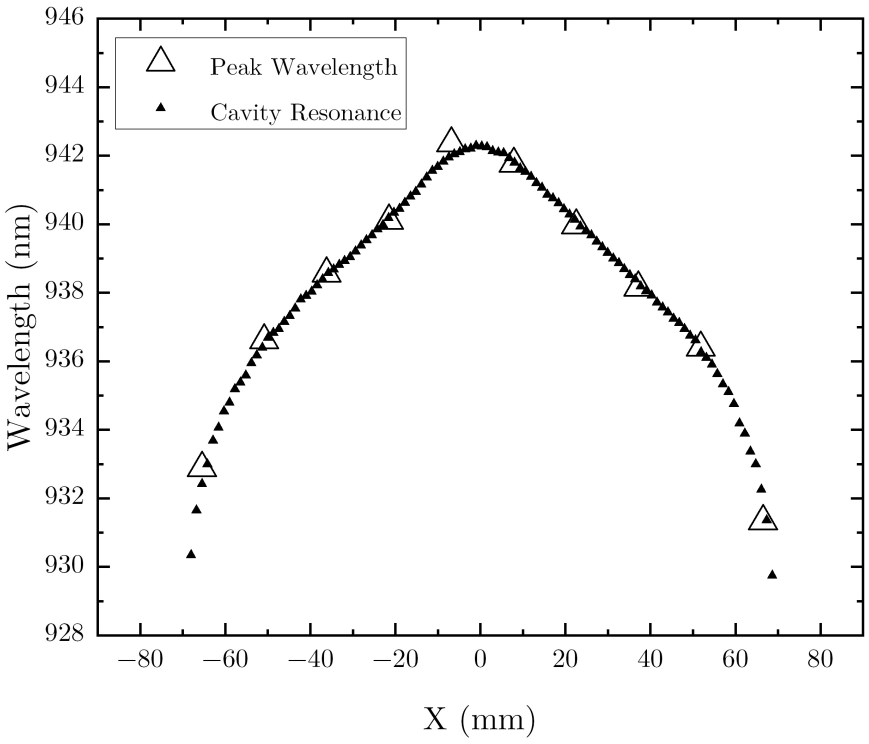

Figure 5.17: Comparison of FP resonance wavelength and peak lasing wavelength just above threshold of 38 µm mesa devices (8-9 µm aperture at centre). The data points represent a horizontal line profile across the 6-inch wafer of Figure 5.2 and 5.16.

a 6-8 µm oxide aperture variation. The origin of the non-uniformity in oxidation extent is the bow of the wafer, as described in section 5.3. This results in factor of 6 variation of I_{th} from the wafer centre, with values for 38 µm mesas ranging from ~ 0.2 mA at the edge where apertures are small to ~ 1.2 mA at the centre where apertures are large. This is compared to a wafer oxidised in a convection-based furnace with < 1 µm oxidation extent variation, for which the threshold current is plotted in Figure 5.19 and which results in a narrower spatial distribution.

To de-couple these effects from device performance, the oxidation extent is measured at locations across the wafer, from which the threshold current density, J_{th}, can be mapped. This is less sensitive to aperture variation so long as scattering and diffraction losses are negligible (apertures > 4 µm). The resulting plot is shown in Figure 5.20. It can be seen that, even after accounting for the impact of oxide aperture, there remains a radial variation in threshold current density. This is shown to be driven by the detuning of the gain peak and cavity resonance wavelengths. In Figure 5.21, the temperature

dependence of threshold current density for devices at the wafer centre and edge are compared. The minima correspond to the alignment of the cavity resonance with the spectral peak of the gain, and this occurs just above room temperature at the edge, compared to $\sim$ 50 °C at the centre. Non-uniformity in the gain-peak detuning is to be expected given the different sensitivities of the cavity resonance and photoluminescence peak wavelengths to epi layer variations presented in this chapter. One consequence of this spatial variation of the detuning is that the threshold current uniformity increases at elevated temperatures (closer to the intended temperature of operation $\sim$ 50 °C). The room temperature gain peak wavelength can be calculated by applying the analysis introduced in section 2.3. The temperature corresponding to gain peak alignment, T_{min} is extracted as $\sim$ 50 and $\sim$ 29 °C for the wafer centre and edge, respectively. Using the fact that the shift of the gain peak with temperature is $\sim$ 0.3 nm/°C (assuming the gain-peak wavelength changes according to the temperature coefficient of the bandgap), the room temperature gain peak wavelength is then calculated as 935.6 and 935.1 nm at the wafer centre and edge, respectively. This difference is of the same order as that of the measured PL wavelength from Figure 5.9. Further, these values can be directly compared to initial design simulations, which has utility as feedback to epitaxy. From section 5.2.2, the PL peak wavelengths are measured as 923.3 and 923.9 nm for the centre and edge, respectively, thus the calculated room temperature gain peak wavelengths are within the expected 10-15 nm redshift relative to the PL. This analysis assumes that any wavelength shift resulting from the difference in threshold requirement (hence carrier density) at different temperatures is negligible. With the impact of the on-wafer variation of oxide aperture de-coupled from device performance and the alignment of the gain peak with the cavity mode wavelength accounted for, the measured threshold current density provides a representative measure of the properties of the epitaxial layers. Again, applying the methods presented in section 2.3.2, it is possible to extract values relating to the optical loss of the devices. The fitting coefficient α is the minimum achievable threshold current (density) and this value is reached when the device is operated at T_{min}. The value of α is determined by the DBR mirror loss and the internal optical loss. Given the relative

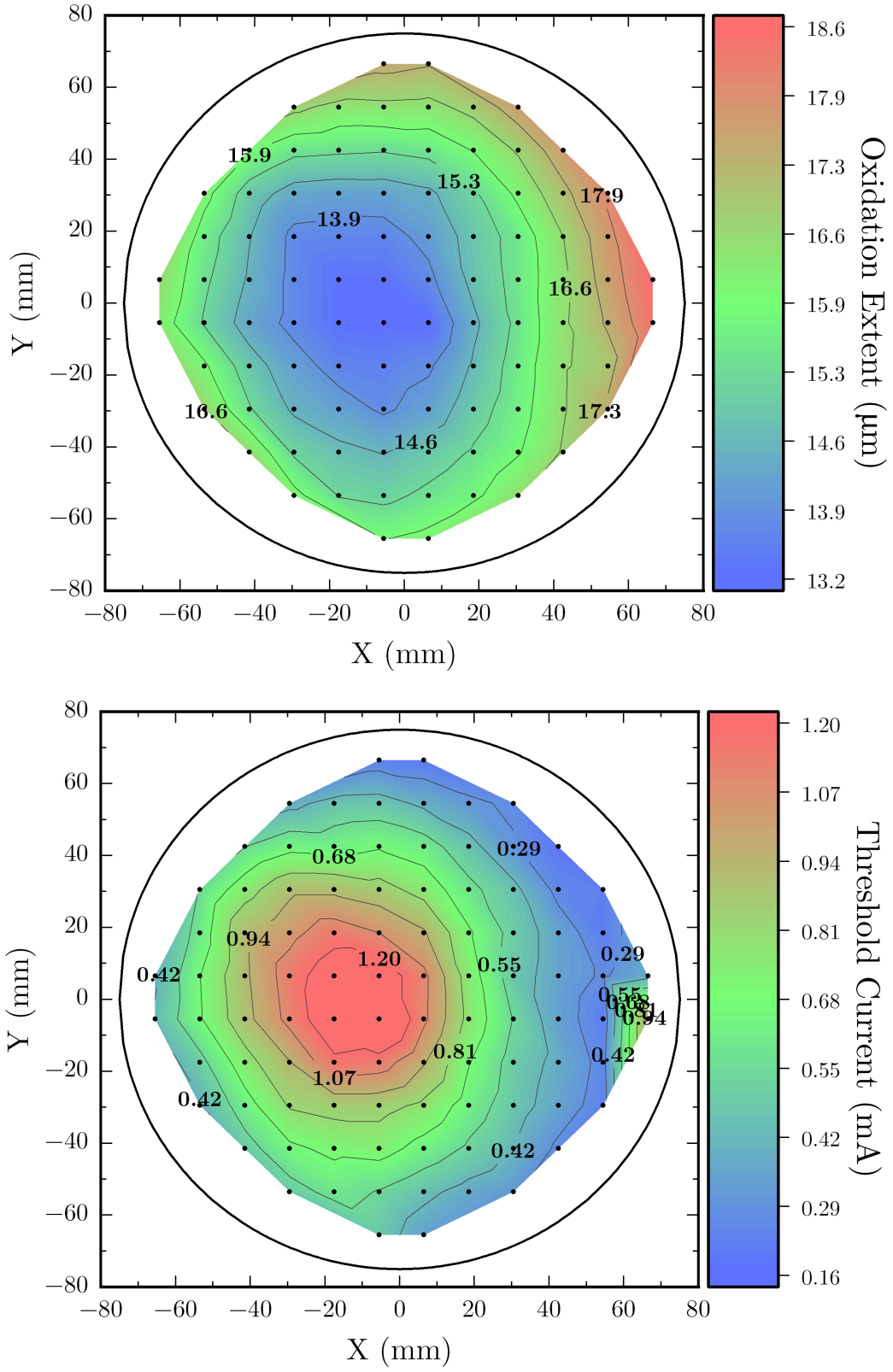

Figure 5.18: Oxidation extent variation from a conduction-based furnace (top) and threshold current variation for 38 µm mesa VCSELs (∼ 12 µm aperture at centre) (bottom). The 5 µm oxidation extent variation results in a factor of 6 centre-to-edge variation in threshold current.

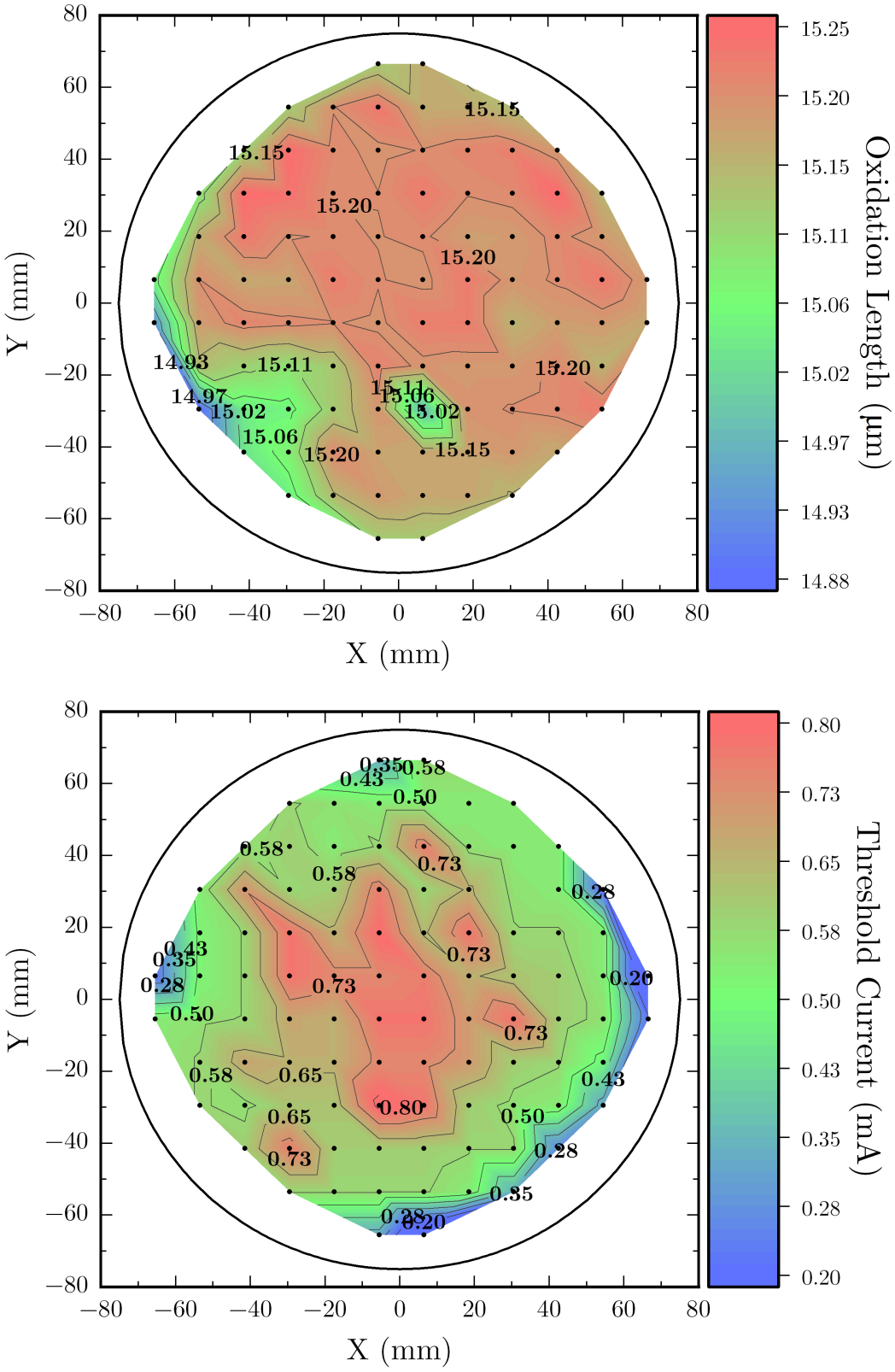

Figure 5.19: Oxidation extent variation from a convection-based furnace (top) and threshold current variation 38 µm mesa VCSELs (8-9 µm aperture at centre) (bottom). Despite the highly uniform oxidation extent, a sizeable centre-to-edge variation in threshold current remains.

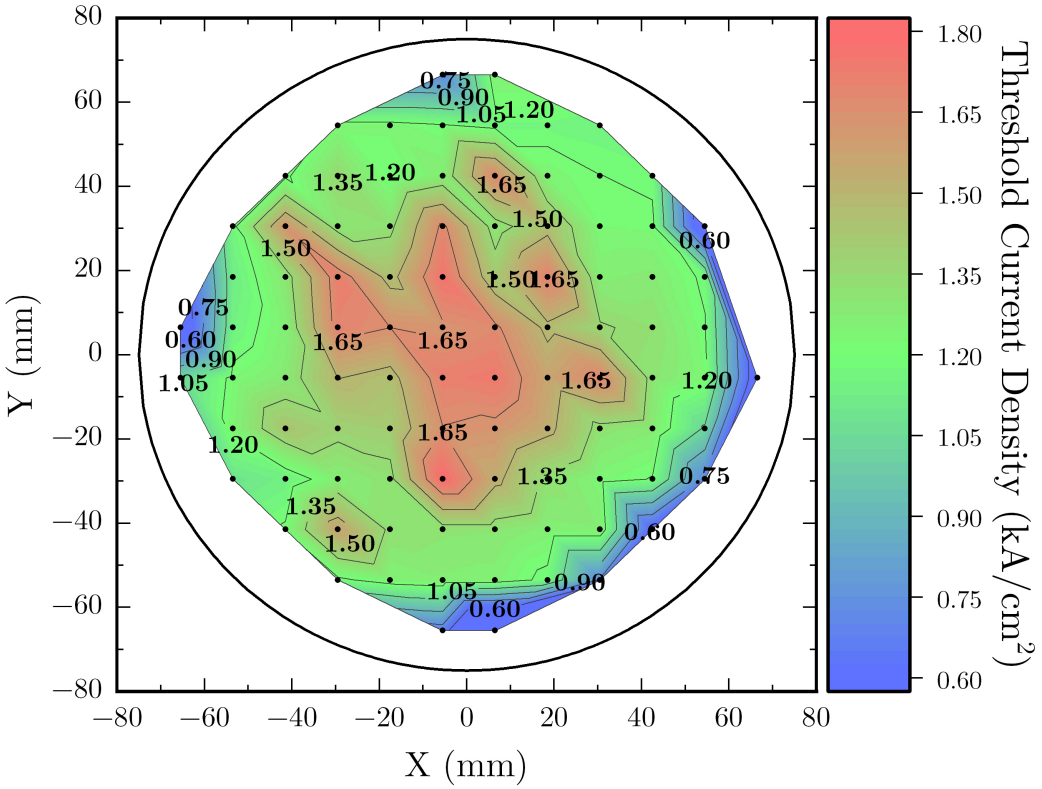

Figure 5.20: Wafe-scale variation of threshold current density for 38 µm mesa VCSELs (8-9 µm aperture at centre) across a wafer oxidised in a convection-based furnace. The residual variation is derived from the properties of the epi-layers.

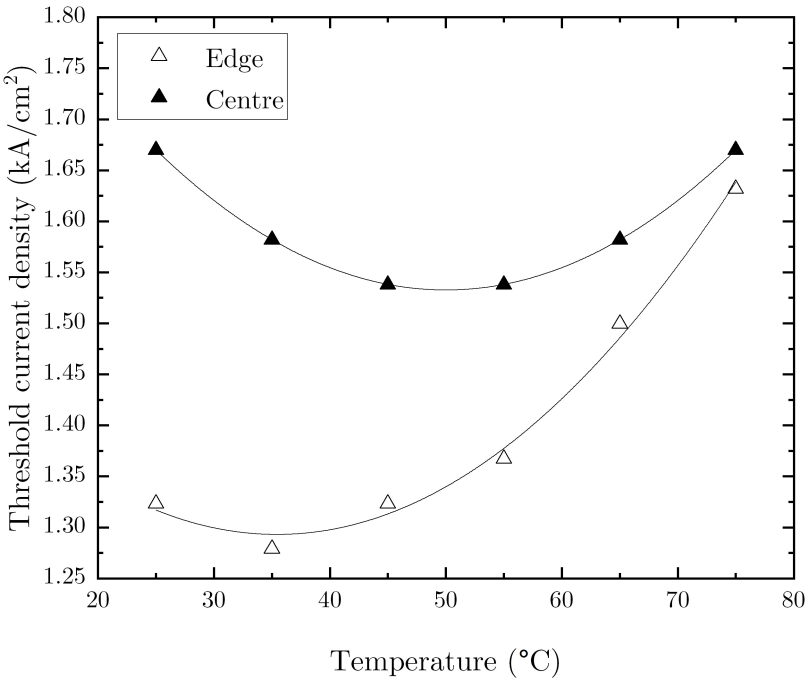

Figure 5.21: Threshold current density as a function of ambient temperature for ∼ 8 µm aperture VCSELs at the wafer edge and centre. The 20 °C difference in T_{min} indicates a spatial variation in the gain peak detuning.

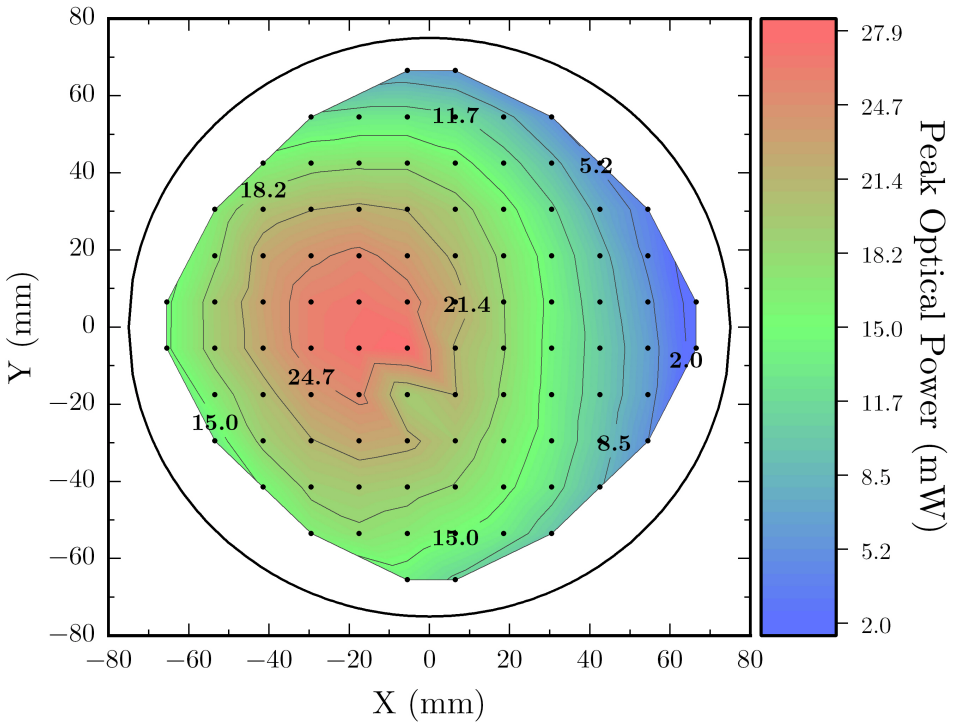

Figure 5.22: Wafer-scale variation of the peak optical power for 38 µm mesa VCSELs (∼ 12 µm aperture at centre), from a wafer oxidised in a conduction-based furnace.

increase in DBR mirror reflectivity at the wafer edge, shown in Figure 5.3, it is likely that the variation in α is influenced by the change in the mirror loss. Values for α are extracted as 1.51 and 1.28 kA/cm^2 at the centre and edge, respectively, the difference of which is on the same order as that observed for the reflectivity ($\sim$ 20%).

5.4.3 Optical Power and Efficiency

The wafer-scale variation in oxide aperture also translates into a variation in optical power, and this can be seen in Figure 5.22. The measurements shown in the figure are performed on the same wafer as that of Figure 5.13, which is oxidised in a conduction-based furnace. The spatial variation matches that observed for the threshold current, producing greater than a factor of 6 change in the measured peak optical power. This is contrasted with Figure 5.23 where the maximum output power of a wafer oxidised in a convection-based furnace with an oxidation extent variation of < 1 µm is mapped. For this case, the range in measured optical power is $\sim$ 3 mW (decrease of 20% from optical power at

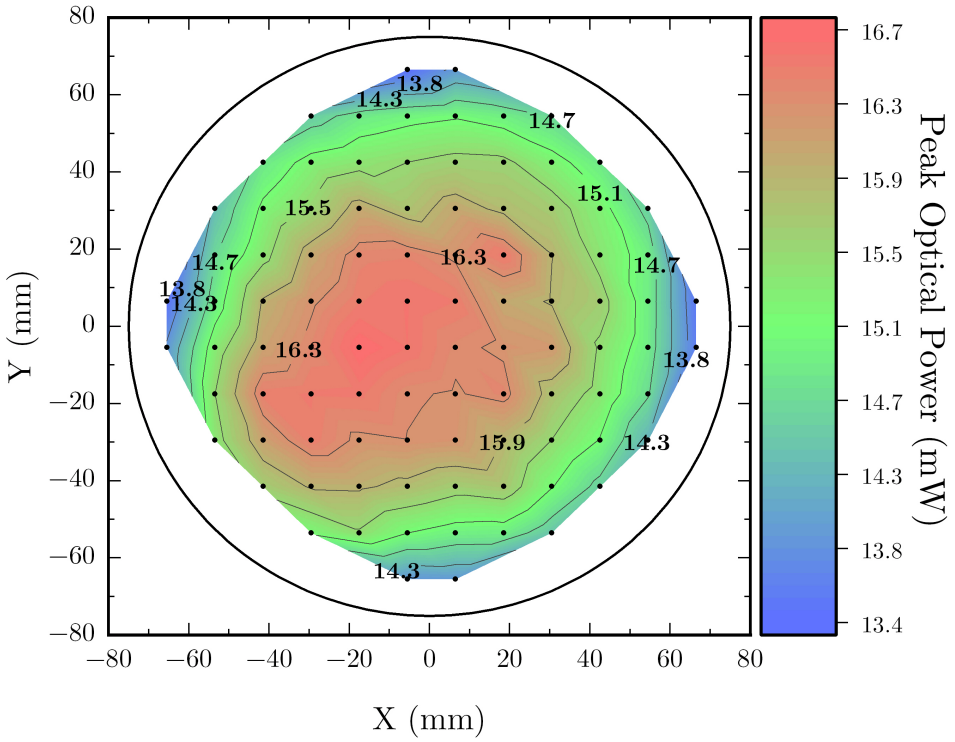

Figure 5.23: Wafer-scale variation of the peak optical power for 38 µm mesa VCSELs (8-9 µm aperture at centre), from a wafer oxidised in a convection-based furnace.

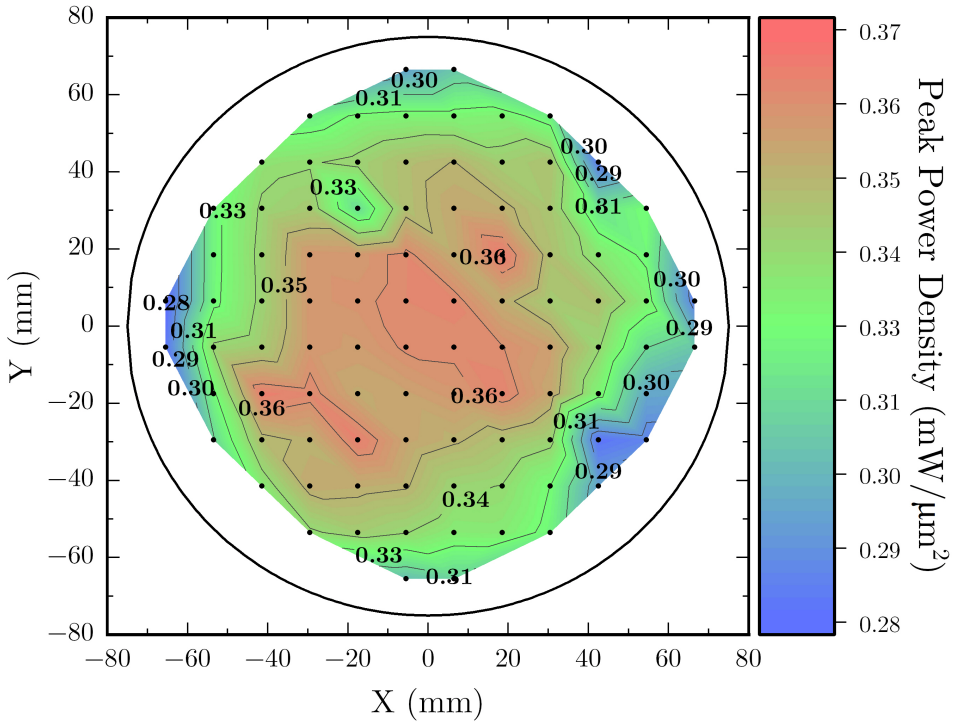

Figure 5.24: Wafer-scale variation of the peak optical power density for 38 µm mesa VCSELs (8-9 µm aperture at centre), from a wafer oxidised in a convection-based furnace.

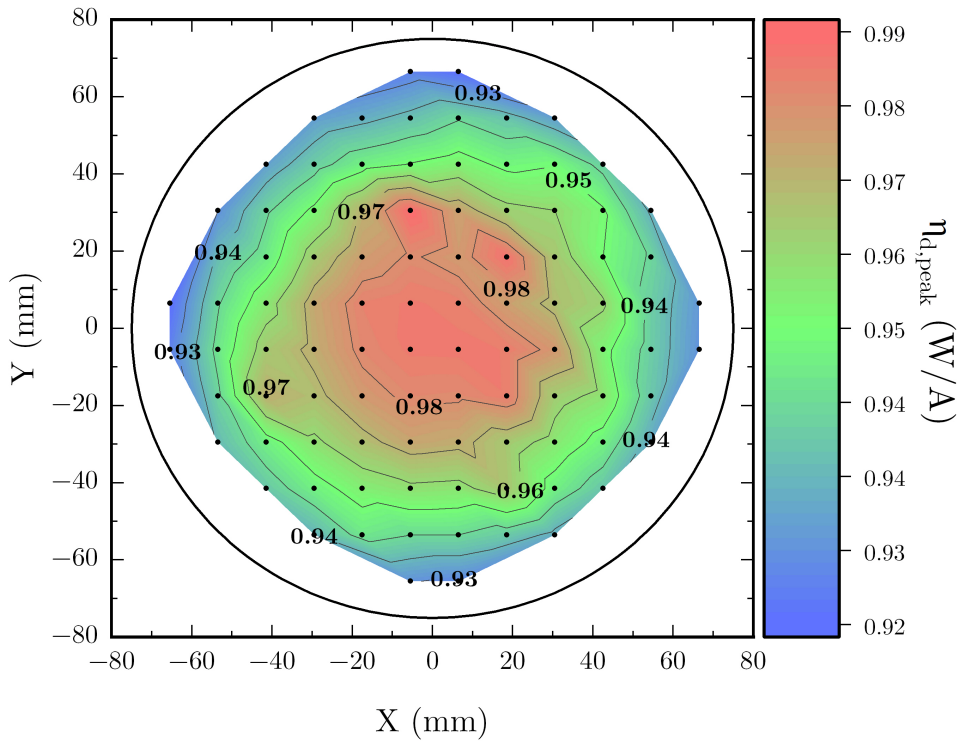

Figure 5.25: Wafer-scale variation of the peak external differential efficiency ($\eta_{d,peak}$ for 38 µm mesa VCSELs (8-9 µm aperture at centre), from a wafer oxidised in a convection-based furnace.

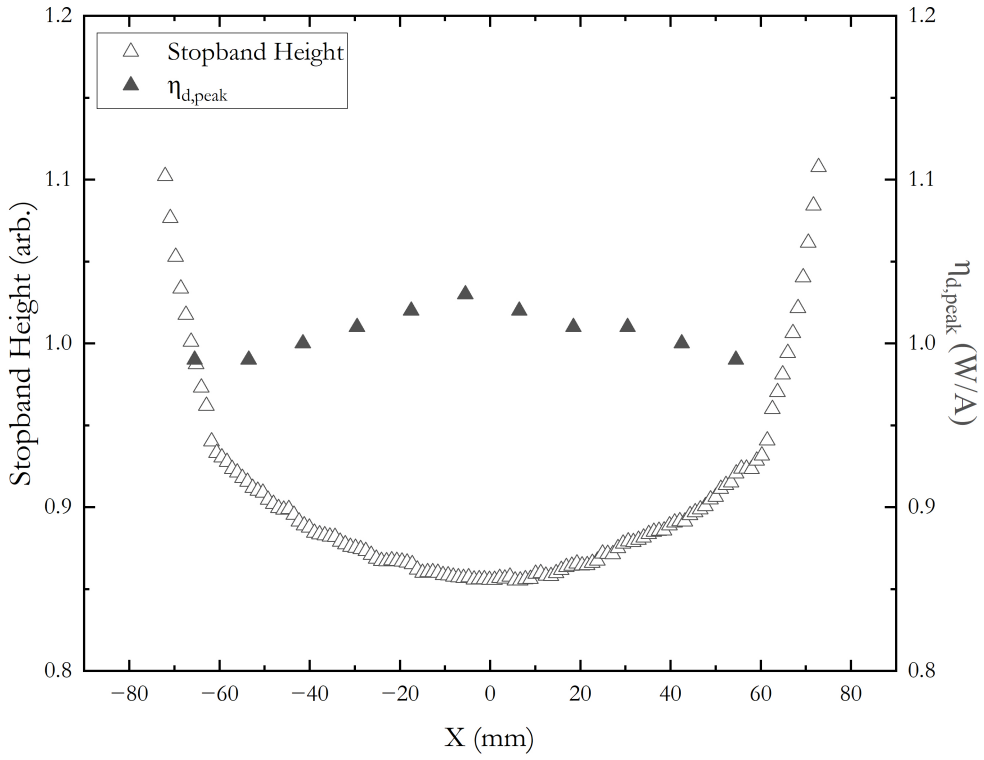

Figure 5.26: Comparison of stopband height and $\eta_{d,peak}$ of 38 µm mesa devices (8-9 µm aperture at centre). The data points represent a horizontal line profile across a 6-inch wafer.

wafer centre) although, over most of the wafer, the variation is closer to 1 mW ($\sim$ 10% drop from wafer centre). To account for residual oxide aperture variation, the optical power density can instead be considered, and this is shown in Figure 5.24. Similar to the threshold current density, the optical power density, is a quantity which better represents the properties of the epi-layers as opposed to the geometry of the device measured. There is a decrease in power density of $\sim$ 10% towards the edge of the wafer. Similarly, in Figure 5.25, the external differential efficiency is also found to decrease by a similar degree towards the wafer edge. This is seen more clearly in the line profile of Figure 5.26. It is possible that the decrease in differential efficiency and optical power density is derived from the increasing mirror reflectivity, as characterised by the stopband height in Figure 5.3. From Equation 2.17, η_{d} is also dependent on the internal optical loss, α_{i}, and the internal quantum efficiency, η_{i}. From the spatial variation of the sheet resistance (Figure 5.12), it is likely that the doping concentration (hence rate of free carrier absorption) is lower at the wafer centre. Assuming absorption by free carriers is the dominant source of internal optical loss, this would result in a decrease of α_{i}. Furthermore, the internal quantum efficiency is dependent on the rate of carrier leakage out of the QWs. If the Al composition of the barriers were to decrease towards the wafer edge, the QW barrier height would be reduced, thus increasing carrier leakage and reducing η_{i} and, as a result, η_{d}. This is a possibility, given that the In mole fraction was deduced to decrease towards the edge. Further investigation would be required to fully understand what drives the variation in the external differential efficiency and optical power density across the wafer, however, this is outside the scope of this thesis.

5.5 Summary

In this chapter, the quality and uniformity of generic MOVPE-grown 6-inch GaAs substrate VCSEL epi-wafers designed for 940 nm emission wavelength was assessed. These assessments were based on post-growth material characterisation, mapping of the oxide

aperture, and through on-wafer testing of QuickSEL devices. In volume production, target yields are expected to be in excess of 90% and, as such, the control of many growth conditions are needed to ensure a uniform deposition throughout the reactor chamber. A radial variation of both the properties of the epitaxial material and QuickSEL device performance is attributed to the spatially non-uniform growth rate in the reactor chamber, as previously illustrated in Figure 3.2. The rotation of the substrate during growth produces a spatial averaging of the deposition rate across individual wafers. This, coupled with the the non-linear decrease from the central gas inlet to the edge of the reactor, leads to a higher deposition rate at the wafer centre, resulting in thickness variation which decreases towards the wafer edge. This was observed to drive the non-uniformity in key parameters, which are summarised here.

From reflectometry measurements, the FP resonance was found to shift to a shorter wavelength towards to the edge of the wafer, which was attributed to a 0.5% decrease in layer thickness. An abrupt shift in the stopband characteristics (width and centre wavelength) 20 mm from the wafer edge was observed and this was shown to result from the gradual appearance of sidebands in the reflectivity spectra. The FP resonance wavelength was shown to align centrally to the stopband centre (within 5 nm) across the whole wafer.

Furthermore, the PL wavelength was demonstrated to vary by < 1.5 nm across the wafer, with a radial decrease towards the wafer edge - consistent with an increasing QW transition energy. Simple calculations showed that layer thickness variations have only a small impact on the QW transition energy, even for sizeable shifts. Therefore, it was explained that the variation in the PL wavelength is most likely derived from an increase in the bandgap energy in the QW, that is, from a decrease in the indium mole fraction. High uniformity in the PL intensity was shown, consistent with a high QW radiative efficiency across the wafer. Similar for the integrated PL signal and linewidth, which was observed to be on the order of that expected from thermal broadening across the whole wafer.

It was also shown that, when oxidised as a whole wafer in a conduction-based furnace, there can be a significant variation in the oxide aperture for a GaAs substrate wafer. The oxidation extent was shown to vary radially, increasing towards the edge, which is

the result of temperature gradients during the oxidation process. The radial variation was observed to be directly related to the bow of a 6-inch GaAs substrate wafer, which resulted in a lower temperature at the wafer centre. The contribution of the furnace non-uniformity was also described. The effect of wafer bow was removed by considering cleaved samples from different regions of a 6-inch wafer. Oxidising samples taken from the centre and edge of the wafer, the oxidation rate was found to be slower at the wafer edge - the opposite effect from what is observed for a whole wafer. This result indicated that the Al composition and/or layer thickness decreases towards the wafer edge, which was consistent with the findings from the FP and PL variation. Furthermore, this demonstrated that the influence of the wafer bow dominates that of the epi-layer variation.

As expected from the variation of the FP wavelength, the lasing wavelength was also shown to vary radially on the wafer, decreasing towards the edge. By assessing < 8 µm aperture devices at currents close to threshold, confinement effects associated with the oxide aperture and effects due to self-heating were negligible. This resulted in the VCSEL emission wavelength tracking very closely with the measured FP resonance wavelength.

The VCSEL threshold current was shown to vary in conjunction with the variation of the oxide aperture across the wafer. The wafer oxidised in a convection-based furnace produced superior oxidation uniformity compared to a conduction-based furnace, which resulted in an improved threshold current uniformity. Wafer-scale mapping of the oxidation extent allowed the variation in threshold current density to be measured, and assessing large diameter devices reduced the impact of oxide aperture variation on the measured performance. Despite this, a radial variation in threshold current density remained. Measurement of the dependence on temperature (and specifically the temperature corresponding to the threshold current minima) revealed a spatial variation in the detuning of the gain peak and cavity resonance wavelengths - which is present due to the different sensitivities of the FP and PL wavelengths to shifts in the properties of the epi-layers. From the known shift of the gain peak wavelength with temperature, the room temperature gain peak wavelength was calculated. One benefit of the variation of the gain peak detuning means that the threshold current uniformity improves at elevated

temperatures, close to the intended temperature of operation ($\sim 50°C$).

The VCSEL peak optical power was also shown to track with the oxide aperture on the wafer. The optical power was observed to vary significantly on a wafer with poor oxidation uniformity. The variation was greatly reduced with a uniform oxidation. Similar to the threshold current density, the optical power density was calculated from the mapping of the oxidation extent across the wafer, and large devices were assessed to account for residual oxide aperture variation. When this quantity was mapped, the variation over most of the wafer was small but a drop off towards the edge was observed. This was compared to the measured height of the stopband for the same wafer, and found to correlate with an increase in reflectivity. The effects of this were also seen in the measured peak external differential efficiency, which was similarly observed to reduce towards the wafer edge.

In conclusion, the quality and uniformity of generic MOVPE-grown 6-inch GaAs substrate VCSEL wafers has been assessed. A decrease in the In mole fraction in the quantum wells was deduced to occur radially towards the wafer edge. This was found to also coincide with a decrease in the thickness of the epitaxial layers. Variation of the oxide aperture across wafers processed whole was shown to have a significant effect on the uniformity of device performance, particularly the threshold current and output power. Even when the oxide non-uniformity was corrected for, some residual variation in device performance was found to remain, which was attributed to the variation in the properties of the epilayers, specifically, a spatially varying detuning of the gain peak and cavity resonance wavelengths and a variation in the mirror reflectivity.

Chapter 6

VCSELs on Germanium

6.1 Introduction

In Chapter 5, the sizeable wafer bow/warp of AlGaAs-based VCSEL structures grown on 6-inch (150 mm) diameter GaAs substrates was shown to significantly impact the uniformity of on-wafer device performance. As discussed in Chapter 3, this results from the non-negligible strain present in the DBR layers, which originates from the lattice-mismatch of AlAs and GaAs. The bowing issue becomes more significant as the wafer diameter is increased and, as such, the further scale-up of volume VCSEL production to 8-inch diameter substrates looks unlikely to occur on GaAs. As a result of this, work has been done to produce high-quality VCSEL structures on Ge as an alternative growth substrate for future scale-up. There are several reasons as to why Ge is a good candidate for a VCSEL substrate which are briefly summarised here. The lattice constant of Ge lies between that of GaAs and AlAas and is more closely matched to AlAs than that of GaAs, which provides a reduction in strain (roughly 0.08% for Ge compared to 0.14% for GaAs). In addition, Ge has a higher fracture toughness than GaAs so should also benefit from fewer wafer breakages during fabrication. The mechanical robustness combined with the reduced strain is also likely to lead to improvements in material and device

yields. Furthermore, Ge substrates can be produced defect-free (zero etch-pitch density) which will reduce the number of threading dislocations formed during growth which is advantageous for both yield and device reliability. Finally, the thermal conductivity of Ge is $\sim 5\%$ higher than GaAs and, therefore, it may be possible to produce lower thermal resistance VCSELs. There are of course drawbacks, for example, the inability to cleave these structures and the need for a buffer at the interface of the Ge substrate and the epitaxial layers. However, these challenges can be overcome. As an alternative to cleaving, for other photonic components grown on Ge (photodetectors and solar cells), laser/plasma dicing techniques are generally used to produce individual chips. Further, MOVPE-grown transition layers can be employed at the Ge-epi interface to reduce electrical resistance and ensure a clean growth surface free from anti-phase domains [26]. Despite this, for Ge to be considered as a viable alternative to GaAs for VCSEL production, it is necessary to show, at a minimum, parity in the performance of devices grown on each material. This requires the assessment of the electrical, optical, and thermal characteristics of like-for-like VCSELs grown on both GaAs and Ge. So far, the reports on the performance of VCSELs on Ge has not been extensive and work has focussed on the material properties and advantages over large diameters wafers. Here, the techniques of the previous chapter are applied to whole 6-inch wafers of nominally identical epitaxial structures designed for 940 nm emission high-power operation grown on both GaAs and Ge substrates. In section 6.2, the performance of VCSELs grown on Ge is assessed experimentally and qualified against that of VCSELs on GaAs. This includes the series resistance, threshold requirement, spectral properties, efficiency, and thermal performance. In section 6.3, work is reproduced from [91] which focusses on the impact of the substrate on material/device uniformity. Throughout the discussion, the VCSELs grown on GaAs and Ge substrates will be referred to as GaAs VCSELs and Ge VCSELs.

6.2 Comparative Study of GaAs and Ge VCSELs

6.2.1 Series Resistance

The VCSEL series resistance is extracted as the slope of the I-V characteristic between 2.4 and 2.5 V. Plotting this against device aperture in Figure 6.1, it is evident that the resistance of the Ge VCSELs is slightly higher. Considering large apertures to minimise the impact of aperture size dependence, an approximate difference of 10 Ω is found. It should be noted that the Ge substrate is approximately 75 µm thicker than the GaAs substrate. From C-TLM measurements, it was found that the contact resistance on the substrate side of the wafer (n-doped) is significantly lower for AuGe/Ni/Au on Ge than for GaAs. Therefore, it is most likely that the observed difference is derived from the properties of the epitaxial layers, this is considered further in section 6.3.2.1. At a minimum, it can be said that the electrical properties are comparable for GaAs and Ge VCSELs, but future investigations may be dedicated to ascertaining whether the difference observed here is non-negligible and towards understanding its origin.

6.2.2 Threshold Requirement

The dependence of threshold current and threshold current density on oxide aperture is very similar for the GaAs and Ge VCSELs, as can be seen in Figures 6.2 and 6.3. Comparable performance is observed with very similar dependence on oxide aperture for both device types. As the aperture is increased, the threshold current density plateaus at $\sim$ 2 kA/cm^2 with a slightly higher value in the Ge VCSELs (5% increase). This is most likely associated with a difference in optical loss in the different epitaxial structures and unrelated to the growth substrate. This is considered in more detail throughout this chapter. Similarly to the series resistance discussion, it is shown that comparable threshold current densities can be achieved for 940 nm emitting VCSELs with Ge as a drop-in substrate replacement.

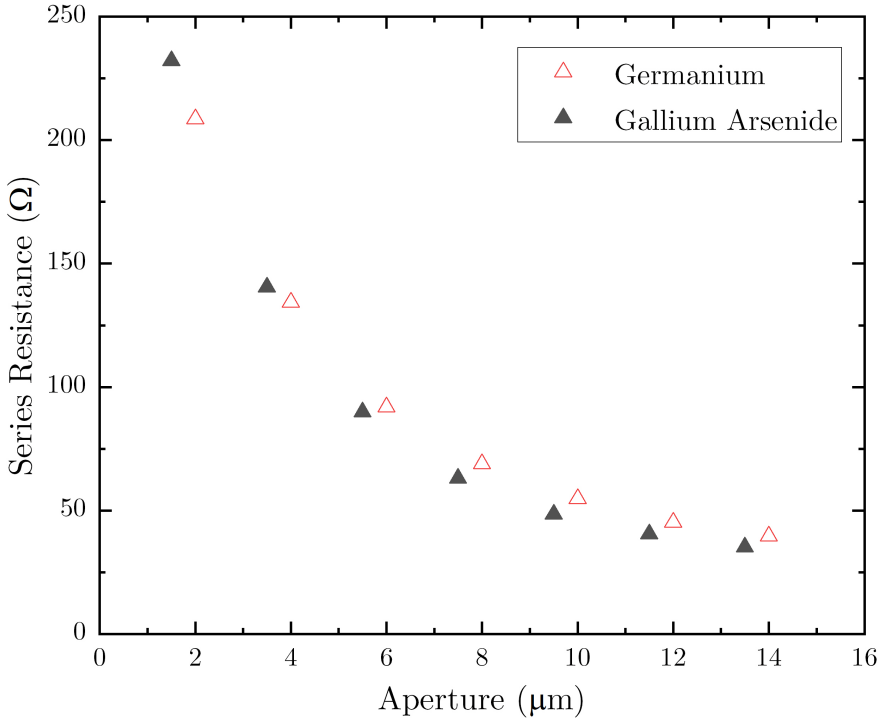

Figure 6.1: Series resistance as a function of oxide aperture diameter for GaAs and Ge VCSELs.

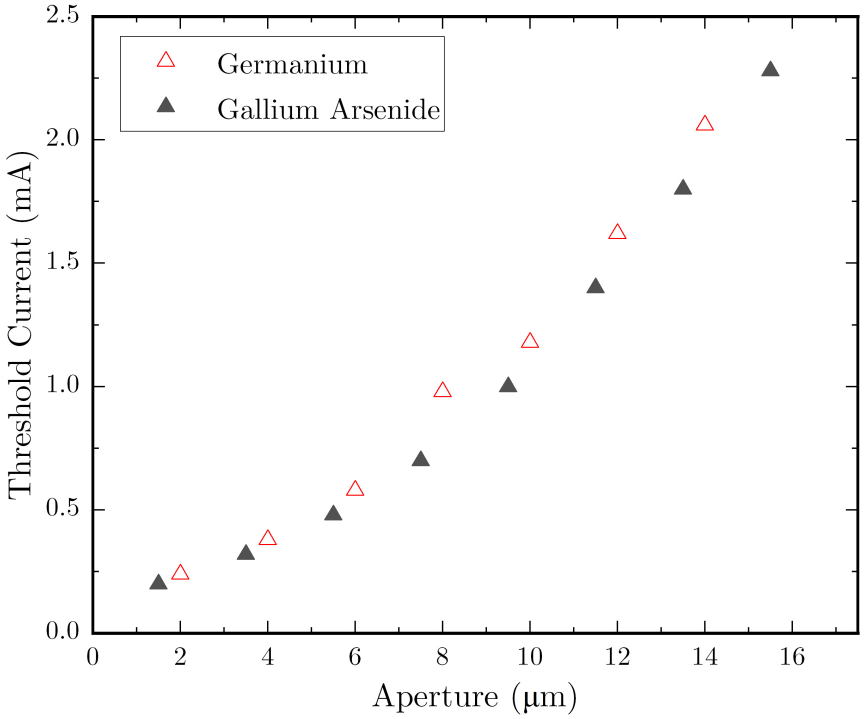

Figure 6.2: Threshold current as a function of oxide aperture diameter for GaAs and Ge VCSELs.

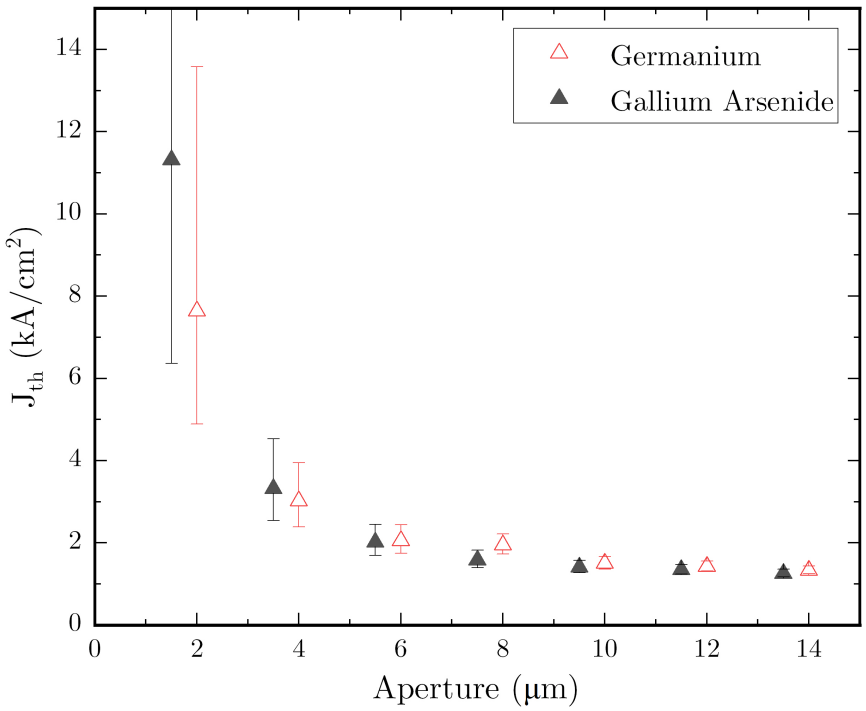

Figure 6.3: Threshold current density as a function of oxide aperture diameter for GaAs and Ge VCSELs. The error bars represent the effect of a 0.5 µm uncertainty in the oxide aperture.

6.2.3 Lasing Wavelength

The room temperature emission wavelength close to threshold closely matches the FP cavity resonance wavelength observed in reflectometry measurements and there is very little difference (< 0.5 nm) between the GaAs and Ge VCSELs for similar aperture sizes. Emission spectra for a 5.5 µm GaAs and 6.0 µm Ge VCSEL are shown in Figure 6.4. The wavelength of the fundamental mode is extracted from the long-wavelength edge of the spectrum. This has an error of $\pm$ 0.3 nm related to the resolution of the spectrometer. These wavelengths are plotted against bias current in Figure 6.5. The quadratic dependence on bias current reveals that the dominant source of internal temperature increase is Joule-heating [124], [125]. The rate of increase in wavelength is highest for the GaAs VCSELs at both 30 and 70 °C. A greater rate of self-heating is to be expected given the slightly smaller oxide aperture (0.5 µm) and mesa diameter (2 µm), although, also seen in Figure 6.5, the difference in the rate of wavelength shift remains when larger device apertures (5.5 and 6 µm) are considered (lower curves).

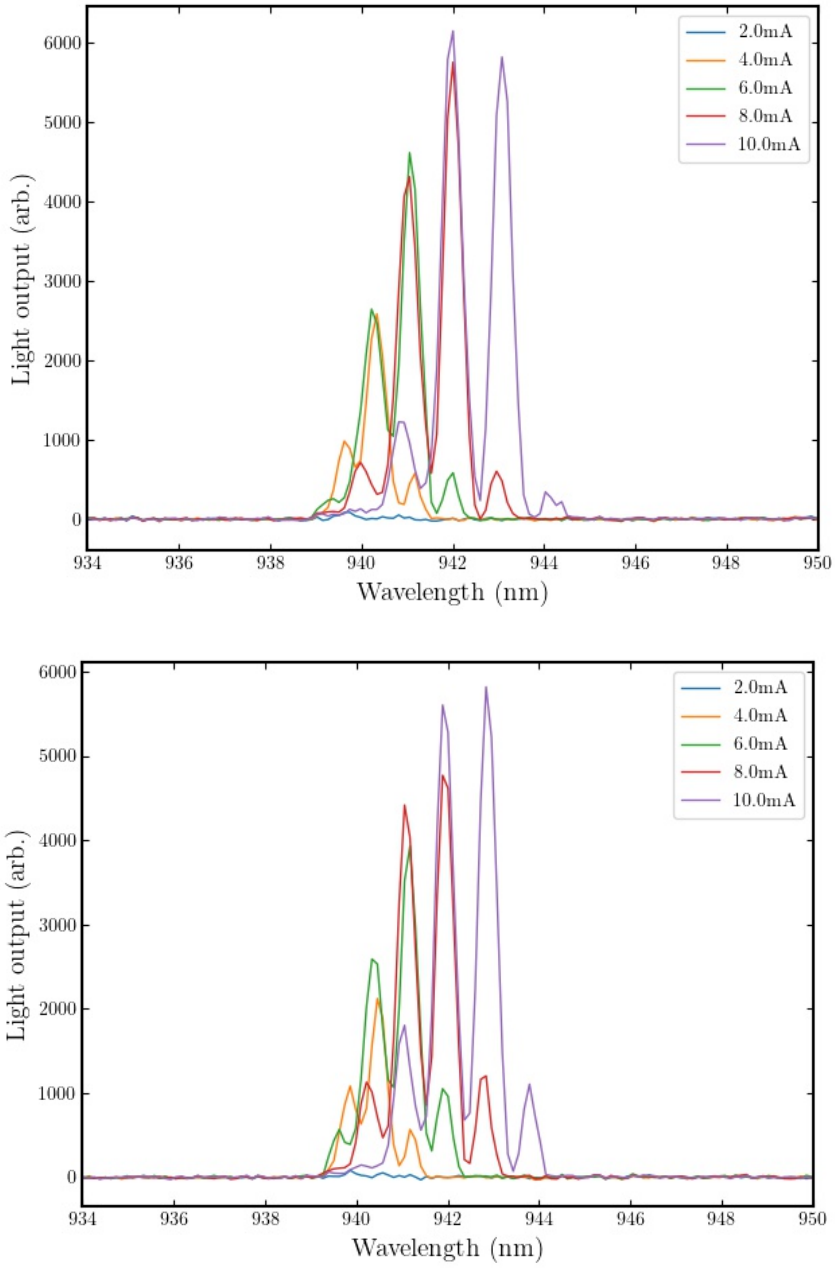

Figure 6.4: Emission spectra measured between 2 and 10 mA for a 5.5 µm aperture GaAs (top) and 6.0 µm Ge (bottom) VCSEL.

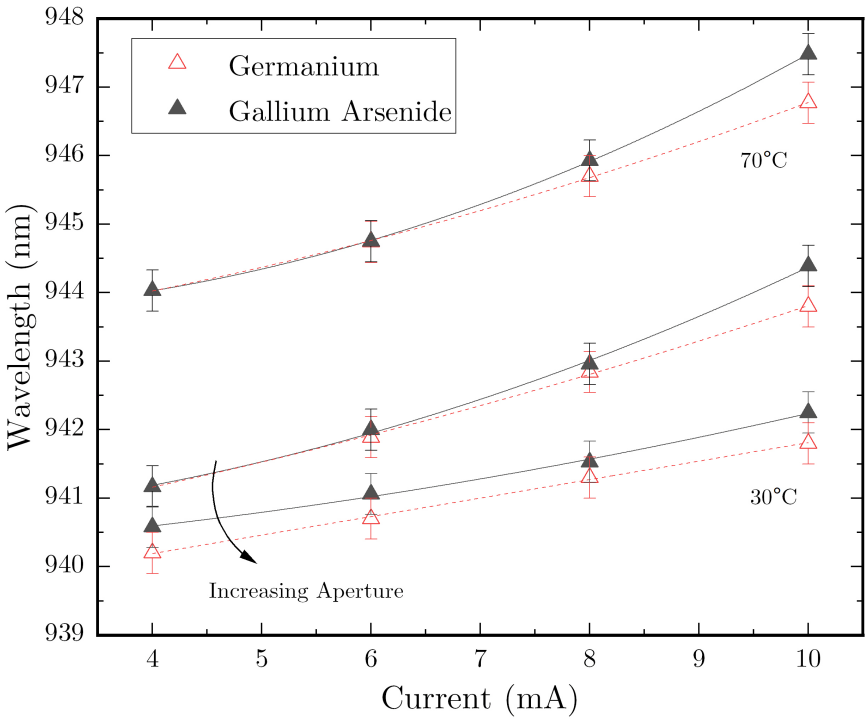

Figure 6.5: Wavelength shift with injection current at 30 and 70 °C for GaAs and Ge VCSELs. A quadratic dependence on current is observed for the 3.5 µm GaAs and 4.0 µm Ge devices. The dependence is approximately linear for when considering 4.5 and 5.0 µm apertures (lower curves).

Additionally, the shift in wavelength with ambient temperature, shown in Figure 6.6, is found to be ~ 0.07 nm/°C for both substrate types which is within the 0.01 nm/°C error in the literature value expected from the refractive index shift of the AlGaAs-based cavity.

6.2.4 Self-Heating

6.2.4.1 Thermal Resistance

Extending the treatment of the previous section, the self-heating can be quantified by measuring the wavelength shift as a function of the dissipated power, as introduced in section 2.6.2.3. The dissipated power is taken as the total electrical power (IV) minus the optical power. Fig. 6.7 shows the resulting plot of wavelength as a function of dissipated power for 34 µm mesa devices, corresponding to a 6.5 µm GaAs VCSEL and 5 µm

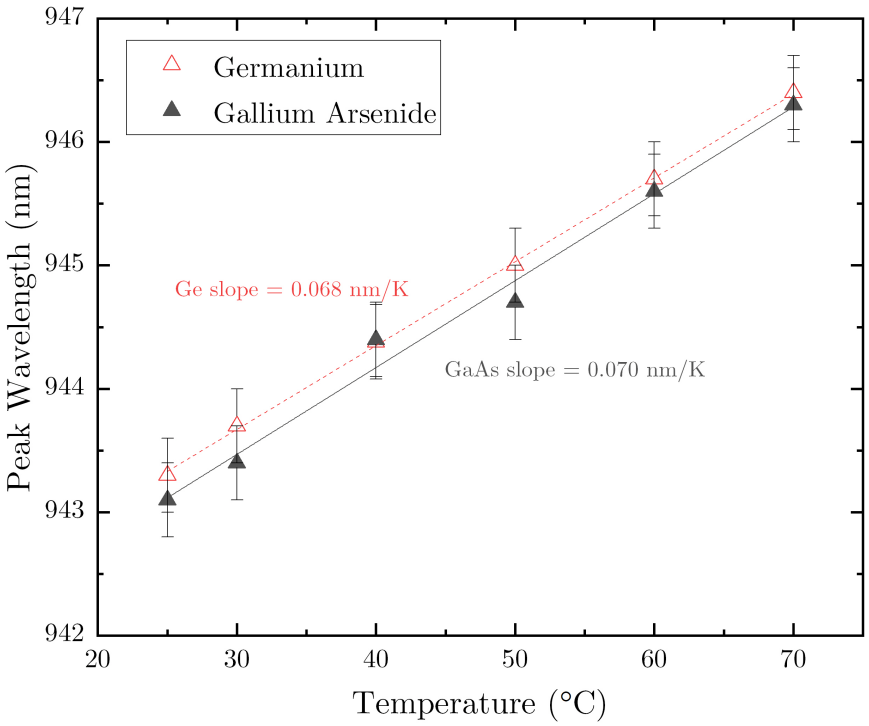

Figure 6.6: Wavelength as a function of ambient temperature. The shift with temperature for both the GaAs and Ge device is measured within error of the expected ~ 0.07 nm/°C value from the literature.

Ge VCSEL. The method used to calculate the thermal resistance is that of [75]. The dependence of R_{Th} on temperature is accounted for by measurement of dR_{Th}/dT. The ratio of the slope of these curves to the slope of the wavelength shift with temperature at zero dissipated power gives the device thermal resistance. Thermal resistances are calculated as $R_{Th,GaAs} = 1.54 \pm 0.38$ °C/mW and $R_{Th,Ge} = 1.49 \pm 0.32$ °C/mW. The large error in the calculated values stems from the lines of worst fit of the curves in Figure 6.7, accounting for the 0.3 nm resolution of the spectrometer. Therefore, it can be said that despite the 1.5 µm smaller oxide aperture and 75 µm thicker substrate, the device thermal resistances are within error. Hence, parity in the thermal performance of VCSELs on GaAs and Ge is shown, with some promise that thermal performance of Ge VCSELs can be enhanced relative to GaAs.

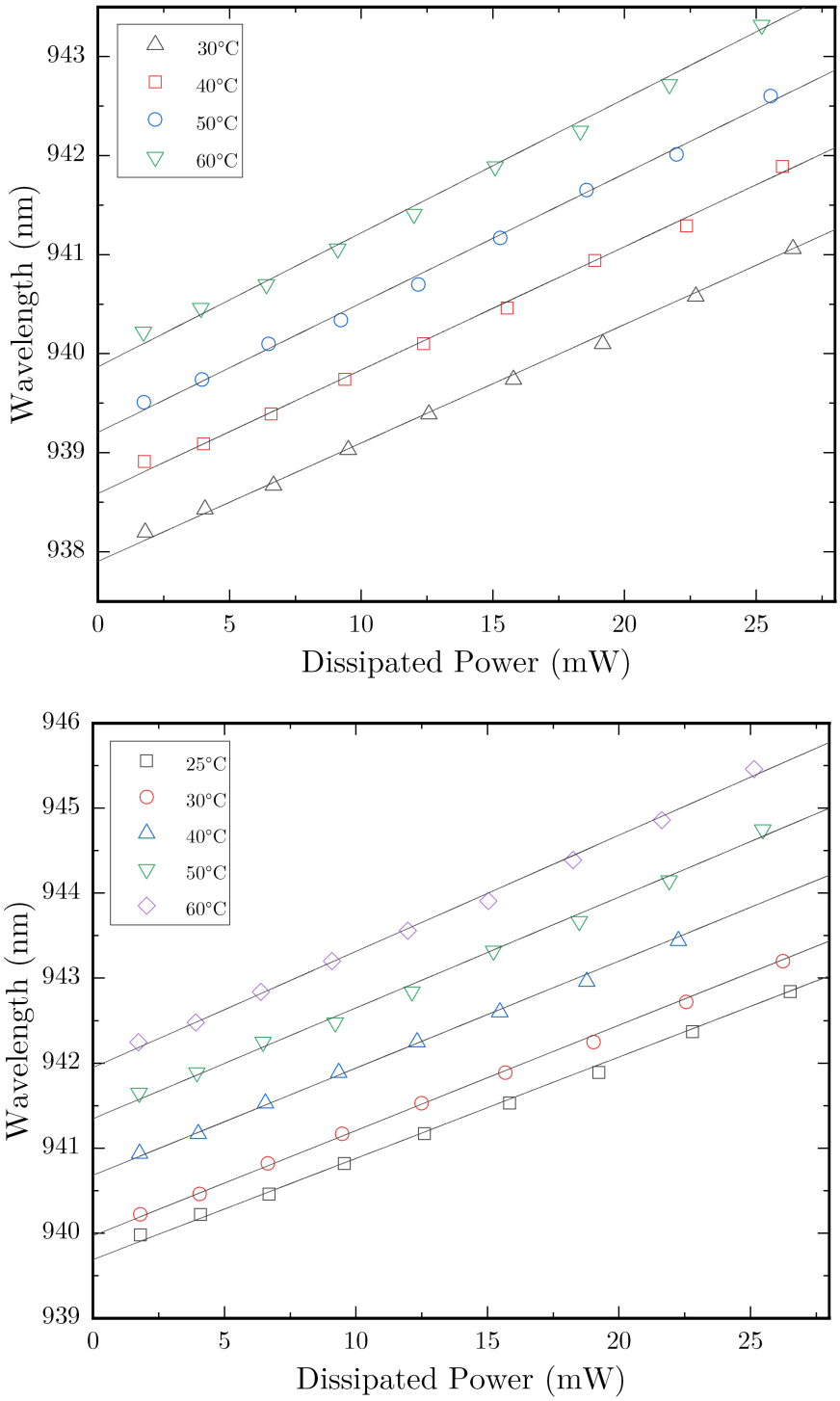

Figure 6.7: Peak wavelength as a function of dissipated power for GaAs (top) and Ge (bottom) VCSELs. The oxide apertures (mesa) diameters are 6.5 (34) and 5 (34) µm for the GaAs and Ge devices, respectively.

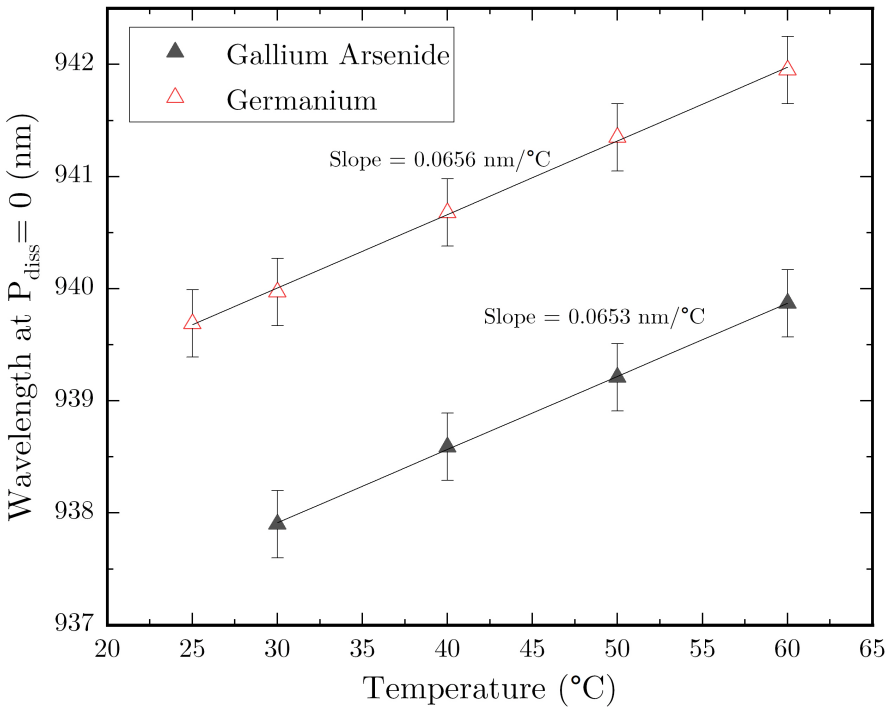

Figure 6.8: Wavelength as a function of temperature for a GaAs and Ge VCSEL. These wavelengths values are found from the intercept of the curves in Figure 6.7. The oxide aperture (mesa) diameters are 6.5 (34) and 5 (34) µm for the GaAs and Ge devices, respectively.

6.2.4.2 Thermal Rollover

The current at which thermal rollover occurs can be used as another indication of the thermal performance of the devices. Figure 6.9 shows the optical power as a function of bias current for large aperture GaAs and Ge devices and the rollover current is similar in both cases with a difference of 1.2 mA. The difference in oxide aperture (13.5 µm GaAs vs 14.0 µm Ge) contributes to the difference in the onset of thermal rollover, and Figure 6.10 shows the dependence on both ambient temperature and oxide aperture diameter. Thermal rollover occurs at a lower current as the ambient temperature is increased due to a reduction in internal quantum efficiency and increases in carrier leakage, carrier thermalisation, spontaneous recombination, and internal optical loss [66]. The difference in rollover current for the ∼14 µm GaAs and Ge devices increases by just 0.2 mA in the range 25 to 70 °C demonstrating no difference in the rollover-producing mechanisms. From Figure 6.10 (right), it is evident that the disparity is explained by the difference in

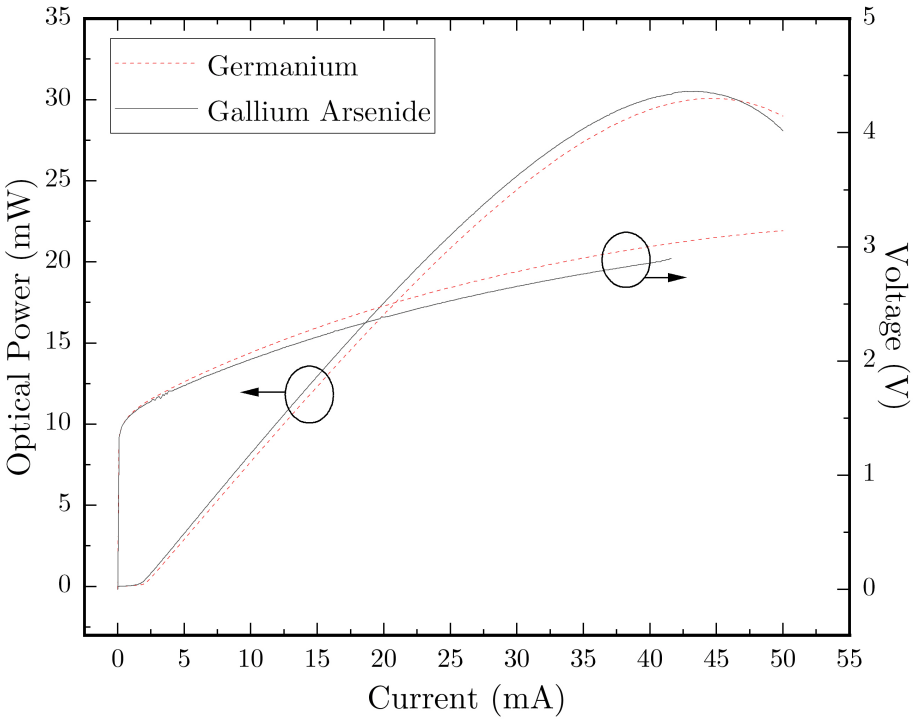

Figure 6.9: Light-current-voltage characteristics up to thermal rollover for a 13.5 µm and 14.0 µm aperture GaAs and Ge VCSEL, respectively.

oxide aperture, and from the slopes of the plot, the expected shift in rollover current due to a 0.5 µm aperture shift in oxide aperture is calculated to be $\sim$ 1.5 mA, which agrees well with observation. This further supports the demonstration of parity in the thermal properties of Ge VCSELs described in the previous section.

6.2.5 Optical Power and Efficiency

The maximum output power of a VCSEL is determined by how efficiently the input electrical power is converted into optical power and the degree of self-heating. For small aperture devices, the high thermal resistance results in the early onset of the thermal rollover and, as such, the peak optical power is low. As the device aperture is increased, the onset of thermal rollover moves to higher current and the peak optical power increases. Figure 6.11 shows a linear dependence between peak optical power and device aperture at 30 °C. Both the GaAs and Ge VCSELs follow the same dependence on aperture with a constant offset of $\sim$ 0.5 mW which is likely related to epi-layer variation, that is, a

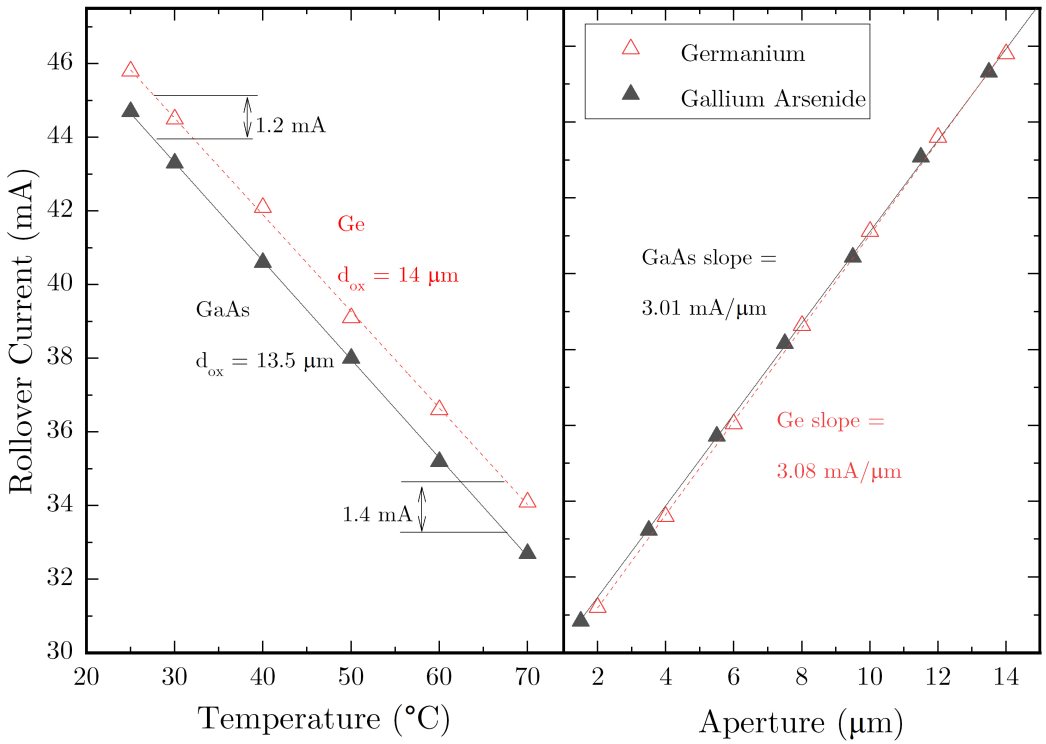

Figure 6.10: Thermal rollover current as a function of temperature (left) and aperture (right) for a 13.5 µm and 14.0 µm aperture GaAs and Ge VCSEL, respectively. The offset seen in the rollover current is explained by the 0.5 µm aperture difference.

difference in mirror or absorption loss.

The dependence of the peak power on aperture becomes sublinear as the ambient temperature is increased to 70 °C. In Figure 6.12, it can be seen that this sublinear relationship arises from the difference in sensitivity to temperature for small and large aperture devices. For the small aperture devices (3.5 and 4.0 µm), the internal temperature is dominated by the effects of self-heating, whereas the larger devices (13.5 and 14.0 µm) are comparatively more sensitive to changes in ambient temperature due to their low thermal resistance.

Similar to the dependence on oxide aperture, it is found that the rate of decrease of peak optical power with temperature is equivalent for the GaAs and Ge VCSELs, and the offset is likely derived from epi-layer variation. Again, here parity in the optical output power characteristics between GaAs and Ge VCSELs has been demonstrated. Further (destructive) characterisation would be needed to fully isolate the effects of epitaxial layer variation. The dependence of the peak external differential efficiency, $\eta_{\mathrm{d,peak}}$, on oxide

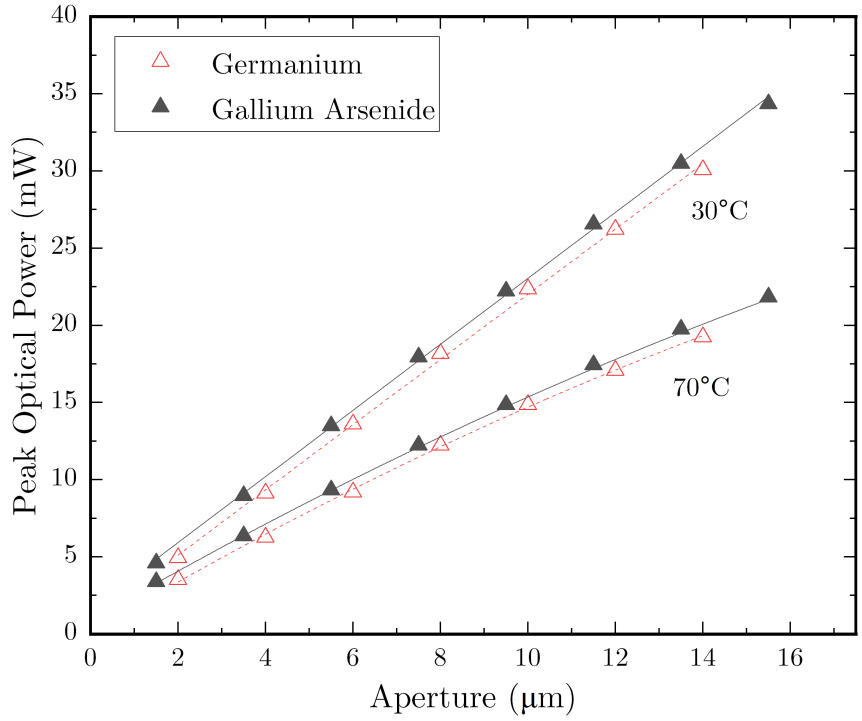

Figure 6.11: Dependence of the peak optical power on oxide aperture for GaAs and Ge VCSELs. The offset in optical power for a given aperture is constant and likely derived from differences in differential efficiency unrelated to the growth substrate.

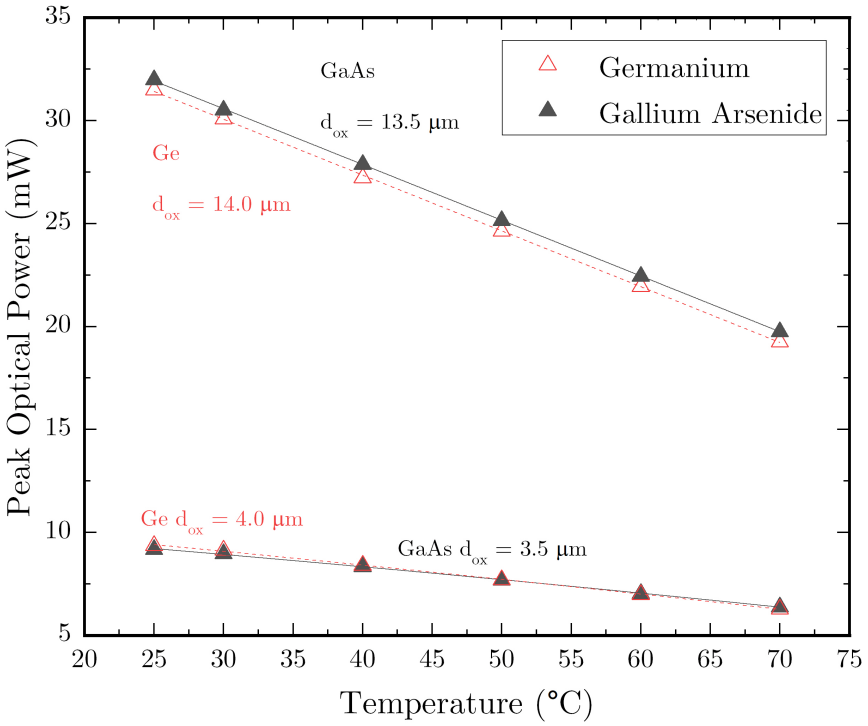

Figure 6.12: Dependence of the peak optical power on ambient temperature. The upper plots represent 13.5 and 14.0 μm aperture GaAs and Ge devices, respectively. The lower plots are for 3.5 and 4.0 μm apertures.

aperture for ~ 8 µm GaAs and Ge VCSELs is shown in Figure 6.13. From Equation 2.17, the external differential efficiency is dependent on the internal quantum efficiency, η_i, the internal optical loss, and the mirror loss. Assuming η_i is constant for both device types, the higher $\eta_{\mathrm{d,peak}}$ observed for the GaAs VCSELs suggests a variation in optical loss between the samples. The difference is $\sim 5\%$, which is comparable to the increased Ge threshold current density seen in Figure 6.3. Therefore, it is likely that this difference is the result of variation of the internal optical loss (reducing $\mathrm{J_{th}}$ and increasing η_{d}).

The power conversion efficiency is dependent on both the differential efficiency and the series resistance. The dependence on oxide aperture for GaAs and Ge is shown in Figure 6.14, with values measured to range between 35 to 42% for all device sizes. $\eta_{\mathrm{p,peak}}$ is found to be consistently higher throughout the temperature range for the GaAs VCSELs. In both cases there is a decrease in η_{p} for small oxide apertures, which corresponds to an increase in series resistance, as well as increased loss due to the confinement of the aperture as the device size is reduced. A decrease for larger apertures is also observed which is typical for VCSELs and relates to the non-uniform current distribution [6]. Additionally, a decrease is observed at elevated temperature which is attributed to thermally-activated carrier leakage. Given that the GaAs VCSELs have a lower resistance and higher $\eta_{\mathrm{d,peak}}$, the increased conversion efficiency is expected.

For both the differential and conversion efficiencies, there is an $\sim 8\%$ decrease in the peak values of the Ge substrate devices. Further work will be devoted to understanding whether this difference is statistically significant relative to expected epitaxial variation. Destructive characterisation could therefore be employed to quantify differences in the properties of the epi-layers and assess how this contributes to the observed disparity.

6.2.5.1 Summary

The key findings from the experimental comparison of GaAs and Ge VCSELs are summarised here. In general, parity in the output characteristics of 940 nm VCSELs grown on GaAs and Ge is observed. There is a difference of 5% in the threshold current density for

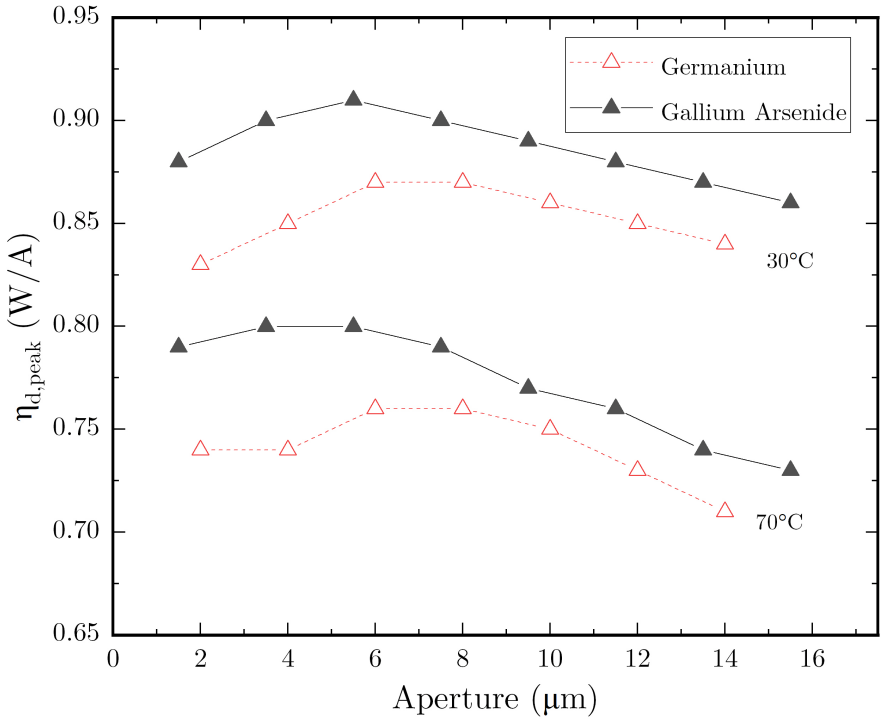

Figure 6.13: Dependence of the peak external differential efficiency on oxide aperture for ∼ 8 µm GaAs and Ge VCSELs at 30 and 70 °C.

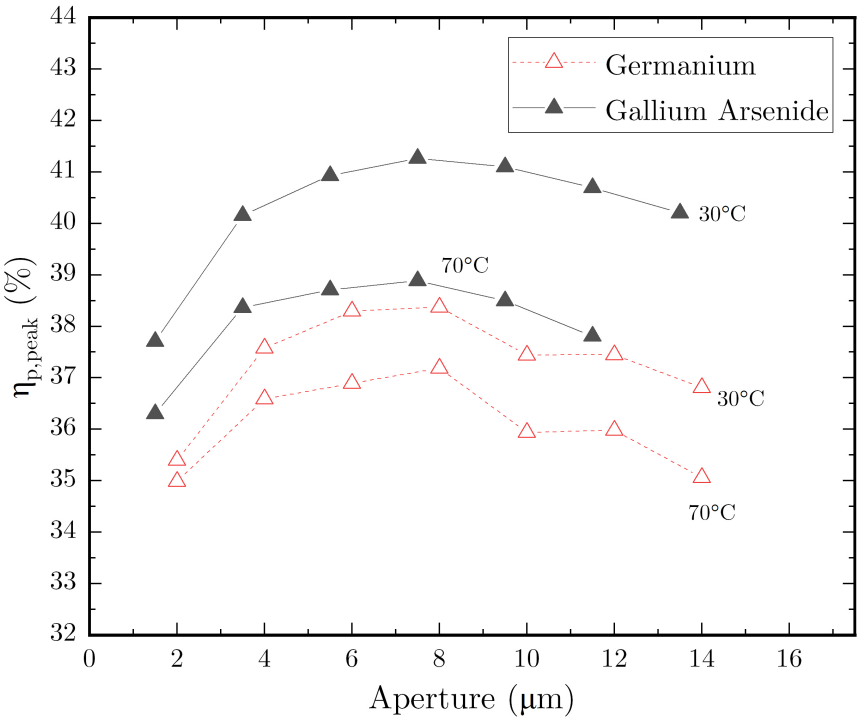

Figure 6.14: Dependence of the peak power conversion efficiency on oxide aperture for ∼ 8 µm GaAs and Ge VCSELs at 30 and 70 °C.

Table 6.1: Comparison of key figures of merit for ~ 10 µm aperture GaAs and Ge VCSELs. The quantities included are series resistance (R), threshold current (I_{th}), peak optical power (P_{max}), thermal rollover current ($I_{rollover}$), peak external differential efficiency ($\eta_{d,peak}$), and peak power conversion efficiency ($\eta_{p,peak}$)

Substrate	Aperture (µm)	R (Ω)	I_{th} (mA)	P_{max} (mW)	$I_{rollover}$ (mA)	$\eta_{d,peak}$ (W/A)	$\eta_{p,peak}$ (%)
GaAs	9.5	45.7	0.96	22.2	31.1	0.89	41.6
Ge	10.0	54.6	1.14	22.4	32.8	0.86	38.5

large aperture devices in the favour of GaAs. The emission spectra and lasing wavelengths are found to be equivalent. The electrical resistance of the Ge VCSELs is slightly higher than that of the GaAs VCSELs, however, this may be derived from properties of epitaxial layers. The shift in emission wavelength with temperature and current is comparable for both device types when accounting for oxide aperture differences. From measurement of the wavelength shift as a function of the dissipated power, the thermal resistance of large diameter devices is found to be within error, despite a smaller oxide aperture and thicker substrate for the Ge VCSELs. This result is attributed to the higher thermal conductivity of Ge, from which it is predicted that an enhancement in the thermal performance can be achieved by growth on Ge substrates. The differences in the observed thermal rollover points are associated with a variation in oxide aperture. The peak external differential efficiency is lower in the Ge VCSELs, likely driven by a difference in the internal optical loss in the different samples. This reduced differential efficiency, as well as the increases electrical resistance, drives a lower power conversion efficiency in the Ge VCSELs. A comparison of key figures of merit for GaAs and Ge VCSELs is given in Table 6.1.

6.3 Wafer-Scale Analysis

6.3.1 Wafer Bow and Oxidation Uniformity

One of the main advantages for growing VCSELs on Ge substrates is the reduction of wafer bow/warp. Figure 6.15 shows the vertical height variation across a 6-inch Ge and

GaAs VCSEL wafer already presented in section 3.2.4. The centre-to-edge height difference measured for a GaAs wafer is larger by a factor of 5 compared to the Ge case. The wafer bow for GaAs substrate VCSELs has a sizeable impact on wafer uniformity, which is measured and presented here. One of the key processes for the production of VCSELs is the definition of the oxide aperture. From section 3.3.3, small temperature variations during the selective oxidation process can result in a significant difference in oxidation rates and, therefore in this case, oxidation extent across the wafer. As demonstrated throughout this thesis, key operating characteristics of VCSELs are highly dependent on the lateral dimensions of the active volume, hence a deviation from the desired oxidation length can result in a significant variation in device performance. The impact of oxidation rate non-uniformity of GaAs and Ge substrate VCSEL wafers was reported in [91]. For conduction-based oxidation furnaces, which rely on thermal contact with a heated chuck for temperature control, the bow of a GaAs substrate wafer leads to an appreciable difference in temperature between the centre and edge of a 6-inch wafer, as presented in section 5.3. The height variation for a 6-inch GaAs and Ge substrate wafer is reproduced in Figure 6.15 and the resulting oxidation extent variation for wafers oxidised in a conduction-based furnace is shown in Figure 6.16. In Chapter 5, the GaAs wafer non-uniformity was shown to drive the variation in device performance for wafers oxidised in a conduction-based furnace. In contrast, improved uniformity for a Ge wafer is observed. This is a result of the uniformity of the Ge oxidation, seen in Figure 6.16. Further, the oxidation extent is found to decrease towards the wafer edge. The impact on the uniformity of threshold current and optical power for 38 µm mesa devices is shown in Figures 6.17 and 6.18. There is an increase in both threshold current and optical power at the regions with shorter oxidation extents (hence larger apertures) close to the wafer edge. This can be seen more clearly in the line profile plot in Figure 6.19. It should be noted, though, that excellent oxidation uniformity is achieved with a convection based furnace both for Ge and GaAs.

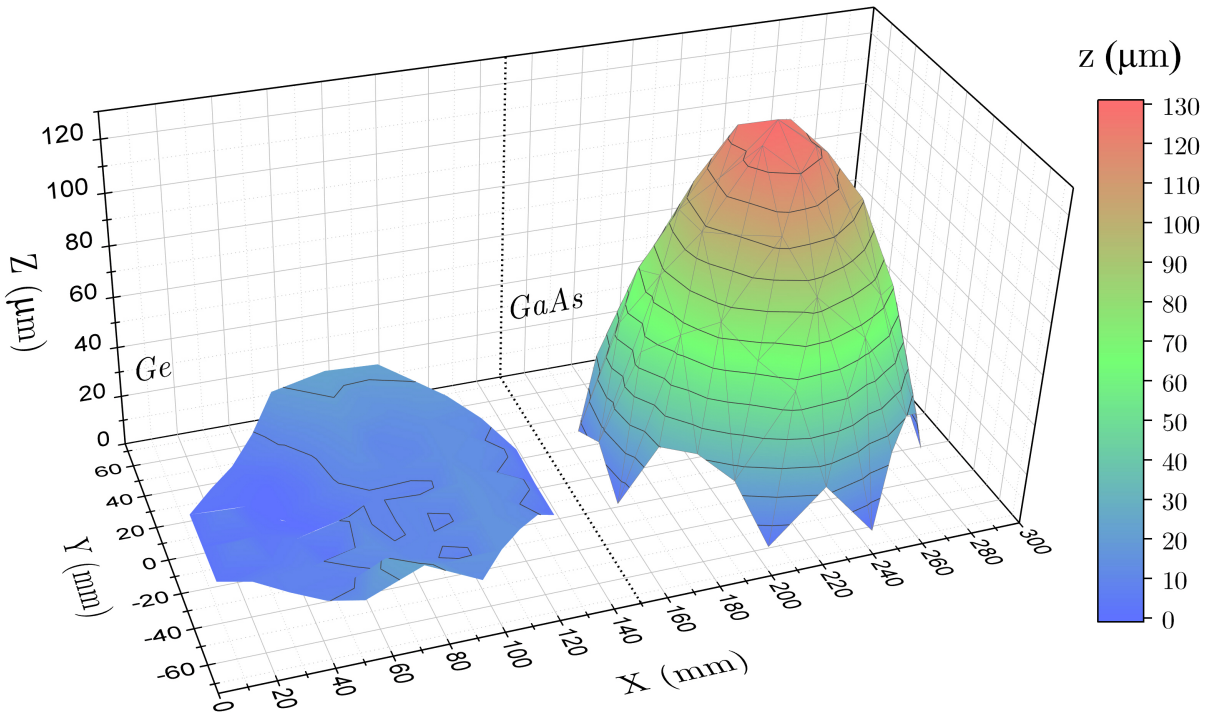

Figure 6.15: Height variation of a 6-inch Ge and GaAs substrate VCSEL wafer. The centre-to-edge difference is ~ 20 µm and 130 µm for the Ge and GaAs wafer, respectively. Reproduced from [91].

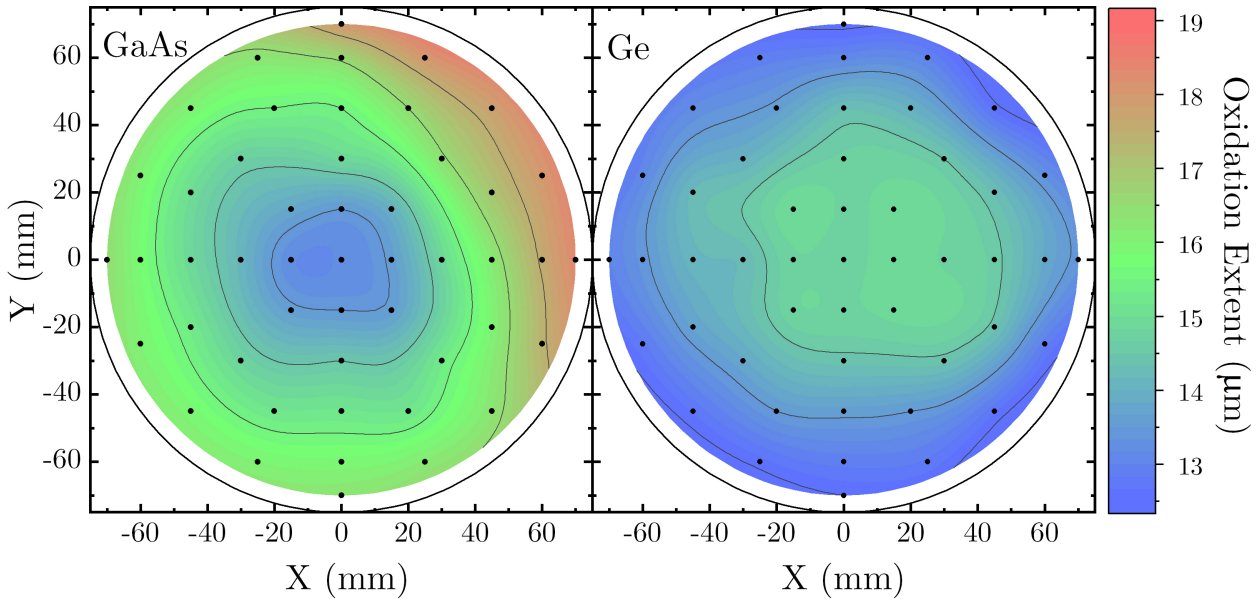

Figure 6.16: Oxidation length variation on a 6-inch GaAs (left) and Ge (right) substrate wafer. The uniformity is improved by a factor of 2 for the Ge wafer due to the lack of bow.

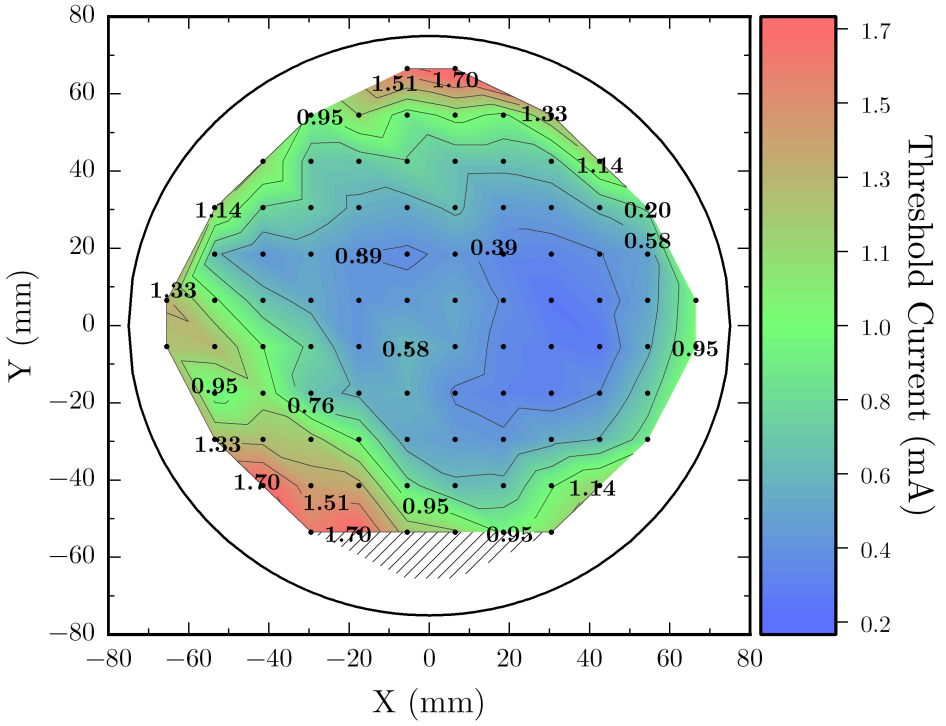

Figure 6.17: Wafer-scale variation of threshold current for 38 µm mesa diameter VCSEL devices across a 6-inch Ge wafer oxidised in a conduction-based furnace.

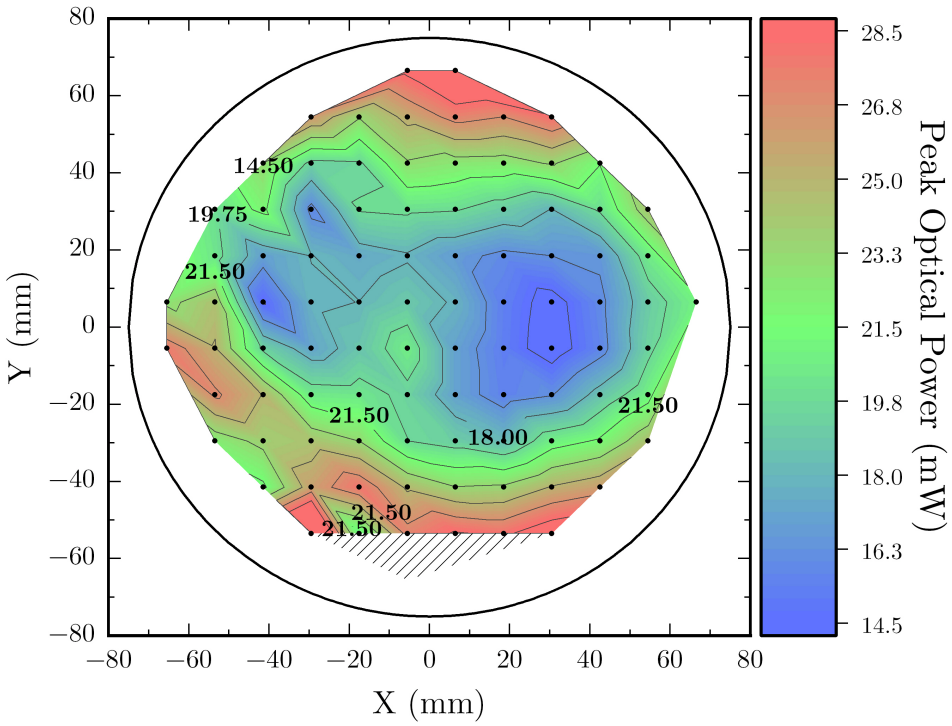

Figure 6.18: Wafer-scale variation of peak optical power for 38 µm mesa diameter VCSEL devices across a 6-inch Ge wafer oxidised in a conduction-based furnace.

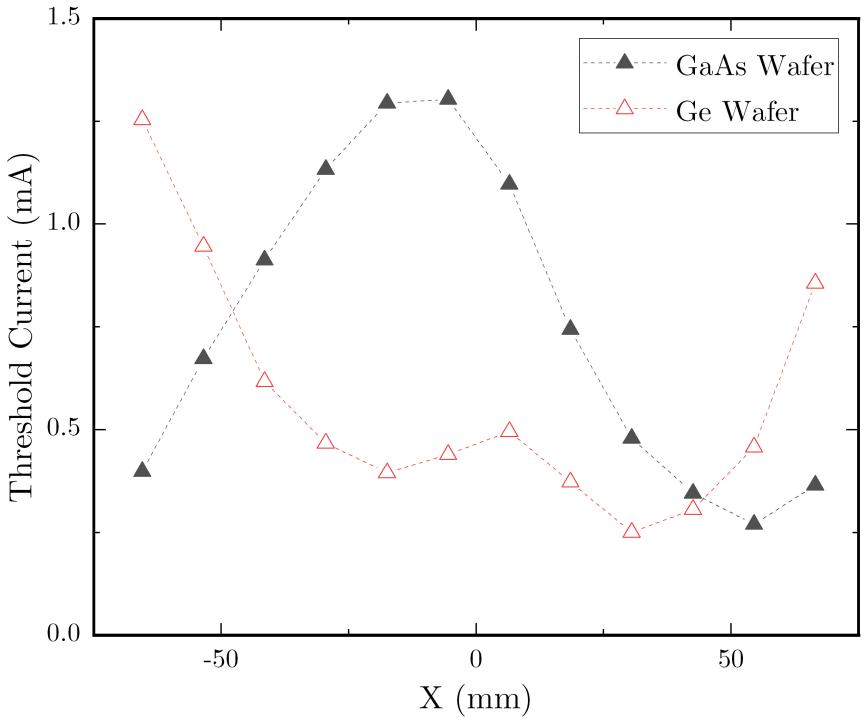

Figure 6.19: Threshold current variation along a horizontal line profile for 38 µm mesa VCSELs from a 6-inch GaAs and Ge wafer. Both wafers are oxidised in a conduction-based furnace.

6.3.2 Properties of the Epitaxial Layers

6.3.2.1 Sheet Resistance

From C-TLM measurements of the emission-side metallisation (as discussed in section 5.2.3 for a GaAs substrate wafer), a radial variation in the sheet resistance is observed. Again, this variation indicates a change in conductivity of the p+ doped GaAs cap of the top DBR. The centre-to-edge difference measured for the Ge wafer is twice as large as that of the GaAs wafer. This reveals a spatial variation in the doping concentration. In Figure 6.20, it can be seen that the centre of the Ge wafer has a higher sheet resistance, associated with a lower doping concentration in the GaAs cap. This likely contributes to the higher electrical resistance of the Ge VCSELs presented in section 6.2.1. The higher R_{sheet} at the wafer centre indicates a possible radial increase in temperature during growth across the Ge wafer, resulting in an increase in the acceptor impurity concentration towards the edge. With growth on Ge there is negligible bowing, and so it is more likely that the

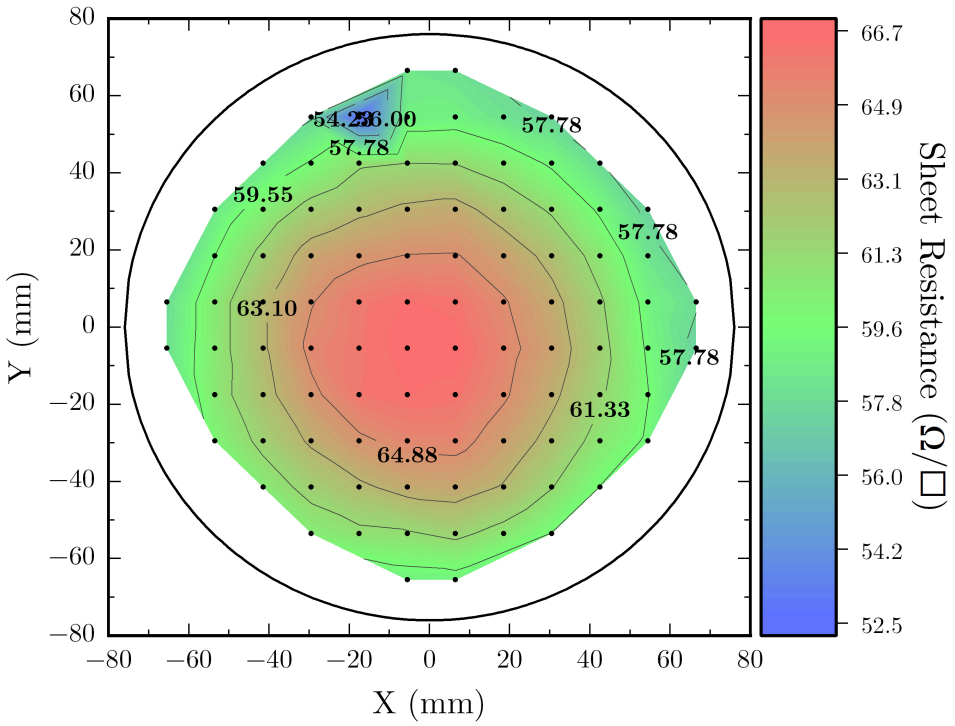

Figure 6.20: Wafer-scale variation of the sheet resistance for a Ge substrate wafer, measured by C-TLM. The radial decrease indicates a spatial variation of the doping concentration in the p+ GaAs cap layer.

temperature uniformity is improved relative to GaAs. Given that Ge is used as a drop-in replacement for GaAs in this study, it is possible that the spatial variation is simply due to the growth recipe being optimised for a bowed GaAs wafer.

6.3.2.2 FP Cavity Resonance Wavelength

Figure 6.21 shows the variation of the FP cavity resonance wavelength extracted from reflectometry measurements for a 6-inch GaAs and Ge substrate wafer. Despite the difference in wafer bow, the same radial decrease is observed for both wafers. This suggests that the origins of the radial variation which is generally seen in MOVPE growth of 6-inch VCSEL wafers does not result from the wafer curvature as has been suggested elsewhere. This gives weight to the argument that the the variation is driven by the non-linear gas-flow rate in the reactor and not temperature.

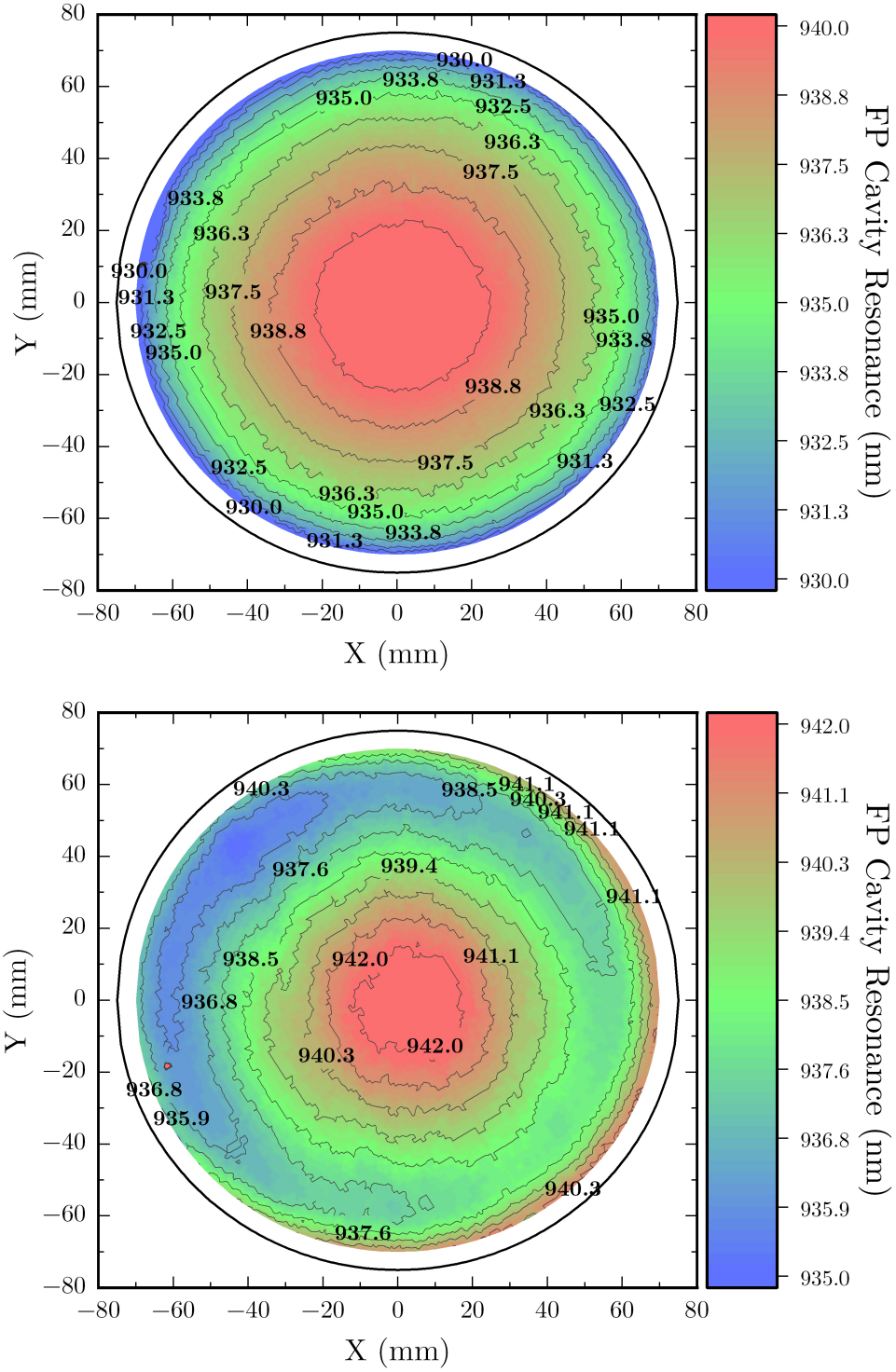

Figure 6.21: FP cavity resonance wavelength of GaAs (top) and Ge (bottom) wafers extracted from reflectometry measurements. A radial variation is observed in both cases despite the lack of bow for the Ge wafer.

6.3.2.3 Photoluminescence - Cavity Resonance Detuning

From Chapter 5, the detuning of the gain peak and cavity resonance wavelengths is known to vary spatially on the wafer. Although the PL peak is not directly representative of the gain peak wavelength, the gain peak detuning can be assessed by considering the spatial variation of the FP cavity resonance and the PL wavelengths. This is shown in Figure 6.22 (top) for the GaAs case. The QWs are grown such that the PL wavelength is shorter than the cavity resonance wavelength across the whole wafer. Clearly, though, the difference in PL and FP wavelengths decreases towards the wafer edge. This is due to the radial decrease in the thickness of the cavity layers. The same radial trend in the detuning is observed for the Ge substrate wafer as is shown in Figure 6.22 (bottom), and this is expected given the equivalent variation of the cavity resonance wavelength (Figure 6.21). The magnitude of the detuning is slightly lower for the Ge wafer ($\sim$ 8 nm vs $\sim$ 10 nm) which is the result of the sharper drop in FP wavelength close to the edge of the GaAs wafer. In both cases, therefore, the detuning of the FP and PL wavelength (and by extension the gain peak wavelength) is found to be greatest at the wafer centre and decreasing towards the edge. The VCSEL threshold current density as a function of temperature is measured on-wafer and a comparison of two locations (labelled A and B in the wafer maps of Figures 6.22) is shown in Figure 6.23. For the regions examined, the PL-FP detuning is -18.6 and -16.0 nm for the GaAs wafer and -18.4 and -16.2 nm for the Ge wafer. The GaAs and Ge VCSEL oxide apertures are 9.5 and 10.0 $\pm$ 0.5 µm, respectively. Lower threshold current densities are found at the wafer edge and T_{min} is also observed to decrease. The decrease in T_{min} is expected from the analysis of the PL-FP detuning where the wavelength difference was seen to drop towards the wafer edge. This means that the temperature-induced shift in the gain peak wavelength required to align to the cavity resonance is reduced, hence occurring at a lower temperature. The difference in T_{min} at the two locations is measured as 7 and 6 °C for the GaAs and Ge wafers, respectively, which, from section 2.3.2, corresponds to a gain peak shift of 2.1 and 1.8 nm. These calculated gain peak shifts are close to that expected from the difference

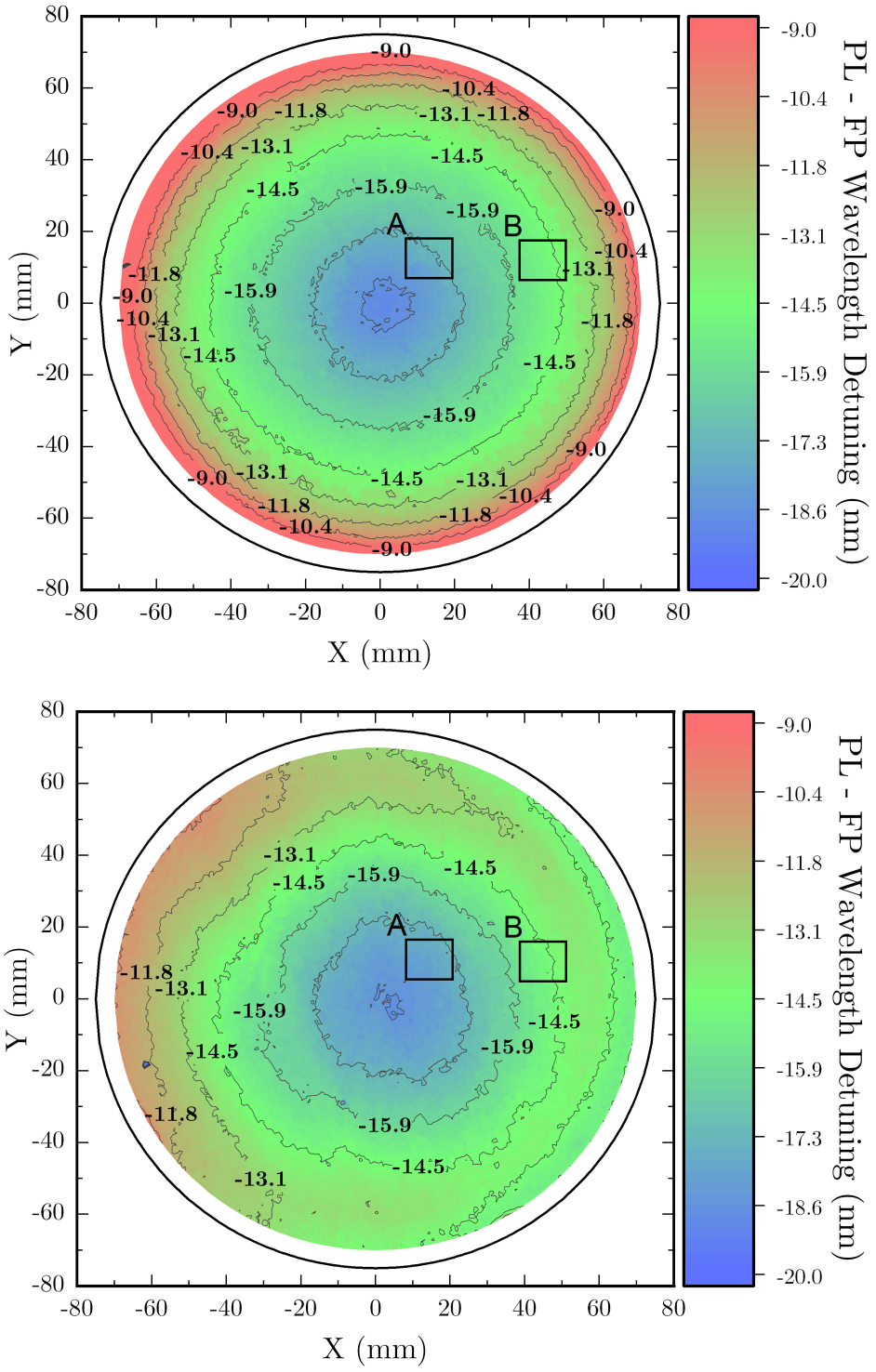

Figure 6.22: Detuning of the photoluminescence peak and FP cavity resonance wavelength across a 6-inch GaAs (top) and Ge (bottom) wafer.

in PL-FP detuning at each location on the wafers, and this, therefore, reveals that the room temperature QW transition wavelength is $\sim$ 14 – 16 nm shorter than the room temperature spectral peak of the gain for both wafers. This value can be quickly checked against simulations of the epitaxial design to assess the quality of growth. As described in Chapter 5, this spatial dependence of the gain peak detuning works to improve the threshold current uniformity at elevated temperatures, closer to the intended operation temperature, and this is the casse for both the GaAs and Ge wafers.

As in Chapter 5 for the GaAs wafer, the minimum achievable threshold current, α, is observed to be higher at the wafer centre than at the edge. This was shown to be correlated with the change in mirror reflectivity (from the stopband height). Similarly, then, it would be expected that α should vary less on the Ge wafer given the uniformity of the stopband height in most regions. In section 6.3.2.3, between regions A and B on the wafer, the minimum threshold current density was observed to decrease by $\sim$0.2 and 0.1 kA/cm^2 for the GaAs and Ge wafer, respectively. Between these locations, the stopband height is found to increase by $\sim$3% for the GaAs wafer and to remain approximately constant for the Ge wafer. This suggests that a change in the optical absorption loss drives the observed variation in $J_{th,min}$ for the Ge wafer, and also likely has a sizeable effect for the GaAs wafer.

6.3.2.4 Stopband Height

As discussed in Chapter 5, mapping of the stopband height can be used to assess the variation of the DBR reflectivity across a wafer. In Figure 6.24 the wafer-scale variation is shown to differ for the GaAs and Ge wafers, with a more uniform distribution on the Ge wafer. For the GaAs wafer there is sharp increase in reflectivity observed towards the edge. The isolated low-stopband-height pocket at the region labelled C on the Ge wafer is likely a measurement issue and not representative of the DBR reflectivity. These pockets were present on all wafers from this particular growth run which were measured together, and in later runs of different epitaxial structures measured with the same tool.

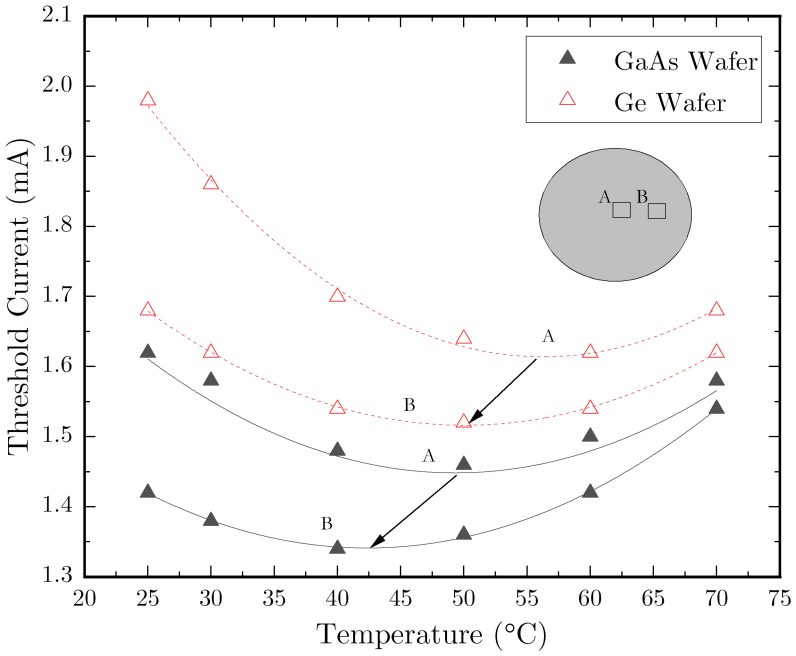

Figure 6.23: Threshold current of ~ 10 µm aperture VCSELs as a function of temperature, measured at two locations on a 6-inch GaAs and Ge wafer. In both cases, there is a decrease of T_{min} towards the edge, indicating a reduced detuning of the gain peak and cavity resonance.

The centre-to-edge difference in the stopband height (15% increase from the wafer centre value) suggests a spatial variation in the mirror loss which, from Equation 2.17, is expected to affect the external differential efficiency. From device measurements at the locations A and C indicated in Figure 6.24, $\eta_{d,peak}$ is found to decrease from 0.99 to 0.94 ($\sim 6\%$) for the GaAs wafer and from 1.05 to 0.91 W/A ($\sim 13\%$) for the Ge wafer. Given that the reflectivity increases for the GaAs wafer, a drop in η_d is expected. The magnitude of the drop is lower than may be expected assuming the mirror loss is the dominant factor. For the Ge wafer, location C is in an isolated pocket of low stopband height and so an increase in η_d would be expected. The opposite is observed, which supports the argument that the pocket is an artifact of the measurement and not representative of the mirror reflectivity. The wafer-scale variation of the peak differential efficiency and peak power density for a GaAs and Ge wafer is shown in Figures 6.13 and 2.13. These wafers were oxidised in a convection-based furnace and the oxidation extent variation across the wafer is < 1 µm. In both cases the differential efficiency is highest at the wafer centre. There is a radial decrease for both wafers, but this is more pronounced for the GaAs

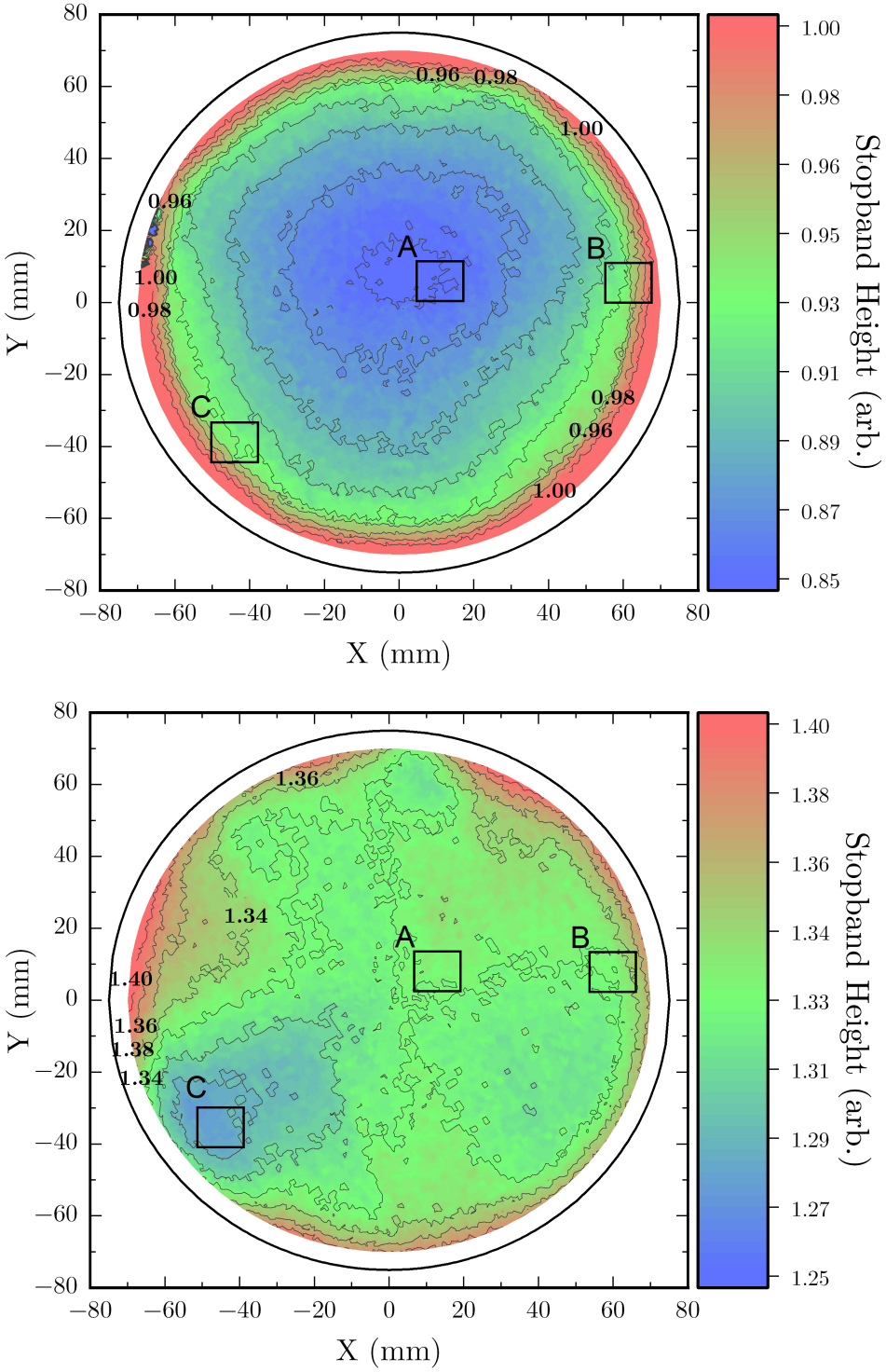

Figure 6.24: Stopband height variation for GaAs (top) and Ge (bottom) 6-inch wafers. The magnitudes are un-calibrated and therefore can only be used to assess variation within the wafer and not to compare the mirror reflectivity between the two wafers.

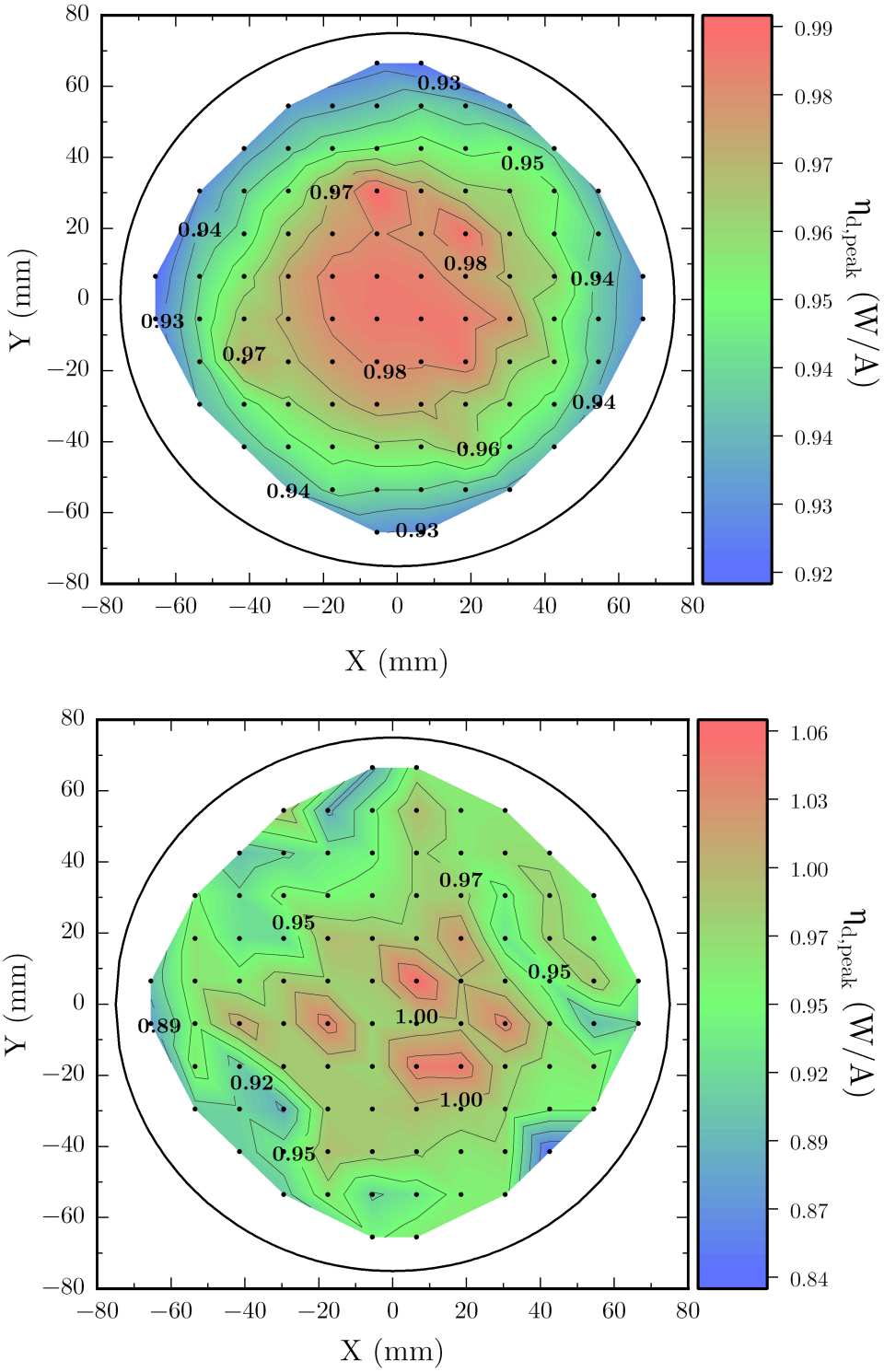

Figure 6.25: Wafer-scale variation of the peak differential efficiency of 38 µm mesa VCSELs across a 6-inch GaAs (top) and Ge (bottom) wafer. Both wafers were oxidised in a convection-based furnace and the oxidation extent variation is < 1 µm.

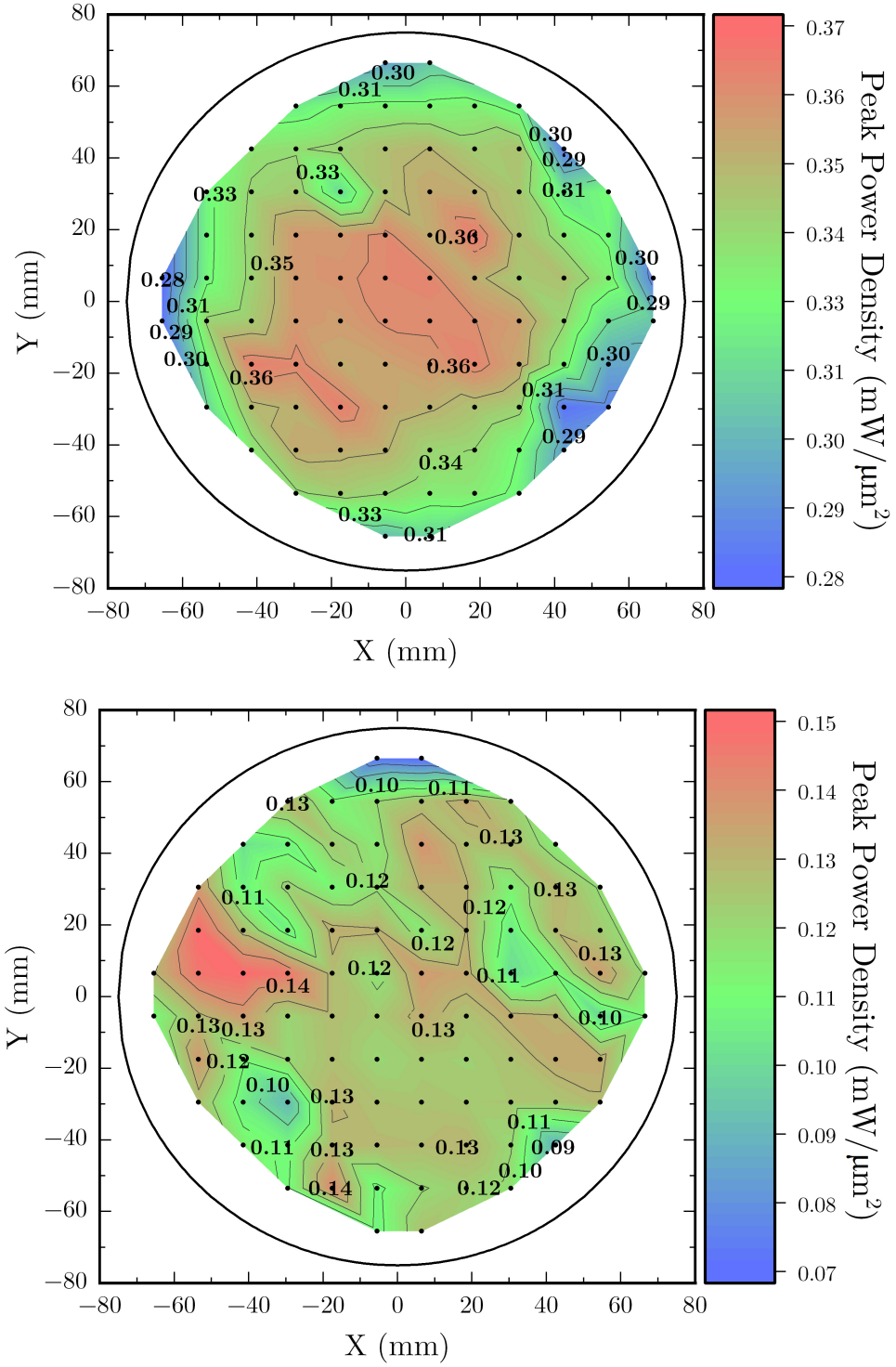

Figure 6.26: Wafer-scale variation of the peak power density of 38 µm mesa VCSELs across a 6-inch GaAs (top) and Ge (bottom) wafer. Both wafers were oxidised in a convection-based furnace and the oxidation extent variation is < 1 µm.

wafer. For the GaAs case, both the differential efficiency and peak optical power drop near the wafer edge, which suggests that the increase in mirror reflectivity (stopband height) plays a role. For the Ge wafer, the variation is observed despite the constant reflectivity measured from the stopband height. This suggests that a change in the optical absorption loss is the dominant contribution to the observed effects on device performance.

6.4 Summary

A detailed experimental comparison of AlGaAs-based 940 nm emission wavelength VCSELs grown on GaAs and Ge substrates has been presented in this chapter. Equivalence in the threshold current and threshold current density was demonstrated, as well as the emission spectra and lasing wavelength. The electrical resistance of the Ge VCSELs was found to be slightly higher than that of the GaAs VCSELs and this has been attributed to a difference in sheet resistance observed from the mapping of C-TLM structures. The shift in emission wavelength with temperature and current was demonstrated to be comparable for both device types. From measurement of the wavelength shift as a function of the dissipated power, the thermal resistance of ~ 6 µm devices was measured and found to be within error ($\pm$ 0.32 °C/mW) despite the smaller oxide aperture and thicker substrate of the Ge VCSELs. The thermal properties were further probed by assessment of the rollover point of the devices, with the observed differences associated with a variation in oxide aperture. The peak external differential efficiency was seen to be lower in the Ge VCSELs, likely driven by a difference in the overall optical loss in the structures and unrelated to the growth substrate. This reduced differential efficiency, as well as the increased electrical resistance, was shown to drive a decrease in power conversion efficiency ($\sim 8\%$) in the Ge VCSELs.

The reduced wafer bow and resulting improved oxidation uniformity of structures grown on Ge was presented, which has been previously demonstrated to improve the uniformity

of critical device performance characteristics, including electrical resistance and threshold current. The wafer-scale analysis of material properties was performed, demonstrating that the quality and uniformity of the VCSEL epitaxial structure is unaffected by growth on a Germanium substrate. The same wafer-scale variations as that of growth on GaAs were observed in the QW and active region layers, with highly uniform PL and FP wavelengths. Very similar behaviour in the detuning of the gain peak and cavity resonance results from this and leads to improved uniformity in the VCSEL threshold current density at elevated temperatures. The wafer-scale variation in the DBR reflectivity was assessed from the height of the stopband measured by reflectometry, however the impact on the external differential efficiency was shown to be minimal, suggesting some spatial variation in the internal optical loss. It should be noted again that Ge was used as a drop-in replacement for GaAs in this study, that is, the growth conditions used were optimised for a GaAs wafer. Subsequent optimisation must take place to account for the un-bowed Ge wafer to further assess the effect on material uniformity and yield.

In conclusion, parity in the performance between GaAs and Ge substrate VCSELs was demonstrated, with potential enhancements in the thermal properties of Ge VCSELs over their GaAs counterparts. The advantages of improved oxidation uniformity associated with the reduced wafer bow of large diameter VCSELs was demonstrated. It was shown that high-performance epitaxial structures can be grown on Ge substrates, with the wafer-scale uniformities equivalent to that of structures grown on GaAs.

Chapter 7

Conclusion

This thesis set out to address three research questions relating to the assessment of uniformity, yield, and reproducibility which arise in the volume production of VCSELs by MOVPE:

1. Can a method of rapid VCSEL fabrication be designed to streamline feedback in manufacturing, such that processing time is sufficiently reduced but device performance is preserved?
2. What wafer-scale non-uniformities arise in VCSEL production by MOVPE as the wafer size is increased?
3. Does growth on alternative substrates, such as Ge, provide any net advantages over growth on GaAs?

7.1 Conclusions

In Chapter 4, the question of whether a method for rapid VCSEL fabrication which preserves device performance was addressed. A QuickSEL process was developed such that devices can be produced within 24 hours using standard processing techniques. The key findings of that experimental study are summarised here.

The initial approach employed a bridge-mesa design, however, these devices were found to suffer from large leakage currents which resulted in high threshold currents. The performance of un-oxidised devices was assessed, and the threshold current was shown to further increase as a result of increased leakage and optical loss at the mesa sidewalls. It was concluded that QuickSELs should retain an oxide aperture to ensure performance better represented that of standard device architectures.

The next generation approach, utilising atypical mesa geometries for the definition of oxide-vias, achieved full electrical isolation and the definition of the VCSEL aperture simultaneously by selective oxidation of buried high-Al content AlGaAs confinement layers. This removed the need for the time-consuming processing step of dielectric-planarisation and required only two metal-deposition steps for the definition of the emission-side and substrate-side contacts (as opposed to three or more in a standard process). Additionally, careful design of the mesa geometry allowed both direct probing and, if required, wire bonding to the top contact as well, whilst the total oxidation length required for full electrical isolation remained reasonable (< 15 μm). These design attributes resulted in a 60% reduction in processing time relative to a standard BCB-planarised structure.

The performance of these QuickSEL devices was shown to be representative of that of standard structures with some limitations. The impact on lasing wavelength was negligible and shown to be determined by the material cavity resonance wavelength with some redshift due to Joule heating for both QuickSEL and standard devices. A difference in the degree of redshift was observed, related to the difference in thermal mass of the devices. This impact of the larger QuickSEL thermal mass was also seen in the wavelength shift with bias current. A calculated internal temperature increase per unit current resulting from a greater degree of self-heating was shown in standard structures. As the oxide aperture is preserved for the QuickSEL, only a small increase in threshold current ($\sim 10\%$) was found, which was attributed to surface recombination at the un-passivated mesa sidewalls. The difference in maximum output power was found to be within error of that expected due to oxide aperture variation, and the mean maximum power conversion efficiency was within the standard deviation for that of all devices measured.

In summary, a device design and fabrication process was developed such that VCSEL devices with performance close to that of standard BCB-planarised structures are produced within 24 hours. This is of use in VCSEL product development cycles and for assessment of wafer-scale, wafer-to-wafer, and run-to-run quality, and in the assessment of uniformity in volume manufacture where minimising operation time is imperative.

In Chapter 5, the quality and uniformity of generic MOVPE-grown 6-inch GaAs substrate VCSEL epi-wafers designed for 940 nm emission wavelength was assessed. These assessments were based on post-growth material characterisation, mapping of the oxide aperture, and through on-wafer testing of QuickSELs.

From reflectometry measurements, the FP resonance was found to shift to a shorter wavelength towards to the edge of the wafer, which was attributed to a 0.5% decrease in layer thickness. An abrupt shift in the stopband characteristics (width and centre wavelength) 20 mm from the wafer edge was observed and this was shown to result from the gradual appearance of sidebands in the reflectivity spectra. The FP resonance wavelength was shown to align centrally to the stopband centre (within 5 nm) across the whole wafer.

The PL wavelength was demonstrated to vary by < 1.5 nm across the wafer, with a radial decrease towards the wafer edge - consistent with an increasing QW photon energy. Simple calculations showed that layer thickness variations have a negligible impact on the QW transition energy, even for sizeable shifts. Therefore, it was explained that the variation in the PL wavelength is most likely derived from an increase in the bandgap energy in the QW, that is, from a decrease in the indium mole fraction. Furthermore, excellent uniformity in the PL intensity was shown, consistent with a high QW radiative efficiency across the wafer. Similar for the integrated PL signal and linewidth, which was observed to be on the order of that expected from thermal broadening across the whole wafer.

It was also shown that, when oxidised as a whole wafer in a conduction-based furnace, there can be a significant variation in the oxide aperture for a GaAs substrate wafer. The oxidation extent was shown to vary radially, increasing towards the edge, which is the result of temperature gradients during the oxidation process. The radial variation

was observed to be directly related to the bow of a 6-inch GaAs substrate wafer, which resulted in a lower temperature at the wafer centre. The contribution of the furnace non-uniformity was also described. The effect of wafer bow was removed by considering cleaved samples from different regions of a 6-inch wafer. Oxidising samples taken from the centre and edge of the wafer, the oxidation rate was found to be slower at the wafer edge - the opposite effect from what is observed for a whole wafer. This indicated that the Aluminium composition and/or layer thickness decreases towards the wafer edge, which was consistent with the findings from the FP and PL variation. Furthermore, this demonstrated that the influence of the wafer bow dominates that of the epi-layer variation.

As expected from the variation of the FP wavelength, the lasing wavelength was also shown to vary radially on the wafer, decreasing towards the edge. By assessing > 8 µm aperture devices at currents close to threshold, confinement effects associated with the oxide aperture and effects due to self-heating were negligible. This resulted in the VCSEL emission wavelength tracking very closely with the measured FP resonance wavelength.

The VCSEL threshold current was shown to vary in conjunction with the variation of the oxide aperture across the wafer. The wafer oxidised in a convection-based furnace produced superior oxidation uniformity compared to a conduction-based furnace, which resulted in an improved threshold current uniformity. Wafer-scale mapping of the oxidation extent allowed the variation in threshold current density to be measured, and assessing > 8 µm aperture devices reduced the impact of oxide variation on the measured performance. Despite this, a radial variation in threshold current density remained.

Measurement of the dependence on temperature (and specifically the temperature corresponding to the threshold current minima) revealed a spatial variation in the detuning of the gain peak and cavity resonance wavelengths - which is present due to the different sensitivities of the FP and PL wavelengths to shifts in the properties of the epi-layers. From the known shift of the gain peak wavelength with temperature, the room temperature gain peak wavelength was calculated. One benefit of the variation of the gain peak detuning means that the threshold current uniformity increases at elevated temperatures, close to the intended temperature of operation (~ 50°C).

The VCSEL peak optical power was also shown to track with the oxide aperture on the wafer. The optical power was observed to vary significantly on a wafer with poor oxidation uniformity. The variation was greatly reduced with a uniform oxidation. Similar to the threshold current density, the optical power density was calculated from the mapping of the oxidation extent across the wafer, and large devices were assessed to account for residual oxide aperture variation. When this quantity was mapped, the variation over most of the wafer was small but a drop off towards the edge was observed. This was compared to the measured height of the stopband for the same wafer, and found to correlate with an increase in reflectivity. The effects of this were also seen in the measured peak external differential efficiency, which was also observed to also reduce towards the wafer edge.

Overall, the quality and uniformity of generic MOVPE-grown 6-inch GaAs substrate VCSEL wafers was assessed. A decrease in the In mole fraction in the quantum wells was deduced to occur radially towards the wafer edge. This was found to also coincide with a decrease in the thickness of the epitaxial layers. Variation of the oxide aperture across wafers processed whole was shown to have a significant effect on the uniformity of device performance, particularly the threshold current and output power. Even when the oxide non-uniformity was corrected for, some residual variation in device performance was found to remain, which was attributed to the variation in the properties of the epi-layers, specifically, a spatially varying detuning of the gain peak and cavity resonance wavelengths and a variation in the mirror reflectivity.

In Chapter 6, a detailed experimental comparison of AlGaAs-based 940 nm emission wavelength VCSELs grown on GaAs and Ge substrates was presented.

Equivalence in the threshold current and threshold current density was demonstrated, as well as the emission spectra and lasing wavelength. The electrical resistance of the Ge VCSELs was found to be slightly higher than that of the GaAs VCSELs and this has been attributed to a difference in sheet resistance observed from the mapping of C-TLM structures. The shift in emission wavelength with temperature and current was demonstrated to be practically equivalent for both device types. From measurement of the wavelength

shift as a function of the dissipated power, the thermal resistance of ~ 6 µm devices was measured and found to be within error ($\pm$ 0.32 °C/mW) despite the smaller oxide aperture and thicker substrate of the Ge VCSELs. The thermal properties were further probed by assessment of the rollover point of the devices, with the observed differences associated with a variation in oxide aperture. The peak external differential efficiency was seen to be lower in the Ge VCSELs, likely driven by a difference in the overall optical loss in the different structures and was not thought to be related to the difference in growth substrate. This reduced differential efficiency, as well as the increases electrical resistance, was shown to drive a decrease in power conversion efficiency ($\sim 8\%$)for the Ge VCSELs. The reduced wafer bow and resulting improved oxidation uniformity of structures grown on Ge was presented, and was demonstrated to improve the uniformity of critical device performance characteristics, including threshold current and the peak optical power. The wafer-scale analysis of material properties was performed, demonstrating that the quality and uniformity of the VCSEL epitaxial structure is unaffected growth on a Ge substrate. The same wafer-scale variations as that of growth on GaAs were observed in the QW and active region layers, with highly uniform PL and FP wavelengths, and a similar spatial variation in the FP-PL detuning. This demonstrated that the radial variation across the wafer is not related to the wafer curvature. The wafer-scale variation in the DBR reflectivity was assessed from the height of the stopband measured by reflectometry.

In summary, parity in the performance between GaAs and Ge substrate VCSELs was demonstrated, with potential enhancements in the thermal properties of 940 nm VCSELs on Ge substrates. The advantages of improved oxidation uniformity associated with the reduced wafer bow of large diameter VCSELs was also shown. It was also shown that high-performance epitaxial structures can be grown on Ge substrates, with the wafer-scale uniformities equivalent to that of structures grown on GaAs.

7.1.1 Summary

To summarise, in this thesis, the development of a QuickSEL process was presented, such that devices can be produced within 24 hours using standard processing techniques without the need for planarisation or deposition of a dielectric. These electrically-isolated and oxide-confined VCSELs produce output characteristics comparable to that of standard BCB-planarised structures. This is intended to be of use in VCSEL product development cycles for the assessment of epi-wafer quality and uniformity, and in mapping wafer-scale, wafer-to-wafer, and run-to-run device performance in volume production settings.

From post-growth material characterisation and wafer-scale device-level testing, the quality and uniformity of generic MOVPE-grown 6-inch GaAs substrate VCSEL wafers was assessed. A decrease in the In mole fraction in the quantum wells was deduced to occur radially towards the wafer edge. This was found to also coincide with a decrease in the thickness of the epitaxial layers. Variation of the oxide aperture across wafers processed whole was shown to have a significant effect on the uniformity of device performance, particularly the threshold current and output power. Even when the oxide non-uniformity was corrected for, some residual variation in device performance was found to remain, which was attributed to the variation in the properties of the epi-layers, specifically, a spatially varying detuning of the gain peak and cavity resonance wavelengths and a variation in the mirror reflectivity.

A comparative experimental study of the performance of 940 nm VCSELs on GaAs and Ge substrates was performed by processing and characterising QuickSEL devices. Parity in performance between GaAs and Ge substrate VCSELs in terms of threshold current, threshold current density, series resistance, emission spectra, and wavelength tuning was demonstrated. The thermal resistance was measured to be within error despite a smaller oxide aperture and thicker substrate for the Ge VCSELs under test. Therefore, there may be potential enhancements to be found in the thermal performance of VCSELs on Ge.

The advantages of improved oxidation uniformity associated with the reduced wafer bow of large diameter Ge wafers was demonstrated. Improvements in the threshold current

and peak optical power uniformity was shown. The variation of the material properties represented by the photoluminescence and Fabry-Perot cavity resonance wavelengths, and the stopband characteristics were found to be equivalent, showing that the radial variation which is generally observed is not driven by the GaAs wafer curvature. This study demonstrated that high-performance epitaxial structures can be grown on Ge substrates with wafer-scale uniformities equivalent to that of structures grown on GaAs.

7.2 Future Work

In this section future directions for this work are discussed. Further investigations will likely centre on expanding on the experimental studies presented in chapters 4, 5, and 6. Whilst the characterisation of QuickSEL devices presented in Chapter 4 was sufficient to show parity with standard BCB-planarised VCSEL structures, further information on QuickSEL device performance may be obtained. Some questions remain relating to the quasi-circular aperture shape and how this affects the beam profile. Near-field imaging may be employed to assess the transverse mode profile of the QuickSELs. In addition, far-field imaging can be used to understand the beam divergence relative to standard circular aperture VCSELs. The latter is of particular concern in studies relating to the production of VCSELs for sensing applications.Furthermore, to more accurately assess the effects of sidewall passivation on device performance, it would be advantageous to produce QuickSEL devices, through the fabrication methods presented earlier, but which also undergo a BCB planarisation step. This would allow the suggestion that a reduction in the rate of sidewall recombination in standard VCSELs contributes to a decrease in threshold current to be verified.

The significant impact of oxide aperture variation on the wafer-scale non-uniformity of device performance was demonstrated in Chapter 5. These assessments were based on optical measurements of the oxidation extent in-situ, however, alternative methods of mapping oxidation length via on-wafer electrical measurements of designated test struc-

tures may also be employed[1]. This technique is promising for efficient and reliable oxide aperture mapping and would benefit from studies correlating with destructive characterisation (SEM) and in-situ optical measurements. Further consideration could also be given to other variations arising in fabrication. For future investigations, a more in-depth study on metallisation, particularly concerning the variation of specific contact resistance, could be conducted. In similarity to the study of oxidation uniformity, this can be related back to temperature gradients within the anneal chamber and how this translates into electrical contact quality. Additionally, more attention to etch-depth uniformity could be given, in particular relating to the effect of aspect ratio dependent etch rates.

To give weight to the conclusions given concerning the origins of on-wafer device performance non-uniformity, future work should include focus on relating destructive characterisation (SIMS, TEM and SEM) to quantify true thickness, composition, and doping concentrations variations. Correlating this information with device measurements and physical models will help to better understand the propagation of material variation through to device performance. In particular, in understanding whether mirror or absorption losses contribute to the observed centre-to-edge differences in the threshold current density minima, and if the latter, assessing whether this correlates with higher doping concentrations. Similarly this approach can be applied to the differential efficiency and oxidation extent variation to ascertain if observations align with the expectations relating to Al composition and layer thickness. Furthermore, the PL peak and FP resonances should be examined to discern whether they are influenced more strongly by fluctuations in material composition (QW In content/cavity effective index) or thickness.

In the context of wafer-scale uniform mode control, the use of an oxide aperture was found to introduce challenges for achieving consistent mode volumes across a large wafer. Future investigations could be employed to explore the uniformity benefits of alternative methods, such as in-phase/anti-phase structures, which may include a cap etch or the deposition of a dielectric layer. This research could lead to a more standardised approach

[1] J. Baker, C. Hentschel, C. P. Allford, S. Gillgrass, J. I. Davies, S. Shutts, P. M. Smowton, 'Characterisation techniques for on-wafer testing of VCSELs in volume manufacture', International Conference on Compound Semiconductor Manufacturing, May 2023.

to mode control in volume production and its comparison to that provided by oxidation would be a valuable study.

This thesis has focussed on variation within individual wafers, however, variation wafer-to-wafer and run-to-run is paramount in manufacturing. The fabrication and characterisation techniques presented in this thesis can also be applied to assess variation for all wafers in a growth run and throughout a growth campaign, characterising overall reactor uniformity and assessing the effect of reactor drift. This study would provide useful insights towards producing refined epitaxial designs and reproducible processes.

Parity in the performance of 940 nm emitting VCSELs grown on both GaAs and Ge substrates was presented in Chapter 6. However, future work could be devoted to further understanding the slight difference in series resistance and whether this relates to the Ge-epi interface. Furthermore, given the higher thermal conductivity of Ge, it was suggested that growth on Ge may yield benefits in the thermal performance of VCSELs. Further characterisation, minimising uncertainty, is required to demonstrate an decrease in thermal resistance. Measurements should also be performed on industry-standard VCSELs grown on Ge (as opposed to QuickSEL devices) to assess the benefits for high-power and high-temperature operation. The thermal performance may also be further improved by growth on thinned substrates, of which there is commercial availability for Ge. This would also provide the economic benefit of using less material per growth run relative to standard GaAs substrates. A study assessing both the performance benefits and impact on wafer-scale variation could therefore be conducted.

Moreover, given that Ge substrates are produced with zero defects, the impact on the reliability of VCSELs on Ge may be assessed. Defect scanning and x-ray diffraction characterisation of VCSELs on Ge can be performed and correlated with accelerated life-testing and failure analysis. The overall impact on yield could quantified by considering the wafer-scale variation in defect density for GaAs and Ge VCSELs.

Despite the potential benefits of Ge in VCSEL manufacturing, there are some challenges to overcome, one relating to chip separation. VCSELs grown on Ge cannot be cleaved like those on GaAs and require laser/etch methods for chip dicing. A comparative study

into different dicing methods for Ge VCSELs and their impact on device performance would be a valuable study towards addressing one of the key technical challenges facing the adoption of Ge for volume VCSEL production.

Bibliography

[1] H. Soda, K. I. Iga, C. Kitahara, and Y. Suematsu, "GaInAsP/InP surface emitting injection lasers," *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers*, vol. 18, no. 12, pp. 2329–2330, 1979, ISSN: 13474065. DOI: 10.1143/JJAP.18.2329.

[2] J. A. Tatum, A. Clark, J. K. Guenter, R. A. Hawthorne III, and R. H. Johnson, "Commercialization of Honeywell's VCSEL technology," in *Vertical-Cavity Surface-Emitting Lasers IV*, K. D. Choquette and C. Lei, Eds., vol. 3946, SPIE, May 2000, pp. 2–13. DOI: 10.1117/12.384359.

[3] K. Iga, "Semiconductor Lasers and VCSEL History," *VCSEL Industry: Communication and Sensing*, pp. 1–27, Jan. 2021. DOI: 10.1002/9781119782223.CH1.

[4] N. Mukoyama, H. Otoma, J. Sakurai, N. Ueki, H. Nakayama Naotaka Mukoyama, and H. Nakayama, "VCSEL array-based light exposure system for laser printing," in *Vertical Cavity Surface Emitting Lasers XII*, vol. 6908, SPIE, Jan. 2008, pp. 146–156, ISBN: 9780819470836. DOI: 10.1117/12.768479.

[5] Doug Collins and Neinyi Li, *Optical mouse using VCSELs*, Aug. 2006.

[6] J.-F. Seurin, C. L. Ghosh, V. Khalfin, A. Miglo, G. Xu, J. D. Wynn, P. Pradhan, and L. A. D'Asaro, "High-power high-efficiency 2D VCSEL arrays," in *Vertical-Cavity Surface-Emitting Lasers XII*, C. Lei and J. K. Guenter, Eds., vol. 6908, SPIE, Feb. 2008, p. 690 808. DOI: 10.1117/12.774126.

[7] N.-Y. Li, D. Collins, S. Jatar, O. Lavrova, C. Helms, a. Nein-Yi Li, W. Luo, L. Liu, C. Liu, M. Qiu, K. Roff, C. Wang, C.-C. Yang, and H.-K. Chiou, "Design and manufacturing of 10G GenX VCSELs at Emcore," in *Integrated Optoelectronic Devices*, vol. 6484, SPIE, Feb. 2007, pp. 11–21, ISBN: 0819465976. DOI: 10.1117/12.715079.

[8] E. Haglund, Å. Haglund, P. Westbergh, J. S. Gustavsson, B. Kögel, and A. Larsson, "25Gbit/s transmission over 500m multimode fibre using 850nm VCSEL with integrated mode filter," *Electronics Letters*, vol. 48, no. 9, pp. 517–519, Apr. 2012, ISSN: 00135194. DOI: 10.1049/EL.2012.0529/CITE/REFWORKS.

[9] D. Cheskis, "Lumentum: Illumination Sources for Head-Mounted Displays," *SPIE AVR21 Industry Talks II*, vol. 11764, p. 117640C, Mar. 2021. DOI: 10.1117/12.2597457.

[10] A. Johnson, A. Joel, A. Clark, D. Pearce, M. Geen, W. Wang, R. Pelzel, and S. W. Lim, "High performance 940nm VCSELs on large area germanium substrates: the ideal substrate for volume manufacture," in *Vertical Cavity Surface Emitting Lasers XXV*, vol. 11704, SPIE-Intl Soc Optical Eng, Mar. 2021. DOI: 10.1117/12.2583207.

[11] J. Iwan Davies, A. D. Johnson, R. I. Pelzel, M. D. Geen, A. M. Joel, and S. Wook Lim, "MOVPE and its future production challenges," *Journal of Crystal Growth*, p. 127 031, Dec. 2022, ISSN: 0022-0248. DOI: 10.1016/J.JCRYSGRO.2022.127031.

[12] *IQE announces the world's first commercially available 200 mm (8") VCSEL wafer — IQE Corporate*, May 2022.

[13] R. Koerner, S. Bader, M. Herper, T. Kischkat-Grimm, J. Tempeler, a. Roman Koerner, A. van der Lee, H. Moench, A. Pruijmboom, M. Aviles Rodriguez, U. Weichmann, and A. Weigl, "Polarization multiplexing in VCSEL-arrays," *Vertical Cavity Surface Emitting Lasers XVII*, vol. 12439, no. 15, p. 1 243 902, Mar. 2023, ISSN: 1996756X. DOI: 10.1117/12.2647683.

[14] R. Morgan, J. Lehman, M. A. Hibbs-Brenner Robert Morgan, J. A. Lehman, and M. K. Hibbs-Brenner, "Vertical-cavity surface-emitting lasers come of age," in *Fabrication, Testing,and Reliability of Semiconductor Lasers*, vol. 2683, SPIE, Apr. 1996, pp. 18–29, ISBN: 0819420573. DOI: 10.1117/12.237688.

[15] M. Grabherr, H. Moench, and A. Pruijmboom, "VCSELs for optical mice and sensing," *Springer Series in Optical Sciences*, vol. 166, pp. 521–538, 2013, ISSN: 15561534. DOI: 10.1007/978-3-642-24986-0{_}17/FIGURES/17.

[16] H. Nakayama, T. Nakamura, M. Funada, Y. Ohashi, and M. Kato, "780nm VCSELs for home networks and printers," in *Electronic Components and Technology Conference*, vol. 2, 2004, pp. 1371–1375. DOI: 10.1109/ECTC.2004.1320290.

[17] T. Kondo, K. Takeda, H. Otoma, A. Murakami, J. Sakurai, H. Nakayama, X. Gu, and F. Koyama, "Developments of VCSELs for printers and optical communications at Fuji Xerox," in *Vertical Cavity Surface Emitting Lasers XX*, vol. 9766, SPIE, Mar. 2016, pp. 51–59, ISBN: 9781510600010. DOI: 10.1117/12.2218316.

[18] H. Frazier, "The 802.3z Gigabit Ethernet Standard," *IEEE Network*, vol. 12, no. 3, pp. 6–7, 1998, ISSN: 08908044. DOI: 10.1109/65.690946.

[19] D. L. Huffaker, D. G. Deppe, K. Kumar, and T. J. Rogers, "Native-oxide defined ring contact for low threshold vertical-cavity lasers," *Appl. Phys. Lett*, vol. 65, p. 97, 1994. DOI: 10.1063/1.113087.

[20] Y. Ou, J. S. Gustavsson, P. Westbergh, Å. Haglund, A. Larsson, and A. Joel, "Impedance characteristics and parasitic speed limitations of high-speed 850-nm VCSELs," *IEEE Photonics Technology Letters*, vol. 21, no. 24, pp. 1840–1842, Dec. 2009, ISSN: 10411135. DOI: 10.1109/LPT.2009.2034618.

[21] P. Westbergh, J. S. Gustavsson, Å. Haglund, M. Sköld, A. Joel, and A. Larsson, "High-speed, low-current-density 850 nm VCSELs," *IEEE Journal on Selected Topics in Quantum Electronics*, vol. 15, no. 3, pp. 694–703, May 2009, ISSN: 1077260X. DOI: 10.1109/JSTQE.2009.2015465.

[22] A. Larsson, "Advances in VCSELs for communication and sensing," *IEEE Journal on Selected Topics in Quantum Electronics*, vol. 17, no. 6, pp. 1552–1567, 2011, ISSN: 1077260X. DOI: 10.1109/JSTQE.2011.2119469.

[23] L. Arthur D'Asaro, Jean-Francois Seurin, and Chuni Ghosh, "VCSELs: Powerful VCSEL arrays beat the heat," *Laser Focus World*, Nov. 2007.

[24] J. Baker, S. Gillgrass, T. Peach, C. P. Allford, J. I. Davies, A. D. Johnson, A. M. Joel, S. W. Lim, S. Shutts, and P. M. Smowton, "Impact of strain-induced bow on the performance of VCSELs on 150mm GaAs- and Ge-substrate wafers," *Semiconductor Lasers and Laser Dynamics X*, vol. PC12141, K. Panajotov, M. Sciamanna, and S. Höfling, Eds., PC1214108, May 2022. DOI: 10.1117/12.2624492.

[25] J. Baker, S. Gillgrass, T. Peach, C. P. Allford, J. I. Davies, A. D. Johnson, A. M. Joel, S. W. Lim, S. Shutts, and P. M. Smowton, "Impact of strain-induced bow on the performance of VCSELs on 150mm GaAs- and Ge-substrate wafers," in *Semiconductor Lasers and Laser Dynamics X*, vol. PC12141, SPIE, May 2022, PC1214108. DOI: 10.1117/12.2624492.

[26] Y. Zhao, J. Guo, M. Feifel, H.-T. Cheng, Y.-C. Yang, L. Wang, L. Chrostowski, D. Lackner, C.-H. Wu, and G. (Xia, "Monolithic integration of 940nm AlGaAs distributed Bragg reflectors on bulk Ge substrates," *Optical Materials Express*, vol. 12, no. 3, p. 1131, Mar. 2022, ISSN: 2159-3930. DOI: 10.1364/OME.452161.

[27] S.-J. Gillgrass, C. P. Allford, A. D. Johnson, J. Baker, J. I. Davies, S. Shutts, and P. M. Smowton, "Characterisation of 200 mm GaAs and Ge substrate VCSELs for high-volume manufacturing," in *SPIE Photonics West, Vertical Cavity Surface Emitting Lasers XXVII*, San Francisco, CA: SPIE, Feb. 2023.

[28] J.-F. Seurin, G. Xu, A. Miglo, R. V. Leeuwen, H. Othman, S. Okur, Y. Zhang, A. Amtout, H. Bian, H. Yuan, and E. M. Shaw, "Multi-junction vertical-cavity surface-emitting lasers in the 800-1100nm wavelength range," *Vertical Cavity Surface Emitting Lasers XXV*, vol. 11704, 117040B, Mar. 2021. DOI: 10.1117/12.2578767.

[29] M. Dummer, A. Ghods, K. Tatah, and K. Johnson, "High-power single-mode multijunction VCSEL," *Conference Digest - IEEE International Semiconductor Laser Conference*, vol. 2022-October, 2022, ISSN: 08999406. DOI: 10.23919/ISLC52947.2022.9943419.

[30] P. Staudinger, W. Pallmann, S. Paul, L. Marigo, S. Marigo, J. Boucart, L. Mutter, and J. Müller, "Multi-junction lasers for LiDAR applications," in *High Power Diode Laser Technology XXI*, vol. 12403, SPIE, Mar. 2023, pp. 14–20. DOI: 10.1117/12.2655771.

[31] E. Hegblom, G. Zhao, J. Yang, Y. Zhu, A. Barve, B. Kesler, S. Xie, M. Dolganov, Y. Li, C. S. Hsieh, S. Burns, K. Zhuang, M. G. Peters, and J. Skidmore, "Addressable High-Performance Multi-junction VCSEL Arrays for Automotive and Mobile LiDAR," *Conference Digest - IEEE International Semiconductor Laser Conference*, 2021, ISSN: 08999406. DOI: 10.1109/ISLC51662.2021.9615759.

[32] M. Gbski, M. Gbski, D. Dontsova, N. Haghighi, K. Nunna, R. Yanka, A. Johnson, R. Pelzel, and J. A. Lott, "Baseline 1300nm dilute nitride VCSELs," *OSA Continuum, Vol. 3, Issue 7, pp. 1952-1957*, vol. 3, no. 7, pp. 1952–1957, Jul. 2020, ISSN: 2578-7519. DOI: 10.1364/OSAC.396242.

[33] J. A. Tatum, L. A. Graham, J. K. Guenter, and P. Khurana, "Commercialization of VCSELs," in *26th Microoptics Conference, MOC 2021*, Institute of Electrical and Electronics Engineers Inc., 2021, ISBN: 9784863487758. DOI: 10.23919/MOC52031.2021.9598106.

[34] B. D. Padullaparthi, "VCSEL Industry," in *VCSEL Industry: Communication and Sensing*, John Wiley & Sons, Ltd, Jan. 2021, ch. VCSEL Industry: Pro... Pp. 47–71, ISBN: 9781119782223. DOI: 10.1002/9781119782223.CH3.

[35] D. Cheskis, "6-inch VCSEL Wafer Fabrication Foundry Economics," *CS Mantech Conference Digest*, 2015.

[36] B. Dayal Padullaparthi, J. A. Tatum, and K. Iga, "Appendix B: Epitaxial Growth Engineering," *VCSEL Industry*, pp. 221–233, Nov. 2021. DOI: 10.1002/9781119782223.APP2.

[37] R. P. Schneider, R. P. Bryan, J. A. Lott, and G. R. Olbright, "Visible (657 nm) InGaP/InAlGaP strained quantum well vertical-cavity surface-emitting laser," *Applied Physics Letters*, vol. 60, no. 15, pp. 1830–1832, Apr. 1992, ISSN: 0003-6951. DOI: 10.1063/1.107178.

[38] R. P. Schneider and J. A. Lott, "Cavity design for improved electrical injection in InAlGaP/AlGaAs visible (639–661 nm) vertical-cavity surface-emitting laser diodes," *Applied Physics Letters*, vol. 63, no. 7, pp. 917–919, Aug. 1993, ISSN: 0003-6951. DOI: 10.1063/1.109844.

[39] P. (Blood, *Quantum confined laser devices : optical gain and recombination in semiconductors*, ISBN: 0191064653.

[40] J. Piprek, T. Tröger, B. Schröter, J. Kolodzey, and C. S. Ih, "Thermal conductivity reduction in GaAs-AlAs distributed Bragg reflectors," *IEEE Photonics Technology Letters*, vol. 10, no. 1, pp. 81–83, Jan. 1998, ISSN: 10411135. DOI: 10.1109/68.651113.

[41] A. Khan, "Vertical cavity surface emitting lasers: Design, characterisation and integration," *Doctoral thesis, University College London (United Kingdom).*, 1995.

[42] S. B. Healy, E. P. O'Reilly, J. S. Gustavsson, P. Westbergh, Å. Haglund, A. Larsson, and A. Joel, "Active region design for high-speed 850-nm VCSELs," *IEEE Journal of Quantum Electronics*, vol. 46, no. 4, pp. 506–512, 2010, ISSN: 00189197. DOI: 10.1109/JQE.2009.2038176.

[43] R. Michalzik, *VCSELs: Fundamentals, Technology and Applications of Vertical-Cavity Surface Emitting Lasers*. Springer, 2012.

[44] S. W. Corzine, R. S. Geels, J. W. Scott, R. H. Yan, and L. A. Coldren, "Design of Fabry-Perot Surface-Emitting Lasers with a Periodic Gain Structure," *IEEE Jour-*

nal of Quantum Electronics, vol. 25, no. 6, pp. 1513–1524, 1989, ISSN: 15581713. DOI: 10.1109/3.29288.

[45] T. E. Sale, "Vertical Cavity Surface Emitting Lasers," Tech. Rep., 1993.

[46] P. Westbergh, J. S. Gustavsson, B. Kögel, Å. Haglund, and A. Larsson, "Impact of photon lifetime on high-speed VCSEL performance," *IEEE Journal on Selected Topics in Quantum Electronics*, vol. 17, no. 6, pp. 1603–1613, 2011, ISSN: 1077260X. DOI: 10.1109/JSTQE.2011.2114642.

[47] M. A. Bobrov, S. A. Blokhin, A. G. Kuzmenkov, N. A. Maleev, A. A. Blokhin, Y. M. Zadiranov, E. V. Nikitina, and V. M. Ustinov, "Effect of the photon lifetime on the characteristics of 850-nm vertical-cavity surface-emitting lasers with fully doped distributed Bragg reflectors and an oxide current aperture," *Semiconductors*, 2014, ISSN: 10637826. DOI: 10.1134/S1063782614120033.

[48] G. R. Hadley, "Effective index model for vertical-cavity surface-emitting lasers," *Optics Letters*, vol. 20, no. 13, p. 1483, Jul. 1995, ISSN: 0146-9592. DOI: 10.1364/ol.20.001483.

[49] D. L. Huffaker, J. Shin, and D. G. Deppe, "Lasing characteristics of low threshold microcavity lasers using half-wave spacer layers and lateral index confinement," *Applied Physics Letters*, vol. 66, no. 14, p. 1723, Jun. 1998, ISSN: 0003-6951. DOI: 10.1063/1.113346.

[50] K. D. Choquette, K. L. Lear, R. P. Schneider, and K. M. Geib, "Cavity characteristics of selectively oxidized vertical-cavity lasers," *Appl. Phys. Lett*, vol. 66, p. 3413, 1995. DOI: 10.1063/1.113371.

[51] K. L. Lear, K. D. Choquette, R. P. Schneider, S. P. Kilcoyne, and K. M. Geib, "Selectively oxidised vertical cavity surface emitting lasers with 50% power conversion efficiency," *Electronics Letters*, vol. 31, no. 3, pp. 208–209, Feb. 1995, ISSN: 00135194. DOI: 10.1049/el:19950125.

[52] E. R. Hegblom, N. M. Margalit, B. Thibeault, L. A. Coldren, and J. E. Bowers, "Current spreading in apertured vertical-cavity lasers," in *Vertical-Cavity Surface-Emitting Lasers*, vol. 3003, SPIE, Apr. 1997, pp. 176–180. DOI: 10.1117/12.271065.

[53] B. Thibeault, E. R. Hegblom, Y. A. Akulova, J. Ko, R. L. Naone, L. A. Coldren, and P. D. Floyd, "Electrical and optical losses in dielectrically apertured vertical-cavity lasers," in *Vertical-Cavity Surface-Emitting Lasers*, vol. 3003, SPIE, Apr. 1997, pp. 86–99. DOI: 10.1117/12.271055.

[54] D. I. Babic and S. W. Corzine, "Analytic Expressions for the Reflection Delay, Penetration Depth, and Absorptance of Quarterwave Dielectric Mirrors," *IEEE Journal of Quantum Electronics*, vol. 28, no. 2, pp. 514–524, 1992, ISSN: 15581713. DOI: 10.1109/3.123281.

[55] Niazul Islam Khan ; Samiul Hayder Choudhury ; Arif Ahmed Roni, "A comparative study of the temperature dependence of lasing wavelength of conventional edge emitting stripe laser and vertical cavity surface emitting laser - IEEE Conference Publication," *Proceedings of the International Conference on Optical Communication Systems*, 2011.

[56] M. B. Panish and H. C. Casey, "Temperature Dependence of the Energy Gap in GaAs and GaP," *Journal of Applied Physics*, vol. 40, p. 163, 1969. DOI: 10.1063/1.1657024.

[57] J. J. Dudley, D. L. Crawford, and J. E. Bowers, "Temperature Dependence of the Properties of DBR Mirrors Used in Surface Normal Optoelectronic Devices," *IEEE Photonics Technology Letters*, vol. 4, no. 4, pp. 311–314, 1992, ISSN: 19410174. DOI: 10.1109/68.127197.

[58] C. H. McMahon, J. W. Bae, C. S. Menoni, D. Patel, H. Temkin, P. Brusenbach, and R. Leibenguth, "Detuning of the gain and reflectivity spectra and its effect on the output characteristics of vertical cavity surface emitting lasers," *Applied*

Physics Letters, vol. 66, no. 17, pp. 2171–2173, Apr. 1995, ISSN: 0003-6951. DOI: 10.1063/1.113936.

[59] D. B. Young, J. W. Scott, F. H. Peters, M. G. Peters, M. L. Majewski, B. J. Thibeault, S. W. Corzine, and L. A. Coldren, "Enhanced Performance of Offset-Gain High-Barrier Vertical-Cavity Surface-Emitting Lasers," *IEEE Journal of Quantum Electronics*, vol. 29, no. 6, pp. 2013–2022, 1993, ISSN: 15581713. DOI: 10.1109/3.234464.

[60] J. Talghader and J. S. Smith, "Thermal dependence of the refractive index of GaAs and AlAs measured using semiconductor multilayer optical cavities," *Applied Physics Letters*, vol. 66, no. 3, p. 335, Jan. 1995, ISSN: 00036951. DOI: 10.1063/1.114204.

[61] W. W. Chow, K. D. Choquette, and S. W. Koch, "Physics of the Gain Medium in Vertical-Cavity Surface-Emitting Semiconductor Lasers," in Springer, Berlin, Heidelberg, 2003, pp. 31–51. DOI: 10.1007/978-3-662-05263-1{_}2.

[62] H. Li, P. Wolf, P. Moser, G. Larisch, A. Mutig, J. A. Lott, and D. H. Bimberg, "Impact of the quantum well gain-to-cavity etalon wavelength offset on the high temperature performance of high bit rate 980-nm VCSELs," *IEEE Journal of Quantum Electronics*, vol. 50, no. 8, pp. 613–621, 2014. DOI: 10.1109/JQE.2014.2330255.

[63] C. Chen, P. O. Leisher, A. A. Allerman, K. M. Geib, and K. D. Choquette, "Temperature analysis of threshold current in infrared vertical-cavity surface-emitting lasers," *IEEE Journal of Quantum Electronics*, vol. 42, no. 10, pp. 1078–1083, Oct. 2006, ISSN: 00189197. DOI: 10.1109/JQE.2006.881828.

[64] C. W. Wilmsen, H. (Temkin, and L. A. (A. Coldren, *Vertical-cavity surface-emitting lasers : design, fabrication, characterization, and applications*. Cambridge University Press, 2001, p. 480, ISBN: 9780521006293.

[65] L. A. (A. Coldren, S. W. (W. Corzine, and M. Mashanovitch, *Diode lasers and photonic integrated circuits*. Wiley, 2012, p. 709, ISBN: 9781118148198.

[66] P. P. Baveja, B. Kögel, P. Westbergh, J. S. Gustavsson, Å. Haglund, D. N. Maywar, G. P. Agrawal, and A. Larsson, "Assessment of VCSEL thermal rollover mechanisms from measurements and empirical modeling," *Optics Express*, vol. 19, no. 16, p. 15 490, Aug. 2011, ISSN: 1094-4087. DOI: 10.1364/oe.19.015490.

[67] J.-F. Seurin, C. Ghosh, V. Khalfin, A. Miglo, G. Xu, a. Jean-Francois Seurin, C. L. Ghosh, J. D. Wynn, P. Pradhan, and L. D. Arthur, "High-power high-efficiency 2D VCSEL arrays," *Proceedings of SPIE*, vol. 6908, no. 29, pp. 45–58, Jan. 2008, ISSN: 0277786X. DOI: 10.1117/12.774126.

[68] H. D. Summers, J. Wu, and J. S. Roberts, "Experimental investigation of thermally induced power saturation in vertical-cavity surface-emitting lasers," *IEE Proceedings: Optoelectronics*, vol. 148, no. 5-6, pp. 261–265, Oct. 2001, ISSN: 13502433. DOI: 10.1049/IP-OPT:20010751.

[69] W. Shockley, "The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors," *Bell System Technical Journal*, vol. 28, no. 3, pp. 435–489, 1949, ISSN: 15387305. DOI: 10.1002/J.1538-7305.1949.TB03645.X.

[70] R. S. Geels, S. W. Corzine, J. W. Scott, D. B. Young, and L. A. Coldren, "Low Threshold Planarized Vertical-Cavity Surface-Emitting Lasers," *IEEE Photonics Technology Letters*, vol. 2, no. 4, pp. 234–236, 1990, ISSN: 19410174. DOI: 10.1109/68.53246.

[71] S. A. Chalmers, K. L. Lear, and K. P. Killeen, "Low resistance wavelength-reproducible p-type (Al,Ga)As distributed Bragg reflectors grown by molecular beam epitaxy," *Applied Physics Letters*, vol. 62, no. 14, pp. 1585–1587, Apr. 1993, ISSN: 0003-6951. DOI: 10.1063/1.109608.

[72] M. Sugimoto, H. Kosaka, K. Kurihara, I. Ogura, T. Numai, and K. Kasahara, "Very low threshold current density in vertical-cavity surface-emitting laser diodes with periodically doped distributed Bragg reflectors," *Electronics Letters*, vol. 28, no. 4, pp. 385–387, 1992, ISSN: 00135194. DOI: 10.1049/EL:19920241.

[73] J. Wu, W. Xiao, and Y. M. Lu, "Temperature and wavelength dependence of gain and threshold current detuning with cavity resonance in vertical-cavity surface-emitting lasers," *IET Optoelectronics*, vol. 1, no. 5, pp. 206–210, Oct. 2007, ISSN: 17518768. DOI: 10.1049/iet-opt:20070039.

[74] M. H. MacDougal, P. D. Dapkus, V. Pudikov, H. Zhao, and G. M. Yang, "Ultralow Threshold Current Vertical-Cavity Surface-Emitting Lasers with AlAs Oxide—GaAs Distributed Bragg Reflectors," *IEEE Photonics Technology Letters*, vol. 7, no. 3, pp. 229–231, 1995, ISSN: 19410174. DOI: 10.1109/68.372729.

[75] M. Daubenschüz, "Determination of the Thermal Resistance of VCSELs Simplified Determination of the Thermal Resistance of Vertical-Cavity Surface-Emitting Lasers," Institute of Optoelectronics, Ulm University, Ulm, Tech. Rep., 2015, pp. 21–28.

[76] H. M. Manasevit and W. I. Simpson, "The Use of Metal-Organics in the Preparation of Semiconductor Materials," *Journal of The Electrochemical Society*, vol. 116, no. 12, p. 1725, Dec. 1969, ISSN: 00134651. DOI: 10.1149/1.2411685/XML.

[77] H. M. Manasevit, "The use of metalorganics in the preparation of semiconductor materials: Growth on insulating substrates," *Journal of Crystal Growth*, vol. 13-14, no. C, pp. 306–314, May 1972, ISSN: 0022-0248. DOI: 10.1016/0022-0248(72)90175-3.

[78] M. J. Ludowise, "Metalorganic chemical vapor deposition of III-V semiconductors," *Journal of Applied Physics*, vol. 58, no. 8, R31, Jun. 1985, ISSN: 0021-8979. DOI: 10.1063/1.336296.

[79] R. D. Dupuis, P. D. Dapkus, C. M. Garner, C. Y. Su, and W. E. Spicer, "Abrupt Ga1xAlxAs-GaAs quantum-well heterostructures grown by metalorganic chemical vapor deposition," *Applied Physics Letters*, vol. 34, no. 5, p. 335, Aug. 2008, ISSN: 0003-6951. DOI: 10.1063/1.90778.

[80] R. D. Dupuis and P. D. Dapkus, "Ga(1x)AlxAs/Ga(1y)AlyAs double-heterostructure room-temperature lasers grown by metalorganic chemical vapor deposition," *Applied Physics Letters*, vol. 31, no. 12, p. 839, Aug. 2008, ISSN: 0003-6951. DOI: 10.1063/1.89569.

[81] F. Koyama, K. Tomomatsu, and K. Iga, "GaAs surface emitting lasers with circular buried heterostructure grown by metalorganic chemical vapor deposition and two-dimensional laser array," *Applied Physics Letters*, vol. 52, no. 7, p. 528, Jun. 1988, ISSN: 0003-6951. DOI: 10.1063/1.99405.

[82] F. Koyama, S. Kinoshita, and K. Iga, "Room-temperature continuous wave lasing characteristics of a GaAs vertical cavity surface-emitting laser," *Appl. Phys. Lett*, vol. 55, p. 221, 1989. DOI: 10.1063/1.101913.

[83] G. B. Stringfellow, "Design of the OMVPE Process," *Organometallic Vapor-Phase Epitaxy*, pp. 235–283, Jan. 1989. DOI: 10.1016/B978-0-12-673840-7.50012-9.

[84] *AIX 2800G4-TM for GaAs/InP based Optoelectronics and p-HEMT/HBT Devices*, 2016.

[85] F. H. Yang, "Modern metal-organic chemical vapor deposition (MOCVD) reactors and growing nitride-based materials," *Nitride Semiconductor Light-Emitting Diodes (LEDs): Materials, Technologies and Applications*, pp. 27–65, Jan. 2014. DOI: 10.1533/9780857099303.1.27.

[86] D. Brien, M. Dauelsberg, K. Christiansen, J. Hofeldt, M. Deufel, and M. Heuken, "Modelling and simulation of MOVPE of GaAs-based compound semiconductors in production scale Planetary Reactors," *Journal of Crystal Growth*, vol. 303, no. 1, pp. 330–333, May 2007, ISSN: 0022-0248. DOI: 10.1016/J.JCRYSGRO.2006.11.319.

[87] Y. Gou, J. Wang, Y. Cheng, Y. Guo, X. Xiao, and S. Zhou, "A Modeling and Experimental Study on the Growth of VCSEL Materials Using an 8 × 6 Inch Planetary MOCVD Reactor," *Coatings 2020, Vol. 10, Page 797*, vol. 10, no. 8, p. 797, Aug. 2020, ISSN: 20796412. DOI: 10.3390/COATINGS10080797.

[88] P. M. Frijlink, "A new versatile, large size MOVPE reactor," *Journal of Crystal Growth*, vol. 93, no. 1-4, pp. 207–215, Jan. 1988, ISSN: 0022-0248. DOI: 10.1016/0022-0248(88)90529-5.

[89] J. Wang, S. Tan, H. Liu, B. Li, Y. Hu, a. Jun Wang, R. Zhao, X. Xiao, Y. Cheng, Y. Guo, W. Zhao, L. Zhang, P. Miao, a. Guo, G. Deng, H. Yang, H. Zhou, H. Zhang, and X. Liao, "Volume manufacturing of high-power diode lasers using 6" wafers," in *High-Power Diode Laser Technology XX*, vol. 11983, SPIE, Mar. 2022, pp. 34–42, ISBN: 9781510648371. DOI: 10.1117/12.2610727.

[90] B. Depuydt, A. Theuwis, and I. Romandic, "Germanium: From the first application of Czochralski crystal growth to large diameter dislocation-free wafers," *Materials Science in Semiconductor Processing*, vol. 9, no. 4-5, pp. 437–443, Aug. 2006, ISSN: 1369-8001. DOI: 10.1016/J.MSSP.2006.08.002.

[91] S. J. Gillgrass, C. P. Allford, T. Peach, J. Baker, A. D. Johnson, J. I. Davies, A. M. Joel, S. Shutts, and P. M. Smowton, "Impact of thermal oxidation uniformity on 150 mm GaAs- and Ge-substrate VCSELs," *Journal of Physics D: Applied Physics*, vol. 56, no. 15, p. 154 002, Mar. 2023, ISSN: 0022-3727. DOI: 10.1088/1361-6463/ACC040.

[92] K. D. Choquette, D. A. Richie, and R. E. Leibenguth, "Temperature dependence of gain-guided vertical-cavity surface emitting laser polarization," *Applied Physics Letters*, vol. 64, no. 16, pp. 2062–2064, Apr. 1994, ISSN: 00036951. DOI: 10.1063/1.111737.

[93] M. Grabherr, B. Weigl, G. Reiner, R. Michalzik, M. Miller, and K. J. Ebeling, "High power top-surface emitting oxide confined vertical-cavity laser diodes," *Electronics Letters*, vol. 32, no. 18, pp. 1723–1724, 1996, ISSN: 00135194. DOI: 10.1049/el:19961155.

[94] F. A. Kish, S. J. Caracci, N. Holonyak, J. M. Dallesasse, K. C. Hsieh, M. J. Ries, S. C. Smith, and R. D. Burnham, "Planar native-oxide index-guided AlxGa1xAs-

GaAs quantum well heterostructure lasers," *Applied Physics Letters*, vol. 59, no. 14, p. 1755, Aug. 1998, ISSN: 0003-6951. DOI: 10.1063/1.106240.

[95] K. D. Choquette, K. M. Geib, H. C. Chui, H. Q. Hou, and R. Hull, "Selective oxidation of buried AlGaAs for fabrication of vertical-cavity lasers," *Materials Research Society Symposium - Proceedings*, vol. 421, no. 1, pp. 53–61, Feb. 1996, ISSN: 02729172. DOI: 10.1557/PROC-421-53/METRICS.

[96] K. D. Choquette, W. W. Chow, G. R. Hadley, H. Q. Hou, and K. M. Geib, "Scalability of small-aperture selectively oxidized vertical cavity lasers," *Applied Physics Letters*, vol. 70, no. 7, pp. 823–825, Feb. 1997, ISSN: 00036951. DOI: 10.1063/1.118234.

[97] J. L. Jewell, J. P. Harbison, A. Scherer, Y. H. Lee, and L. T. Florez, "Vertical-Cavity Surface-Emitting Lasers : Design, Growth, Fabrication, Characterization," Tech. Rep. 6, 1991.

[98] T. Tanigawa, T. Onishi, S. Nagai, and T. Ueda, "12.5-Gbps operation of 850-nm vertical-cavity surface-emitting lasers with reduced parasitic capacitance by BCB planarization technique," *IEEE Journal of Quantum Electronics*, vol. 42, no. 8, pp. 785–790, Aug. 2006, ISSN: 00189197. DOI: 10.1109/JQE.2006.878186.

[99] a. Ludovic Marigo-Lombart, J.-B. Doucet, A. Lecestre, B. Reig, B. Rousset, H. Thienpont, K. Panajotov, G. Almuneau, and L. Marigo-Lombart, "Self-aligned BCB planarization method for high-frequency signal injection in a VCSEL with an integrated modulator," *https://doi.org/10.1117/12.2227529*, vol. 9892, pp. 272–280, Apr. 2016, ISSN: 1996756X. DOI: 10.1117/12.2227529.

[100] B. Dayal Padullaparthi, J. A. Tatum, and K. Iga, "Appendix C: Wafer Process Engineering," *VCSEL Industry*, pp. 235–244, Nov. 2021. DOI: 10.1002/9781119782223.APP3.

[101] L. Marigo-Lombart, C. Viallon, A. Rumeau, A. Arnoult, A. Lecestre, L. Mazenq, A. Ghannam, H. Thienpont, K. Panajotov, and G. Almuneau, "Electro-Absorption

Modulator Vertically Integrated on a VCSEL: Microstrip-Based High-Speed Electrical Injection on Top of a BCB Layer," *Journal of Lightwave Technology*, vol. 37, no. 15, pp. 3861–3868, Aug. 2019, ISSN: 15582213. DOI: 10.1109/JLT.2019.2921806.

[102] D. Naidu, "Characterisation of lateral carrier out-diffusion and surface recombination in ridge waveguide devices -ORCA," Ph.D. dissertation, 2009.

[103] L. A. Coldren, S. W. Corzine, and M. L. Mašanović, "Gain and Current Relations," *Diode Lasers and Photonic Integrated Circuits*, pp. 157–246, Feb. 2012. DOI: 10.1002/9781118148167.CH4.

[104] J. Baker, S. Gillgrass, C. Allford, T. Peach, C. Hentschel, T. Sweet, J. I. Davies, S. Shutts, and P. Smowton, "VCSEL Quick Fabrication for Assessment of Large Diameter Epitaxial Wafers," *IEEE Photonics Journal*, 2022, ISSN: 19430655. DOI: 10.1109/JPHOT.2022.3169032.

[105] G. Giaretta, M. Y. Li, G. S. Li, W. Yuen, and C. J. Chang-Hasnain, "A novel 4 × 8 single-mode independently addressable oxide-isolated VCSEL array," *IEEE Photonics Technology Letters*, vol. 9, no. 9, pp. 1196–1198, Sep. 1997. DOI: 10.1109/68.618475.

[106] C. L. Chua, R. L. Thornton, and D. W. Treat, "Planar laterally oxidized vertical-cavity lasers for low-threshold high-density top-surface-emitting arrays," *IEEE Photonics Technology Letters*, vol. 9, no. 8, pp. 1060–1062, Aug. 1997. DOI: 10.1109/68.605499.

[107] K. M. Geib, K. D. Choquette, A. A. Allerman, R. D. Briggs, and J. J. Hindi, "Comparison of fabrication approaches for selectively oxidized VCSEL arrays," in *Vertical-Cavity Surface-Emitting Lasers IV*, vol. 3946, SPIE, May 2000, pp. 36–40. DOI: 10.1117/12.384385.

[108] C. L. Chua, R. L. Thornton, D. W. Treat, and R. M. Donaldson, "Independently addressable VCSEL arrays on 3-μm pitch," *IEEE Photonics Technology Letters*, vol. 10, no. 7, pp. 917–919, Jul. 1998, ISSN: 10411135. DOI: 10.1109/68.681269.

[109] Y. Hao, G. Liu, Y. Feng, L. Hou, C. Yan, Y. Zhao, and Y. Wang, "Optimal design for improving performance of VCSELs," *2010 Academic Symposium on Optoelectronics and Microelectronics Technology and 10th Chinese-Russian Symposium on Laser Physics and Laser Technology, RCSLPLT/ASOT 2010*, pp. 93–95, 2010. DOI: 10.1109/RCSLPLT.2010.5615393.

[110] R. E. Williams, *Gallium arsenide processing techniques*. Artech House, 1984, p. 406, ISBN: 0890061521.

[111] P. Arivazhagan, S. S. Bhattacharya, and K. Baskar, "Circular Transmission Line Measurement (CTLM) Studies on Epitaxial Layers of AlGaN," *Materials Today: Proceedings*, vol. 5, no. 3, pp. 10 110–10 117, Jan. 2018, ISSN: 2214-7853. DOI: 10.1016/J.MATPR.2017.11.007.

[112] P. D. Berger, C. Bru, T. Benyattou, G. Guillot, A. Chenevas-Paule, L. Couturier, and P. Grosse, "Investigations of vertical cavity surface emitting laser by photoreflectance spectroscopy," *Applied Physics Letters*, p. 4, 1995, ISSN: 00036951. DOI: 10.1063/1.116753.

[113] J. Baker, C. P. Allford, S. Gillgrass, T. Peach, J. Meiklejohn, C. Hentschel, W. Meredith, D. Powell, T. Sweet, M. Haji, J. I. Davies, S. Shutts, and P. M. Smowton, "VCSEL quick fabrication of 894.6 nm wavelength epi-material for miniature atomic clock applications," *IET Optoelectronics*, vol. 17, no. 1, pp. 24–31, Feb. 2023, ISSN: 1751-8776. DOI: 10.1049/OTE2.12082.

[114] J. Baker, C. P. Allford, S.-J. Gillgrass, R. Forrest, D. G. Hayes, J. Nabialek, C. Hentschel, J. I. Davies, S. Shutts, and P. M. Smowton, "Quick Fabrication VCSELs for Characterisation of Epitaxial Material," *Applied Sciences 2021, Vol. 11, Page 9369*, vol. 11, no. 20, p. 9369, Oct. 2021. DOI: 10.3390/APP11209369.

[115] G. Lafleur, G. Almuneau, A. Arnoult, H. Camon, and S. Calvez, "Anisotropy in the wet thermal oxidation of AlGaAs: influence of process parameters," 2018. DOI: 10.1364/OME.8.001788.

[116] K. D. Choquette, G. Hasnain, Y. H. Wang, J. D. Wynn, R. S. Freund, A. Y. Cho, and R. E. Leibenguth, "GaAs Vertical-Cavity Surface Emitting Lasers Fabricated by Reactive Ion Etching," *IEEE Photonics Technology Letters*, vol. 3, no. 10, pp. 859–862, 1991, ISSN: 19410174. DOI: 10.1109/68.93241.

[117] M. Ogura and H. C. Hsieh, "Effect of surface recombination velocity on the threshold current and differential quantum efficiency of the surface-emitting laser diode," *IEEE Journal of Quantum Electronics*, vol. 32, no. 4, pp. 597–606, Apr. 1996, ISSN: 00189197. DOI: 10.1109/3.488832.

[118] G. M. Yang, M. H. MacDougal, V. Pudikov, and P. D. Dapkus, "Influence of Mirror Reflectivity on Laser Performance of Very-Low-Threshold Vertical-Cavity Surface-Emitting Lasers," *IEEE Photonics Technology Letters*, vol. 7, no. 11, pp. 1228–1230, 1995, ISSN: 19410174. DOI: 10.1109/68.473454.

[119] D. K. Serkland, K. M. Geib, G. M. Peake, R. Lutwak, A. Rashed, M. Varghese, G. Tepolt, and M. Prouty, "VCSELs for atomic sensors," in *Vertical Cavity Surface Emitting Lasers XI*, vol. 6484, SPIE, Feb. 2007, pp. 48–57, ISBN: 0819465976. DOI: 10.1117/12.715077.

[120] D. Zaouris, M. Knapp, M. Haji, P. Gill, S. Shutts, P. M. Smowton, I. Eddie, A. Mckee, W. Meredith, and D. Powell, "MacV: VCSELs For Miniature Atomic Clocks," *IFCS/EFTF 2019 - Joint Conference of the IEEE International Frequency Control Symposium and European Frequency and Time Forum, Proceedings*, Apr. 2019. DOI: 10.1109/FCS.2019.8856005.

[121] B. D. Padullaparthi, J. A. Tatum, and K. Iga, "VCSEL Industry: Communication and Sensing," *VCSEL Industry: Communication and Sensing*, pp. 1–312, Jan. 2021. DOI: 10.1002/9781119782223.

[122] M. Dummer, K. Johnson, S. Rothwell, K. Tatah, M. M. Hibbs-Brenner Dummer, and M. Hibbs-Brenner, "The role of VCSELs in 3D sensing and LiDAR," in *Optical Interconnects XXI*, vol. 11692, SPIE, Mar. 2021, pp. 42–55, ISBN: 9781510642195. DOI: 10.1117/12.2577885.

[123] G. B. Stringfellow, "Specific Materials," *Organometallic Vapor-Phase Epitaxy*, pp. 391–484, Jan. 1999. DOI: 10.1016/B978-012673842-1/50011-9.

[124] C. J. Chang-Hasnain, C. E. Zah, G. Hasnain, J. P. Harbison, L. T. Florez, N. G. Stoffel, and T. P. Lee, "Effect of operating electric power on the dynamic behavior of quantum well vertical-cavity surface-emitting lasers," *Applied Physics Letters*, vol. 58, no. 12, pp. 1247–1249, Mar. 1991, ISSN: 0003-6951. DOI: 10.1063/1.104325.

[125] G. Hasnain, K. Tai, Y. H. Wang, R. J. Fischer, J. D. Wynn, B. Weir, N. K. Dutta, A. Y. Cho, and L. Yang, "Performance of Gain-Guided Surface Emitting Lasers with Semiconductor Distributed Bragg Reflectors," *IEEE Journal of Quantum Electronics*, vol. 27, no. 6, pp. 1377–1385, 1991, ISSN: 15581713. DOI: 10.1109/3.89954.