A Differential Combiner for Quasi-Complete Cancellation of Output Capacitance in mm-Wave Power Amplifiers With High-Q Devices

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***Abstract*—This paper proposes a new and simpler methodology to combine two transistors for high-frequency applications. By using a $\lambda/4$ transmission line to connect the drain pads of the identical transistors, the line characteristic impedance can be chosen to almost perfectly cancel out the output capacitance at the design frequency f_0. When the combined network is loaded with a real impedance, the real part of the impedance seen at each of the intrinsic devices is twice the value of that load, while the imaginary part is exactly zero for one of the transistors, and depends on f_0 for the other. This imaginary part is inversely proportional to f_0 and becomes relatively small with high Q-factor (defined as product between optimum intrinsic load and output capacitance susceptance) devices at the frequency of operation (f_0). To demonstrate the effectiveness of this methodology, a 28 GHz Doherty Power Amplifier (DPA) based on the NP15 Microwave Monolithic Integrated Circuit (MMIC) process from WIN Semiconductors, has been designed using the proposed combining method for the main and auxiliary branches. The continuous wave (CW) characterization of this amplifier shows competitive results, which are comparable with the state of the art in terms of efficiency, output power, gain and bandwidth. Over a band between 27.5 and 29.5 GHz, the obtained saturated output power is higher than 32 dBm. The power added efficiency (PAE) at 6 dB output back-off (OBO) is in the range of 21 to 24 %, while is from 24 to 34 % at saturation. The saturated gain is between 8 and 12 dB over the above mentioned band.**

***Index Terms*—Doherty, GaN, Millimeter-wave (mm-wave), power amplifiers (PAs), power combining.**

I. Introduction

In the ever-evolving landscape of wireless communications, the demand for high-performance millimeter-wave (mm-wave) Power Amplifiers (PAs) has surged exponentially. These PAs serve as pivotal components in next-generation communication systems, including 5G and beyond, automotive radar, and various emerging applications [1]–[3]. The relentless pursuit of higher data rates, extended coverage, and reduced latency necessitates mm-wave PAs that can deliver substantial output power. However, the transistor reduced periphery necessary to operate at very high frequencies makes it difficult to harness sufficient power with only one device. Therefore, it is imperative to explore device combining strategies that minimize additional losses which negatively affect both output power and efficiency.

The most common approaches for combining transistors are parallel and series (stacked) connections [4], [5]. The parallel connection, although seemingly straightforward, struggles to compensate for the reactive parasitic effects associated with the transistors. To address this issue, additional matching networks are often required, making the circuit more complex and potentially narrower in bandwidth [4], [6]. On the other hand, stacked cells offer a solution that can increase gain while reducing chip area. However, discrepancies often arise between schematic-level designs and electromagnetic (EM) simulations due to the persistent presence of crosstalk effects [4], [7]. Consequently, the only viable solution is a design process based on EM optimization, which can be a time-consuming trial-and-error endeavor.

This paper introduces a straightforward structure for combining two transistors and doubling the current delivered to the load. By employing a single-section $\lambda/4$ transformer as a connection between the drains of the transistors, this combiner effectively compensates for the typical drain-to-source capacitance (C_{OUT}) at high design frequencies (f_0). Consequently, the transistors behave in first approximation as "current sources" when connected to the load, simplifying the design of mm-wave PAs. The methodology is utilized to design and fabricate a Doherty Power Amplifier (DPA) which is the preferred solution to improve average efficiency when using advanced modulation schemes, currently dominating the base-station market and being proposed also at mm-wave bands [8]–[14]. The design employed $4 \times 50\,\mu\mathrm{m}$ GaN-on-SiC devices, implemented on the NP15 process from WIN Semiconductors, resulting in a 27.5-29.5 GHz Microwave Monolithic Integrated Circuit (MMIC) DPA with more than 32 dBm of output power. At a 6 dB of output back-off (OBO), the power added efficiency (PAE) ranged from 21 to 24 %, and it was in the range of 24 to 34 % at saturation. These results are competitive with the state-of-the-art of DPAs at this frequency range [8]–[14].

The paper unfolds as follows. Sections II and III introduce the novel combining circuit methodology and its application to PA design. Section IV presents a bandwidth analysis of the structure when applied to a specific PA design, at three

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different design frequencies. Sections V and VI puts the methodology into practice by showing the design of the 28 GHz MMIC DPA and its simulation, while Section VII shows the competitive experimental results in terms of efficiency, output power, gain, and bandwidth. Finally, in section VIII, some conclusions are drawn.

II. Novel Combining Circuit

Given the various drawbacks associated with the traditional approaches to combining transistors in high-frequency applications, there arises a compelling need to explore novel solutions. Fig. 1 illustrates a new proposal along with its equivalent circuit. In this representation, the transistor outputs, assumed here for convenience as Field-Effect Transistor (FET), function as current generators, while their parasitic output effects are encapsulated in first approximation by the equivalent capacitance denoted as C_{OUT} [15]–[18]. For the sake of simplicity in the subsequent analysis, both devices are presumed to be identical and operating within the linear region. The initial step involves an examination of the equivalent network and the establishment of conditions that render it an effective combining structure.

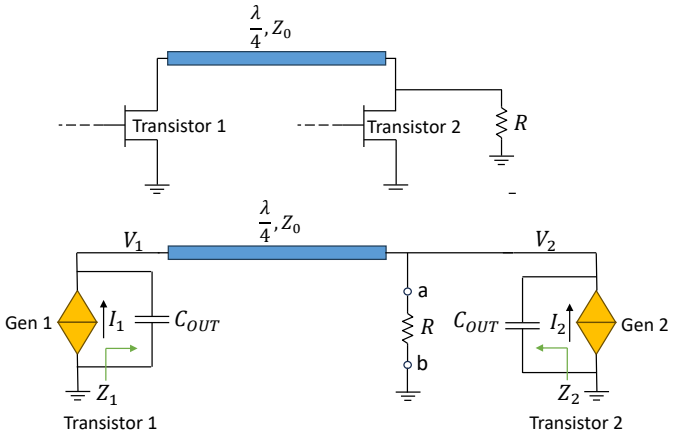

Fig. 1. Proposed two-transistor combiner and its equivalent circuit.

At the design frequency f_0, the combiner structure, as depicted in Fig. 2, can be represented by its $\mathbf{Z}$ matrix, obtained as transformation from the $\mathbf{ABCD}$ matrix which is the multiplication of four elements' $\mathbf{ABCD}$ matrices as follows:

$$\mathbf{ABCD}_{\mathrm{T}} = \begin{bmatrix} 1 & 0 \\ Y_{\mathrm{C}} & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_0 \\ j\frac{1}{Z_0} & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{1}{R} & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_{\mathrm{C}} & 1 \end{bmatrix}, \quad (1)$$

where the inner matrices represent the $\mathbf{ABCD}$ matrix of the quarter-wave line and the resistor load R, respectively, while the outer matrices correspond to the shunt capacitances on each side, where $Y_{\mathrm{C}} = jB_{\mathrm{C}} = j\omega_0 C_{\mathrm{OUT}}$ and $\omega_0 = 2\pi f_0$. By multiplying the matrices the result is:

$$\mathbf{ABCD}_{\mathrm{T}} = \begin{bmatrix} -B_{\mathrm{C}}Z_0 + j\frac{Z_0}{R} & jZ_0 \\ j\left(\frac{1}{Z_0} - B_{\mathrm{C}}^2 Z_0\right) - \frac{B_{\mathrm{C}}Z_0}{R} & -B_{\mathrm{C}}Z_0 \end{bmatrix}. \quad (2)$$

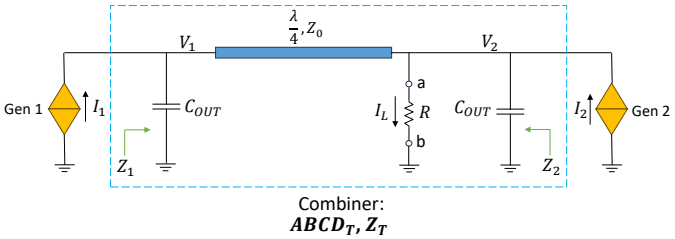

Fig. 2. Combiner definition.

Utilizing (2), we can calculate the $\mathbf{Z}$ matrix of the combiner through the conversion equation as:

$$\begin{aligned} \mathbf{Z}_{\mathrm{T}} &= \frac{1}{C}\begin{bmatrix} A & AD - BC \\ 1 & D \end{bmatrix} \\ &= \frac{1}{C}\begin{bmatrix} -B_{\mathrm{C}}Z_0 + j\frac{Z_0}{R} & 1 \\ 1 & -B_{\mathrm{C}}Z_0 \end{bmatrix} \end{aligned} \quad (3)$$

with

$$C = -B_{\mathrm{C}}\frac{Z_0}{R} + j\left(\frac{1}{Z_0} - B_{\mathrm{C}}^2 Z_0\right). \quad (4)$$

Assuming the condition where the characteristic impedance of the transmission line matches the impedance magnitude of the capacitors, i.e.,

$$Z_0 = \frac{1}{\omega_0 C_{\mathrm{OUT}}} \quad (5)$$

then $\mathbf{Z}_{\mathrm{T}}$ simplifies to

$$\mathbf{Z}_{\mathrm{T}} = R\begin{bmatrix} 1 - j\frac{1}{\omega_0 C_{\mathrm{OUT}} R} & -1 \\ -1 & 1 \end{bmatrix} \quad (6)$$

Having obtained the impedance network of the combiner, we can now solve the circuit by injecting the currents from the equivalent sources representing the transistors. The voltages at current generators reference planes V_1 and V_2 can be expressed as:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \mathbf{Z}_{\mathrm{T}} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (7)$$

which means

$$V_2 = R(I_2 - I_1). \quad (8)$$

Hence, the current passing through the load R is given by

$$I_{\mathrm{L}} = \frac{V_2}{R} = I_2 - I_1. \quad (9)$$

There are two important observations that can be made here. First, the current I_{L} is independent of R, meaning that the combiner network functions as an equivalent current generator or, seen from another point of view, that the Norton impedance seen from terminals a and b in Fig.2 is infinite. Additionally, (9) indicates that the output power is maximised when the transistors are operated in a differential way:

$$I_1 = -I_2, \quad (10)$$

which means

$$I_{\mathrm{L}} = 2I_2. \quad (11)$$

III. Analysis of Ports Terminations

Thus far, this combining methodology appears promising for small signal amplifiers, where the devices are expected to operate in a linear region. However, further analysis can be undertaken to demonstrate its applicability in large signal amplifiers.

In particular, obtaining the optimum fundamental impedance at the current generator reference plane is the key target to achieve high power and efficiency [19], [20]. This impedance delineates the saturation conditions of the transistors and, to a large extent, the voltage and current intrinsic drain waveforms.

By using (7) and the conditions specified in (5) and (10), we can determine the voltages at each current source reference plane:

$$\begin{cases} V_1 = \left(2R - j\frac{1}{B_C}\right) I_1 \\ \\ V_2 = 2RI_2 \end{cases} \tag{12}$$

Thus, the intrinsic impedance Z_1 and Z_2 for each generator in Fig. 2 are as follows:

$$\begin{cases} Z_1 = 2R - j\frac{1}{B_C} \\ \\ Z_2 = 2R \end{cases} \tag{13}$$

From (13), it is evident that Z_2 is real-valued and twice the load R. Therefore, the transistor can be optimally matched to its intrinsic optimum, i.e. $Z_2 = R_{\mathrm{OPT}}$, by selecting a load such that $R_{\mathrm{OPT}} = 2R$.

For Z_1, which can be re-written as:

$$Z_1 = 2R - j\frac{1}{2\pi f C_{\mathrm{OUT}}} \tag{14}$$

there is an additional imaginary part that needs to be considered. If the magnitude of the real part is significantly greater than the magnitude of the imaginary part (i.e., $R_{\mathrm{OPT}} \gg 1/B_{\mathrm{C}}$), then this imaginary part can be tolerated with minimal impact on output power and efficiency. This condition, equivalent to assuming a high Q-factor for the transistor output circuit, which is defined as $Q = R_{\mathrm{OPT}} B_{\mathrm{C}}$, is very common in mm-wave PA applications using GaN-based devices, which have a significant output capacitance that would be difficult to compensate for, and a relatively large intrinsic optimum real load.

To evaluate the impact of the imaginary part of Z_1, we can define the intrinsic reflection coefficient as:

$$\Gamma_1 = \frac{Z_1 - R_{\mathrm{OPT}}}{Z_1 + R_{\mathrm{OPT}}}. \tag{15}$$

which gives an idea of the accuracy of the matching when using the proposed combiner with a certain transistor technology at a given frequency band.

In summary, for high-Q devices (i.e., $R_{\mathrm{OPT}} \gg 1/B_{\mathrm{C}}$), and assuming a combiner line with characteristic impedance $Z_0 = 1/B_{\mathrm{C}}$, the impedance matrix $\mathbf{Z}_{\mathrm{T}}$ of the combiner can be approximated as:

$$\mathbf{Z}_{\mathrm{T}} \simeq R \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{16}$$

indicating a differential combiner with the ability of compensating for the output capacitance.

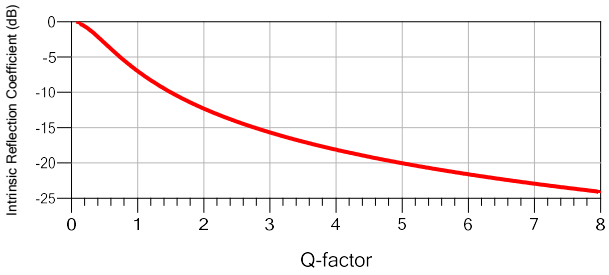

Fig. 3. Intrinsic Reflection Coefficient as a function of Q factor.

Fig. 3 shows how $|\Gamma_1|$ decreases very rapidly with the increase of the Q-factor.

IV. Bandwidth Analysis

In order to assess the potential bandwidth of the proposed combiner, let's estimate the output power and efficiency as a function of frequency for a power amplifier designed using it. The amplifier incorporates transistors with specific characteristics: $C_{\mathrm{OUT}} = 0.1\,\mathrm{pF}$, $V_{\mathrm{k}} = 4\,\mathrm{V}$, and $I_{\mathrm{MAX}} = 0.2\,\mathrm{A}$. These values, typical for a $4 \times 50\,\mu\mathrm{m}$ device in the NP15 process from WIN Semiconductors Corp, are utilized alongside a drain bias voltage of 20 V and a class B bias condition to simplify calculations. For this transistor $R_{\mathrm{opt}} = 160\,\Omega$ and therefore $R = 80\,\Omega$ (see Fig. 1).

Within this framework, we assume that the combiner cell saturates when at least one of the transistors reaches voltage or current saturation for a particular input drive level. For simplicity, the amplitude of the fundamental voltage and current at the current generator reference plane of each transistor is limited to $16\,\mathrm{V}$ (i.e. $V_{\mathrm{DD}} - V_{\mathrm{k}}$) and $0.1\,\mathrm{A}$ (i.e. $I_{\mathrm{MAX}}/2$), respectively. In essence, the combined cell is here considered saturated when at least one transistor exceeds its maximum fundamental voltage or current.

To analyze this condition, a simulation has been conducted assuming that each device operates as a current source with its output capacitance in parallel. In Fig. 4a, the estimated saturated output power and efficiency for $f_0 = 28\,\mathrm{GHz}$ are presented, while Figures 4b and 4c display the associated intrinsic drain voltages and currents, respectively. Similar estimations were performed for $f_0 = 14\,\mathrm{GHz}$ and $f_0 = 56\,\mathrm{GHz}$, and their respective efficiency, output power, drain voltages, and currents are depicted in Figures 5 and 6. For each case, the values of Z_0 were calculated using (5).

The theoretical efficiency and output power of a class B PA with a knee voltage of $4\,\mathrm{V}$ and maximum current twice the one for the aforementioned device, assuming a lossless output matching network, are $62.8\,\%$ and $32\,\mathrm{dBm}$, respectively. Referring to Fig. 4a and Fig. 6a, we observe that the output power and efficiency closely align with these values at the design frequency, particularly at the highest design frequency, $f_0 = 56\,\mathrm{GHz}$. This underscores the effectiveness

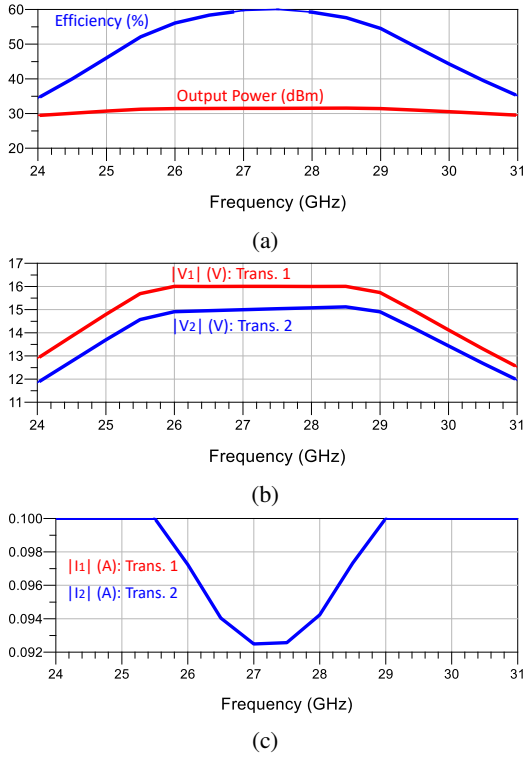

Fig. 4. Bandwidth analysis for a $f_0 = 28\,\text{GHz}$ PA using the proposed combiner ($Z_0 = 56.8\,\Omega$): estimation of (a) output power and efficiency, (b) fundamental drain voltages and (c) fundamental drain currents.

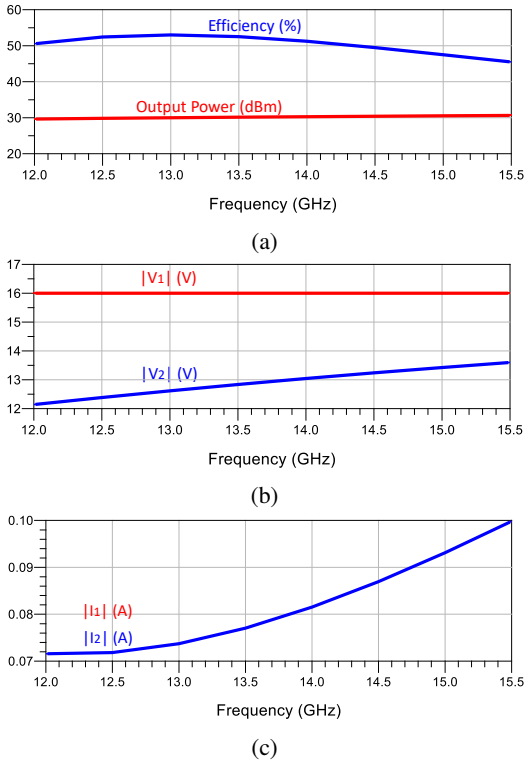

Fig. 5. Bandwidth analysis for a $f_0 = 14\,\text{GHz}$ PA using the proposed combiner ($Z_0 = 113.7\,\Omega$): estimation of (a) output power and efficiency, (b) fundamental drain voltages and (c) fundamental drain currents.

of the proposed combiner for high frequency applications. Additionally, the bandwidth assessment can be inferred from these figures. In both cases, an efficiency higher than 50 % is sustained approximately across a 4 GHz bandwidth. However, for $f_0 = 14\,\text{GHz}$, depicted in Fig. 5a, the output power and efficiency deteriorates due to the increased value of the imaginary part of Z_1, as expressed in (13).

V. MMIC DPA DESIGN

The proposed combiner is applied to the design of a DPA at 28 GHz using the NP15 process from WIN Semiconductors Corp., which is a GaN High Mobility Transistor (HEMT) on SiC MMIC process with 0.15 μm gate length. The device chosen for the design is the $4 \times 50\,\mu\text{m}$, which has an output capacitance $C_{\text{OUT}} = 0.1\,\text{pF}$, and an optimum load for maximum power of $160\,\Omega$ when biased at 20 V. This means that the proposed combiner will use a $\lambda/4$ transmission line with impedance:

$$Z_0 = \frac{1}{B_{\text{C}}} = \frac{1}{2\pi f C_{\text{OUT}}} \simeq 57\,\Omega. \tag{17}$$

The quality factor of the selected transistor is:

$$Q = R_{\text{OPT}} B_{\text{C}} = 2.8 \tag{18}$$

which, according to Fig. 3, will lead to a matching for Z_1 better than -15 dB at 28 GHz.

To summarize, at 28 GHz, the combiner will lead to $Z_1 = (160 + j56.8)\ \Omega$ and $Z_2 = 160\,\Omega$. Although the imaginary part of Z_1 seems to be comparable with its real part, from the results estimated in section IV for $f_0 = 28\,\text{GHz}$, it can be observed that its impact on the cell efficiency and power is not very significant (see Fig. 4a), and thus, it was decided to tolerate it.

The structure of the proposed DPA is depicted in Fig. 7, showing that both main and auxiliary stages use the proposed combiner. Since it leads to an equivalent current source with no reactive elements, a DPA impedance inverter of impedance Z_{II} can be connected directly at the output of the main branch without extra matching or offset lines, by choosing:

$$Z_{\text{II}} = \frac{R_{\text{opt}}}{2}, \tag{19}$$

while the common load at the output of the DPA R_{L} becomes:

$$R_{\text{L}} = \frac{R_{\text{opt}}}{4}. \tag{20}$$

For the selected transistor, these result in $Z_{\text{II}} = 80\,\Omega$ and $R_{\text{L}} = 40\,\Omega$. At the output of the auxiliary branch, a $\lambda/2$ transmission line is used instead of connecting directly to the auxiliary combiner as this solution offers some flexibility in terms of impedance matching that can improve performance over frequency [21]. The characteristic impedance of this line is therefore carefully tuned for bandwidth considerations.

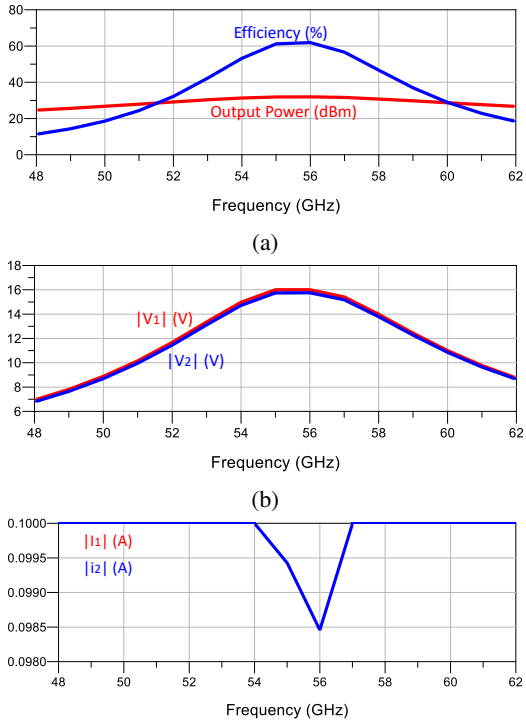

Fig. 6. Bandwidth analysis for a $f_0 = 56\,\text{GHz}$ PA using the proposed combiner ($Z_0 = 28.4\,\Omega$): estimation of (a) output power and efficiency, (b) fundamental drain voltages and (c) fundamental drain currents.

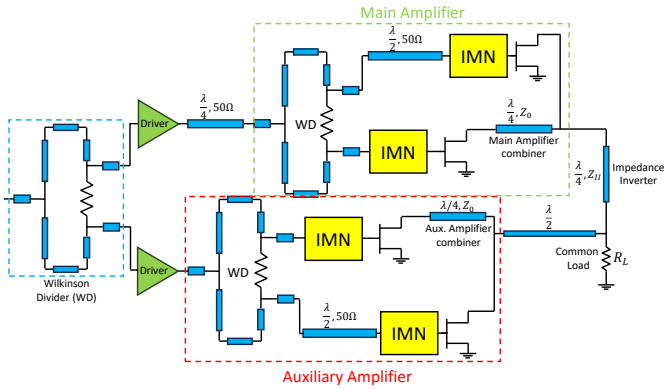

Fig. 7. Structure of the designed DPA using the proposed combiner.

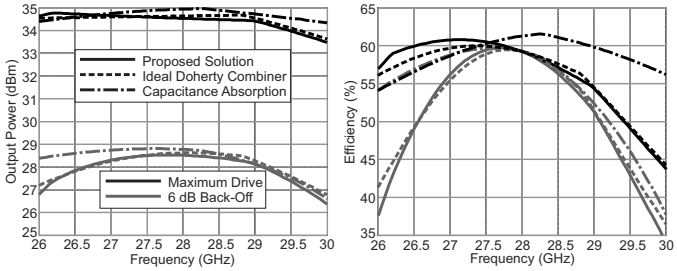

Fig. 8. Simplified prediction [22] of maximum drive (black lines) and 6 dB back-off (grey lines) performance of output power (left) and efficiency (right). Comparing the proposed solution (solid lines) with the differential combiner + frequency independent Doherty combiner (dotted lines) and the capacitance absorption method of [22] (dot-dashed line).

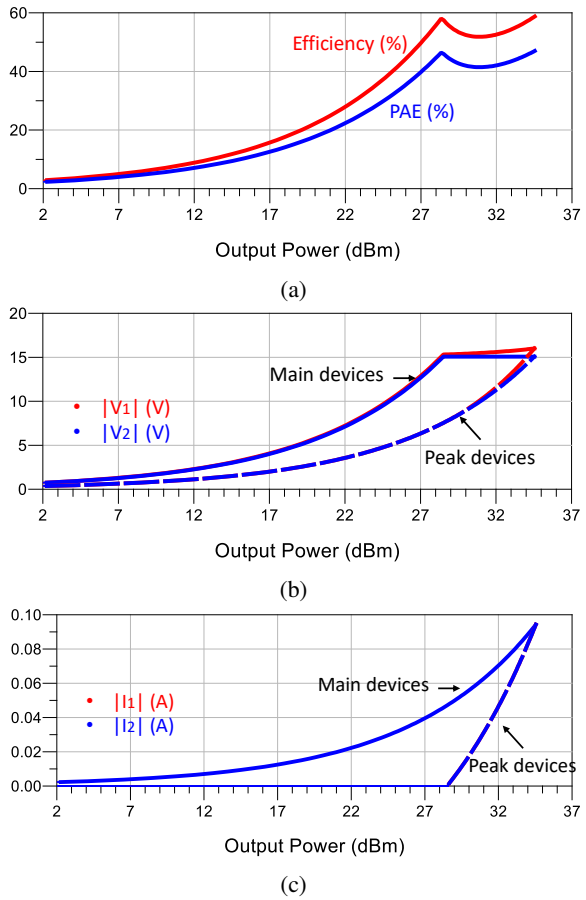

Fig. 9. Performance prediction for the designed DPA at 28 GHz. Efficiency and PAE (a), fundamental drain voltages (b), and fundamental drain currents (c).

To understand if the Doherty combiner proposed could be improved in terms of bandwidth, a simplified method for bandwidth estimation [22] was used. An ideal Doherty combiner with a frequency independent impedance inverter was used as reference for comparison. The performance difference between the proposed Doherty combiner and the ideal one resulted negligible (see Fig. 8), meaning that the bandwidth of the Doherty is in this case limited by the differential combiner we propose for combining the transistor pairs. Another comparison was made with the use of capacitance absorption into the Doherty combiner, which is a commonly adopted technique to improve frequency response. In this case, the capacitance absorption, using the topology also proposed in [22] leads to slightly better performance compared to our proposed combiner (Fig. 8), but also to unpractical impedance levels around $5\,\Omega$ for the common load, and $10\,\Omega$ for the auxiliary $\lambda/2$ line, which

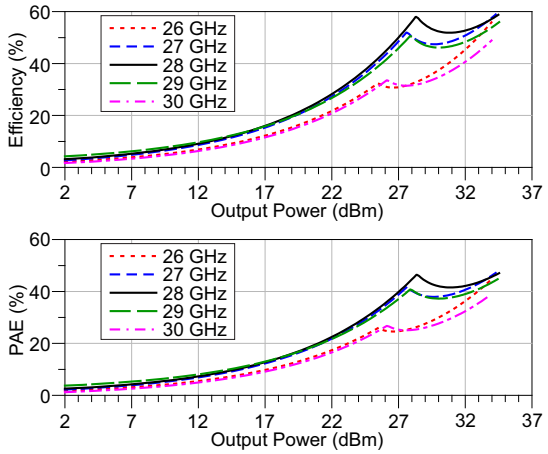

Fig. 10. Efficiency (top) and PAE (bottom) prediction for the designed DPA from 26 to 30 GHz.

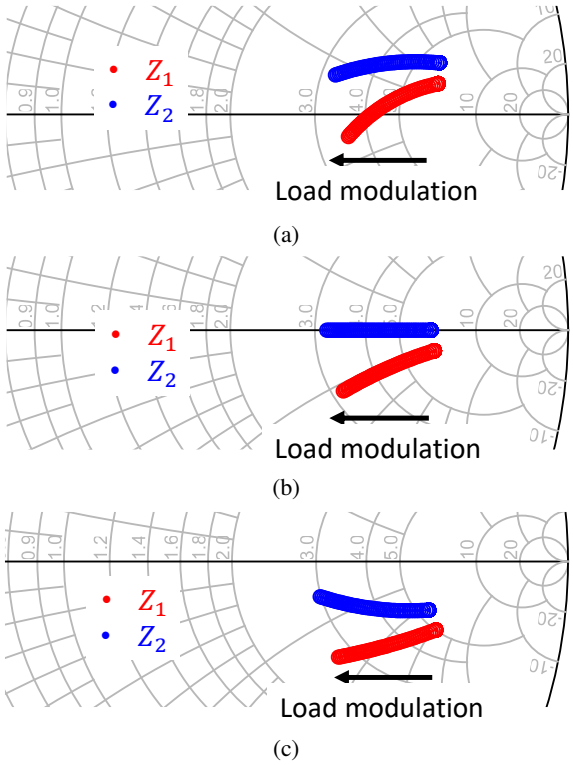

Fig. 11. Simulation of the load modulation effect for the designed DPA. 27 GHz (a), 28 GHz (b) and 29 GHz (c).

would be difficult to synthesize in an MMIC without leading to significant insertion loss and further bandwidth limitation.

Considering each transistor as a current source with its associated output capacitance C_{OUT}, an estimation of the efficiency profile for different frequencies around the design frequency $f_0 = 28\,\mathrm{GHz}$, for the designed DPA (excluding drivers), was performed. In this analysis, saturation is defined as occurring when at least one of the four devices (two of the main amplifier and two of the peak amplifier) exceeds its maximum drain voltage or current constraints, namely fundamental amplitude of 16 V and 0.1 A, respectively. To simplify the analysis, the peak amplifier cell is assumed to operate under class B conditions, switching on at the midpoint of the maximum driving level and increasing its drain currents continuously and twice as fast as the ones of the main cell. Fig.9 shows the estimated efficiency profiles, together with the drain voltages and currents for the main and peak devices at 28 GHz. Fig. 10 compares the efficiency and PAE prediction at 28 GHz with the prediction at 26, 27, 29 and 30 GHz. The PAE was estimated assuming cells of 7 dB of operative gain, which is roughly the expected gain for this transistor. Additionally, the estimated load modulation for the main cell devices are presented in Fig. 11 at 27 GHz, 28 GHz and 29 GHz. Finally, the ideal components used in the estimation process were transformed to real ones.

On the input side of the DPA, as shown in Fig. 7, the power division is achieved using a Wilkinson divider. Subsequently, a driver amplifier is employed in each branch to enhance the overall gain of the DPA with minimal impact on PAE [23]. These drivers also use the $4 \times 50\,\mu\mathrm{m}$ device. Additional Wilkinson dividers are utilized at the input of each combined stage, with the differential drive obtained by means of a $50\,\Omega$ $\lambda/2$ transmission line. The unconditional small-signal stability of each device is ensured by the inclusion of resistive networks at the input matching networks. To match the $50\,\Omega$ system impedance to R_{L}, a $\lambda/4$ transformer is employed.

The $\lambda/2$ transmission line at the output combiner of the auxiliary cell offers connection flexibility, with its characteristic impedance carefully tuned for bandwidth considerations.

The complete schematic of the DPA can be seen in Fig. 12.

VI. Simulations

The designed DPA, as shown in Fig. 12, was simulated using Keysight's Advanced Design System (ADS). Schematic and electromagnetic (EM) simulations were conducted to demonstrate the correct load modulation effects and define the expected results in terms of gain, efficiency, and output power. Fig. 13a presents the simulated values for these performance metrics as functions of frequency, while Fig. 13b provides a sample profile of gain and PAE versus output power at an in-band frequency.

For this purpose, a drain bias voltage of 20 V was used for each transistor, and a gate bias voltage of -1.8 V (corresponding to a drain current of 10% the maximum current, denoted as $0.1I_{\mathrm{MAX}}$) was applied to the drivers and main amplifier cell devices. In contrast, a gate bias voltage of -4.7 V was chosen to meet class C conditions for the auxiliary cell devices.

From Fig. 13a, a saturated output power between 32 dBm and 34 dBm is expected over the frequency band between 27.5 and 29.5 GHz. Within this band, a simulated PAE higher than 20 % at 6 dB OBO is obtained, and exceeding 35 % at saturation. The saturated gain is expected to be higher than 7 dB within this frequency range. Fig. 13b shows the simulation of a typical Doherty profile, demonstrating the application of the proposed combiner in load-modulated amplifiers.

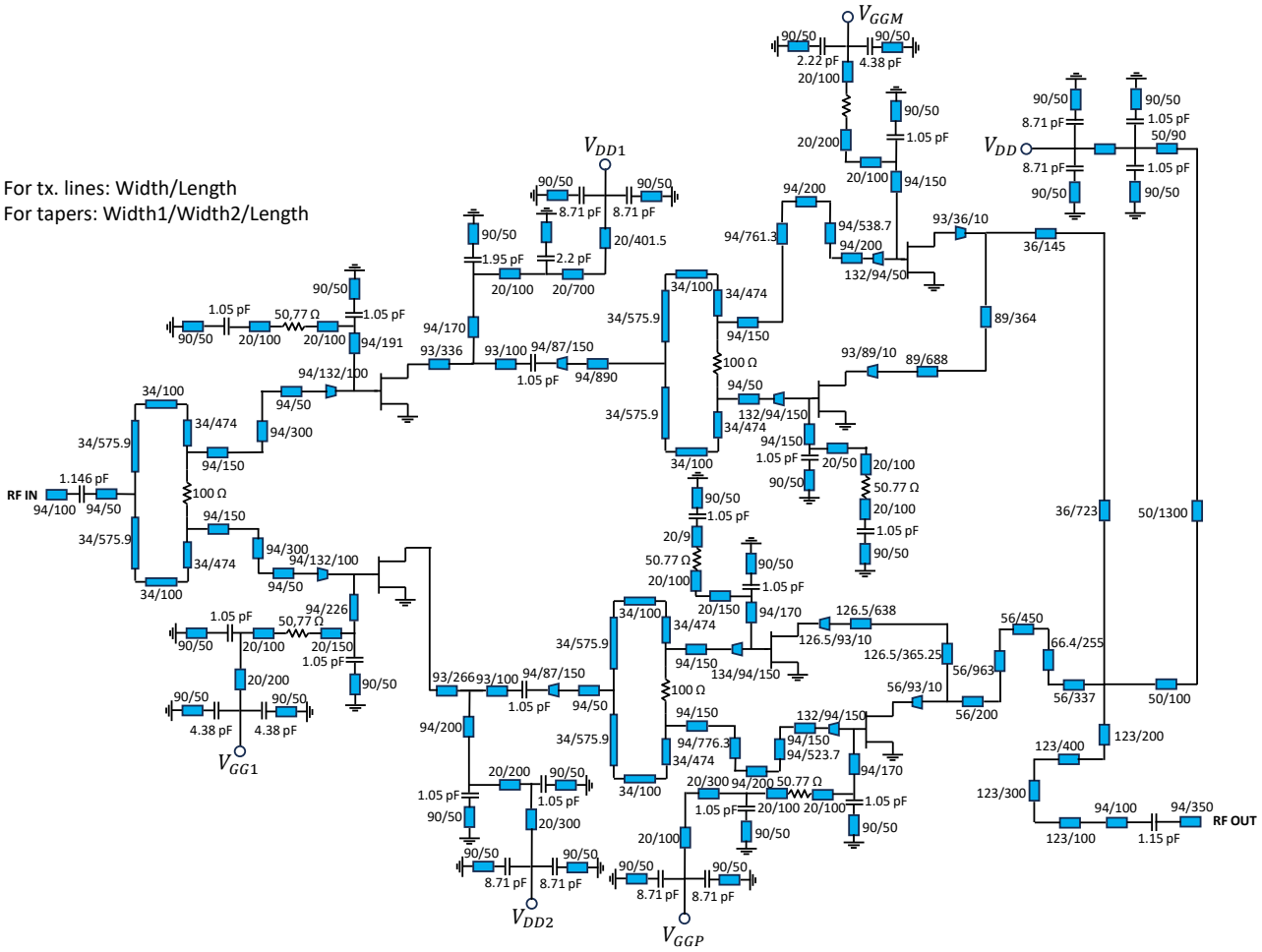

Fig. 12. Schematic of the designed DPA.

Additionally, the load modulation effect was simulated. Figures 14a, 14b, and 14c show the simulation of the estimated intrinsic impedance Z_1 and Z_2 at 27 GHz, 28 GHz and 29 GHz respectively, as seen at the current generator reference planes of each transistor comprising the main amplifier cell. As indicated by these figures, the load modulation closely matches the estimated behavior shown in Fig. 11. For an in-depth analysis, the impedance magnitudes $|Z_1|$ and $|Z_2|$ are simulated as functions of the output power, along with the magnitude of the intrinsic impedances of the auxiliary cell, here referred to as $|Z_3|$ and $|Z_4|$, at 28 GHz. It can be observed that load modulation starts at approximately 6 dB OBO. Notably, there is a difference between the impedance magnitudes, which is expected, partly due to the additional imaginary part as defined in (13).

VII. Characterisation

The fabricated MMIC, whose microscope picture is shown in Fig. 15, has been tested in continuous wave (CW) operation to determine the RF performance, in particular the output power, gain, and PAE profiles at both maximum output power and 6 dB OBO.

The MMIC samples have been mounted with silver epoxy on a small copper carrier alongside chip capacitors for bias-by pass (100 pF and 10 nF). Gold bond wires are used to connect the bias pads on the MMIC samples to the chip capacitors, and then to external printed circuit boards that use larger capacitor values for low-frequency by-pass. A probe station with Ground-Signal-Ground RF probes is used to connect the RF ports. The characterisation is performed using a Vector Network Analyzer (ZVA67 from Rohde & Schwarz) with external directional couplers.

In Fig. 16, we present the performance profiles obtained at various frequencies in the vicinity of 28 GHz. These measurements revealed a 6 dB OBO efficiency exceeding 20 % in the 27.5 to 29.5 GHz range, along with a saturation efficiency surpassing 24 %. The output power ranged from 32 to 33 dBm across the mentioned frequency band.

A comparison between simulations and measurements is provided in Fig. 17. Fig. 17a demonstrates a close agreement between measurements and simulations in terms of output power and gain. The measured PAE at 6-dB-OBO is also in close alignment with the simulations, with a difference of no more than 6 % over our band of interest. As shown

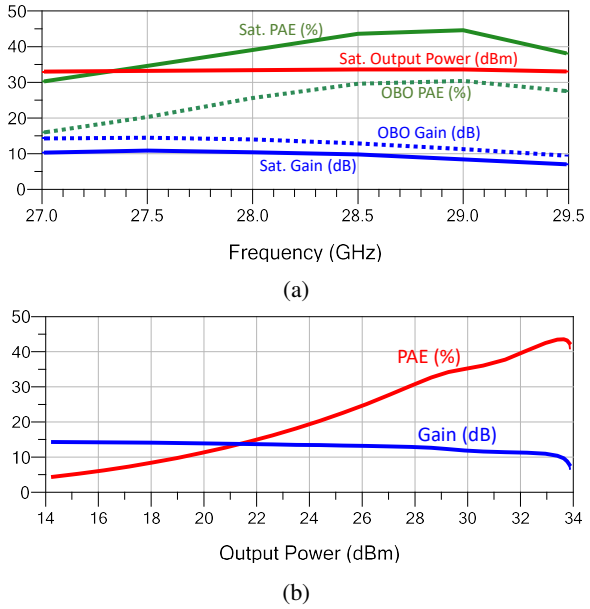

Fig. 13. CW simulations of the designed DPA. Saturated output power, saturated PAE, OBO PAE, saturated gain and OBO gain vs. frequency (a). PAE and gain vs. output power at 28.5 GHz (b).

in Fig. 17b, when considering the PAE at saturation, the simulations indicate a higher value, especially at the highest frequencies within the band, but it remains reasonably close. However, the difference between the simulated and measured saturated PAE at 28 GHz, which was the design frequency, does not exceed 6 %, as depicted in Fig. 17b.

Table I presents a comparison to some state-of-the-art DPAs, demonstrating competitive results for our proposal.

TABLE I
COMPARISON WITH STATE OF THE ART MMIC DPAS WITH SIMILAR FREQUENCY AND OUTPUT POWER RANGE

Ref	[8]	[9]	[10]	[12]	This work
BW (GHz)	24–28	28–29	24–28	28	**27.5–29.5**
PAE_{6dB} (%)	14–32	13–16	18.1–30.1	31	**21–24**
PAE_{sat} (%)	23–41	20–22	27.8–36.8	42	**24–34**
P_{OUT} (dBm)	34–36	34–34.3	35.4–36	26.5	**32–33**
S. Gain (dB)	11–13	8–12	8–11	11.8	**8–12**

The system level performance, in terms of average output power, average efficiency, linearity and linearize-ability was experimentally tested using the system level characterization setup at the Compound Semiconductor Applications Catapult (picture in Fig. 18), alongside the on-wafer large signal characterisation setup. The system level measurements were carried out using the Amplifier Testing tool from R&S that coordinates the signal source (SMW200A) and analyzer (FSW). The large signal system is a source-/load-pull system, used in this case to physically probe the devices and, thanks to the large signal calibration, provide an accurate measurement of the absolute power at the MMIC ports. The output from the system is connected to the FSW by an attenuator for protecting the FSW,

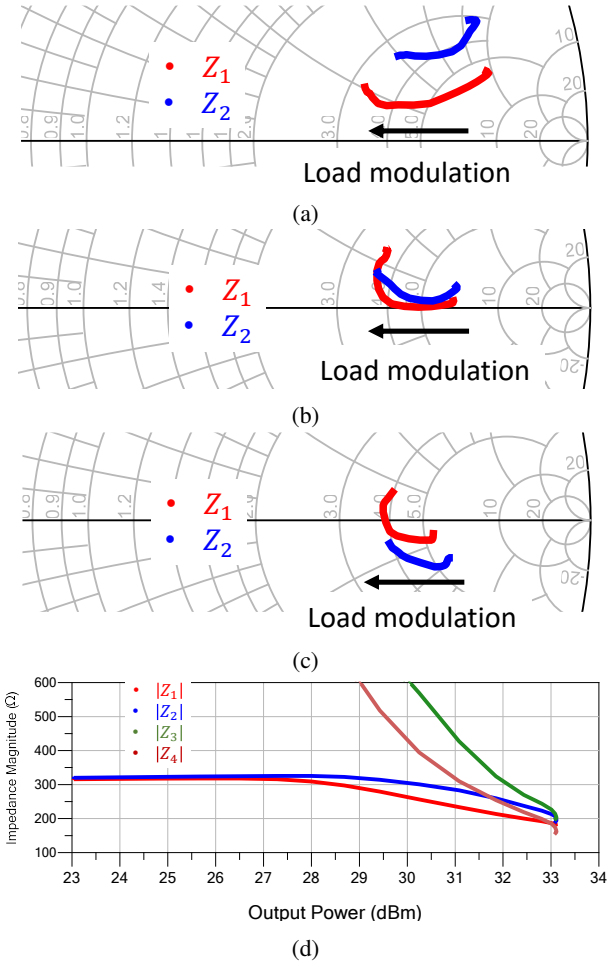

Fig. 14. Load modulation: simulation of Z_1 and Z_2 modulation effect at 27 GHz (a), 28 GHz (b) and 29 GHz (c), and simulation of main and peak amplifiers load modulation at 28 GHz (d).

unfortunately reducing the dynamic range of the measurement. The FSW measurement can be corrected using the calibrated measurement on the large-signal characterisation system by applying, frequency by frequency, a CW signal that is measured both by the FSW and the large-signal measurement system. A driver amplifier was used to drive the signal at the input of the DUT. Its distortion was tested and resulted negligible, i.e., below the dynamic range of the FSW. The test signal used was an example of 5G FR2 signal, with crest factor limited at 8 dB, and with different channel bandwidth of 50, 100, 200 and 400 MHz, supplied at the centre frequency of 28 GHz. Fig. 19 shows the results for the 50 MHz and 100 MHz cases. The Adjacent Channel Power Leakage (ACLR) results already very good before digital predistortion (DPD), with values better than -30 dBc and little asymmetry between the sides, with an Error Vector Magnitude (EVM) around 6% in both cases. By applying the Direct DPD algorithm provided by the Amplifier Testing Tool, the ACLR can be reduced significantly in both cases, result in of -46 dBc and -43 dBc at 50 MHz and 100 MHz channel, respectively, while the EVM was brought

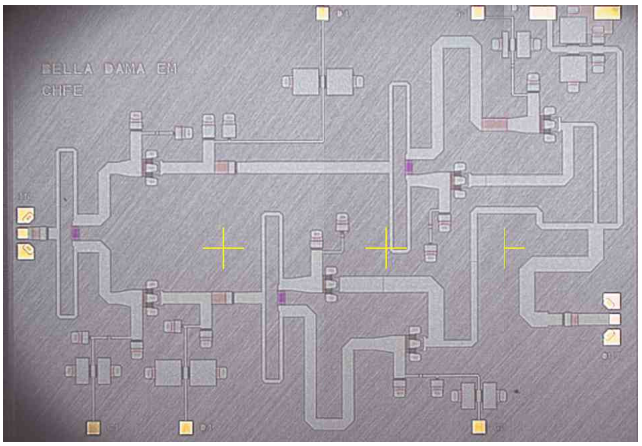

Fig. 15. Microscope picture of the DPA designed using the proposed combiner. The MMIC size is $4.8\times3.4\,\mathrm{mm}^2$.

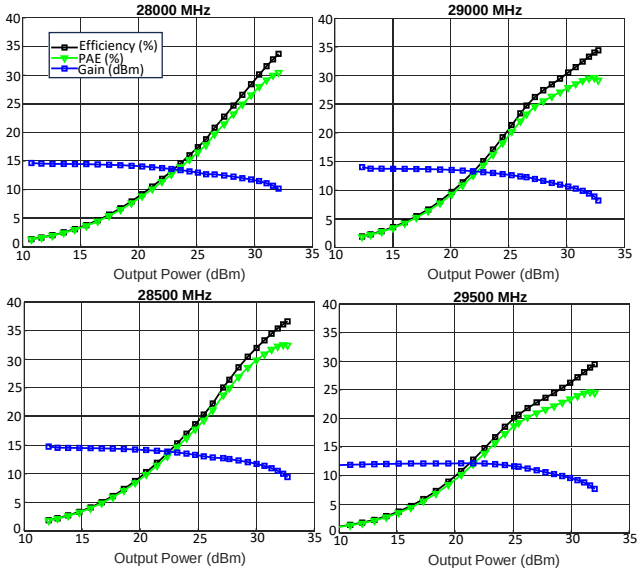

Fig. 16. PAE, gain and output power measurement profiles of the designed MMIC DPA.

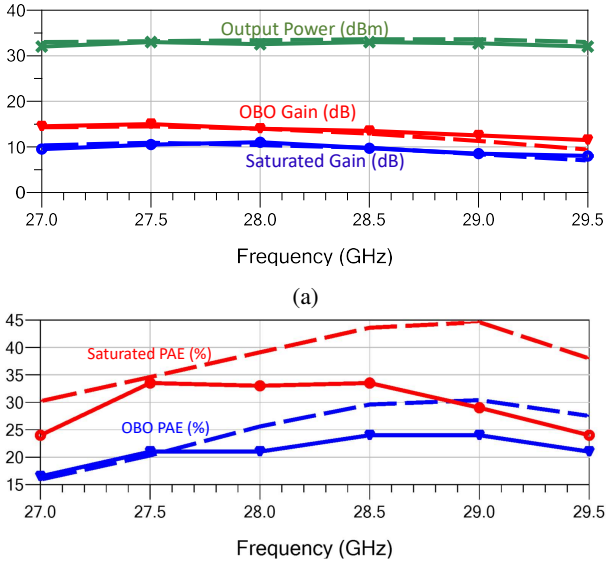

Fig. 17. CW measurements (symbols) and simulations (dashed lines) of the designed DPA: (a) saturated output power, saturated gain and OBO gain (b) saturated PAE and OBO PAE.

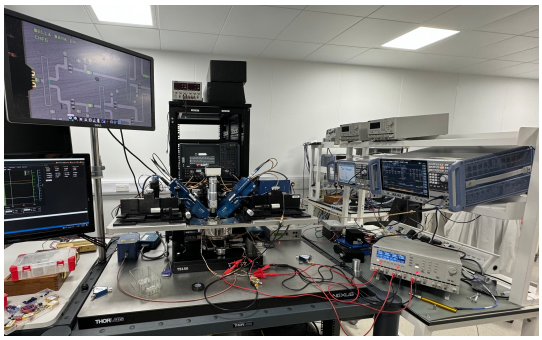

Fig. 18. Picture of the measurement system for the system level characterization.

below 2% in both cases. The measurements were captured at an average output power of 27.3 dBm, with a corresponding average drain efficiency of at least 24%. Fig. 20 shows the results for the 200 MHz and 400 MHz cases. For these channel bandwidths, the DPD algorithm did not converge to a useful solution, probably due to insufficient gain and output power equalization of the DUT across such a large bandwidth, and increased memory (ACLR starts becoming asymmetric). On the other hand, the reduced dynamic range at the receiver when increasing the capture bandwidth might also influence the convergence of the algorithm. The non-DPD results are reported, still showing a good linearity, with ACLR better than -28 dBc, but the EVM now increased at around 9%. The average efficiency at the average power of 27.3 dBm is slightly higher than at smaller channel bandwidth as it now captures the device response at frequencies with better efficiency. Overall, the device shows a fair intrinsic linearity up to 400 MHz bandwidth, and good linearize-ability at least up to 100 MHz channel bandwidth.

VIII. Conclusion

In conclusion, we have introduced a novel transistor combining methodology based on a simple $\lambda/4$ transmission line. The proper choice of the transmission line's characteristic impedance yields a combining effect, particularly advantageous at high frequencies. Following the combination, the two identical combined transistors effectively act, at least in a first order, linear, approximation, as a pure current generator, delivering twice the drain current of each individual transistor.

While we assumed a resistor as the load for the combiner network, the real part of the impedance observed at the generator reference planes of the devices are identical. However, an imaginary part is also present in one of them, but

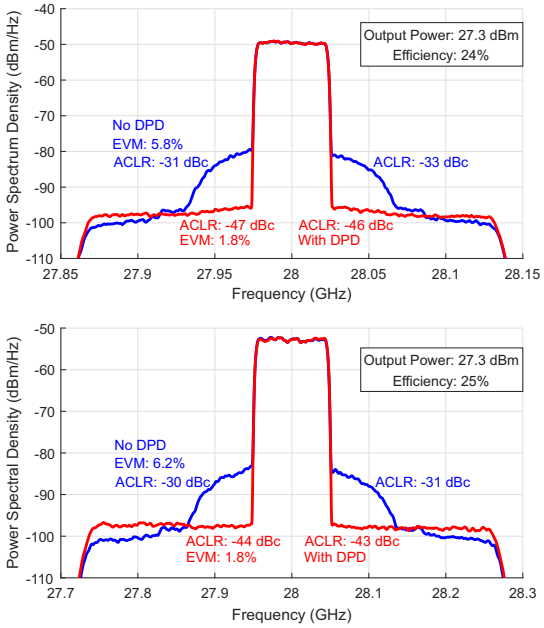

Fig. 19. Measured output spectra at 28 GHz carrier frequency with 5G FR2 signal with crest factor of 8 dB. 50 MHz (top) and 100 MHz (bottom) channel width. Without DPD (blue) and with direct DPD (red) applied.

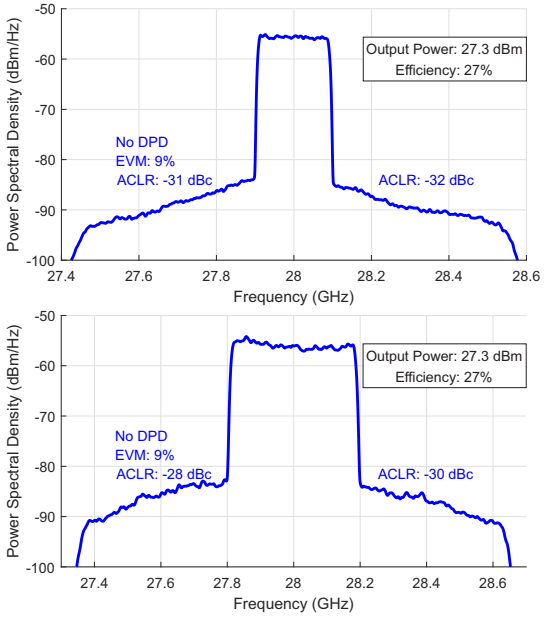

Fig. 20. Measured output spectra at 28 GHz carrier frequency with 5G FR2 signal with crest factor of 8 dB, without DPD. 200 MHz (top) and 400 MHz (bottom) channel width.

it becomes negligible for high design frequency. These characteristics result in nearly perfect high-frequency combination and simultaneous parasitic compensation, making this method highly suitable for the design of Power Amplifiers (PAs) at millimeter-wave (mm-wave) frequencies.

As a demonstrative application, we designed a Doherty Power Amplifier at 28 GHz using the proposed combiner, and the results were very good in terms of output power, efficiency, and gain, and quite in good agreement with simulations. This methodology opens up new possibilities for high-frequency PA design and holds promise for advancing mm-wave applications.

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