Modulation and Design for High-Efficiency SiC-Based Motor Drive Systems

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Abstract

The need for inverters with ever increasing power density, efficiency and reliability has recently become the driving factor for research in motor drives. Silicon carbide MOSFETs (SiC MOSFETs), a class of wide bandgap semiconductors, mark a substantial leap towards fulfilling this demand. These devices not only reduce the size and weight of passive components but also enhance thermal performance through their capacity for high switching frequencies. However, the adoption of SiC MOSFETs is not without its difficulties; it necessitates the management of increased losses at higher frequencies and the control of overvoltage due to their high voltage slew rate ($\mathrm{d}v/\mathrm{d}t$) characteristics. Addressing these challenges, this thesis presents innovative solutions for optimising SiC MOSFET switching frequency and minimising operational impediments due to high $\mathrm{d}v/\mathrm{d}t$.

This thesis first investigates the enhancement of SiC-based motor drive efficiency via variable switching frequency pulse-width modulation (VSF-PWM). By leveraging accurate motor drive loss modelling, a VSF-PWM method is proposed that determines the optimal switching frequency providing the lowest system losses, contingent on motor speed and torque. Adopting this loss modelling approach to vary the switching frequency leads to a system efficiency improvement of up to 0.3%, which is a notable gain compared to a fixed high-frequency operation. However, the technique also leaves potential for limiting peak current ripple. To address this, an additional VSF-PWM modulation control scheme is subsequently introduced, which adaptively varies the switching frequency in response to both the current ripple magnitude and the established loss model technique. This approach is especially relevant in industries where stringent standards mandate limitations on peak current ripple.

In SiC-based cable-fed motor drives, the high $\mathrm{d}v/\mathrm{d}t$ and impedance mismatches can trigger the reflected wave phenomenon, increasing the risk of motor overvoltage. Such a scenario can hasten the deterioration of the motor stator winding insulation due to partial discharges, jeopardising the system's longevity and reliability. In response to this, the second part of the thesis presents the use of a zero-voltage switching (ZVS) inverter, designed to actively modulate voltage rise and fall times. Comprehensive guidelines on the selection of inductor and capacitor parameters, aiming for ZVS and overvoltage mitigation, are detailed. Results indicate that the ZVS inverter provides up to a 1% efficiency gain and a 30% volume reduction when compared with alternative solutions.

The research work documented in this thesis is underpinned by comprehensive simulations, further validated through experimental results.

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Contents

List of Figures

List of Tables

Nomenclature

Acronyms

CM	common-mode
CSF-PWM	constant switching frequency pulse-width modulation
DM	differential-mode
EMI	electromagnetic interference
EVs	electric vehicles
FEM	finite element method
FOM	figure of merit
GaN	gallium nitride
IGBT	insulated-gate bipolar transistor
MOSFET	metal-oxide-semiconductor field-effect transistor
PD	partial discharge
PDIV	partial discharge inception voltage
PMSM	permanent magnet synchronous motor
PWM	pulse-width modulation
Q3L	quasi-three-level
RWP	reflected wave phenomenon
Si	silicon
SiC	silicon carbide

SPWM	sinusoidal pulse-width modulation
SVPWM	space-vector pulse-width modulation
THD	total harmonic distortion
VSF-PWM	variable switching frequency pulse-width modulation
WBG	wide bandgap
ZVS	zero-voltage switching

Number Sets

$\mathbb{Z}^+$	positive integer

Symbols

Δv_a	voltage ripple of phase a
$\eta_{sys,meas}$	measured system efficiency
$\eta_{sys,sim}$	simulated system efficiency
Γ_i	reflection coefficient at the inverter terminals
Γ_m	reflection coefficient at the motor terminals
$\hat{i}_{p,peak}$	predicted peak current ripple
$\hat{i}_{set}$	predefined current ripple limit
$\hat{i}_{x,p,peak}$	predicted peak current ripple of phase x
$\mathrm{d}v/\mathrm{d}t$	voltage slew rate
ω_r	rotational speed
$\overline{v}_a$	average voltage of phase a
θ_e	electrical angle
θ_r	rotor angle
C_{cable}	cable per-unit length capacitance
C_c	clamping capacitor

C_{ds}	drain-source capacitance
C_{gd}	gate-drain capacitance
C_{gs}	gate-source capacitance
C_{iss}	input capacitance
C_{oss}	output capacitance
C_{rt}	total resonant capacitance
C_r	resonant capacitance
D_a	duty cycle of phase a
d_o	turn-off duty cycle of switch S_7
E_{cond}	conduction energy loss
E_{off}	turn-off switching energy loss
E_{on}	turn-on switching energy loss
f	fundamental frequency
f_{sw}^*	optimised switching frequency
f_{rwp}	oscillation frequency
$f_{sw,r}^*$	optimised ripple switching frequency
f_{sw}	switching frequency
i_{boost}	boost current
i_{Cc}	clamping capacitor current
i_d	drain current
i_{Lr}	resonant inductor current
i_{m_max}	maximum motor phase current
i_m	motor phase current
L_{cable}	cable per-unit length inductance

L_d	direct-axis stator inductance
L_q	quadrature-axis stator inductance
L_r	resonant inductance
m_i	modulation index
p	number of motor pole pairs
P_{aux}	auxiliary switch total power loss
P_{Cu}	motor copper power loss
P_{Fe}	motor iron power loss
P_{filter}	filter power loss
$P_{m,cond}$	inverter conduction power loss
$P_{m,sw,off}$	inverter switching turn-off power loss
$P_{m,sw,on}$	inverter switching turn-on power loss
$P_{m,sw}$	inverter switching power loss
Q_{oss}	output charge
$R_{ds,on}$	specific on-state resistance
R_s	stator winding resistance
t_{fr}	resonant fall time
T_L	load torque
t_n	natural rise time
t_p	propagation time
t_{rr}	resonant rise time
t_r	rise time
$t_{sw,off}$	turn-off switching time
$t_{sw,on}$	turn-on switching time

T_s	switching period
v	wave propagation velocity
V_{ab}	line voltage between phase a and phase b
V_a	voltage of phase a
V_{bus}	bus voltage
V_{Cc}	clamping capacitor voltage
V_{dc}	dc-link voltage
$V_{ds,\max}$	maximum drain-source voltage
V_{ds}	drain-source voltage
V_g	gate voltage
$V_{i,ab}$	inverter line voltage between phase a and phase b
V_i	inverter output voltage
V_i	inverter voltage
$V_{m,ab}$	motor line voltage between phase a and phase b
V_m	motor voltage
V_{on}	average forward threshold voltage
Z_0	cable characteristic impedance
Z_i	inverter characteristic impedance
Z_m	motor characteristic impedance
Z_r	resonant impedance

Chapter 1

Introduction

1.1 Background and Motivation

Power electronics, a critical branch of electrical engineering, revolves around the conversion and control of electrical power using inverters. Made predominantly from semiconductor materials, these devices underpin a plethora of modern-day applications. They are pivotal in transportation electrification, where they manage battery charging and power delivery to drive motors, with voltages ranging from 400 to 800 V [1, 2]. Additionally, in renewable energy systems they help convert solar or wind energy into usable electrical power [3]. Beyond these, they are critical in applications such as aerospace [4], railway [5], marine propulsion [6], and industrial machinery [7, 8]. With its vast influence on our daily lives and the evolving energy landscape, power electronics inverters stands at the nexus of innovation, steering us toward a more sustainable and technologically advanced future [9].

At the core of inverters, the semiconductor device plays a pivotal role by adeptly converting direct current (dc) voltage into alternating current (ac) voltage. This transformation is foundational for motor drive applications, where precise control over motor speed and torque is paramount. As depicted in Figure 1.1, inverters facilitate the operation of motors at variable speeds, achieving impressive efficiencies typically ranging from 85% to 98% [10]. The design intricacies of inverters, including the selection of semiconductor materials and the electronic topologies, significantly influence their performance and efficiency. Given their influential role in motor drive innovations, design of inverters is essential for enhancing both performance and energy efficiency.

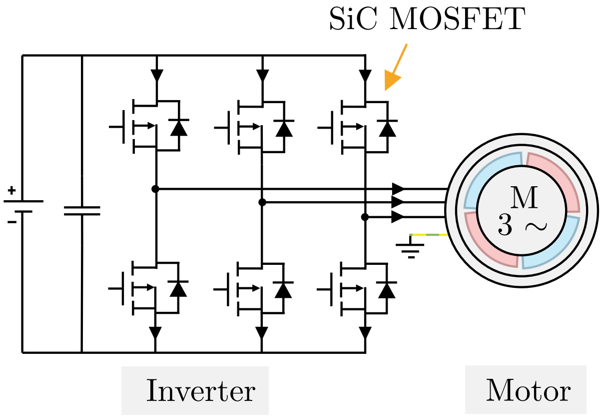


Figure 1.1: SiC-based motor drive system.

1.1.1 An Overview of SiC MOSFETs

Silicon (Si) has long been the preferred material for power semiconductor devices used in inverters due to their abundant availability, high quality and low cost [11]. The extensive availability of Si has spurred innovations in both unipolar and bipolar devices [12]. However, the push for greater power density, enhanced efficiency, and the ability to operate at higher temperatures is stretching the capabilities of Si to its limits [13]. As a result, wide-bandgap (WBG) semiconductors are gaining attention.

Among WBG materials, silicon carbide (SiC) stands out. It is unique in that it can be thermally oxidised to form silicon dioxide (S_iO_2) which is both chemically and thermally stable [14]. This property is crucial for the effectiveness of metal-oxide-semiconductor field-effect transistors (MOSFETs) [15]. Moreover, SiC's relative maturity compared to other WBG materials, such as gallium nitride (GaN), makes it a leading candidate to replace Si in high-voltage power electronics [16]. A notable comparison is portrayed in Figure 1.2, showing the figure of merit (FOM) against semiconductor maximum drain-source voltage $V_{\mathrm{ds,MAX}}$ or maximum collector-emitter voltage. This highlights that SiC MOSFETs outperform Si insulated-gate bipolar transistors (IGBTs) in efficiency for voltages between 600 V and 1200 V. Conversely, GaN FETs show superior efficiency at 100 V to 600 V compared to SiC MOSFETs and Si IGBTs.

Currently, GaN FETs face challenges in motor drive applications due to limitations in voltage and current ratings, as well as concerns over reliability under high-voltage stress conditions [17]. Most commercially available GaN FETs support up to 600-650V and drain currents up to 30 A, which falls short for high-power motor drives. Advanced cascode configurations can increase current capabilities but still do not match the performance of SiC MOSFETs and Si insulated-gate bipolar transistors (IGBTs) [18].

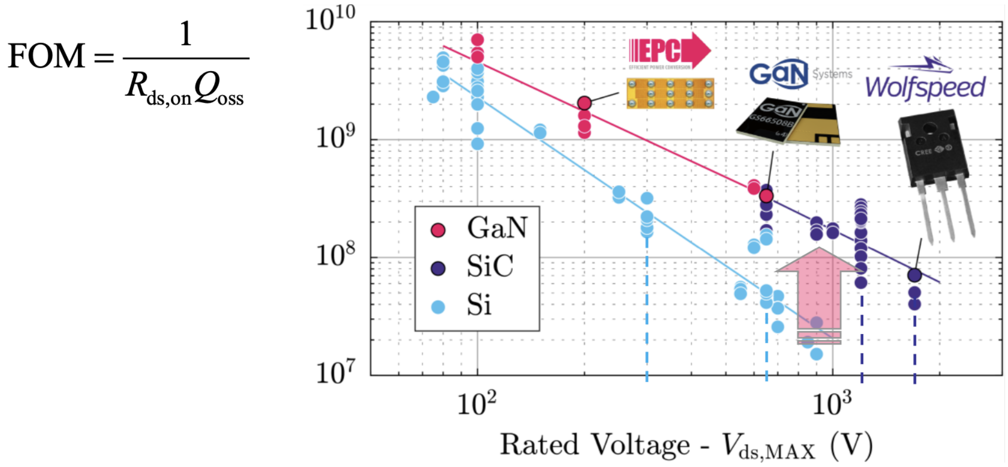


Figure 1.2: Comparison of GaN FET, SiC MOSFET and Si IGBT FOM with rated voltage [21]. ($R_{ds,on}$ = on-state resistance, Q_{oss} = output charge.)

The reliability of GaN devices at the high temperatures and power levels typical of motor drive applications is an area of active research and development, focusing on device packaging and thermal management improvements for broader adoption.

In sectors ranging from automotive and aerospace to renewable energy, SiC MOSFETs have established a strong presence [13]. They offer superior characteristics such as a wider energy gap, higher electric breakdown field, better thermal conductivity, and faster electron velocity [13]. These advantages enable SiC MOSFETs to handle higher voltages, temperatures, and switching frequencies than traditional Si-based devices [16]. Currently, Cree offer a SiC MOSFET rated 1200 V with drain current of 125 A [19], representing a significant enhancement over the existing GaN FET solutions. They can even operate at temperatures up to 500°C enhancing thermal conductivity and reducing thermal resistance from the junction to the case [20]. This enables more compact designs and efficient cooling methods, clearly demonstrating why the power electronics sector is increasingly favoring SiC MOSFETs over Si IGBTs for motor drives.

1.1.2 Loss Mechanisms in Motor Drives

Motor drive systems inherently experience various power losses that can reduce their overall efficiency and performance. These losses, which manifest as energy dissipation and heat generation, stem from the inverter, motor and feeder cables. A meticulous understanding of these losses is paramount, not just for diagnostic reasons, but to refine the energy conversion process. When these losses are mitigated, it paves the way for superior system efficacy. Engineers, equipped with this knowledge, can innovate

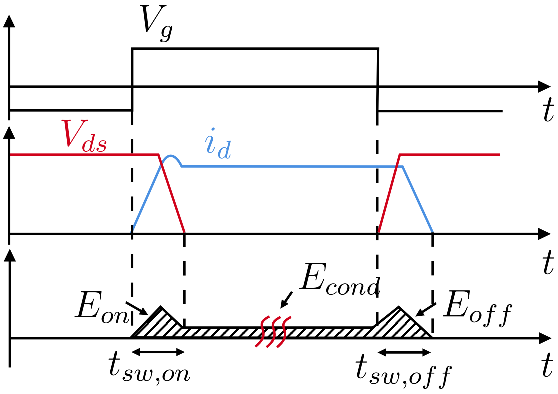


Figure 1.3: Typical inverter switching waveforms for a MOSFET.

designs that not only enhance energy utilisation but also reduce energy wastage. As a result, the motor drive systems become more efficient, cost-effective, and durable.

The primary losses in a hard-switching inverter are shown in Figure 1.3, where conduction energy losses are represented as E_{cond} and switching energy losses during both turn-on, E_{on}, and turn-off, E_{off} phases. The overlapping of the drain-source voltage V_{ds} and drain current i_d during turn-on $t_{sw,on}$ and turn-off $t_{sw,off}$ leads to losses, quantified as the integral of their product. When comparing equivalent SiC MOSFETs and Si IGBTs, the SiC MOSFETs exhibit lower switching losses due to their faster rise times [22]. However inverter techniques have also been introduced to further reduce switching losses, such as soft-switching [23,24]. These techniques involve modifying inverter topologies and implementing unique control mechanisms to shape the voltage and current of the power device during switching transients. By doing so, the overlap between V_{ds} and i_d during switching transitions is substantially reduced. These techniques not only reduce switching losses but also alleviate voltage stress on power devices and minimise electromagnetic interference (EMI) noise [25].

Soft-switching primarily encompasses two forms: zero-voltage switching (ZVS) and zero-current switching. ZVS facilitates a switch's transition from its off-state to its on-state precisely when the voltage across it reaches zero [26]. This method effectively reduces the interval during which both voltage and current coexist, thereby decreasing power losses in the switching phase. Conversely, zero-current switching ensures that the switch transitions when there is no current flowing through it, enhancing the efficiency and safety of the process [27].

In electric motors, the primary energy losses can be categorised into iron (core) and copper losses [28]. Iron losses manifest in the magnetic components of the motor, specifically the stator and rotor, and are the result of hysterisis and eddy current losses. Hysteresis losses arise due to the incessant realignment of magnetic domains in response to a fluctuating magnetic field. Eddy current losses emerge from currents induced within the iron core by this changing magnetic field, leading to resistive heating within the core itself. Conversely, copper losses pertain to the resistive heating observed in the motor's windings, encompassing both the stator and rotor. As current traverses these windings, the inherent resistance results in heat generation and consequent energy dissipation. Notably, the magnitude of copper losses is contingent on the square of the current, rendering them variable based on the motor's operational load current.

Losses can also arise from the feeder cables in motor drives [29], particularly when there is a significant distance between the inverter and the motor. These losses may be resistive losses, that occur due to the inherent resistance of the cable material and high-frequency losses, such as the skin and proximity effects. Additionally, longer cables can introduce capacitive and inductive losses, affecting the overall power quality and efficiency.

Given that faster switching incurs more losses, there is a constant demand for approaches that comprehensively examine how switching frequency influences the spectrum of losses in motor drives. In accordance with this, approaches such as variable switching frequency pulse-width modulation (VSF-PWM) have been of high interest [30–32] The primary object is to reduce these power losses, current ripple and peak electromagnetic interference (EMI) by varying the switching frequency. Additionally, by varying the switching frequency according to system operational conditions, it is possible to enhance the overall performance and efficiency of the motor drives, thus extending their operational lifespan and reliability.

1.1.3 Fast Switching of SiC MOSFETs

One of the distinct characteristics of SiC MOSFETs is their fast switching, often characterised by a high voltage slew rate ($\mathrm{d}v/\mathrm{d}t$) [33]. Compared to Si IGBTs, SiC MOSFETs offer significantly shorter switching times, which bring notable advantages. These not only include an improvement in overall power conversion efficiency by reducing switching losses but also the capability for these devices to operate at higher switching frequencies [13]. Consequently, power electronic systems can utilise smaller passive components, resulting in both size and weight reductions [34]. Moreover, the reduced switching losses lead to less heat generation, thus improving the device's thermal performance, longevity, and reliability. The fast response time of SiC MOSFETs is particularly beneficial in applications requiring swift reactions, such as motor drives or active power factor correction circuits.

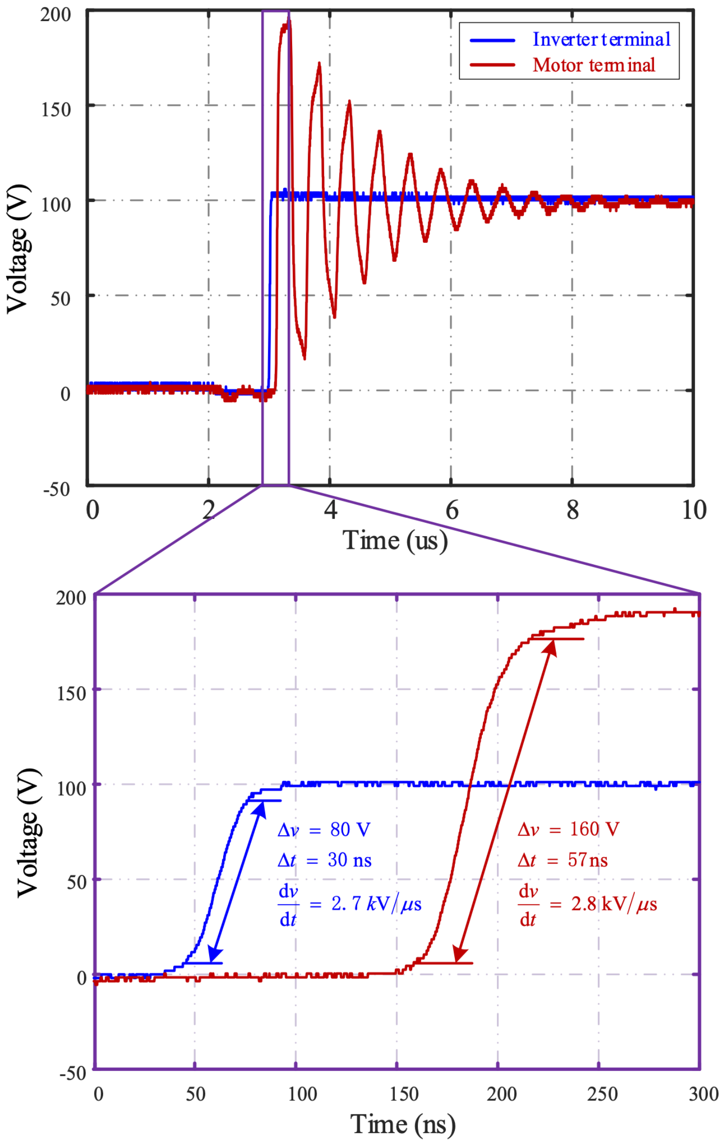


Figure 1.4: Measured inverter and motor terminal voltage in cable-fed drive at 20 m cable length [35].

Despite these advantages, fast switching can also cause significant challenges. High dv/dt can lead to an increased risk of voltage overshoot during switching transitions, potentially stressing the device beyond its maximum voltage rating and compromising its reliability [36]. Moreover, fast voltage transitions can couple noise into adjacent circuits, especially if there is inadequate shielding or improper layout, leading to EMI issues [37]. This can disturb the operation of nearby electronic devices and may necessitate additional filtering or shielding solutions.

A pressing concern arises from motor overvoltage oscillations caused by the reflected wave phenomenon (RWP) [38]. This issue stems from the high dv/dt and impedance mismatches when long cables connects the inverter and motor, typically referred as a cable-fed motor drive system. With the motor impedance usually being larger than the characteristic impedance of the cable, fast switching voltage pulses from the inverter undergo repeated voltage reflections [39, 40]. The phenomenon aligns with wave movement in transmission lines [41]. Consequently, the differential-mode (DM) voltage at the motor terminal can surge to twice the value of the inverter DM voltage, as illustrated in Figure 1.4.

The resultant overvoltage stress on the motor stator winding not only expedites winding insulation aging but also reduces the motor's lifespan [42, 43]. This is primarily caused by the onset of partial discharges (PDs), leading to the deterioration and localised heating of the motor stator coil's organic coatings, consequently impacting the reliability of the motor drive system [44–46]. In addition to the previously mentioned challenges, fast switching can lead to uneven voltage distribution across the motor's stator windings [47]. Typically, the most significant voltage stress is observed in the initial turns close to the motor terminals. Further exacerbating the issues with PDs and insulation stress in the first few turns.

When WBG devices are integrated into motor drives, they often facilitate for higher switching frequencies. This increased frequency can trigger a double pulsing effect, pushing the motor voltage to exceed twice that of the inverter [48]. This is where the first pulse has not fully damped before the second pulse is sent. As a consequence, incorporating WBG devices can significantly compromise the reliability of the motor. Challenges rooted in the RWP, particularly due to the high $\mathrm{d}v/\mathrm{d}t$, might curtail the widespread adoption of WBG technologies in these systems. Given this, there is an imperative need to both recognise these challenges and engineer mitigation techniques, ensuring the efficient and safe implementation of WBG devices.

1.2 Thesis Outline

This thesis is organised into seven chapters, with the overarching structure depicted in Figure 1.5. Chapter 2 delves into pivotal modulation methods designed to increase system efficiency in SiC-based motor drives, with a special emphasis on VSF-PWM and current ripple prediction. Additionally, the chapter offers an insight into cable-fed motor drives, highlighting the technical challenges posed by the high $\mathrm{d}v/\mathrm{d}t$ of SiC MOSFETs and conventional mitigation methods. The chapter concludes with an overview on high-frequency simulation modelling techniques pertinent to cable-fed motor drives.

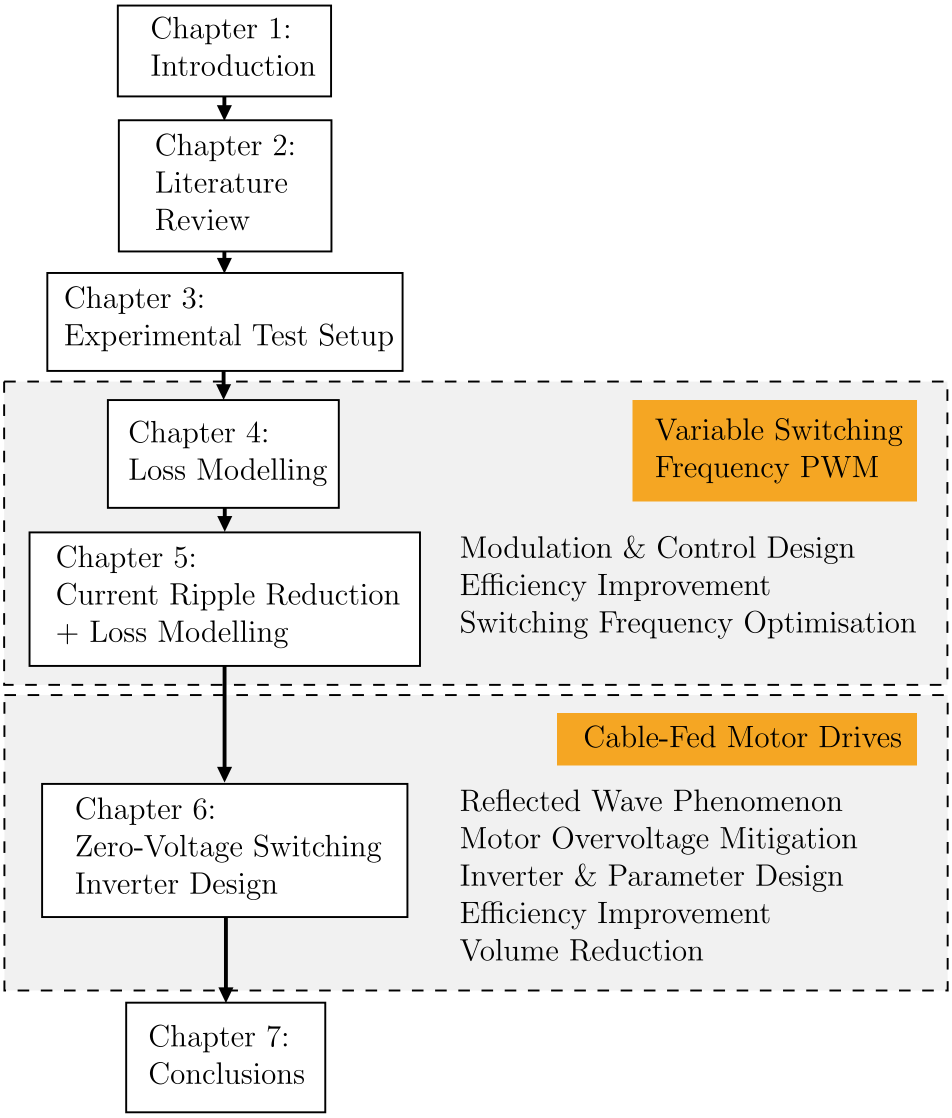


Figure 1.5: Thesis structure.

Chapter 3 provides a comprehensive overview of the experimental setup employed in this thesis, including a detailed description of the control system and its real-time monitoring capabilities for current and voltage.

Chapter 4 introduces loss modelling tailored for a SiC-based motor drive system, detailing the process of computing system efficiency. Through adept utilisation of this loss modelling, an optimal switching frequency of a motor drive is determined, influenced by load conditions, such as speed and torque. This, in turn, facilitates the creation of an offline lookup map. The chapter subsequently explores the application of VSF-PWM, leveraging this offline lookup map to fine-tune system efficiency across a range of operating conditions. Emphasising adaptability, the chapter modulates the switching frequency in response to varied load conditions, all underpinned by the loss modelling, prioritising system efficiency.

Chapter 5 delves deeper into the VSF-PWM loss modelling technique, enriching it with the integration of current ripple reduction. This process necessitates a refined modulation and control design, aiming to further improve system efficiency whilst limiting peak current ripple. Notably, this chapter capitalises on the insights from Chapter 4, specifically the loss modelling and uneven current ripples observed in each switching cycle to achieve this enhancement.

Chapter 6 presents a remedy for the RWP and motor overvoltage challenges inherent in SiC-based cable-fed motor drives. A solution to addressing these issues requires the integration of a ZVS inverter that modulates the $\mathrm{d}v/\mathrm{d}t$, thereby diminishing power losses and mitigating motor overvoltage. To further streamline the solution, a modified space vector PWM (SVPWM) has been integrated into the control design, with intricate details delineated in Appendix A. Accompanying this, a high-frequency cable and motor simulation model is employed, with a thorough breakdown on parameter extraction available in Appendix B. This chapter focuses on the inductor and capacitor design for the presented ZVS inverter to achieve $\mathrm{d}v/\mathrm{d}t$ profiling and mitigate motor overvoltage in cable-fed systems.

Chapter 7 provides a comprehensive summary of the main conclusions drawn from this thesis and explores potential directions for future investigations.

1.3 Research Objectives and Contributions

This research emphasises two main areas: enhancing the efficiency of SiC-based motor drive systems using VSF-PWM and mitigating motor overvoltage in cable-fed systems, all while preserving the advantages of SiC MOSFETs. This includes employing optimal modulation and design strategies to address the challenges posed by high $\mathrm{d}v/\mathrm{d}t$. The study seamlessly blends theoretical exploration with simulation verification and experimental validation, structured around three core research objectives and contributions:

- **Objective 1:** Investigate the correlation between switching frequency and power losses to enhance system efficiency in SiC-based motor drives.

  Contribution 1: An innovative VSF-PWM control method is introduced designed to significantly enhance the efficiency of motor drive systems, a key research interest in automotive applications. The core advancement lies in dynamically adjusting the inverter's switching frequency to minimise system power losses, thus addressing a prevalent limitation in the industry.

  - Power Loss Analysis: The method begins with a comprehensive analysis of how switching frequency influences power losses within the system. This includes both inverter losses and motor losses.
  - Optimal Switching Frequency Identification: Through accurate loss modelling, the novel method identifies an optimal switching frequency that achieves a balance between inverter and motor losses, enhancing overall system efficiency.
  - Dynamic Adjustment Based on Load Conditions: Recognising that the optimal switching frequency varies with motor load conditions, the method leverages an offline lookup map. This map catalogs optimal switching frequencies across a range of load conditions, enabling the system to adjust the switching frequency in real-time to match current operating conditions. The method uses linear interpolation to smoothly transition between switching frequencies, preventing disruptions and ensuring consistent motor performance.

  The VSF-PWM control method directly addresses the automotive industry's need for more efficient motor drive systems. By optimising the switching frequency according to real-world operating conditions, this approach significantly reduces power losses, thereby enhancing the energy efficiency of electric vehicles. This improvement in efficiency can lead to longer vehicle ranges and lower energy consumption, key factors in the widespread adoption of EVs.

- **Objective 2:** To design a control strategy that enhances SiC-based motor drive efficiency whilst limiting peak ac current ripple.

  Contribution 2: A novel approach to controlling ac current ripple in motor drive systems through a VSF-PWM method is introduced. Leveraging advanced loss modelling techniques, this method specifically aims to minimise current ripple, thereby enhancing the system's overall efficiency—a critical aspect for improving EV performance.

  - Current Ripple Control: The proposed VSF-PWM method dynamically adjusts the inverter's switching frequency to limit the maximum current ripple. This adjustment is crucial for maintaining optimal system efficiency and performance under varying operational conditions.

  - Integration with Optimised Switching Frequency: Building on the optimised switching frequency identified in the first contribution, this novel approach further refines system efficiency by adjusting the switching frequency based on the current ripple magnitude and loss modelling. This ensures that the motor drive operates at the highest efficiency point, even with fluctuating load demands typical in automotive applications.
  - Dynamic Performance Consideration: Unlike existing VSF-PWM techniques that might overlook the motor's dynamic changes in speed and torque, this method incorporates these variables into its optimisation process. By doing so, it ensures the motor drive system's efficiency and performance are maintained across the full spectrum of operational conditions.

  This advanced control method addresses a key challenge in electric vehicle technology by optimising the ac current ripple, thus significantly enhancing motor drive efficiency and performance.

- **Objective 3:** To mitigate motor terminal overvoltage in cable-fed systems by dynamically shaping the voltage slew rate ($\mathrm{d}v/\mathrm{d}t$) of SiC MOSFETs.

  Contribution 3: In marine applications, electric propulsion systems face significant challenges related to motor overvoltage, which can lead to efficiency losses and potential equipment damage. Traditional solutions, such as multilevel inverters and $\mathrm{d}v/\mathrm{d}t$ passive filters, while effective in mitigating overvoltage, often result in increased system volume and losses. A proposed method is introduced for selecting inductor and capacitor parameters in a ZVS inverter from [24], designed to overcome motor overvoltage issues in marine motor drive systems.

  - ZVS Inverter Design: The ZVS inverter from [24], distinguishes itself from other solutions by incorporating a single additional active switch on the positive dc terminal. This offers a simpler yet effective alternative to conventional two-level and three-level inverters, reducing the complexity and potential for overvoltage conditions.
  - Component Parameter Selection: Through a meticulous selection process for inductor and capacitor parameters, the novel method significantly suppresses overvoltage oscillations. This optimisation focuses on controlling $\mathrm{d}v/\mathrm{d}t$, minimising switching losses, and averting the need for bulky passive filters or complex multilevel inverters.

  - Efficiency and Volume Improvements: Comparative analysis with existing overvoltage mitigation techniques, such as two-level passive filters and three-level inverters, showcases the superiority of the proposed method. Demonstrating a 1% increase in efficiency and a 30% reduction in system volume, this approach marks a significant advancement for marine applications.

Addressing overvoltage challenges with an innovative ZVS inverter design and optimised parameter selection represents a pivotal improvement for marine electric propulsion systems. The reduction in volume and enhancement in efficiency directly contribute to more sustainable and effective marine operations, allowing for better energy management and reduced environmental impact.

1.4 List of Publications

The following articles were published or under preparation during the course of the present research work.

Journal articles:

- **S. Yunus**, W. Ming and C. E. Ugalde-Loo, "Variable Switching Frequency for Current Ripple Control and Loss Reduction in SiC-Based Motor Drives," (under review).

- **S. Yunus**, W. Ming and C. E. Ugalde-Loo, "Motor Overvoltage Mitigation Using SiC-Based Zero-Voltage Switching Inverter," *IEEE Transactions on Power Electronics*, vol. 39, no. 1, pp. 1195-1208, Jan. 2024, IEEE.

Conference articles:

- **S. Yunus**, W. Ming and C. E. Ugalde-Loo, "Adaptive Variable Switching Frequency Control for SiC-based PMSM Drive Systems," *IECON 2022 - 48th Annual Conference of the IEEE Industrial Electronics Society*, Brussels, Belgium, 2022, pp. 1-6, IEEE.
- **S. Yunus**, W. Ming and C. E. Ugalde-Loo, "Efficiency Improvement Analysis of a SiC MOSFET-based PMSM Drive System with Variable Switching Frequency," *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, Ghent, Belgium, 2021, pp. 1-9, IEEE.

Chapter 2

Literature Review

2.1 Introduction

Within SiC-based motor drives, there has been a focused effort to pioneer methods that capitalise on the superior switching capabilities of SiC MOSFETs [30, 49–51]. One prominent research area concentrates on refining VSF-PWM strategies to reduce power losses that occur due to the high switching frequencies of SiC MOSFETs [30]. Dynamic adjustment of the switching frequency allows for varied control strategies, which are instrumental in optimising system operation [52]. This approach not only minimises system losses but also improves the overall efficiency and energy conservation of motor drive systems. Consequently, exploring VSF-PWM techniques is a key research direction that promises substantial improvements in the energy efficiency and performance of SiC-based motor drives.

Parallel to the pursuit of VSF-PWM techniques, another critical research area with SiC MOSFETs has emerged in the context of cable-fed motor drives—mitigating motor overvoltage. The integration of long cable connections in motor drive systems introduces new challenges, such as the occurrence of the RWP and overvoltages stemming from the fast switching transitions and high $\mathrm{d}v/\mathrm{d}t$ associated with SiC MOSFETs [53, 54]. Reflected waves generated during the switching process pose a substantial risk, potentially leading to voltage spikes that can damage the motor winding insulation and compromise the reliability of the system [48]. Consequently, considerable efforts have been devoted to investigate and develop effective strategies for mitigating motor overvoltage [55, 56]. These endeavors aim to ensure the long-term operational integrity and safe functioning of cable-fed motor drives. This chapter presents a review of existing literature relating to both of these research areas.

2.2 Modulation Techniques for Motor Drive Systems

Efforts to enhance efficiency of motor drives have been ongoing. One significant approach has been through the use of soft switching topologies such as ZVS [57]. Soft switching inverters effectively curtail switching losses, yet they introduce additional components, making them more complex than their conventional counterparts. Thus, while the benefits of soft switching are evident, it is essential to weigh them against the added intricacies. Another critical approach, is the precise selection and application of PWM methods. When done right, these techniques minimise power losses, manage current ripple, and reduce EMI – all of which considerably elevate the overall performance of the motor drive, without requiring additional components [58].

The sinusoidal PWM (SPWM) method, one of the most common PWM techniques, uses a reference sinusoidal signal compared against a high-frequency triangular waveform. When the sinusoidal value surpasses that of the triangular waveform, the output is turned on and vice versa. This approach offers a predictable harmonic spectrum but does not maximise the use of the available dc bus voltage. On the other hand, SVPWM represents three-phase inverter voltages as a single rotating vector in a two-dimensional plane. By selecting appropriate switching vectors, SVPWM can achieve a higher voltage output than SPWM for the same dc bus voltage [59]. Meanwhile, other PWM techniques such as discontinuous PWM do not modulate all the inverter phases simultaneously, reducing switching transitions and associated losses, but can introduce more harmonics. The selection between these techniques hinges on the application, design objectives, and desired tradeoffs [60]. Each technique presents distinct benefits, tailored to specific operational scenarios. Given its prominence, Chapters 4 and 5 delve deeper into a widely-adopted variation of SVPWM, termed VSF-PWM.

2.2.1 Variable Switching Frequency PWM

In power electronics, current ripple significantly impacts efficiency, heat dissipation, EMI, and overall power quality [58, 61]. When an inverter in a motor drive system is modulated, it generates harmonics in the output voltage. These harmonics, in turn, lead to ripple in the load current, which increase the motor's copper and iron losses. Although a higher switching frequency can reduce this ripple, it concurrently increases the switching losses, reducing the system's efficiency. In addition, the magnitude of current ripple can be influenced by the specific PWM technique employed [62]. In

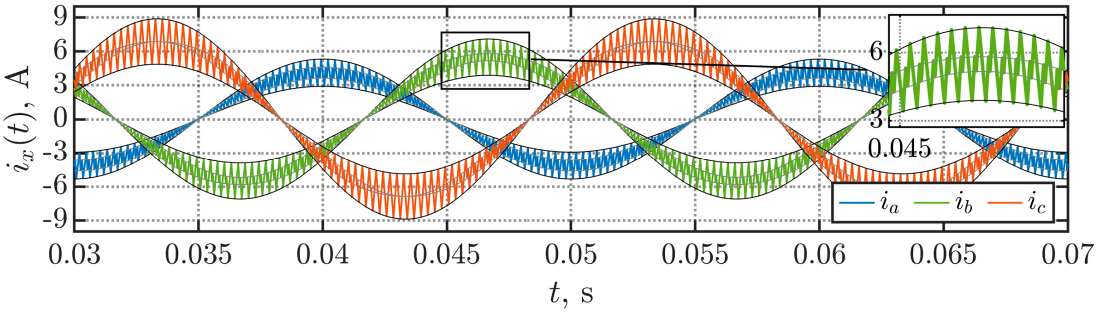


Figure 2.1: Three-phase current waveforms $i_x(t)$ showing uneven current ripple at different modulation index m_i. Phase a: $m_i = 0.3$, phase b: $m_i = 0.4$, phase c: $m_i = 0.5$. Switching frequency $f_{sw} = 3.6$ kHz [64].

the case of CSF-PWM, the generated current ripple in one time period is distributed unevenly [63]. As shown in Figure 2.1, the peaks of the ac current waveforms tend to have higher current ripple. Moreover, the uneven current ripple becomes more pronounced at a higher modulation index. It is worth noting that although the switching frequency is only 3.6 kHz in the referenced figure, the ripple unbalance is also noticed at higher frequencies [52]. Consequently, it is imperative to calibrate the balance between switching frequency and current ripple.

While CSF-PWM is prevalent due to its ease of control development, VSF-PWM considers the switching frequency as a variable, allowing for improved converter performance [30, 63, 65]. Over recent years, there has been a significant push to integrate VSF-PWM in motor drives and other three-phase PWM converters [66, 67]. A particularly effective strategy within this context is the utilisation of the random PWM technique. This approach is designed to mitigate both acoustic and EMI noise by introducing variability into the operating frequency, allowing it to fluctuate within a predefined range [68]. By employing such randomisation, the technique effectively disperses the harmonic energy across a broader spectrum of frequencies. This strategic spreading of energy not only minimises the potential for interference with nearby electronic systems but also ensures that the concentration of noise power is distributed more evenly. As a result, the peak levels of noise are significantly reduced, enhancing the overall performance and reliability of the electronic device in question [69]. Consequently, while random PWM can reduce peak electromagnetic emissions—facilitating compliance with EMI standards—the system's total harmonic energy typically remains unchanged. Instead, it is dispersed across diverse frequencies [60].

For SPWM, variable switching frequency is achieved by modifying the frequency of the carrier wave. This directly impacts the number of switching events within the inverter, allowing for finer control over the output waveform's quality and the inverter's

Table 2.1: CSF-PWM and VSF-PWM Comparison

	CSF-PWM	VSF-PWM
Switching frequency	Constant	Varied
Complexity	Simple	More complex
Harmonic content	At constant frequency	Spread over range
Efficiency	Baseline	Higher than CSF-PWM
Applications	Widely used	Where EMI and ripple control are prioritised [70]

efficiency. On the other hand, SVPWM involves altering the switching frequency by adjusting the sampling time and, consequently, the dwell times of the space vectors. This approach provides a more sophisticated method of controlling the inverter's output, enabling management of the efficiency and the harmonic content in the output voltage. It is important to note that the term constant switching frequency PWM (CSF-PWM) within the context of SVPWM emphasises maintaining a constant sampling time. This is since the switching rate of PWM pulses in SVPWM is inherently varied.

Initially proposed for single-phase converters in [65], VSF-PWM based on current ripple boasts significant benefits, including reduced switching losses and a more extensive spread of current harmonic spectra. Encouraged by these results, subsequent studies have expanded the use of this VSF-PWM approach to grid-connected three-phase systems [30] and permanent magnet synchronous motor (PMSM) drives [70]. As evidenced in literature, modulating the switching frequency according to current ripple magnitude is garnering interest. Consequently, setting the switching frequency to rise in high current ripple areas and reduces in regions of low current ripple. This strategy sets a maximum threshold for current ripple [30]. A general comparison between the CSF-PWM and VSF-PWM methods is presented in Table 2.1.

2.2.2 Current Ripple Prediction

In modulation strategies such as VSF-PWM, the ability to predict the current ripple is crucial. This predictive capability enables the control system to effectively accommodate potential delays inherent in processes such as data acquisition and computational processing. Furthermore, the preemptive nature of this approach allows for more control over the dynamics of current ripple modulation.

Numerous ripple prediction techniques have been introduced in the existing literature [30, 70–72]. These methods encompass a range of strategies, some of which involve intricate modelling of the load as an RL load with symmetrical back EMF for induc-

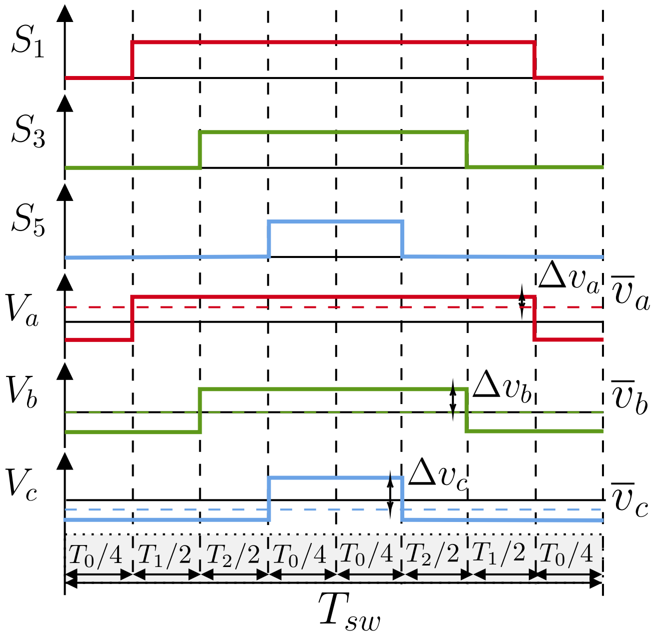


Figure 2.2: Output voltage waveforms V_x (including average voltage $\overline{v}_x$ and voltage ripple Δv_x) in one switching period T_{sw}, where x = phase.

tion machines and surface-mounted PMSMs. Alternatively, an innovative approach in [70] employs a comprehensive yet straightforward dq analysis of ripple voltage using SVPWM for PMSMs. This technique is employed in Chapter 5, and described in this section.

The dq analysis technique utilises the output voltage waveforms for a seven sector SVPWM switching waveform, as shown in Figure 2.2. Taking duty cycle of switch S1 in phase a as an example, the output voltage waveform V_a is the result of the sum of the average voltage $\overline{v}_a$ and voltage ripple Δv_a.

$$V_a = \overline{v}_a + \Delta v_a \tag{2.1}$$

Where $\overline{v}_a$ can be calculated from V_{dc} and the duty cycle of phase a, D_a, at both turn-on and turn-off.

$$V_a = D_a \frac{V_{dc}}{2} + (1 - D_a)(-\frac{V_{dc}}{2}) = (2D_a - 1)\frac{V_{dc}}{2} \tag{2.2}$$

The voltage ripple of phase a is calculated as

$$\Delta v_a = -\frac{V_{dc}}{2} - V_a = -V_{dc} D_a, \text{ when } \mathrm{S}_1 \text{ is off} \tag{2.3}$$

$$\Delta v_a = \frac{V_{dc}}{2} - V_a = V_{dc}(1 - D_a), \text{ when } \mathrm{S}_1 \text{ is on} \tag{2.4}$$

Likewise, the average voltage and voltage ripple of the remaining two phases can be calculated following the procedure used for phase a. After acquiring the voltage ripple for all three-phases, Park transform is applied to convert them into the dq reference frame. This transformation facilitates the correlation of dq voltage ripple with the stator inductance and current ripple

$$\Delta v_d = L_d \frac{d\Delta i_d}{dt} + R_s \Delta i_d - \omega_r L_q \Delta i_q \tag{2.5}$$

$$\Delta v_q = L_q \frac{d\Delta i_q}{dt} + R_s \Delta i_q + \omega_r L_d \Delta i_d \tag{2.6}$$

In induction machines and surface PMSM, the direct-axis stator inductance L_d and the quadrature-axis stator inductance L_q are generally calculated based on the phase-to-phase stator inductance, where $L_d = L_q$. On the other hand, for interior PMSM, these inductance's require more sophisticated techniques for accurate determination. Advanced numerical methods such as finite element method (FEM) simulations [73,74], or specialised analytical calculations [75], are commonly employed. This difference in approach is due to the complex magnetic circuit in interior PMSM, which arises from the embedded nature of the permanent magnets within the rotor. Such complexities make the straightforward methods that are often adequate for induction or surface PMSM insufficient for obtaining accurate values of L_d and L_q.

Considering the ripple component is analysed for a PMSM, the stator winding resistance R_s can be neglected because its effects are minor compared to the effects of inductance at the high switching frequencies used in motor control. Moreover, at steady state the impact of rotational speed ω_r on voltage ripple is minimal because the constant speed results in a steady back-EMF, and the voltage ripple is mainly due to the high-frequency current ripples caused by the inverter switching. These variations occur at a much higher frequency than changes in ω_r and therefore are the primary cause of voltage ripple. Consequently at steady state, (2.5) and (2.6) can be simplified as the following

$$\frac{d\Delta i_d}{dt} = \frac{\Delta v_d}{L_d} \tag{2.7}$$

$$\frac{d\Delta i_q}{dt} = \frac{\Delta v_q}{L_q} \tag{2.8}$$

By applying the inverse Park's transform, the three-phase current ripple can be derived. Based on the prediction of current ripple, the switching frequency can be varied accordingly with VSF-PWM. The dq methodology for predicting the current ripple is illustrated in Figure 2.3.

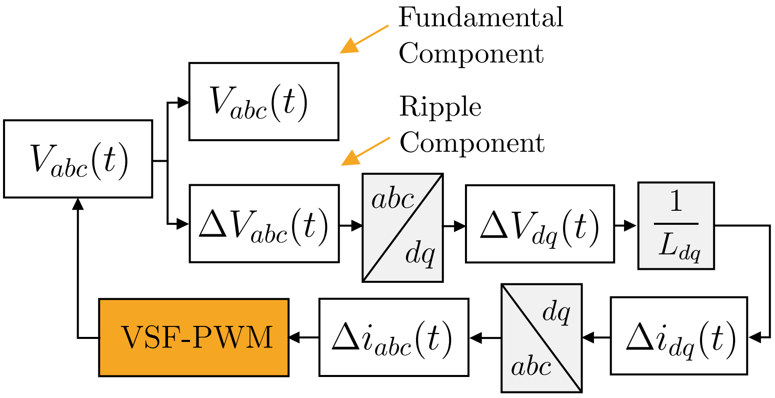


Figure 2.3: Current ripple prediction method using dq analysis.

2.3 Reflected Wave Phenomenon in Cable-Fed Motor Drives

In challenging and harsh environments, such as mining operations [76], oil exploration sites [77], and remote-operated vehicles [78], it is common practice to separate the installation of the inverter and motor due to volume constraints [41]. This is achieved by connecting the inverter and motor using long cables, creating a configuration known as a cable-fed motor drive systems, as illustrated in Figure 2.4. However, the use of these cables introduces characteristic impedance mismatches at the points of connection, such as at the inverter or motor terminals [79]. This leads to a complex environment where voltage and current waveforms interact and reflect off impedance mismatches. This phenomenon is referred to as the RWP or voltage reflection theory [43, 80].

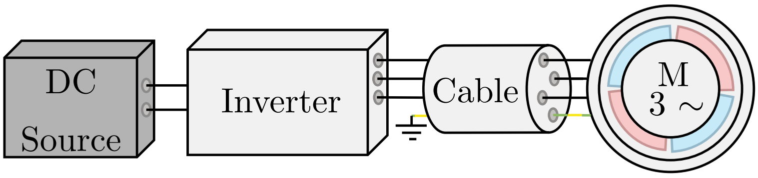


Figure 2.4: Three-phase cable-fed drive system.

RWP in cable-fed motor drives is a crucial concept that plays a significant role in comprehending the behaviour of electrical power transmission [81]. These mismatches lead to a portion of the voltage wave being reflected back towards the source, while the remaining portion propagates forward. The reflections can interfere with the incident wave, resulting in voltage and current distortions, and potentially causing voltage spikes up to 2 p.u., or waveform distortions at the motor terminals [48].

The magnitude and timing of these reflections are influenced by several factors,

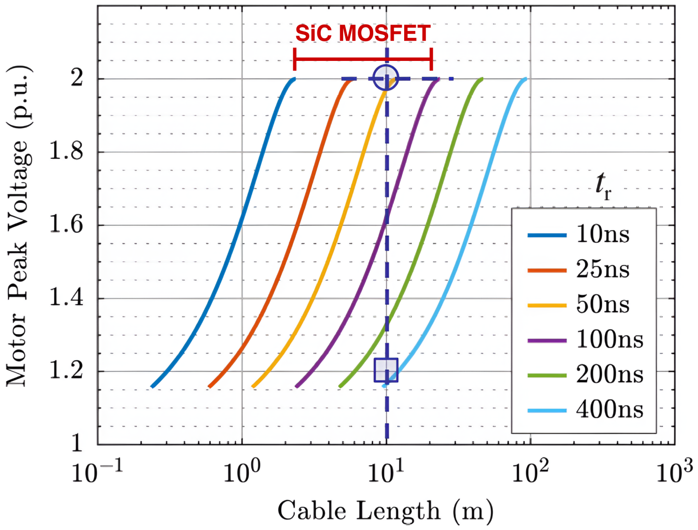


Figure 2.5: Motor peak voltage depending on cable length and rise time [82].

including the characteristic impedance of the cable, cable length, and the voltage rise time of the active switches [38]. Figure 2.5 illustrates this relationship, where an increase in cable length leads to a larger motor peak voltage. It is observed that motor overvoltage can occur even at shorter cable lengths when there is a faster voltage rise time t_r—typically around 10-100 ns for SiC MOSFETs and 100-400 ns for Si IGBTs [53]. This further exacerbates the overvoltage issue for SiC MOSFETs, as a rise time of 10 ns necessitates a cable length of only 2 meters before the overvoltage reaches 2 p.u.

Another crucial RWP concept when operating at higher switching frequencies is the double pulsing effect [83]. This effect involves a second voltage pulse reaching the motor terminals before the first reflected pulse has fully decayed, occurring due to closely spaced PWM pulses [48, 84]. As a consequence, the inverter output voltage at the motor terminal may exceed more than 2 p.u. Despite this, operating at higher switching frequencies might be necessary to fully harness the advantages offered by SiC MOSFETs.

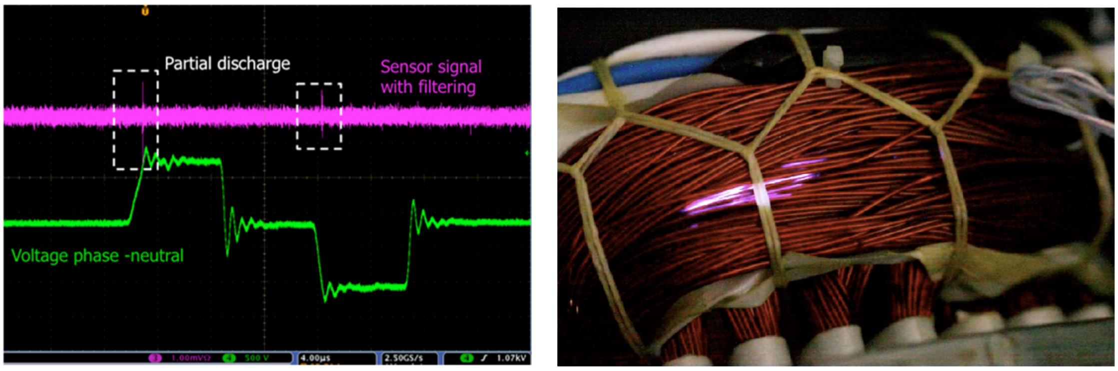
Understanding RWP is essential for engineers involved in the design of cable-fed motor drive systems. By comprehending the principles of voltage reflection and its effects, engineers can make informed decisions regarding cable selection and length [85]. Proper mitigation techniques, such as impedance matching at cable ends or employing appropriate mitigation control techniques, play a crucial role in minimising reflections and ensuring efficient power transfer. Moreover, an in-depth understanding of RWP allows engineers to implement suitable filtering and protection measures to mitigate voltage spikes, minimise EMI, and maintain the integrity and reliability of the motor drive system [86]. By leveraging the insights provided by RWP, engineers can optimise the performance of cable-fed motor drive systems, addressing impedance mismatches and wave reflections effectively while maximising power transmission efficiency and minimising potential issues.

2.3.1 Impact of Fast Switching in Cable-Fed Motor Drives

In addition to the RWP posed by incorporating a feeder cable, the high $\mathrm{d}v/\mathrm{d}t$ of SiC MOSFETs is expected to significantly affect the dependability and lifespan of the cable-fed motor drive system. These effects stem from PDs [45–47, 87–91], insulation stress [92–94], uneven voltage distribution on stator windings [95,96], EMI [97–99], and motor bearing currents [51, 100, 101].

Partial Discharge and Insulation Stress

The high $\mathrm{d}v/\mathrm{d}t$ exhibited by SiC MOSFETs can also give rise to significant issues concerning cable and motor insulation [93,94]. Generally, the insulation systems of PMSM and induction motors are not specifically designed to withstand high overvoltages [46]. Consequently, the voltage spikes up to 2 p.u. stemming from high $\mathrm{d}v/\mathrm{d}t$ can subject the cable and motor stator windings to stress [87]. This may lead to the occurrence of PDs, as shown in Figure 2.6. These PDs are localised electrical discharges that manifest within the insulation material. They can occur if the peak voltages surpass the partial discharge inception voltage (PDIV) of the cable and stator windings. Over time, the insulation can deteriorate as a result of these discharges, ultimately leading to insulation breakdown, diminished motor lifespan, and potential motor failure [47].



(a) (b)

Figure 2.6: PD in cable-fed motor drives. (a) PD detection with filtering [102]. (b) PD activity in motor stator endwindings (1013 mbar) [44].

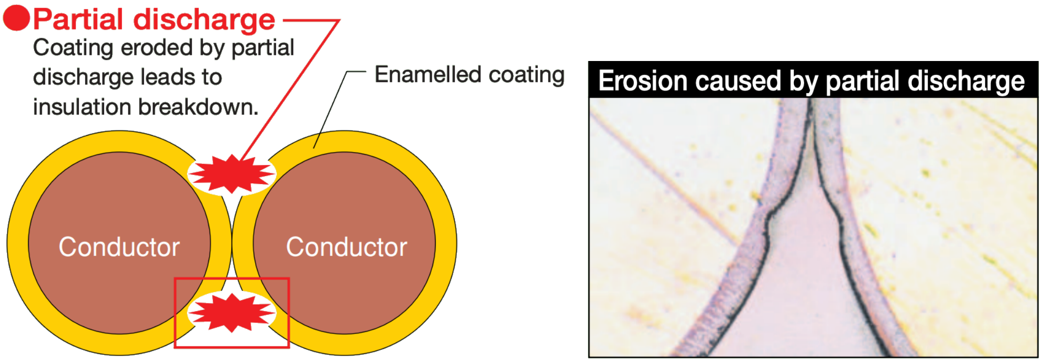


Figure 2.7: Insulation breakdown due to PD activity in motor stator windings [103].

This issue is particularly troublesome in applications involving high voltages, as the magnitude of the PDs can be substantial. The repetitive nature of PDs weakens the insulation, thereby establishing pathways for further breakdown and jeopardising the motor's structural integrity. In severe instances, PDs can give rise to motor failures, entailing operational downtime, costly repairs, and potential safety hazards [89].

It is worth noting that the occurrence of a PD event has a direct impact on the residual electric field within the insulation system as a result of space charge effects [90]. The decay of this residual electric field requires a certain amount of time. Consequently, in situations where motor overvoltage oscillations are closely spaced together, such as in the case of RWP, it is highly likely that only one PD event will transpire during each switching event.

Figure 2.7 visually depicts the phenomenon where stator winding erosion is attributed to PDs. Notably, this erosion does not necessarily transpire in the narrowest section of the air-gap, indicating the existence of a critical distance for PD initiation. This observation suggests that there exists a specific combination of electric field strength and distance that creates optimal conditions for ionisation to transpire across the air-gap [91].

It has been observed that a faster rise time leads to a higher peak motor overvoltage. However, this also results in a greater percentage of voltage being distributed across the first two turns of the motor winding. According to standard IEC 60034-18-41 [46], when the rise time is around 200 ns, the first two coils of a motor experience 40% of the voltage. Consequently, when a fast transient voltage is present at the motor terminals, the voltage distribution becomes uneven across each coil and turn [47, 89]. This uneven distribution indicates that the first few turns of the motor winding are more susceptible to insulation stress and PDs [96]. Thus, these regions of the winding face heightened risk, potentially leading to insulation degradation and related issues.

2.3.2 Passive Mitigation Solutions for Voltage Reflections

With the significant challenges posed by motor overvoltage, and the rising prominence of SiC MOSFETs known for their fast switching speeds, the need to mitigate motor overvoltage becomes even more critical [53]. Typically, to counteract the effects of the RWP, passive filters are commonly employed [104]. One approach involves implementing passive filters at the inverter terminal to extend the voltage rise time [40, 105]. Another method utilises impedance matching passive filters installed at the motor terminal [106]. These strategies are simple to implement and aim to safeguard the motor from harmful overvoltage conditions, ensuring its optimal performance and longevity.

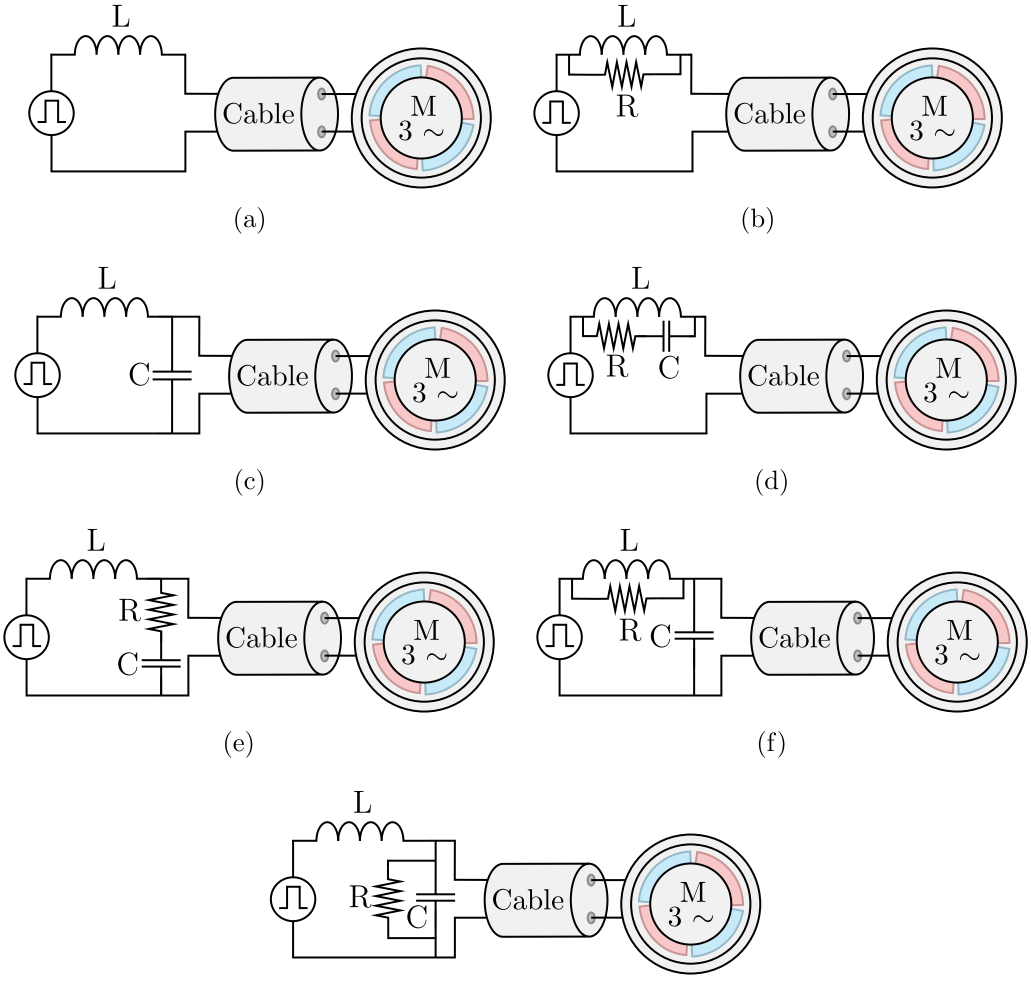
Passive Filters at Inverter Terminal

The main purpose of using passive filters at the inverter terminals is to increase the rise and fall times of the PWM voltage pulses [45]. Figure 2.8 illustrates various configurations of L, R, and C filters that can be employed to limit the $\mathrm{d}v/\mathrm{d}t$ and mitigate motor overvoltage.

The simplest and cost-effective approach involves implementing an output inductor L in series with the cable and motor, as depicted in Figure 2.8(a) [104, 105]. This configuration is designed to restrict the $\mathrm{d}v/\mathrm{d}t$ of the output voltage by increasing the voltage rise and fall times [107]. However, due to the entire load current passing through L, significant power losses occur. Additionally, this method can only limit the motor overvoltage to approximately 1.4 p.u., and achieving further limitation would necessitate a much larger inductance. Consequently, this would extend the damping time, leading to increased switching losses. Therefore, this makes this filter suitable for low switching frequencies and low cable length applications.

An alternative approach involves the use of an LR filter [56], illustrated in Figure 2.8(b), which offers improved mitigation of motor overvoltage. The resistor is carefully chosen to achieve impedance matching, while the value of L is designed based on the magnitude of voltage overshoot. However, precise parameter selection is crucial due to the impact of parasitic inductance of the resistor [105]. Additionally, this filter may result in increased switching losses.

Another commonly employed option in traditional motor drive systems (without the feeder cable) is the LC filter [104], depicted in Figure 2.8(c). LC filters are known for their cost-effectiveness and low losses [108]. However, when applied in cable-fed motor drive systems, they may not be the most optimal choice due to the potential risk of overvoltage arising from filter resonance [109]. Moreover, selecting the appropriate filter parameters becomes challenging to prevent resonance at low switching frequencies.



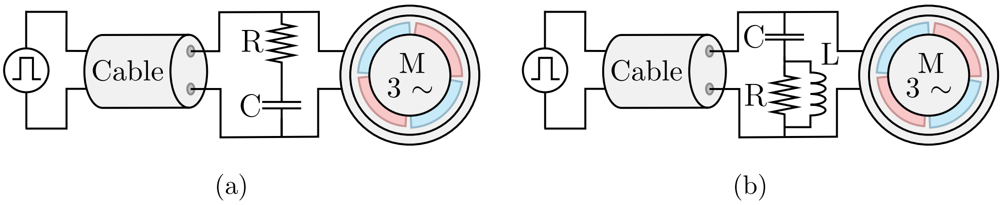
(a) (b) (c) (d) (e) (f) (g)

Figure 2.8: Different passive filters at inverter terminal. (a) L filter. (b) LR parallel filter. (c) LC filter. (d) LRC filter 1. (e) LRC filter 2. (f) LCR filter 3. (g) LRC filter 4.

The LRC filter, commonly known as the dv/dt filter, stands out as the most popular inverter-side filter in cable-fed systems [105, 110–112]. Its versatility is evident in the various combinations depicted in Figure 2.8(d)-(g). With the LRC filter, the RC network takes charge of impedance matching, while the output inductor effectively limits the dv/dt of the voltage pulses. The dv/dt filter proves highly effective in mitigating motor overvoltage. However, it comes with the tradeoff of experiencing high switching losses and power losses in the resistor [104].

Passive Filters at Motor Terminal

By implementing a long cable, the difference in characteristic impedance between the cable and motor gives rise to the RWP, which leads to motor overvoltage [36]. The fundamental idea behind impedance matching filters is to address this issue by ensuring that the motor terminal's equivalent characteristic impedance Z_m aligns with that of the cable Z_0 [106]. In doing so, the filters effectively prevent any reflections of fast-switched PWM voltage pulses at the motor terminals. The two popular impedance matching filters are the RC and RLC filter [104], as shown in Figure 2.9.



(a) (b)

Figure 2.9: Different passive filters at motor terminal. (a) RC filter. (b) LRC filter.

To ensure proper functioning of the RC filter, it is essential that the equivalent impedance of the filter matches the impedance of the cable, leading to:

$$Z_m = Z_0 = \sqrt{R_f^2 + \left(\frac{1}{j\omega_f C_f}\right)^2} = \sqrt{\frac{L_{cable}}{C_{cable}}} \tag{2.9}$$

where R_f and C_f are the filter resistance and capacitance [104]. Therefore, R_f needs to be carefully chosen to create an overdamped circuit, effectively preventing motor overvoltage at the motor terminals.

$$R_f > 2\sqrt{\frac{L_f}{C_f}} \tag{2.10}$$

In contrast, the RLC filter needs to match the cable impedance, but it necessitates an additional component, L. In terms of suppressing voltage overshoot, the RC filter proves to be more effective than the RLC filter [104, 105, 113]. Nevertheless, it is important to note that both filters lead to significant power losses.

Given these considerations, the selection of a passive filter at the inverter or motor terminal is not a straightforward decision and relies on the particular application. Additionally, except for the LC filter, all other passive filters lead to substantial power losses, prompting researchers to explore active mitigation methods.

2.3.3 Active Mitigation Solutions for Voltage Reflections

While passive filters offer ease of implementation and effective reduction of motor overvoltage, they come with a significant drawback of causing considerable power losses in motor drive systems. Additionally, their bulky nature may render them unsuitable for deployment in the demanding and harsh conditions that cable-fed systems often require. To address these issues, this section introduces active mitigation methods, namely multilevel inverters and active gate drivers, which aim to provide more efficient and adaptable solutions.

Multilevel Inverter

Multilevel inverters offer an effective solution to tackle motor overvoltage issues by increasing the number of steps in each PWM voltage transition, leading to the distribution of $\mathrm{d}v/\mathrm{d}t$ across each step. With a greater number of steps, the peak motor overvoltage will be reduced. An investigation into a three-level inverter revealed a peak motor overvoltage of 1.5 p.u., which is notably lower than the 2 p.u. peak motor overvoltage observed in two-level inverters [114].

For even more steps, the use of a modular multilevel converter comes into play, as it employs additional active switches to increase the number of steps. This approach has been studied in the context of mitigating motor overvoltage in cable-fed systems [115–117]. Nonetheless, it is essential to consider that this advantage is balanced by the necessity of more switches, leading to higher capital costs, lower reliability, and the requirement for larger heatsinks. Careful consideration of these factors is vital when implementing multilevel inverters to ensure an optimal solution for motor overvoltage control.

Quasi-Three-Level Inverter

It has been established that multilevel inverters, particularly the three-level inverter, reduce motor overvoltage. However, the conventional three-level inverter still exhibits a 1.5 p.u. motor overvoltage at long cable lengths [114]. To tackle this issue, a quasi-three-level (Q3L) PWM scheme for the three-level T-type inverter has been introduced in [40].

The Q3L PWM approach, ensures that the motor terminal receives two identical voltages, each with an amplitude of $0.5V_{dc}$. The middle voltage level during the rising and falling transitions is generated by the auxiliary branch of the T-Type inverter, shown in Figure 2.10. To achieve motor overvoltage mitigation, two identical pulses

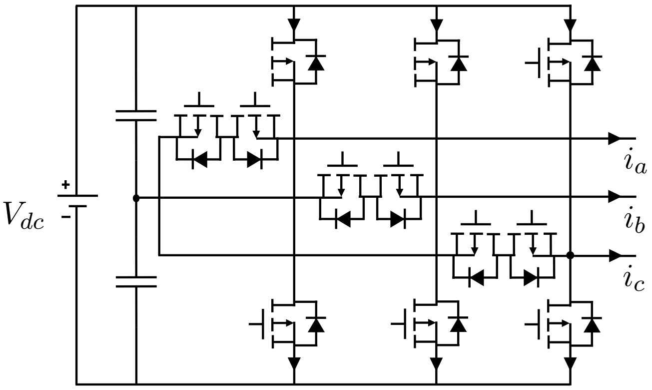


Figure 2.10: Three-level T-type inverter.

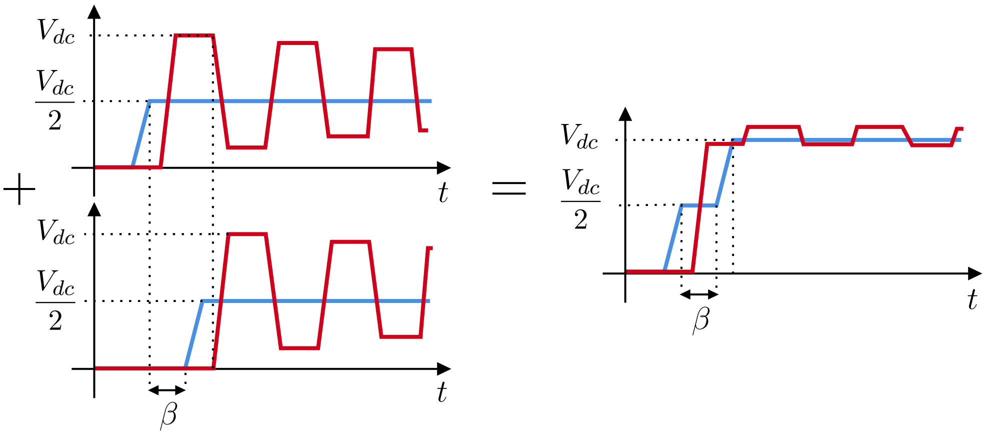


Figure 2.11: Q3L PWM Scheme for three-level T-type inverter.

with a pre-determined time delay β based on cable propagation t_p, typically set as $\beta = 2t_p$, are transmitted.

This technique strategically counterbalances the motor overvoltage resulting from each pulse, effectively canceling them out. Figure 2.11 illustrates the Q3L PWM scheme, wherein two rising voltage pulses with the time delay β are combined to yield the three-level pulse while successfully mitigating motor overvoltage to 1.2 p.u.

The Q3L PWM scheme has also been implemented in the single-phase H-bridge inverter without requiring any additional active switches [118]. This is possible since the H-bridge inverter utilises four active switches; however, it is not possible to utilise this PWM scheme for three-phases in a two-level inverter, due to the extra voltage step required.

Active Gate Driver

As a developing technology, active gate drivers have the capability to refine the switching transient process of power semiconductors, guided by feedback signals that reflect the system's operating state [119, 120]. Unlike conventional approaches, active gate drivers offer the flexibility to modulate the voltage slew rate dynamically, thereby enabling a more nuanced balance between EMI noise, switching loss and transient overvoltage. However, the switching transient of SiC devices can be finalised within a few nanoseconds. This necessitates meticulous design considerations for the circuit schematics, component bandwidth, control strategy, and timing strategy to ensure optimal performance [121].

Presently, four primary methods exist for managing voltage slew rates in active gate drivers: the variable gate resistance, variable gate capacitance, variable gate current and variable gate voltage approaches [121]. The variable resistance method is commonly employed to actively manage the switching process through adjustments in gate resistance. This method involves the use of multiple parallel resistors to modulate both the turn-on and turn-off phases. Nonetheless, the precision in controlling the $\mathrm{d}v/\mathrm{d}t$ may be compromised due to the limitations in gate resistor sizing. Furthermore, the gate capacitance approach, while attempting to regulate the voltage slew rate, inadequately does so and increases the risk of false triggering, especially when a large external capacitance is applied [122].

The variable gate current and gate voltage methods typically employ a variable current/voltage source to fine-tune the gate current or voltage during switching, thereby achieving precise control over the switching process. Nevertheless, these methods are challenged by the necessity for precise detection and management of the MOSFET's electrical characteristics, including currents and voltages. For effective regulation, the associated detection and feedback mechanisms must operate very fast, necessitating bandwidths that can reach up to 100 MHz to accommodate the dynamics of the switching events [123].

Therefore, whilst active gate drivers can be effectively implemented to control voltage slew rate, they come with a significant drawback — they can be costly and complex to design and implement [124]. Despite their benefits, careful consideration must be given to cost and complexity factors when deciding to incorporate them into a system.

2.4 Modelling of Reflected Wave Phenomenon

Accurate simulation modelling of cable-fed motor drive systems in the high-frequency range assumes a crucial role in addressing overvoltage and EMI concerns [55]. It is worth mentioning that motor overvoltage occurrences predominantly manifest at frequencies in the megahertz range. However, the currently available basic cable and motor models in simulation platforms such as PLECS (Plexim) and MATLAB/Simulink fall short in accurately predicting the magnitude and frequency of these overvoltages [42]. As a result, more sophisticated and detailed simulation models are required to provide precise insights into the behaviour of motor drive systems under high-frequency conditions [29]. By leveraging these advanced models, researchers and engineers can gain a deeper understanding of the overvoltage phenomena and devise effective strategies to mitigate their potential detrimental effects on motor drive systems.

2.4.1 Analysis of Reflected Wave Phenomenon

The analysis of the RWP in motor drive systems, extensively studied in the literature [48, 125, 126], provides valuable insights into the reflection of voltage waves and the mitigation of motor overvoltage in a cable-fed drive. In the high-frequency model, depicted in Figure 2.12, the inverter is represented as an ideal PWM source with a series impedance Z_i, while the cable is simplified as a lossless transmission line with a characteristic impedance Z_0 as given by the equation below.

$$Z_0 = \sqrt{L_{cable}/C_{cable}} \tag{2.11}$$

where L_{cable} (H/m) is the cable inductance and C_{cable} (C/m) is the cable capacitance.

To determine the per unit cable parameters, a high-frequency precision LCR meter can be utilised to measure the inductance and capacitance at various frequencies in both short circuit and open circuit conditions [126]. Appendix B provides further elaboration on this process, specifically tailored to the motor drive system employed in this thesis. On the other hand, the motor is represented as an impedance Z_m, incorporating factors such as stator winding leakage inductance, parasitic capacitance, and the resistances between the stator winding and motor frame, as well as between the stator neutral and motor frame [126].

The inverter PWM pulse, denoted as $V_s(s)$, is transmitted through the cable and represented as $V(0, s)$. After traversing a cable of length l (m), the voltage reaching

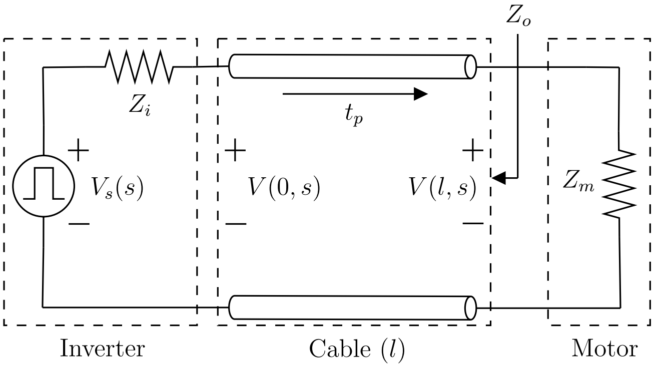


Figure 2.12: Simplified representation of cable-fed drive system.

the motor terminals is denoted as $V(l,s)$, with the propagation delay t_p given by [113].

$$t_p = l\sqrt{L_{cable}C_{cable}} \tag{2.12}$$

RWP implies due to the impedance mismatch between the cable and motor, reflections will occur at the motor terminal. Thus, successive reflections back and forth result in increased motor overvoltage. The reflection coefficients at the inverter terminals Γ_i and motor terminals Γ_m are denoted as:

$$\begin{aligned} \Gamma_i &= \frac{Z_i - Z_0}{Z_i + Z_0} \approx -1 \\ \Gamma_m &= \frac{Z_m - Z_0}{Z_m + Z_0} \approx 1 \end{aligned} \tag{2.13}$$

Under the assumption that the impedance of the inverter Z_i is much smaller compared to the impedance of the motor Z_m, and that Z_m is greater than the characteristic impedance Z_0 [113], the motor's power factor, Γ_m, can be approximated as approximately unity in large machines and 0.9 in smaller machines [85]. Consequently, it can be assumed that the voltage is completely reflected at both the inverter and motor terminals.

The voltage measured at the motor terminals, $V(l,s)$, can be expressed as the sum of all the forward traveling components, $V^+(l,s)$, and backward traveling voltage components, $V^-(l,s)$. Taking into account the propagation time, t_p, the following representation can be established using the motor reflection coefficient, Γ_m [127].

$$V(0,s) = V^{+}(0,s) + V^{-}(0,s) \tag{2.14}$$

$$\begin{aligned} V(l,s) &= V^{+}(l,s)e^{\tau s} + V^{-}(l,s)e^{-\tau s} \\ &= (1 + \Gamma_m e^{-2\tau s})V^{+}(l,s)e^{\tau s} \end{aligned} \tag{2.15}$$

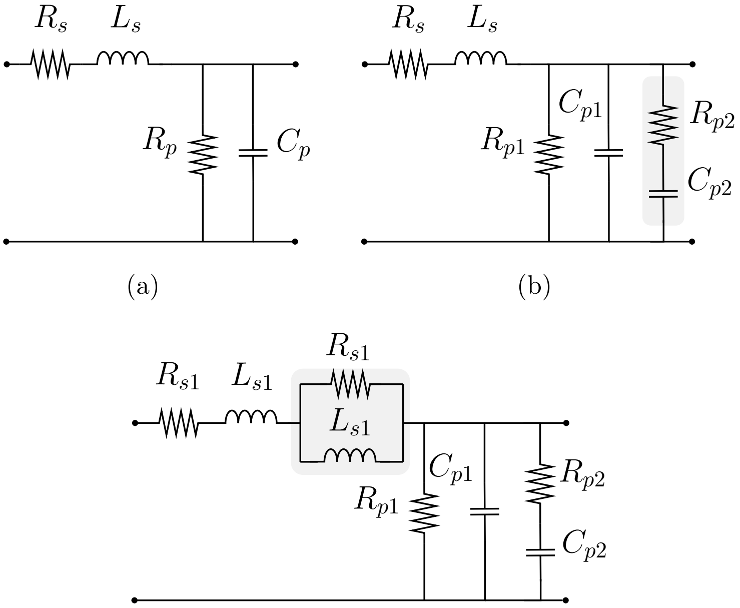
Therefore, the motor voltage reflections continue until they are fully damped to align with the inverter PWM voltage. The time required for damping depends on the ac skin resistance, proximity effects, and dielectric losses of the ac cable [126].

2.4.2 High-Frequency Cable Model

The study of modelling long cables for analysis in RWP has been an area of high interest [126, 128–131]. The conventional cable model, depicted in Figure 2.13(a), employs a simplistic approach consisting of a series resistance and inductance, alongside parallel conductance and capacitance [106]. While the simplicity of the equivalent circuit is beneficial, this model often overlooks the frequency-dependent nature of these components, a critical factor at high frequencies [126]. Moreover, its parameters are typically determined at the motor terminal's resonant frequency, which can vary based on cable length and might present challenges in accurate prediction. An improved cable model, introduced in [42], incorporates a high order parallel branch to represent the dielectric losses using as shown in Figure 2.13(b).

However, to achieve accurate predictions of motor overvoltage in cables, it is essential to consider frequency-dependent phenomena such as ac resistance, skin effect, and proximity effect. These factors play a significant role in shaping the cable's behavior and influencing the overvoltage characteristics in motor drive systems. To address these complexities, the simulation cable model presented in [126] is employed. This model shown in Figure 2.13(c), combines the parallel branch from Figure 2.13(b) and utilises higher order series branches to represent skin and proximity effects.

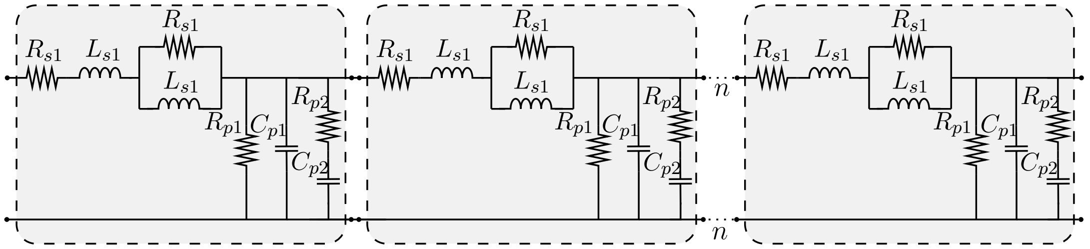
The parallel configuration allows the impedance of the cable to change with frequency. At low frequencies, the parallel inductor has a high impedance and the parallel resistor has a low impedance, so they have little effect on the total impedance of the cable. As frequency increases, the impedance of the inductor decreases and the impedance of the resistor increases, having a greater effect on the total impedance. If these elements were in series, they would affect the impedance at all frequencies, which is not characteristic for the skin and proximity effects.



(a) (b)

(c)

Figure 2.13: Per-meter DM cable models. (a) Conventional model. (b) Model considering dielectric loss [42]. (c) Model considering high-frequency phenomena [126].



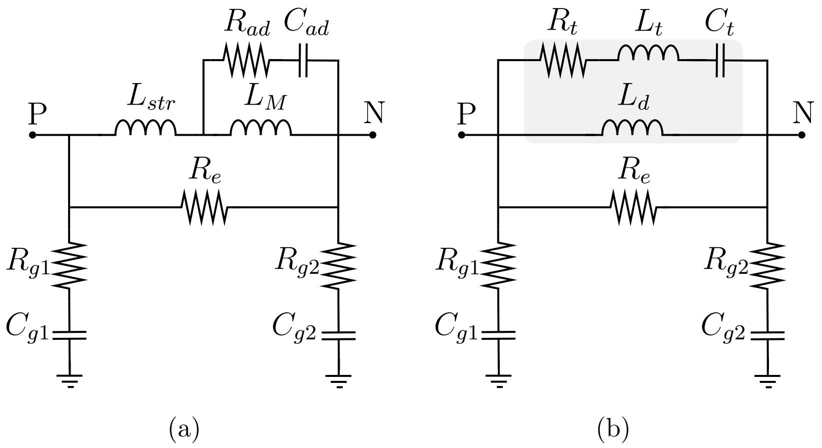
(a)

Figure 2.14: High-frequency cable model for simulation study. (a) per-meter cable mode. (b) Cascaded cable length model.

The incorporation of dielectric losses is represented by a high-order parallel branch containing resistor R_{p1}. The skin and proximity effects are taken into account through the high-order series inductor L_{s1} and resistor R_{s1}, respectively. To determine the model parameters, extensive measurements of the DM impedance characteristics are conducted across a wide frequency range, spanning from 100 Hz to 10 MHz. Further details on the parameter identification procedure are described in Appendix B.1, providing a comprehensive understanding of the model's accuracy with the experimental platform. Moreover, this versatile cable model can be cascaded multiple times, as shown in Figure 2.14, to accurately achieve the desired cable length for various system configurations.

2.4.3 High-Frequency Motor Model

Several motor models have been proposed in the literature to facilitate high-frequency EMI analysis and motor overvoltage prediction [126, 132–139]. The parameters of these models are determined based on the motor's impedance characteristics and/or geometric dimensions. Among these models, the one presented in [137], as shown in Figure 2.15(a), is gaining traction for its simple model structure and accuracy in high-frequency analysis. The additional resistance R_{ad} and capacitance C_{ad} form a series resonance with the stray inductance L_{str}. However, the parameters for R_{ad} and C_{ad} are difficult to obtain using analytical formulas, and usually require a trial and error approach in addition to frequency-domain simulations [137].



(a) (b)

Figure 2.15: High-frequency motor model per-phase for simulation study. (a) Model proposed in [137]. (b) Model with simpler parameter identification [126].

The model introduced in [126], depicted in Figure 2.15(b), adapts and improves this high-frequency motor model by introducing a series R_t, L_t and C_t branch to replace the R_{ad} and C_{ad} branch, retaining the model's accuracy. Since this new series branch has its own resonance, analytical calculation of parameters can be carried out in a more straightforward way from the measured impedance's. For this reason, this motor model is selected for predicting RWP in this thesis due to its ability to accurately capture the high-frequency DM and CM impedance characteristics. Moreover this offers a straightforward parameter identification method, making it easily reproducible for further investigations.

Specifically, the motor model shown in Figure 2.15(b) includes several critical components to account for various parasitic effects and high-frequency phenomena. The parasitic resistance and capacitance between the stator winding and motor frame are represented by R_{g1} and C_{g1}, respectively. Similarly, R_{g2} and C_{g2} model the parasitic resistance and capacitance between the stator neutral and motor frame. To capture the stator winding leakage inductance, the model incorporates L_d, while R_e accounts for the high-frequency iron loss of the stator winding. Additionally, to address the second resonance in the motor impedance characteristic, possibly induced by skin effect and inter-turn capacitance of the stator windings, the parameters L_t and C_t are included.

These components play a pivotal role in shaping the motor model's accuracy and enable the simulation to capture critical high-frequency effects and parasitic behaviours in the motor drive system. As such, determining these parameters is crucial for precise motor overvoltage prediction and reliable EMI analysis in high-frequency scenarios. Additional insights into the parameter identification process are provided in Appendix B.2.

2.5 Summary

This chapter explored modulation methods and inverter design techniques crucial for improving the efficiency and reliability of SiC-based motor drives. This began with an in-depth look at VSF-PWM, a popular approach designed to address the uneven ac current ripple associated with CSF-PWM and improve system efficiency. Additionally included is a methodology for predicting current ripple in PMSM drives, enriching the understanding of VSF-PWM.

The high $\mathrm{d}v/\mathrm{d}t$ of SiC MOSFETs, while beneficial for reducing switching losses, can pose technical challenges such as motor overvoltage in cable-fed motor drives. To address this, mitigation strategies are presented. Subsequently, a high-frequency modelling approach for cables and motors is discussed for simulation studies. A detailed modelling framework is provided, and further information on parameter extraction can be found in Appendix B.

Chapter 3

Experimental Test Setup

3.1 Introduction

The purpose of this chapter is to provide a high-level overview of the experimental platform used in this thesis. It offers comprehensive descriptions and specifies the parameters of the SiC-based motor drive system. Additionally, the chapter elaborates on the control platform, outlining its design principles and discusses how it integrates with the motor drive system. The aim is to provide an understanding of the system's capabilities and the technical considerations involved in experimental validation. This test setup provides a foundation for examining the modulation, control, and inverter design within applications in the automotive (Chapters 4 and 5) and marine sectors (Chapter 6).

3.2 System Overview

In this thesis, a 1.23 kW experimental SiC-based motor drive system operating in a closed-loop configuration is used to validate the simulation findings discussed in Chapters 4 through 6. Figure 3.1 presents a detailed view of the experimental setup under controlled conditions. The system's design integrates a personal computer (PC) for operational control, a motor drive, and advanced feedback mechanisms, highlighting the setup's capacity to provide valuable insights into motor drive performance.

Within this system, two 1.23 kW PMSM motors are connected back-to-back in a series configuration. This setup is a regenerative test platform where a primary motor, driven by an inverter, is mechanically coupled to a secondary motor operating as a generator with a resistive load bank attached. The primary motor converts electrical energy from the inverter into mechanical energy, generating torque to drive

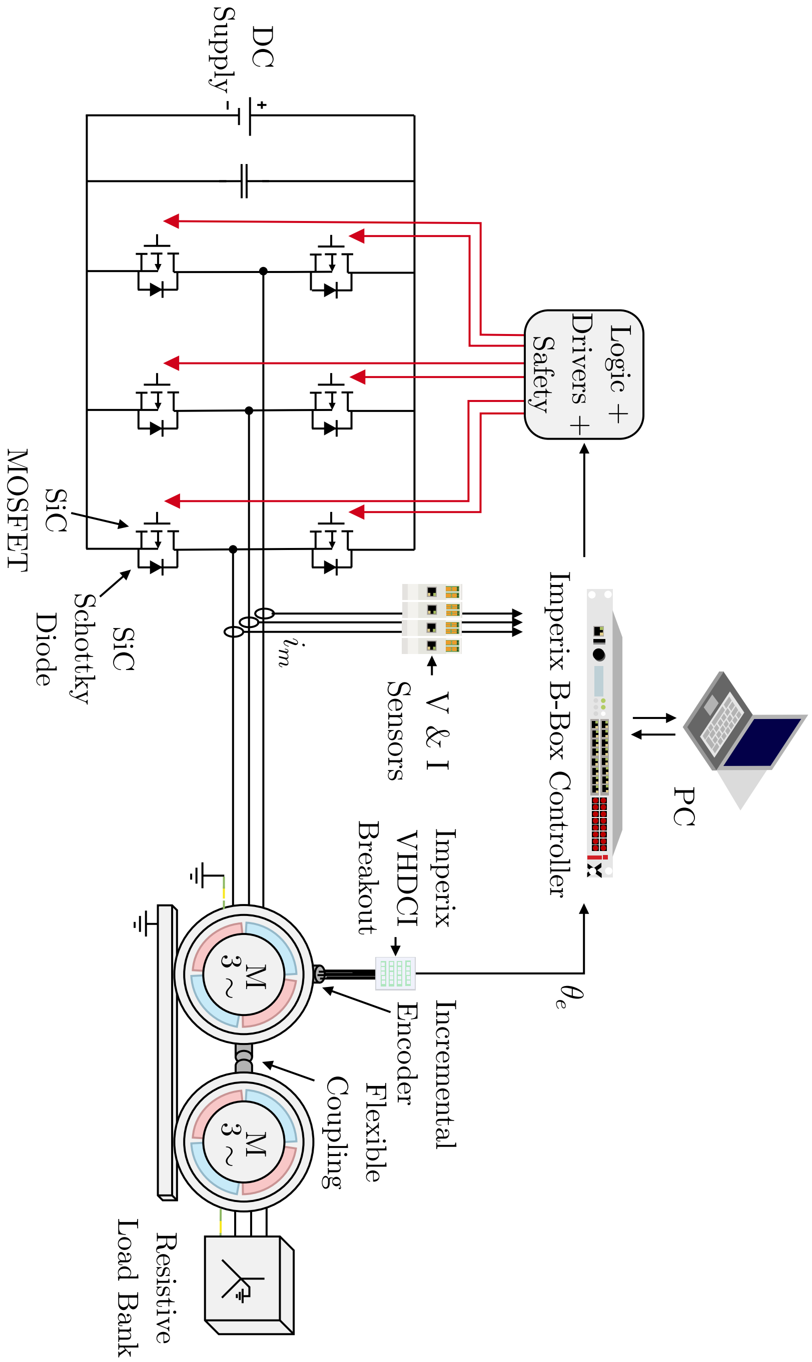


Figure 3.1: Overview of experimental setup.

the secondary motor. The secondary motor, in turn, generates electrical energy due to electromagnetic induction, providing a counteracting torque; the attached resistive load bank allows for dissipation of this generated energy and control over the load experienced by the primary motor. A flexible coupling is used to connect the motors, allowing compensation for any misalignment or angular displacement between their shafts.

The primary motor operates under a three-phase inverter's control and is set up for closed-loop field-oriented control, allowing it to adhere to a specified reference speed. It is equipped with a high-resolution incremental encoder that delivers the electrical angle, thereby facilitating the determination of measured speed. These measurements are processed by a digital signal processor (DSP), the Xilinx Zynq 7030 SoC [140], housed within the Imperix B-Box controller. This DSP is responsible for creating the drive signals that are subsequently transmitted to the SiC MOSFET power switches. Additionally, Tektronix TCP0020 50 MHz probes are utilised for real-time measurements with the Tektronix MSO58 oscilloscope. To evaluate the measured efficiency of the motor drive, the Yokogawa WE1806 power analyser was utilised. Figure 3.2 presents a photograph of the testing setup in the laboratory.

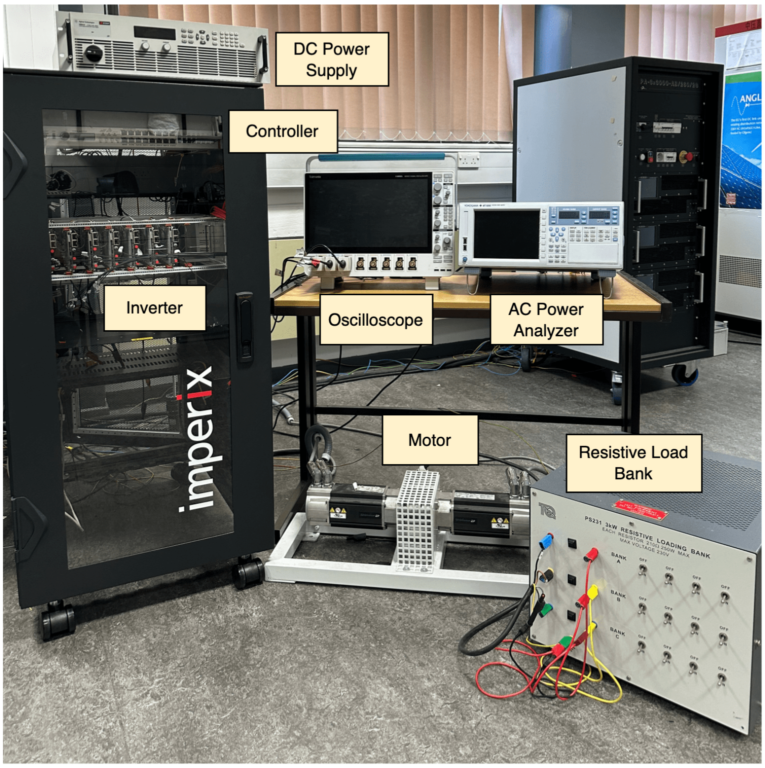


Figure 3.2: Experimental test bench of motor drive system.

3.2.1 Power Converter

The power converter incorporates three 800 V/ 24 A PEB8024 half-bridge modules by Imperix, featuring seamless plug-and-play integration with the Imperix B-Box RCP programmable controller. These modules are equipped with optical fiber PWM inputs, and galvanic isolated onboard sensors, which deliver analog measurements of dc voltage and ac output current. Additionally, the modules are designed with built-in protections to safeguard against over-current, over-voltage, and over-temperature conditions. Figure 3.3 shows a visual representation of the module layout.

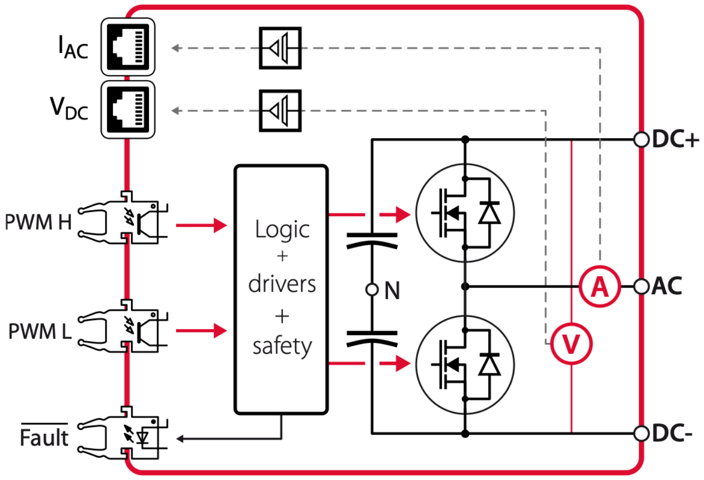


Figure 3.3: Schematic overview of the PEB 8024 module [141].

The measured ac current is utilised in field-oriented control via RJ45 connections, while the dc voltage is employed exclusively in space vector modulation. It is noteworthy that the modules are equipped with large dc-link capacitors, a design choice aimed at minimising dc voltage ripple, thereby enhancing the overall system stability and efficiency. The ac connection is directly linked to the corresponding motor phase, and the dc connections are interfaced with two additional PEB8024 modules to construct a three-phase inverter and a high-voltage dc power supply.

Table 3.1: Power Converter Main Components [141]

Component	Devices
Power switches	2x Cree C2M0080120D [142]
Capacitors	1x 235 μF at 800 V (2 banks of 10x47 μF each)
Drivers	2x Texas Instruments ISO5452-Q1 [143]
Current sensor	1x LEM LKSR50-NP [144]
Voltage sensor	1x Resistive divider + TI AMC1311B [145]
Cooler	1x Dynatron G199 [146]

3.2.2 Controller Architecture

The field-oriented control system has been modeled using MATLAB/Simulink and PLECS, employing the Imperix automated code generation (ACG) software development kit for efficient development. This integration facilitates direct programming of Imperix B-Box controllers via Simulink or PLECS, enabling precise simulations ahead of experimental validation. Deployment of the code to the controller is achieved through the Cockpit software, utilising an RJ45 Ethernet connection for communication between the PC and the controller. Additionally, Cockpit offers real-time interaction and monitoring capabilities from the host PC.

The Imperix B-Box controller utilises the AMX/Xilinx Zynq 7030 SoC [140], which integrates a dual-core ARM processor (CPU) and a Kintex-based programmable logic (FPGA). User-defined control tasks operate on the CPU, while the FPGA handles low-level and time-sensitive tasks, such as PWM modulation or interlock safety mechanisms. This results in a fast floating-point processor DSP to power converter control, capable of operating at high switching frequencies in closed-loop operation. For a comprehensive understanding of the controller architecture utilised in the motor control, a detailed diagram is included in Figure 3.4 to illustrate the components and their interconnections.

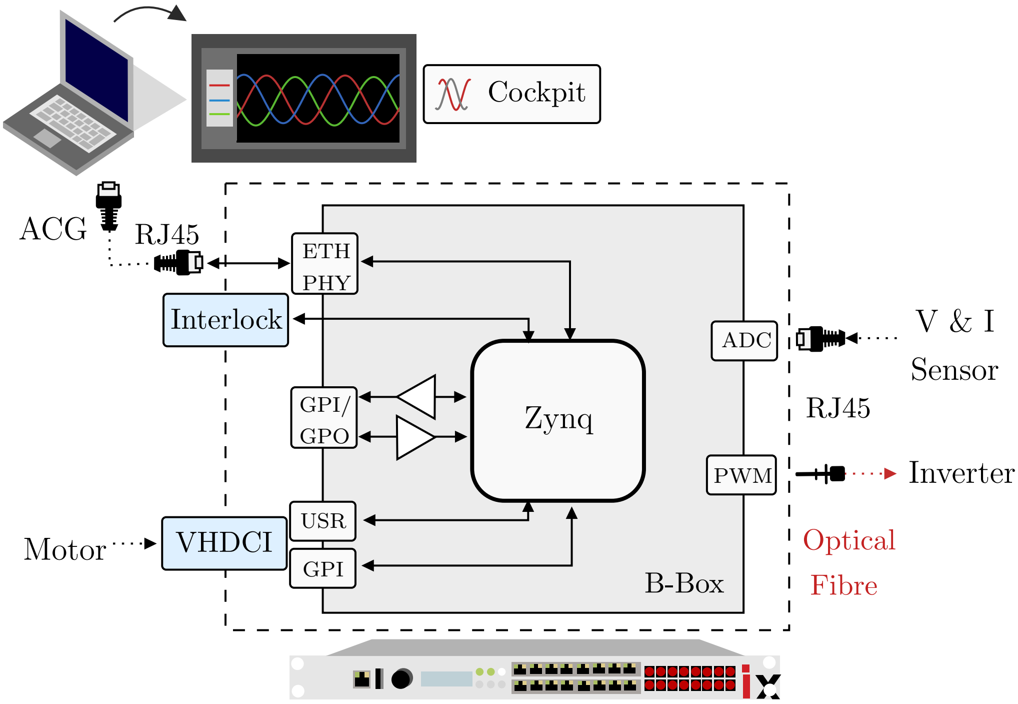


Figure 3.4: Controller architecture.

The incremental encoder attached to the motor interfaces with the VHDCI port's GPI inputs through a dedicated VHDCI adapter board. This setup allows for precise tracking and management of motor position and speed. Furthermore, critical parameters such as current and voltage are monitored by connecting to the system's analogue inputs using RJ45 connectors. These measurements, including the rotor angle, current, and voltage, are integral to the implementation of field-oriented control within the Simulink ACG environment. Optical fibre PWM outputs are directly linked to Imperix's integrated gate drivers, which are designed for SiC MOSFETs. By leveraging optical fibers, the system not only eliminates EMI in the PWM signals, a common issue in high-speed electronic systems, but also ensures the signal integrity.

3.2.3 Control Algorithm Implementation

Utilising the Imperix Simulink ACG, the Simulink Coder engine facilitates the automatic generation of C++ code during the model's compilation process. It configures both the analog and digital inputs/outputs for the B-Box RCP controller, where analog signals are sampled according to the control period CTRLPERIOD, and digital PWM outputs operate at the frequency of the provided clock. Following the generation and compilation of the C++ code, the Cockpit software uploads the executable to the B-Box controller. As illustrated in Figure 3.5, this process outlines the implementation of the SVPWM control strategy within this thesis, laying the foundational framework for the discussion that follows in subsequent chapters.

The CONFIG block specifies an ADC clock signal, which is required to be linked to the clock input of all ADC blocks. Additionally, this supplies a PWM clock signal that must be connected to the clock input of all PWM blocks. This is essential to configure the control task frequency and ADC sampling. Subsequently, the ADC input blocks captures the analog inputs from the corresponding channels on the Imperix controller. Similarly, the configurable SVPWM block determines the output channels for the optical fiber PWM signals, taking into account the clock frequency.

The rotor angle is determined using quadrature-encoded signals generated by the motor's incremental encoder. Subsequently, the rotational speed, ω_r, is derived within the user application from the observed rotor angle, θ_e. Given that the rotor speed represents the angle's rate of change, it is computed by evaluating the difference in the angle measurements across two consecutive samples.

$$\omega_r(k) = \frac{\theta_e(k) - \theta_e(k-1)}{T_s} \tag{3.1}$$

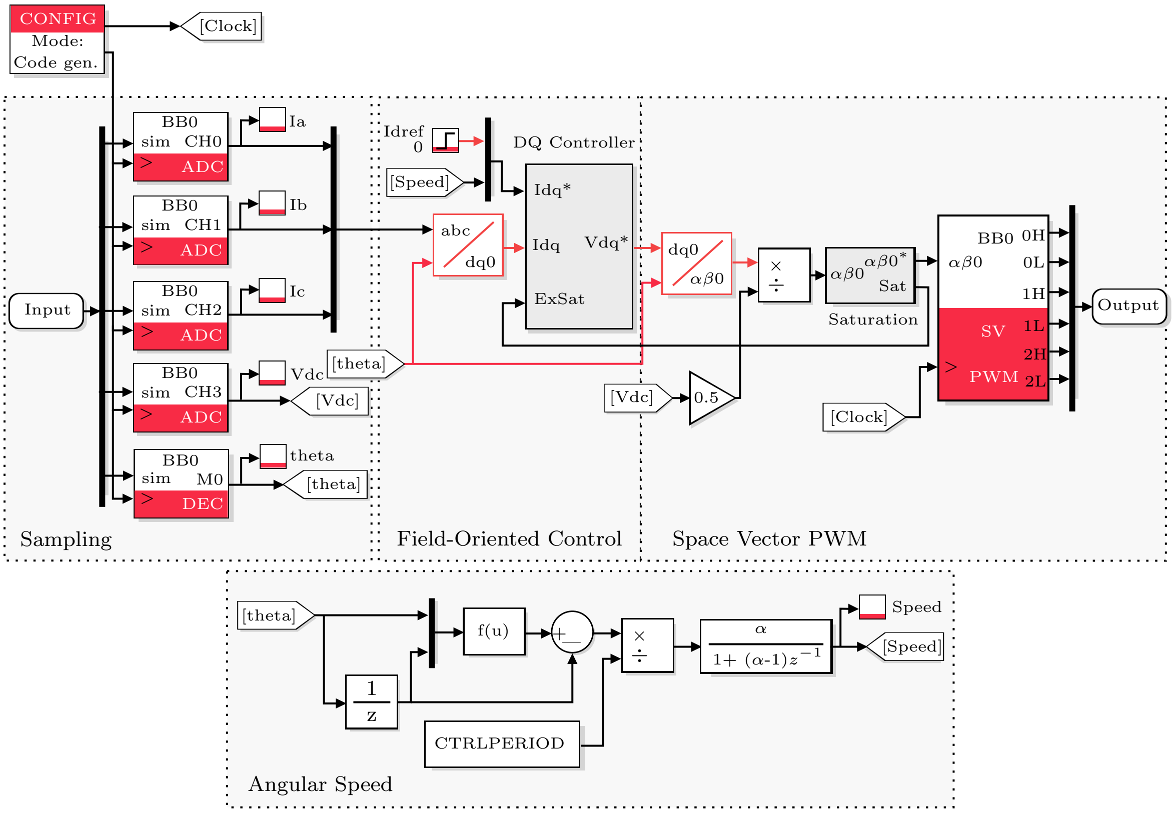


Figure 3.5: Imperix Simulink ACG for SVPWM control of motor drive.

To minimise the effects of quantisation errors from the angle incremental encoder on the speed value, filtering is required. For this reason, an infinite impulse response filter is used, where α is determined based on the cutoff frequency $f_c = 1/(2\pi t_c)$ and the sampling period $T_s = 2$ µs. To note the value of f_c varied throughout this thesis based on the system design.

$$\alpha = \frac{T_s}{T_c + T_s} = \frac{2\pi f_c T_s}{1 + 2\pi f_c T_s} \tag{3.2}$$

The following Simulink function addresses discontinuities in the measured angle:

$$f(u) = u(1) + 2\pi\Big(\big(u(1) - u(2)\big) < -\pi\Big) - 2\pi\Big(\big(u(1) - u(2) > \pi\big)\Big) \tag{3.3}$$

3.3 Hardware Parameters

The specifications and parameters for the hardware are detailed in Table 3.2. The parameters for the inverter, motor and load are utilised throughout this thesis, serving as foundational elements in all chapters. Meanwhile, the cable parameters are of particular importance and relevance to the discussions presented in Chapter 6.

3.4 Summary

This chapter presented the test system utilised for the experimental validation of the research conducted in this thesis, offering a high-level summary centered on the components and control of the motor drive. The experimental validation's control system was executed using the Imperix Simulink ACG. Additionally, the Imperix platform facilitates the real-time visualisation of chosen variables through the Cockpit software. Finally, specifics regarding the motor drive's parameter values, as employed consistently throughout the thesis, are provided.

Table 3.2: Motor Drive Parameters

	Parameter	Value
Supply	DC power supply	Keysight N8944A [147]
Inverter	SiC MOSFET	Cree C2M0080120D [142]
	DC voltage V_{dc}	300 V
	Fundamental frequency f	50 Hz
	Modulation index m_i	0.8
	Output capacitance C_{oss}	92 pF
	ON-state resistance $R_{ds,on}$	80 mΩ
	External gate resistance R_{g-ex}	2.5 Ω
	Internal gate resistance R_{g-in}	3.9 Ω
	Gate drive turn-on voltage V_{ggh}	20 V
	Gate drive turn-off voltage V_{ggl}	-5 V
Motor	Control Techniques model no.	095U2B300BACAA100190
	Type	AC PMSM
	Rated power	1.23 kW
	Rated phase voltage	400 V
	Rated phase current	2.7 A
	Rated torque	3.9 Nm
	Rated speed	3000 rpm
	Pole pairs p	3
	Stator resistance	3.4 Ω
	Stator inductance L_d, L_q	12.15 mH
	Kt	1.6 Nm/A
	Ke	98 V/krpm
	K_{s-EC}	2.214×10^{-3} W/V^2
	K_{s-hys}	4.4 W/V
	n	1.642
	PM flux	0.25 Wb
	Moment of inertia	2.9 kg cm^2
	Encoder	Incremental with 4096 ppr
Cable (Ch. 6)	Type	Lapp 4 core unscreened [148]
	Lengths	5 m, 10 m, 15 m, 20 m
	Gauge	16 AWG
	Per meter inductance L_{cable}	0.26 μH
	Per meter capacitance C_{cable}	104.9 pF
Load	Three-phase resistive load bank	Tecquipment PSA50 [149]

Chapter 4

Optimisation of Switching Frequency for Improved Efficiency

The research presented in this chapter provides significant insights into efficiency optimisation for high-performance SiC-based motor drive systems predominantly used in automotive applications. To achieve this objective, a comprehensive analysis is conducted to understand the relationship between the switching frequency of the inverter and its impact on system losses. Initially, through simulation studies, this chapter establishes that an increase in switching frequency results in higher inverter switching losses. Conversely, it is observed that higher switching frequencies lead to lower motor copper losses. With these relationships in mind, a novel closed-loop control scheme that incorporates a VSF-PWM strategy is implemented, leveraging an offline lookup table to dynamically adjust the switching frequency in response to the loss tradeoff. The effectiveness of this approach is further validated through experimental results, which show an enhancement in the overall efficiency of the motor drive system.

4.1 Introduction

To enhance energy conservation and improve performance within automotive applications, the industry is witnessing a significant shift towards motor drives that offer high efficiency and power density [13, 150, 151]. This evolution is underscored by a growing demand for technologies that not only meet these requirements but also push the boundaries of what's possible in terms of power electronic systems. Leading these innovations are SiC MOSFETs, which have emerged as a highly promising solution to the challenges of energy conservation and performance enhancement [152, 153]. SiC MOSFETs are favored for their reduced switching and conduction losses, especially at high switching frequencies, compared to traditional Si IGBTs [154]. This advantage is crucial in automotive applications where high switching frequencies can lead to reduced current harmonics, enhanced power quality, and the possibility of using smaller, more compact filters [17, 58].

Given the critical role of inverters in three-phase systems, the conventional choice has often been CSF-PWM, owing to its simplicity in system design and control. However, a new area of research interest that has emerged is VSF-PWM, offering the potential to minimise harmonic distortions and enhance the dynamic response of power electronic systems [155, 156]. Its capability for dynamic adjustment of switching frequency based on system operating conditions further facilitates improved efficiency under varying load conditions, thereby enabling the achievement of specific performance objectives. This flexibility opens up new avenues for system optimisation and power quality improvement.

Despite the promising attributes of SiC MOSFETs and the potential of VSF-PWM, the literature reveals a gap in comprehensive exploration, particularly in the integration of SiC MOSFETs with optimised VSF-PWM strategies. Previous research predominantly focused on varying the switching frequency based on criteria such as current ripple [30], torque ripple [32, 52], and circulating current [31], with less emphasis on tailoring SiC MOSFET switching frequency based on system losses. Moreover, while the concept of adjusting the switching frequency to balance inverter and motor losses has been briefly addressed with GaN field-effect transistors [157, 158], a thorough investigation using SiC MOSFETs remains unexplored. This gap signifies a substantial opportunity to enhance inverter efficiency, especially in the context of operational motor drive systems [2, 159].

This chapter aims to bridge this gap by utilising precise loss modelling simulations, employing tools such as PLECS (Plexim) and MATLAB/Simulink, to discern the trade-off between inverter and motor losses across various switching frequencies. The aim is to identify the optimal switching frequency for SiC MOSFETs that maximises the motor drive system's overall efficiency. To achieve this, the proposed VSF-PWM method considers motor loading conditions, including rotor speed and torque load, to dynamically adjust the switching frequency through an offline lookup table derived from the motor drive system's profile. The effectiveness of this strategy is substantiated through simulation studies and experimental analysis, focusing on an ac PMSM.

By providing a comprehensive understanding of the benefits and implications of VSF-PWM in power electronic systems, this chapter aims to advance the modulation techniques in power electronic systems. In doing so, this lays the foundation for future innovations in high-performance and energy-efficient automotive applications.

4.2 Mathematical Modelling of Drive System Losses

Within a conventional motor drive system, achieving optimal efficiency requires a comprehensive understanding of power losses in the inverter and the motor. This section delves into the mathematical representations of loss models tailored to a PMSM drive system. By accurately modelling and quantifying these losses, it becomes possible to identify areas for efficiency improvement and optimise the overall system performance.

4.2.1 Inverter Loss Modelling

Switching losses $P_{m,sw}$, which occur during the MOSFET switching transitions, are a significant contributor to overall power losses. To accurately quantify switching losses, parameters such as the E_{on} and E_{off} switching energies of the MOSFET and the reverse recovery energy E_{rr} of the power diode are considered. These values are typically provided by the manufacturer and are obtained from the datasheet of the specific MOSFET used in the inverter design [142]. The values of these switching energies depend on the properties of the MOSFET and i_d. The conduction losses $P_{m,cond}$ are determined by summing up the average losses, which take into account the specific on-resistance $R_{ds,on}$ and average forward threshold voltage V_{on} of both the diode and MOSFET [160, 161].

$$P_{m,sw} = \frac{6}{\pi}\big(E_{on} + E_{off} + E_{rr}\big) f_{sw} V_{dc} i_d \tag{4.1}$$

$$P_{m,cond} = 6\Big[\Big(\frac{1}{\pi}V_{on} + \frac{1}{4}R_{ds,on} i_d\Big) i_d\Big] \tag{4.2}$$

The efficiency of the inverter η_{inv} is determined using the input power P_{in} and the total inverter losses, which are the sum of $P_{m,sw}$ and $P_{m,cond}$.

$$\eta_{inv} = \frac{P_{in} - P_{m,sw} - P_{m,cond}}{P_{in}} \times 100; \quad P_{in} = V_{dc} I_{dc} \tag{4.3}$$

4.2.2 Motor Loss Modelling

The primary losses in a three-phase motor include copper losses P_{Cu} and core losses P_{Fe}, both of which are crucial factors in assessing the overall power dissipation and efficiency of the motor. Core losses, a significant contributor to the total losses, is further divided into two main components: eddy current losses P_{EC} and hysteresis losses P_{hys}. The core losses are given by $P_{Fe} = P_{EC} + P_{hys}$. These losses depend on the flux level inside the PMSM and ω_r [162]. To accurately calculate these losses, they are evaluated in the *dq*-axis reference frame, which allows for a more precise representation of the losses. This reference frame is based on the frequency of the stator currents, taking into account the effects of flux variations and ω_r, given as:

$$P_{EC} = k_{s-EC}\omega_r^2\lambda_{\mathrm{dq}}^2 \tag{4.4}$$

$$P_{hys} = k_{s-hys}\omega_r\lambda_{\mathrm{dq}}^n \tag{4.5}$$

In the given equation, λ_{dq} represents the flux linkages in the *dq*-axis. The value of the exponent n depends on the core material properties, reflecting the unique characteristics of the specific motor design. To determine the coefficients for eddy current losses k_{s-EC}, hysteresis losses k_{s-hys}, as well as the value of the exponent n, there are two common approaches. The first approach involves utilising FEM analysis techniques to simulate the motor's electromagnetic behaviour and calculate the loss coefficients. The second approach involves experimental measurements, which require conducting tests on physical motor prototypes to directly quantify the loss coefficients [163, 164].

Unlike the stator iron losses P_{Fe}, obtaining an analytical expression for the rotor core losses is not feasible, and experimental estimation of these losses poses significant challenges. However, in the context of a synchronous motor, the rotor core losses are generally considered to be insignificant [165]. This is attributed to the rotor's operation at synchronous speed, resulting in an exceedingly small slip speed and rotor frequency. Additionally, the rotor core experiences lower magnetic flux densities and occupies a smaller volume compared to the stator core. Consequently, the focus is primarily directed towards considering the stator losses.

Stator copper losses are a significant component of power loss in electrical machines and systems. In dc systems, where current flow is constant, copper losses are relatively straightforward to calculate using the formula $P_{Cu} = I^2R_{dc}$, where R_{dc} represents the dc resistance of the conductor. Since this resistance remains unchanged regardless of frequency in a dc circuit, the calculation is simple. However, the situation is markedly different in ac systems, particularly in ac motors. Here, the copper losses are determined by the equation:

$$P_{Cu} = \frac{3}{2}R_s\left(i_{sd}^2 + i_{sq}^2\right) \tag{4.6}$$

where R_s denotes the stator resistance, and i_{sd} and i_{sq} are the dq-axis currents, influenced by the angular relationship between the stator currents and the dq-axis. Unlike in dc systems, R_s in ac motors is not a constant but varies with frequency due to the skin and proximity effects, necessitating a frequency-dependent analysis of R_s. This analysis must consider the conductor's geometry, the operating frequency, and the conductors' relative positioning within the magnetic fields to accurately calculate ac copper losses.

The intricacies of calculating losses in ac systems are compounded by skin and proximity effects, which become more pronounced with increased switching frequencies [166]. The skin effect leads to ac current concentrating near the conductor's surface, effectively reducing the cross-sectional area for current flow and increasing resistance. Concurrently, the changing magnetic fields induce eddy currents in nearby conductors, further influencing the current distribution and resistance. This scenario underscores the substantial rise in power losses at higher switching frequencies, a phenomenon that begins to manifest even at relatively low frequencies [167]. However, it is important to highlight that simulation results in Chapters 4 and 5 focus solely on dc copper loss. For enhanced accuracy, considering ac loss is also crucial.

Mitigation strategies for these ac effects include the selection of conductors with dimensions tailored to minimise these losses. Specifically, choosing a conductor diameter smaller than the skin depth, δ, calculated as:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}} \tag{4.7}$$

where ρ represents the electrical resistivity, and μ_0 and μ_r are the permeability of free space and relative permeability of the conductor, respectively, can significantly reduce the skin effect. Addressing the proximity effect involves optimising conductor positioning within their slots and possibly utilising windings made of parallel strands or Litz wires composed of thinner strands wired together. While the adoption of such windings introduces challenges, such as increased manufacturing complexity and potential for uneven current distribution, it also facilitates a higher fill factor and can be more cost-effective compared to alternatives like Litz wire [167].

The efficiency of the motor η_{mot} can be determined using the total motor losses, which is simplified as the sum of P_{Fe} and P_{Cu}:

$$\eta_{mot} = \frac{P_{m,in} - P_{Fe} - P_{Cu}}{P_{m,in}} \times 100; \quad P_{m,in} = P_{in} - P_{m,sw} - P_{m,cond} \tag{4.8}$$

4.2.3 Total Power Loss

The total power losses $P_{loss,t}$ and system efficiency η_{sys} of the motor drive are related by the motor losses $P_{loss,m}$ and inverter losses $P_{loss,inv}$:

$$P_{loss,t} = \underbrace{\left[P_{Cu} + P_{EC} + P_{hys}\right]}_{P_{loss,m}} + \underbrace{\left[P_{m,sw} + P_{m,cond}\right]}_{P_{loss,inv}} \tag{4.9}$$

$$\eta_{sys} = \frac{P_{in} - P_{loss,t}}{P_{in}} \times 100 \tag{4.10}$$

4.3 Analysis of System Losses Influenced by Switching Frequency

4.3.1 Simulation Setup

This section aims to comprehensively investigate the influence of switching frequency on both inverter and motor losses in a SiC-based motor drive system. To achieve this objective, a co-simulation approach is employed using PLECS (Plexim) and MATLAB/Simulink. This framework enables accurate simulation of the inverter in PLECS (Plexim), considering precise loss modelling of switching and conduction losses based on manufacturer datasheets and multi-dimensional lookup tables. The PMSM is modelled in MATLAB/Simulink, utilising machine state equations to estimate power losses associated with the motor. In addition, field-oriented control is employed to decouple motor flux and torque, using the dq-axis, simplifying motor control. The loss calculations from the inverter and motor are inputted into MATLAB, where the results are graphically plotted. This setup is illustrated in Figure 4.1, showcasing the function of each simulation platform.

This comprehensive co-simulation setup facilitates a detailed analysis of the interplay between switching frequency, inverter losses, and motor losses, contributing to a deeper understanding of overall system performance. Table 3.2 in Chapter 3 provides detailed system parameters for the inverter and motor. For the purposes of the simulation study, the dc voltage is set at 300 V, alongside a modulation index of 0.8.

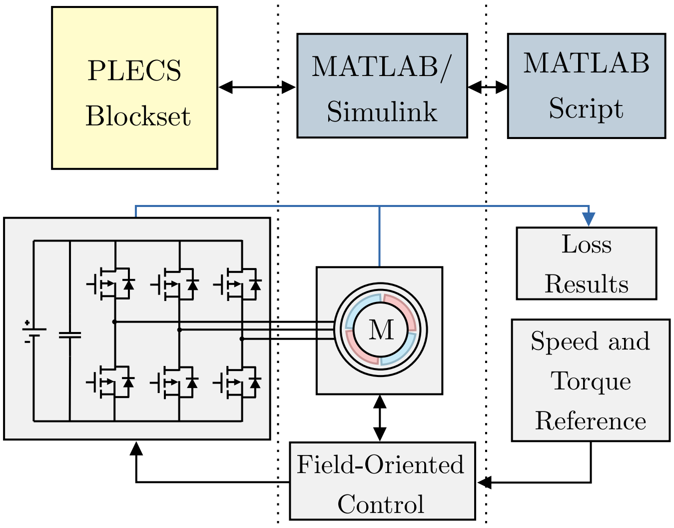


Figure 4.1: MATLAB and PLECS co-simulation setup.

While co-simulation leverages the computational strength of both MATLAB and PLECS's, assuming accurate models, parameters, the use of ideal components, and steady-state initial conditions, it encounters limitations. These include computational demands, difficulties in accurately modelling non-linear behaviors, variations due to real-world discrepancies, and sensitivity to the simulation time step. Nonetheless, this approach remains valuable for the detailed analysis and design of motor drives, with careful consideration for the assumptions and limitations to ensure real-world applicability of the simulation results.

The field-oriented control used in simulation is shown in Figure 4.2. The i_q current is aligned perpendicular to the rotor's magnetic field and is directly responsible for controlling the torque of the motor. By controlling i_q, the system can control the motor torque very precisely. The i_d current is aligned parallel to the rotor's magnetic field and is responsible for controlling the magnetic flux in the motor. Since this thesis uses a non-salient pole motor, the motor does not exhibit any significant reluctance torque, which is the torque due to the difference in inductance. Since the rotor permanent magnets provide the necessary magnetic flux adding any additional i_d does not significantly enhance the motors magnetic field. Therefore to maximise torque per ampere efficiency, this reference is set to zero.

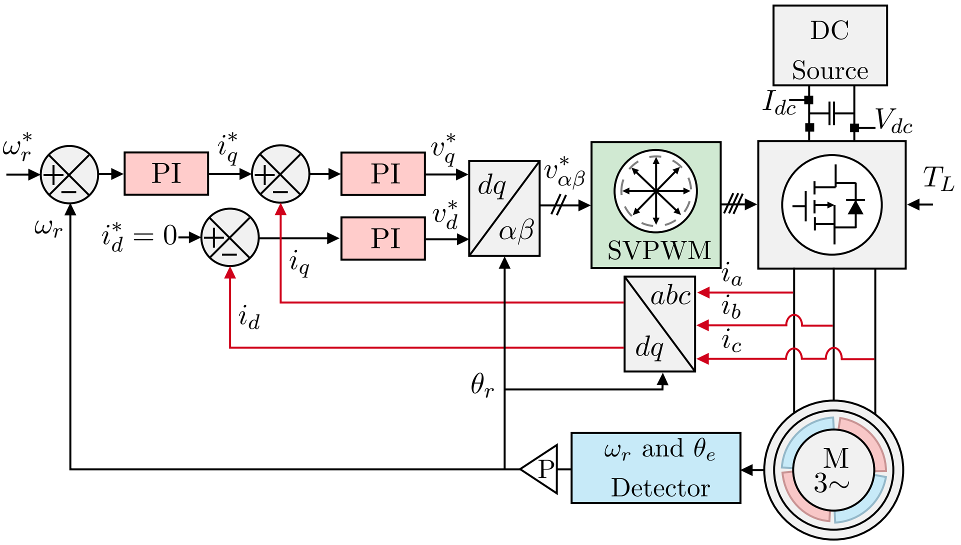


Figure 4.2: Field-oriented control and motor drive setup.

The electrical torque T_e is generated by the motor, based on the interaction between the motor's magnetic flux linkage and stator currents, as follows

$$T_e = \frac{3}{2} p(\lambda_{sd} i_{sq} - \lambda_{sq} i_{sd}) \tag{4.11}$$

The load torque reference T_L is applied directly to the motor and the difference between T_e and T_L applied to the motor's shaft results in angular acceleration $\mathrm{d}\omega_r/\mathrm{d}t$, governed by the motor's moment of inertia J.

$$T_e - T_L = J \frac{\mathrm{d}\omega_r}{\mathrm{d}t} \tag{4.12}$$

The PI controller parameters used in the field-oriented control are listed in Table 4.1, and where determined through a trial-and-error tuning approach for simplicity.

Table 4.1: Vector Control PI Parameters

Controller	Parameter	Value
Inner controllers	Proportional gain	19.1
	Integral gain	2.1
Outer controller	Proportional gain	7.6
	Integral gain	1.8

4.3.2 Simulation Loss Study

Simulation modeling is utilised to examine the losses in both the inverter and the motor, applying (4.9) to determine the efficiency of the motor drive's speed-torque profile. This process involves adjusting the speed and torque references while calculating the system efficiency at various operational points. The resultant speed-torque efficiency profile is illustrated in Figure 4.3, where contour lines signify regions of the same efficiency. These regions are differentiated by gradual transitions, which are visually represented through a color-coded legend.

The analysis indicates that the peak system efficiency reaches 96.3% at approximately 2200 rpm and a torque of 5 Nm. However, a significant decline in efficiency is observed at lower speeds and torques, primarily due to the cumulative effects of copper losses, eddy current losses, and hysteresis losses within the motor. While these losses are principal factors in determining the efficiency distribution across the motor drive system, the effect of the switching frequency on the system's losses requires further study. This additional study could highlight the mechanisms influencing motor drive efficiency, offering avenues for enhancement across diverse operating conditions.

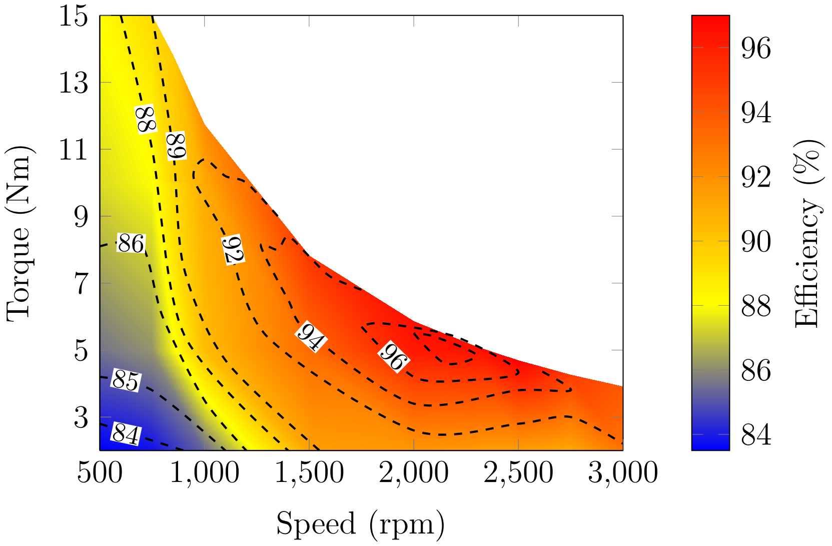


Figure 4.3: SiC-based motor drive system efficiency at $f_{sw} = 20$ kHz.

The impact of f_{sw} on $P_{m,sw}$, as indicated by (4.1), is apparent. As f_{sw} increases, there is a corresponding proportional rise in the $P_{m,sw}$. This relationship is expected, as the increased number of switching transitions results in higher losses associated with the switching process. Conversely, $P_{m,cond}$ is unaffected by changes in f_{sw}. This is due to $P_{m,cond}$ being directly proportional to the square of the current $i_d^2 R_{ds,on}$. Simulation results presented in Figure 4.4(a) support this relationship, showing minimal sensitivity

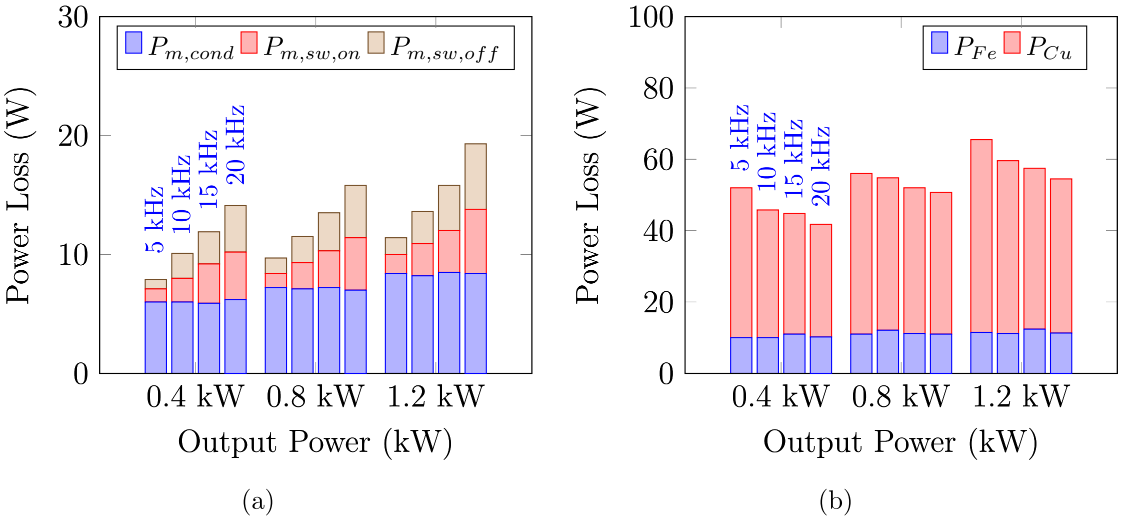


Figure 4.4: Impact of switching frequency and output power on three-phase SiC MOSFET-based inverter efficiency. (a) Inverter losses. (b) Motor losses. (Simulation Parameters: $V_{dc} = 300$ V, $f = 50$ Hz, $m_i = 0.8$, f_{sw}= 5 kHz, 10 kHz, 15 kHz and 20 kHz.)

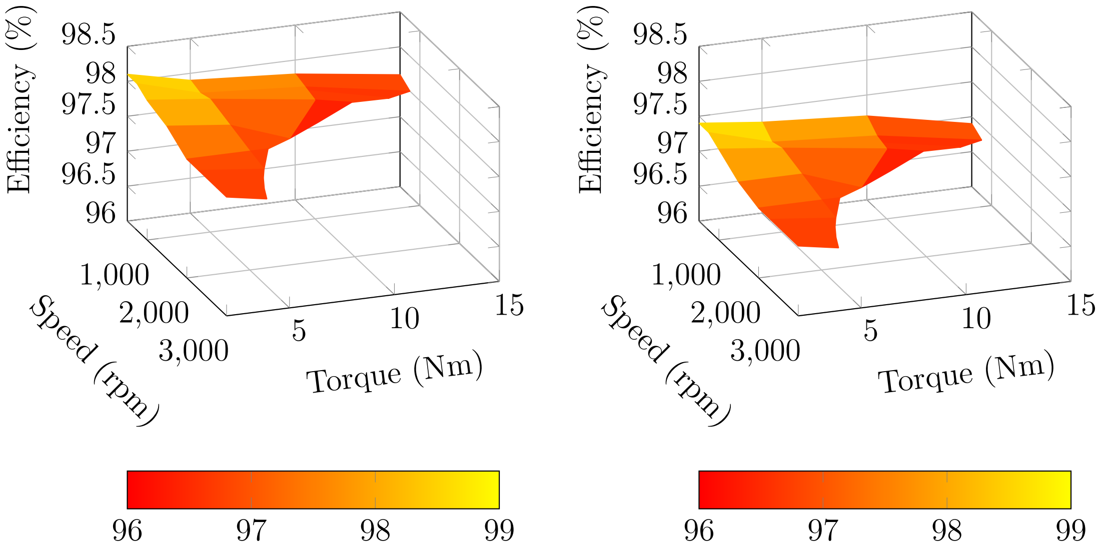
of $P_{m,cond}$ to f_{sw}, while both switching turn-on $P_{m,sw,on}$ and switching turn-off $P_{m,sw,off}$ losses increase proportionally. Table 4.2 displays the motor's operating points that correspond to the output power.

Table 4.2: Simulation Scenarios

Power (kW)	Speed (rpm)	Torque (Nm)
0.4	1900	2.0
0.8	1400	5.5
1.2	900	12.7

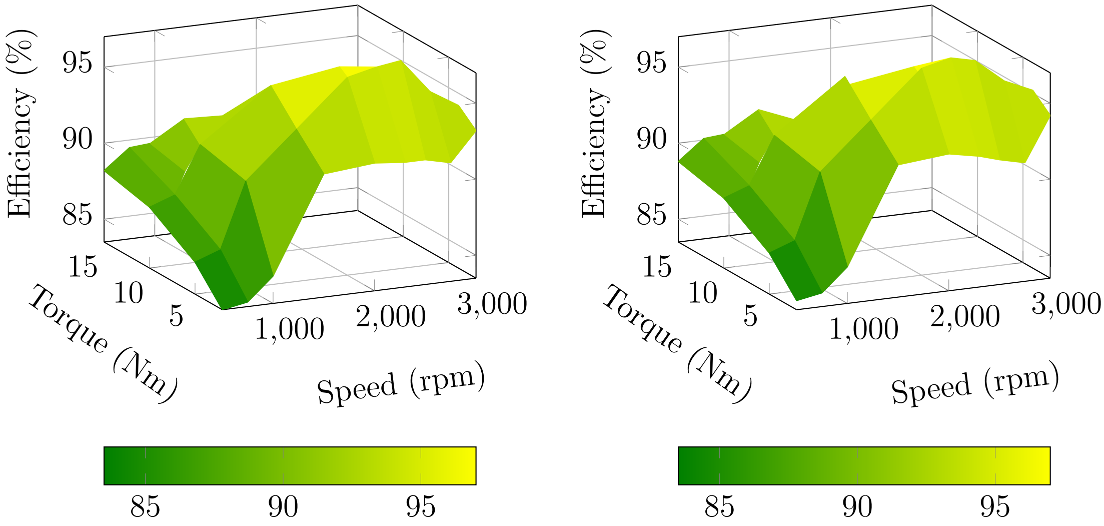
Furthermore, insights into the simulation of motor losses are provided in Figure 4.4(b). It is observed that at lower switching frequencies, P_{Cu} in the motor are notably higher, while their dependence on modulation decreases at higher frequencies. In contrast, f_{sw} has minimal influence on the overall P_{Fe} losses partly due to the utilisation of low-loss core materials that exhibit insignificant modulation effects. The magnetic field generated by the PMs in the motor predominates over the influence of the armature reaction field [160]. These findings contribute to a better understanding of the distribution of losses in the motor drive system. They highlight the importance of considering the frequency-dependent behaviour of P_{Cu} and the dominant influence of the magnetic field generated by the PMs in minimising the impact of P_{Fe}.

Figure 4.5 illustrates the impact of f_{sw} and motor operating conditions on the



(a) (b)

Figure 4.5: Impact of inverter switching frequency f_{sw} and motor loading conditions on inverter efficiency. (a) $f_{sw} = 10$ KHz. (b) $f_{sw} = 20$ kHz.



(a) (b)

Figure 4.6: Impact of inverter switching frequency f_{sw} and motor loading conditions on motor efficiency. (a) $f_{sw} = 10$ KHz. (b) $f_{sw} = 20$ kHz.

inverter efficiency. As expected, by increasing f_{sw} by 10 kHz in Figure 4.5(b), this results in a noticeable drop in inverter efficiency for all operating points. This is predominantly due to the increased switching losses. Furthermore, it is demonstrated that efficiency is comparatively higher at lower output power levels than at high power levels. This is likely due to higher current conduction losses at these lower power levels. A similar comparative analysis is conducted to evaluate motor efficiency across a range of operating conditions, as shown in Figure 4.6. As the motor achieves its rated operating conditions (i.e., $\omega_r = 3000$ rpm, $T_L = 3.9$ Nm), its efficiency progressively improves. Furthermore, motor efficiency exhibit a slight increase across all operating conditions as the switching frequency rises by 10 kHz. Building upon this observation, it becomes possible to assess the impact of increasing the switching frequency on the overall losses of the motor drive system.

Based on this simulated analysis, a discernible tradeoff between inverter and motor losses and the switching frequency becomes apparent. Such that increasing switching frequency increases inverter losses, but reduces motor losses. However, the question of determining the optimum switching frequency f_{sw}^* for operating the inverter at each motor ω_r and T_L remains. The subsequent section will discuss the criteria for selecting the f_{sw}^* for optimised efficiency.

4.4 Proposed Variable Switching Frequency PWM Strategy

Through simulations, it has been empirically determined that distinct switching frequencies are crucial for maximising the overall efficiency of the motor drive under different operating conditions. This necessity arises from the observation that inverter losses increase with higher switching frequencies, while motor losses decrease. To identify the most optimal switching frequency f_{sw}^*, simulations are systematically conducted at various operating points, as shown in Figure 4.7, cycling through a range of discrete frequencies, such as 5 kHz, 10 kHz, 15 kHz, and 20 kHz. The switching frequency associated with the least losses is then selected for each operating point and defined in an offline lookup table. For this strategy, the speed reference was kept constant, whilst increasing the load torque.

It is important to acknowledge that the significance of this phenomenon mostly diminishes beyond the 20 kHz threshold, primarily due to the reduced influence of P_{Cu} at higher switching frequencies. Consequently, when operating above 20 kHz, the losses incurred by the inverter outweigh the losses of the entire motor drive system.

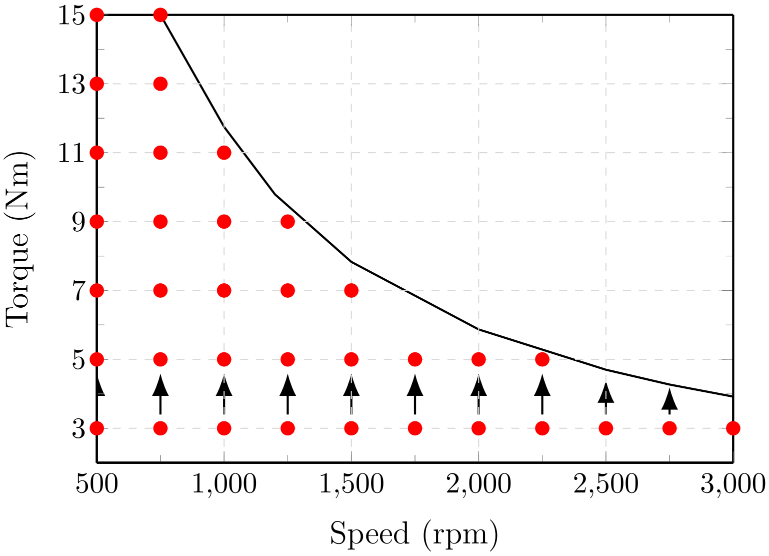


Figure 4.7: Optimisation framework for discrete operating conditions.

To ensure a smooth transition between these discrete points, a linear interpolation technique is applied. This involves connecting the switching frequencies with linear segments, establishing a continuous range of optimal switching frequencies throughout the operating range of the motor drive. This interpolated switching frequency profile allows for seamless real-time adjustments, maximising efficiency and improving the overall performance of the system.

4.4.1 Simulation Results

This approach enables the system to dynamically adapt its switching frequency at different operating points, enhancing efficiency. To support the implementation of this method, a switching frequency map is developed in Figure 4.8. This contour plot graphically represents the relationship between speed, torque, and switching frequency for the motor drive system. The contour lines connect points with the same switching frequency, which is indicated by the color-coded legend. Between contour lines, the switching frequency gradually changes; areas closer to the lower frequency contours (blue) indicate a region of lower switching frequency, while areas closer to the higher frequency contours (red) suggest a higher switching frequency. The plot illustrates that when the motor functions at lower (500 rpm) or higher speeds (3000 rpm), there is a noticeable decrease in switching frequencies. This observation provides insights into the optimal operational parameters for efficiency and performance.

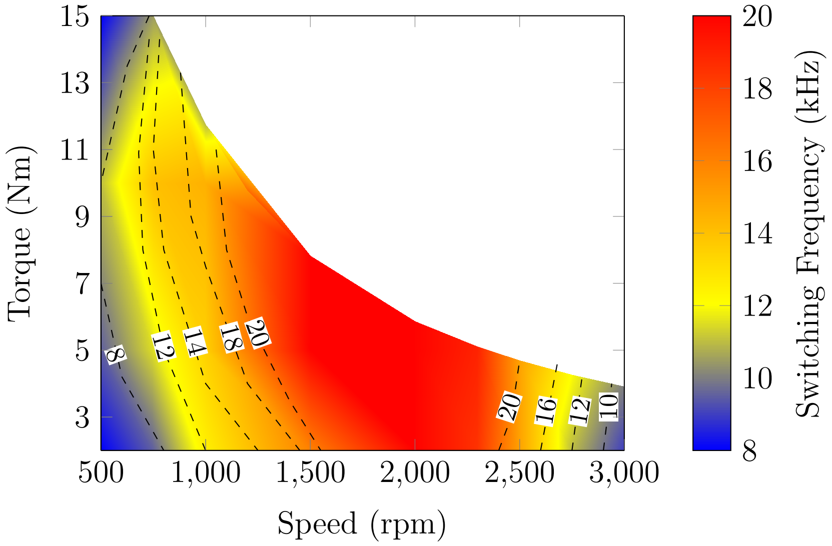


Figure 4.8: Simulated optimum switching frequency map to maximise system efficiency.

It should be noted that the switching frequency directly influences the motor's performance, and by identifying optimal frequencies for different operating points, the overall system efficiency is significantly improved. The generation of the switching frequency map involves comparing the inverter and motor power losses, as illustrated in Figures 4.5 and 4.6. Through this comparative analysis, regions exhibiting superior efficiency are identified, representing the points at which the system operates most efficiently. Corresponding switching frequencies are determined accordingly and implemented in an offline lookup table. The control diagram system implementation is depicted in Figure 4.9 and the guideline procedure is shown in Figure 4.10.

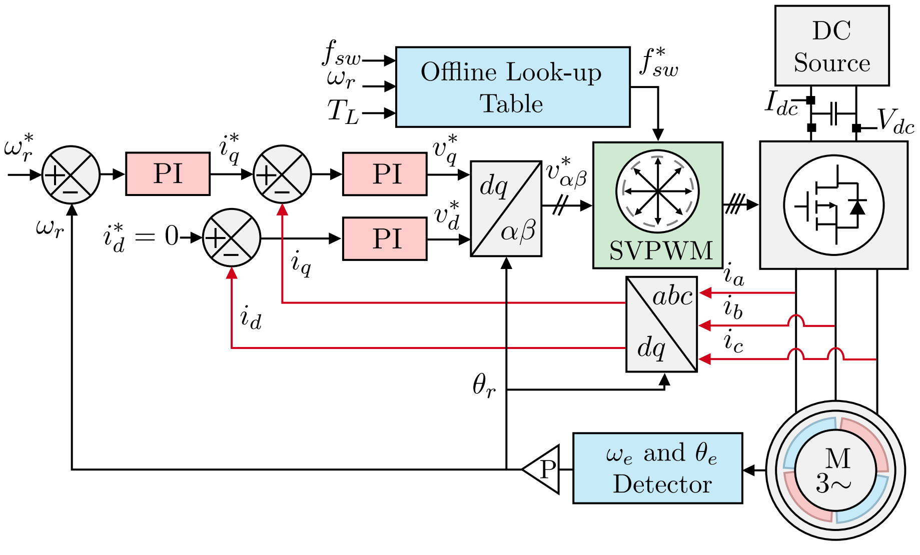


Figure 4.9: Control diagram for proposed VSF-PWM based on loss modelling.

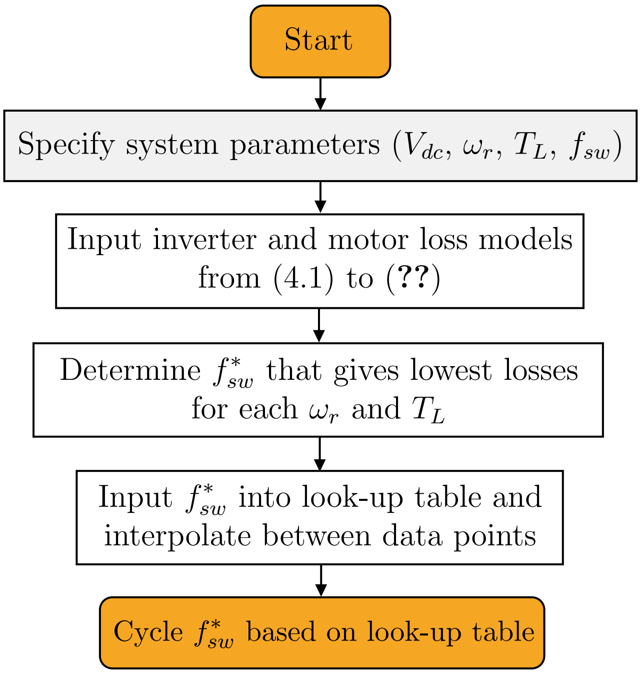


Figure 4.10: Guideline procedure for determining the optimum switching frequency map.

Table 4.3: Simulated Efficiency Improvement of Proposed VSF-PWM Compared to CSF-PWM (16 kHz)

T_L (Nm) / ω_r (rpm)	3	5	7	9	11	13	15
500	0.25%	0.20%	0.17%	0.07%	0.16%	0.18%	0.23%
1000	0.15%	0.01%	0.00%	0.09%	0.26%	-	-
1500	0.18%	0.28%	0.25%	-	-	-	-
2000	0.26%	0.36%	-	-	-	-	-
2500	0.24%	-	-	-	-	-	-
3000	0.29%	-	-	-	-	-	-

To validate the improvement in efficiency, the motor drive system was operated at a constant switching frequency of 16 kHz alongside the VSF-PWM approach. Simulated efficiency data points between the VSF-PWM and CSF-PWM methods were compared. The differences in efficiency, represented as (VSF-PWM - CSF-PWM), are outlined in Table 4.3. Notably, the simulated efficiency is superior at all operating points, with a maximum efficiency boost of 0.36%.

4.4.2 Experimental Verification

The current investigation so far has focused solely on a simulation study. However, it is crucial to expand the loss analysis by conducting experimental tests with the physical motor. This step is necessary since there may be differences between the simulated inverter and motor losses, and actual hardware being examined. To address this, an experimental validation is performed on a 1.23 kW PMSM drive, as depicted in Figure 3.2 in Chapter 3.

Optimum Switching Frequency Map

To construct the experimental optimum switching frequency map, it is necessary to measure the efficiency at every switching frequency for each operating point, following the guideline procedure depicted in Figure 4.10. In order to accomplish this, the ac precision power analyser is connected in a star configuration with neutral-to-ground. The measured efficiency $\eta_{sys,meas}$ is calculated by determining the ratio of output power to input power, represented as:

$$\eta_{sys,meas} = \frac{\int_0^{T_s} V_a I_a + \int_0^{T_s} V_b I_b + \int_0^{T_s} V_c I_c}{V_{dc} I_{dc} T_s} \times 100 \tag{4.13}$$

where T_s is the sampling period. Following an iterative process of calculating the efficiency for every operating point, the optimum switching frequency map is shown in Figure 4.11.

The measured switching frequency map demonstrates a close alignment with the simulated map, indicating a high-level of agreement between the two. However, there are minor discrepancies observed in the switching frequency values. For instance, at 1250 rpm and 5 Nm, the optimum switching frequency is reported as 20 kHz, while the measured optimum switching frequency is slightly lower at 18 kHz. Nevertheless, by systematically cycling through each switching frequency, it becomes feasible to enhance the overall efficiency of the motor drive system.

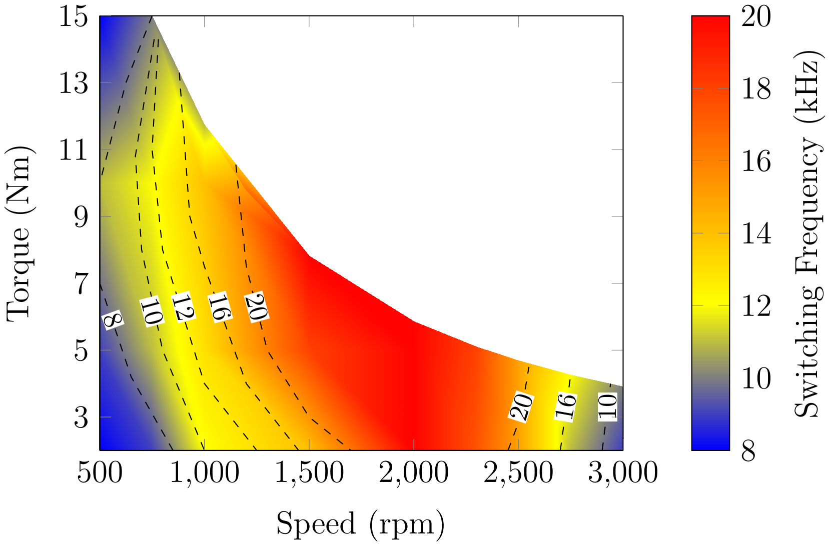


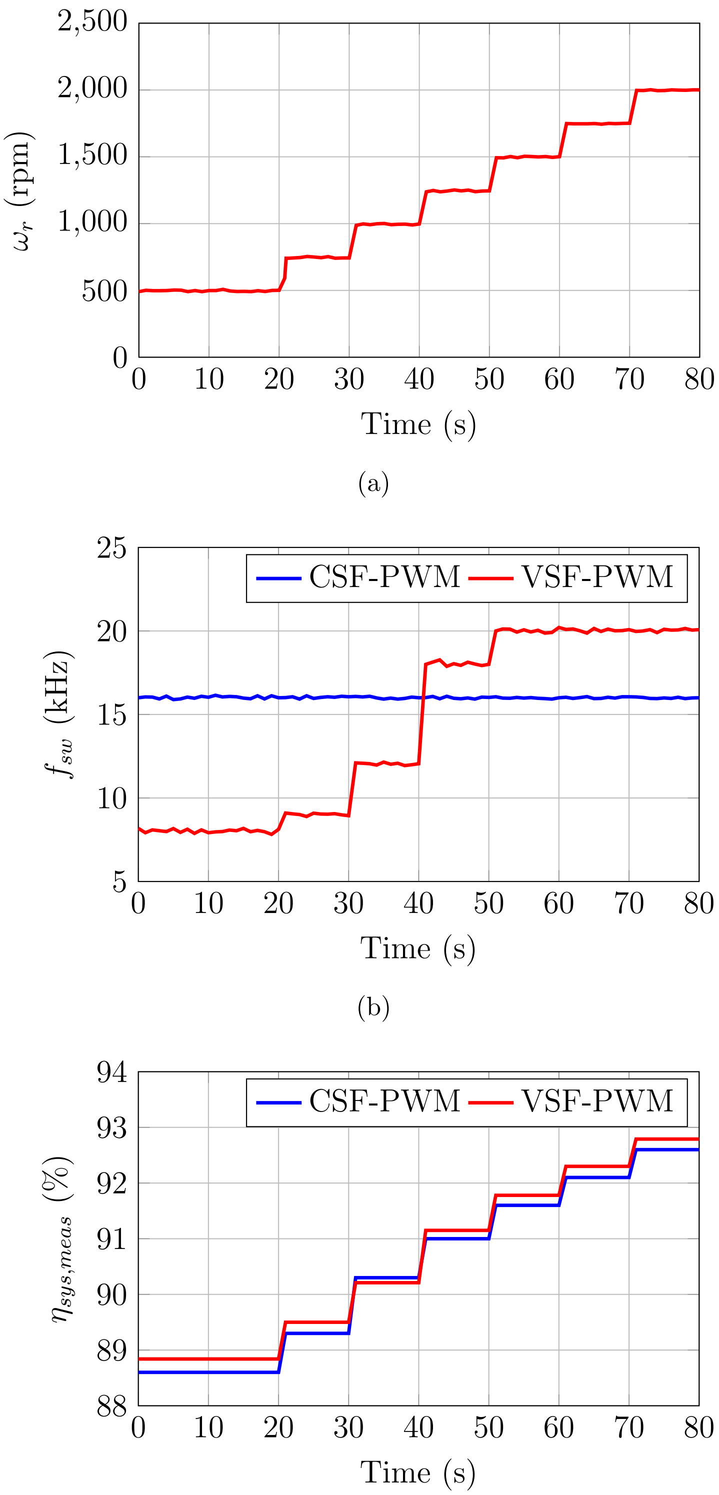
Figure 4.11: Experimental optimum switching frequency map to maximise system efficiency of SiC-based motor drive.

Efficiency Improvement Compared to CSF-PWM

To highlight the improvements in efficiency, the ω_r is adjusted in 250 rpm step changes, ranging from 500 rpm to 2000 rpm. Throughout these adjustments, a consistent T_L of 5 Nm was maintained, as illustrated in Figure 4.12. This methodology allows for a seamless transition across diverse switching frequencies with the increase of ω_r. Figure 4.12(c) presents the measured efficiencies for both the traditional CSF-PWM (16 kHz) and the proposed VSF-PWM.

The findings accentuate the advantages of utilising VSF-PWM when making step alterations to ω_r. An in-depth analysis of motor operating conditions unveiled a noteworthy efficiency surge-up to 0.29%-under specific scenarios. However, there is an observed marginal dip in efficiency below the CSF-PWM between 30 s and 40 s. This deviation is likely attributed to the slight inaccuracies inherent in the experimental measurements. Still, the predominant efficiency enhancement across the majority of operating points is rooted in the tradeoff between inverter and motor losses, further refined by the optimisation of the switching frequency.

The influence of step changes on the three-phase current is illustrated in Figure 4.13, where ω_r shifts from 1250 rpm to 1500 rpm. This adjustment prompts a change in frequency from 18 kHz to 20 kHz. Importantly, despite this change, the current ripple remains relatively unaffected, largely due to the minimal increase in frequency.



(a)

(b)

(c)

Figure 4.12: System response measurements of the motor drive using both CSF-PWM (16 kHz) and the proposed VSF-PWM method at $T_L = 5$ Nm. (a) Rotational speed. (b) Switching frequency. (c) System efficiency comparison.

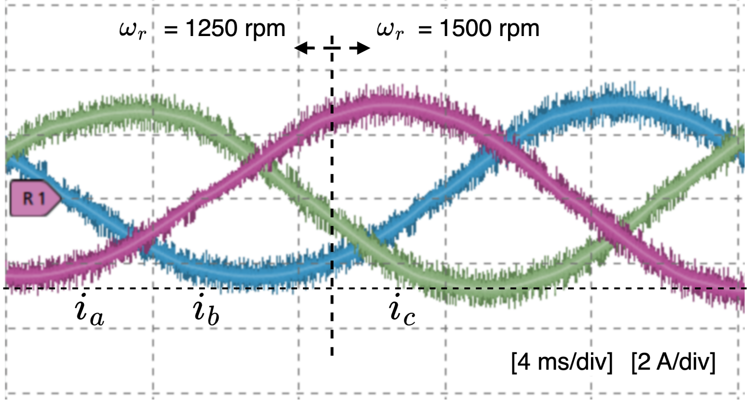


Figure 4.13: Three-phase ac currents showing ω_r step change from 1250 rpm to 1500 rpm and $f_{sw,lut}$ from 18 kHz to 20 kHz.

Table 4.4: Experimental Efficiency Improvement Compared to CSF-PWM (16 kHz)

T_L (Nm) / ω_r (rpm)	3	5	7	9	11	13	15
500	0.25%	0.24%	0.17%	0.19%	0.19%	0.22%	0.23%
1000	0.16%	-0.09%	0.00%	-0.04%	0.18%	-	-
1500	0.00%	0.18%	0.31%	-	-	-	-
2000	0.19%	0.29%	-	-	-	-	-
2500	0.22%	-	-	-	-	-	-
3000	0.23%	-	-	-	-	-	-

The crux of the study is evident: by adeptly balancing inverter and motor losses and fine-tuning the switching frequency, there is a notable potential to increase the efficiency of motor drive systems. These insights offer a clearer perspective on how different factors intertwine to influence system performance. A detailed comparison of the efficiency between the presented VSF-PWM and CSF-PWM at 16 kHz is shown in Table 4.4. The emphasis is clear: tailored optimisation strategies are vital to attaining optimal efficiency under real-world conditions.

4.5 Summary

This chapter presented an analysis of switching frequency on motor drive system losses. It was observed that as the switching frequency increases, the inverter switching losses proportionally increase, while the motor losses decrease. This tradeoff between losses is thoroughly examined through simulation modelling, aiming to determine the optimal switching frequency for the motor drive system, considering various loading conditions. Based on the obtained data, an offline efficiency map was constructed to effectively optimise the overall efficiency of the motor drive system as operating conditions change.

The effectiveness of the offline map was experimentally validated, revealing improvements in system efficiency of up to 0.29% when compared to CSF-PWM under specific operating conditions.

While this chapter focuses on VSF-PWM and the optimisation of system efficiency through loss modelling, it is important to note that the approach can be further extended to consider current ripple. This extension holds the potential for additional improvements in efficiency and the establishment of maximum current ripple limits. The details of this extension are described in the subsequent chapter.

Chapter 5

Variable Switching Frequency PWM for Current Ripple Reduction

Building on the foundation laid by the exploration of VSF-PWM in automotive applications, this chapter introduces an alternative VSF-PWM strategy. Specifically, this chapter integrates a novel approach that relies on the prediction of current ripple in conjunction with the loss modelling technique detailed in Chapter 4. The primary objectives are to minimise peak current ripple, distribute current harmonics more evenly, and consequently improve overall system efficiency. The efficacy of this method has been confirmed through simulations conducted in PLECS and MATLAB/Simulink, as well as through experimental validation.

5.1 Introduction

In Chapter 2, the concept of VSF-PWM and current ripple prediction was introduced, highlighting its significance in motor drives and various three-phase PWM converter applications [63, 70, 168]. The control of current ripple is pivotal for enhancing system performance, boosting efficiency, mitigating EMI, and reducing the current stress on components [58]. Moreover, adhering to specific industry standards necessitates keeping the current ripple below certain thresholds. These benefits are critical in surpassing the limitations of traditional CSF-PWM techniques, particularly in automotive applications where system performance and efficiency are paramount.

Despite their advantages, a notable drawback of traditional VSF-PWM methods is the rigidity of the base switching frequency, which remains fixed regardless of the load conditions. This approach results in minimal adjustments to the switching frequency, constrained to oscillations between two pre-defined values, ignoring the dynamic operating conditions of the motor drive. As emphasised in [70], there is a necessity for an adaptive VSF-PWM strategy that considers variables specific to the motor, such as rotor speed and load torque. Given the significance of dynamic performance and the potential for system loss improvements, discussed in Chapter 4, it is crucial to explore approaches that accommodate changing conditions in the motor drive. However, finding the optimal base switching frequencies for different speeds and torques, given their considerable impact on loss distribution and current ripple amplitude, is a complex task. Thus, the question remains as to how to effectively select the switching frequency based on current ripple magnitude and system losses.

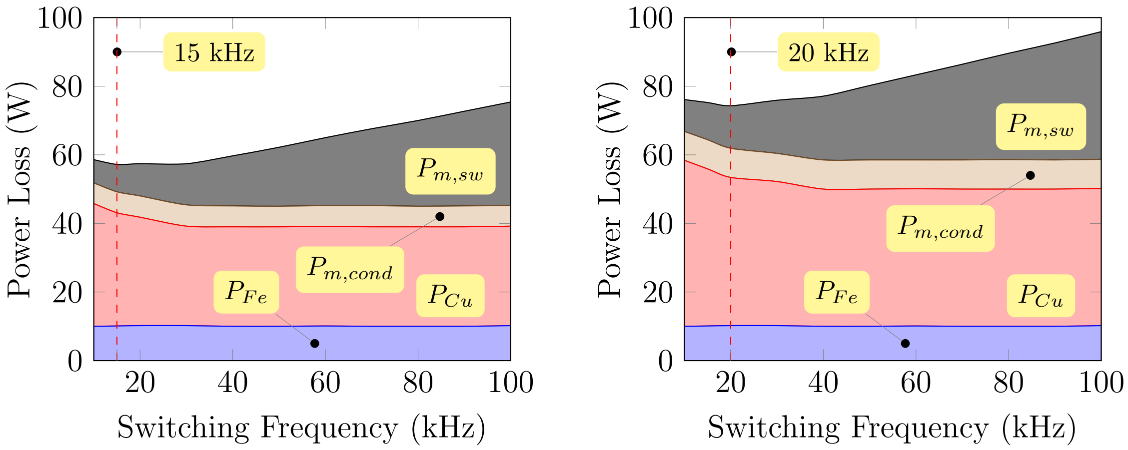
Addressing this challenge, this chapter introduces a novel VSF-PWM methodology tailored for SiC-based motor drive systems. This method diverges from existing current ripple techniques by establishing a unique and optimal base switching frequency for each rotor speed and load torque, utilising an offline lookup table detailed in Chapter 4. This strategy not only optimizes dynamic performance but also significantly enhances system efficiency by dynamically adjusting the switching frequency in response to the magnitude of the current ripple. The resultant benefits include reduced losses and a broader total harmonic distortion (THD), outperforming traditional VSF-PWM methods.

To substantiate the advantages of the proposed method, the chapter presents comparative analyses through simulated and experimental loss models, along with efficiency maps for the PMSM drive system. Efficiency curves and the harmonic spectrum of the phase current are showcased to highlight the superior performance of the proposed VSF-PWM method against the conventional CSF-PWM approach, underlining its potential for automotive applications where efficiency and reliability are critical.

5.2 Adaptive Variable Switching Frequency PWM

5.2.1 Loss Modelling

In Chapter 4, it has been experimentally verified that optimising the switching frequency considering the motor's load conditions enhances the system efficiency by approximately 0.3%. The observation indicates that increasing the switching frequency results in a reduction of motor copper losses but a simultaneous increase in inverter switching losses. The core principle explored in Chapter 4 is to find the optimal tradeoff between these losses. This tradeoff is simulated in Figure 5.1 for two distinct operating conditions to showcase the system losses at both low output power and high power. In the case of low output power, as depicted in Figure 5.1(a), the system losses are minimised when operating at 15 kHz. This outcome is primarily influenced by the balance between decreasing P_{Cu} and increasing $P_{m,sw}$. This relationship is further demonstrated in Figure 5.1(b) for high output power, where the optimum switching frequency is found to be 20 kHz. Therefore, by employing an offline lookup table design and dynamically adjusting the switching frequency based on each operating point, the system achieves a substantial enhancement in efficiency.



(a) (b)

Figure 5.1: Simulated comparison of SiC-based motor drive system losses at two operating points. (a) 0.4 kW. (b) 1.2 kW.

It is crucial to emphasise that despite utilising this modulation approach, the switching frequency remains the same unless the operating conditions change. Specifically, when there are changes in loading conditions, such as during motor acceleration, the switching frequency transitions to VSF-PWM. However, it seamlessly reverts back to CSF-PWM when the loading conditions stabilise and remain constant. Furthermore, the current ripple throughout each waveform cycle remains uneven, which poses challenges in industrial applications that have maximum current ripple requirements. Consequently, the current ripple-based VSF-PWM technique combined with the loss modelling approach remains unexplored. The subsequent section describes how to further optimise the switching frequency based on the current ripple and loss modelling.

5.2.2 Variable Switching Frequency PWM Based on Loss Modelling and Current Ripple

To optimise current ripple control using VSF-PWM, accurate prediction of current ripple prior to activating switching pulses is essential. This proactive approach is key to dynamically adjusting the switching frequency, thereby effectively reducing current ripple magnitude. The prediction method, utilising dq transformations, was specifically tailored for PMSM drives and is outlined in [70]. The methodology, as elaborated in Chapter 2, involves a thorough comparison of fundamental voltage and voltage ripple, facilitated by calculating sector duty cycles for SVPWM. By considering the motor dq inductance L_d and L_q, the current ripple is determined using the current-voltage relationship of the inductor.

In addition, the forthcoming switching period's peak current ripple $\hat{i}_{x,p,peak}$ is calculated by finding the absolute value of the phase current $|\Delta i_x|$, where subscript x denotes the phase. The collective predicted peak current ripple $\hat{i}_{p,peak}$ of all three phases is subsequently determined, allowing for customised frequency adjustments based on peak ripple magnitude. However, it is noteworthy that current ripple behavior exhibits variations across motor operating points, predominantly under high-load conditions [63]. To address this concern, a predefined current ripple value $\hat{i}_{set}$, is assigned to each operating point, calculated according to the system's maximum current specification. These thresholds are determined either via simulations or experiments. This process involves creating an offline look-up table recording each operating point's $\hat{i}_{set}$ depending on the peak current ripple. The current ripple thresholds for the simulated system are shown in Figure 5.2. It is noteworthy that $\hat{i}_{set}$ is higher at low speed and high torque conditions. This phenomenon can be attributed to Faraday's law, wherein the motor generates a lower back electromotive force at low speeds. Consequently this increases the dependence of the voltage across the motor windings on the applied voltage resulting in higher current ripple. This effect is particularly pronounced when the motor operates at high torque, where the current demand is significant [169].

Should the anticipated current ripple exceed this set limit, the switching frequency

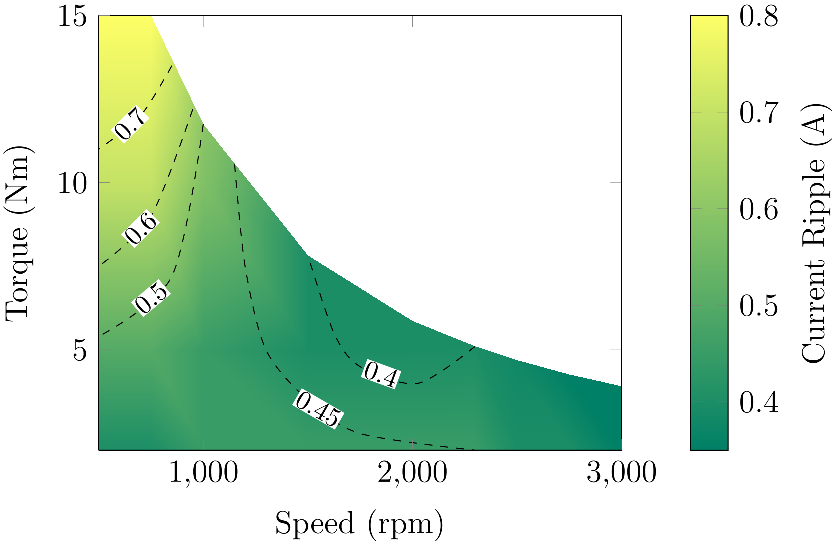


Figure 5.2: Simulated current ripple threshold $\hat{i}_{set}$ map for motor operating conditions.

is increased to keep the ripple within acceptable bounds. This is accomplished by adhering to (5.1) and updating the ripple switching frequency $f^*_{sw,r}$ accordingly. In doing so, the peak value of the three-phase current ripple will ideally be maintained below $\hat{i}_{set}$, thereby achieving VSF-PWM based on current ripple.

$$f^*_{sw,r} = f^*_{sw} \times \frac{\hat{i}_{p,peak}}{\hat{i}_{set}} \tag{5.1}$$

Contrary to other literature sources on VSF-PWM based on current ripple [70,168], this approach uniquely adjusts the fundamental switching frequency each cycle, considering the influence of ω_r and T_L on the motor drive losses. The revised switching frequencies are then adjusted according to the current ripple observed at this fundamental frequency. The entire scheme is outlined through the following steps, accompanied by the procedural guidelines and control diagram depicted in Figures 5.3 and 5.4:

1. Determine the optimum base switching frequency f^*_{sw} from the loss modelling tradeoff approach (Chapter 4) to achieve optimised efficiency for each operating point.

2. Predict the peak current ripple $\hat{i}_{p,peak}$ by analysing the dq components of the fundamental and ripple voltage.

3. Predetermine $\hat{i}_{set}$ for each operating point.

4. Using (5.1), compare $\hat{i}_{p,peak}$ with $\hat{i}_{set}$ and vary switching frequency accordingly.

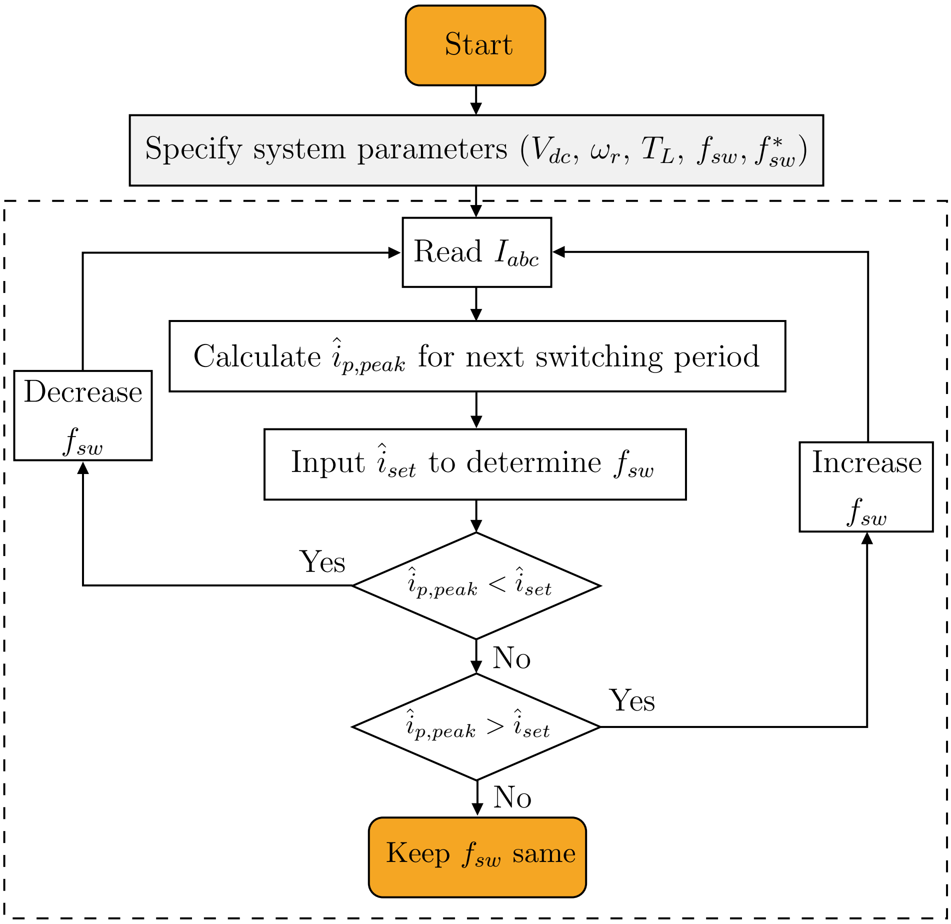


Figure 5.3: Guideline procedure for determining the optimum switching frequency map.

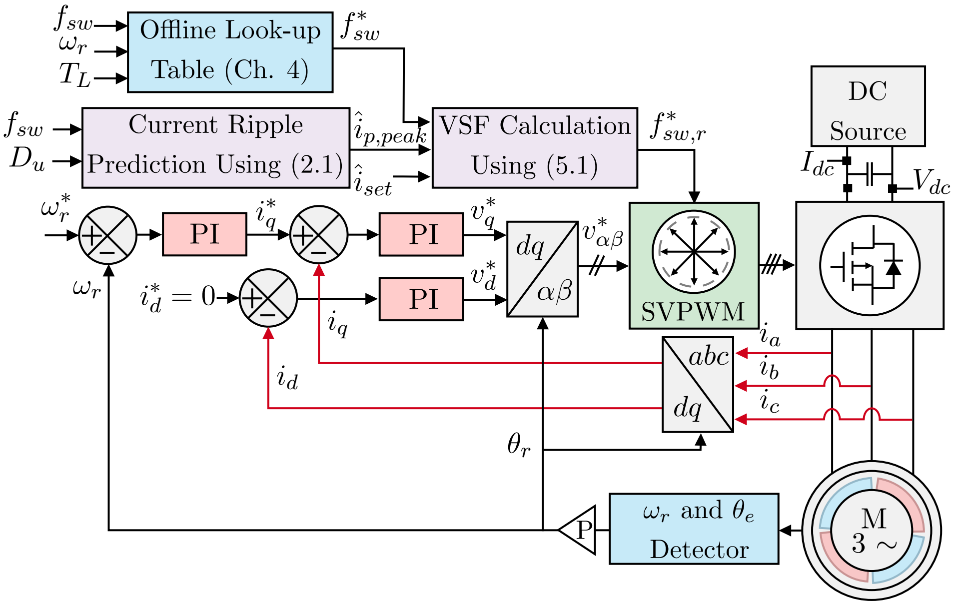


Figure 5.4: Control diagram for proposed VSF-PWM based on current ripple.

5.3 Modulation Verification

To validate the proposed VSF-PWM methodology, which uses the prediction of current ripple, the system parameters detailed in Chapter 3, and employed in Chapter 4 were retained. This entails the consistent utilisation of inverter and motor parameters for both simulation and experimental validation. This methodological consistency enables a comparative assessment of the efficiency improvements attained between the two modulation approaches, as expounded upon in Chapter 5.3.1.

Furthermore, the analysis of the loss model for determining f_{sw}^* remains consistent and is applied in the same manner as previously described. This ensures continuity in the evaluation of the system's performance and facilitates the examination of the benefits derived from the proposed VSF-PWM technique based on current ripple and loss modelling. The main simulation and experimental operating parameters are listed in Table 5.1, with further system parameters detailed in Table 3.2.

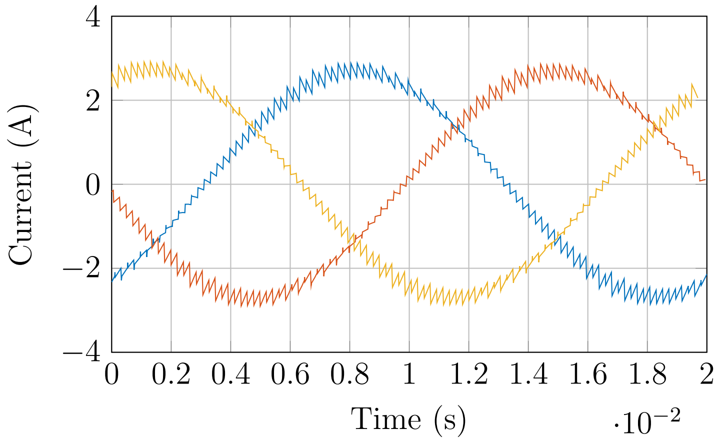
Table 5.1: System Operating Parameters

Parameter	Value
DC voltage V_{dc}	300 V
Rotor speed ω_r	2000 rpm
Load torque T_L	5 Nm
Fundamental frequency f	50 Hz
Modulation index m_i	0.8

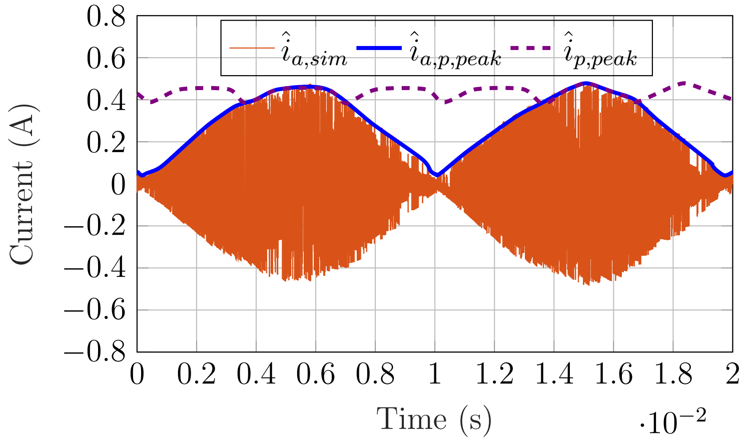
5.3.1 Simulation Results

To ensure the validation of the current ripple prediction, the SiC-based motor drive system was subjected to modelling through MATLAB/Simulink and PLECS (Plexim). Field-oriented control was used to control the rotational speed, as depicted in Figure 5.4, with the proposed modelling approach introducing a variation in the sampling time, thereby affecting the dwell times within the SVPWM modulation and consequently the switching frequency. The objective of this comparison is to validate the predictive accuracy of the current ripple, ensuring that the theoretical predictions are in concordance with the simulated results.

The determination of the f_{sw}^* begins with the application of the loss modelling approach described in Chapter 4, which takes into account the loading conditions. This initially provides the optimum switching frequency based on system losses and motor operating condition. However, as shown in Figure 5.5(a), the current displays variations in ripple within each wavelength. Subsequently following Section 2.2.2, a *dq* analysis of the ac voltage is conducted to predict the current ripple in each phase. Figure 5.5(b), shows the simulated current ripple for phase a $\hat{i}_{a,sim}$. By calculating the value of $\hat{i}_{a,p,peak}$, the significant variations in ripple are emphasised. The same *dq* methodology is carried out for all three-phases, with the peak current ripples shown as $\hat{i}_{p,peak}$.



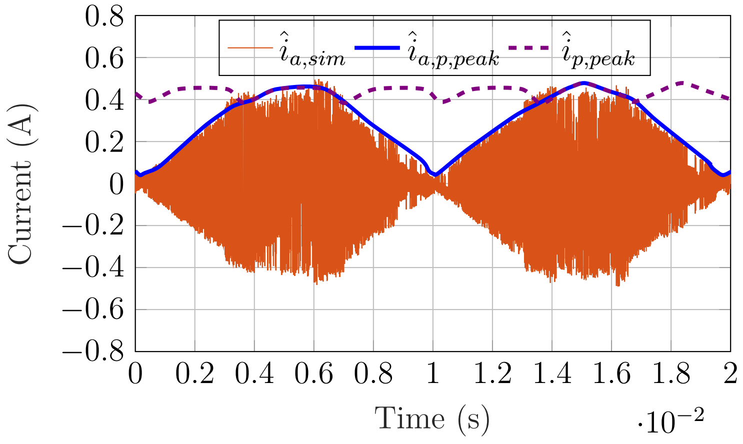
(a)



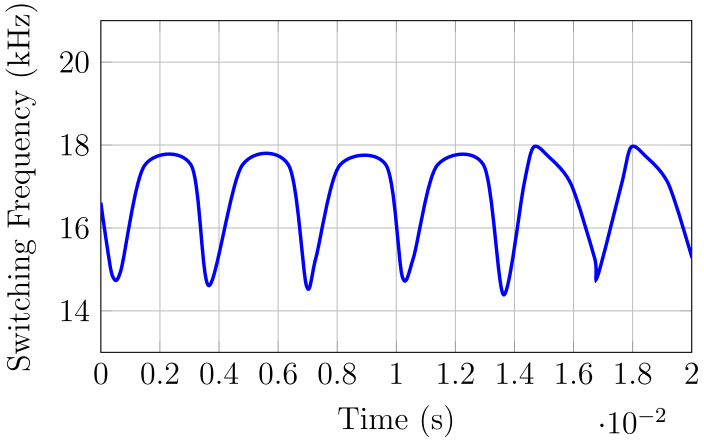
(b)

Figure 5.5: Simulated CSF-PWM current waveforms for motor drive system. (a) Three-phase current waveforms. (b) Phase a current ripple $\hat{i}_{a,sim}$ and predicted peak current ripple $\hat{i}_{a,p,peak}$. (Constant switching frequency f_{sw} = 16 kHz.)

The variability observed in the current ripple presents an opportunity to establish maximum limits for its magnitude. For the simulated operating point of $T_L = 5$ Nm and $\omega_r = 2000$ rpm, the target current value of $\hat{i}_{set}$ is set at 0.4 A, based on Figure 5.2. As $\hat{i}_{p,peak}$ exceeds this current magnitude, the switching frequency increases correspondingly. This is observed in Figure 5.6 where the current ripple is limited to ∼0.4 A by varying the switching frequency between 14.5 kHz and 17.5 kHz. When $\hat{i}_{p,peak} > \hat{i}_{set}$, the switching frequency $f^*_{sw,r}$ is correspondingly increased. Conversely, as $\hat{i}_{p,peak} < \hat{i}_{set}$, $f^*_{sw,r}$ would be slightly reduced. This differs from the CSF-PWM approach where the max current ripple observed is ∼0.5 A at 16 kHz.



(a)



(b)

Figure 5.6: Proposed VSF-PWM methadology. (a) Simulated current ripple $\hat{i}_{a,sim}$ and predicted peak current ripple $\hat{i}_{p,peak}$ of phase a. (b) Variations in switching frequency.

Efficiency Comparison

In addition to mitigating current ripple, the effect on efficiency when altering the switching frequency holds significant importance. For this reason, simulations of the motor drive's power losses were conducted using PLECS and MATLAB/Simulink. Furthermore, the reference rotor speed, ω_r^*, was incrementally increased from 1500 rpm to 3000 rpm, while maintaining the motor load torque, T_L, constant at 3 Nm. The efficiency of the proposed model was evaluated through comparison with SVPWM operating at a constant frequency of 16 kHz, the VSF-PWM method described in Chapter 4, and a VSF-PWM model referenced in [70], as illustrated in Figure 5.7. The proposed approach improved efficiency at all operational points in comparison to the other modulation techniques. In particular, when compared to CSF-PWM, the efficiency showed an improvement of 0.34%.

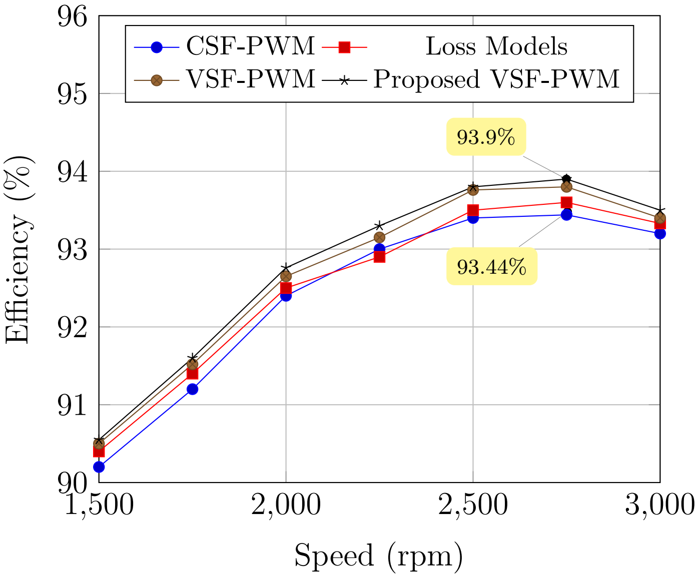


Figure 5.7: Simulated system efficiency at $T_L = 3$ Nm comparing the different modulation techniques: CSF-PWM (16 kHz), VSF-PWM [70], loss model VSF-PWM (Chapter 4), proposed VSF-PWM.

Total Harmonic Distortion

While these advantages are significant, it is essential to examine the THD behavior in the current spectrum, as shown in Figure 5.8. The VSF-PWM method demonstrates a broader spectrum than the CSF-PWM, especially noticeable between 10 kHz and 18 kHz frequencies. This effect stems from the loss modeling strategy detailed in Chapter 4, leading to reduced peak current THD magnitudes at intervals of 8 kHz. The simulated current magnitudes for CSF-PWM and VSF-PWM are 0.12% and 0.15%,

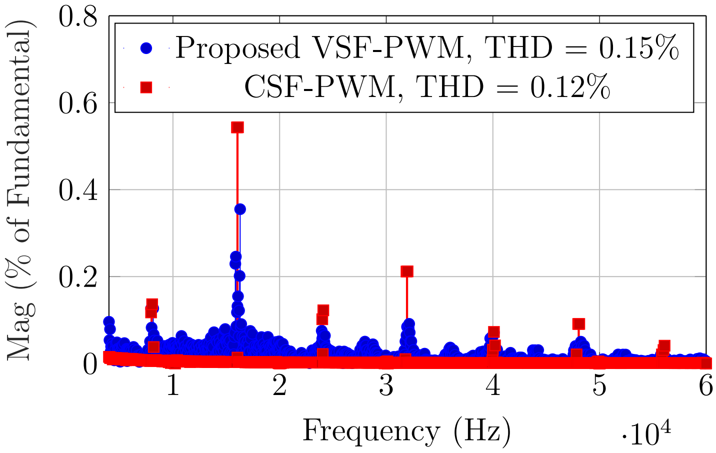


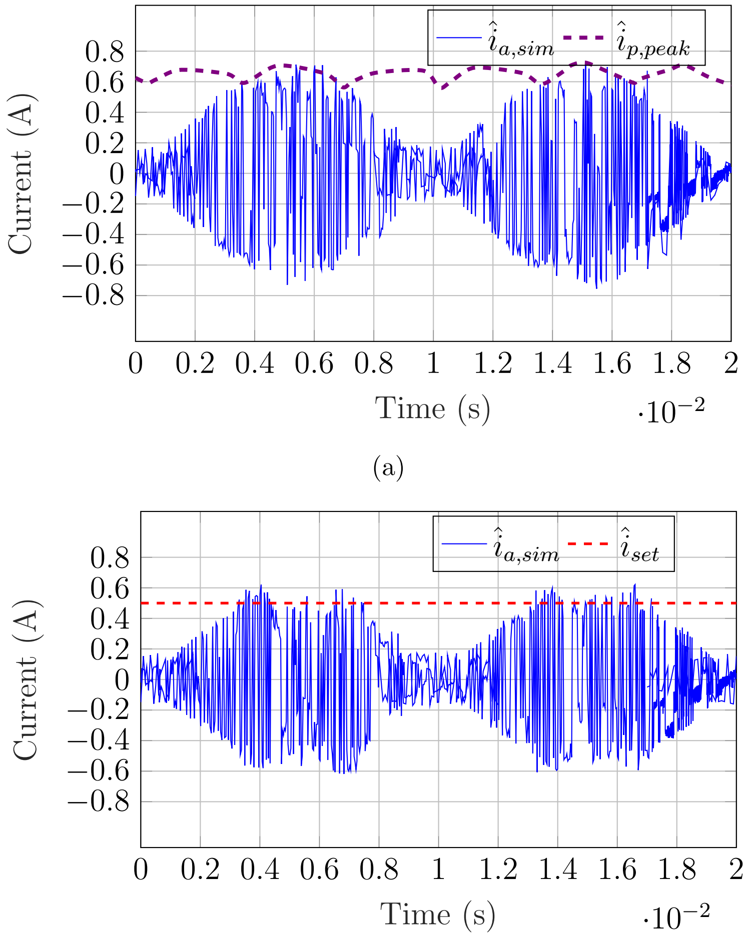
Figure 5.8: Simulated THD current spectrum comparing proposed VSF-PWM scheme with CSF-PWM.

respectively. However, the increased THD spans a wider frequency range, resulting in a more evenly distributed signal quality degradation rather than being concentrated at specific frequencies. Without careful consideration, this broader THD impact could potentially interfere with other systems operating within this frequency range, thereby elevating EMI concerns. Furthermore, this dispersion of harmonics across multiple frequencies may pose greater challenges in filtering efforts, as the harmonics are not localised to a single frequency.

5.3.2 Experimental Verification

It is often expected that experimental current ripple is larger than simulated current ripple due to factors including non-ideal components, environmental influences and parasitic elements such as trace resistance and capacitance, which may not be accurately captured in simulations. For this reason, the implementation of the theoretical and simulated study for experimental validation is crucial. The test bench is modelled in the laboratory as depicted in Figures 3.2 and 3.1.

The experimental CSF-PWM current ripple for one phase at T_L = 5 Nm and ω_r = 2000 rpm is shown in Figure 5.9(a). Due to parasitic capacitance in the MOSFET switches and motor, the peak current ripple exceeds the predicted value, but still fits well. As expected, the current ripple has variations in the magnitudes over one cycle with the peak current ripple reaching 0.7 A. This differs slightly to the simulated results, as the simulated current ripple is slightly lower at 0.5 A. For this reason, the values for $\hat{i}_{set}$ needs to be redefined for every operating point based on system requirements of maximum current ripple.

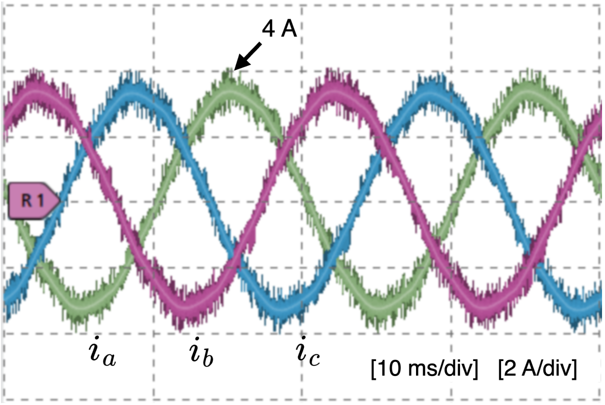


(a)

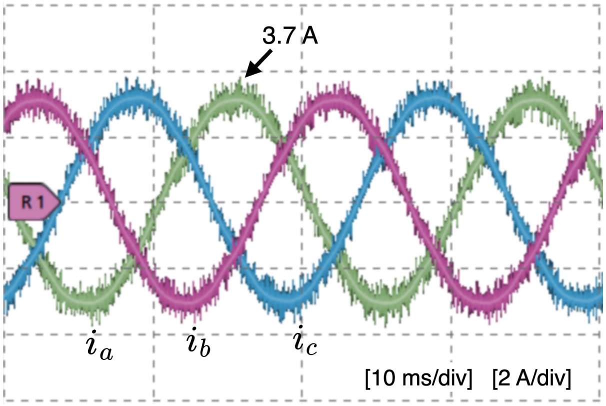
(b)

Figure 5.9: Experimental current ripple $\hat{i}_{a,sim}$ and maximum set current ripple $\hat{i}_{set}$ of phase a.

As shown in Figure 5.9(b), the predetermined value for $\hat{i}_{set}$ is defined as 0.5 A based on the operating conditions, which is intended to limit the current ripple to this value under normal operating conditions. However, it is noted that in some exceptional instances, transient conditions may cause the current to briefly exceed the $\hat{i}_{set}$ limit before stabilising back to the defined threshold. This is due to the switching frequency decreasing as the current ripple magnitude drops from either phases b or c. Although, the general trend of the current ripple is below $\hat{i}_{set}$. The full ac current waveforms for CSF-PWM and the presented VSF-PWM are shown in Figure 5.10. It is notable that the current ripple in the presented VSF-PWM has decreased as the current peaks of each phase decrease from 4 A to 3.7 A. This is noticed in all three-phases as the switching frequency varies in accordance to the current ripple magnitudes.



(a)



(b)

Figure 5.10: Three-phase ac currents. (a) showing uneven voltage ripple for CSF-PWM at 17 kHz. (b) VSF-PWM at 16 kHz and 20 kHz.

Efficiency Comparison

In addition to restricting the magnitude of current ripple, this methodology offers an inherent advantage in terms of efficiency improvement. To measure the efficiency in the motor drive system, an ac power analyser was used connecting each phase. The measured efficiency data is extracted at many operating points up to the operating limits of the motor. This is achieved by keeping the T_L constant whilst increasing ω_r. An efficiency comparison between the proposed VSF-PWM, VSF-PWM (from [70]), loss modelling VSF-PWM (Chapter 4) and CSF-PWM (16 kHz) is shown for different T_L values in Figure 5.11.

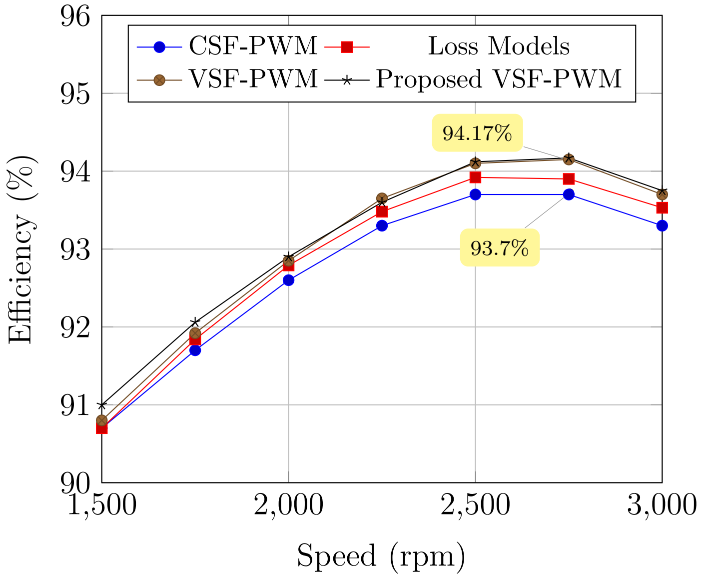


Figure 5.11: Measured system efficiency at 3 Nm comparing the different modulation techniques: CSF-PWM (16 kHz), VSF-PWM [70], loss model VSF-PWM (Chapter 4), proposed VSF-PWM.

Table 5.2: Measured Efficiency Improvement of Proposed VSF-PWM Compared to CSF-PWM (16 kHz)

T_L (Nm) / ω_r (rpm)	3	5	7	9	11	13	15
500	0.18%	0.21%	0.19%	0.16%	0.25%	0.31%	0.27%
1000	0.21%	0.11%	0.07%	0.09%	0.21%	-	-
1500	0.15%	0.24%	0.35%	-	-	-	-
2000	0.30%	0.35%	-	-	-	-	-
2500	0.42%	-	-	-	-	-	-
3000	0.45%	-	-	-	-	-	-

The measured efficiency is improved for the whole system by up to 0.45% when compared to CSF-PWM by varying the switching frequency based on current ripple and loss modelling. This also improves the motor's dynamic performance; that is, the efficiency increases as the motor accelerates, up to the operating limits. Table 5.2 details the full efficiency improvement. Contrary to other VSF-PWM based on current ripple this approach improves the efficiency more consistently over the range of operating conditions of the motor. Moreover, there is an improvement in efficiency for all operating points when compared the loss modelling approach in Chapter 4.

Since CSF-PWM uses a 16 kHz base switching frequency, the improvements in efficiency will be minimal since the drive system being modelled is generally more efficient at this frequency. Therefore, comparing against 10 kHz or lower would yield a much greater efficiency improvement.

Fast Fourier Transform

A fast Fourier transform (FFT) analysis of the experimental phase current is shown in Figure 5.12. It is noticed that by using CSF-PWM the current harmonics have large spikes at integer multiples of the carrier frequency. An example of this is seen at 16 kHz, where the peak current reaches 0.95 A and at 32 kHz reaches 0.4 A. Using the presented VSF-PWM approach, the current harmonics are more spread out over a range of frequencies. In addition, the peak current values are reduced, when compared to CSF-PWM. This is synonymous with the simulated results as the peak values of VSF-PWM is more spread out than CSF-PWM.

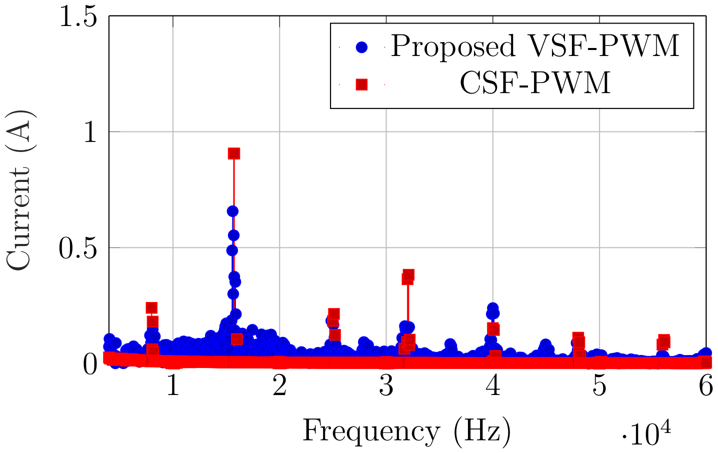


Figure 5.12: Measured harmonic current spectrum comparing proposed VSF-PWM scheme with CSF-PWM.

5.4 Summary

In this chapter an adaptive VSF-PWM control scheme was presented to set limits to the maximum current ripple and improve the efficiency of the whole motor drive system. The modulation technique varies the switching frequency based on the current ripple magnitude. Contrary to other VSF-PWM literature the presented approach considers the dynamic performance of the motor, i.e., where the ω_r and T_L is always changing. This is accomplished by applying the loss modelling technique described in Chapter 4 to establish an optimum switching frequency, which is then fine-tuned according to the magnitude of the current ripple.

To validate the theoretical approach, the control model was first simulated in PLECS (Plexim) and MATLAB/Simulink and then experimentally verified using a practical motor drive system. The results show the system efficiency improves up to 0.45% when compared to a CSF-PWM approach at 16 kHz. Moreover, the maximum current ripple can be limited based on system requirements. In addition, the current harmonics are more spread out instead of centred at a constant frequency. The superior performance of the adaptive VSF-PWM scheme results from combining the advantages from conventional VSF-PWM and loss model techniques.

Chapter 6

Mitigating Motor Overvoltage Using Zero-Voltage Switching

Building on the foundation of high-performance SiC-based motor drives, this chapter shifts focus to inverter design, tailored for applications that necessitate long ac feeder cables leading to the motor. Distinctly, this targets marine applications, as well as mining and oil exploration operations. In this context, the chapter introduces a novel approach to selecting inductor and capacitor parameters for a ZVS inverter. This strategy is aimed at mitigating motor overvoltage issues in systems fed by cables. The method achieves this mitigation by actively shaping the $\mathrm{d}v/\mathrm{d}t$ across all types of commutations within the ZVS inverter, including both resonant and natural commutations. Additionally, it outlines how the turn-off switching losses in the ZVS inverter are minimized by extending the rise time of the PWM voltage pulse.

The efficacy of these strategies is underscored by experimental results, showing a reduction in motor overvoltage from 2 p.u. to 1.06 p.u. Moreover, simulations reveal that the inverter not only improves efficiency by 1% but also achieves a 30% reduction in volume when compared to conventional hard-switching two-level and three-level solutions. These advancements, coupled with the reduced switching losses, position the ZVS inverter and its parameter design as a highly competitive option for cable-fed motor drive systems. The methodology for designing and modulating the ZVS inverter to attain a reduction in motor overvoltage is meticulously discussed within this chapter. Experimental findings further corroborate the effectiveness and adaptability of the proposed approach under varying motor load conditions, showcasing its practical applicability.

6.1 Introduction

In Chapters 4 and 5, the discussion centers on the advantages of employing a variable switching frequency in SiC MOSFETs specifically for automotive applications. However, the fast switching transitions associated with SiC MOSFETs can introduce technical challenges, such as motor overvoltage when long ac feeder cables are used between the inverter and motor [170, 171]. This type of configuration is often found in marine applications, or in harsh and inaccessible environments to enhance serviceability [172]. Effectively mitigating motor overvoltage under these conditions, while maintaining high efficiency and minimising volume and cost, remains an active area of research.

The conventional approach to mitigate overvoltage is to use LCR filters at the inverter terminal to limit the $\mathrm{d}v/\mathrm{d}t$ of PWM pulses or RC filters at the motor terminals to match the impedance of the cable and motor [105, 109, 127, 173]. Other mainstream approaches include utilising three-level converters, as presented in [40, 118], or employing active gate drivers [174]. However, as explained in Chapter 2, these methods have drawbacks such as the requirement for bulky LCR passive components, additional active switches, and increased capital costs [48]. In light of these limitations, this chapter introduces a novel approach for addressing motor overvoltage using a ZVS inverter.

Most ZVS topologies described in the literature necessitate several additional active switches for three-phase systems, which may not be suitable for cable-fed systems due to volume and cost constraints in harsh conditions. Therefore, this chapter adopts the ZVS topology presented in [24], depicted in Figure 6.1, as it requires only one additional active switch on the dc positive terminal. This results in a compact inverter design compared to conventional motor overvoltage mitigation solutions. Moreover, by employing a modified SVPWM sequence, the switching losses, EMI, and power density is improved without significantly compromising the general structure of the two-level topology [175, 176].

As discussed in [175,177], the presented ZVS inverter exhibits three types of commutations: resonant rise, resonant fall, and natural commutations. However, the rise and fall times during resonant and natural commutations are not the same [178]. Therefore, characterising $\mathrm{d}v/\mathrm{d}t$ solely for resonant commutations may lead to discrepancies in the observed value during natural commutations. Consequently, it is crucial to consider additional timing considerations to consistently prevent motor overvoltage at each switching transition. Failure to adequately address this issue may still result in repetitive PDs during resonant or natural commutations, potentially leading to motor

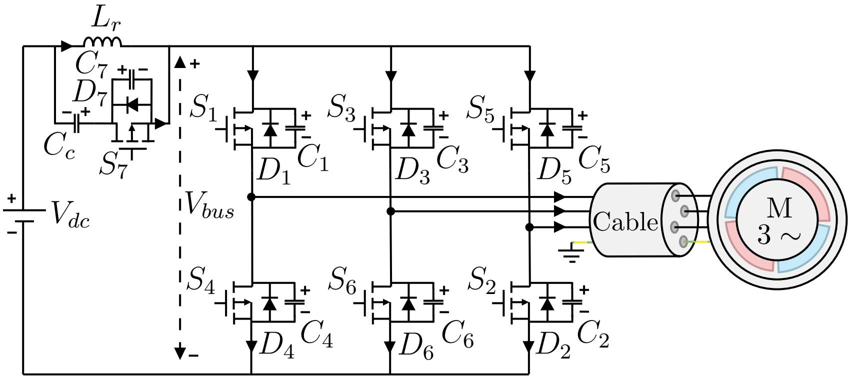


Figure 6.1: ZVS three-phase cable-fed drive system.

insulation failure [179]. Further research is thus necessary to explore the implementation and design parameters of the ZVS inverter for motor drives and overvoltage mitigation, specifically in the context of cable-fed systems.

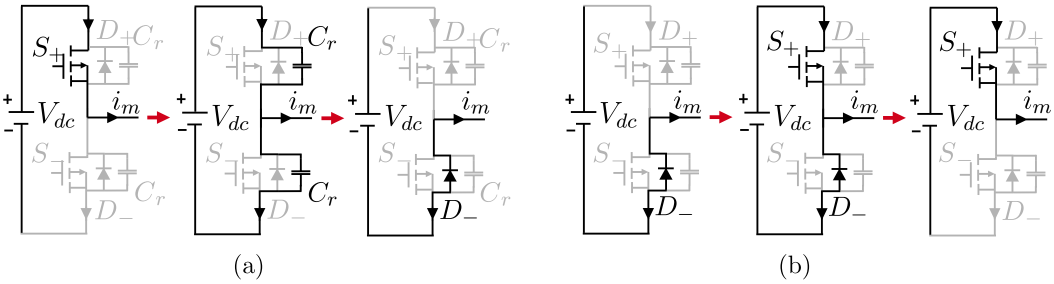
Through the proposed inductor and capacitor parameter selection, the $\mathrm{d}v/\mathrm{d}t$ of the ZVS inverter commutations has been actively profiled to avoid exciting cable antiresonance, thereby mitigating motor overvoltage. Typically, extending the PWM voltage rise time in hard-switching inverters increases the switching losses. However, as explained in this chapter, the ZVS turn-off losses have been significantly reduced. Given that ZVS switching already incurs negligible turn-on switching losses, the proposed approach enhances the efficiency of the entire motor drive system. Along with reduced volume, the ZVS inverter originally presented in [24] offers a promising alternative for mitigating motor overvoltage in cable-fed drives, where capital cost and volume are critical considerations.

This chapter provides an overview of the ZVS inverter under study. The inherent advantages of ZVS, notably its capacity for significantly reducing switching losses, are also presented. Additionally, a refined parameter selection is introduced, specifically optimised for mitigating overvoltage in cable-fed motor drive systems. Fundamental analysis is conducted to demonstrate the reduced volume of the ZVS inverter compared to conventional hard-switching inverter solutions. High-frequency software simulations in PLECS (Plexim) and MATLAB/Simulink are performed to verify the improved motor overvoltage mitigation and reduced switching turn-off losses. Experimental validation is also conducted to verify motor overvoltage mitigation under varying load conditions.

6.2 Three-Phase Zero-Voltage Switching Inverter

The first step in comprehending the resonant parameter design presented is to examine the three-phase ZVS inverter from [24]. This section offers a succinct overview and analysis of the control mechanism employed in the ZVS inverter. The diagram depicted in Figure 6.1 illustrates the arrangement of the ZVS inverter and a cable-fed ac PMSM, with an auxiliary circuit connected in series with the dc positive terminal of the inverter.

6.2.1 Topology and Principle of Operation



(a)
(b)

Figure 6.2: Switching current commutation for ZVS legs at positive phase current: (a) Case I, (b) Case II.

There are two different scenarios for current commutation possible in the ZVS legs: Case I and Case II. An example of Case I for positive phase current i_m is illustrated in 6.2(a). Here, the process of turning off the switch S_+ results in i_m transitioning from S_+ to the lower anti-parallel diode D_-. This transition is aided by the resonant capacitor C_r that provides ZVS and helps in regulating $\mathrm{d}v/\mathrm{d}t$ by varying its value. In contrast, 6.1(b) depicts Case II commutations, whereby i_m transitions from D_- to S_+, turning-on S_+. In Case II commutations C_r is bypassed before S_+ is activated, which results in hard-switching and an increase in switching losses. It is also important to note that commutations are dependant on the current polarity. For example, at positive output current Case II commutations occur when S_+ is switched-on. Conversely, at negative output current Case II commutations occur when S_+ is switched off.

In order to facilitate ZVS during the switching transitions that occur in Case II, and to avoid the occurrence of hard-switching, it is necessary to incorporate an auxiliary switch denoted as S_7, as well as a clamping capacitor C_c. S_7 conducts most of the time, storing energy in C_c. As later discussed later in Section 6.2.2, prior to Case II transitions, it is essential to ensure that the bus voltage V_{bus} resonates to zero. This is achieved by deactivating the auxiliary switch, S_7. Hence, in a conventional SVPWM

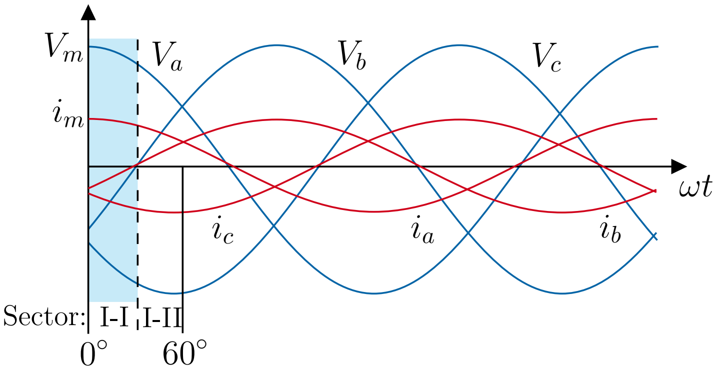


Figure 6.3: Space vector sector definition based on current polarity.

modulation scheme this would require S_7 switching three times per PWM switching cycle, resulting in large switching losses.

As mentioned in [180], the switching frequency of S_7 is reduced by modifying the SVPWM switching states based on the current polarity. This will result in lower switching losses and control complexity. This approach ensures that S_7 operates at the same switching frequency as the main switches and only requires one transition per PWM cycle. For the example shown in Figure 6.3, Sector I is subdivided into two sectors; where there are four switching states: 000, 111, 100, 110. In this switching state the first number refers to switch S_1, the second number is switch S_3 and the third number is switch S_5. The number '0' denotes a switch in off-state and '1' references the switch in on-state.

Sector I-I is defined when the polarity of i_b is negative and Sector I-II is defined when the polarity of i_b is positive. Each subsector has its own vector sequence of switching states, i.e., in Sector I-I the following arranged sequence is 111-100-110-111. In this case, the zero vector is always 111 and switch S_1 is always in conduction. Moreover, the switches S_3 and S_5 switch simultaneously when transitioning between the zero states and the first vector. Therefore, S_7 only needs to act once in this switching cycle to suppress the reverse recovery currents of the anti-parallel diodes of S_3 and S_5 and achieve ZVS. The full vector switching sequence is defined in Appendix A.

6.2.2 Control of Zero-Voltage Switching Inverter

It was mentioned earlier that this chapter focuses on the parameter selection of the ZVS inverter. However, it is imperative to firstly understand how the inverter achieves ZVS control. The steady-state operation of the ZVS inverter is summarised in Figure 6.4 and is divided into six distinct stages of operation for Sector I-I [175]. In the figure the switching patterns focus on achieving ZVS in the Case II transitions utilising S_7. The ZVS of the main switches are attained at t_1-t_2 and the ZVS of the auxiliary switch is attained at t_5-t_6. Case I transitions are shown at t_7 and t_8 where ZVS is achieved through the parallel capacitors.

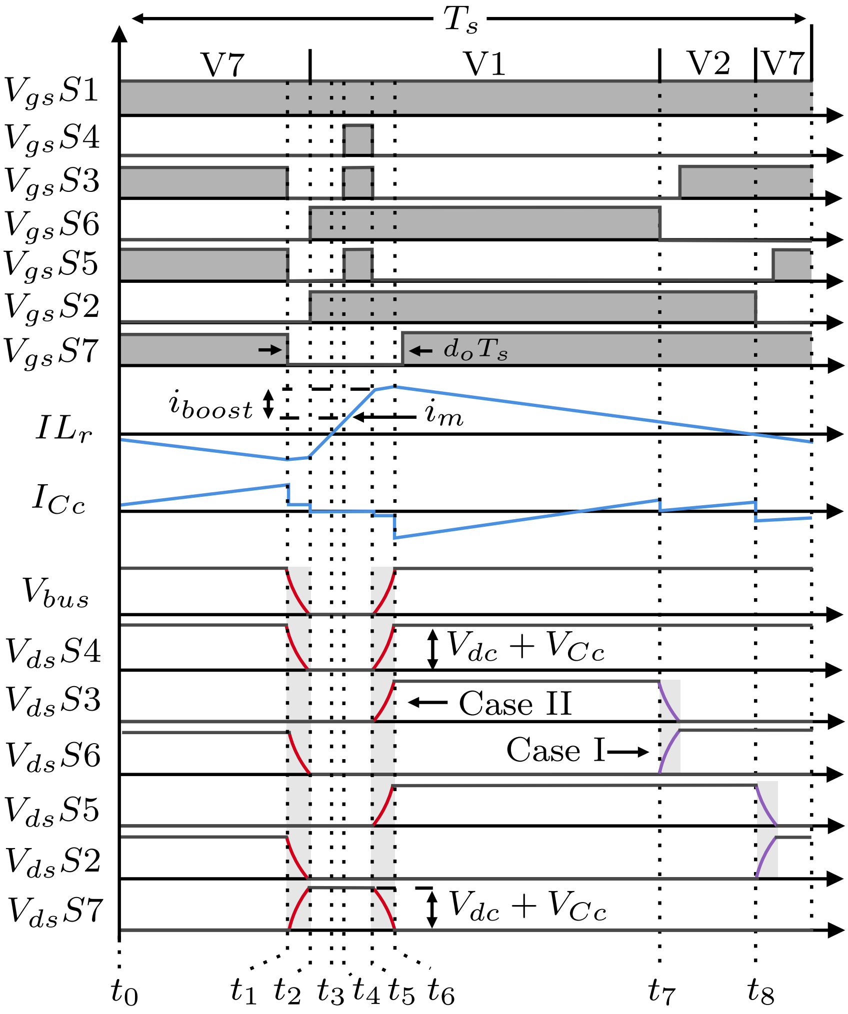


Figure 6.4: Switching patterns and theoretical waveforms of V_{gs}, I_{Lr}, I_{Cc} and drain-source voltage V_{ds} in Sector I-I. Case I commutation is shown in purple, while Case II commutation is shown in red.

Stage 1 ($t_0 - t_1$): Initial Stage.

The output vector of the inverter is in zero-state 111 with S_7, D_3 and D_5 in conducting state. In the auxiliary circuit, S_7 is in conducting state and the resonant inductor L_r is charged by C_c. The size of C_c is large enough that the voltage across C_c is constant during a switching cycle. In the initial stage, the current across the auxiliary switch is $i_{S7} = -I_{Lr}$ and $V_{bus} = V_{dc} + V_{Cc}$. The equivalent circuit of the initial stage is shown in Figure 6.5(a).

Stage 2 ($t_1 - t_2$): First Resonance.

Upon deactivation of S_7, the resonant inductor L_r discharges the parallel capacitors C_4, C_6, C_2 and resonates V_{bus} to zero. The time for the first resonance in the main switches is called the resonance fall, denoted as t_{fr}. Simultaneously, L_r also resonates the voltage of C_7 to the sum of the dc voltage V_{dc} and the clamping capacitor voltage V_{Cc}. The equivalent circuit diagram is shown in Figure 6.5(b).

Stage 3 ($t_2 - t_4$): Freewheeling Diodes.

Following the first resonance, freewheeling body diodes D_4, D_6 and D_2 begin to conduct and ZVS is realised for S_6 and S_2. The resonant inductor current I_{Lr} reaches zero at t_3 and the freewheeling diodes are turned-off. The motor currents of phase b, i_{mb} and phase c, i_{mc} now commutate the diodes D_3 and D_5 to S_6 and S_2. I_{Lr} is now the the sum of $i_{mb} + i_{mc}$ at t_4. The equivalent circuit diagram is shown in Figure 6.5(c).

Stage 4 ($t_4 - t_5$): Short Circuit.

At t_4, all six main switches are turned-on, entering the short-circuit mode. This results in I_{Lr} increasing linearly by the boost current i_{boost}; whereas, V_{bus} is clamped to zero. During this stage, L_r stores energy for the ZVS turn-on of the auxiliary switch S_7. This stage is necessary to raise the value of I_{Lr}, and without this stage ZVS of the auxiliary switch can not be achieved. The equivalent circuit diagram is shown in Figure 6.5(d).

Stage 5 ($t_5 - t_6$): Second Resonance.

At t_5, Switch S_4, S_3 and S_5 are turned-off, and the energy stored in L_r discharges the voltage of the clamping capacitor. This resonates C_4, C_3 and C_5 to $V_{dc} + V_{Cc}$ and C_7 to zero. This stage ends when S_7 achieves ZVS. The time for the second resonance in the main switches is called the resonance rise, denoted as t_{rr}. The equivalent circuit diagram is shown in Figure 6.5(e).

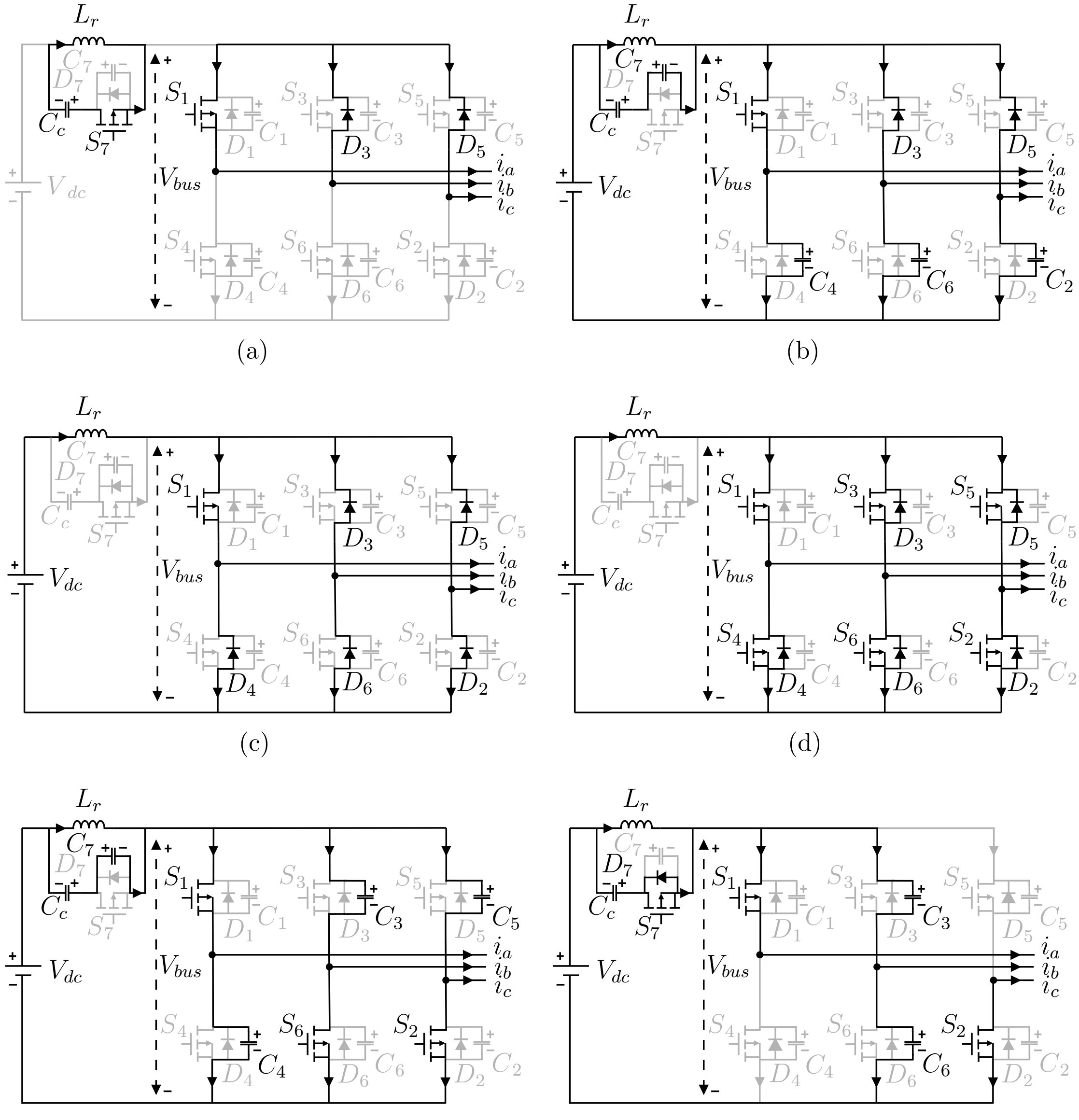
Stage 6 (t_7/t_8): Case I Commutation.

At t_7, S_6 is turned-off and initiates the charging of capacitor C_6. Subsequently, capacitor C_3 is discharged as S_3 is turned-on. Similarly at t_8, switch S_2 is turned-off and S_5 is turned-on through the parallel capacitors, as shown in Figure 6.5(a). The charging and discharging of parallel capacitors occur for a duration corresponding to the natural rise and fall time t_n. The equivalent circuit corresponding to this process at time t_7 is illustrated in Figure 6.5(f).

6.2.3 Limitations of Existing Inverter for Overvoltage Mitigation

Previous investigations of the ZVS topology have exclusively focused on photovoltaic and grid-connected inverters. To this case, extending the $\mathrm{d}v/\mathrm{d}t$ is possible by varying the resonant parameters. However, any attempts to characterise $\mathrm{d}v/\mathrm{d}t$ during resonant commutations could lead to inconsistencies in the observed $\mathrm{d}v/\mathrm{d}t$ value during natural commutations. In cable-fed motor drives, $\mathrm{d}v/\mathrm{d}t$ control of both resonant and natural commutations is necessary to not excite the cable antiresonance, and mitigate motor overvoltage [125]. As shown in Figure 6.4, the time for each commutation will not be the same value, i.e., $t_{rr} \neq t_{fr} \neq t_n$. This is further elaborated with experimental validation in Section 6.4.2. How to characterise and profile all types of ZVS commutations is addressed in this chapter.

It is also highlighted in previous literature that the ZVS turn-off losses in soft-switching inverters can be substantially reduced by extending the voltage rise time [178]. However, in most cases this is not practical since prolonging the rise time will significantly sacrifice system performance at high switching frequencies. Since this chapter focuses on profiling each type of resonant and natural commutation, the switching turn-off losses are improved by extending the rise time to a specific value without negatively impacting the system performance.



(a) (b)

(c) (d)

(e) (f)

Figure 6.5: Equivalent circuits of resonant and natural stages. (a) Stage 1 - initial stage ($t_0 - t_1$). (b) Stage 2 - first resonance ($t_1 - t_2$). (c) Stage 3 - freewheeling diodes ($t_2 - t_4$). (d) Stage 4 - short circuit ($t_4 - t_5$). (e) Stage 5 - second resonance ($t_5 - t_6$). (f) Stage 6 - Case I commutation (t_7).

6.3 Resonant Parameter Design

Following a detailed study into the control of the inverter, it has been established that ZVS is possible through the resonant action of L_r and C_r. In general, the principles to select the resonant parameters has been discussed before [178]. Also the principle of actively profiling $\mathrm{d}v/\mathrm{d}t$ to not excite cable antiresonance has been extensively discussed [125]. The essence of profiling the $\mathrm{d}v/\mathrm{d}t$ is applied to this ZVS inverter at each type of commutation. As a result, the following section focuses on how to select the resonant parameters of L_r and C_r.

6.3.1 Selection of the Resonant Inductor L_r

The ZVS inverter's resonant stages or also referred as Case II commutations are comprised of two distinct events: resonant fall and resonant rise commutations. The resonant inductor is designed to charge and discharge the resonant capacitors in these stages by storing energy. However, it is preferable to limit the value of the inductor to reduce capital costs, inverter losses and volume. The analysis of the maximum $\mathrm{d}v/\mathrm{d}t$ for the resonant stages is analysed by the application of Kirchhoff's voltage law [178] as follows:

$$\frac{\mathrm{d}}{\mathrm{d}t}v_{fr\_\max} = \frac{V_{dc}}{\sqrt{L_r C_{rt}}} \tag{6.1}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}v_{rr\_\max} = \frac{V_{dc}}{\sqrt{L_r C_{rt}}} - \left[\frac{\sqrt{3}I_{m\_\max}}{2C_{rt}} + \frac{3m_i I_{m\_\max}}{2C_{rt}}\right] \tag{6.2}$$

where $v_{fr\_\max}$ is the maximum resonant fall voltage and $v_{rr\_\max}$ is the maximum resonant rise voltage.

Assuming that all the parallel resonant capacitors are of the same value, i.e. $C_r = C_1 = C_3 = C_5 = C_4 = C_6 = C_2 = C_7$, the total resonance capacitance, $C_{rt} = 4(C_r + C_{oss})$ where C_{oss} is the output capacitance (for this chapter, the value for the SiC MOSFET Wolfspeed C2M0080120D is used, with a value of 92 pF [142]).

Given that the maximum drain-source voltage V_{ds} is expressed as $V_{dc} + V_{Cc}$, and assuming unequal rise times for resonant fall commutations and resonant rise commutations, L_r is designed based on the falling commutations (6.1), using

$$L_r = \frac{1}{C_{rt}}\left(\frac{V_{dc}t_{fr}}{V_{dc} + V_{cc}}\right)^2 \tag{6.3}$$

The resonant inductance can also be determined by the rising commutations; however, as later described in Section 6.3.3, only the falling commutations are required.

6.3.2 Selection of the Resonant Capacitor C_r

In the context of Case I natural commutation, the determination of the optimal voltage slew rate $\mathrm{d}v_n/\mathrm{d}t$ configuration relies upon the distinctive charging and discharging attributes exhibited by C_r associated with each main switch. This in turn, affects the $\mathrm{d}v_n/\mathrm{d}t$ values for each main switch in Case I natural commutation. The application of Kirchhoff's first law enables the assessment of $\mathrm{d}v/\mathrm{d}t$ for each main switch, taking into account the charging and discharging characteristics of C_r:

$$\frac{\mathrm{d}}{\mathrm{d}t}v_n = \pm\frac{i_m}{2(C_r + C_{oss})} \tag{6.4}$$

whereby the polarity change represents the charging and discharging of the resonant capacitors. Since the SVPWM has been modified to allow for two concurrent commutations, the maximum motor current is $\frac{\sqrt{3}}{2}I_{m\_\max}$ with respect to the conventional SVPWM [178]. The natural commutation slew rates using $I_{m\_\max}$ is found as

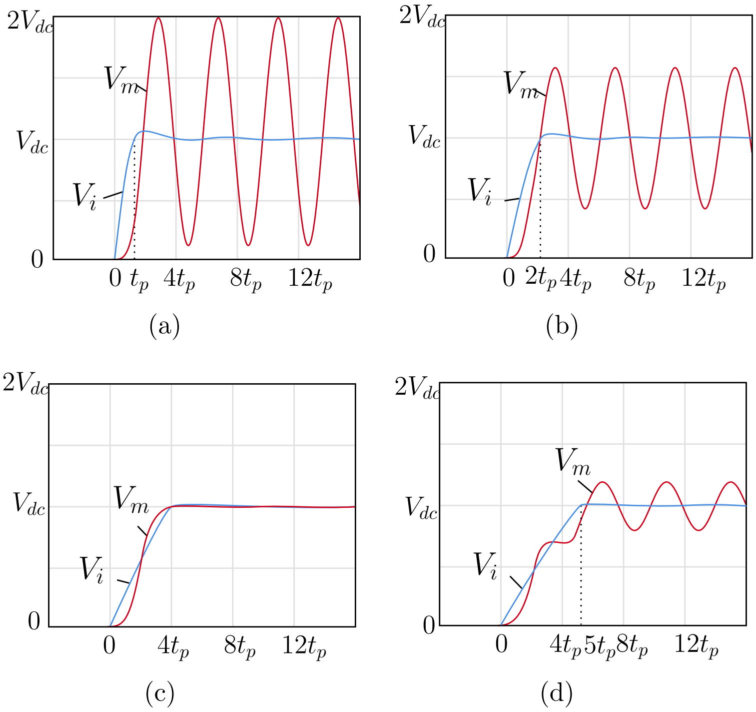
$$\frac{\mathrm{d}}{\mathrm{d}t}v_n = \pm\frac{\sqrt{3}I_{m\_\max}}{C_{rt}} \tag{6.5}$$

With the specified natural rise and fall times t_n and $I_{m\_\max}$ of the modified SVPWM, the parallel resonant capacitance is determined from (6.5) as:

$$C_r = \frac{\sqrt{3}t_n I_{m\_\max}}{4(V_{dc} + V_{Cc})} - C_{oss} \tag{6.6}$$

6.3.3 Design Procedure for Overvoltage Mitigation

The relationship between motor overvoltage and the propagation delay t_p is depicted in Figure 6.6. It is observed that the overvoltage oscillations can effectively be suppressed by designing the rise times to $4t_p$, with t_p being determined by the specific cable length and its inherent characteristics. As shown in Figure 6.6(d), the motor voltages V_m no longer fully neutralise one another at $5t_p$, resulting in an overvoltage despite the longer rise time. Thus, complete suppression of V_m occurs when the inverter voltage V_i does not excite the cable antiresonance, and



(a) (b)

(c) (d)

Figure 6.6: Drive system inverter voltage V_i and motor voltage V_m at increasing rise times for cable propagation time $t_p = 65$ ns. (a) t_p. (b) $2t_p$. (c) $4t_p$. (d) $5t_p$. (Simulation study representing PWM source of varying rise times feeding into 15 m ac cable with motor-side represented as an open circuit.)

$$t_r = 4at_p \tag{6.7}$$

where $a \in \mathbb{Z}^+$. This phenomenon is explained by the superposition principle, where V_i is divided into two equal pulses with a temporal time displacement of $2t_p$. Given the assumption of unity reflection coefficients [127], both inverter voltages are reflected at twice the magnitude at the motor terminals. Due to the time displacement, the resultant motor voltages cancel each other at $4at_p$ [125].

As the ZVS inverter encompasses distinct commutation modes such as resonant fall, resonant rise, and natural, the rise times exhibit variability. To guarantee the uniform mitigation of overvoltage in the ZVS inverter, meticulous consideration must be given to the design of the rise times at each resonant and natural commutation event. As noticed from (6.1) and (6.2), the values of $\mathrm{d}v/\mathrm{d}t$ can not be equal without restricting V_{dc} or $I_{m\_\max}$, such that:

$$\left|\frac{\mathrm{d}}{\mathrm{d}t}v_{fr\_\max}\right| > \left|\frac{\mathrm{d}}{\mathrm{d}t}v_{rr\_\max}\right| \tag{6.8}$$

To this extent, the resonant rise $\mathrm{d}v_{rr\_\max}/\mathrm{d}t$ from (6.2) is denoted as a function of the resonant fall $\mathrm{d}v_{fr\_\max}/\mathrm{d}t$ from (6.1) and natural $\mathrm{d}v_n/\mathrm{d}t$ from (6.5) with a modulation index $0.4 \leq m_i \leq 0.8$ as follows:

$$\begin{aligned}\frac{\mathrm{d}}{\mathrm{d}t}v_{rr\_\max} &= \frac{V_{dc}}{\sqrt{L_r C_{rt}}} - \left[\frac{\sqrt{3}I_{m\_\max}}{2C_{rt}} + \frac{3m_i I_{m\_\max}}{2C_{rt}}\right] \\ &= \frac{\mathrm{d}}{\mathrm{d}t}v_{fr\_\max} - \frac{\mathrm{d}}{\mathrm{d}t}v_n\left[\frac{1}{2}\left(1+\sqrt{3}m_i\right)\right] \\ &\approx \frac{\mathrm{d}}{\mathrm{d}t}v_{fr\_\max} - \frac{\mathrm{d}}{\mathrm{d}t}v_n\end{aligned} \tag{6.9}$$

From (6.9), it is observed that the $\mathrm{d}v/\mathrm{d}t$ can be profiled by carefully selecting the rise time at each commutation. This is possible since the change in PWM voltage magnitude at each commutation have the same value (i.e., $V_{dc} + V_{Cc}$). The rise time selection for each $\mathrm{d}v/\mathrm{d}t$ is mathematically expressed as follows:

$$\underbrace{\frac{\mathrm{d}}{\mathrm{d}t}v_{rr\_\max}}_{t_{rr}=8t_p} \approx \underbrace{\frac{\mathrm{d}}{\mathrm{d}t}v_{fr\_\max}}_{t_{fr}=4t_p} - \underbrace{\frac{\mathrm{d}}{\mathrm{d}t}v_n}_{t_n=8t_p} \tag{6.10}$$

By using this expression, with the predetermined rise times for each commutation the motor overvoltage can be mitigated. Following this, it is imperative first to establish C_r in (6.6) by utilising $t_n = 8t_p$. Subsequently, L_r can be calculated using the established capacitance and inductance from (6.3) by using $t_{fr} = 4t_p$. As per (6.1), by setting a constraint on the maximum rise time, this will enable t_{rr} to be equal to $8t_p$. From this selection the $\mathrm{d}v/\mathrm{d}t$ at each commutation does not excite the cable antiresonance. Therefore, complete overvoltage suppression can be achieved at both the resonant and natural rise times. A diagram outlining this process is found in the guidelines illustrated in Figure 6.7.

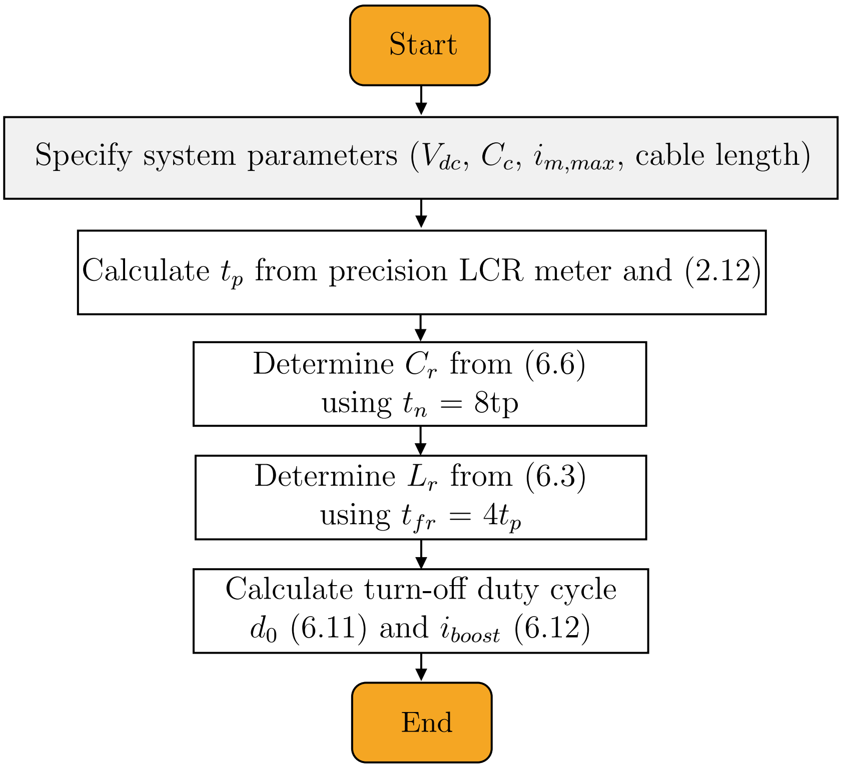


Figure 6.7: Guideline procedure for determining the ZVS inverter resonant parameters.

6.3.4 Voltage and Current Stress on Main Switches

When MOSFETs are subjected to high voltage and current stress, there is a risk of them becoming damaged or even failing altogether. This results in reduced efficiency, reduced power output, and increased heat dissipation, which ultimately leads to premature failure of the MOSFET and the inverter as a whole. Therefore, upon designing the resonant parameters, it is equally as important to ensure the voltage and current are within the limits of the active switches.

To this extent, when the converter is operating at steady state, the clamping capacitor voltage V_{Cc} is be defined since the resonant inductor must obey the volt-second balance principle:

$$V_{Cc} = \frac{d_o}{1 - d_o} V_{dc} \tag{6.11}$$

whereby d_o is defined as the ratio S_7 is switched-off, also referred as the turn-off duty cycle. Since the voltage across the main switches is $V_{dc} + V_{Cc}$, to avoid high voltage stress, d_0 should be designed less than 0.1 [181]. This will result in V_{Cc} approximately less than 10% of V_{dc}. However, it is worth mentioning that this will also result in higher

S_7 conduction losses, as will be explained later in the simulation loss study.

To examine the current stress on the active switches, the minimum i_{boost} must first be calculated. Assuming that all the parallel resonant capacitors are of the same value, the minimum i_{boost} is expressed as [181]

$$i_{boost} \geq \sqrt{\left(\frac{V_{dc}^2 - V_{Cc}^2}{Z_r^2} - 2I_{m\_\max}\right)^2 - \frac{V_{dc}^2 - V_{Cc}^2}{Z_r^2}} \tag{6.12}$$

where the resonant impedance, $Z_r = \sqrt{L_r/C_{rt}}$. From this expression, the current of the resonant inductor, I_{Lr} [175] is expressed as

$$I_{Lr}(t_6) = \sqrt{\frac{V_{dc}^2 - V_{Cc}^2}{Z_r^2} + i_{boost}^2} + i_m \approx \frac{V_{dc}}{Z_r} + \sqrt{3}i_m m_i \tag{6.13}$$

The current stress at the auxiliary switch ($i_m + i_{L_r}$) and main switches ($i_m + i_{boost}/3$) can be calculated using (6.12) and (6.13). It is noticed that the current stress can be limited by increasing the resonant impedance, Z_r [175]. Therefore, the design for overvoltage mitigation must consider Z_r or increase the current rating of the auxiliary and main switches. One way to accomplish this is to increase L_r with respect to C_r. Specifically, a different set of resonant rise and fall time requirements can be chosen as long as t_r (6.7) is met for all natural and resonant commutations. Adherence to this condition ensures that the voltage does not cause excitation of the cable antiresonance. Neglecting the influence of Z_r may give rise to MOSFET malfunctioning, particularly in extended utilisation periods, potentially incurring higher expenses in maintenance and replacement.

6.3.5 Volume Considerations

Considering cable-fed motor drives are designed to operate in harsh conditions where space may be limited, the volume of the inverter is critical. The dimensions of the primary components in the ZVS system are presented in Figure 6.8. The selection of passive components was based on the system specifications, which were meticulously evaluated to satisfy the demands of a 1.23 kW ac PMSM, functioning at a 20 kHz switching frequency and powered by a dc voltage of 300 V. The $\mathrm{d}v/\mathrm{d}t$ prerequisites were taken into consideration to ensure seamless system operation and to preclude any issues that may arise, such as voltage spikes or excessive heat. Through the selection

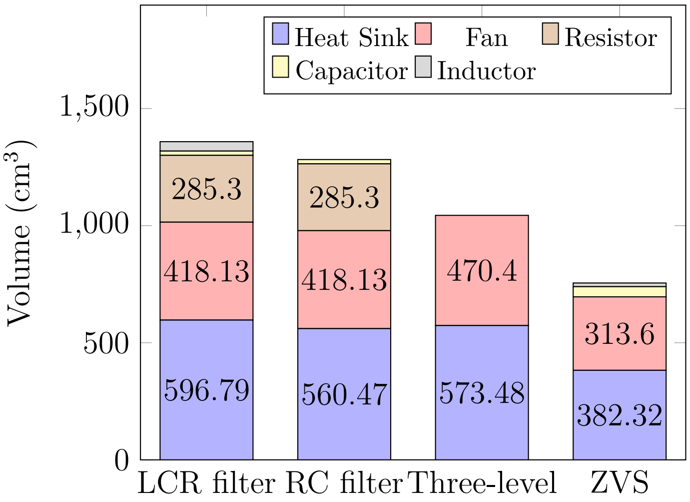


Figure 6.8: Volume comparison of main components of conventional two-level inverter with a passive LCR and RC filter, Q3L three-level inverter and ZVS inverter. The total volumes of the inverter (including the resonant inductor and capacitance) are correspondingly 1358.45, 1282.13, 1043.88 and 742.54 cm^3. These values increase to 1359.7, 1283.4, 1046.4 and 743.8 cm^3 when the gate drivers (Texas Instruments ISO5452-Q1) are accounted for.

of passive components that can accommodate the necessary dv/dt specifications, the system can operate securely and uphold consistent performance.

The sizing of the heat sink is determined by natural air convection and involves calculating the thermal resistance of the heat sink. This calculation takes into account the simulated power losses, as later discussed in Section 6.4.1, and also considers the heat sink temperature from PLECS (Plexim) simulations. The ambient temperature of 40°C is taken into consideration for these computations [182]. Subsequently, the heat sink volume can be found using the method described in [183]. This process includes using curve fitting techniques to establish a correlation between the volume of different extruded heat sinks and their corresponding heat sink thermal resistances. Additionally, for all active switches, the packaged DYNATRON heat sink and cooling fan (Part No. G199) [146] are employed to ensure effective heat dissipation.

The ZVS inverter and two-level with LCR filter utilises ferrite leaded inductors from Würth Elektronik [184], whereas the two-level filter inverters uses low-inductive 100 Ω resistors from Ohmite [185]. Additionally, 10 nF polypropylene film capacitors from Panasonic [186] are utilised in both the ZVS inverter and passive filters. The volume of each component was determined based on the dimensions specified in their respective datasheets. Only a basic LCR and RC passive filter was implemented in this study; however, comprehensive information on more advanced filters is available in the literature [105].

The ZVS inverter exhibits a volumetric reduction of ≈30% compared to the Q3L three-level inverter and ≈40% reduction compared to the two-level inverter with an LCR and RC filter. It is also worth reminding that the LCR passive filter is typically installed at the inverter terminal, where the RC passive filter is installed at the motor terminal. Moreover, determining the size of C_c in the ZVS inverter is contingent upon the dc voltage stipulations to provide a constant voltage across its terminals in a switching period. Therefore, its practicality can be impacted by the availability of suitable constituent elements.

6.4 Design Verification

Table 6.1 presents the propagation time t_p for each cable length, as well as the computed values of C_r, L_r, and Z_r, which were obtained by following the prescribed protocol illustrated in Figure 6.7 and using a GW INSTEK precision LCR meter (LCR-8000G) operating up to 10 MHz. This step was critical for ensuring the precision and accuracy of the high-frequency transient overvoltage prediction prior to experimental validation.

Table 6.1: Cable Length and Resonant Parameters

Cable length (m)	t_p (ns)	C_r (nF)	L_r (μH)	Z_r (Ω)
5	21.6	0.59	2.27	28.88
10	43.3	1.27	4.55	28.90
15	65.0	1.96	6.82	28.87
20	86.7	2.64	9.10	28.86

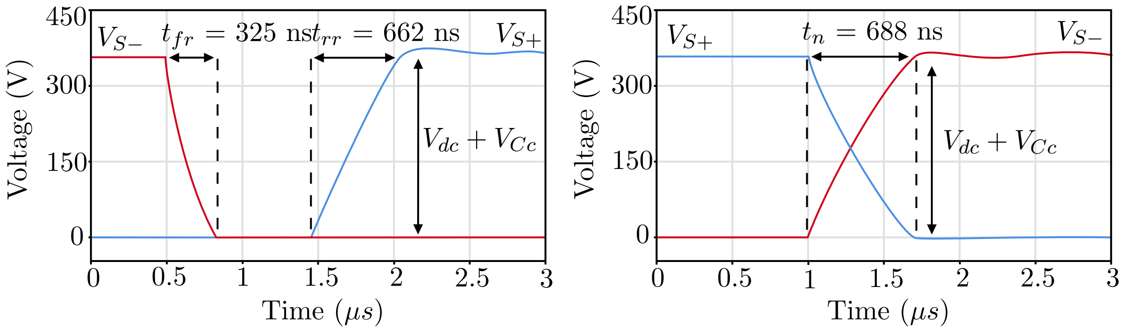
The resonant components, namely C_r and L_r, were rounded to the nearest commercially available component. Notably, it was observed that Z_r remained nearly the same value despite increasing the cable length. This is because the ratio of C_r and L_r was kept constant, and only t_p varied. It is important to note that these parameters were determined based on an experimental dc voltage of $V_{dc} = 300$ V and a maximum motor phase current of $I_{m\_\max} = 3$ A. A comprehensive summary of the system parameters for both simulation and experimental findings can be obtained from Table 3.2. Changing these system parameters, such as the load current, can slightly impact the mitigation of motor overvoltage, as discussed in Section 6.4.2.

6.4.1 Simulation Results

To assess the effectiveness of the ZVS topology in mitigating overvoltage, a co-simulation was performed using MATLAB/Simulink and PLECS (Plexim). The simulation utilised a high-frequency ac cable and motor model from [126], as outlined in Chapter 2 and Appendix B.1.2, to ensure the faithful reproduction and forecasting of transient overvoltage oscillations. This cable model includes the impact of both the skin and proximity effects and the dielectric losses at high-frequency range.

Overvoltage Mitigation Comparison

The resonant commutations during the rise and fall phases of a single switching transition is depicted in Figure 6.9(a). It is crucial, as per (6.8), to ensure that the $\mathrm{d}v/\mathrm{d}t$ during the resonant fall commutations surpasses that of the resonant rise commutations. To achieve this, the duration of t_{rr} is established as 8 times the duration of t_p, while t_{fr} is set to 4 times t_p. The resonant rise time and resonant fall time were computed using a measured value of t_p of 86.7 ns for a 20 m cable. The computed values for the resonant rise time and resonant fall time were 693.6 ns and 346.8 ns, respectively. A comparison of these computed values with the simulated results revealed a disparity of approximately 5%. Similarly, in Figure 6.9(b), the natural commutations during the rise and fall transitions are also configured to last 8 times t_p to satisfy (6.10), and a comparison with the computed rise times showed a deviation of 1% in the simulated outcomes. These commutations are arranged in such a way as to prevent cable antiresonance and thereby minimise overvoltage.



(a) (b)

Figure 6.9: ZVS commutation comparison of inverter voltages V_s with active $\mathrm{d}v/\mathrm{d}t$ profiling. (a) Resonant fall and resonant rise commutations. (b) Natural fall and natural rise commutations. (Simulation parameters: Resonant inductance $L_r = 9.10$ μH, resonant capacitance $C_r = 2.64$ nF, cable length = 20 m and cable propagation time $t_p = 86.7$ ns.)

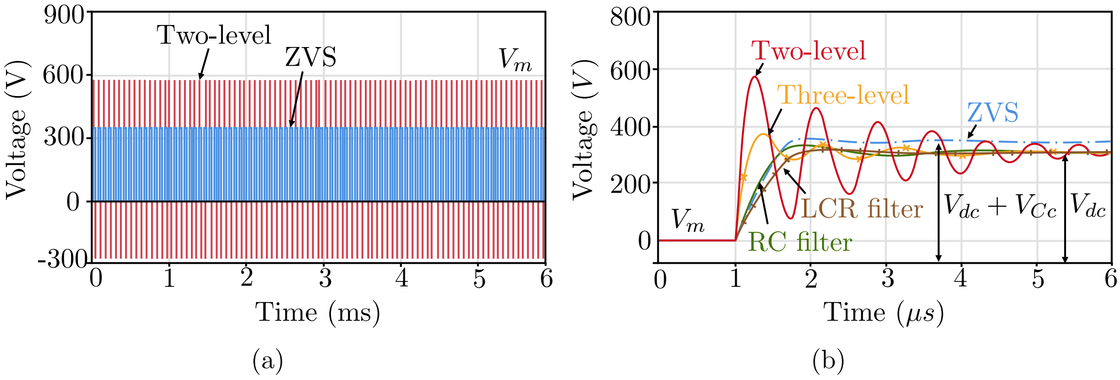


Figure 6.10: Simulated motor voltage V_m comparisons. (a) Motor voltage comparing two-level inverter with no passive filter with the ZVS topology. (b) Extended view comparing two-level inverter with no passive filter, two-level with LCR and RC filter, Q3L three-level inverter and ZVS inverter. (Simulation parameters: $L_r = 9.10\ \mu$H, $C_r = 2.64$ nF, cable length = 20 m and $t_p = 86.7$ ns.)

It has been established that maintaining the motor voltage at V_{dc} is crucial, as any excess voltage surpassing the PDIV may lead to motor damage. In order to evaluate this, the performance of the ZVS topology was compared with that of the conventional two-level converter without any passive dv/dt filters, while keeping the basic parameters the same, as depicted in Figure 6.10(a). The two-level converter was utilised as a baseline example to identify the worst-case scenario for motor overvoltage. It was observed that the two-level converter phase voltage V_m was simulated to reach approximately double the inverter dc voltage V_{dc} at 560 V, which could lead to rapid insulation failure and compromise the motor's long-term reliability. Irrespective of the V_{dc} magnitude, it is noteworthy that the motor overvoltage in the two-level converter will rise. For instance, if V_{dc} is equal to 2000 V, the estimated V_m would be around 4000 V at long cable lengths (i.e., $\geq$ 20 m).

Through the implementation of the ZVS topology with active dv/dt profiling, the overvoltage of the motor is effectively eradicated and limited to the inverter bus voltage $V_{dc} + V_{Cc}$ at 345 V, as illustrated in Figure 6.10(b). It is noteworthy that the phase-to-phase voltage $V_{i,ab}$ of the ZVS inverter is equivalent to $V_{dc} + V_{Cc}$ due to the existence of the clamping capacitor and resonant action in the auxiliary circuit, thereby reducing the motor overvoltage to this higher voltage level. The elimination of motor overvoltage is accomplished by prolonging and actively regulating the rise times of each commutation type, as further depicted in Figure 6.9. Consequently, the motor voltage remains below PDIV, resulting in a longer lifespan for the motor.

It is worth noting that extended exposure to high temperatures or mechanical stress can lead to slight fluctuations in the values of C_r, which can influence the pre-

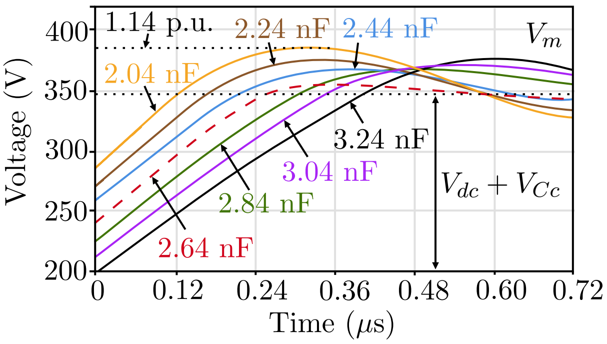


Figure 6.11: Motor voltage V_m with variations in resonant capacitance C_r during natural rise commutation. (Simulation parameters: $L_r = 9.10\ \mu$H, cable length = 20 m and $t_p = 86.7$ ns.)

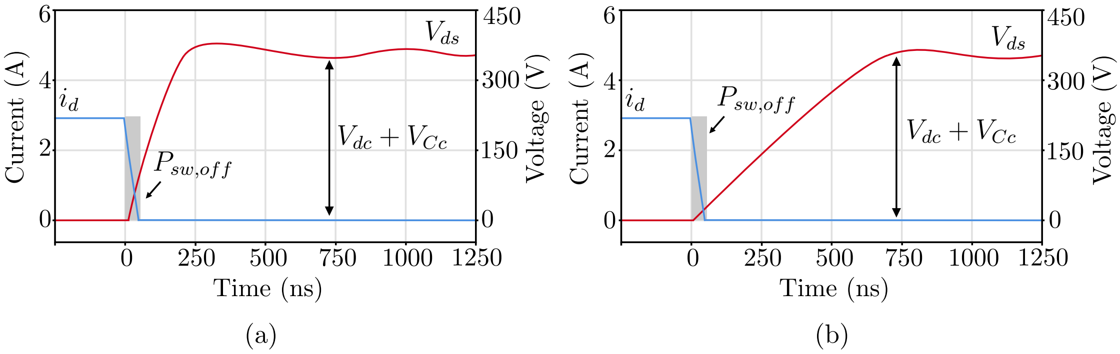
determined rise and fall times, ultimately affecting overvoltage mitigation. Figure 6.11 illustrates the simulated relationship between C_r and V_m for a 20 m cable, revealing that V_m increases up to 1.14 p.u. when C_r deviates from the optimal value of 2.64 nF. While variations in L_r can also impact V_m, its effect is less significant, particularly if L_r does not deviate considerably from its ideal value. Moreover, these variations in L_r only affect resonant commutations and not natural commutations.

Furthermore, passive components may undergo gradual ageing effects over extended periods, contingent on factors such as component quality, construction, and operating conditions. To mitigate the risks associated with ageing phenomena, it is advisable to opt for components with appropriate tolerances and perform regular inspections and replacements.

Loss Distributions

The switching loss, encompassing both turn-on and turn-off losses, was investigated through simulations in PLECS (Plexim) using SiC MOSFET C2M0080120D and various resonant parameters in the ZVS inverter. The inverter losses were calculated based on parameters provided in the Wolfspeed datasheet [142]. This includes the internal gate resistance R_{g-in}, external gate resistance R_{g-ext} and normally on-state resistance $R_{ds,on}$. The gate drive voltage is set as $-5/20$ V during turn-off V_{ggl} and turn-on V_{ggh}. The critical parameters are extracted from the datasheet and further detailed in Table 3.2. By using manufacturer data, multi-dimensional lookup tables were employed to accurately estimate and average the losses.

In order to ascertain the switching losses in the ZVS topology, simulation was performed on different ZVS inverter models featuring distinct resonant parameters.



(a) (b)

Figure 6.12: Simulated ZVS switching turn-off waveforms at different rise times showing the turn-off losses $P_{sw,off}$. Switching waveforms with actively profiled natural fall times for a: (a) 5 m cable; (b) 20 m cable.

These models were simulated for cable lengths of 5 m, 10 m, 15 m, and 20 m as shown in Table 6.1. The 1 m cable with no $\mathrm{d}v/\mathrm{d}t$ profiling was only used as a base comparison, as the overvoltage phenomenon does not occur at this cable length. The simulated efficiency of the whole motor drive system can also be calculated by subtracting the respective power loss of each component such that

$$\eta_{sys,sim} = \frac{P_{in} - \left(P_{inv} + P_{mot} + P_{cable}\right)}{P_{in}} \times 100 \tag{6.14}$$

Although the ZVS inverter exhibits negligible switching turn-on losses, an additional switching turn-off loss $P_{sw,off}$ is associated with the addition of the short circuit stage. Therefore, comprehending the significance of $P_{sw,off}$ when encountering slower $\mathrm{d}v/\mathrm{d}t$ is crucial. The ZVS turn-off loss is computed for each of the simulated inverter models and documented in Table 6.2. It is observed that the power loss is marginally reduced by employing a longer rise time. As further shown in Figure 6.12, during the ZVS turn-off transition, the voltage gradually rises from zero while the current rapidly decreases. In the ZVS inverter the voltage slew rate is systematically controlled through the parallel capacitors. In Figure 6.12(b), by increasing the duration of the turn-off transition, the drain-source voltage V_{ds} across the active switch rises, leading to a reduction in the product of V_{ds} and i_d during turn-off. However, it is crucial to carefully consider the tradeoff between desired performance metrics and optimal efficiency in order to determine the most favorable rise time for the specific ZVS inverter application. Additionally, while the turn-off power loss may decrease, this benefit is slightly offset by the increased power loss in the longer cable.

The power losses of the presented ZVS inverter are also compared to those of other

Table 6.2: Power Loss and Efficiency with Varying Cable Length

Cable ($8t_p$)	Power loss (W)	Efficiency
1 m (34.4 ns)	3.88	96.89%
5 m (172.8 ns)	3.85	96.89%
10 m (346.4 ns)	3.63	96.91%
15 m (520 ns)	2.75	96.98%
20 m (693.6 ns)	2.50	97.00%

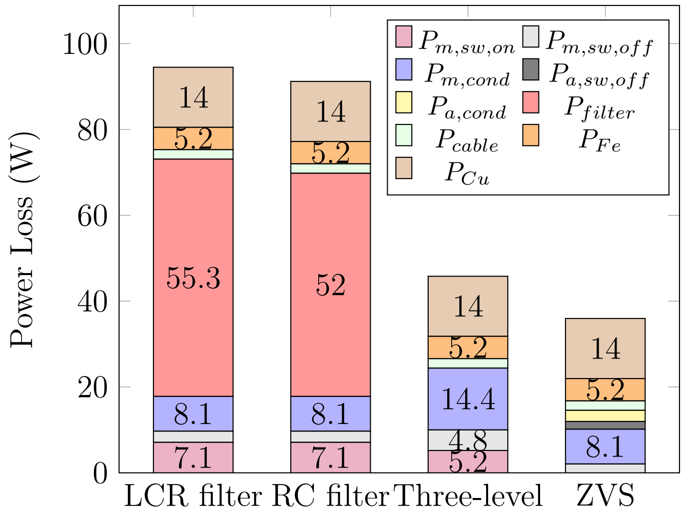


Figure 6.13: Power loss distribution comparison of two-level inverter with passive LCR and RC filter, Q3L three-level inverter and ZVS inverter. $P_{a,sw,off}$ and $P_{a,cond}$ are the switching turn-off and conduction power loss of the auxiliary switch. P_{filter} and P_{cable} is the filter power loss and power loss of the 20 m three-phase cable. The total power losses of the motor drive system are correspondingly 91.5 W, 88.2 W, 45.8 W and 36.0 W. (Simulation parameters: $T_L = 4$ Nm, $\omega_r = 3000$ rpm, $f_{sw} = 20$ kHz and $t_p = 86.7$ ns.)

conventional techniques employed for mitigating motor overvoltage, as depicted in Figure 6.13. The findings indicate that, despite the two-level converter requiring six active switches, it still incurs switching turn-on losses as well as significant power dissipation caused by the bulky RC and LCR filters. The Q3L three-level converter, while not requiring the use of passive filters, necessitates twelve active switches, thereby leading to increased switching and conduction losses relative to the ZVS inverter. Consequently, the ZVS inverter is deemed the most efficient solution. The total motor drive system efficiency at increasing load power is depicted in Figure 6.14. The outcomes show that the ZVS topology surpasses the conventional alternatives in terms of efficiency, with efficiency increasing for all topologies when approaching the rated power of 1.23 kW.

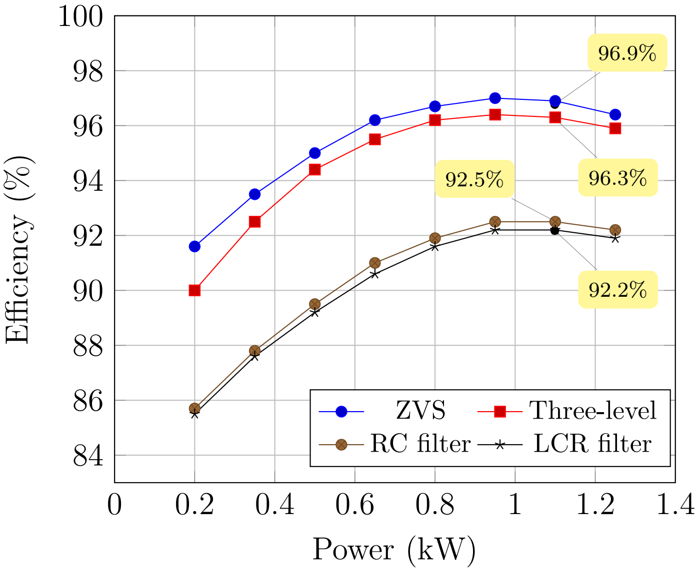


Figure 6.14: Simulated system efficiency of ZVS motor drive system compared with Q3L three-level inverter, two-level inverter with passive LCR and RC filter. ($t_p = 86.7$ ns, $f_{sw} = 20$ kHz, $m_i = 0.8$.)

6.4.2 Experimental Verification

To confirm the suitability of the presented ZVS parameter selection for mitigating motor overvoltage, the three-phase ZVS inverter is employed to deliver power to a motor via a range of long cables (5 m, 10 m, 15 m and 20 m). In line with this configuration, a four-core unscreened 16 AWG cable from Lapp [148] was employed with the earth core grounded. This provides a return path for CM currents, reducing the EMI within the cable and minimising interference with surrounding equipment and circuits.

A Tektronix THDP0200 200 MHz high voltage differential probe is utilised to measure the DM voltage between phase a and phase b, whereas the ac current is measured using a Tektronix TCP0020 50 MHz probe. The ground wire of the ac cable in this study was connected to a common-ground, although it may be the subject of future investigations exploring CM voltages. The experimental setup is further illustrated in Figure 6.15 and the inverter, motor and cable parameters are detailed in Table 3.2. Figure 6.16 shows the experimental platform in the laboratory. It should be noted that the same system parameters found in Table 3.2 are used in both simulation and experimental verification.

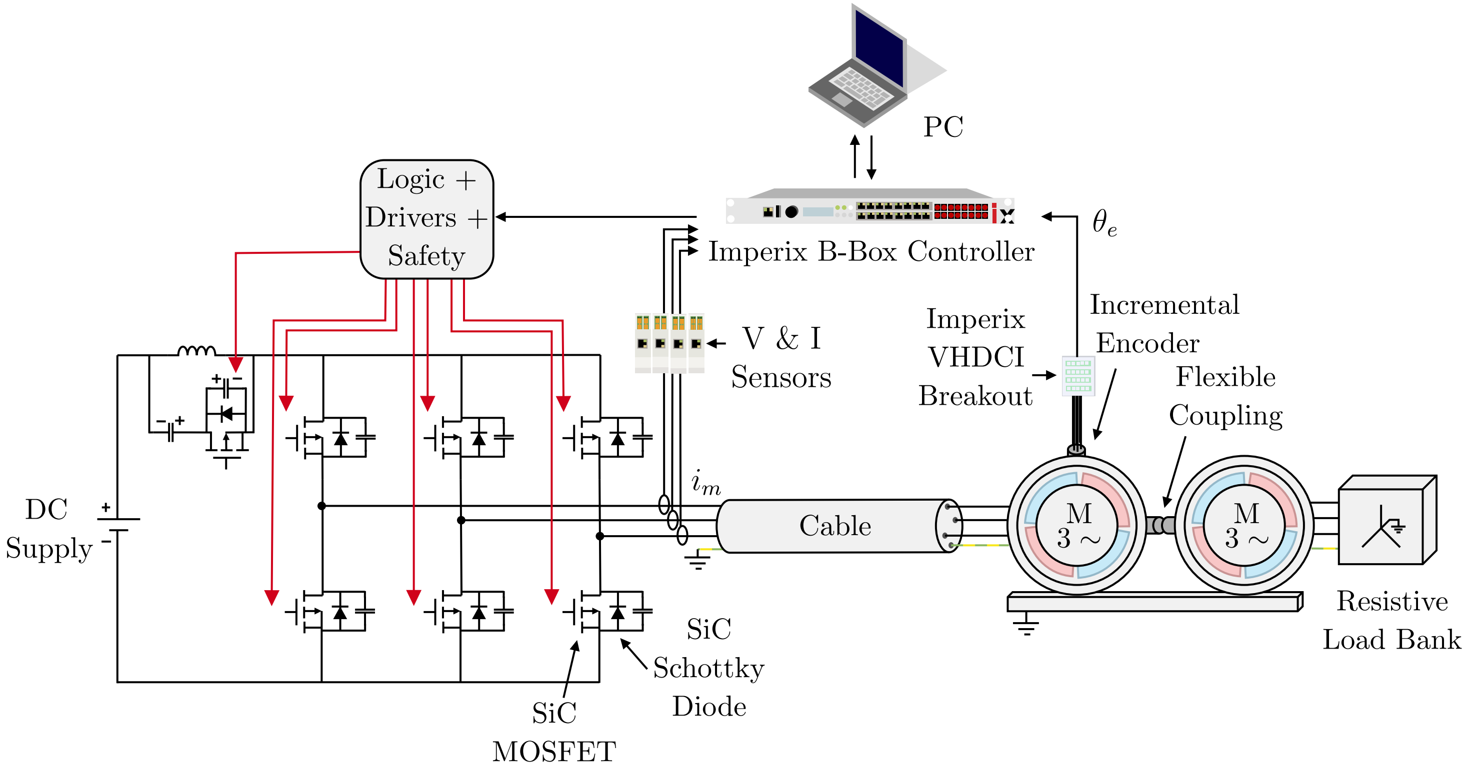


Figure 6.15: Overview of experimental setup.

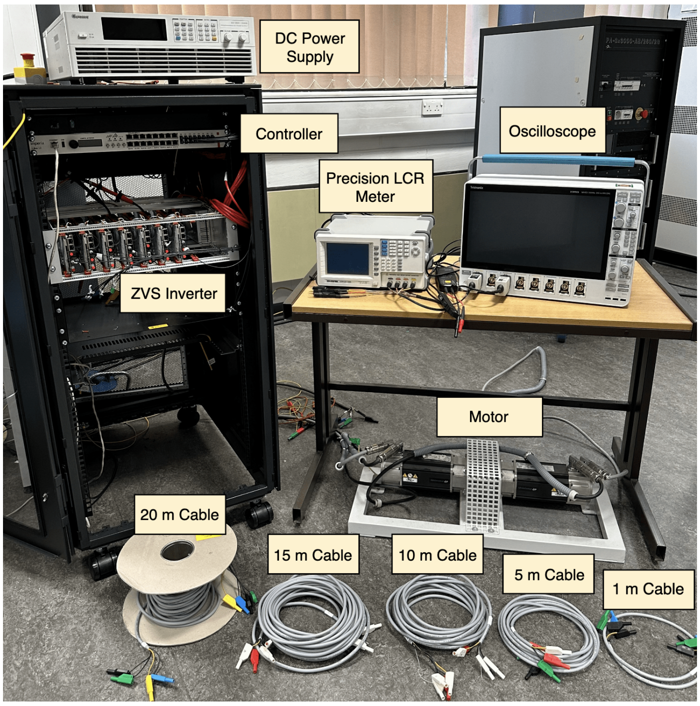
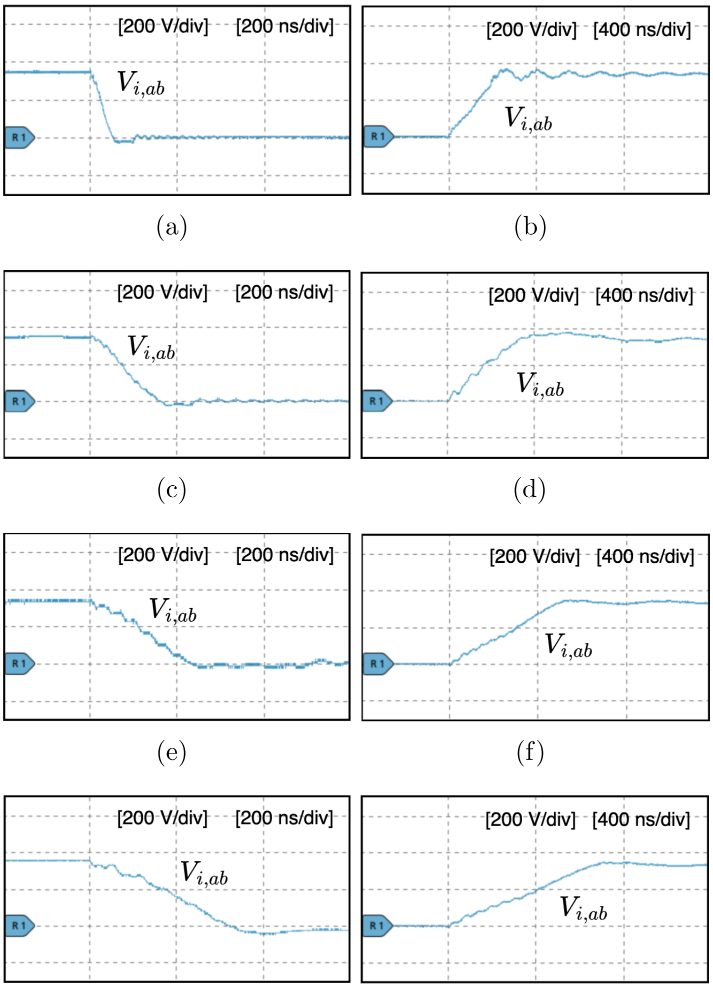


Figure 6.16: Experimental test bench of ZVS inverter and cable-fed motor.

Impact of Cable Length

To mitigate the motor overvoltage, it is imperative to develop an inverter that takes into account cable length and t_p. In this regard, four inverter models were established by utilising the parameters described in Table 6.1, incorporating actively profiled $\mathrm{d}v/\mathrm{d}t$ based on the cable length. As demonstrated in Figure 6.17, the $\mathrm{d}v/\mathrm{d}t$ for resonant fall and resonant rise commutations are increase when compared to the cable length. For example, with a 10 m cable, the resonant fall time $4t_p$ measures at 180 ns, whereas with a 20 m cable, it measures at 348 ns. Similarly, the resonant rise time $8t_p$ at 10 m measures at 400 ns, while at 20 m, it is 662 ns. It is pertinent to note that in hard-switching inverters, longer rise times are typically undesirable, as they increase switching losses. However, as mentioned in Chapter 6.4.1, this characteristic does not adversely impact losses in the ZVS inverter.

Upon conducting experimental analysis with a cable length of 20 m, a discrepancy of 7% was observed between the measured resonant fall times and the simulated values of 325 ns. Additionally, a deviation of 4% was noted between the measured and simulated resonant rise times of 688 ns. These deviations could be attributed to parasitic effects from the MOSFETs within the motor drive system or minor inaccuracies in the parameter modelling. Despite these variances, the $\mathrm{d}v/\mathrm{d}t$ remains within an acceptable range for effectively mitigating motor overvoltage, as illustrated in Figure 6.17.



(a) (b)

(c) (d)

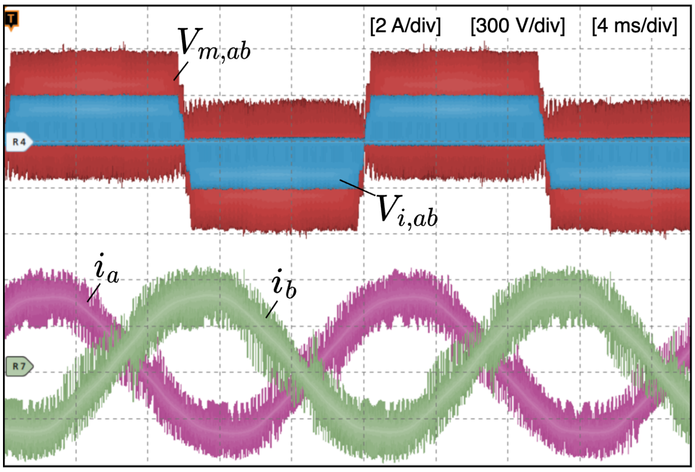
(e) (f)

(g) (h)

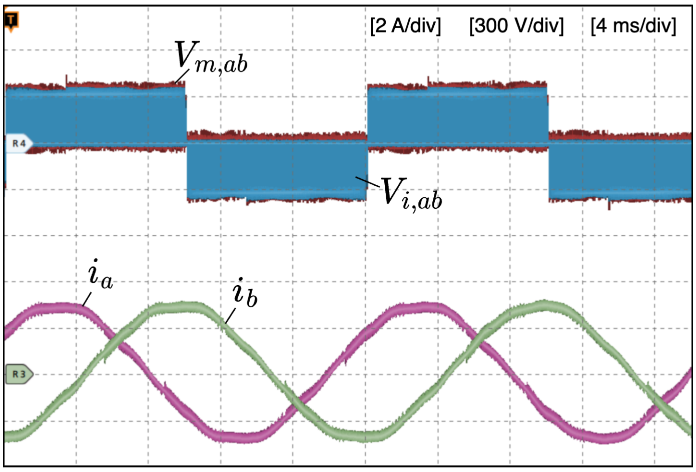
Figure 6.17: Experimental inverter switching waveforms of resonant fall ($4t_p$) and resonant rise ($8t_p$) showing the actively profiled $\mathrm{d}v/\mathrm{d}t$ for each cable length. (a)-(b) Cable length = 5 m. (c)-(d) Cable length = 10 m. (e)-(f) Cable length = 15 m. (g)-(h) Cable length = 20 m.

Figure 6.18 depicts a comparison of overvoltage mitigation between a hard-switching two-level inverter and the ZVS inverter with $\mathrm{d}v/\mathrm{d}t$ profiling, both implemented with a 20 m cable. To establish a base comparison, the hard-switching two-level inverter without a $\mathrm{d}v/\mathrm{d}t$ filter is designed by short-circuiting the auxiliary branch and removing the parallel resonant capacitors. To note, $V_{m,ab}$ represents the voltage on the DM motor side, whereas $V_{i,ab}$ represents the voltage on the DM inverter side between phases a and b. The measured rise and fall times for the two-level inverter with no filter are 52 ns and 31 ns correspondingly.

According to Figure 6.18(a), the motor experiences significant overvoltage, as evidenced by $V_{m,ab}$ reaching 2 p.u. This is attributed to the impact of the RWP and the



(a)



(b)

Figure 6.18: DM motor-side voltage V_m, inverter-side voltage V_i and two motor phase currents with a cable length of 20 m. (a) Hard-switching two-level inverter. (b) ZVS inverter.

high dv/dt of the SiC MOSFETs. However, if the motor and cable is not designed to tolerate this voltage range, the resultant overvoltage may surpass the PDIV of the rotor winding. This, in turn, could generate PDs, leading to a significant decline in the motor's operational lifespan. Furthermore, it is observed that the phase currents i_a and i_b exhibit a considerable amount of high-frequency harmonics. This phenomenon can be ascribed to the charging and discharging of the parasitic capacitance of the cable during the fast switching transients, leading to the occurrence of high magnitude spike currents.

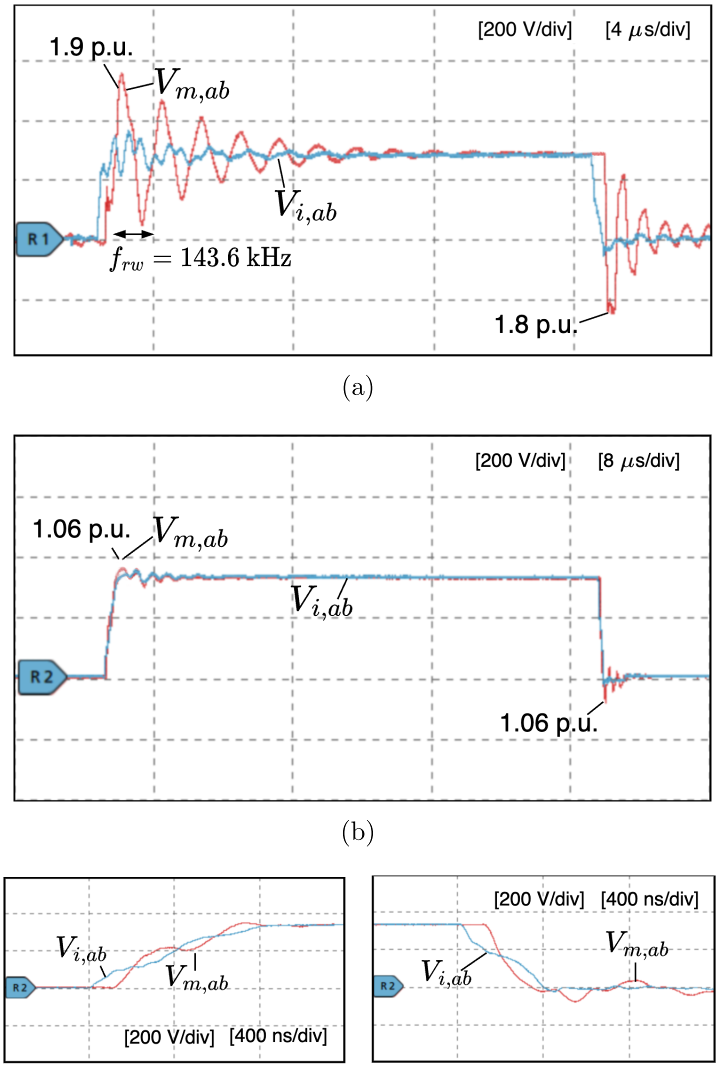
In contrast, the utilisation of the ZVS inverter technique can mitigate motor overvoltage, as depicted in Figure 6.18(b), where the $V_{m,ab}$ is reduced to approximately

1 p.u. This outcome can be attributed to the dv/dt profiling of all three types of commutations, including resonant rise, resonant fall, and natural commutations. Additionally, this method yields a smoother PWM voltage pulse, leading to a considerable reduction in the occurrence of high-frequency harmonics in the motor phase currents.

Figure 6.19 provides a view of the motor voltage within one PWM voltage pulse. Upon analysing the hard-switching two-level motor drive system in Figure 6.19(a), it is observed that the maximum motor overvoltage is 1.9 p.u. during the rising edge and 1.8 p.u. during the falling edge. This phenomenon is consistent with the simulated results, which also exhibit a peak overvoltage of 1.9 p.u., as illustrated in Figure 6.10(b). The occurrence of this issue can be attributed to the high dv/dt, which leads to the RWP in the motor drive system. Moreover, the analysis also indicates that the frequency of the motor overvoltage is 143.6 kHz, which aligns with the calculated reflected wave frequency f_{rwp} [54].

$$f_{rwp} = \frac{1}{4lt_p} = 144.2 \text{ kHz} \tag{6.15}$$

In contrast, Figure 6.19(b) demonstrates that the ZVS inverter technique effectively mitigates the overvoltage problem. This is attributed to the joint application of a longer rise time and the profiling of dv/dt. The effect of the profiling on the motor voltage can be more clearly observed in Figure 6.19(c),(d), which show an extended view of the motor voltage waveform. It is apparent that the motor voltage closely conforms to the results presented in Figure 6.6. Specifically, the natural rise commutation, set at $8t_p$, leads to three intersections between $V_{m,ab}$ and $V_{i,ab}$. On the other hand, the resonant fall commutation, configured as $4t_p$, results in a single intersection between $V_{m,ab}$ and $V_{i,ab}$, as depicted in Figure 6.6(c). To note, the time difference between $V_{m,ab}$ and $V_{i,ab}$ at each switching transition is the time for the inverter voltage to reach the motor-side also known as the propagation time t_p. This is measured as 87 ns, which agrees with the calculated t_p of a 20 m cable as 86.7 ns.



(a)

(b)

(c)

(d)

Figure 6.19: DM motor-side voltage $V_{m,ab}$ and inverter-side voltage $V_{i,ab}$ with a cable length of 20 m. (a) Hard-switching two-level inverter. (b) ZVS Inverter. (c) Extended view of ZVS inverter showing natural rise ($8t_p$). (d) Extended view of ZVS inverter showing resonant fall ($4t_p$).

Actively Profiling One Type of Commutation

As briefly discussed in Section 6.2.3, the existing literature on ZVS has established that it is possible to regulate the $\mathrm{d}v/\mathrm{d}t$ during switching transitions, enabling the active profiling of a specific type of commutation. However, actively profiling one type of commutation does not guarantee active profiling of other types of commutation. This issue is exemplified in Figure 6.20, which demonstrates that while rising resonant commutations have been actively profiled to $8t_p$, falling resonant commutations have not been actively profiled to $4t_p$, resulting in a motor overvoltage of 2 p.u. Although the ZVS inverter has led to lower losses and the mitigation of one type of commutation, it can still cause long-term damage to the motor windings. The proposed motor overvoltage mitigation approach alleviates this problem, as it actively profiles all three types of commutation simultaneously.

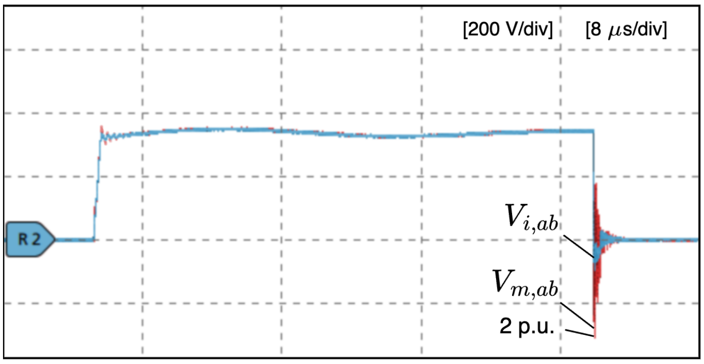


Figure 6.20: Motor voltage $V_{m,ab}$ when only resonant rise commutation is actively profiled using 20 m cable.

Variations in Load Conditions

It is essential to account for the impact of motor overvoltage and its effects on rise and fall times in a typical motor drive system, particularly when operating conditions deviate from rated power. These deviations can alter the maximum phase current, leading to changes in rise and fall times, as shown in (6.2) and (6.5). Figure 6.21 presents the impact of motor overvoltage for a 20 m cable in comparison to instances of power deviation from the rated power of 1.23 kW.

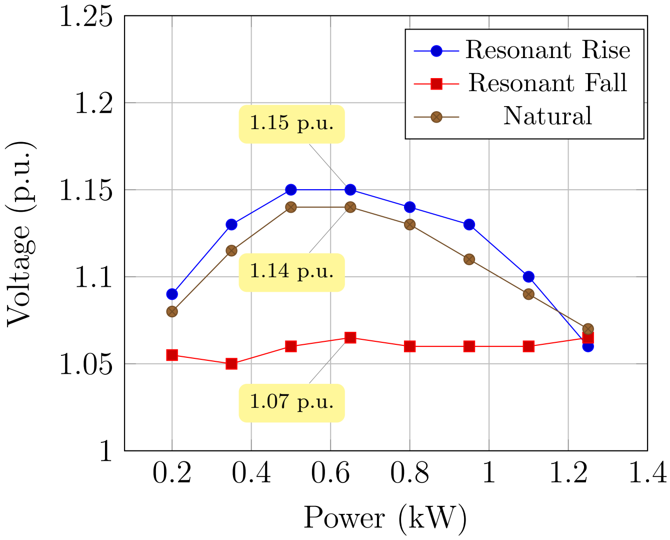


Figure 6.21: Experimental motor overvoltage for the different types of commutations when output power deviates from rated power. (Cable length = 20 m.)

According to the results, deviations from the optimal rise times can marginally increase the motor voltage, especially at 0.6 kW output power compared to 0.2 kW. This is due to the fact that as the power deviates from the rated power, the rise times will increase and in this scenario, they become longer than $8t_p$. When the power output is around 0.6 kW, the dv/dt is no longer actively profiled, leading to an increase in motor voltage. However, at 0.2 kW, the rise times approach $12t_p$, and they are actively profiled according to (6.7). Since a longer rise time always leads to a lower motor overvoltage, the maximum overvoltage is limited to 1.15 p.u. On the other hand, changes in loading conditions have a minor impact on falling resonant commutations, as evidenced by (6.1). Nevertheless, variations in load conditions have a minimum effect on overvoltage, as the presented approach ensures a maximum overvoltage of 1.15 p.u.

Zero-Voltage Switching

The waveforms of the MOSFET V_{ds} and i_d during a switching transition in Sector I-I are shown in Figure 6.22. Observing the graph, it becomes apparent that ZVS is initiated, and the main switch is activated as i_d increases, following the clamping of V_{ds} to zero. The decrease in V_{ds} occurs at a rate actively controlled by both the resonant parameters and cable propagation time. This ZVS switching inverter results in negligible turn-on losses compared to those incurred by a two-level hard-switching inverter, as demonstrated by the minimum overlap between V_{ds} and i_d.

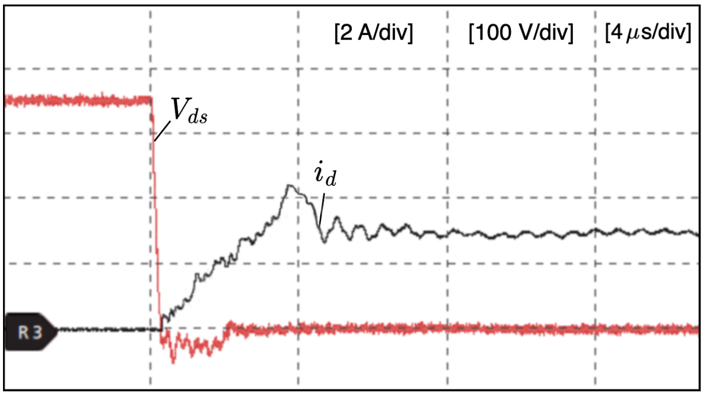


Figure 6.22: MOSFET drain-source voltage V_{ds} and drain current i_d during turn-on switching transients.

6.5 Summary

This chapter introduced a parameter selection strategy of a SiC-based ZVS inverter as a potential remedy for motor overvoltage in cable-fed drives. The proposed strategy involves regulating the $\mathrm{d}v/\mathrm{d}t$ of each resonant and natural commutation to prevent the activation of cable antiresonance and mitigate overvoltage. This method necessitates carefully selecting resonant parameters based on the length of the cable and t_p. The performance of the inverter was assessed through theoretical analysis, simulations, and experiments. The ZVS topology is compared to conventional solutions, such as the Q3L three-level converter and the two-level converter with passive RC and LCR filters. The results indicate that the ZVS inverter has advantages in terms of lower losses and volume. Furthermore, the ZVS inverter can effectively mitigate motor overvoltage, with limited impact when varying motor load conditions due to the prolonged rise/fall times.

By exploring the application of the ZVS topology in cable-fed motor drives, this chapter contributes to the existing research on motor overvoltage mitigation. The findings demonstrate the potential of the ZVS inverter as a promising solution to address motor overvoltage challenges, providing insights into its advantages over conventional solutions. The research outcomes provide valuable guidance for the design and implementation of the ZVS inverter, leading to more efficient and reliable cable-fed motor drive systems.

Chapter 7

Conclusions

The present chapter provides concluding remarks and a critical discussion of the research conducted across Chapters 4 to 6, followed by an outline of potential areas of focus for future research.

7.1 Conclusions

The integration of SiC MOSFETs into motor drives introduces distinct challenges, primarily stemming from their fast switching frequencies and the inherent high $\mathrm{d}v/\mathrm{d}t$ characteristics. This thesis advances the traditional state-of-the-art by proposing systematic and comprehensive solutions to these challenges. The introduced methodologies promote the development of highly efficient and reliable WBG-based power electronic inverters. Furthermore, they reduce the need for multiple switches and mitigate the dependency on large passive components. The principal findings related to the research objectives are summarised as follows:

Research objective 1: Investigate the correlation between switching frequency and power losses to enhance system efficiency in SiC-based motor drives.

- A modulation method based on VSF-PWM and system power losses is proposed for SiC-based motor drives, intending to optimise system efficiency. The method distinguishes itself by using a variable switching frequency, which adapts to operational conditions, rather than a fixed-frequency approach prevalent in current practices. This allows for optimisation for efficiency, reduction of EMI, and improved performance under varying load conditions.
- Through PLECS and MATLAB/Simulink loss modelling, it is shown that while increasing switching frequency can incur higher inverter losses, it concurrently

reduces motor losses by diminishing current ripple effects. This may be crucial for extending the motors operational life by reducing heat generation, EMI, and mechanical stress. It also results in smoother, quieter motor operation with better control dynamics and potential energy savings despite the higher inverter losses from increased switching frequency. Within this framework, a tradeoff can be achieved between total power losses and optimum switching frequency. Identifying this balance underpins the presented VSF-PWM methodology.

- The VSF-PWM method marks a substantial change from conventional fixed-frequency PWM strategies by introducing an offline lookup table to tailor the switching frequency for each operational condition of a SiC-based motor drive. This innovation leverages the fast switching capabilities of SiC MOSFETs, achieving both simulated and experimental improvements in system efficiency of up to 0.36% and 0.29%, respectively, when compared to CSF-PWM. By doing so, it acknowledges and utilises the potential for varied operational demands, offering a pragmatic and advanced approach to reduce overall system power losses and improve practical efficiency and effectiveness.

Research objective 2: To design a control strategy that enhances SiC-based motor drive efficiency whilst limiting peak ac current ripple.

- Whilst conventional CSF-PWM techniques are simple to implement, they produce uneven current ripple. To address this, a VSF-PWM strategy has been developed to limit peak current ripple. This strategy operates by increasing the switching frequency in areas of higher current ripple, limiting its magnitude. The choice of switching frequencies are dependant on a pre-configured offline lookup table, which determines both the base switching frequency and the ripple limit. This methodology would be of particular importance in industry's where specific standards mandate strict requirements on current ripple.

- The proposed method demonstrates a substantial advancement by not just mitigating peak current ripple but also improving system efficiency This is evidenced through simulations indicating an efficiency enhancement of up to 0.34%, while experimental validation shows an increase to 0.45%. Moreover, the distribution of current harmonics across a wider frequency spectrum plays a crucial role in mitigating component degradation and extending the drive's operational lifespan. However, without careful consideration this could potentially interfere with other systems operating within this frequency range, increasing EMI concerns.

- Previous research on VSF-PWM primarily focuses on the reduction of peak current ripple without fully considering the efficiency impacts on the inverter and motor. This research goes a step further by incorporating power loss considerations into the control strategy, thus combining with the first research objective. Therefore the proposed modulation technique not only limits current ripple to meet industry standards but does so with an optimised efficiency profile for the inverter and motor—harmonising the reduction in ripple and enhanced efficiency.

Research objective 3: To mitigate motor terminal overvoltage in cable-fed systems by dynamically shaping the $\mathrm{d}v/\mathrm{d}t$ of SiC MOSFETs.

- The aforementioned research has been devoted to improve motor drive efficiency and limit the current ripple. However, the high $\mathrm{d}v/\mathrm{d}t$ associated with SiC MOSFETs become problematic when used with long motor feeder cables, as they may instigate the RWP. It is imperative to address this issue since it culminates in motor overvoltage, which can cause PD and hasten insulation breakdown. In response to these challenges, a novel strategy involving a ZVS SiC-based inverter has been proposed to mitigate motor overvoltage in such systems.

- This method improves upon previous ZVS inverter designs that utilise a single auxiliary circuit by regulating the $\mathrm{d}v/\mathrm{d}t$ of each switching commutation. By doing so, it prevents the triggering of cable antiresonance, which is a common cause of overvoltage events. Additionally, the methodology suggests specific inductor and capacitor parameter values that are informed by the cable's length and propagation time along the cable. This provides a practical framework to optimise inverter design and improve the overall reliability of cable-fed drive systems.

- The proposed method is evaluated by comparing it with traditional solutions, including the three-level inverter and the two-level inverter, both of which are outfitted with passive RC and LCR filters. Efficiency simulations conducted in PLECS indicate that the ZVS inverter achieves a 0.6% increase in efficiency relative to the three-level inverter and as much as a 4.7% improvement when compared to the use of passive filters. Furthermore, the ZVS inverter, which is essentially a two-level inverter with an additional active switch, demonstrates a significant reduction in volume. It exhibits approximately a 30% volumetric decrease compared to the three-level inverter, and around a 40% reduction when compared to the two-level inverter equipped with LCR and RC filters. This makes the ZVS inverter not only more efficient but also more compact than its conventional counterparts.

7.2 Future Work

This thesis introduced innovative modulation and design strategies to enhance the efficiency and reliability of SiC-based motor drives. While this research successfully improved system efficiency and addressed motor overvoltages in cable-fed motor drives, many intriguing areas and prospective studies remain to maximise and promote the use of WBG devices in motor drives. Future research could center on the following aspects:

1. VSF-PWM at higher switching frequencies: Typically, VSF-PWM strategies operate at frequencies up to 20 kHz, primarily due to the diminished current and torque ripple observed beyond this frequency. As technological advancements continue, there is potential to push these boundaries. Future approaches could explore VSF-PWM at even higher switching frequencies. By doing so, not only would it align these strategies more harmoniously with WBG devices, but it might also unlock benefits in terms of efficiency, system compactness, and faster response times.

2. Mitigation of motor overvoltage using active gate drivers: Active gate drivers stand out as a promising solution in mitigating motor overvoltage. Their innate capacity to control and manage the power flowing through active switches makes them an appealing solution. However, as of now, the complexities and high costs associated with their implementation have been a barrier to their widespread adoption. While the efficacy of these drivers is undeniable, the present-day challenges in their deployment make it essential for researchers and developers to rethink their approach. Future research and development efforts could thus focus on designing less complex and more cost-effective active gate drivers with the capability to mitigate motor overvoltage. By simplifying these components, not only can the industry benefit from their mitigation capabilities, but it could also lead to a broader acceptance and integration in standard motor drive setups.

3. Evaluation of PD activity relative to insulation thickness: Exceeding the insulation's PDIV can initiate PDs, which, over time, can degrade and cause localised heating of the organic coatings on motor windings. However, to the best of the author's understanding, there is no established correlation between motor overvoltage in cable-fed systems and the requisite minimum insulation thickness needed to ensure longevity of motor windings. If a comprehensive guideline for the tradeoff between power density, PDs and insulation thickness in cable-fed sys-

tems is provided, it could potentially eliminate PD activity concerns, rendering mitigation strategies unnecessary.

4. Harmonics and resonance phenomena impact on PD activity: The operation of SiC MOSFETs at higher switching frequencies in motor drives can introduce harmonics into the system. These harmonics, especially when combined with existing system resonances, can lead to amplification effects that exacerbate motor overvoltage and consequently increase the risk of PD activity. Future research could delve into understanding these harmonic interactions in depth. The primary objective would be to characterise the nature and behaviour of harmonics generated by SiC-based motor drives and identify specific frequency ranges or resonance conditions that heighten the risk of PDs. Such insights could pave the way for improved mitigation strategies, either through tailored modulation techniques or through the design of specific filters that attenuate harmful harmonics and mitigate resonance effects.

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Appendix A

Modified Space Vector PWM Sequence of Zero-Voltage Switching Inverter

A.1 Modified SVPWM Sequence

This appendix gives a detailed overview of the modified SVPWM switching sequence required for three-phase control of the ZVS inverter in Chapter 6. The following sequence in Table A.1 is implemented in MATLAB to reduce the number of switching transitions required for ZVS by subdividing each SVPWM sector into two, as shown in Figure A.1. The MATLAB code used is shown in Section A.2.

Table A.1: SVPWM Switching Sequence

Sector	Zero vector	First vector	Second vector	Zero vector
I-I	111	100	110	111
I-II	000	110	100	000
II-I	000	110	010	000
II-II	111	010	110	111
III-I	111	010	011	111
III-II	000	011	010	000
IV-I	000	011	001	000
IV-II	111	001	011	111
V-I	111	001	101	111
V-II	000	101	001	000
VI-I	000	101	100	000
VI-II	111	100	101	111

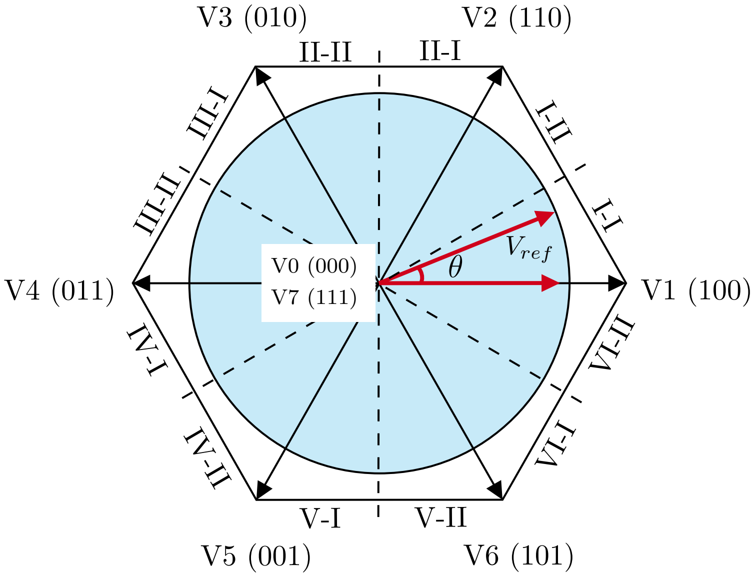


Figure A.1: SVPWM when reference voltage V_{ref} is in Sector I-I.

A.2 MATLAB Code

```
function [Mag,ang,Sec, Sec2] = fcn(u, abc)

a=abc(1);
b=abc(2);
c=abc(3);
complexo=u(2)+ i * u(3);
Mag=abs(complexo);
ang=atan2(imag(complexo),real(complexo));
alpha=ang*180/pi;

Sec = (alpha>0 & alpha≤60)*1+ (alpha>60 & alpha≤120)*2  + ...
    (alpha>120 & alpha≤180)*3 +(alpha>-180 & alpha≤-120)*4+ ...
    (alpha>-120 & alpha≤-60)*5 + (alpha>-60 & alpha≤0)*6;

Sec2 = ((alpha≥0 & alpha≤60)&(a≥0 & b≤0 & c≤0))*1 +
     ((alpha≥0 & alpha≤60)&(a≥0 & b≤0 & c≥0))*2  +
     ((alpha≥60 & alpha≤120)&(a≥0 & b≤0 & c≥0))*3 +
     ((alpha≥60 & alpha≤120)&(a≤0 & b≤0 & c≥0))*4 +
     ((alpha≥120 & alpha≤180)&(a≤0 & b≤0 & c≥0))*5 +
     ((alpha≥120 & alpha≤180)&(a≤0 & b≥0 & c≥0))*6 +
     ((alpha≥-180 & alpha≤-120)&(a≤0 & b≥0 & c≥0))*7 +
     ((alpha≥-180 & alpha≤-120)&(a≤0 & b≥0 & c≤0))*8  +
```

```
    ((alpha≥-120 & alpha≤-60)&(a≤0 & b≥0 & c≤0))*9 +
    ((alpha≥-120 & alpha≤-60)&(a≥0 & b≥0 & c≤0))*10 +
    ((alpha≥-60 & alpha≤0)&(a≥0 & b≥0 & c≤0))*11 +
    ((alpha≥-60 & alpha≤0)&(a≥0 & b≤0 & c≤0))*12;

function pwm  = fcn(Fs,Mag,ang,Sec, Sec2, Vdc,clk)

% Time synchronization with the simulink clock.
t=clk;

% General expression for the calculation of T1, T2 and T0.
T1=(sqrt(3)*(Mag/Vdc))*sin(Sec*pi/3 -ang)/Fs;
T2=(sqrt(3)*(Mag/Vdc))*sin(ang - ((Sec-1)*pi/3))/Fs;
T0= (1/Fs -T1- T2)/2;

% Change of sectors
sec_ant=mod(floor(Sec),2);
sec_ant2=mod(floor(Sec2),2);

if(sec_ant2≠1)  % detection sector exchange
 T1=(sqrt(3)*(Mag/Vdc))*sin(ang - ((Sec-1)*pi/3))/Fs;
 T2=(sqrt(3)*(Mag/Vdc))*sin(Sec*pi/3 -ang)/Fs;
end

% Time intervals
int1=T0/4;
int2=int1+T1/2;
int3=int2+T2/2;
int4=int3+T0/2;
int5=int4+T2/2;
int6=int5+T1/2;

ref= 1/Fs * rem(t,1/Fs)/(1/Fs);
timet=1+(ref≥int1)+(ref≥int2)+(ref≥int3)+(ref≥int4)+(ref≥int5)+ ...
    (ref≥int6);

%Initialize key states -> 3 rows, 7 columns and 12 vectors.
sw_array=zeros(3,7,12);




%                ----Arm A ----  ----Arm B ---- ----Arm C ----
%sector 11
```

```
sw_array(:,:,1)= [1 1 1 1 1 1 1; 1 0 1 1 1 0 1; 1 0 0 1 0 0 1];
%sector 12
sw_array(:,:,2)= [0 1 1 0 1 1 0; 0 1 0 0 0 1 0; 0 0 0 0 0 0 0];
%sector 21
sw_array(:,:,3)= [0 1 0 0 0 1 0; 0 1 1 0 1 1 0; 0 0 0 0 0 0 0];
%sector 22
sw_array(:,:,4)= [1 0 1 1 1 0 1; 1 1 1 1 1 1 1; 1 0 0 1 0 0 1];
%sector 31
sw_array(:,:,5)= [1 0 0 1 0 0 1; 1 1 1 1 1 1 1; 1 0 1 1 1 0 1];
%sector 32
sw_array(:,:,6)= [0 0 0 0 0 0 0; 0 1 1 0 1 1 0; 0 1 0 0 0 1 0];
%sector 41
sw_array(:,:,7)= [0 0 0 0 0 0 0; 0 1 0 0 0 1 0; 0 1 1 0 1 1 0];
%sector 42
sw_array(:,:,8)= [1 0 0 1 0 0 1; 1 0 1 1 1 0 1; 1 1 1 1 1 1 1];
%sector 51
sw_array(:,:,9)= [1 0 1 1 1 0 1; 1 0 0 1 0 0 1; 1 1 1 1 1 1 1];
%sector 52
sw_array(:,:,10)=[0 1 0 0 0 1 0; 0 0 0 0 0 0 0; 0 1 1 0 1 1 0];
%sector 61
sw_array(:,:,11)=[0 1 1 0 1 1 0; 0 0 0 0 0 0 0; 0 1 0 0 0 1 0];
%sector 62
sw_array(:,:,12)=[1 1 1 1 1 1 1; 1 0 0 1 0 0 1; 1 0 1 1 1 0 1];

if t≤1e-6
    Sec2=1;
end

S1=sw_array(1,timet,Sec2);
S4= ¬S1;
S3=sw_array(2,timet,Sec2);
S6= ¬S3;
S5=sw_array(3,timet,Sec2);
S2= ¬S5;
pwm= [S1 S4 S3 S6 S5 S2];

end
```

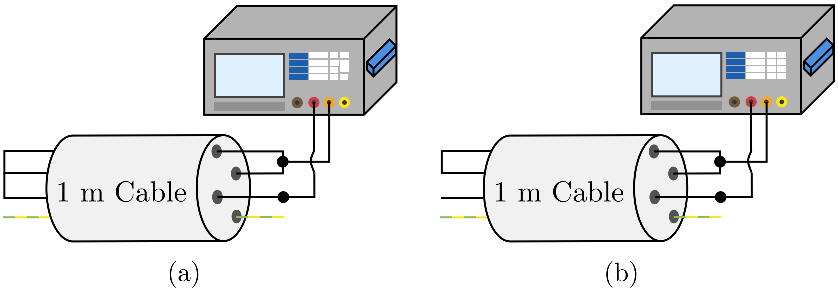
Appendix B

High-Frequency Parameter Measurements

Typically, the technical specifications and datasheets for cables and motors do not include information regarding their high-frequency parameters. However, such parameters may be obtained through the application of a high-frequency precision LCR meter during short-circuit and open-circuit measurements. This chapter shows the methodology employed to measure high-frequency parameters, which are employed for simulation as discussed in Chapter 6.

B.1 Cable Parameter Measurement

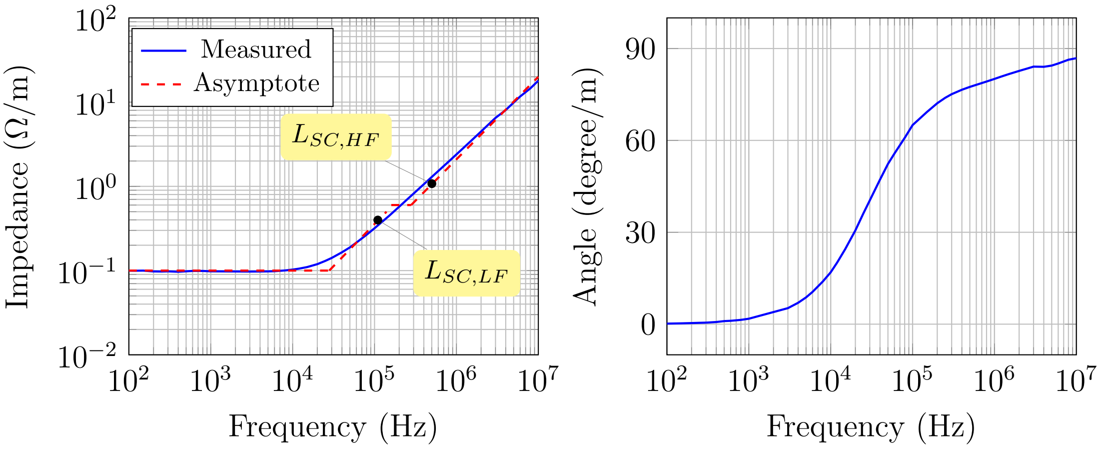
The LCR precision meter and cable configuration in short-circuit and open-circuit are shown in Figure B.1. The impedance and phase angle measurements for a 1 m cable at high frequency are shown in Figure B.2 and B.3. C_{OC} is determined at low and high frequencies from a -20 dB/decade slope of open-circuit impedance. L_{SC} is similarly determined from a 20 dB/decade slope of the short-circuit impedance.



(a)

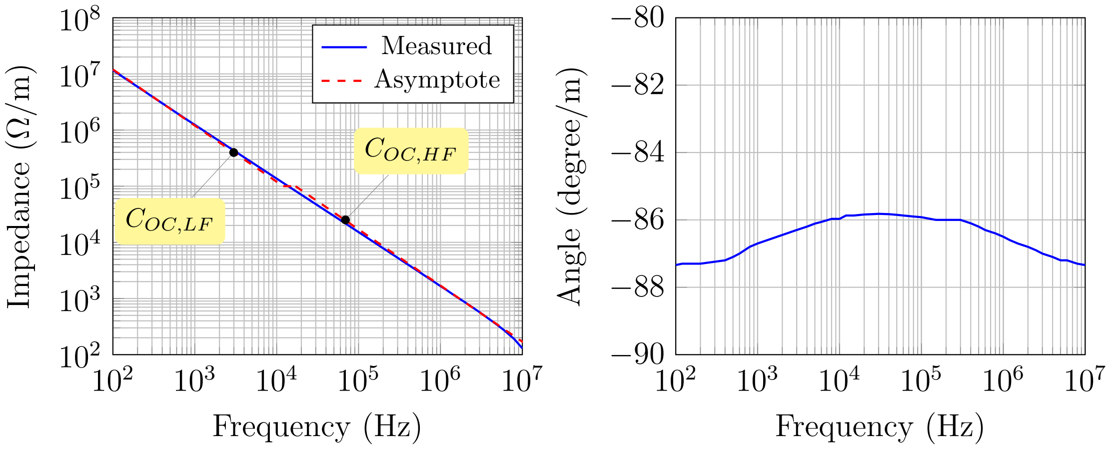
(b)

Figure B.1: Cable measurement using LCR precision meter. (a) Short-circuit. (b) Open-circuit.



(a) (b)

Figure B.2: Short-circuit cable measurement using LCR precision meter. (a) Impedance. (b) Angle.



(a) (b)

Figure B.3: Open-circuit cable measurement using LCR precision meter. (a) Impedance. (b) Angle.

B.1.1 Per Unit Cable Capacitance, Inductance and Resistance

Based off the measured plots in Figure B.2 and B.3 and using the following equations (B.1 - B.6) the high-frequency cable parameters are calculated in Table B.1.

$$L_{s1} = L_{SC-HF} \tag{B.1}$$

$$L_{s2} = L_{SC-LF} - L_{s1} \tag{B.2}$$

$$R_{s1} = |Z_{SC-LF}| \cos(\theta_{SC-LF}) \tag{B.3}$$

$$R_{s2} = |Z_{SC-HF}| \cos(\theta_{SC-HF}) - R_{S1} \tag{B.4}$$

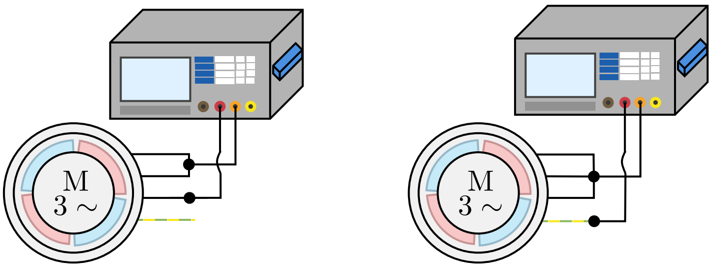
$$C_{p1} = C_{OC-HF} \tag{B.5}$$

$$C_{p2} = C_{OC-LF} - C_{p1} \tag{B.6}$$

Table B.1: Cable High-Frequency Parameters

Parameter	Value
L_{s1}	0.4057 μH
L_{s2}	0.0743 μH
R_{s1}	97.9527 mΩ
R_{s2}	148.779 mΩ
C_{p1}	98.95 pF
C_{p2}	29.95 pF

B.2 Motor Parameter Measurement



(a) (b)

Figure B.4: Motor measurement using LCR precision meter. (a) DM measurement. (b) CM measurement.

Figure B.4 depicts the DM and CM measurement method for the ac PMSM. The high-frequency cable parameters are calculated in Table B.2. The measurements received from the LCR precision meter at high-frequencies are shown in Figure B.5 and B.6.

$$C_{g1} = \frac{1}{3} C_{HF} \tag{B.7}$$

$$C_{g2} = \frac{1}{3} (C_{total} - C_{HF}) \tag{B.8}$$

$$L_{CM} = (12\pi^2 C_{g2} f_{Z1}^2)^{-1} \tag{B.9}$$

$$R_e \approx \frac{2}{3} |Z_p| \tag{B.10}$$

$$R_{g1} = \frac{2}{3} |Z_3| \tag{B.11}$$

$$L_d = L_{CM} + \frac{4}{9} L_{DM} \tag{B.12}$$

$$R_{g2} \approx \frac{1}{3} |Z_1| \tag{B.13}$$

$$C_t \approx \frac{1}{6} (C_{g1} + C_{g2}) \tag{B.14}$$

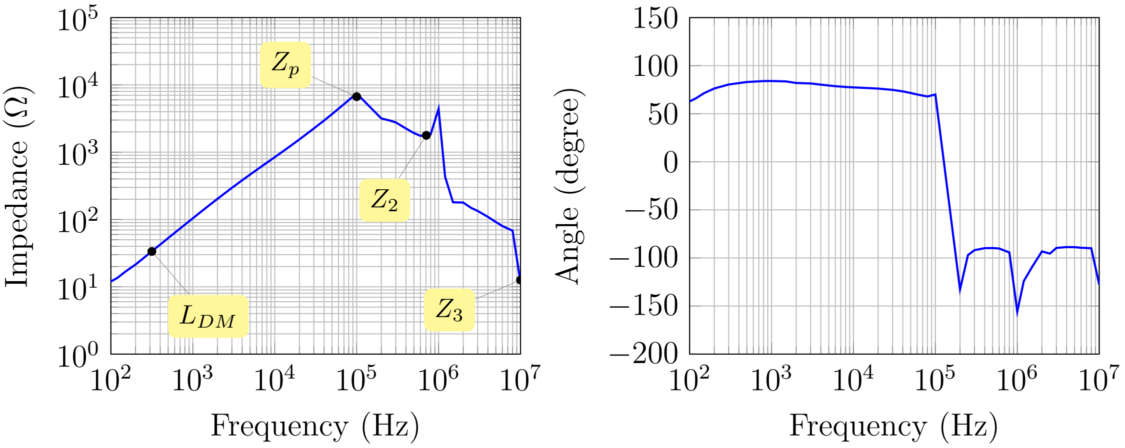
$$L_t = \frac{1}{C_t} \left(\frac{1}{2\pi f_{Z2}^2} \right)^2 \tag{B.15}$$

$$R_t = |Z_p| \cos \theta_{Z2} \tag{B.16}$$

$$L_{zu} = 3(16\pi^2 C_{g1} f_{Z3}^2)^{-1} \tag{B.17}$$

Table B.2: Motor High-Frequency Parameters

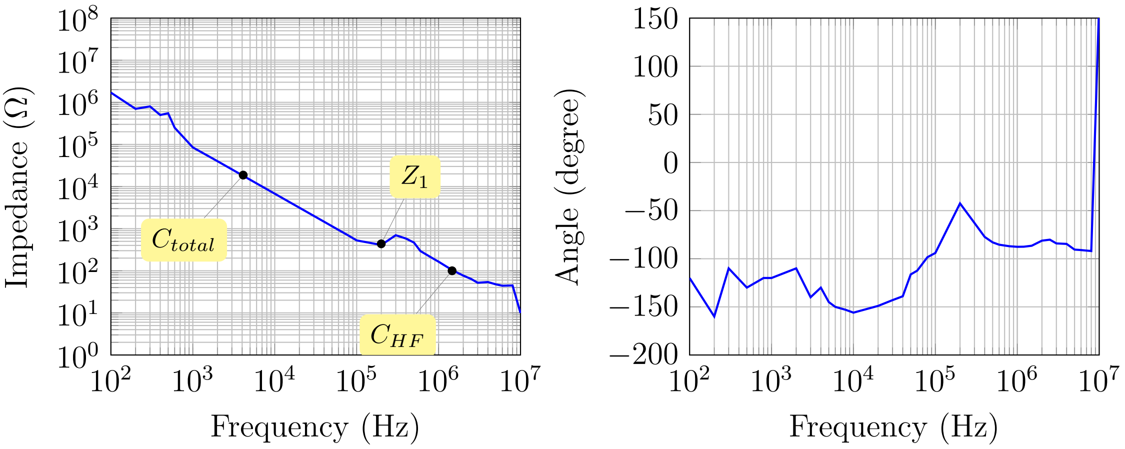
Parameter	Value	Parameter	Value
C_{g1}	353.67 pF	R_{g2}	133.33 Ω
C_{g2}	309.48 pF	C_t	110.52 pF
L_{CM}	0.68 mH	L_t	0.47 mH
R_e	4.30 kΩ	R_t	244.30 Ω
R_{g1}	9.30 Ω	L_{zu}	537.16 nH
L_d	7.76 mH		



(a)

(b)

Figure B.5: DM characteristics of motor. (a) Motor impedance. (b) Motor phase.



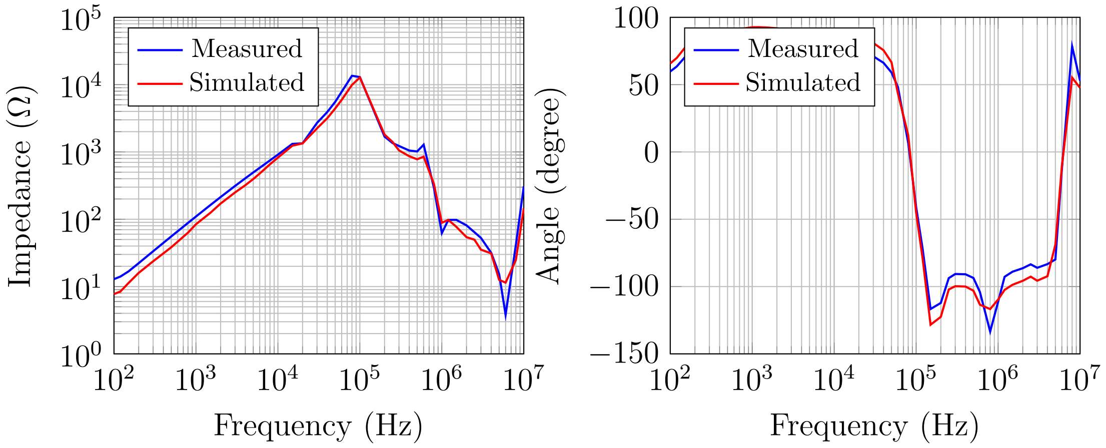
(a)

(b)

Figure B.6: CM characteristics of motor. (a) Motor impedance. (b) Motor phase.

B.3 Simulated Model of Cable and Motor

To verify the accuracy of the simulated cable and motor model with the experimental setup for high-frequency analysis, impedance and phase measurements are taken in MATLAB/Simulink. As shown in Figure B.7, the simulated model is in good agreement with the experimental setup.



(a) (b)

Figure B.7: Motor + cable measurement using LCR precision meter. (a) Measured and simulated impedance of motor + 5 m cable. (b) Measured and simulated phase of motor + 5 m cable.