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Design of an FPGA-Based High-Speed Data Acquisition System for Frequency Scanning Interferometry Long-Range Measurement

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ABSTRACT Frequency scanning interferometry (FSI) has become a popular method for long-range, target-based, distance measurements. However, the cost of developing such systems, particularly the electronic components required for high-speed data acquisition (DAQ), remains a significant concern. In this article, we present a cost-effective, FPGA-based real-time DAQ system specifically designed for FSI, with a focus on long absolute distance measurements. Our design minimizes the use of third-party intellectual property (IP) and is fully compatible with the Xilinx FPGA 7 series families. The hardware employs a 160-MS/s, 16-bit dual-channel ADC interfaced to the FPGA via a low-voltage differential signaling (LVDS). The proposed system incorporates an external sampling clock, referred to as the K-clock, which linearizes the laser's tuning rate, enabling optical measurements to be sampled at equal optical frequency intervals rather than equal time intervals. Additionally, we present the design of a high-speed, 160-MS/s ADC module for the front-end analog signal interface and the LVDS connection to the chosen FPGA. We demonstrate that the digitized data samples can be efficiently transmitted to a polarization controller (PC) application via a USB interface for further processing.

INDEX TERMS Data acquisition (DAQ), FIFO, FPGA, frequency scanning interferometry (FSI) hardware, high-speed DAQ, LIDAR.

I. INTRODUCTION

OPTICAL-BASED distance measurement systems utilizing tunable optical sources have gained popularity in recent years. Frequency scanning interferometry (FSI) also known as, frequency-modulated continuous-wave (FMCW) reflectometry, has found applications in various scientific and engineering fields [1]. FSI is primarily used in swept source optical coherence tomography (SS-OCT) for medical imaging applications [2], [3], relying on the observation of optical interference phenomena. The scope of FSI applications has expanded to large science projects, such as alignment and deformation monitoring of the CERN ATLAS detector [4], and improving manufacturing efficiency and accuracy, such as large airplane wing assembly requiring 40-μm precision [5]. Light source modulation techniques can achieve uncertainties of up to 1 part per million (PPM) [5], [6], [7], [8] over distances spanning several tens of meters [5], [9]. Certain implementations also enable simultaneous detection of multiple targets or objects, significantly advancing metrology and its applications.

If the optical path difference (OPD) between an object and sensor changes during an FSI measurement, the Doppler effect causes a magnified change in the result. The error magnitude depends on the laser tuning bandwidth. For a laser

sweeping from 1530 to 1560 nm, the magnification factor is ~50. If the OPD changes by 1 μm during a measurement, the system detects a movement of 50 μm. This effect dramatically reduces the precision of FSI measurements and presents a significant drawback for industrial use.

The Doppler effect can be minimized during an FSI measurement by generating a secondary laser sweep in the opposite direction and multiplying the two signals together [8]. Generating a secondary, opposite laser sweep perfectly synchronized with the primary sweep source using four-wave mixing (FWM) is possible. The FWM technique is an effective method for improving measurements on vibrating targets, employing dual laser sweeps in opposite directions without needing laser synchronization, and using a single primary tunable laser source (TLS) [10]. Detecting dual FSI measurements simultaneously requires two ADC channels per sensor head.

The signal quality of FSI-based measurements also depends on the tuning rate of the TLS, which should be linear during the measurement. In reality, the tuning rate of a laser is not particularly linear. Several techniques have been proposed to address laser source nonlinearity, including preprocessing to resample the measured data and eliminate sweep nonlinearity [11], [12], [13]. One common method involves using an auxiliary interferometer, which generates a sampling clock known as the K-clock [14]. Typically, a fiber-based Mach–Zehnder interferometer serves as this auxiliary interferometer [15].

These complex measurements demand high-performance real-time electronic systems. To meet these requirements, several challenges must be addressed. The signal generated by the measurement interferometer has an extremely high frequency (several hundred MHz), proportional to the target distance. To satisfy the Nyquist theorem, the sampling clock or K-clock frequency must be twice the maximum frequency of the signal detected by the measurement arm. This is typically achieved by increasing the OPD of the auxiliary interferometer, which is twice the OPD of the measurement interferometer.

The FSI system measures distance over tens of meters, and certain implementations can measure multiple objects simultaneously. High-resolution, long-distance measurements result in a large number of samples. Real-time data processing requires high-speed ADCs with high data transfer rates. Additionally, a vast number of data points must be retained onboard during the measurement for further signal processing to achieve micrometer resolution [13].

It is possible to use commercially available high-performance data acquisition (DAQ) systems; however, often, the specifications are not optimally matched for the application and can often include unwanted additional functionality not required for a particular usage. For example, a 16-GHz bandwidth high-speed oscilloscope with a sampling rate of 50 GS/s was used as DAQ hardware for optical coherence tomography (OCT) measurements [16], [17]. Adapting similar off-the-shelf components for our FSI application would result in nonoptimized sampling and equipment more suited to a laboratory than manufacturing environments. Furthermore, the cost of such systems is often prohibitive for many commercial applications.

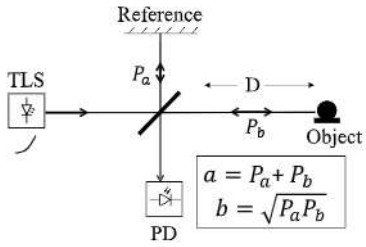

FIGURE 1. Michelson interferometry optical arrangement.

Recent advancements in electronic systems and devices have enabled the design of flexible, cost-effective, high-bandwidth, and low-noise devices. The real-time DAQ system for the long-range FSI measurement requires multichannel ADCs with an external sampling clock and is required to contain large data memory, with a high sampling rate. These requirements cannot be met using low-profile real-time systems such as embedded systems. High-performance systems, such as FPGAs, are required. FPGA-based real-time hardware acquisition systems can now be developed at a cost 10% of that of commercial models [18], [19]. Custom-designed DAQs require more effort in initial design and testing.

In this article, we describe the development of a cost-effective FPGA-based real-time DAQ hardware for FSI measurement systems. We propose the development of a 150-MS/s ADC module and an external clock driver circuit to drive the ADC sampling. Section II explains the theoretical background of FSI systems and the effect of the K-clock sampling method. Sections III and IV discuss the design and development of hardware for the ADC module and digital design for FPGA-based DAQ systems, respectively. Section V covers the experimental configuration for interfacing FSI systems with the DAQ measurement system. Finally, Sections VI and VII present the results and conclusions, along with closing remarks.

II. FSI-BASED MEASUREMENT SYSTEM

A. PRINCIPLES OF THE FREQUENCY SCANNING INTERFEROMETRY

FSI systems use a tunable light source to measure the OPD between an object and a reference path. The actual implementation varies depending on the application. The simple Michelson interferometer optical setup is shown in Fig. 1.

The FSI system utilizes the TLS, with an optical frequency that changes over the sweep period (t_p). The light from TLS is split into two beams. One is focused on the reference mirror, whereas the other is on the object at a distance D. Both reflected lights are coherently detected by the

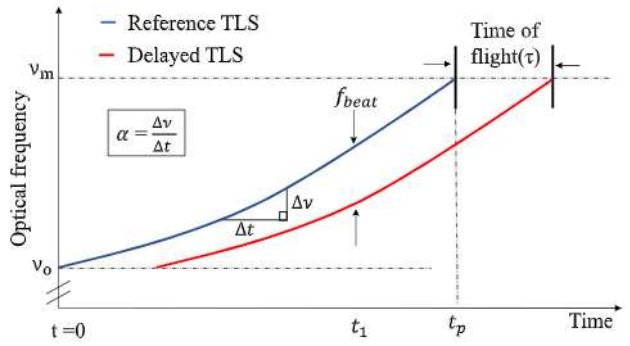

FIGURE 2. FSI measurement principle of the FSI with the reference laser beam and reflected beam.

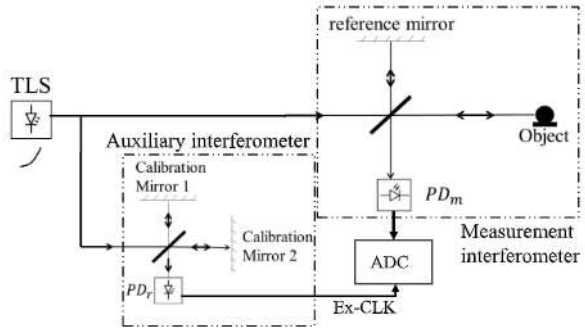

FIGURE 3. Principle of measurement setup showing passive linearization using an auxiliary interferometer.

photodetector (PD). Here, $a = P_a + P_b$ is the sum of the optical power directly from both interferometric arms, $b = \sqrt{P_a P_b}$ is the amplitude of the signal detected by the PD.

Fig. 2 illustrates the simple measurement principles using this technique. The optical frequency swept from ν_o to ν_m over a period of time t_p (blue) and the delayed optical signal which is reflected from the object (red) are shown. The delay τ between reference and delayed tunable laser signal creates an oscillating intermediate optical frequency f_{beat}. For a given rate of change in optical frequency, α (Hz/s), the signal detected by the PD creates alternating voltages as the optical frequency changes over the sweep period, causing a phase change between the reference and delayed optical signals. The voltage detected by the PD, which is sampled by the ADC at a sampling interval k can be given as

$$S(ki) = a + b\ \cos(\omega ki + \theta) \tag{1}$$

where $i = 1, 2, \ldots N$ is the ADC sample number, $\theta = 2\pi dn\nu_0/c$ is the initial phase of the optical interference signal at an optical frequency ν_0, and d is the OPD and n is the refractive index. However, it is assumed $n = 1$ throughout this article for simplicity. Here, $\omega = 2\pi f_{\text{beat}}$ is the angular frequency. The relative difference between the measurement and reference optical path delay τ is proportional to the OPD d, which is twice the distance D to the object, this is given as

$$D = \frac{\tau c}{2n} \tag{2}$$

where c is the speed of light. Here, $\alpha(r) = (\delta\nu/\delta t)$, and the intermediate beat frequency f_{beat} given as

$$f_{\text{beat}} = \alpha(t)\tau. \tag{3}$$

Further, from (2) and (3), the beat frequency can be expressed in terms of the object distance given as

$$f_{\text{beat}} = \frac{D}{c} 2\alpha(t). \tag{4}$$

Here, for a given constant $\alpha(t)$, the distance D is proportional to the f_{beat}. Hence, the direct measurement of the beat frequency reflects the absolute distance to the object. However, if α is not constant a measurement error occurs.

The discrete function of the output voltage from the PD can be obtained by substituting (4) into (1) for ω yield the object distance D given as

$$S_m(k, i) = a + b\ cos\left(4\pi \frac{D}{c}\alpha(t)ki + 4\pi \frac{D}{c}\nu_0\right). \tag{5}$$

Here, the absolute distance to the object is half the optical path distance. From (4), the object distance D corresponding to the group delay τ can be determined by obtaining the Fourier transform of the signal detected by the PD. Further, the approximate spatial resolution, ΔD, can be described as $\Delta D = (c/2n\Delta\nu)$, [12]. For example, for $\Delta\nu = 3.77074$ THz and $n = 1$, $\Delta D = 39.77\ \mu$m.

B. MEASUREMENT ERROR AND IMPLEMENTATION OF K-CLOCK

The tuning rate of the TLS influences the direct measurement of the object distance. In practice, TLSs suffer from the nonlinear effect [20], [21], reducing the measurement resolution and accuracy, and introducing a distance measurement error.

Many methods using hardware and software have been used to correct the nonlinear effects of the laser. The software approaches mostly use digital signal processing (DSP) techniques to eliminate the nonlinear components [11], [15]. This method includes using the Fourier transform to extract the phase information, which is treated as an auxiliary interferometer for post-processing. This post-processing software approach usually limits or compromises the real-time measurement capability due to the computational intensity.

The feedforward method is another common method that uses hardware resources to linearize the laser tuning rate [2], [8], [9]. The method uses the reference interferometer to actively or passively correct the variations in the tuning rate. The active linearization utilizes the feedback from the auxiliary interferometer to adjust the tuning rate error caused by the laser diode, therefore the laser diode drivers can be adjusted. However, passive linearization uses the auxiliary interferometer as a sampling clock to resample the signal detected by the PD. Such use of an auxiliary interferometer using K-Space resampling methods is shown in Fig. 3.

Here, two interferometers are used for measurement. One of the measurement arms is focused on the object and another

to the fixed reference mirror. The auxiliary interferometer contains two fixed arms of different lengths, generating a periodic fringe pattern as the laser sweeps. The oscillating fringe pattern generated by the auxiliary interferometer is used as the K-clock, which satisfies the Nyquist frequency. In this arrangement, the sampling interval (k) varies during the measurement.

C. OUTPUT OF THE MEASUREMENT INTERFEROMETER AS FUNCTION OF THE AUXILIARY INTERFEROMETER

When the passive linearization method (K-Clock) is used, the sampling interval k becomes a nonconstant value that can be expressed as a function of time. From (5), the signal detected by the PD_m can be rewritten as

$$S_m(k_a, i) = a + b\ cos\left(4\pi \frac{D_m}{c}\alpha(t)k_a(t)i + 4\pi \frac{D_m}{c}\nu_0\right) \quad (6)$$

here, D_m is the absolute distance to the object (measurement arm), $k_a(t) = (1/f_{\text{beat}(a)})$ is the sampling interval defined by the auxiliary interferometer, which can also be expressed as

$$k_a(t) = \frac{c}{D_a\alpha(t)}. \quad (7)$$

Here, D_a is the OPD created by the auxiliary interferometer. Substituting $k_a(t)$ from (7) in (6) results

$$S_m(i) = a + b\cos\left(4\pi \frac{D_m}{D_a}i\ + 4\pi \frac{D_m}{c}\nu_0\right). \quad (8)$$

Equation (8) is not only a function of sample number but also independent of the tuning rate of the TLS (α); in fact, the oscillating frequency now depends on the ratio between OPD created by the auxiliary (D_a) and measurement (D_m) interferometers. Further, the term (D_m/D_a) is constant, assuming that the measured target is kept at vibration-free during the measurement. Equation (8) also can be expressed in terms of measurement and auxiliary group delay τ_m and τ_a, respectively, as shown in

$$S_m(\tau_m, \tau_a) = a + b\cos\left(2\pi \frac{\tau_m}{\tau_a}i\ + 2\pi\nu_0\tau_m\right). \quad (9)$$

From (9), we could find that the signal detected by the measurement interferometer is not affected by the variation in α but by the time delay created by the auxiliary and measurement interferometers. To satisfy the sampling theorem

$$d_a \geq 2d_m. \quad (10)$$

Here, d_a and d_m are OPD created by the auxiliary and measurement interferometers, respectively. However, $d_m = 2D_m$, this results

$$d_a \geq 4D_m. \quad (11)$$

Therefore, the auxiliary interferometer OPD, d_a must be four times the maximum FSI absolute target distance, D_m.

III. DESIGN OF ANALOG-TO-DIGITAL CONVERTER MODULE

We have demonstrated the need for a custom DAQ system for the FSI system. The requirements are dual ADCs per sensor, an external time variable clock (external sampling clock), ADC acceptance of laser trigger signals, and real-time data processing capability using FPGA or similar high-performance hardware systems.

High-performance hardware systems, such as FPGAs, are typically used to achieve real-time measurements. However, achieving optimal performance, such as high-resolution and long-distance measurements (tens of meters), necessitates the collection of a larger number of samples. DSP techniques, like fast Fourier transform (FFT), are used to compute spectral information to determine the distance to multiple objects. Moreover, using FWM to minimize the Doppler effect has garnered increased interest in real-time signal processing [22]. This process is computationally intensive and must be executed in real time. It requires a dual-channel ADC with a common external sampling clock (K-clock). Furthermore, most TLSs provide feedback about their current operations, such as valid and nonvalid tuning information, referred to as "Trigger."

To address these complex demands, commercially available hardware systems are often expensive or require significant modifications to accommodate FSI-based measurement requirements. This renders such systems less appealing and affordable for commercial applications.

A. CUSTOM-DESIGNED ADC MODULE

Fig. 4 presents the block diagram of the custom-designed ADC module for FSI measurement. This 16-bit, dual-channel, 160-MS/s ADC is designed to operate with an input voltage range of ±2.4 V and an external sampling clock. A low-power 32-bit microcontroller (MCU) is integrated into the circuit, making the ADC highly configurable for various operations during and after DAQ development. These operations include selecting the ADC input voltage range, adjusting the ADC's internal operating clock, and optimizing the module for various power modes, such as sleep and power-down. Fig. 5 displays the custom-designed four-layer PCB containing populated components for the ADC modules. SMA connectors are chosen to interface high-frequency external signals.

ADC (ADC16DV160): The ADC16DV160, a 68-pin VQFN package 16-bit CMOS ADC with a maximum sampling rate of 160 MS/s, is used for the design. A significant feature of this device is its configurability via a 3-wire serial bus interface (SPI). The dual input channel with an external sampling clock feature has a data interface between an external device, such as an FPGA, via dual data rate (DDR) low-voltage differential signaling (LVDS) output. The input channels are protected against overvoltage beyond ±2.6 V and can achieve more than 75-dB SNR. The 8-bit differential data output can capture odd and even bits at the

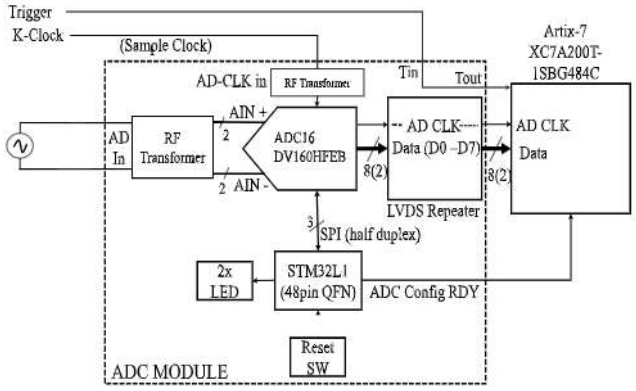

FIGURE 4. Block diagram of the customized ADC module and its interface to Artix-7 FPGA.

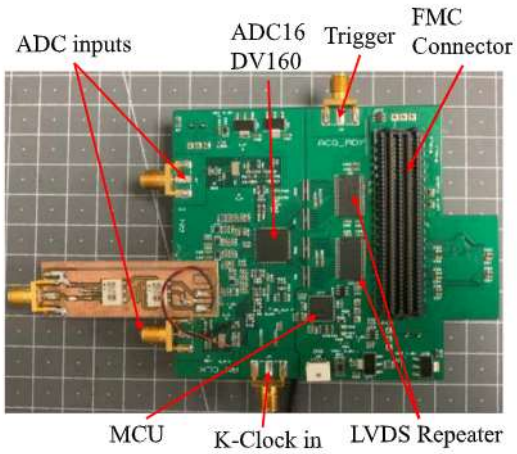

FIGURE 5. Custom-designed four-layer PCB with the fully populated components and connectors for the ADC modules.

falling and rising edges of the respective output clock before decomposing the bits to form 16-bit data per channel.

LVDS Repeater and the Trigger: LVDS is a general-purpose interface standard for efficient high-speed signal transmission. Sixteen differential data lines (eight differential repeaters per data channel) and a clock are buffered through the LVDS repeater. The repeater's input terminals are terminated with external 100-Ω resistors, while the output differential terminals are expected to be terminated with internal 100-Ω resistors as part of the FPGA buffer resources for improved signal conditioning and power consumption. The repeater is externally powered by 3.3 V for a typical differential output swing of 330 mV.

Microcontroller (MCU): It is essential to develop an embedded system to configure the ADC for its precise operation. The ARM Cortex M3-based stm32L1 ultralow power 32-bit MCU was selected to configure the ADC. The firmware was developed to self-contain configuration parameters. The MCU was designed to interface with two LEDs, a reset switch, and a 3-wire SPI interfaced to ADC. The developed firmware configures the ADC's internal registers, such as operating modes, data format, input voltage range, sampling clock, and output clock phase. The custom-developed firmware also supports the calibration and diagnoses for the ADC. A single MCU port pin is also interfaced with the FPGA, called "ADC Config RDY," for the power-on reset handshake mechanism.

FPGA: The Artix-7 family XC7A200T-1SBG484C FPGA was selected for the DAQ design. This high-performance FPGA has 33k logic slices and 1.625 MB of block RAM (BRAM). The device includes a 3.75-Gb/s transceiver module that can potentially develop a PCIe interface for extended applications. To minimize the effort in developing complex PCB design, the Nexys Video from Digilent was selected for initial application development. The Nexys development board features a USB to UART bridge and 160-pin FMC connector for external interfacing. FMC connectors are interfaced with the ADC module via the FPGA IOs. The UART interface within the Nexys video is used to stream data from the DAQ system for further processing and digital design validation.

RF Transformer: Three ADT1-1WT+ RF transformers are interfaced with two ADC input channels and the K-clock interfaces. They provide excellent amplitude and phase unbalance of 0.1 dB and 1°, respectively. Eliminating dc from the input signal is essential for both the ADC input signal and the input to the K-clock; this also ensures that the sampling clock is triggered at the zero crossing to maintain consistent sampling. The operating frequency range for the RF transformer is between 0.4 and 800 MHz, which is well within the external input signal bandwidth requirement.

IV. DEVELOPMENT OF A DIGITAL HARDWARE SYSTEM FOR DAQ

A. DIGITAL HARDWARE DESIGN

Fig. 6 shows the block diagram of the designed and developed DAQ hardware for Artix7 FPGA. The modules shown in the block diagram have been designed and developed using the Xilinx Vivado IDE with VHDL. The design aims to limit the use of intellectual property (IP) to increase portability and design reuse. A finite state machine (FSM) has been designed and interfaced with each module to ensure smooth data flow control. Fig. 7 shows the ADC module interfaced with the Nexys video FPGA trainer board showing the external connections to the FSI system.

DDR Interface and Data Decoding Using Sampling Clock: The asynchronous signals, such as Data and clock (K-clock), from the ADC must be synchronized with the FPGA clock domain. This is a significant step to avoid timing violations such as metastability. Further, the parallel input data (8 bits) is sampled at both edges of the ADC clock for odd and even bits. Fig. 8 explains such timing behavior to sample the ADC data.

The 8-bit data is sampled at the rising and falling edge of the AD CLK for odd (D0) and even (D15) bits, respectively. The clock and data signal integrity are ensured by not violating the setup (t_{su}) and hold (t_h) times for the input

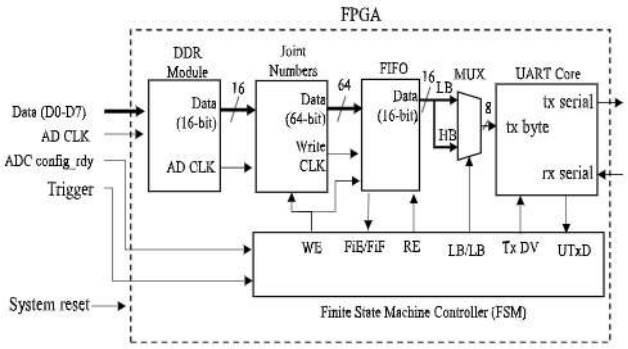

FIGURE 6. Block diagram shows the hardware architecture of the DAQ system.

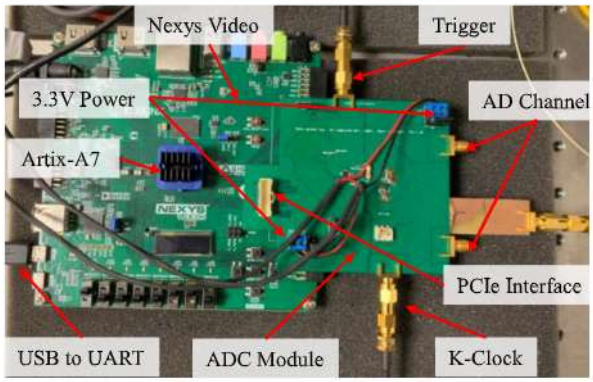

FIGURE 7. ADC module interfaced with the Nexys Video FPGA trainer board.

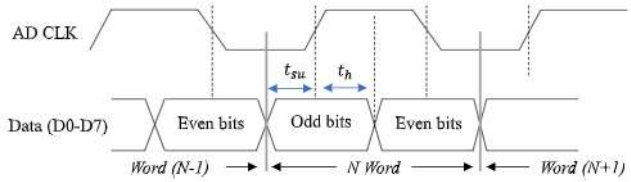

FIGURE 8. ADC output timing diagram shows 8-bit LVDS data and the clock (AD CLK).

constraint, while the FPGA differential input buffer samples the signal. This is achieved by configuring the ADC's internal synchronization mode register via SPI by adjusting the phase of the output clock during the initial power-up sequence.

Simple differential signaling input buffers "IBUFDS" and "IBUFGDS" are used for both Data and AD CLK inputs, respectively. The input termination for the buffers is configured for LVDS termination with 2.5 V, improving signal integrity and reducing the use of external components such as a 100-Ω termination resistor at the receiver end. The Fig. 9 shows the register transfer level (RTL) arrangement of a DDR interface. The two flip-flops (FFs) FF1 and FF2 sample the 8-bit data at the clock's falling and rising edges, respectively. The data from FF1 and FF2 are concatenated and captured by FF3 at the falling edge of the clock. This arrangement ensures that the 16-bit data from FF3 is validated at the rising edge of the AD CLK.

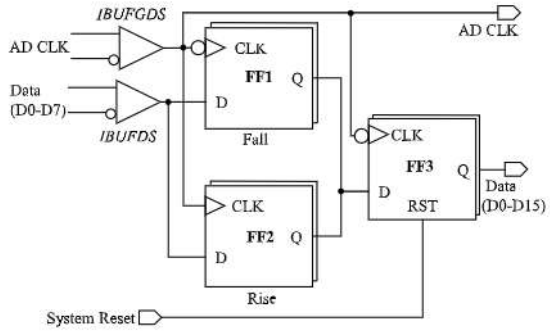

FIGURE 9. RTL arrangement of the DDR interface for capturing data at the rising and falling edge of the ADC sampling clock.

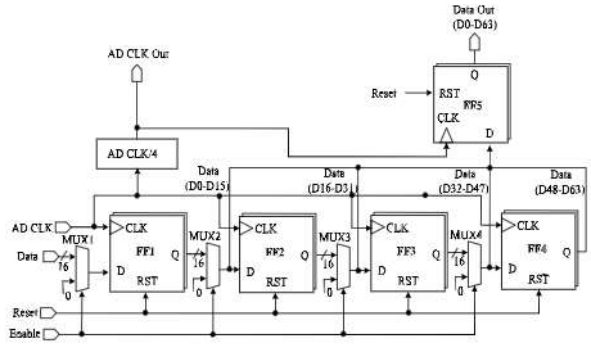

FIGURE 10. RTL arrangement for the joint number block to increase the word size to 64 bit.

Increase FIFO Data Depth: Crossing the clock domain is particularly challenging and could result in metastability if care is not taken. The BRAM-based FIFO has been selected to cross the clock domains and to buffer the data received from the DDR block. This is the only module that utilizes the IP to generate an independent clock FIFO with eight synchronization stages, especially when sampling and the onboard system clocks lie in different clock domains. The eight-stage synchronizer ensures a high mean time between failures (MTBF) when the clock domains are crossed. However, the Xilinx IP is limited to generating the maximum write FIFO depth of 131 072. This limits the number of 16-bit data that could be written into the FIFO regardless of the BRAM capacity. To overcome the limitation to increase the data depth, the write word length has increased from 16 to 64 bit for 131 072 data depth. This increases the total 16-bit data depth to 524 288, sufficient for the application's buffer requirement without configuring external RAM. The "joint numbers" block combines four 16-bit data to form a 64-bit word before it is written into the FIFO. Below, Fig. 10 shows the RTL schematic for such Joint Numbers block.

The FF1–FF4 are daisy-chained to sample the 16-bit serial data at the rising edge of the AD CLK. The four FF's outputs are combined to form the 64-bit word. The FF5 then samples the concatenated words. The AD CLK is reduced by the factor of 4, and used to samples the data by FF5 at the rising edge. Further, the divided clock is used as the FIFO

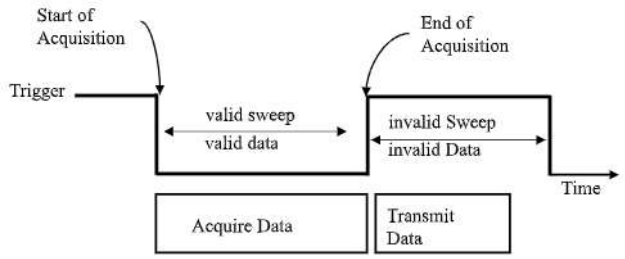

FIGURE 11. Timing sequence of DAQ process with respect to the trigger signal from the TLS.

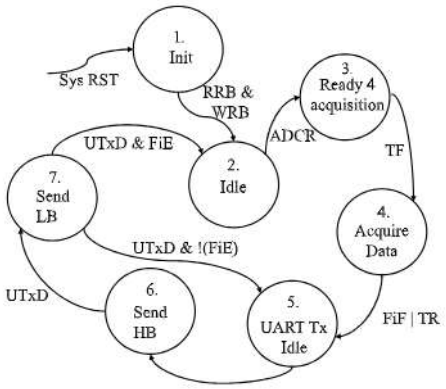

FIGURE 12. FSM state transition diagram for the DAQ sequence.

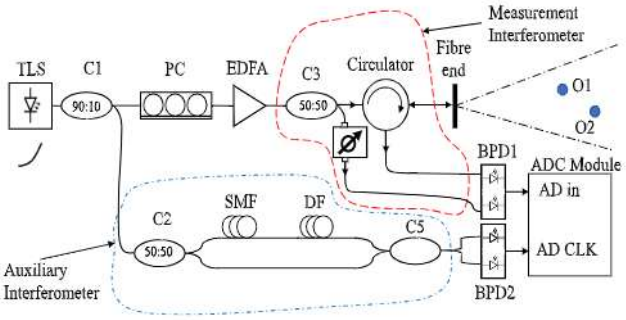

FIGURE 13. Arrangement of a fiber-based optical system for FSI measurement.

write clock (Write CLK). The Multiplexers MUX1–MUX4 are used to clear the FF(s) during the acquisition process at the start of each new measurement. Moreover, the FIFO is controlled by the FSM using four control I/Os named FIFO empty (FiE), FIFO full (FiF), read enable (RE), and write enable (WE).

Data Transmissions Over UART: As shown in Fig. 6, the UART module contains two control signals: 1) transmit data valid (TxDV) and 2) transmit done (UTxD). Further, the module is preconfigured at a baud rate of 460 800. The FSM controls these handshaking signals. Further, the UART reads 16-bit data from the FIFO, which is multiplexed for lower byte (LB) and higher byte (HB) before being transmitted via serial transmission.

FSM for Controller: The sequence of module operations must be controlled via a handshaking sequence. The entire sequential process of the operations of the DAQ was simplified using an FSM. The initial sequence begins with the trigger signal from the TLS, which must be continuously monitored for valid laser sweep and, thus, valid data measurement by the FSI system. The DAQ is designed to acquire data during the valid sweep period and then transmit data via UART during the invalid sweep period. Fig. 11 illustrates its principal operation.

After the four-stage synchronizer, the FSM monitors the falling and rising edges of the trigger signal to determine the start and end of the acquisition process. Further, the state machine was designed to handle handshaking sequences to generate further control signals for the FIFO and UART modules to ensure smooth data flow.

The state diagram in Fig. 12 shows the seven state transitions for the FSM. After issuing a system reset, the Initialization state (1) waits for the read reset busy (RRB) and write reset busy signal (WRB) from the FIFO before it transitions to Idle (2). The ADC configuration ready (ADCR) signal is monitored at the Idle state, which is asserted soon after the MCU completes the ADC configuration. This is done during the initial power-up sequence. The state moves to Ready for acquisition (3) and waits to detect the falling edge from the trigger (TF) signal before moving to Acquire Data (4) state to begin the acquisition. The FIFO write enable (WR) signal is asserted to begin acquiring data from the ADC as the transition takes place from (3) to (4). Assertion of either the rising edge (TR) of the trigger signal or the FiF signal terminates the DAQ, and the state will be transitioned to UART transmit Idle (5), where the FIFO RE is asserted. After the following clock cycle, the state transitions to Send HB (6), where the TxDV is asserted while the FIFO RE is de-asserted, and the state transmits the HB via UART serial bus. State 6 monitors for the UART transmit done (UTxD) signal, which confirms the successful UART transmission, before transitioning to Send LB (7) where UTxD is monitored again before the state returns to 5. This sequence continues until the FIFO is empty before the state returns to 2.

V. FSI EXPERIMENTAL SETUP

In this article, the performance of the FSI system with the custom-developed DAQ is compared with the commercially available real-time acquisition system: a National Instruments NI5752 and FlexRIO. The optical setup for FSI system is shown in Fig. 13. The TLS with the output power of 1 mW and a tuning range of 30 nm (1530–1560 nm) was used. The tuning rate of the laser was set to 2000 nm/s throughout the experiment. The trigger signal from the TLM-8700 is interfaced with the ADC module(s) to synchronize the valid measurement cycle.

In this proposed configuration, the measurement and auxiliary interferometers receive respective power of 90% and 10% from the TLS after coupler C1. The light to the measurement interferometer is passed through the polarization controller (PC) and then via erbium-doped fiber

TABLE 1. Average cost comparison.

Compact DAQ System	Average Cost (£)	Sample rate (MS/s)	Interface	Number of ADC Channels
Custom Designed DAQ	830	160	USB	2
NI5752&FlexRIO	25,468	50	PXIe	16
XA-160M	7,700	160	PCIe	2

amplifier (EDFA) to the coupler C3. The 3-dB coupler C3 splits the light, where one end inputs to the circulator, focusing on objects O1 and O2. Another output from the C3 is fed through a variable optical attenuator. Both the circulator and the variable optical attenuator outputs are connected to the balanced photodetector1 (BPD1). The circulator acts as a sensor head that transmits and receives light to the objects (O1, O2), where O1 and O2 are retro-reflecting spheres with a refractive index of $n\sim1.955$ at a wavelength of 1550 nm. The output from the BPD1 is interfaced to one of the ADC channels. The auxiliary interferometer has been adapted to the Mach–Zehnder type with a mismatch path length of 22.44 m. The auxiliary interferometer is illuminated using the 10% optical power from C2. The single-mode fiber (SMF) is used in series with the matching dispersion compensation fiber to minimize the fiber dispersion [23]. The coupler C5 creates an interference pattern which the BPD2 detects. The signal detected by the BPD2 generates the oscillating voltage created by the interference pattern. The sinusoid signal generated by BPD2 is converted to a suitable clock signal for the external ADC clock using the clock-generating circuit discussed in [20].

VI. RESULTS AND DISCUSSION

The comparison between NI5752 and the custom-designed DAQ (C-DAQ) was performed by comparing FSI measurements taken simultaneously by both systems. Both National Instruments vertex-5-based PXIe-7966R and the Artix-7-based Nexys video FPGA development board are designed with similar digital design methods including the state machine. The total manufacturing cost of a customized ADC module is estimated to be £280, including PCB and the electronic components. The average cost comparison for such DAQ containing programable FPGA and the ADC module is listed in Table 1. The table compares the two commercially available DAQ systems. The XA-160M has been identified as a potential commercial DAQ for the FSI long-range measurement system.

The custom-designed DAQ systems utilize the USB interface, which has adapted to a virtual COM at a baud rate of 460 800, limiting the data being transferred to the host application. However, the chosen FPGA has an integrated block for the PCIe core, this feature allows the development of a PCIe endpoint application with little or no cost to the DAQ system.

The FSI results obtained by the custom-designed DAQ are shown in Fig. 14. The host application processor has been

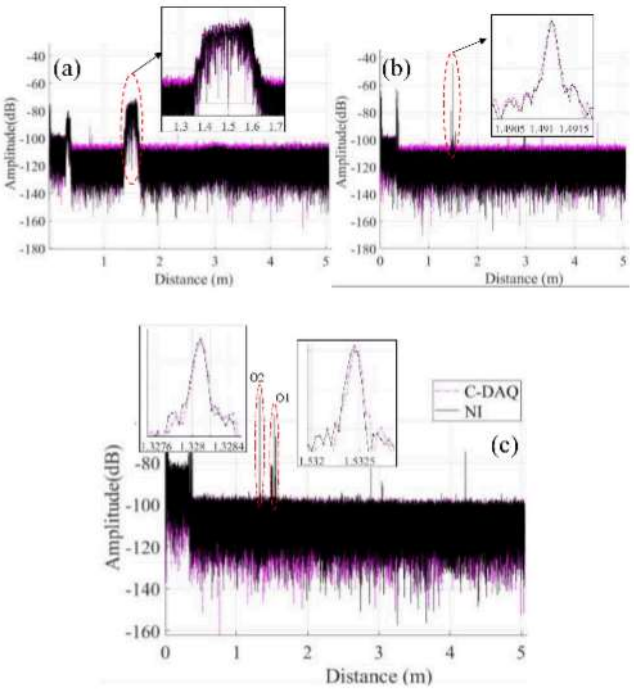

FIGURE 14. FSI measurement results comparison between C-DAQ and NI. (a) Distance measurement of a single object at a distance of 1.49115 m using a constant sampling clock. (b) Same object at a distance measured using the K-clock method. (c) Two objects O1 and O2 are simultaneously detected at a distance of 1.53244 and 1.32810 m, respectively.

used to compute the FFT. As it can be seen in Fig. 14(a), the detected peak is broadened due to the nonlinear tuning of TLS, where DAQ uses the constant sampling clock for the measurement. However, Fig. 14(b) shows the narrow peak showing the object distance with the resolution of 40 μm when it uses a K-clock for sampling. It also should be noted that the unwanted frequency components at the lower distance between 0 and 0.380257 m are also detected. The Rayleigh backscattering in the length of the fiber end and the reflections inside the circulator is responsible for the unwanted multiple peaks [24]. Since these unwanted signals are constant across the measurement and they could be easily removed using signal processing techniques. Fig. 14(c) also shows the simultaneous detection of objects O1 and O2 at distances of 1.53244 and 1.32810 m, respectively.

The SNR summary of simultaneous FSI measurement results between C-DAQ and NI FlexRIO-based DAQ is shown in Fig. 15. The NI system outperformed with SNR over C-DAQ. This is due to the nonideal configurations in the analog ground plane for ADC16DV160. The PCB can be further improved by extending the ground plane between the ADC16DV160 exposed pad and the analog ground. For a given set of laser sweep parameters, the number of samples for each scan is expected to be constant. However, variations in the number of data points between two DAQ systems were found in each of the ten samples over five corresponding object distances at 0.575736, 0.874762, 1.49091, 2.65118, and 2.90585 m. The standard deviation

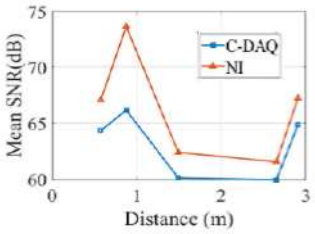

FIGURE 15. FSI SNR performance between NI and C-DAQ.

of variations in sample number for the NI Flex RIO-based systems and the C-DAQ was 6.1905 and 4.6077, respectively. This is due to the asynchronous trigger interface to both DAQ systems, where C-DAQ has four four-stage synchronizers, causing less variability of samples compared to the two-stage synchronizers NI FlexRIO-based DAQ. The results show that the C-DAQ has shown fewer sample number variations over NI FlexRIO, showing that the selection of hardware and the design method can potentially improve measurement quality as well as the cost of the systems.

VII. CONCLUSION

This study presents the design and implementation of a cost-effective dual-channel ADC module, in conjunction with an FPGA-based DAQ system, that is fully compatible with FSI measurements. It further underscores the crucial role of the external K-Sampling clock in linearizing the behavior of the TLS. The resulting systems, while being 10% the cost of comparable commercial alternatives, do not compromise on functionality. Important considerations for developing such a system to measure FSI signals using FPGA are also detailed, providing insights into key aspects of the design process. We have compared the performance of our developed FPGA-based DAQ system with the commercial NI PXIe-based FlexRIO equipped with NI5752, which shares a very similar design to our C-DAQ. Additionally, we have elaborated on the discrete mathematical model that aids in mitigating the nonlinearity behaviors of the TLS by employing the K-Clock sampling method. One limitation observed in the C-DAQ was the data transfer throughput to the host application, which is recognized as an area for improvement. The FPGA chosen for this project, integrated with a Gen 2 PCIe hard IP core, holds the potential to replace the USB with a 4-lane PCIe for improved performance for extended applications. This is a recommended upgrade for future iterations of the system.

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