Epitaxial III-V on silicon-on-insulator platforms for photonic integration

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Abstract

An epitaxially integrated laser has long been considered a holy grail of silicon photonics as it is the last piece of the fabrication process to be fully integrated on-chip. This thesis studies three different approaches to move past the physical constraints imposed by growing mismatched crystals, each with their own advantages and application potential.

The first approach uses defect filter layers and quantum dots as defect-resistant gain material to minimise the effects of threading dislocations. Using a novel InAsP/InP thick defect filter layer on silicon we achieve a threading dislocation density of $7.3 \times 10^7 \mathrm{cm}^{-2}$ using a buffer under 2 $\mu\mathrm{m}$ thick. To improve the gain and uniformity of quantum dots on InP, a desorption step is performed by stopping the arsenic flow during the growth interruption.

The second approach uses inherently threading dislocation free InGaAs nanowires on silicon to create surface emitting photonic crystal lasers. By deforming a honeycomb lattice, flat band edge emission at the Γ point is achieved with a very low threshold of 1.25 $\mu\mathrm{J}\,\mathrm{cm}^{-2}$. Curved photonic crystal cavities are also demonstrated for the first time, showing independence of bending radius due to whispering gallery modes.

The third approach, tunnel epitaxy, is used to create planar, defect-free III-V slabs on silicon and SOI. By using aspect ratio trapping and changing the growth direction from vertical to horizontal we are able to grow 3×250 $\mu\mathrm{m}$ GaAs slabs. In-plane and cross-sectional TEM and room-temperature PL analysis are used to study the defect trapping mechanism and strain relaxation.

Contents

List of Publications

- **Bogdan-Petrin Ratiu**, Balthazar Temu, Cristian Messina, Oumaima Abouzaid, Samir Rihani, Graham Berry, Sang Soon Oh, Qiang Li, *Curved InGaAs nanowire array lasers grown directly on silicon-on-insulator*, Optics Express 31, 22, 2023
- Cristian Messina, Yongkang Gong, Oumaima Abouzaid, **Bogdan-Petrin Ratiu**, Tim Grieb, Zhao Yan, Andreas Rosenauer, Sang Soon Oh, Qiang Li, *Deformed Honeycomb Lattices of InGaAs Nanowires Grown on Silicon-on-Insulator for Photonic Crystal Surface-Emitting Lasers*, Advanced Optical Materials 11, 5, 2023
- Zhao Yan, **Bogdan-Petrin Ratiu**, Weiwei Zhang, Oumaima Abouzaid, Martin Ebert, Graham T Reed, David J Thomson, Qiang Li, *Lateral tunnel epitaxy of GaAs in lithographically defined cavities on 220 nm silicon-on-insulator*, Crystal Growth & Design 23, 11, 2023
- Hui Jia, Xuezhe Yu, Taojie Zhou, Calum Dear, Jiajing Yuan, Mingchu Tang, Zhao Yan, **Bogdan-Petrin Ratiu**, Qiang Li, Alwyn Seeds, Huiyun Liu, Siming Chen, *Long-wavelength InAs/InAlGaAs quantum dot microdisk lasers on InP (001) substrate*, Applied Physics Letters 122, 11, 2023
- Richard Brown, **Bogdan-Petrin Ratiu**, Hui Jia, Khalifa M Azizur-Rahman, Manyu Dang, Mingchu Tang, Baolai Liang, Huiyun Liu, Qiang Li, *Mid-infrared InAs/InAsSb Type-II superlattices grown on silicon by MOCVD*, Journal of Crystal Growth 598, 2022

- A Enderson, P Mishra, Z Cao, FT Albeladi, S Gillgrass, **BP Ratiu**, N Peng, M Tang, HY Liu, S Shutts, PM Smowton, *Monolithic InAs QDs based Active-Passive Integration for Photonic Integrated Circuits*, IEEE Photonics Conference (IPC), 2023

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List of Acronyms

SiPh Silicon photonics

CMOS Complementary metal oxide semiconductor

SOI Silicon on insulator

CS Compound semiconductor

FCC Face centered cubic

BCC Body centered cubic

ZB Zinc blende

TD Threading dislocation

TDD Threading dislocation density

MD Misfit dislocation

PD Partial dislocation

SF Stacking fault

APB Antiphase boundary

APD Antiphase domains

MOCVD Metalorganic chemical vapour deposition

MBE Molecular beam epitaxy

CCS Close coupled showerhead

AFM Atomic force microscopy

RMS Root mean square

PL Photoluminescence

SEM Scanning electron microscopy

TEM Transmission electron microscopy

ECCI Electron channeling contrast imaging

EDX Energy Dispersive X-ray Spectroscopy

HAADF High angle annular dark field

FDTD Finite difference time domain

DFL Defect filter layer

ART Aspect ratio trappming

NW Nanowire

PhC Photonic crystal

PML Perfectly matched layer

LL Light-light

ART Aspect ratio trapping

DBR Distributed Bragg reflector

UID Unintentionally doped

Acknowledgements

The work presented in this thesis was made possible only through collaboration with many people both inside and outside our research group. As a result, the thesis contains significant contributions from others which will be acknowledged in greater detail at the end of every chapter. I would like to thank all the contributors for their invaluable time and support.

I would like to thank my supervisor, Dr. Qiang Li, for being an amazing mentor and providing the advice and resources needed to see this project to completion. I would also like to acknowledge my current and former group members for their technical support and helpful discussions. In particular I'd like to thank Dr. Oumaima Abouzaid, Dr. Pradeep Siddham, Dr. Zhao Yan, Dr. Shangfeng Liu and Dr. Parco Wong for the MOCVD growth of many of the samples presented in this thesis, along with Cristian Messina for his support with Lumerical and Legume simulations. I would also like to thank Dr. Huiyun Liu and Dr. Hui Jia, from University College London, for providing access to characterisation facilities and for providing experimental support, respectively.

Finally I would like to thank my family, friends and their pets for their invaluable love and support that helped me retain sanity during my studies.

Chapter 1

Introduction

Advancements in material science have been used to define periods within humanity's history, from the Bronze Age to the contemporary period, which some call the "silicon age" [1]. Silicon (Si) is the material of choice for micro- and nano-electronics due to its natural abundance, synergy with its natural oxide and mature manufacturing processes [2].

The semiconductor revolution has certainly shaped the world we live in, giving rise to things such as high-speed general computing [3], the internet [4], modern transportation systems [5], improved physical and medical sensing [6], and photovoltaic solar panels [7]. Many of these applications have been made possible by the miniaturization and integration of silicon devices such as transistors, photodiodes, and modulators. Decades of research have been invested in all facets of silicon manufacturing, leading to extremely efficient, low cost and high-yield processes. This has led us from the wardrobe-sized mainframes of the 50s, where each transistor was an individual device, to the current integrated circuit board computers which comfortably fit in a pocket. By integrating many different devices on a single chip, it is possible to create much smaller and efficient products.

In recent years, researchers and the industry began showing increased interest in devices that take advantage of silicon's optical properties, not just its electrical ones [8]. This field of study is called silicon photonics (SiPh) and it deals with the manipulation of light using silicon-based devices. Silicon photonics is complementary to traditional sil-

icon electronics, and shares many of its application areas. In particular, great efficiency improvements are expected in the areas of long-haul fibre optics communication and physical and biosensing [9]. One of the main promises of silicon photonics is that it will leverage the mature silicon manufacturing processes to bring higher efficiency and new functionalities to the platform. The global silicon photonics market is estimated to be worth 1.3 billion USD in 2022, and is predicted to grow to 8 billion USD by 2030 [10].

Other photonics platforms exist, each with their own advantages and disadvantages. Optical communication typically uses C- and O-band wavelengths because optical fibre has minima of absorption and dispersion at these wavelengths. Material platforms such as InP, GaAs, SOI and SiN can be used to make suitable waveguides at optical wavelengths.

Silicon photonics has the ability to manufacture many different types of high-performance devices such as high-speed optical modulators, photodetectors working from visible to mid-infrared and low loss waveguides [9]. All these devices manipulate light in various ways, by routing, modulating, diffracting or absorbing. However, none of these devices are able to generate light. The emission efficiency of silicon is very low, leading to the necessity of using other semiconductors with higher emission efficiencies. Compound semiconductors (CS) have very good emission properties and are currently the material of choice for visible and infrared wavelengths. A chart showing relevant III-V compound semiconductors is shown in Fig. 1.1.

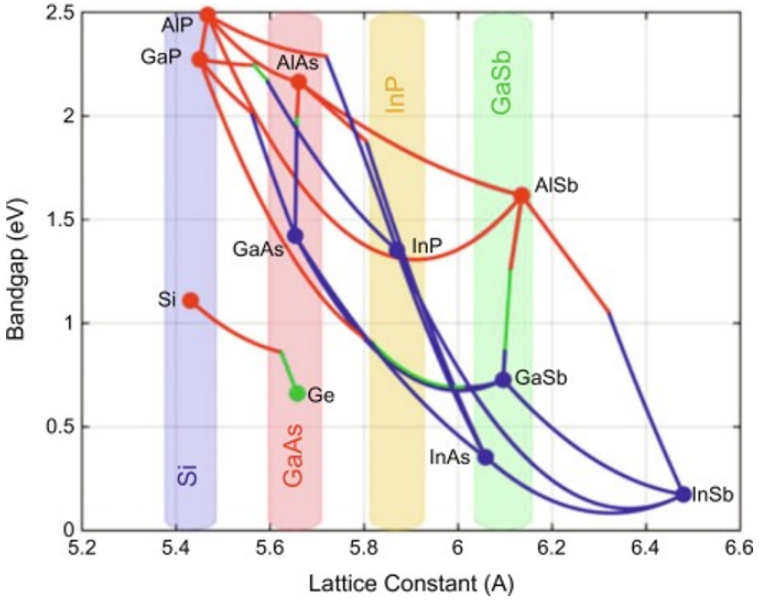

Figure 1.1: III-V semiconductors lattice constant and bandgap chart showing ternary alloys as lines between binary compounds. Blue lines indicate direct bandgaps, red and green lines indicate indirect bandgaps. Commercially available substrates are highlighted with bands showing lattice-matched areas [11].

Industrially, the integration of compound semiconductors to silicon photonics is currently done through wafer bonding [12] or transfer printing [13]. Both techniques involve glueing the compound semiconductor on top of the silicon photonics circuit. In wafer bonding, the whole wafer is bonded and then processed into devices, whereas in transfer printing the devices are manufactured first on the CS wafer and then transferred to the silicon photonics circuit. Both of these methods have major disadvantages, compound semiconductor wafers are small, brittle and expensive; there are very stringent cleanliness and positional accuracy requirements; and the contact surface tends to have high thermal and electrical resistance. These disadvantages tend to be ultimately of an economic nature, leading to lower yields and much higher costs. However, the efficiency of the resulting devices is very high, as demonstrated for example by Intel's recent product line of 100 Gb/s transceivers [14].

Like the electronics industry, the optical communications industry tends towards higher levels of integration, represented in Fig. 1.2. Every new generation provides an increase in the number of bits transmitted per second and a decrease in the power consumption per bit transmitted. Initial photonics chips used pluggable transceivers to transfer electrical to optical signals. These designs have not scaled well to the massive demands of current data centres, as the transceivers consume an increasing portion of the total energy consumption. Following generations integrated the transceiver onto the chip through an on-board optics module. More recent designs use co-packaged optics which combine the electrical and optical packages, while the laser is separate and linked through optical connections. The major advancement of the next generation is predicted to be the integration of the laser source with the optics and electronics package directly, which will further increase performance by limiting device and coupling losses.

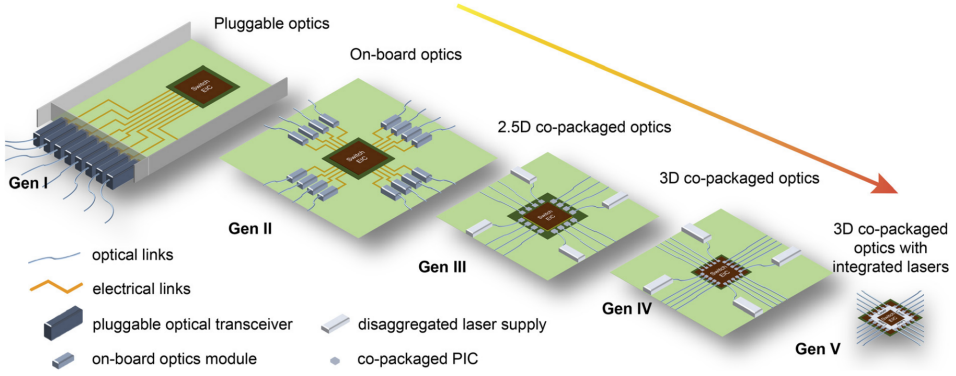

Figure 1.2: Silicon photonics integration trends for data centre applications. The trend shows the generations of products increasing the integration of optical components packaged on the same chip. The future Gen V is expected to integrate an all-optical circuit with on-chip lasers [15] .

The increased level of integration and miniaturization allows not just higher speeds, but higher density of devices on a single photonic integrated circuit. Trends for the three most common platforms are shown in Fig. 1.3. Initial photonic circuits used

direct band gap indium phosphide (InP) as a material for both active regions and passive components. InP wafers are more expensive than silicon wafers, more difficult to process, and have very high loss, causing them to fall out of favour. The silicon platform, despite not being a direct band gap semiconductor, is much cheaper and easier to process. The number of components per waveguide has rapidly increased due to the favourable properties of the platform and the high industrial demand. Both off-chip and on-chip light sources have seen similar improvements so far, but it is expected that on-chip sources will take over as we reach fifth-generation architectures.

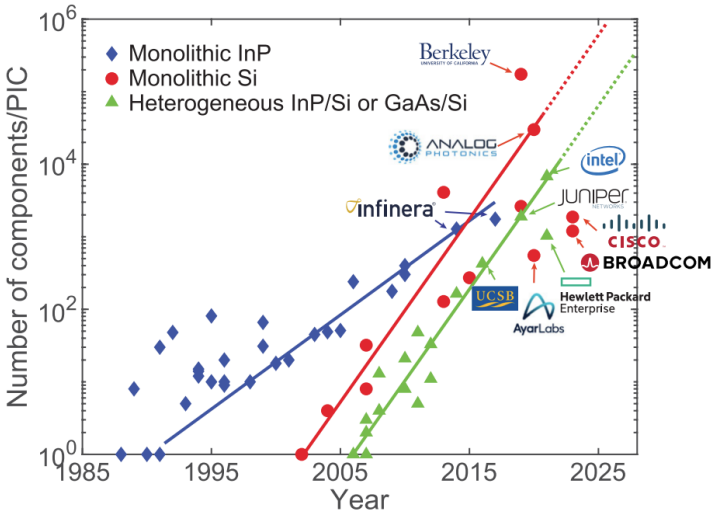

Figure 1.3: The number of components integrated on a single waveguide for different photonic integrated circuit (PIC) platforms: InP with integrated lasers, Si with off-chip lasers (monolithic) and Si with on-chip lasers (heterogeneous) [15].

Epitaxy is a manufacturing process used to deposit monocrystalline thin films, and it is widely used to grow compound semiconductors on compound semiconductor wafers (homoepitaxy). It is an essential part of the industry standard manufacturing processes as it is used to create the active region materials that are positioned on top of silicon photonics circuits using transfer printing or wafer bonding. [16] It is desirable to be able to deposit compound semiconductors directly on the silicon photonics circuit [17], thus eliminating the need for costly transfer or bonding techniques. However,

the growth of compound semiconductors directly on silicon (heteroepitaxy) yields very poor material quality, making it unsuitable for industrial uses.

The aim of this thesis is to study the heteroepitaxy in the context of integration with silicon photonics. By using non-standard growth techniques and defect-resistant materials, it is possible to achieve high quality semiconductors suitable for active photonic devices.

1.2 Review of III-V on Si integration techniques

Despite silicon's many favourable properties, it is a very poor light emitter due to its indirect bandgap. Silicon based lasers have been experimentally demonstrated [18, 19]. Direct bandgap group IV lasers have also been demonstrated [20, 21] but they suffer from low gain, only achieving electrical pumped lasing at low temperatures. Direct bandgap III-V lasers [22] offer the best lasing performance. Moreover, III-V compounds have much larger electron mobilities than silicon, which makes them desirable materials for high speed modulators [23] and high-speed, high-frequency transistors [24]. However, they are difficult to epitaxially integrate on silicon photonics platforms due to fundamental mismatches in material properties between III-V and silicon.

Current industrial integration techniques avoid direct III-V on Si epitaxy due to the resulting high defect density in the III-V epilayer. Instead, the III-V material is pre-processed and placed on the silicon photonics wafer. There are two main techniques, wafer bonding and transfer printing, schematically represented in Fig. 1.4. A summary of the advantages and disadvantages of these techniques is presented in Table 1.1.

Table 1.1: Comparison of advantages and disadvantages of the most common III-V on silicon integration techniques.

	Advantages	**Disadvantages**
Wafer bonding [12, 25]	Currently in use industrially Large choice of materials and adhesive techniques High throughput High yield	III-V and Si wafer size mismatch Adhesive lowers thermal cooling and electrical conductivity Donor wafer is wasted Only evanescent coupling possible Roughness requirements
Transfer printing [13, 26]	Currently in use industrially, but not for laser integration Can easily place different devices and materials Pre-test devices before transfer	Very high positioning requirements Low heat dissipation Low coupling efficiency
Direct epitaxy [26–28]	Cheapest and fastest manufacturing Lowest wasted III-V material Evanescent and butt coupling possible Dense integration New functionality	In research stage Material mismatch Limited thermal budget for epitaxy

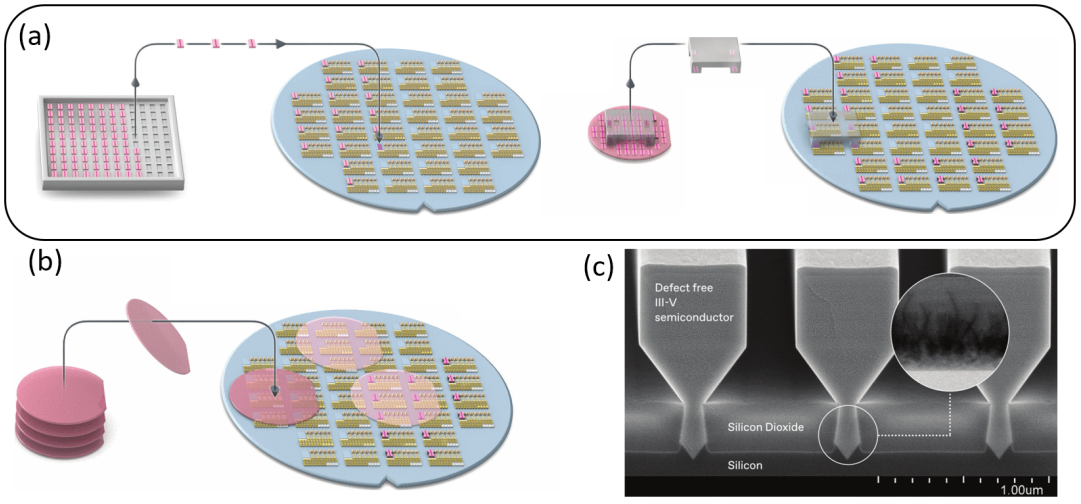

Figure 1.4: Diagrams showing the main integration techniques of III-V on Si. (a) Flip-chip and microtransfer printing. (b) Wafer bonding. (c) Epitaxial integration using nanoridges [29].

Wafer bonding. Homoepitaxy does not suffer from the material mismatch issues of heteroepitaxy and can produce very high quality III-V devices grown on lattice-matched substrates. Wafer bonding techniques place the entire III-V wafer over the SiPh wafer, where it is bound using various techniques. The active region can be

placed close to waveguides and can be coupled using evanescent coupling. The rest of the wafer can be removed through chemical mechanical polishing. This allows comparatively large, defect free III-V to be placed on the photonics wafer in parallel with high throughput.

Despite the good optical quality, the thermal and electrical properties can suffer due to the bonding interface. Direct wafer bonding uses very smooth and clean interfaces to allow van der Waals interactions and hydrogen bonds to connect the two wafers together. [30] The binding strength is lower than covalent bonds, so a high temperature annealing step is required. The high annealing temperature can damage III-V and metal contacts, however, plasma-assisted annealing can help reduce the temperature to safe levels. Another popular binding technique makes use of adhesive polymers. The smoothness and cleanliness requirements are lowered, and the annealing temperature is within the thermal budget of the wafer. Unfortunately, the polymer interface has very low electrical and thermal conductivity. Alignment can be an issue as well, as the wafer tends to slide on the adhesive before it is cured. [31]. Other techniques include surface activated bonding, thermocompression bonding, eutectic bonding, glass frit bonding and anodic bonding [12].

Recent research has demonstrated lift-off processes using remote graphene epitaxy [32] which can be used to reduce the III-V wafer waste through substrate reuse. However, most manufacturers currently simply remove the excess III-V material from the wafer without reusing it. As III-V wafers are small and expensive, this can add up to be a major financial cost.

Transfer printing. Devices grown and fabricated on native III-V substrates can achieve very high performance due to the lack of material defects. Transfer printing techniques make use of pre-fabricated devices on native substrates, which are then positioned on the silicon photonics wafer using a pick-and-place process. The devices are undercut using a wet etch so that they are only loosely bound to the III-V wafer. Using a stamp,

the devices are broken off the wafer and placed on the receiving silicon wafer. The stamp can carry thousands of devices at once, making this a reasonably high throughput process. The devices adhere to the silicon wafer using van der Waals forces. The device is coupled using evanescent coupling to the silicon photonics waveguide.

Another similar transfer method is flip-chip transfer, most popularly used for electronic devices. The process starts with fully manufactured III-V devices, which have been individually tested beforehand. Instead of using van der Vaals forces to attach the device, the device is placed on balls of solder. Because the device is suspended over the silicon, butt coupling must be used. This technique is very simple but requires very high precision and has low throughput.

Epitaxy. Monolithic epitaxial integration is the ideal technique for large-scale manufacturing. Epitaxy removes the binding and aligning requirements of other techniques while reducing the amount of wasted III-V materials. MOCVD has a high growth speed of up to microns per hour, and many wafers can be processed in parallel in large planetary reactors, leading to very high throughput. Moreover, there is more freedom in the way the III-V material is shaped and placed, with the potential of increasing efficiencies in ways not feasible using binding and transfer techniques. However, direct epitaxy is difficult due to the natural mismatch in material properties between III-V and Si, leading to high crystal defect densities.

More thorough literature reviews of the direct epitaxy methods used in this thesis will be presented at the start of their respective chapters.

1.3 Contributions

The work presented in this thesis contributes to the field of semiconductor manufacturing by investigating three different methods of integrating III-V semiconductors on silicon on inslulator wafers for silicon photonics applications through direct epitaxy.

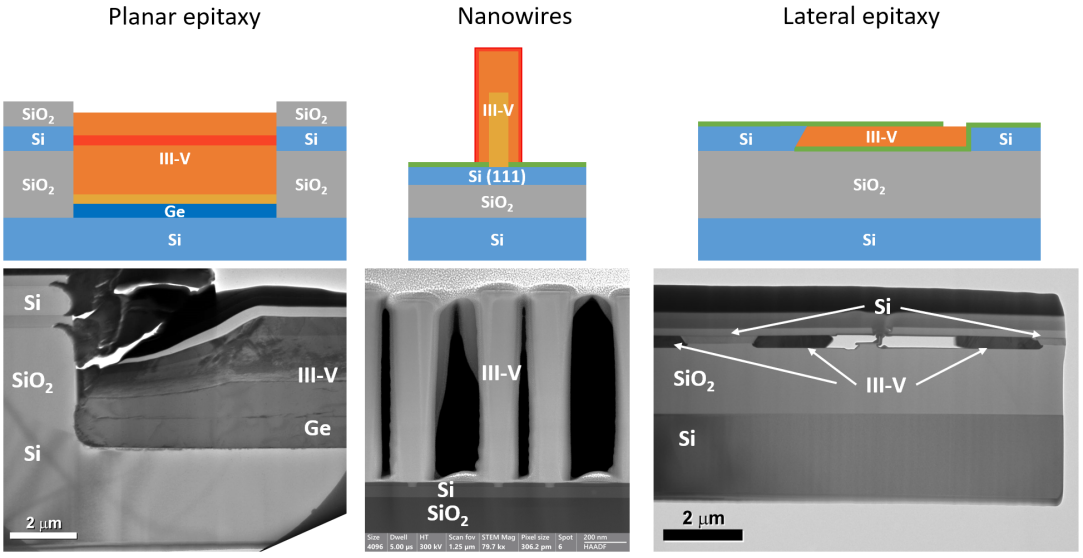

Figure 1.5: Representative diagrams of the three III-V on SOI integration methods studied in this thesis, with corresponding TEM cross sectional images.

Large area epitaxy. Defect filter layers and quantum dots have been widely researched and used in the past as methods of mitigating the effects of the defects inherent in heteroepitaxy [33, 34]. In this thesis, different defect filter layer materials and structures are studied and compared. It is found that a thick III-V-V layer is more effective at reducing the defect density compared to traditional III-III-V superlattices. The growth of 1.55 µm quantum dots is also investigated as a method to grow defect resistant gain material. InAs/InP quantum dots have inherently broad emission spectra beyond 1.5 µm. In this thesis, a new growth technique based on desorption is presented which blueshifts, narrows and brightens the emission peak.

Nanowire photonic crystals. Nanowire based photonic crystals have been proposed as a threading dislocation free solution to the problem of growing a laser on silicon [35]. This thesis presents the first realisation of a deformed honeycomb nanowire photonic crystal grown directly on silicon. Deformed lattices are a building block for topological lasers which provide significant advantages in terms immunity to manu-

facturing variations and beam quality. Additionally, the possibility of using nanowire arrays was investigated as a means to exploit whispering gallery modes to achieve densely integrated laser sources.

Lateral tunnel epitaxy. Lateral epitaxy uses aspect ratio trapping to create thin defect free layers on silicon [36]. Currently, the layer areas that can be achieved are limited to a few microns. The physical limitations of this technique are investigated. Thin, 200 μm long tunnels were used to create long III-V stripes in plane with the silicon device layer. Detailed analysis of defect trapping and propagation mechanisms was performed.

Chapter 2

Background theory and methods

2.1 Theory

This chapter introduces some background theory and notation that will be used throughout the thesis.

2.1.1 Crystal structures and defects

Basic crystal geometry. A crystal is a periodic arrangement of atoms. A crystal lattice is the grid that describes the position of the atoms in space and is defined by the unit cell. The unit cell is the smallest unit that has the full symmetry of the crystal structure. A motif is found at every lattice point. The motif can be a single atom (silicon, diamond) or an arrangement of atoms (compound semiconductors).

Miller indices are used to describe directions and planes in a crystal. For cubic crystals, we have a cubic unit cell. We define three perpendicular unit vectors h,k,l along the sides of the cube. The Miller index notation for planes and vectors inside a unit cell is shown in Table 2.1. A particular plane refers to only a single specific plane, whereas a general plane refers to all planes parallel to a particular plane in a given direction.

Table 2.1: Tabel showing the Miller index bracket notation.

Miller notation	Meaning
$[h\,k\,l]$	Particular direction
$\langle h\,k\,l\rangle$	General direction
$(h\,k\,l)$	Particular plane
$\{h\,k\,l\}$	General plane

Zinc blende crystals. Most III-As/P/Sb compound semiconductors have face-centred cubic (FCC) crystal lattices. A FCC unit cell consists of a cubic unit cell with six extra atoms added in the centres of every square side. At every lattice point, there is a motif consisting of two atoms, one group III atom at (0,0,0) and one group V atom at (¼,¼,¼) or vice versa. This can also be thought of as adding one extra atom in the centre of every tetrahedron formed by the FCC lattice atoms. This structure is called a zinc blende (ZB) crystal structure. Silicon has the same structure, but both atoms in the motif are silicon. This is called a diamond crystal structure. Diagrams of FCC crystals and their principal directions are shown in Fig. 2.1. Nitride compound semiconductors typically have a hexagonal wurtzite crystal structure, but they are less relevant to this thesis.

In a ZB crystal all [100] directions are equivalent, but [001] is typically arbitrarily chosen to be the growth direction. The silicon wafers used for silicon photonics are typically oriented with a (001) plane on the upper surface, usually denoted as (001) Si. The most closely packed plane is $\{1\,1\,1\}$, which has a hexagonal symmetry as seen in Fig. 2.1 (c). It has an ABCABC type stacking, meaning it repeats itself every three layers when seen from a parallel direction.

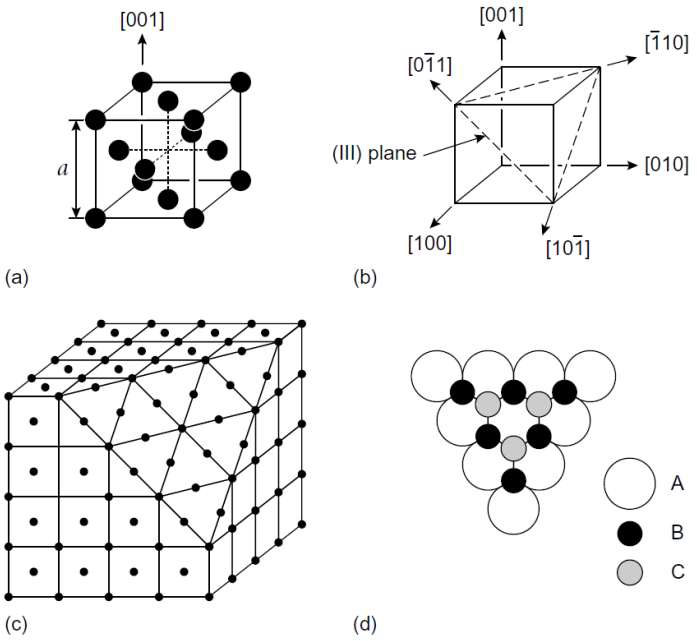

Figure 2.1: Diagrams of face-centred cubic structures. (a) FCC unit cell with lattice constant *a*. (b) High symmetry directions and planes in cubic crystals. (c) Atom arrangement in a FCC crystal showing the $\{0\,0\,1\}$ and $\{1\,1\,1\}$ planes. (d) Close packing stacking order on the $\{1\,1\,1\}$ plane showing the ABC stacking sequence [37].

Ternary compounds. Vegard's rule, Eq. 2.1, is an empiric observation which relates a ternary semiconductor's properties to the binary semiconductors that compose it. It states that the properties of a compound semiconductor, a_{AB}, is a linear combination of the properties of its constituents,a_{A} and a_{B}. Sometimes a bowing parameter, $-bx(1-x)$, is included to more accurately fit the real world scenarios where some materials are non-linear in terms of their alloy properties. It can be written as

$$a_{\mathrm{AB}} = (1-x)a_{\mathrm{A}} + xa_{\mathrm{B}} - bx(1-x) \tag{2.1}$$

where a_{AB} is the property of the ternary A_xB_{1-x}, a_{A} and a_{B} are the properties of

the two constituent binaries A and B, b is an experimentally determined bowing parameter, and x is the concentration of B in the ternary. For quaternary compounds, the same reasoning can be applied to estimate their parameters by considering them as a combination of two ternary compounds.

Crystal defects. A defect is defined as any break in the periodicity of the crystal. Defects can be separated into three categories, one dimensional (1D), two dimensional (2D) and three dimensional (3D). Defects can change the properties of the crystal and degrade device performance. Defects that carry an inherent localized charge are particularly detrimental as they can act as current leakage paths and nonradioative recombination centres. Non-charged defects can still influence the local electronic band structure, changing the optical emission properties of the material.

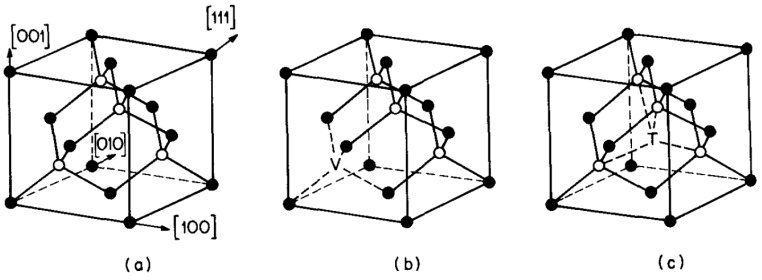

Figure 2.2: Diagram showing examples of 1D defects. (a) Zinc-blende unit cell with no defects. (b) Vacancy. (c) Interstitial defect.

One dimensional defects affect single atoms. These can be an atom missing (vacancy), an extra atom (interstitial), or a substitution. Diagrams of these defects can be seen in Fig. 2.2. Dopants can be considered to be 1D substitutional defects.

Substitution. In MOCVD growth unintentional carbon incorporation is a common defect due to the nature of the carbon-containing precursors. In III-V materials a C substitution can be either an N-type dopant if a group III atom is substituted, or a P-type dopant if a group V atom is substituted. The ratio of dopant types depends on

many factors such as growth temperature, V/III ratio, and semiconductor composition [38, 39].

Dislocations. Dislocations are charged one dimensional defects caused by crystal planes sliding over each other. They are created using the strain energy which is built up during heteroepitaxy and helps relax the crystal to its natural lattice constant. A dislocation is characterized by an additional half-plane disrupting the crystal structure. The edge of this half-plane is the dislocation line. The dislocation is defined by the dislocation line vector and the Burgers vector. The line vector describes the direction of propagation of the dislocation and lies along the dislocation line. The Burgers vector describes the displacement of atoms at the dislocation line. Dislocations are classified depending on the angle between the dislocation line vector and the Burgers vector into edge (90°), screw (0°) and 60° dislocations.

In heteroepitaxy, it is useful to divide dislocations into misfit dislocations (MD) and threading dislocations (TD). Misfit dislocations propagate in plane with the substrate (line vector $\langle 1\,\bar{1}\,0\rangle$) and are pure edge dislocations. They are the main source of strain relaxation. Threading dislocations are dislocations that have a vertical propagation component (line vector $\langle 1\,1\,1\rangle$). These dislocations typically pass through a device's active region and degrade device performance. The two types of dislocations are shown in Fig. 2.3 along with their common creation mechanisms. Threading dislocations propagating from the substrate can bend and create misfit dislocation segments propagating along the interface. The threading dislocation glides under stress, increasing the misfit segment distance to relax the crystal. Threading dislocations can also be created at the growth surface in a dislocation half loop. The half loop propagates until it hits an interface, where it splits into two threading dislocations connected by a misfit dislocation. As before, the misfit dislocation segment can elongate to relieve the stress.

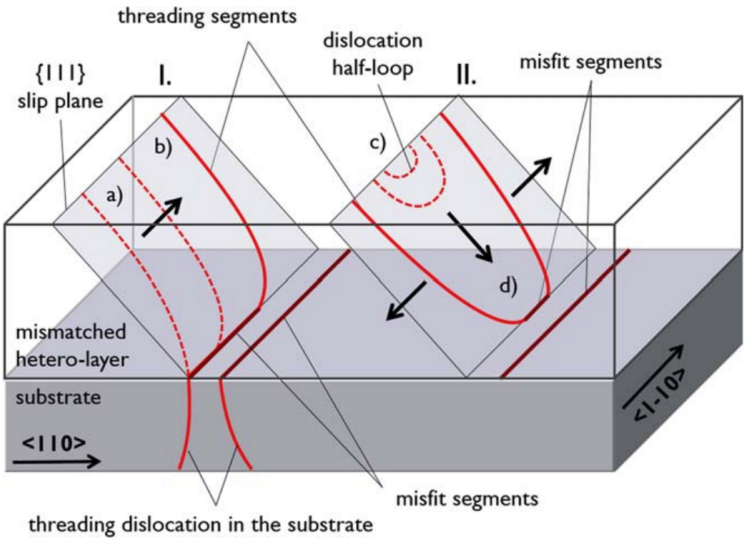

Figure 2.3: Sketch of misfit dislocation formation by threading dislocation glide (I) TDs bend over and glide along the slip planes, (a) to (b) and half-loop formation (II) half-loop nucleation at the surface and gliding down to the interface, (c) to (d) [40].

Partial dislocations (PD) are also common in FCC crystals. Partial dislocations have a Burgers vector that is not a translational lattice vector and are characterized by having a plane of stacking faults between the two paired dislocations. The two main types of partial dislocations in FCC crystals are Frank dislocations (Burgers vector $\pm a/3\langle 1\,1\,1\rangle$) or Shockley dislocations (Burgers vector $\pm a/6\langle 1\,1\,2\rangle$). Diagrams of partial dislocations can be seen in Fig. 2.4. Partial dislocations often nucleate at imperfections on the surface such as defects or particles.

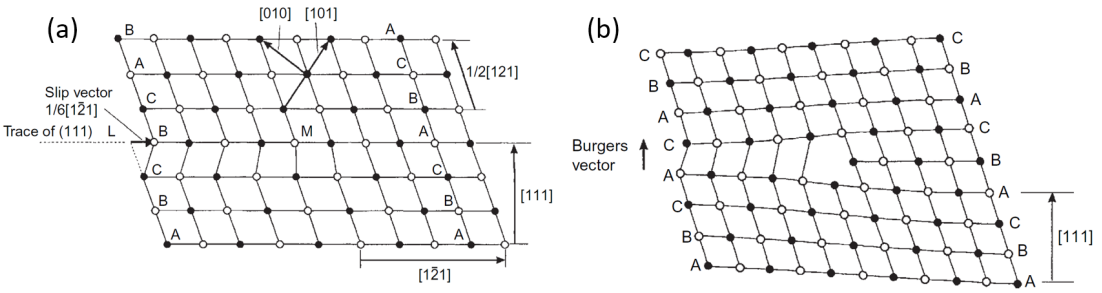

Figure 2.4: Partial dislocations and stacking faults diagram with relevant directions indicated. Filled circles represent atoms in the layers above and below unfilled circles. The close packing layers are labelled ABC, showing stacking fault disruption. (a) $1/6\ [1\,\bar{2}\,1]$ **Shockley partial dislocation due to slip along the LM line. (b)** $1/3\ [1\,1\,1]$ **Frank partial dislocation [41].**

Stacking faults. Stacking faults are planar, uncharged, two dimensional defects. They are formed by changing the close packing stacking order of $\{1\,1\,1\}$ planes. This is equivalent to adding (extrinsic SF) or removing (intrinsic SF) a $\{1\,1\,1\}$ monolayer. They can also be thought of as a monolayer thick layer of wurtzite inside a zinc-blende crystal, which is useful for understanding their electronic properties. Stacking faults are always bounded by two partial dislocations which are easily nucleated at hetero-interfaces. However since the SF is electrically uncharged and the lattice displacement is small, they are relatively less impactful than other types of defects. Diagrams of stacking faults can be seen in Fig. 2.4.

Antiphase boundaries. Antiphase boundaries (APB) are charged two dimensional defects. Antiphase boundaries separate antiphase domains (APD) which occur when the polarity of a binary semiconductor is flipped, and can propagate along $[0\,0\,1]$ or $[1\,1\,1]$ directions. They appear frequently in the growth of polar crystals on non-polar surfaces, such as in the heteroepitaxy of III-V compounds on Si.

When growing III-V on Si, the first monolayer will be formed of group V atoms.

A monoatomic step on the Si surface will cause a one-monolayer offset in the III-V material, causing a phase inversion. This is shown in Fig. 2.5. A diatomic step maintains the structure of the III-V material. Depending on the orientation of the ABP, it can self-annihilate (for $[1\,1\,1]$) or propagate upwards (for $[0\,0\,1]$). Careful preparation of the silicon surface before III-V growth is a crucial part of heteroepitaxy.

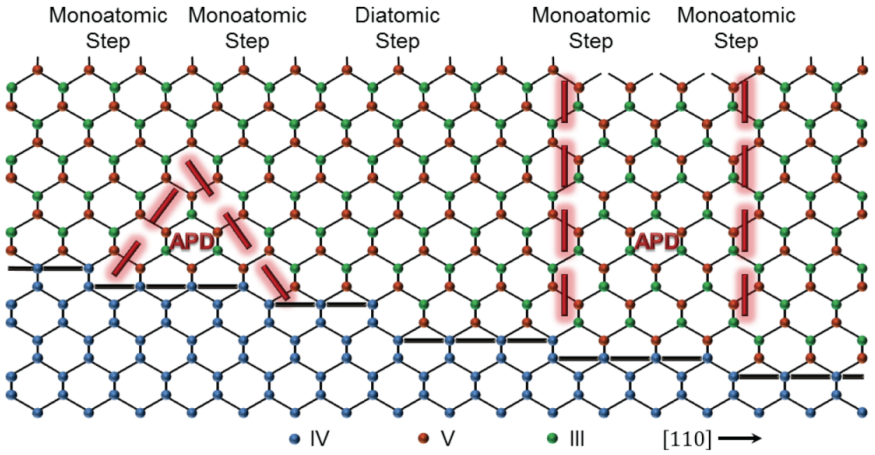

Figure 2.5: Diagram of antiphase boundaries at a III-V/Si interface showing the effect of monoatomic and diatomic steps on the Si substrate [42].

2.1.2 Electrons and photons in semiconductors

Unlike in free space, inside a crystal, an electron can only have energies allowed by the crystal's band structure. The band structure arises from the interaction of the electron with the periodic electric potential created by the atoms of the crystal. The electron energies that are not permitted inside the crystal are called the bandgap. Semiconductors have comparatively small band gaps, on the order of 1 eV. The high energy band is called the conduction band and the low energy band is the valence band.

Inside the allowed energy bands, electrons are arranged based on the density of states of the crystal. The density of states is given by the size and shape of the crystal. It arises from the electron wavefunction confinement inside the crystal. The occupation

of the available electron states is described by the Fermi level and the Fermi-Dirac distribution.

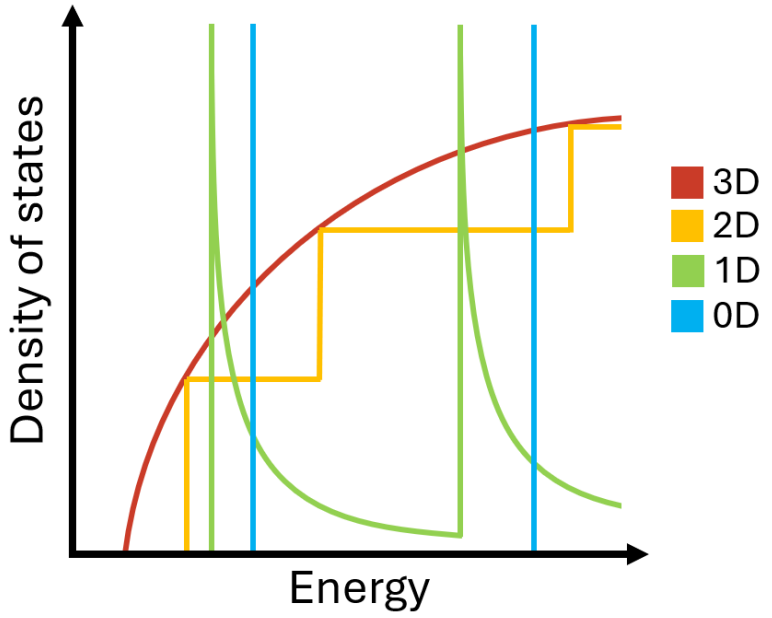

Figure 2.6: Electronic density of states for confined structures

Since the density of states is related to the size and shape of the crystal, it is possible to change it by growing confined structures. Electron confinement occurs when carriers are trapped in a low bandgap material surrounded by higher bandgap material. By confining the electrons we change the density of states of states in the material, as seen in Fig. 2.6.

2.2 Epitaxy

Metalorganic chemical vapour deposition (MOCVD) is the most popular industrial growth technique for compound semiconductors. MOCVD reactors differ from each other, but the basics are components and physical principles are the same.

MOCVD anatomy. The MOCVD reactor consists of a heated substrate inside chamber into which various gases are pumped. The two main control parameters available are gas flows and substrate temperature. Various MOCVD reactor types exist, with features such as vertical or lateral gas flow, and hot or cold walled growth chamber. For this thesis we use a vertical close-coupled showerhead reactor with a cold walled chamber.

The precursors are held in temperature controlled gas bubblers. Ultra pure hydrogen gas is used as carrier gas and flown through the bubbler to extract precursor vapour. The precursors are carried to the growth chamber. The precursors flow through separate pipes to limit any chemical reactions before reaching the reactor. For this thesis, all samples have been grown in a closed coupled showerhead (CCS) AIXTRON reactor. This type of reactor uses a showerhead structure to introduce the precursors into the growth chamber. The CCS has the III and V precursor outlets distributed uniformly across the surface to ensure uniform precursor distribution in the chamber and, therefore uniform growth across the wafer.

Inside the reactor, the wafers are positioned on a temperature controlled, rotating susceptor. The susceptor has pockets for the wafers to be placed into, in a 1x4 inch or 3x4 inch configuration. The susceptor is heated using a three-zone heater to ensure the temperature distribution across the wafer is uniform. The carrier gas, precursors and other residual compounds are evacuated from the chamber into a filtering system designed to capture dangerous compounds.

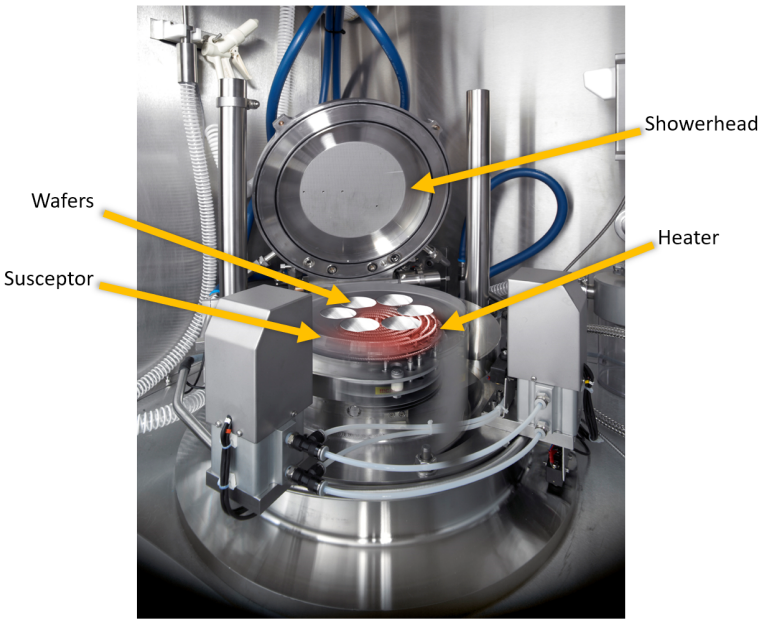

Figure 2.7: AIXTRON MOCVD reactor with its main components labelled, similar to that used for this thesis.

Precursor choices. The 'metalorganic' part of MOCVD refers to the precursor gases used. These gases are made up of specifically designed molecules that carry one metallic atom bound to organic carbon based compounds. The metal-carbon bond is not very strong and easily breaks through pyrolysis (cracking) at the high temperatures in the reactor, releasing the metallic atom to be absorbed into the crystal. Generally speaking, the longer the organic compounds, the lower the cracking temperature and the higher the carbon contamination. A list of precursors is given in Table 2.2. Other notable widely used precursors include arsine and phosphine, however they come with additional risks as they are very flammable and poisonous.

Crystal growth physics. The physics of crystal growth can be very complex and difficult to measure in an MOCVD reactor. In MOCVD the process begins when the precursor gases enter the hot reactor. Through pyrolysis one or more of the organic compounds will break apart from the molecule, leaving the metallic atom ionised.

Table 2.2: Table of precursors used in this work with their abbreviations and chemical composition.

Abbreviation	Name	Composition
TMGa	Trimethylgallium	$(CH_3)_3Ga$
TEGa	Triethylgallium	$(C_2H_5)_3Ga$
TMIn	Trimethylindium	$(CH_3)_3In$
TMAl	Trimethylaluminum	$(CH_3)_3Al$
TBAs	Tributylarsine	$(C_4H_9)_3As$
TBP	Tributylphosphine	$(C_4H_9)_3P$
TESb	Triethylantimony	$(C_2H_5)_3Sb$

Through diffusion, the molecule will reach the surface. It is likely that some organic compounds are still bound to the adatom at this point, and will likely be incorporated as carbon impurities. After the metallic atom reaches the surface, we call it an adatom. The adatom can go through diffusion on the surface or desorption from the surface. The diffusion length and desorption time are related to the adatom species, substrate and growth conditions. In standard layer-by-layer growth, the adatoms are most likely to be incorporated at the edges of layers, particularly at kinks. New layers are created when a few adatoms bind together and begin growing outwards.

Epitaxial growth modes. The chemical potential of the growth surface is given by the binding energies of the epilayer atoms and the strain energy from the lattice mismatch. The atoms of the epilayer can have different binding energies to their own species and to the substrate atoms. This means that the binding energy to the substrate atoms will have a noticeable influence on the first few monolayers grown. Assuming the epilayer is strained, this adds another component to the dependence of surface energy on thickness. If the epilayer is relaxed through misfit dislocations, these dislocations will induce a smaller strain field around them which will induce variations in the in-plane direction as well. All these effects will influence the shape in which the

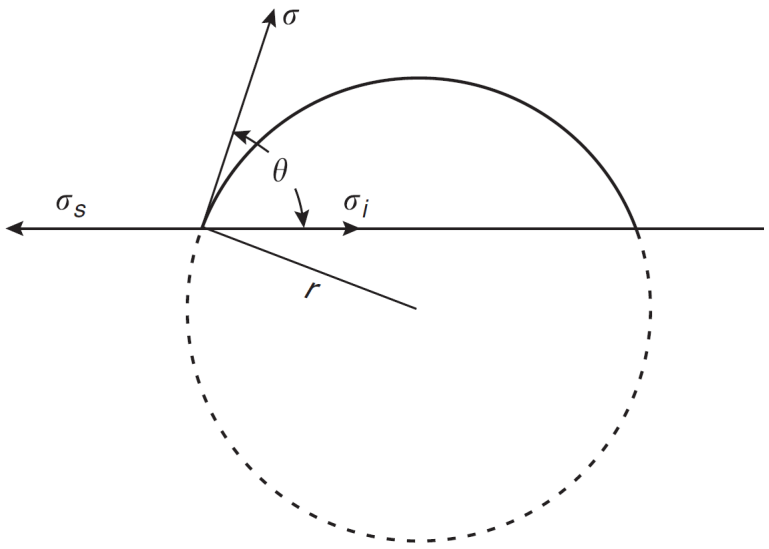

Figure 2.8: Surface energies of a nucleated crystal. The arrows represent the forces an atom experiences at the edge of the droplet due to the droplet itself, the substrate and the substrate-droplet interface, labelled as σ, σ_s and σ_i respectively [43].

crystal will grow. Such a first principle analysis can get very complex. Instead, we can gain a more intuitive understanding by comparing the situation with a physically similar one of a droplet of liquid on a surface.

A droplet will have three main free surface energies to consider: the droplet itself, the substrate and the substrate-droplet interface. All the complex physical interactions of the atoms at these interfaces will result in a droplet with a certain wetting angle, θ, the angle between the edge of the droplet and the substrate. The crystal will then reach equilibrium when:

$$\sigma_s = \sigma_i + \sigma \cos\theta \tag{2.2}$$

Taking the wetting angle to be zero corresponds to layer-by-layer growth, the Frank–van der Merwe (FM) mode. This corresponds to the case where the epilayer atoms are bound more strongly to the substrate than themselves, $\sigma_s > \sigma + \sigma_i$. The opposite

case causes 3D island growth, the Volmer–Weber (VM) mode. This corresponds to the case where epilayer atoms are more strongly bound to themselves than the substrate, $\sigma_s < \sigma + \sigma_i$. Diagrams of these modes are shown in Fig. 2.9.

The third growth mode occurs only in lattice mismatched epitaxy. The first few layers grow in the FM mode due to the large binding energy between the epilayer and substrate atoms. Assuming no dislocations are nucleated, the layer will be strained. This is called the wetting layer. As the thickness of the wetting layer increases, the influence of the substrate decreases. After a few atomic layers, the growth changes to a 3D layer growth similar to VM. The strain accumulated in the wetting layer is coherently relaxed at the lateral edges of the islands.

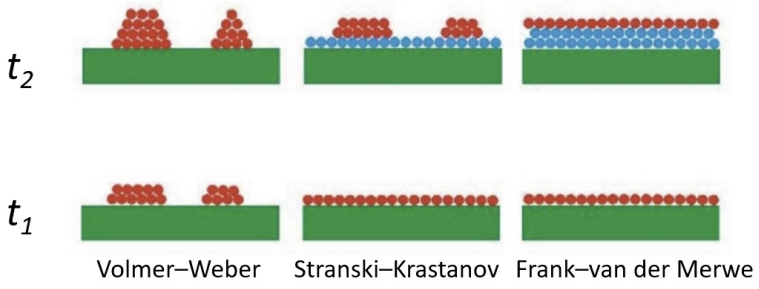

Figure 2.9: Diagram of the three heteroepitaxial growth modes progressing from time t_1 to t_2. [44] .

Critical thickness. Heteroepitaxy deals with growing layers of materials with mismatched lattice coefficients. The lattice mismatch f is defined as:

$$f = \frac{a_{sub} - a_{epi}}{a_{sub}} \tag{2.3}$$

where a_{sub} and a_{epi} are the unstrained lattice constants of the substrate and the epitaxial layer. The lattice mismatch between Si and GaAs is 4.0%, the mismatch between Si and InP is 8.1%. Such a large mismatch causes the epilayer to relax through the creation of misfit dislocations.

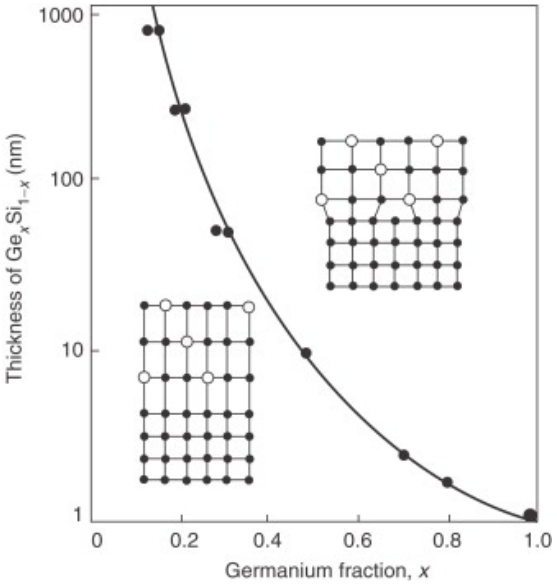

Figure 2.10: Critical thickness with the misfit f for $Si_{1-x}Ge_x$ layers on Si$(0\,0\,1)$ based on experimental measurements, where the misfit is proportional to the Ge fraction. The lattice mismatch between Si and Ge is 4%. Diagrams of strained and relaxed growth are included [51].

The layer thickness at which dislocations start to form in heteroepitaxial growth is called critical thickness. Various theoretical approaches have been used to predict the critical thickness, leading to different contradictory formulas [45–49]. A discussion of these approaches can be found in reference [50]. A commonly accepted expression of the critical thickness states:

$$h_c = \frac{b}{4\pi f(1+\nu)}\left[\ln\left(\frac{h_c}{b}\right)+1\right] \tag{2.4}$$

where h_c is the critical thickness, f is the lattice mismatch, ν is the Possion ratio of the epilayer, and b is the Burgers vector of the dislocation. An example of the critical thickness of SIGe grown on Si is plotted in Fig. 2.10, separating the pseudomorphic (strained) and metamorphic (relaxed through defect) regions. It's important to note equation 2.4 is valid only for layer-by-layer growth.

Nanowire critical thickness. Since the derivation of Equation 2.4 assumes an infinite plane of growth, it is not a good description of nanowires of finite radius. Nanowires can relax by stretching (or compressing) into the surrounding air to reach their relaxed lattice constants without the introduction of dislocations. By comparing the energy of the strained and relaxed systems, a theoretical approach can be used to predict the onset of defect formation as a function of nanowire radius and height as [52]:

$$\begin{gathered}\Delta W\left(r_0,h\right)=\frac{Er_0}{1-\nu}\left[f_\nu\left(\frac{h}{2r_0}\right)\pi r_0 h\left(\frac{\alpha^2 b_{\text{eff}}^2}{4r_0^2}-\frac{\alpha b_{\text{eff}}}{r_0}\epsilon_0\right)+C\left(1+\ln\frac{\bar{h}(r_0,h)}{b}\right)\right.\\ C=\left(1-\nu\cos^2\theta\right)b^2/[2\pi(1+\nu)]\end{gathered} \tag{2.5}$$

where $\Delta W\left(r_0,h\right)$ is excess energy of the system with dislocations and the completely coherent system, r_0 and h are the diameter and height of the nanowire, E is Young's modulus, ν is Poisson's ratio, $\alpha=4/\pi$, b_{eff} is the in-plane component of the Burgers vector, ϵ_0 is the lattice mismatch. The lateral relaxation into the surrounding air is given by f_v which can be approximated as

$$f_\nu(\rho)=1/\left(1+A_\nu\rho\right) \tag{2.6}$$

where ρ is the nanowire aspect ratio and $A_\nu=27.3\pm0.55$ is a numerically evaluated parameter, related to ν. The effective height is the distance nearest surface, $\bar{h}$ is defined as $\bar{h}=h \quad \text{if } h\leq\beta r_0, \quad \bar{h}=\beta r_0 \quad \text{if } h\geq\beta r_0.$

Equation 2.5 does not have an analytic solution and must be evaluated numerically. A plot of the critical height vs nanowire radius is shown in Fig. 2.11 (a). For large radius values, the solution approaches the standard planar critical thickness value. At a lower nanowire radius, the impact of lateral relaxation becomes dominant and acts to increase the critical height. The critical height is shown to become infinite for sufficiently thin wires, theoretically allowing for infinitely long nanowires.

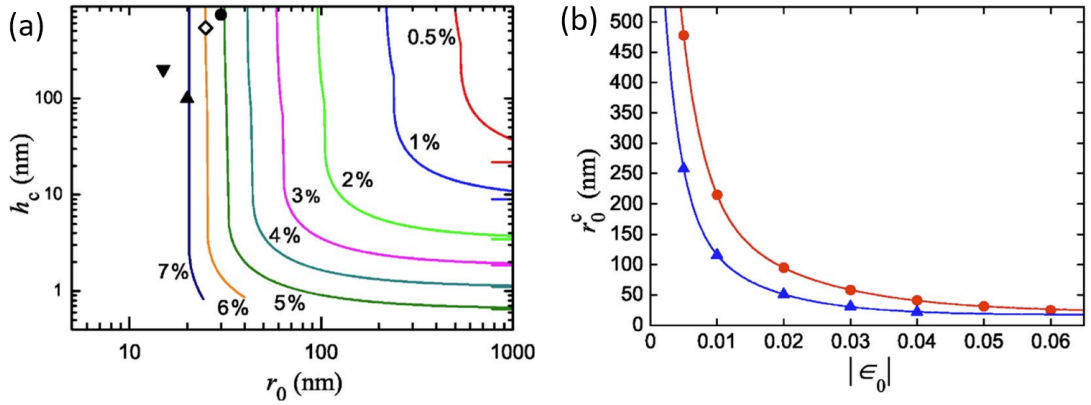

Figure 2.11: Nanowire critical thickness plots. (a) Nanowire critical height as a function of nanowire radius, shown for different lattice mismatch values. Black markers are experimental data points. (b) Critical nanowire radius below which infinitely thick layers could be grown coherently as a function of misfit. Triangles and disks correspond to plastic relaxation by edge and 60° dislocations respectively [52].

By taking the infinite aspect ratio $\rho \to \infty$ limit of Equation 2.5, the equation for the critical diameter for which infinite nanowire growth is possible becomes:

$$\frac{2\pi}{A_\nu}\left(\frac{\alpha^2 b_{\text{eff}}^2}{4} - \alpha b_{\text{eff}} \epsilon_0 r_0^c\right) + C\left(1 + \ln\frac{\beta r_0^c}{b}\right) = 0 \tag{2.7}$$

where all symbols are defined as before. A plot of this equation is shown in Fig. 2.11 (b). A full derivation of this equation is available in reference [52].

2.3 Characterization

The characterization of semiconductors can be split into two types of measurement: in-situ and ex-situ. In-situ measurements happen during the growth of the sample and ex-situ happen after the sample is taken out of the reactor.

In-situ measurements. In our reactor, we have two in-situ measurements available, temperature and reflectivity. The temperature is measured by an Argus sensor which measures the blackbody radiation emitted by the sample. The reflectance is measured by emissivity corrected pyrometry [53] using a commercial package, Laytec EpiTT [54]. It gives information about the layer thickness, composition and roughness of the sample during growth. EpiTT uses a virtual substrate algorithm which is able to remove reflections from previously grown interfaces. This allows the live tracking of the currently grown layer on its own.

The EpiTT reflectance measurements can be used to debug issues on a layer-by-layer basis. Decreases in reflected light intensity signify a large increase in surface roughness. This identifies the problematic layer which can then be fixed on subsequent growths. An example of EpiTT data is shown in Fig. 2.12. The oscillation during a layer growth is caused by interference from the reflections from the top and bottom of the layer. The wavelength of this oscillation can be used to measure the layer thickness. In the example data set there was an unexpected spike in reflectance at the end of the last InAlGaAs step, indicating a possible growth issue.

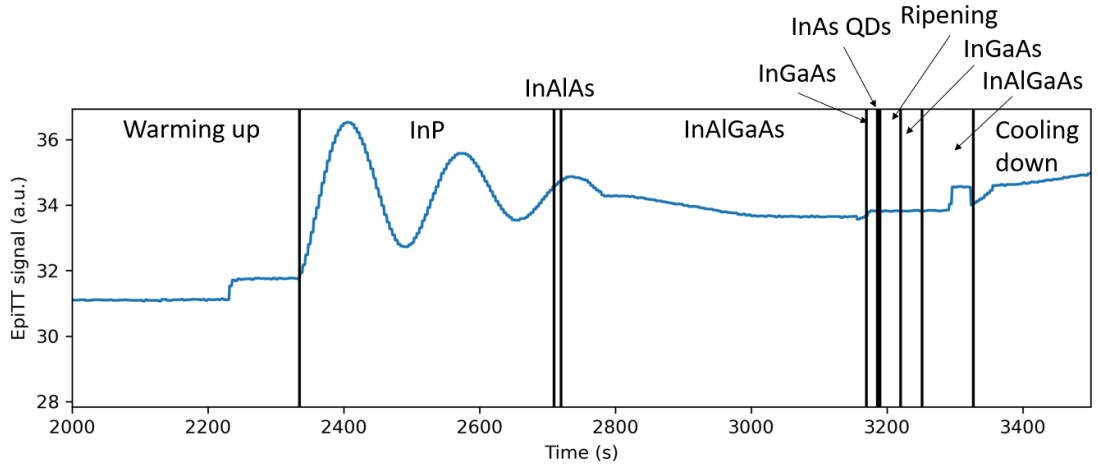

Figure 2.12: Reflectance data for a standard one layer capped QD sample, with every growth step labelled.

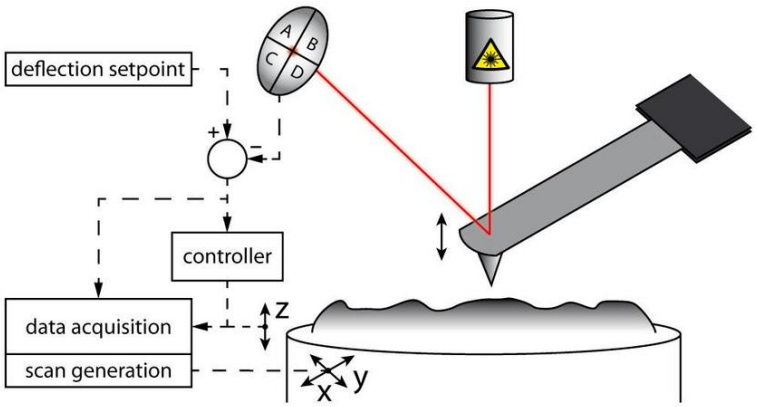

Figure 2.13: Schematic of AFM setup [55].

Atomic force microscopy. Atomic force microscopy (AFM) is a scanning probe microscopy technique which involves measuring the deflection of a cantilever as it passes over a surface. The height of the cantilever is measured by reflecting a laser off its back into a photodetector. A diagram of the setup is shown in Fig. 2.13 A topography or height map of the sample is produced by taking a grid of height measurements across the surface of the sample.

Traditionally, AFM measurement for semiconductor samples is done in tapping mode. In a tapping mode measurement, the cantilever is driven to oscillate at close to the resonant frequency. During the measurement, the tip interacts with the sample through Van der Vaals forces, changing the amplitude of the oscillation. Using the ScanAsyst mode from Bruker AFM Systems [**?**] it's possible to measure with less setup time and less noise compared to tapping mode. This is achieved using peak force tapping. The tip is mechanically lowered and raised from the sample and the force on the tip is measured at every point in time. The force curve provides information about the height and material properties. Moreover, through ScanAsyst cantilever tuning is not needed and measurement parameters are adjusted automatically during measurement which increases the speed and ease measurement.

The software we used for analysing AFM data is Gwyddion [56], an open-source image analysis program written for material science use. The analysis steps are important as

the key values are directly taken from the software. The analysis steps used ensure the data is replicable and comparable between samples.

The analysis begins by cleaning up the image and removing the background data caused by measurement artefacts. The sample might not be perfectly perpendicular to the AFM tip. This can create a gradient which makes it difficult to measure the relevant features. The tip motion is also not perfectly linear so extra tilt and bowing can be added over the heightmap. An example of such measurement including bow and tilt can be seen in Fig. 2.14. To solve this issue, a two-dimensional linear slope is fit to the data, then subtracted. The result can be seen in Fig. 2.14.

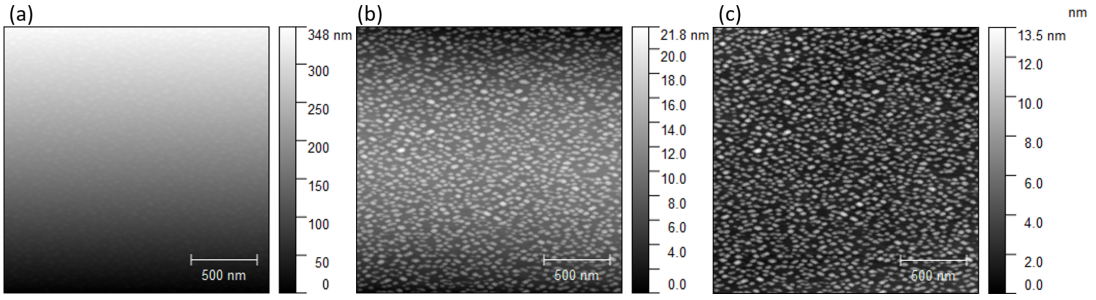

Figure 2.14: AFM heightmap tilt and bow correction. (a) Original image. (b) Image with tilt subtracted. (c) Image with tilt and bow subtracted.

Another common class of AFM artefacts are line effects. One type of line effect manifests as long one-pixel-wide strips of seemingly wrong data. An example can be seen in Fig. 2.15. This is commonly caused by outside vibrations. Meaningful data can be extracted from this using line-by-line background subtraction. This process fits every row using a 1D function (usually parabolic) and subtracts it, one line at a time. The results of using this technique are shown in Fig. 2.15. Depending on the function chosen, this might not completely remove the background, leaving some stripe artefacts in the image. This can be mitigated by selecting the affected area and interpolating over the outlier pixels.

Defects are also created by the line-by-line background removing method discussed

previously. Tall particles on the surface will skew the fit around them. This will cause a shadow-like effect next to the tall particle. This can be seen in Fig. 2.15. Two-dimensional fits should be relatively safe against this type of error. If line-by-line fits are needed, different functions will react differently to high peaks in the data. Higher order functions generally perform better, as do moving-averages functions. This technique can introduce 'shadows' when there are large sample features that influence the fit.

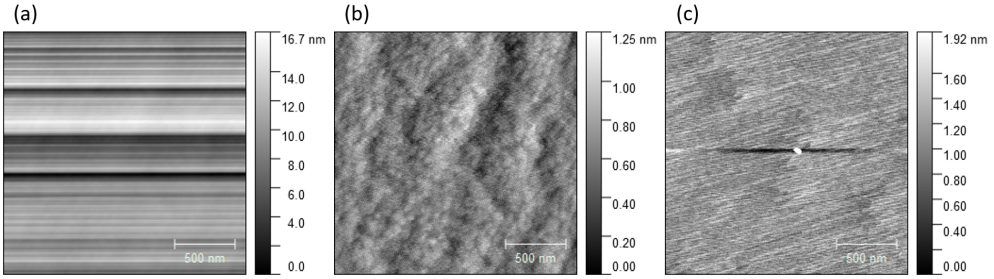

Figure 2.15: AFM image line-by-line corrections. (a) Original image. (b) Image with parabolic line-by-line background removed and with outliers removed. (c) Example of shadowing that can arise from line-by-line background removal.

AFM scans are very important in the study of quantum dots, giving a measurement of dot density, size and shape before capping is applied. As a single $1\,\mu\mathrm{m}^2$ scan typically contains around 300 dots, it's impractical to measure every dot by hand. Instead, an automated approach makes this task much easier. To do this, the pixels that contain a dot are masked by an algorithm. The easiest method is a simple masking based on thresholding, where every pixel above a height threshold gets masked. This works if the underlying surface is very flat and all dots have similar height, unfortunately, this is rarely the case as shown in Fig. 2.16.

A watershed algorithm [57] can mark the dots much more effectively. For visual convenience, the height map can be considered to be inverted. Watershed is a two-step algorithm which can be visualised as water pouring down on the height map. The first step involves finding the minima of the surface, the second step finds the boundaries of

the dot. The first step can be thought of as dropping a drop of water at every point in the image and simulating its flow downwards. The drops will reach a stable position at a minimum of the surface and will accumulate into 'lakes' or 'grains'. Ideally, each lake corresponds to a dot, but if the dots are very close to each other they might be combined into the same lake. The second step deals with the segmentation of such lakes by taking into account the path every drop has taken to reach the lake and dividing the lake such that similar paths are grouped together. The algorithm is controlled by a few parameters which can be changed to obtain a better masking such as drop sizes, lake threshold values and number of iterations. These parameters are important to ensure grain location and segmentation follow the distribution and shape of the dots.

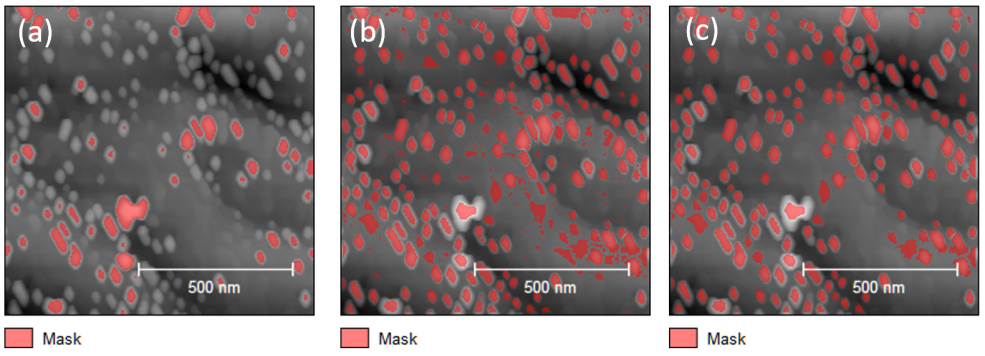

Figure 2.16: Masking QDs in an AFM image. (a) Threshold mask. Many dots are not masked correctly. (b) Watershed algorithm. All dots are correctly masked, but other unwanted features are masked as well. (c) Watershed algorithm after filtering. Every dot on the sample is masked with a single grain.

Filtering the results of the watershed algorithm is required, as it can create grains that do not select dots. For example, small grains a few pixels wide created by noise or roughness in the sample, or large grains in otherwise flat and dotless areas. For the sample image, the grains were filtered based on their size (reject anything under a few pixels), and RMS width of height distributions (reject any grains that are too flat). The resulting mask, Fig. 2.16, successfully selects every dot as a single grain. This allows us to extract statistical information about the dots.

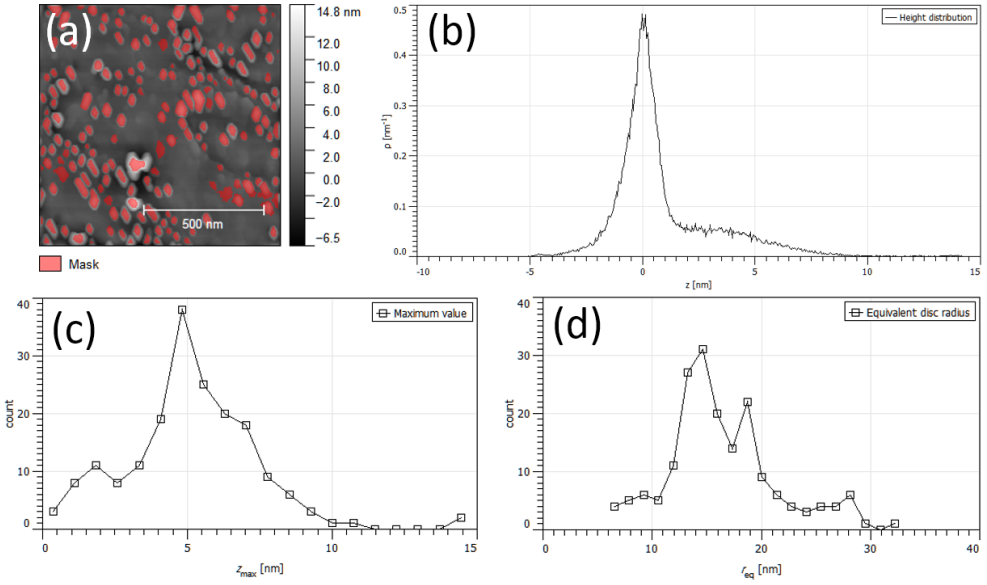

Figure 2.17: AFM dot height and diameter distributions. (a) Image with background flattened. (b) Image height distribution centred at a height of zero. (c) Dot height distribution. (d) Dot diameter distribution.

Finally, to extract the dot height distribution we need to ensure the zero point for height is the same across all samples. This can be done by setting the peak of the height distribution as the zero point. To minimise the effect of surface roughness we need to flatten the surface. This can be done by a high order polynomial background subtraction, similar to the parabolic background subtraction from before. If more precise control is needed, it's usually possible to flatten the surface by editing the Fourier spectrum of the image. A fifth-order background subtraction is used in Fig. 2.17 (a). The resulting height and diameter distributions are also shown in Fig. 2.17. While the height distribution is accurate and comparable between samples, the diameter distribution is much less reliable. It computes the diameter based on the shape of the masked grains. Using the watershed algorithm it's difficult to accurately mask the edges of a dot, as they are not very well defined.

Photoluminescence. Photoluminescence (PL) is the process in which a semiconductor absorbs a photon and then releases a lower energy photon, with an energy close to the bandgap of the semiconductor. A diagram of the process is shown in Fig. 2.18. A light source (usually a laser) is used to produce a pumping beam with photon energy higher than the bandgap energy of the material. The pumping light is absorbed by the semiconductor by exciting electrons to the conduction band. Carrier-phonon scattering interactions happen on timescales on the order of 100fs. Since phonons have comparatively high momentum and low energy, many such interactions can happen before an electron reaches the bottom of the conduction band. Radiative recombination happens on much longer timescales, on the order of nanoseconds. Given the timescales of the two processes, it is most likely that an electron has time to fully relax to the bottom of the band edge before recombining. This means that the emitted photon will have an energy close, slightly higher, than that of the bandgap. If the measurement is taken at room temperature the emission peak will be broadened due to the carriers obeying Boltzmann statistics.

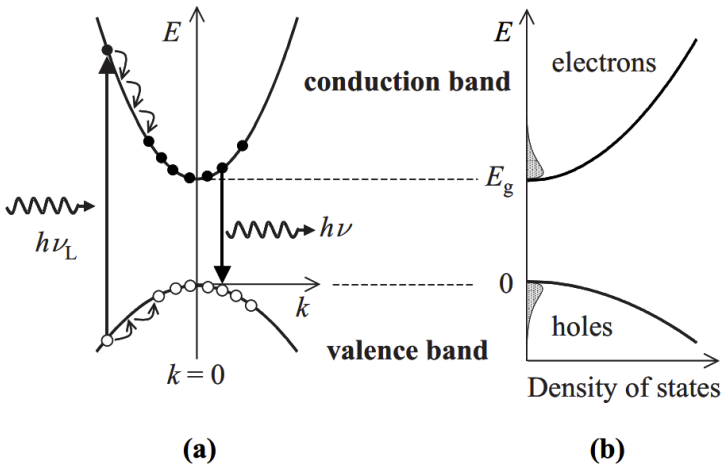

Figure 2.18: Diagram of the photoluminescence mechanism. (a) An incoming photon of energy $h\nu_L$ excites an electron from the valence band to the conduction band, leaving a hole in the valence band. The two carriers relax toward the band gap edge through fast phonon interactions. Close to the band gap, the carriers recombine releasing a photon at an energy close to that of the band gap, $h\nu$. (b) Density of states and carrier densities during optical pumping [58].

Fig. 2.18 (b) shows the carrier density during optical pumping, for low pumping powers. The peak of the photoluminescence energy spectrum can be taken to be the semiconductor bandgap. For high pumping powers, the carriers will be excited to the conduction band faster than they can radiatively recombine. This leads to a pile-up of carriers at the bottom of the band which leads to a broadening and a blueshift of the emission spectrum. This is called the band-filling effect [59].

For our measurements we are interested in very small devices, making spatial resolution an important part of the measurement. An objective lens is used to focus the pumping laser and collect the emitted light in a technique called microphotoluminescence. A diagram of the setup used for the measurements in this thesis is shown in Fig. 2.19. Three lasers are used to provide optical excitation: a low power 622nm HeNe laser, a pulsed supercontinuum laser passed through a acousto-optic funable filter, and

a high power femtosecond pulsed 780nm laser. Pulsed lasers are used for samples that require high pumping powers but are easily thermally damaged such as nanowires. The bright pulses satisfy the power requirement, while the low total average power helps to not overheat the sample. Flip mount mirrors are used to select the laser source. Additionally, a broad area white light lamp can be used to illuminate a large area on the sample which is useful for focusing and finding patterns on the sample.

A dichroic mirror is used to selectively reflect visible light from the pumping lasers and the lamp into the tube lens and to the sample. The dichroic mirror is transparent to infrared wavelengths, allowing the photoluminescence emission to pass through into the detector. A silicon CCD camera can be inserted into the optical path to help align the desired area on the sample with the laser spot. To focus the light into a small spot on the detector, a focusing lens can be inserted in front of the slit. A red light filter stops any pumping laser light that made it through the dichroic mirror from entering the detector. From there the light goes into a Princeton Instruments HRS 750 Action Spectra Pro diffraction grating spectrometer and a 512×512 pixe Princeton Instruments NIRvana 640 InGaAs 2D array detector.

The InGaAs array detector can be used to image both the zeroth and first-order diffraction patterns. In zeroth order, this is equivalent to a simple reflection allowing us to use the array detector as a camera showing spatial information. Using the detector in camera mode we can align the pumping laser spot to various parts of the pattern under study with sub-micron precision. When observing the first diffraction order, spatial information can still be observed in the vertical axis of the detector, while the horizontal axis displays the light spectrum. This is equivalent to taking 512 spectra at different positions on the sample. The focusing lens can be added to focus the spatially separated light beam into a single small spot which is used for measurements with small slit apertures.

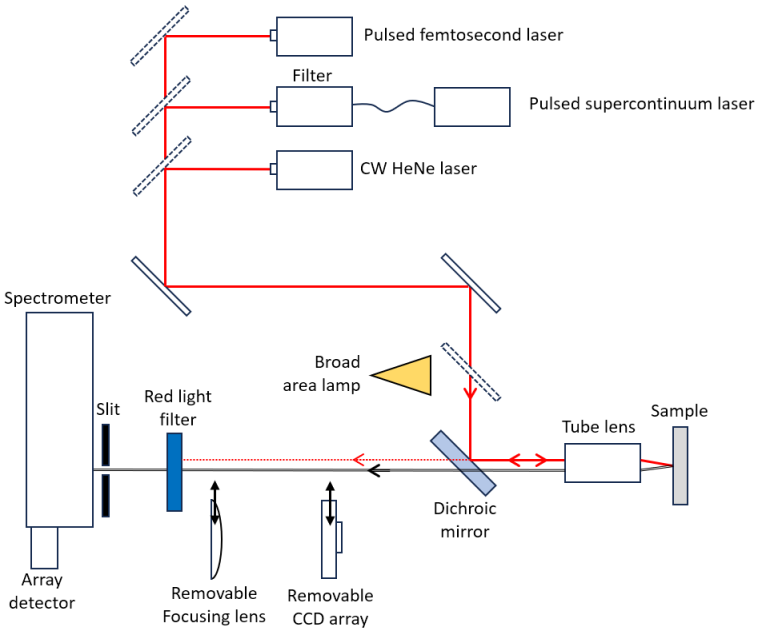

Figure 2.19: Micro-photoluminescence setup diagram. The pumping laser can be chosen using flip-mount mirrors. The laser is focused by an objective lens. The PL emission is collected by the same lens and imaged using the spectrometer and IR detector. For visual imaging, a lamp and silicon CCD can also be used..

Scanning electron microscopy. Electron microscopy is used to resolve details smaller than the wavelength of visible light. The main components of a scanning electron microscope (SEM) are a high energy electron souce and adjustable magnetic lenses, along with a suite of different detectors. The SEM operates by shooting a focused electron beam at the sample and measuring the resulting scattered electrons and X-rays. The interactions between the beam electrons and the material is quite complicated, involving many different physical interactions, shown in Fig. 2.20. The types of measurements are used in this thesis are: secondary electrons, characteristic X-rays, back scattered electrons, transmitted and diffracted electrons. Transmitted and diffracted electrons are part of transmission electron microscopy (TEM) and will be discussed later.

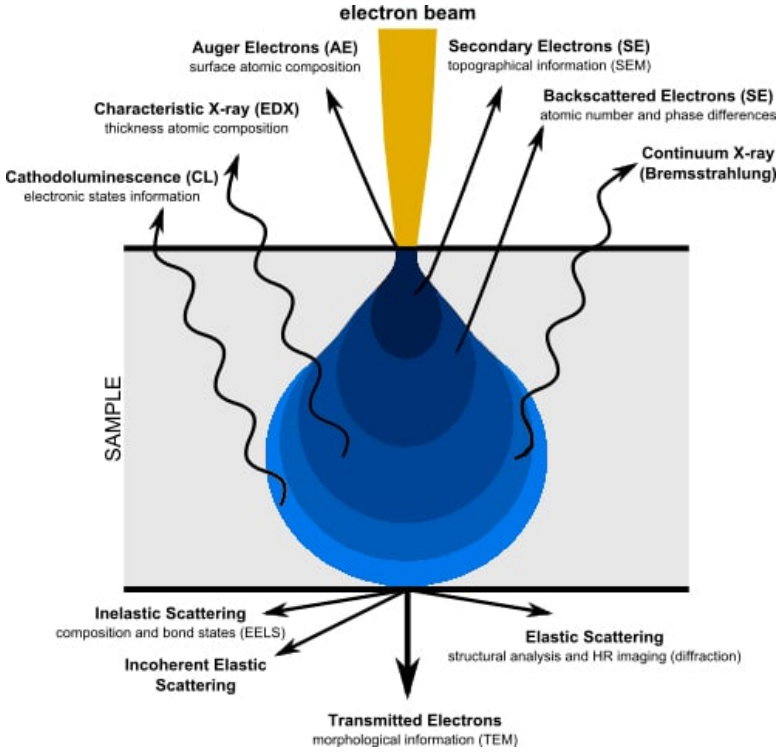

Figure 2.20: SEM interaction volume showing the different physical interactions that happen between the beam and sample, along with their measurable effects [60].

Secondary electrons are emitted from a small interaction volume, close to the surface of the sample. Contrast is created mainly by the change in available interaction volume due to changes in the angle of the surface. Secondary electron imaging is therefore best for imaging surfaces in high detail.

Characteristic X-rays are emitted by electrons, excited by the electron beam, falling to lower energy levels. The interaction volume is larger than secondary electron, providing significant depth information. The spectrum of the X-rays can be used to identify the elements being imaged, and to approximate material composition.

Electron channelling contrast imaging (ECCI) is a non-destructive technique used to image defects close to the surface of semiconductors. We consider electrons passing through a crystal by modelling electrons as particles. Electrons will interact and get

scattered by atoms close to the surface of the crystal, as shown in Fig. 2.21 (a). If the electron beam is aligned with one of the high symmetry directions of the crystal, the electrons can propagate much further into the material without interacting with the lattice, as shown in Fig. 2.21 (b). These directions are called 'open channels' and they considerably decrease the number of backscattered electrons. Dislocations locally break the crystal periodicity and possibly close the open channels, as shown in Fig. 2.21 (c). By aligning the electron beam to an open channel, we can measure dislocations as high contrast spots on the backscattered electron image. Stacking faults and grain boundaries are also visible in these images since they break the crystal lattice as well.

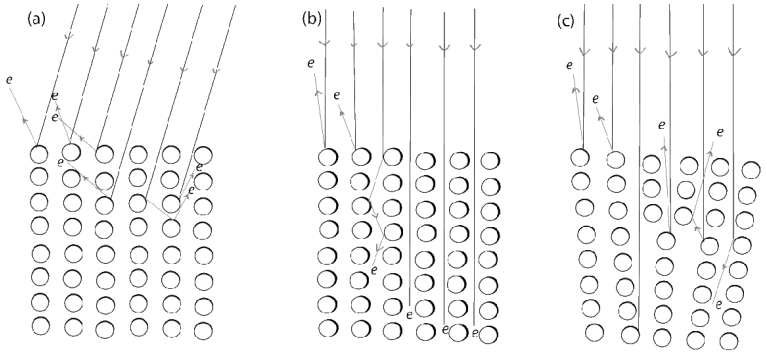

Figure 2.21: Open and closed channels in ECCI. (a) Imaging at an arbitrary angle resulting in high backscattering. (b) Imaging parallel to a lattice direction (open channel) resulting in low backscattering. (c) Imaging an open channel next to a dislocation resulting in high backscattering [61].

Other information that can be found using ECCI includes the type of dislocation, as the size of the strain field of the dislocation is proportional to the magnitude of its Burgers vector we can distinguish between edge and screw dislocations. Additionally, the direction of the Burgers vector can be found by imaging multiple different open channels and considering the $g \cdot b = 0$ condition.

Transmission electron microscopy. To measure transmitted and diffracted electrons, the samples must first be sufficiently thinned to around 100 nm, typically with a focused ion beam. Considering the incoming electron beam as a planar wave, each crystal plane will cause diffraction and create coherent interference at one point in the image plane, resulting in a diffraction pattern specific to the crystal type. By measuring the intensity of the central transmitted spot or one of the diffracted spots at multiple points on the sample, bright field and dark field images can be formed respectively. TEM images can be used to see defects in the crystal structure with atomic resolution, along with crystal phase and orientation.

X-ray diffraction. The working mechanism of X-ray diffraction measurements is similar to that of transmission electron microscopy. Instead of an electron beam, X-ray are used to probe the structure of the sample. X-rays have a much higher penetration depth, allowing for non destructive characterisation of samples. X-rays incident on the sample will be diffracted by the atomic planes of the crystal. The relationship between diffraction angle and interplanar spacing is given by Bragg's law:

$$n\lambda = 2d \sin\theta \tag{2.8}$$

where n in the diffraction order, typically 1, λ is the X-ray wavelength, d is the interplanar spacing, typically measured for the $(0\,0\,4)$ plane, and θ is the diffraction angle. The position of the diffracted peak depends on the distance between atomic planes, which allows for a direct measurement of the out-of-plane lattice constant. There is no direct information about the in-plane lattice constant. Reciprocal space mapping, or assumptions about the level of relaxation of the material are required to find the in-plane lattice constant. XRD results are useful for growing mismatched materials as it provides a quick, non destructive measurement of lattice constant and composition.

Resonators and lasers. A laser cavity consists of a gain medium and two reflectors facing eachother. Light emitted by the gain material will be reflected between the two mirrors, passing through the gain material and contributing to stimulated emission. The field inside the cavity will resonate at specific frequencies, related to the length of the cavity.

The confined light can escape the cavity in multiple ways. Mirrors will never be 100% efficient, and typically one mirror is intentionally made less reflective to favour emission from a single facet. Sidewall roughness, mirror facet roughness, bending losses, and defects inside the gain material all contribute to loss of light. To quantify this, the Q factor of the resonant cavity is typically used. It is defined a measure of the strength of dampening of an oscillator. For an optical resonator it can be written as

$$Q = \frac{2\pi\nu T}{l} = \frac{\nu}{\delta\nu} \tag{2.9}$$

Where ν is the resonant frequency, T is the round trip time, l is the fractional power loss, and $\delta\nu$ is the FWHM of the resonant peak spectrum. The first definition shows the relation to damping, while the second definition provides an easy way to experimentally measure Q.

Chapter 3

Large area planar heteroepitaxy

Large-area planar heteroepitaxy involves growing epilayers on the whole wafer, or in large lithographically defined pockets and trenches with an area large enough to allow for complete relaxation of the material. This type of epitaxy results in very high defect densities as the epilayers are allowed to relax through the creation of misfit dislocations. To be fully compatible with silicon photonics, the wafer surface is a (001) oriented Si surface, which induces antiphase boundaries into the epilayer. There are two main types of defect reduction techniques employed in planar epitaxy, modifying the Si surface and adding defect filter layers.

3.1 Introduction

Silicon substrates. As most defects are nucleated at the substrate interface, controlling the growth surface is very important in reducing defects. Growth on offcut wafers was one of the first techniques for removing APBs. Large offcuts, typically around $4°$, create bilayer atomic steps on the silicon surface, thus removing the ABP creation conditions, as shown in Section 2.1.1. This technique is very effective, however, offcuts this large are incompatible with CMOS fab processes.

More recent APD removal techniques make use of the silicon surface reconstruction structure. For a nominally non-offcut Si wafer, the surface steps will be monoatomic [62]. The surface reconstruction will create dimer pairs in alternating directions on

every step, shown in 3.1 (a). The adatoms will have a higher diffusion length in the dimer direction, causing anisotropic growth for every domain, shown in 3.1 (b). Because of the higher growth rate in the direction perpendicular to the steps, the main phase will start overlapping and growing over the antiphase, confining the antiphase close to the Si boundary. This technique requires the size and shape of the III-V nucleation islands to be small which requires careful optimization of the growth parameters.

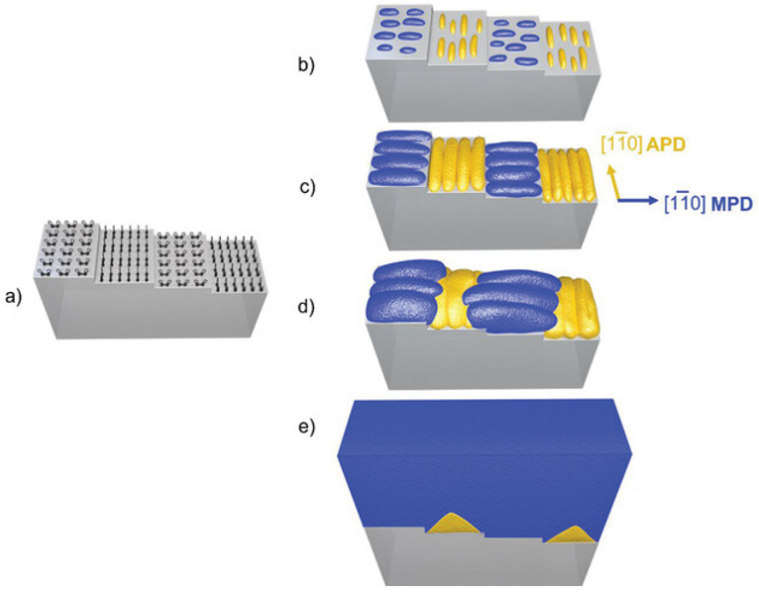

Figure 3.1: Antiphase boundary removal mechanism. (a) Initial dimer structure on the monoatomic step Si surface. (b)-(e) Epilayer evolution showing efficient removal of the antiphase domain (ABD) from the main phase domain (MPD) [63].

Another technique involves the high-temperature annealing of nominally non-offcut CMOS compatible wafers (usually offcut under 0.1∘). Annealing Si at high temperatures (over 900 °C) in a hydrogen-rich atmosphere produces an anomalous behaviour of promoting diatomic layer steps. [64] This is favourable for APB removal, but raises concerns about the thermal budget.

Blanket epitaxy. The threading dislocation density decreases with the thickness of the epilayer due to the interaction and annihilation of TDs. The TDD is expected to

follow the inverse square of epilayer thickness [65], so thick buffer layers are desirable for defect reduction. However, thick buffers suffer from bowing and cracking issues, particularly for GaAs [66, 67]. Thick InP buffers can be grown thicker (over 10 µm) due to the lower InP coefficient of thermal expansion mismatch to silicon (about double) compared to GaAs (about triple). To reduce bowing and cracking, selective area epitaxy can be employed to reduce the total thermal strain. Growth in pockets or trenches can limit this issue and improve the waveguide coupling efficiency. [68–70]

To slightly mitigate the effects of the large lattice mismatch between InP and Si, layers of intermediate lattice constant such as GaAs and GaP can be used. These intermediate layers reduce the stress in the InP layer and the TDD. [71]

Defect filter layers. The critical thickness for a coherently strained thin layer is twice that for a single strained layer, due to the additional strained interface. This allows the creation of strained quantum wells of considerable thickness. A pre-existing threading dislocation passing through a strained layer will experience forces based on the strain field. If the layer exceeds its critical thickness, the dislocation will experience equal and opposite forces at the two interfaces, so it will continue propagating on the initial path.

Intentionally exceeding the critical thickness of the capped layer will result in the dislocation being pushed in one direction as the forces at the two interfaces are not balanced. This could be done either in situ during growth or in a post-growth annealing step. The use of thick slightly strained layers has been proven to be more effective than strained layer superlattices for GaAs/Si [72].

Strained layer superlattices are still a popular choice for defect filter layers. An SLS has two relevant critical thicknesses, the individual layer thickness and the average structure thickness. Exceeding the average structure critical thickness is similar to using a single thick layer with equivalent strain. The advantage of SLS is that it provides a large number of strained interfaces, increasing the probability of bending dislocation,

and potentially causing them to interact and self annihilate.

Quantum dots have been used in a similar manner as they are surrounded by strong strain fields [73].

The efficiency of a DFL is measured as the ratio of the measured defect density at the surface and the defect density without the filter layer. The defect density without the filter layer can be approximated as following a t^{-2}, where t is thickness, or measured from a sample grown with no filter layer [74].

Planar epitaxy review. Recent work on large-area epitaxy has made use of numerous methods to reduce the defect density in the active layer. Offcut substrates, v-groove patterned substrates, and surface treatments have been used to eliminate anti-phase boundaries. Defect densities have been reduced using various types of defect filter layers such as strained superlattices, and strained quantum dots. Table 3.1 shows selected recent results, showcasing the variety of techniques and materials currently in use.

The best GaAs on Si devices with low defect densities on the order of $10^6\ \mathrm{cm}^{-2}$ [72] are approaching industrially acceptable levels of threshold and lifetime. However, due to the much larger lattice mismatch, InP based devices are still unavailable due to the high defect densities. The best InP results have been achieved using v-groove substrates and SLS defect filter layers, achieving a TDD on the order of 10^{-7} using a total buffer thickness of 6.4 $\mu\mathrm{m}$.

The use of thick buffers makes coupling the active region to a waveguide difficult. In recent years, growth in pockets has been used to bring the active region and the waveguide to the same level.

Table 3.1: Recent achievements in large area epitaxy on silicon, showcasing the different defect reduction methods used. Representative images collected in Fig. 3.2.

	Chinese Academy of Sciences [68]	University of California Santa Barbara [69]	University of Montpellier [70]	University of California Santa Barbara [75]	Hong Kong University of Science and Technology [73]
Year	2023	2022	2023	2020	2018
TDD [cm^{-2}]	2.6×10^7	6×10^8	5×10^7	4.5×10^7	3×10^8
Gain material	1.3 µm InAs/GaAs QD	1.3 µm InAs/GaAs QD	2.3 µm Sb-based QCL	1.5 µm InGaAsP QW	1.5 µm InAs/InP QD
Material system	GaAs	GaAs	Sb	InP	InP
Defect reduction techniques	Homoepitaxial V-groove, Large area patterning	InGaAs DFL MOCVD GaP seed	0.5deg [110] offcut Si wafer	Large area V-groove patterning InGaAs/InP SLS DFL Graded InGaAs buffer	InAs/InP QD DFL
Growth technique	MBE	MBE + MOCVD	MBE	MOCVD	MOCVD

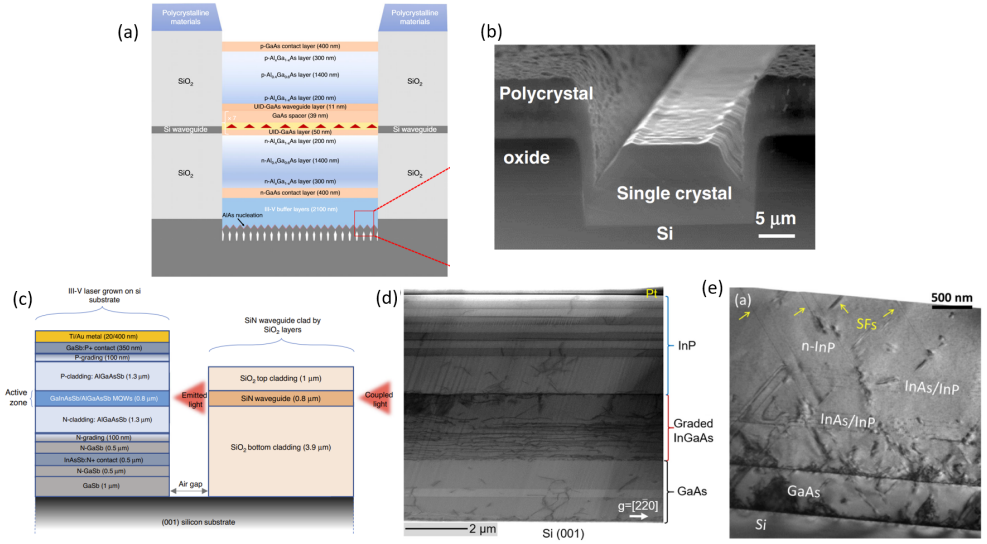

Figure 3.2: Representative images of recent advancements in large area planar heteroepitaxy. Relevant details are presented in Table 3.1. (a) GaAs/Si grown in-pocket on a homoepitaxial Si V-groove surface [68]. (b) GaAs/Si grown in-trench on a flat Si surface [69]. (c) GaSb/Si grown on a flat Si surface with a small offcut [70]. (d) InP/Si grown on large area V-groove surface [75]. (e) InP/Si grown on a large flat Si surface [73] .

3.2 InP on Silicon

We aim to create CMOS compatible InP on Si templates which minimize the defect density. Since the thermal expansion coefficient mismatch between InP and Si is comparatively small, we can grow thick buffer layers; however, this makes light coupling difficult even with a pocket epitaxy approach. Our approach uses low offcut silicon wafers with a GaAs nucleation step to remove antiphase boundaries, followed by InP bulk with strained defect filter layers to reduce the threading dislocation density.

GaAs on Si. For our buffer templates, we use $(0\,0\,1)$ oriented silicon wafers, with low offcuts of less than 1°. The lower offcut could be relatively more acceptable for

CMOS processing, unlike the larger 4° commonly used in the past. For comparison, we place a nominally zero-offcut wafer in the reactor as well. The wafers are taken out of the reactor for measurement after every layer. New wafers are grown from scratch for every additional layer and used for the next set of measurements. The measurements are shown in Fig. 3.3.

The growth process begins with a dilute HF dip to remove the native oxide on the silicon substrate. The substrates are placed in the reactor and annealed at a temperature of 900°C for 10 minutes to remove any residual oxide and prepare the stepped surface for growth. The first 10nm low temperature GaAs nucleation layer is grown at 380°C. Following that, 50nm of GaAs are grown at a higher temperature of 550°C. The temperature is kept the same, but the growth rate is tripled for the final 500 nm.

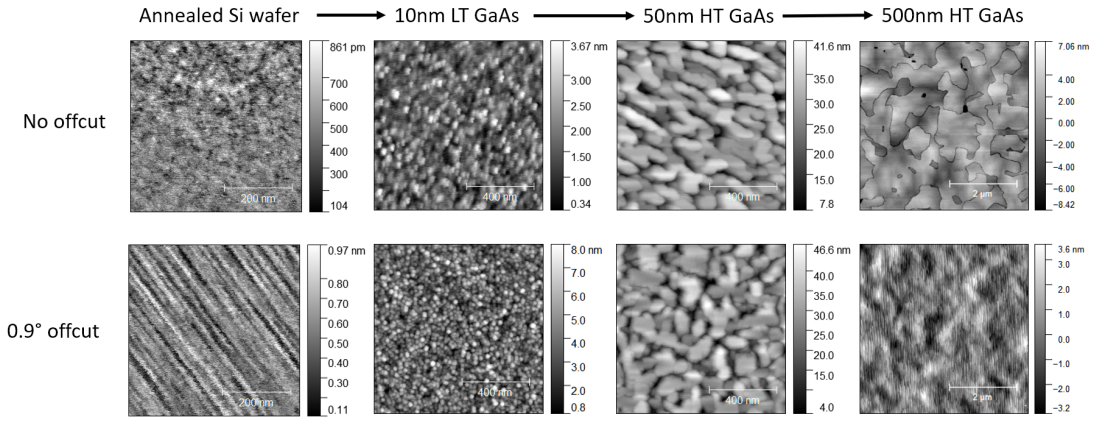

Figure 3.3: Comparison of GaAs growth directly on silicon with nominally 0° and with 0.9° offcut. The surface scans are taken after every growth step, from low temperature (LT) nucleation to high temperature (HT) buffer. While the nucleation layer appears similar, after a 500 nm thick buffer layer the antiphase domains become visible for the no-offcut wafer.

Nucleation and APB removal. Fig. 3.3 shows the progression of the surface at every growth step. The annealed wafer is taken out of the reactor and the surface is measured using AFM. The surface is likely oxidized by the time the measurement is taken.

Neither sample shows clear steps, but the offcut wafer shows clear linear structures. It's likely that surface steps are present under the oxide, but we could not determine if they are single or diatomic height. The zero-offcut wafer appears amorphous, likely due to the sparse surface steps.

The GaAs nucleation layer shows a much clearer surface structure since it is not oxidized. The nucleation density is much higher on the offcut sample. This is expected for a surface with higher density steps since nucleation is most likely to occur at a step edge. Since the layer thickness is much higher than the step size, the effects of step height are not very visible at this point.

The next 50 nm step at a higher temperature shows the nucleation islands merging together. The different phases appear to be separated at this point. Interestingly, the orientation of the domains is different for the two samples. The growth rate is dependent on the dimer direction, which is different for the two phases. This suggests that the zero offcut sample is mainly in the same phase in the scan area, and the offcut sample has both phases in the scan area. Using the growth model presented in Fig. 3.1 we expect the high step density on the offcut sample to create alternating polarity boundaries. This confirms that at 60 nm GaAs growth thickness we are at step (c) of the model. This model holds true for monoatomic silicon surface steps, but not for diatomic steps. This implies that the steps on the offcut sample are mainly monoatomic.

The following 500 nm presents a stark difference between the two samples. The zero offcut sample has clear high density antiphase boundaries. This is expected since the annihilation distance depends on the distance between monoatomic steps. For the 0.9° sample no antiphase boundaries are observed on the surface. Due to the dense monoatomic steps on the surface, we were able to achieve antiphase boundary free GaAs/Si on CMOS compatible wafers.

InP on Si. We grow 1 $\mu\mathrm{m}$ InP on the GaAs/Si templates using a strained 300 nm InAlAs layer inserted into the InP layer. The samples are grown starting from the

silicon wafer. The GaAs layers are grown as described in the previous section. InP growth starts with a low temperature, low growth rate 50 nm layer at 450 °C. The temperature is then increased to 560°C and the growth rate is gradually increased. The filter layer is then grown at the same temperature, using various materials and structures. Finally, 500 nm InP is grown to finish the structure.

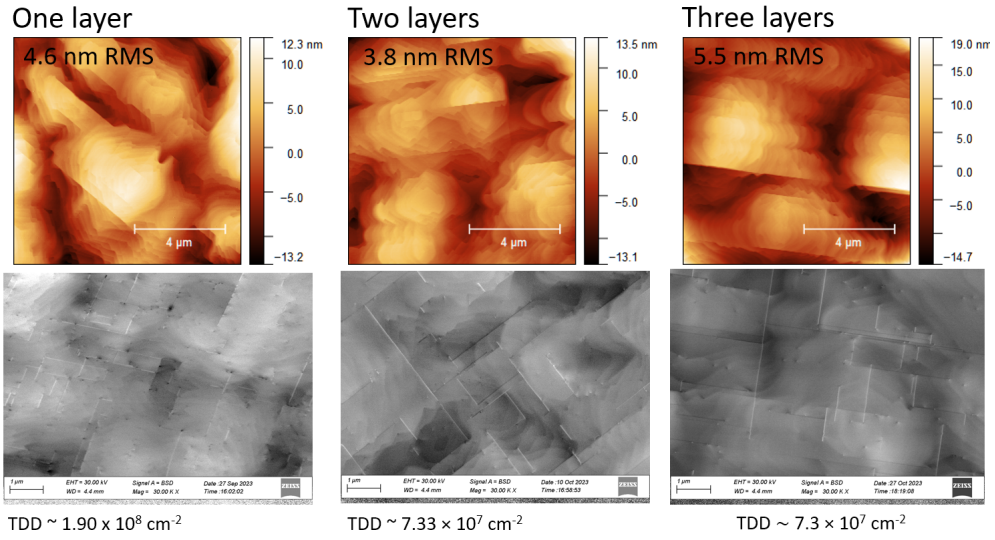

Figure 3.4: Defect filter layer structure diagrams for InP/Si. All samples were grown under identical conditions, with the only difference being the defect filter layer..

We used four different defect filter layer designs: a 200 nm InGaAs layer and a set of three different 300 nm InAlAs structures. The three InAlAs structures were designed to have the same total strain and thickness to create a fair comparison. Sample (a) uses three InAlAs layers of different thicknesses: 50, 100, 150 nm, and with different compositions: 50%, 60%, and 70% indium. Sample (b) Uses the same three-layer structure with the same compositions, but the layer thicknesses are all set to 100 nm. Sample (c) uses a single 300 nm layer with a composition of 60% indium. Sample (d) uses a 200 nm InGaAs defect filter layer with a 60% indium composition. Diagrams of these structures are shown in Fig. 3.5. The surfaces of these four samples are rougher than the GaAs/Si template. The smallest roughness was found for sample (a) with an

RMS of 3 nm, while the others are in the range of 5-6 nm.

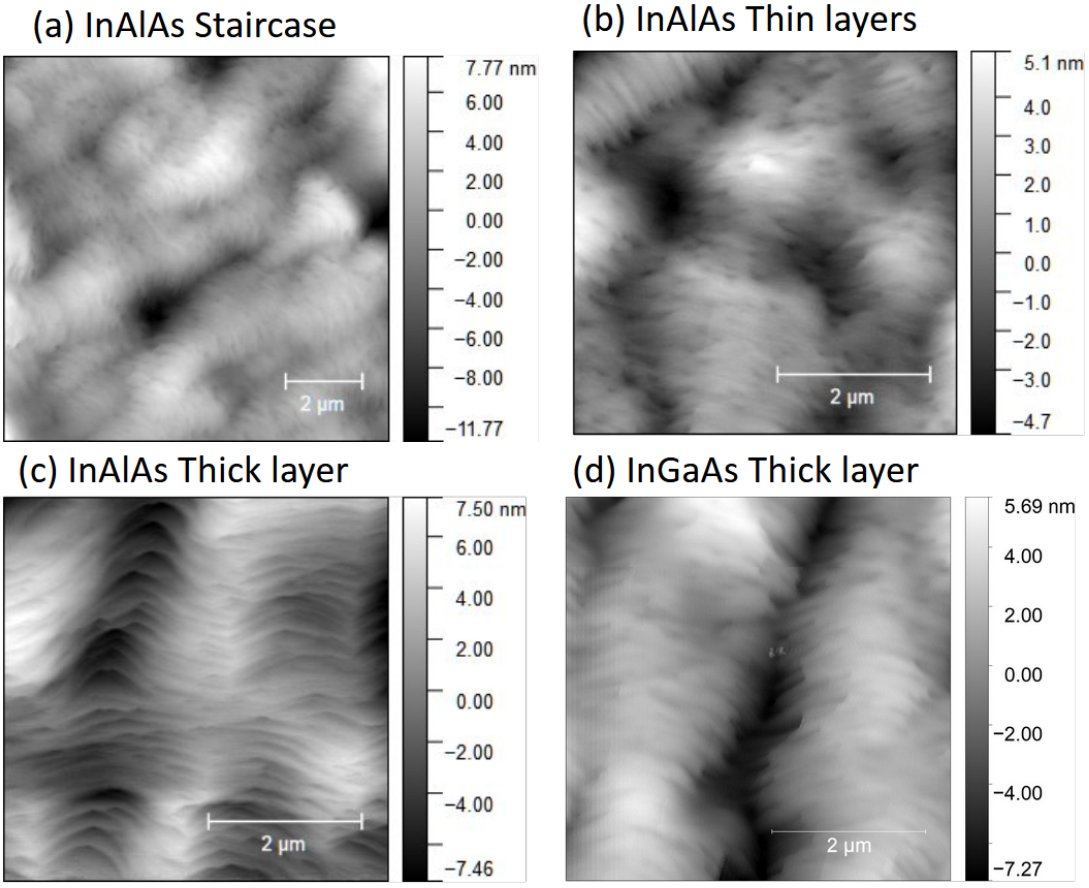

Figure 3.5: AFM images of the four defect filter layers grown on silicon wafers. Note different scale for (a).

XRD studies. X-ray diffraction has been used to measure the composition of the InGaAs and InAlAs layers. Using Vegard's law, Equation 2.1, it is possible to determine the composition by knowing the lattice constant of the material. We find the lattice constant from the position of the XRD peaks, assuming that the layers are completely relaxed. The XRD measurements are presented in Fig. 3.6.

Additionally, XRD can be used to estimate the threading dislocation density in the InP layer using Equation 3.1. This equation assumes that the width of the peak is

$$\text{TDD} = A(\frac{\beta}{3b})^2 \tag{3.1}$$

where β is the FWHM the XRD peak, A is an experimentally measured constant, and b is the Burgers vector of the dislocation. The A constant accounts for the difference between the XRD and ECCI measurements, where it is assumed the ECCI gives the true surface TTD number. For InP the Burgers vector is $\frac{1}{2a[\bar{1}\,1\,0]}$ where $a = 5.8$Å is the relaxed lattice constant.

To calibrate the estimation of threading dislocation density using Equation 3.1, sample (b) was measured using both XRD and ECCI. ECCI is a more accurate technique as it only uses surface level information, rather than bulk material. The TDD measured by ECCI was approximately half that estimated by XRD. Using the found calibration factor of $A = 0.46$ we can find the actual surface TDD for all samples.

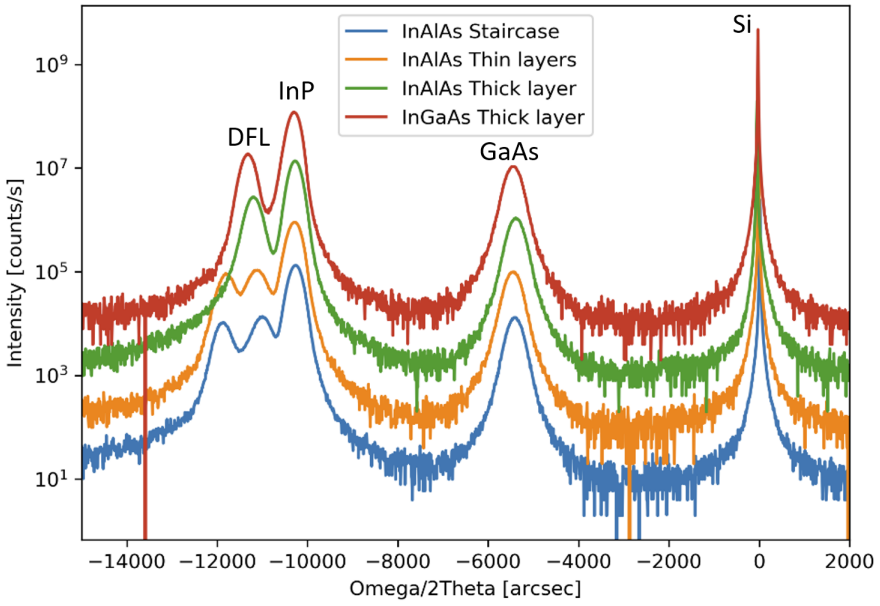

Figure 3.6: XRD patterns for the four defect filters layers

Using this technique we find the threading dislocation densities of samples (a), (b), (c) and (d) to be 2.8, 5, 3.2, 3.0 $\times 10^8$ cm^{-2} respectively. All defect filter layers appear to be similarly effective, with the only outlier being sample (b) with three 100 nm InAlAs

steps. It's not immediately apparent why this filter layer is less efficient. One possible explanation for the broader InP peak of this sample is that the 150 nm InAlAs layer is not perfectly lattice matched with InP. The slight mismatch will appear as a slightly broader InP peak, as the peaks are too close together to be distinguished. This effect would be reduced for the sample with 100 nm as the peak is weaker. The other two samples do not have any lattice matched layers, so the FWHM approximation should be accurate.

CEA-Leti InP/Si template. We also received some InP/Si templates through collaboration with CEA-Leti. These templates are grown using MOCVD and consist of small offcut silicon wafers with a 400 nm GaAs layer and a 140 nm InP layer, shown in Fig. 3.7 (a). The antiphase boundaries are removed using a plasma cleaning and thermal annealing procedure on the silicon wafer before growth [64].

The as-delivered template was found to have pinholes and debris on the surface, as seen in Fig. 3.7. There is a large density of crystal defects on the surface, including threading dislocations and stacking faults. The threading dislocation density is $1.6 \times 10^{9} \mathrm{cm}^{-2}$ and the stacking fault number density is $2.1 \times 10^{9} \mathrm{cm}^{-2}$ as counted from the ECCI images. The threading dislocation density count does not include the partial dislocations bounding the stacking faults. The RMS roughness of the template, discarding debris, is 1.5 nm.

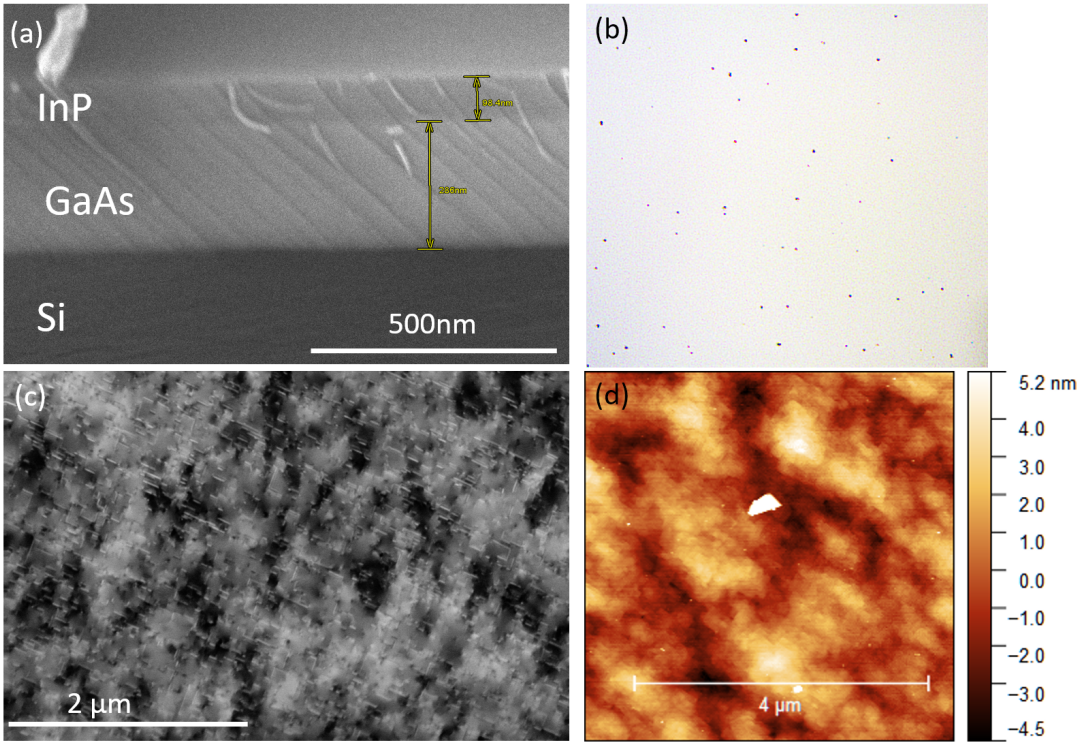

Figure 3.7: CEA-Leti InP/Si template (a) cross-sectional, (b) optical microscope image showing pinholes over an approximately 50×50 µm area and (c) ECCI image showing surface defects and (d) AFM image showing the surface and debris.

InP epitaxy. The debris and pinholes on the surface of the template posed an issue during growth, as they act as nucleation for further defects. After growing 1200 nm of InP at 590°C, the surface roughness increases to 3.3 nm and small dense pinholes appear on the surface. To improve the surface quality, a lower temperature 100 nm layer was grown at 450°C was used. This was successful in removing the small nanometre-wide pinholes, however, the larger pinholes nucleated at the debris on the template were still present. However, the RMS roughness increased slightly to 4.4 nm.

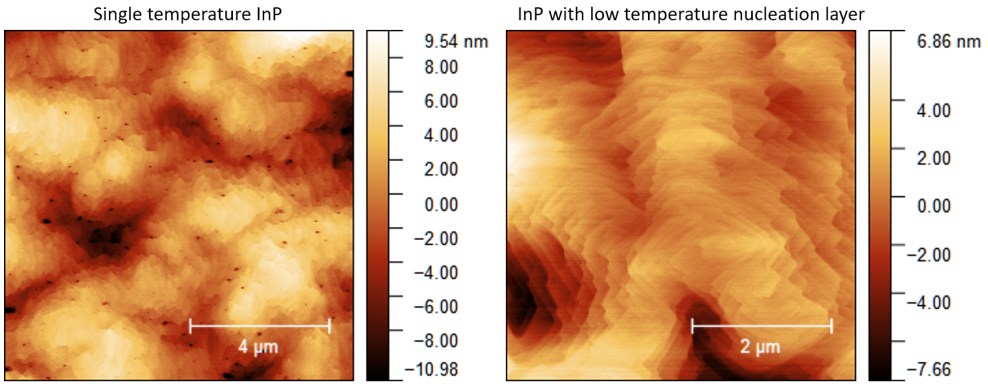

Figure 3.8: AFM images of different InP on InP/Si samples with and without a low-temperature nucleation step. Note the different scale bar.

The threading dislocation density of the pure InP grown on the InP/Si template was $9 \times 10^8 \mathrm{cm}^{-2}$ for the sample with the low-temperature layer. For the sample with no LT layer, the TDD is $7.5 \times 10^8 \mathrm{cm}^{-2}$. The lower TDD for samples with pinholes could be due to dislocations terminating at a pinhole before reaching the surface. However, the effect is quite small and can be neglected. For the following DFL studies, we grow samples of similar thickness to allow for a fair comparison of defect densities.

InAsP epitaxy. An initial attempt of growing a 200 nm InAsP defect filter layer resulted in a very poor surface quality as shown in Fig. 3.9 (a). The DFL was inserted between two 500 nm InP layers grown on the CEA-Leti template. The gas ratio of As/V was set to 5%, aiming for a 5% arsenic incorporation in the solid. The surface was very rough and large pinholes can be observed. The composition of the InAsP layer was approximated using the peak of the photoluminescence emission, as shown in Fig. 3.9. The solid arsenic ratio was found to be ten times that of the gas phase ratio.

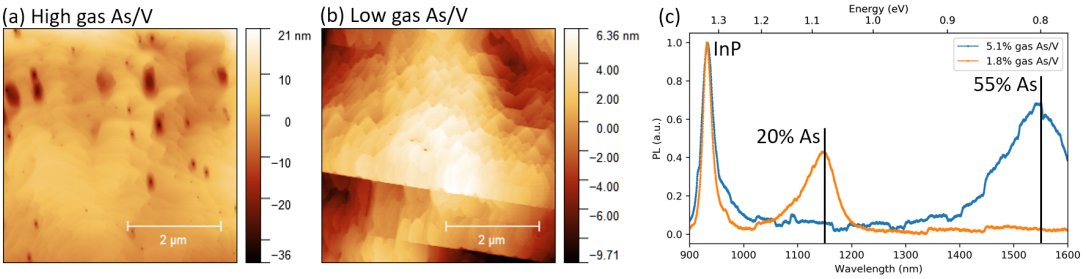

Figure 3.9: As/P incorporation difference in InAsP ternary. (a), (b) AFM images of the high and low As/V defect filter layers showing a rough surface with pinholes and stacking faults respectively. (c) PL comparison between the samples with two gas As/V ratios, showing the solid incorporated arsenic ratios. The sharp corners in the 5.1% As/V curve are stitching artefacts.

The growth of InAsP ternary is made difficult by the difference in incorporation rate of As and P [76], where the incorporation rate of arsenic is much higher than that of phosphorus. The incorporation ratio is also dependent on the temperature, allowing for an additional control parameter. To approach the desired 5% solid arsenic ratio, we set the arsenic flow to the lowest stable value possible in our system resulting in an As/V gas ratio of 1.8%. The solid arsenic ratio is twenty times higher than the gas phase at this low arsenic flow. The resulting surface is smoother and free of large pinholes, shown in Fig. 3.9 (b). The resulting solid arsenic content is around 20%. Further decreasing the solid arsenic content can be done by increasing the P precursor flow or by increasing the growth temperature.

In Fig. 3.9 (c) the InP photoluminescence peak is narrower for the low arsenic ratio sample, showing the increased crystal quality.

DFL material comparison. On the CEA-Leti templates, we grow two samples with a tensile strained $In_{0.95}Ga_{0.05}P$ and a compressively strained $InAs_{0.2}P_{0.8}$ as defect filter layers. The DFLs are grown between two 500 nm InP layers. We compare these two samples with the previously presented InAlAs and InGaAs DFL samples grown

on the Cardiff InP/Si templates. The total thickness is similar across these samples, ensuring a fair comparison. The comparison is shown in Fig. 3.10 All samples show similar surface roughnesses. The samples on CEA-Leti templates still show pinholes as they were grown without LT nucleation layers, however, the impact of pinholes on TDD is negligible.

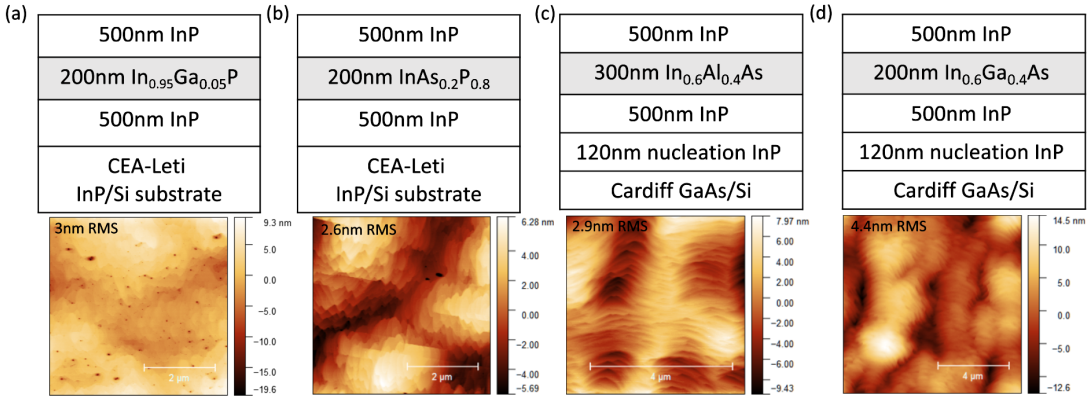

Figure 3.10: Comparison between the different defect filter layer materials, showing a sample diagram and an AFM of the top surface. RMS roughnesses also shown for every sample. The DFL layers are (a) InGaP, (b) InAsP, (c) InAlAs, and (d) InGaAs.

Figure 3.11 shows ECCI images for the two samples grown on the CEA-Leti templates. The TDD for the samples grown on our Cardiff template is estimated using XRD as detailed in the previous section. Compared to the 1200 nm of InP grown on the CEA-Leti template sample with TDD of $9 \times 10^{8}\mathrm{cm}^{-2}$, all the compressively strained defect filter layers show a reduction of dislocations at the surface. The InGaP defect filter layer shows a slight increase in dislocation density at the surface. Assuming the DFL is over its critical thickness, it's possible that the misfit dislocations that are formed are not dense enough to form a network and to significantly reduce the propagating TDD. Then, the additional TDs would come from the top of the DFL layer, which is now mismatched with the top InP layer. Our results contradict previously published studies, where a tensile InGaP DFL has been observed to be as efficient as a compressive

InGaAs DFL [77]. The difference could be due to the lower TDD in the cited paper, as their samples were grown on GaAs substrates.

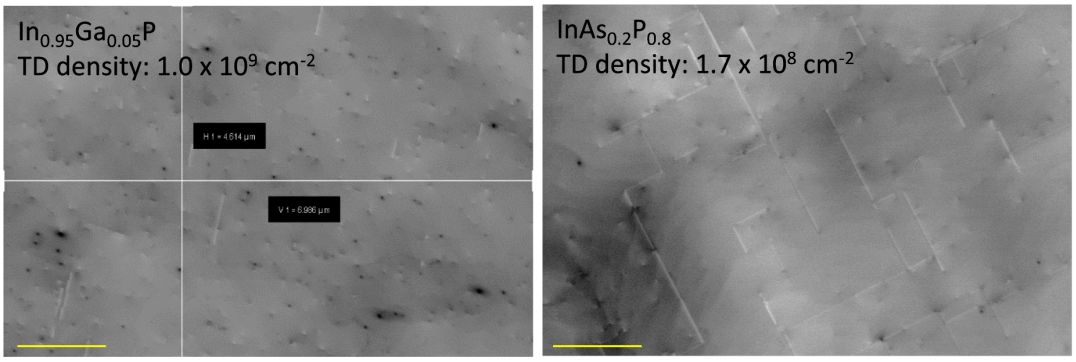

Figure 3.11: ECCI images of the InGaP and InAsP on CEA-Leti template. The threading dislocation densities are also shown. The scale bar is 1 μm**.**

The InAsP DFL shows the smallest roughness and TDD, half that of the InAlAs and InGaAs DFL. This is unexpected, as most DFL found in the literature are InGaAs based [75, 77–79]. InGaAs could be preferred due to its ease of growth compared to InAsP. Compared to the other samples, the ECCI reveals long stacking faults along the surface. It's possible that the partial dislocations of the stacking fault help relax the lattice mismatch, leading to the small TDD observed.

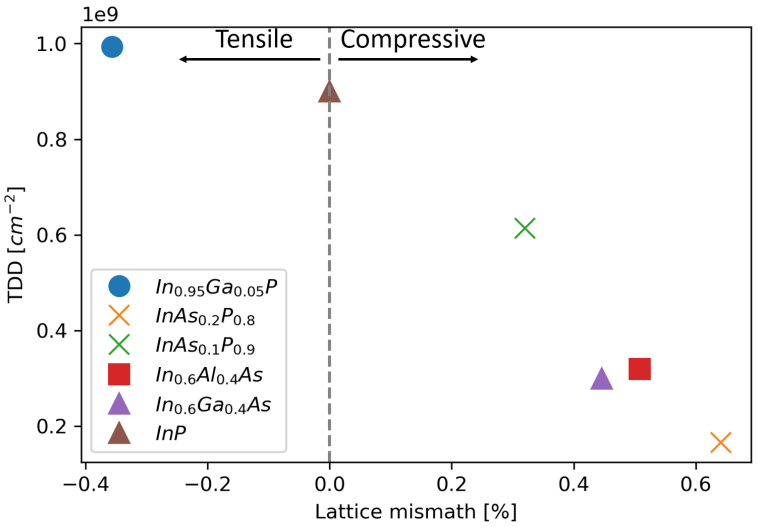

Figure 3.12: Plot of lattice mismatch vs TDD for various DFL materials in comparable samples.

A comparison of the results of the DFL material study is shown in Fig. 3.12. We find a clear trend of TDD decreasing as compressive strain increases. As the strain increases, the larger the network of misfit dislocations must be to accommodate it which increases the likelihood of dislocation annihilation. However, the strain will also generate new threading dislocations. We have not found the optimal stress for our defect filter layers yet, it is possible that increasing the strain could reduce the TDD even more.

InAsP DFL types. We continue to develop defect filter layers based on InAsP, as it has shown the most promising results out of the tested DFL materials. Figure 3.13 shows the two new defect filter layers (b), and (c), compared to the initial InAsP DFL (a). Sample (b) consists of an equivalent strained superlattice consisting of 20 repetitions of 10 nm of InP and 10 nm of $InAs_{0.2}P_{0.8}$ is grown as a DFL. This sample was grown with the same total thickness as the previous samples by reducing the thickness of the final InP layer, and at the same total arsenic content in the DFL. Sample (c) is the same as sample (a) but with a different composition of $InAs_{0.1}P_{0.9}$. The decrease in arsenic was made possible by increasing the TBAs bubbler pressure from 1000 mbar to

1700 mbar which had the effect of halving the arsenic flow while maintaining stability.

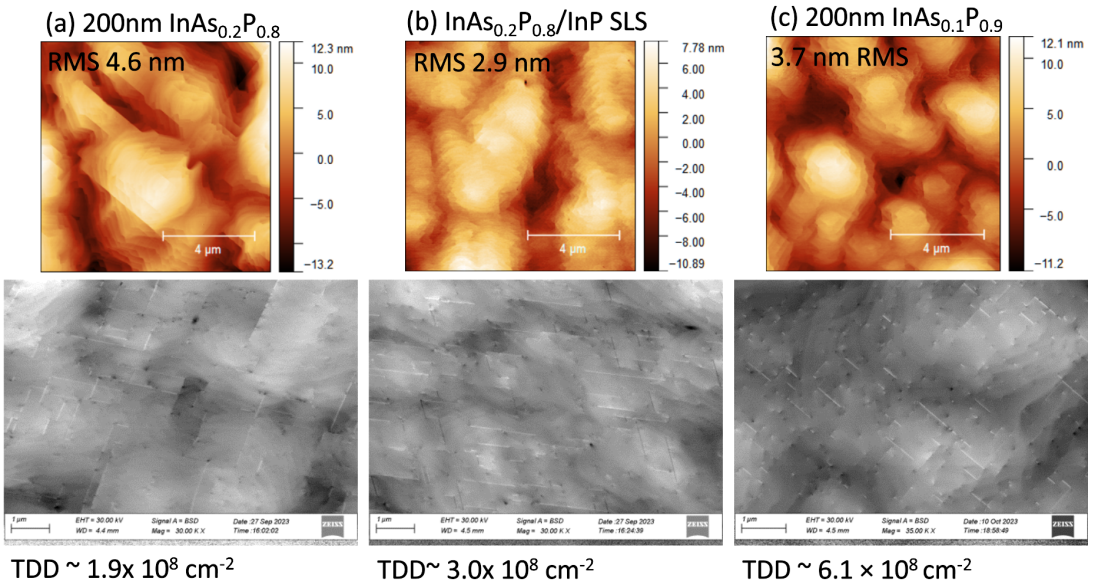

Figure 3.13: AFM and ECCI for different InAsP DFL. (a) $InAs_{0.2}P_{0.8}$ **200** nm **DFL. (b)** $InAs_{0.2}P_{0.8}$ **/** InP **strained superlattice with 20 repetitions of 10** nm**/10** nm **layers. (c)** $InAs_{0.1}P_{0.9}$ **200** nm **DFL .**

The superlattice sample (b) shows a smoother surface than the initial sample, however the TDD is slightly higher. The stacking faults at the surface are shorter and denser. The sample with reduced strain (c) has a yet higher TDD. The initial 300 nm $InAs_{0.2}P_{0.8}$ defect filter layer proves to be the best between these DFL types.

Staking DFLs. To further reduce the TDD, we grow multiple 200 nm $InAs_{0.2}P_{0.8}$ defect filter layers on top of each other. A comparison of one, two, and three DFL layers is shown in Fig. 3.14. Adding an additional layer decreases the TDD to $7.3 \times 10^7 \mathrm{cm}^{-2}$. The stacking faults visible in ECCI appear to be much longer than in the previous sample, and the threading dislocations appear to be clustered together. Adding a third layer does not seem to impact the TDD, remaining at $7.3 \times 10^7 \mathrm{cm}^{-2}$. A possible explanation for this is that the efficiency of the dislocation filter is dependent on

the initial dislocation density. A higher dislocation density will create a denser misfit dislocation network, thus increasing the DFL efficiency.

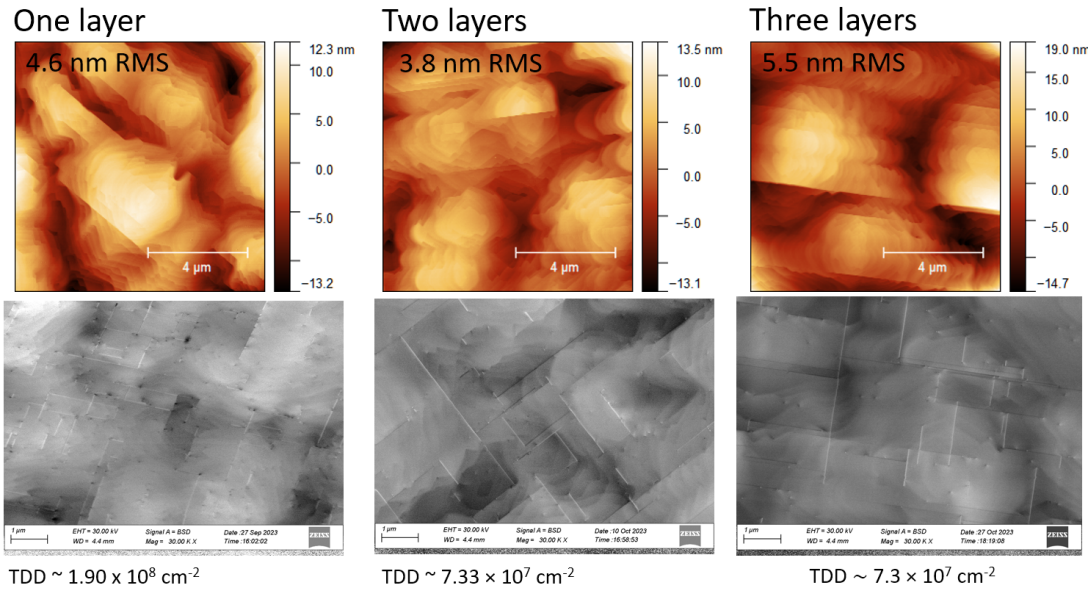

Figure 3.14: Comparison of samples with multiple defect filtering layers. showing one, two, and three 200 nm $InAs_{0.2}P_{0.8}$ **layers. Each sample has a representative AFM and ECCI image, along with the RMS roughness and TDD.**

A summary of all the defect filter layers in this chapter is shown in Fig. 3.15. We have successfully grown defect filter layers with a TDD similar to the best results from literature but with considerably smaller thicknesses using planar unpatterned silicon substrates.

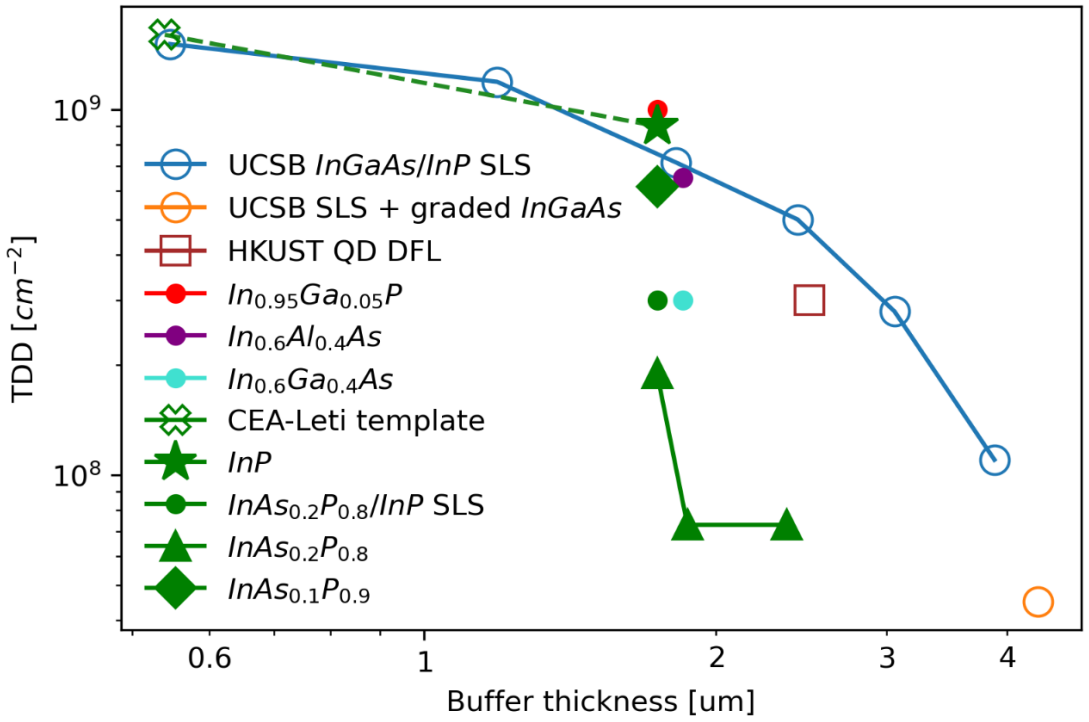

Figure 3.15: Comparison of the defect filter layers described in this chapter, with two results from literature for comparison [73, 75]. Filled markers show samples grown at Cardiff. Green markers show samples grown on the CEA-Leti template.

3.3 InAs/InAlGaAs Quantum dots

Quantum dots (QDs) are nanocrystals a few nanometres in size which confine carriers in all directions. InAs grown on InAlGaAs lattice matched to InP grows in the Stranski-Krastanov (SK) mode. A wetting layer of a few monolayers is first formed called the wetting layer, and then growth continues with island formation. A more detailed description of the SK growth mode is found in the previous Epitaxy section. Since InAs has a lower bandgap than InAlGaAs, carriers are confined within the islands, acting as quantum dots.

Using quantum dots to provide laser gain has many benefits compared to traditional quantum wells. The discrete nature of the energy levels in a quantum dot helps reduce

temperature dependence on the lasing threshold and wavelength [80, 81]. Low lasing thresholds have been observed even on devices grown directly on silicon [82–84].

While QDs are resistant to threading dislocations [85], the presence of TDs in the active gain region induces the creation of dislocation networks through recombination enhanced dislocation climb which degrades device lifetime [86, 87]. Compared to quantum wells, quantum dots still show orders of magnitude higher lifetimes when grown directly on silicon [88]. For InAs/GaAs lasers, laser lifetimes on the order of hundreds of years have been manufactured [89, 90]. Most results are based on InAs/GaAs QDs targetting 1.3 µm lasers. While InP lasers are expected to have an increased resistance to dislocations in the active region [91, 92], results for the lifetime of 1.5 µm QD lasers on InP are as of yet unavailable in the literature.

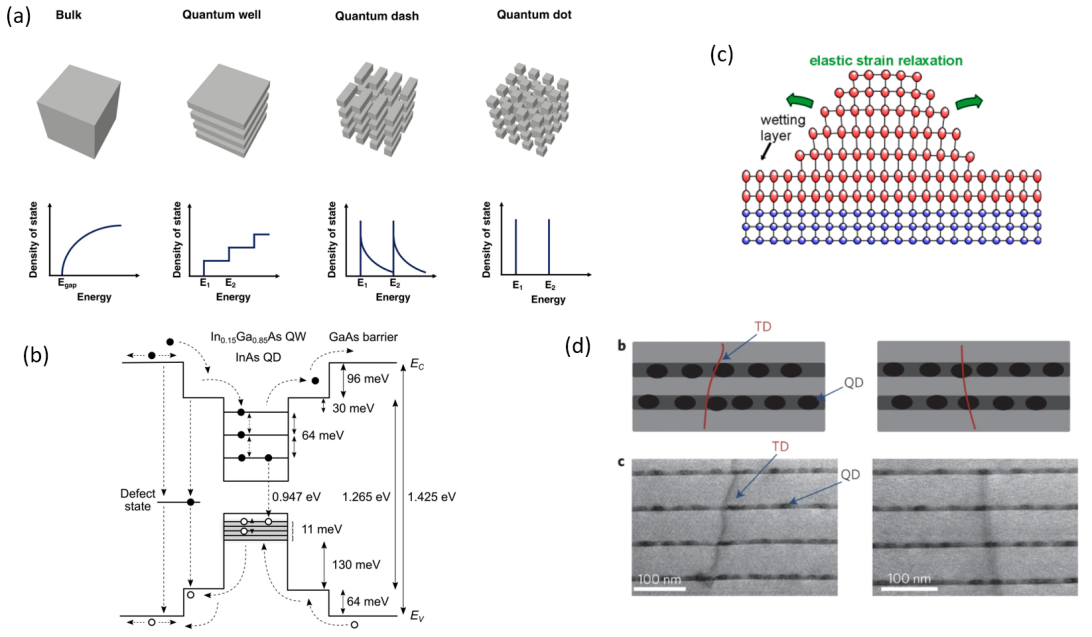

Figure 3.16: QD energy states and defect resistance. (a) Density of states and quantum confinement in multiple dimensions [93]. (b) Real space band diagram for a InAs/GaAs dot in well structure [94] (c) Schematic of a SK quantum dot showing the elastic strain relaxation mechanism [95]. (d) Threading dislocation bending by the strain field around a quantum dot [96] .

Defect resistance mechanisms. Quantum dots are defined by their carrier confinement properties. The density of states for carriers confined in multiple dimensions is shown in Fig. 3.16 (a). A perfect quantum dot will have a delta-function like density of states, similar to electrons in an atom. The strength of confinement is dependent on the size of the dot and the difference in bandgap between the dot and the surrounding material. InAs/InP quantum dots have a height of a few nanometres and diameters of around 30 nm. Since the height is the smallest dimension, it has a much higher influence over the quantum confinement. This is a useful tool when optimizing growth, as it allows us to change the energy of the ground state by changing the height of the dot.

To increase the likelihood of carriers falling into the quantum well of the dots, dots are usually grown inside quantum wells. An example of the band diagram of this dot-in-well structure for InAs/GaAs dots in InGaAs wells is shown in Fig. 3.16 (b). For an InAs/InP QD system, the potential well of the dot will be much shallower, often only allowing for a single electron level. The main carrier transitions are indicated with arrows, showing carriers in bulk falling into well states, and from well into the dot levels. The opposite can happen as well, due to thermal energy carriers can escape dot and well states. This spatial carrier confinement explains one of the ways quantum dots are resistant to threading dislocations [94]. A threading dislocation passing next to a dot will create a mid-bandgap defect state that acts as a nonradiative recombination centre. However, carriers in the quantum dot can not reach the defect state and can only recombine radiatively at the bandgap. Only carriers which escape the dot through thermal energy will be able to fall into the dislocation state. Carriers inside the quantum well can freely recombine through the defect state, however, the existence of the dots inside the well reduces the electron diffusion lengths by an approximated four times [97]. This also reduces the capture radius for the dislocations, thus further limiting the nonradiative loss of carriers.

Growing highly mismatched layers beyond their critical thicknesses results in threading dislocations. However, in the SK growth of quantum dots, the misfit strain energy is

relaxed through lateral expansion of the islands as shown in Fig. 3.16 (c). This elastic deformation results in high strain fields around the dot. The strain field generated is strong enough to pin and bend threading dislocations, as shown in Fig. 3.16 (d). This enables the use of QDs as defect filter layers [73]. It also provides an increased resistance to nonradiative recombination. In a quantum well dislocations can easily move in-plane to accommodate the strain of the QW, however in a dot-in-well structure the dislocations are pinned by the dots. Because of this, a dislocation will interact with at most a single dot.

QD epitaxy. We use quantum dots as gain medium to take advantage of their resistance to threading dislocations. We grow the QD samples at the same time by placing both an InP and an InP/Si Cardiff template in the reactor to ensure no run-to-run variations. Growth begins with a 320 nm InP buffer. A thin strained interlayer of 2 nm $In_{0.4}Ga_{0.6}As$ is grown next. The strain affects the surface energy which modifies the shape and density of the dots as the SK growth mode is dependent on surface energy. The QDs are grown at a very small flow rate, with a V/III ratio of 0.9 at a temperature of 475$^{\circ}\mathrm{C}$. The indium flow is stopped for 30 seconds to give the dots time to self assemble. For AFM study, a set of samples is taken out of the reactor at this step. For photoluminescence study, another set of samples is grown similarly and growth continues with a capping layer. The first low-temperature capping layer consists of 2nm InP. The purpose of this layer is to protect the dots from desorption at higher temperatures. The temperature is then increased to 600$^{\circ}\mathrm{C}$ for the second capping layer of 40nm InP. The QD structure is repeated three times to increase gain. This structure is shown in Fig. 3.17 (a).

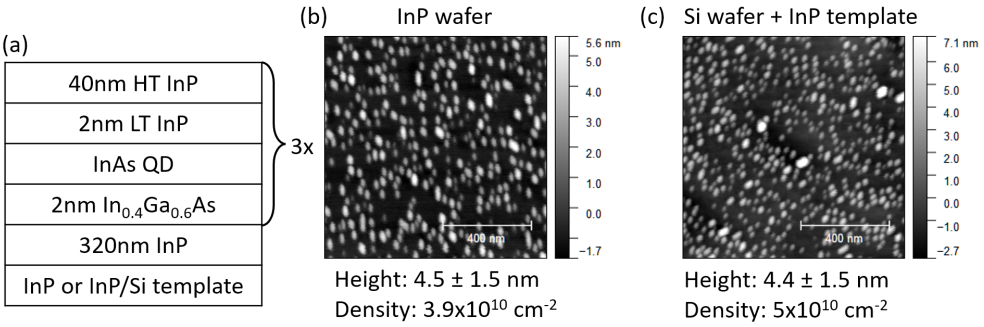

Figure 3.17: QDs grown on InP and InP/Si templates. (a) Layer diagram of the QD samples. (b) and (c) AFM images of the first QD layer before the capping layer is grown for the InP and InP/Si sample, respectively..

QDs are observed on the surface as shown in Fig. 3.17 (b) and (c). The dots are uniform on both the InP and InP/Si, having the same height and height distribution width. The densities are high, similar to those of InP/GaAs QDs [98]. Interestingly, the density is higher on the Si template sample. This is likely because the higher surface roughness creates more monolayer edges, which provide more nucleation sites for dots.

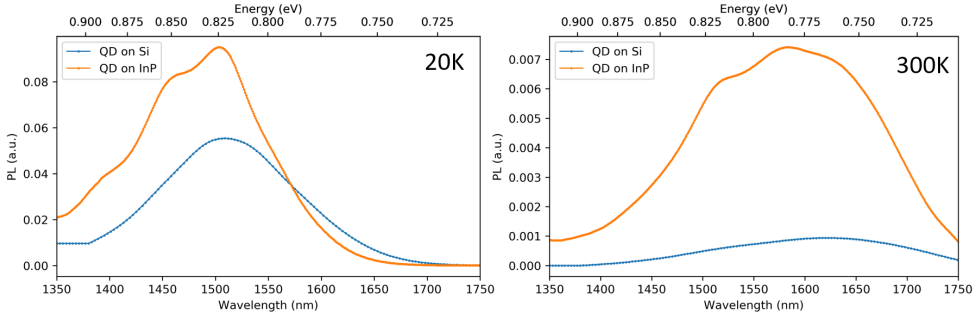

Figure 3.18: PL comparison between QDs on InP and Si wafers at low and high temperature.

At low temperature, the QDs on InP are approximately twice as bright as those on the Si template. The ratio drastically decreases as the temperature increases. These measurements are taken at very low pumping powers on the order of 1 $\mathrm{W\,cm^{-2}}$, ensuring that the threading dislocation states are not saturated. At low temperature the electrons

confined in the dots do not have sufficient thermal energy to jump into the well state, increasing the localization of carriers. The increased spatial confinement limits the interaction between electrons and threading dislocation states.

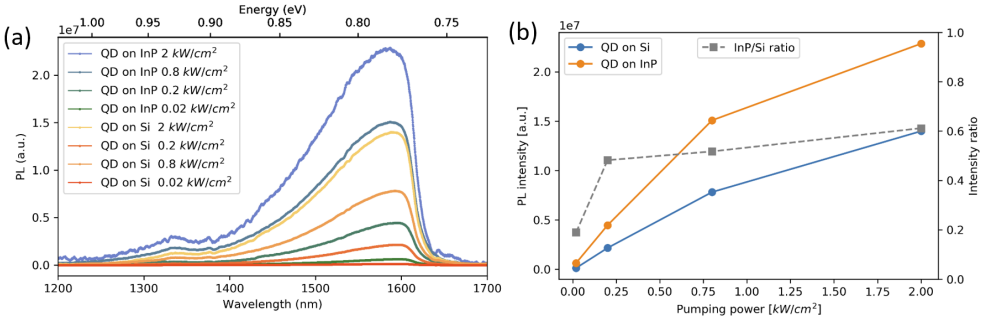

Figure 3.19: Room temperature QD pumping power study comparing samples on InP and Si. (a) PL spectra at various pumping powers. (b) PL brightness comparison with the ratio between samples indicated.

A power-dependent room temperature PL study is shown in Fig. 3.19. At high pumping powers, the brightness ratio between samples on InP and Si substrates is around 50%, similar to the low-temperature scenario. This is because the pumping power is high enough to saturate the dislocation states, despite the high likelihood of carrier escape. The ratio is roughly constant for sufficiently high pumping power. At lower power, the ratio drastically decreases, suggesting that the saturation pumping power is around 0.2 $\mathrm{kW\,cm^{-2}}$.

QD desorption. The previous spectra shown in Fig. 3.18 show that the peak emission wavelength is lower than the targeted 1550 nm. There are many methods to blueshift QDs, such as lowering dot height or increasing the confining potential energy. Dot height can be reduced by decreasing growth time, but this also decreases the QD density, leading to lower gain. The increase in confinement energy can be achieved by increasing the gallium content in the InGaAs interlayer. From previous calibration samples (not included here) the increase in gallium content also has the effect of

increasing the surface energy, promoting the growth of smaller, denser dots. Unfortunately, it also has the effect of broadening the dot size distribution, and the PL emission peak.

In MBE-grown QDs a common method to blueshift the emission while keeping the dot height uniform is indium flush [99]. This technique makes use of a similar low-temperature capping layer to protect the smaller dots, while the larger dots remain exposed. Increasing the temperature will promote the desorption of the uncovered dots, thus culling the dot distribution. There are reports of this technique being successfully used in MOCVD [100]; however, we were unable to replicate these results in our reactor.

We found success by turning the all precursor flow off during the growth interruption, before the growth of the LT capping layer. During the growth interruption, the dots self assemble into their stable island shapes. MOCVD growth is typically done using group V overpressure to minimise desorption from the surface. By turning off the group V source, we allow the adatoms on the surface to freely desorb given the high temperature. A growth diagram is shown in Fig. 3.20

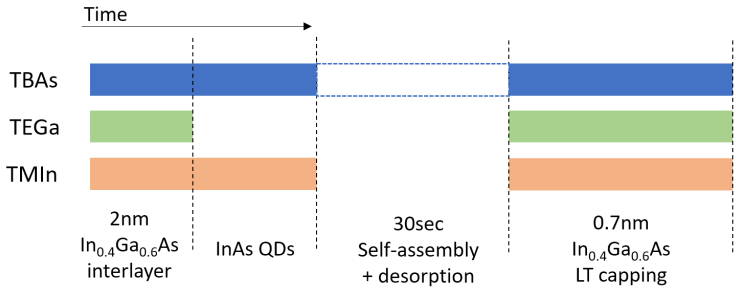

Figure 3.20: Flow diagram of the QD desorption process

This growth interruption without arsenic process has a significant effect on the self-assembly process. It results in the preferential desorption of smaller dots as their surface binding energies are smaller. The desorbed species can be desorbed reabsorbed onto the surface multiple times, until settling on a stable dot.

A new set of QD samples is grown, with and without arsenic in the growth interruption. Both samples are grown on InP wafers. Growth begins with a 500 nm InP buffer, followed by a 600 nm InAlGaAs layer lattice matched to InP with a 50/50 Al/Ga ratio grown at 580°C. The quaternary buffer layer offers a higher refractive index, which increases the optical confinement of the final laser structure. The interlayer is made of 2 nm $In_{0.4}Ga_{0.6}As$. The QDs are grown at 460°C with a V/III ratio of 0.9. The group III precursor flow is closed for 30 seconds during the growth interruption step. For the desorbed sample, the arsenic flow is also closed. Then the 0.7 nm low-temperature $In_{0.4}Ga_{0.6}As$ capping layer is grown. The temperature is ramped up over 5 minutes back to the quaternary growth temperature. The high-temperature capping layer consists of 40 nm InAlGaAs. Samples used for AFM inspection were taken out of the reactor after the growth interruption step.

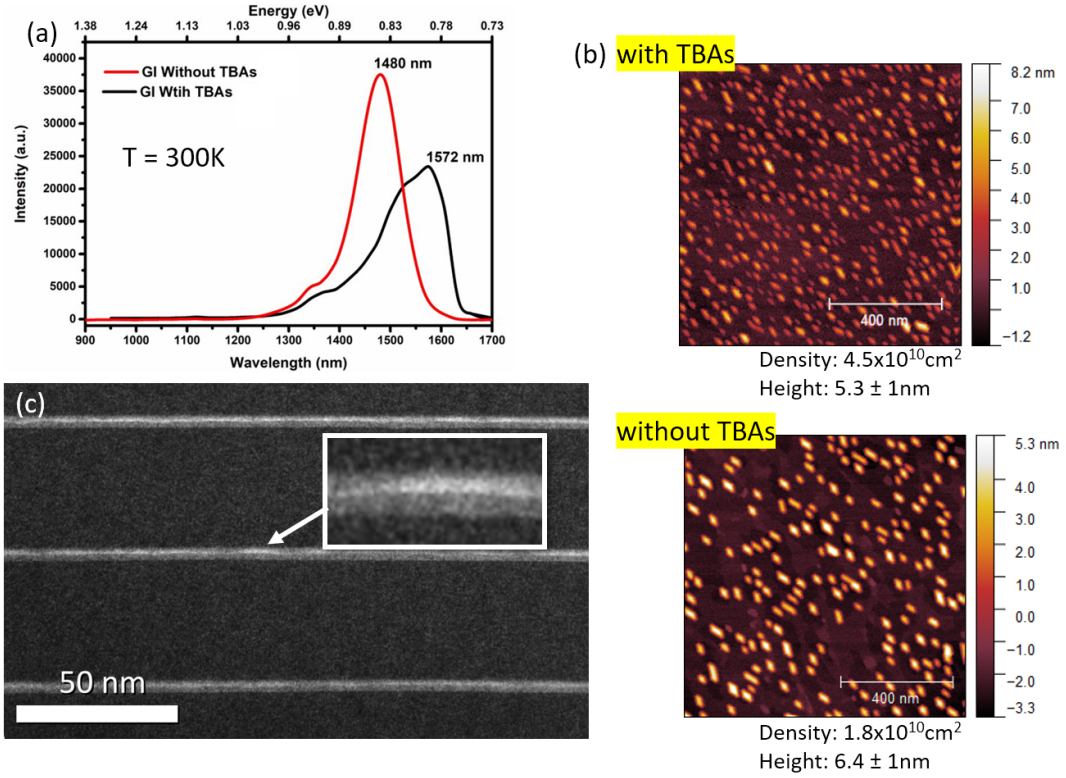

Figure 3.21: Characterization of desorbed QDs. (a) PL comparison between samples with and without arsenic flow during the growth interruption (GI). (b) AFM images comparing samples with and without arsenic during the GI. Dot density and height are labelled for each sample. (c) TEM image of the sample without arsenic during the GI.

A room temperature photoluminescence comparison reveals that the blueshift goal was successful, shown in Fig. 3.21 (a). The desorbed sample was blue-shifted approximately 100 nm. Moreover, the peak is narrower and brighter, indicating the dot heights are more uniform. The small peak at around 1300 nm is attributed to recombinations from the quantum well state. The influence of the desorption step on the dot shape can be seen in the AFM figures shown in Fig. 3.21 (b). The dot density decreases in the sample with no arsenic during the GI as a result of the desorption of smaller QDs. The height increases slightly, however the height variance remains similar. Since the uniformity is similar, we expect a similar width of the emission peak, but this is not

the case. In the cross-sectional TEM image shown in Fig. 3.21 (c), the dots are not well-defined. Small dots of roughly 2 nm in height can be seen. However, they are sparse and diffuse, making the resulting structure resemble a roughened quantum well more than individual quantum dots. This could explain why the PL peak is narrower despite the dot height variance being similar. The high-quality dots seen on AFM before capping seem to disappear and diffuse into the surrounding InGaAs cladding. The most likely issue is that the capping layer does not adequately protect the dots during the temperature ramp up.

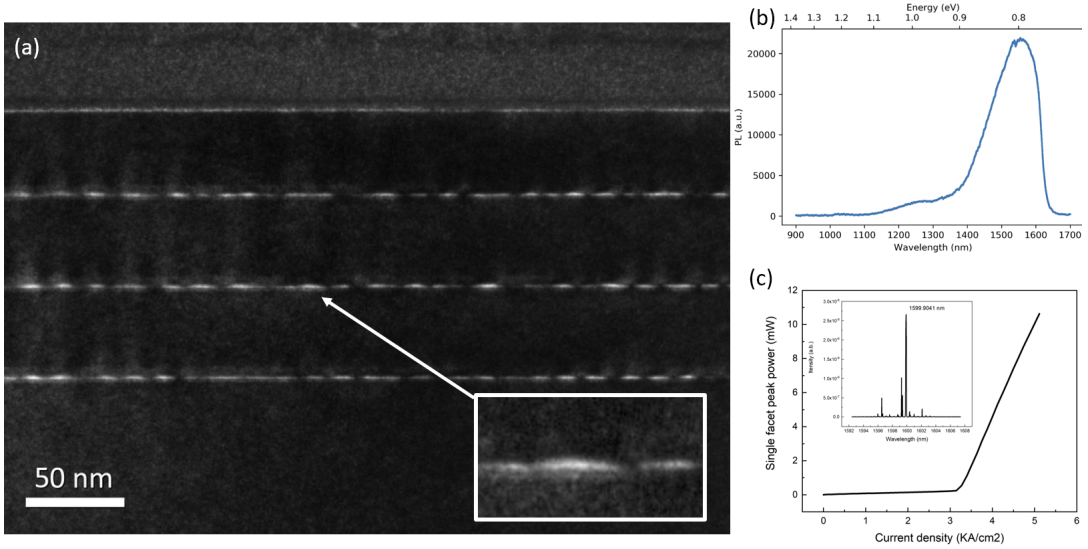

Figure 3.22: Optimized desorbed QDs and laser results. (a) TEM image of the optimised desorbed QDs. (b) Photoluminescence of the optimised QD. (c) Spectrum and power curve of an electrically driven ridge laser using optimised QDs.

A series of optimisations were done on the desorbed QD sample to improve dot definition and confinement after the capping procedure. The InP buffer thickness was lowered to 200 nm. The InAlGaAs buffer thickness was lowered to 240 nm. The thickness of these buffers shouldn't impact the dots, they were reduced to preserve precursors. The InGaAs interlayer and low-temperature capping layer was changed from 40% to 35% indium composition. The LT InGaAs layer thickness was increased from 0.7 nm to 4 nm to better protect the dots during the temperature ramp up. The

high temperature InAlGaAs layer was changed from 590°C to 550°C to decrease the diffusion of the dots into the InGaAs cladding. The whole QD structure is repeated three times.

The improvement in dot lateral confinement is shown in the TEM image, Fig. 3.22 (a). The dots have sharper edges and a clear spatial separation. Unfortunately, the increase in the InGaAs LT capping layer thickness leads to an increase in average QD height, thus red-shifting the emission peak. Figure 3.22 (b) shows the photoluminescence spectrum of this optimised sample. The PL peak width is larger, as expected of self-assembled quantum dots. The peak gain is at around 1600 nm, slightly longer than the targetted 1550 nm.

We collaborated with another group at Cardiff University to fabricate electrically driven ridge lasers using the optimized quantum dot material. For a 0.66 mm cavity length laser, the threshold current density under pulsed pumping is around 3 $\mathrm{kA\,cm^{-2}}$. The emission peak is at 1600 nm as defined by the gain spectrum. These results prove the quality of our quantum dot material, which can provide sufficient gain for electrically pumped lasers.

Pocket epitaxy. While it is possible to overcome the height difference between a thick buffer and the waveguide by using gratings to direct the laser beam downwards [101, 102], for a photonic circuit strong evanescent coupling would be ideal. Using elective area epitaxy, it is possible to grow a thick buffer inside an etched pocket on an SOI wafer to allow sufficient space for the defect trapping layers. A structure based on our DFL and QD results is presented in Fig. 3.23. The QD active region is placed inside an InAlGaAs waveguide for optical confinement of the mode. Using this technique it is possible to epitaxially vertically align the gain region and the confined mode with the waveguide, increasing the coupling coefficient.

Initial work on this was done, but due to issues with the pocket fabrication related to the roughness of the initial growth surface and insufficient masking of the silicon

waveguide facet we were unable to grow smooth III-V inside the cavity. Future work can be done to improve the quality of the fabricated patterns by optimizing the etching and mask deposition steps.

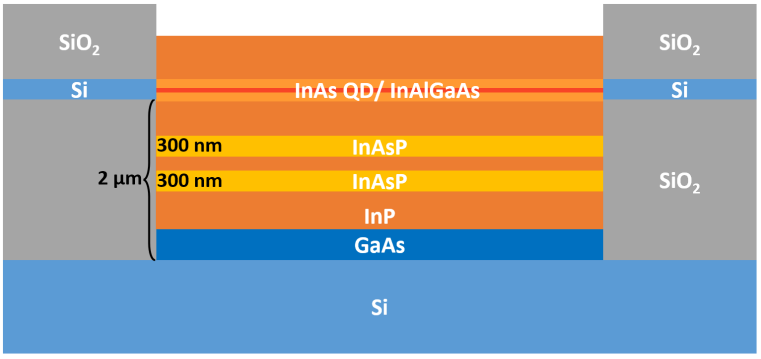

Figure 3.23: Schematic showing an in-pocket laser structure using InAs QDs and InAsP DFL for silicon photonics integration on SOI.

3.3.1 Contributions

Significant contributions to the work presented in this chapter have been made by a number of people. Dr. Qiang Li, Dr. Oumaima Abouzaid and Dr. Pradeep Siddham, Dr. Parco Wong, and Dr. Shangfeng Liu helped with sample growth by operating the MOCVD reactor for many of the samples presented. Dr. Hui Jia and other University College London collaborators measured the XRD and ECCI results shown in this chapter. Some of the InP/Si buffer templates were grown and provided by CEA-Leti. Dr. Hui Jia also assisted in measuring the low temperature PL of the QD samples. Prof. Richard Beanland measured the cross-sectional TEM of the QD sample. Analysis of the data measured by others was done by the author, as well as all work not highlighted here.

Chapter 4

Nanowires

Nanowires are structures with diameter on the scale of nanometres and potentially unlimited length. They can be made from many materials (metals, semiconductors, oxides, etc.) and grown on many substrates (silicon, tungsten, compound semiconductors, corn [103], etc.). Nanowires made of arsenide and phosphide semiconductors grown on silicon are of particular interest for this thesis.

For heteroepitaxial integration, nanowires provide one unique benefit in that they can be grown completely threading dislocation free. This is a great promise but it comes with substantial challenges. Nanowires are limited in size, making it impossible to build traditional laser structures using them. Moreover, electrically pumping nanowires is particularly challenging, since the metal contacts will need to be placed in close proximity with the resonator, considerably degrading the Q factor.

4.1 Review of III-V on Si nanowire epitaxy

Two main growth methods are used to grow nanowires on silicon: vapour-liquid-solid (VLS) and vapour-solid (VS). The VS mechanism incorporates adatoms directly from the gas phase, whereas the VLS method uses a metallic droplet to collect adatoms from the gas phase with a much higher absorption rate. Each method has various pros and cons. Some relevant differences between the two modes are shown in Table 4.1.

Table 4.1: A comparison of some of the relevant differences between VS and VLS nanowire growth [104].

	Vapour-solid	**Vapour-liquid-solid**
Aspect ratio	Lower aspect ratio	High aspect ratio
Heterostructures	Radial structures possible, difficulty with axial structures	Good control of lateral and radial structures
Shape control	Only hexagonal pillar shape possible	Lateral growth possible, tapered shapes possible
Shape uniformity	Very high size and shape uniformity	Size and shape non-uniformity
Nanowire placement	Arbitrary, defined by e-beam patterned SAE	Random nanowire placement, SAE possible but difficult
CMOS compatible	Use of (111)Si substrates, difficulty in using (001)Si	Au seed incompatible with CMOS
SiPh compatible	SiPh compatible	Needs pick and place to integrate with SiPh
InGaAs growth	InGaAs growth possible for low In composition	InGaAs difficult to grow by self catalized growth on Si
Material uniformity	Ternary compounds almost perfectly uniform	Ternary compounds very non-uniform

VLS has much higher control over the crystal growth rates, both axially and radially. This allows the growth of very long nanowires of up to tens of microns before the critical plastic deformation point is reached. A theoretical model of the critical height vs nanowire diameter for various mismatch values is shown in Fig. 4.1 (d). Additionally, it is possible to easily create radial structures such as thin quantum wells. By varying the growth parameters during growth it is possible to increase or decrease radial growth rate creating needle like shapes. It is even possible to completely change growth direction, nucleating new nanowires that grow laterally [105]. VLS growth typically uses randomly positioned catalysts leading to randomly positioned nanowires. Selective area growth can be used to deterministically place the catalysts. However, the yield tends to be too low for photonic crystal applications. Higher yield growth is possible on native substrates, but using silicon substrates further decreases the yield. The issue in deterministically placing the NWs makes them difficult to use for silicon photonics. Most SiPh devices using nanowires use a pick and place technique to transfer the nanowire onto the device. The VLS process is not very compatible with CMOS as the typically used gold catalysts can create contamination resulting in deep level traps in silicon. Newer methods use self seeded growth by employing indium or gallium catalyst droplets, which cause less damaging contamination [106]. Growing ternary semiconductors using VLS can result in non-uniform nanowires. For InGaAs, indium incorporation rates are different for VS and VLS growth, however it's impossible to

completely suppress VS growth resulting in a low indium concentration shell around the wire, as shown in Fig. 4.1 (e).

Vapour-solid nanowires are typically grown using selective area epitaxy and do not use a metallic catalyst. Holes are etched into the growth mask to uncover the substrate underneath, where the nanowire can nucleate. High growth temperatures are required to ensure that no nucleation happens on the mask itself, which limits the growth parameter window. VS nanowires have much faster lateral growth rates than VLS, meaning that the maximum heights are on the order of a few microns. Both radial and axial heterostructures have been demonstrated [107], but it is difficult to grow exclusively only one type of heterostructure. The yield and uniformity can approach perfect values for very well tuned growth parameters, making them perfect for photonic crystal applications. The difference between self assembled and selective area growth uniformity and crystal quality can be seen in Fig. 4.1 (a). A SAE GaN nanowire photonic crystal is shown in Fig. 4.1 (c). Integration with silicon photonics passive devices has been demonstrated [108]. Typically, VS nanowires are grown on (111) oriented silicon substrates, which are not compatible with CMOS processes. A method of using (001 wafers) has been demonstrated [109]. It uses (111) angled waveguides etched into (001) wafers, which could solve the CMOS compatibility issues. However, the high growth temperature requirement can still be an obstacle to CMOS integration. The material uniformity is reasonably high for InGaAs nanowires. Indium incorporation is lower at high order facets, which creates a slight non uniformity of a few percent points. The maximum indium composition is lower compared to VLS, as higher indium flow leads to high lateral growth rates in VS growth.

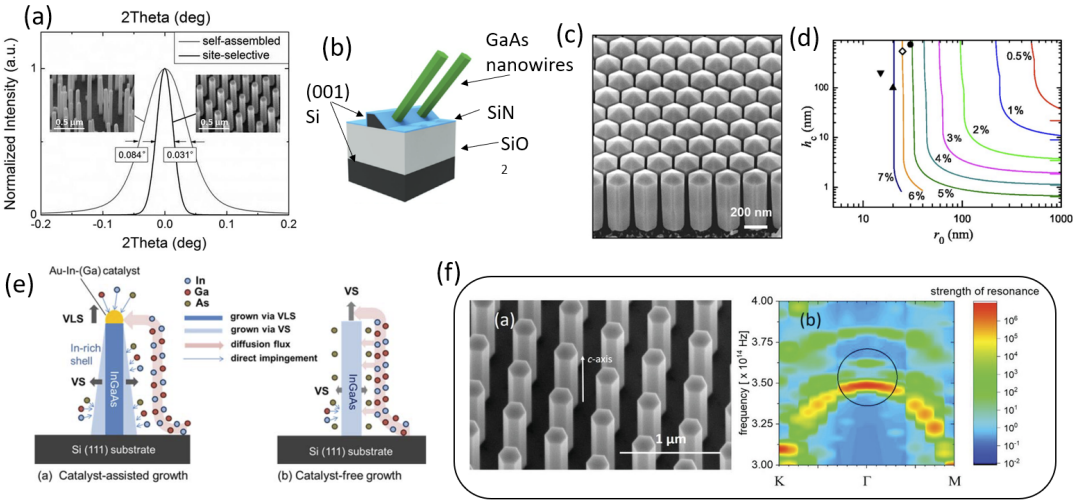

Figure 4.1: Selected relevant results in photonic crystal vapour-solid nanowires. (a) Comparison of XRD peaks showing the increased crystal quality of SAE nanowires [110]. (b) Integration of GaAs nanowires on a (001)Si wafer waveguide for silicon photonics applications [111]. (c) Electrically pumped GaN nanowire photonic crystal surface emitting laser [112]. (d) Critical thickness of nanowires as a function of radius for different mismatch values [52]. (e) Schematic representation of VLS and VS growth mechanisms [104]. (f) Vertically emitting InP nanowire based photonic crystal laser and its band structure around the Γ point [113].

Photonic crystals. A photonic crystal is a medium with periodic changes in refractive index. If the period of the crystal is close to the wavelength of light propagating to it, the light will experience strong wavelength dependent dispersion due to repeated reflections interfering with themselves. The mechanism of repeated reflections is mathematically similar to that of electrons in a crystal lattice, the main difference being that photons are bosons, unlike electrons, so effects like band transitions or band filling do not occur. Selective area nanowires are especially well suited to photonic crystal applications due to their small size and positioning accuracy. Examples of nanowire photonic crystals are shown in Fig. 4.1 (c) and (f) showing a triangular and square

lattice respectively.

The dispersion relationships in a photonic crystal are typically presented as a band diagram, showing the resonant frequencies as a function of the E field k vector. For two-dimensional photonic crystals, the k vectors of interest lie along high symmetry directions and are typically labelled K, Γ, M, X. The K, X and M points are directed in plane, while the Γ point represents standing waves with $k = 0$. The notation convention is different for square and triangular symmetries, which use X and K respectively. A photon at a frequency and momentum matching one of the band edges will be reflected strongly by the photonic crystal. If such a photon originates from inside the crystal, for example one emitted through photoluminescence, it will become trapped inside the crystal creating a very high Q factor resonant cavity. A photon not matching a photonic band will be quickly scattered out of the cavity.

The slope of the band edges defines the group velocity of the mode. At flat band edges the group velocity becomes zero which increases the interaction time between the field and the gain material, thus increasing gain. Having a flat band edge at the Γ point is favourable for surface emitting lasers and can be achieved using triangular, square or honeycomb patterns. An example of an experimentally measured band gap of a surface emitting laser, with a flat Γ point band edge, is shown in Fig. 4.1 (f).

Photonic crystal lasers have demonstrated better performance compared to traditional edge emitting lasers and VCSELs in terms of threshold current, brightness, and beam divergence [114–118]. Photonic crystal lasers on silicon platforms have conventionally been fabricated using wafer bonding or similar layer transfer methods, followed by a top-down etch to define the patterns [119, 120]. These methods can provide very high quality III-V active regions; however, there are issues with sidewall surface scattering and passivation. Nanowires provide an attractive solution as they bypass the lattice matching requirement of planar heteroepitaxy, while defining the cavity in a single growth step. Nanowires show atomically smooth surfaces and passivation is easily achieved in-situ by growing a core-shell structure.

Photonic crystals resonators have been used to experimentally demonstrate cavities with Q factor on the order of 10^7 [121].

4.2 Nanowire growth and characterization

Growth and methods. The nanowires are grown using our CCS Aixtron MOCVD reactor. Starting with an SOI wafer with a 40nm $(1\,1\,1)$ oriented silicon wafer. The silicon layer is intentionally thin to stop the photonic crystal mode from leaking into the silicon. A 20 nm SiN layer is deposited using plasma enhances chemical vapour deposition to act as a growth mask. Electron beam lithography was used to etch circular nanoholes into the SiN layer to expose the silicon surface. The nanoholes were as small as 30 nm, and positioned to create various honeycomb photonic crystal patterns. The nanoholes are shown in Fig. 4.2 (a). The sample is cleaned before growth using a dilute 2.5% hydrofluoric acid to remove the native silicon oxide, then the sample is placed in the reactor. The sample is smaller than the 2 inch susceptor pocket, the rest of the pocket was filled with dummy sapphire wafers to protect the susceptor and maintain the uniform gas flow. The growth starts with a 20 minute, 850 $^\circ\mathrm{C}$ annealing in a 50 mbar hydrogen atmosphere to desorb any remaining oxide traces on the surface. The precursors used for nanowire growth are triethylgallium, trimethylindium, tertiarybutylarsine, and tertiarybutylphosphine. Growth starts with a GaAs core at 680 $^\circ\mathrm{C}$ and a V/III ratio of 82. The next step is growing InGaAs at 610 $^\circ\mathrm{C}$ with a V/III ratio of 40 and an In/III ratio of 40%. Finally, a 15 nm InGaP shell is grown at 570 $^\circ\mathrm{C}$.

The best honeycomb sample also used a flow modulated epitaxy step after the GaAs core. The III-precursor flow was looped on for 20 seconds and off for 40 seconds for a total of 15 iterations. The resulting nanowire honeycomb arrays can be seen in Fig. 4.2 (e). The sample presented for the curved array chapter did not use flow modulated epitaxy, and used a much smaller GaAs core. All other growth parameters are the same.

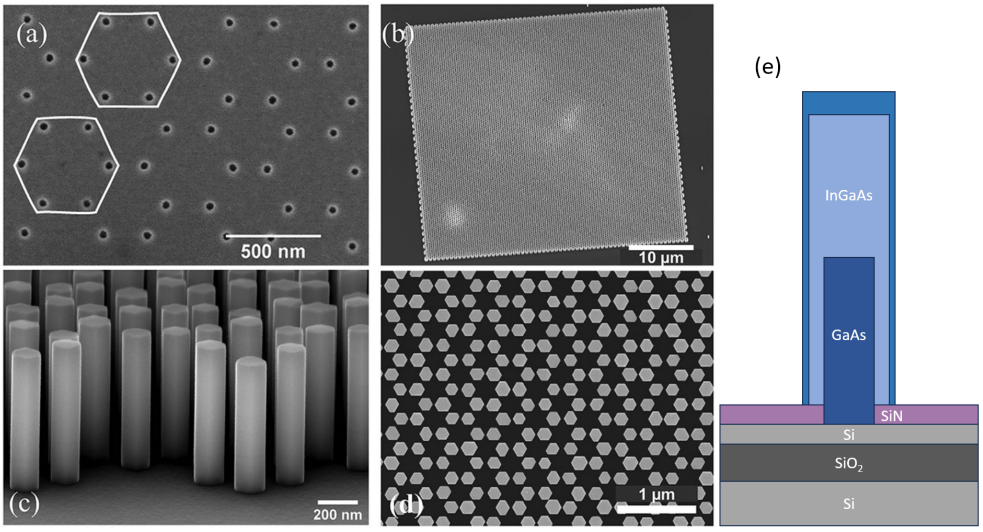

Figure 4.2: SEM images of the nanowire honeycomb pattern and structure. (a) Top-view SEM image of the initial nanohole array. (b) Tilted view SEM image of a 40 × 40 μm nanowire array. (c) Zoom-in tilted view SEM image of the nanowires. (d) Top view SEM image showing the hexagonal cross-sections of the nanowires..

Following the selective area epitaxy steps, an almost 100% yield was achieved for honeycomb nanowire arrays as large as 60 × 60 μm^2 with good uniformity. The SEM images of the nanowire arrays in Fig. 4.2 show the high yield and uniformity of a 40 × 40 μm^2 array. From SEM images, the height and diameter of the nanowires are measured to be 630 $\pm$ 10 and 163 $\pm$ 8 nm, respectively.

Material analysis. To check that the intended nanowire growth structure was successful, transmission electron microscopy and energy (TEM) dispersive x-ray spectroscopy (EDX) were used. Two TEM samples were prepared. The first sample was cut into a thin lamella using a focused ion beam. This was used to study the Si/GaAs interface and to take atomic resolution images of the material. The second sample was intentionally scratched to detach the nanowires. Then the nanowires were transferred to a TEM grid for imaging. This was used to measure side views of the whole nanowire at once. The images were taken with a scanning tunnelling electron microscope using

high-angle annular dark field detector (STEM-HAADF).

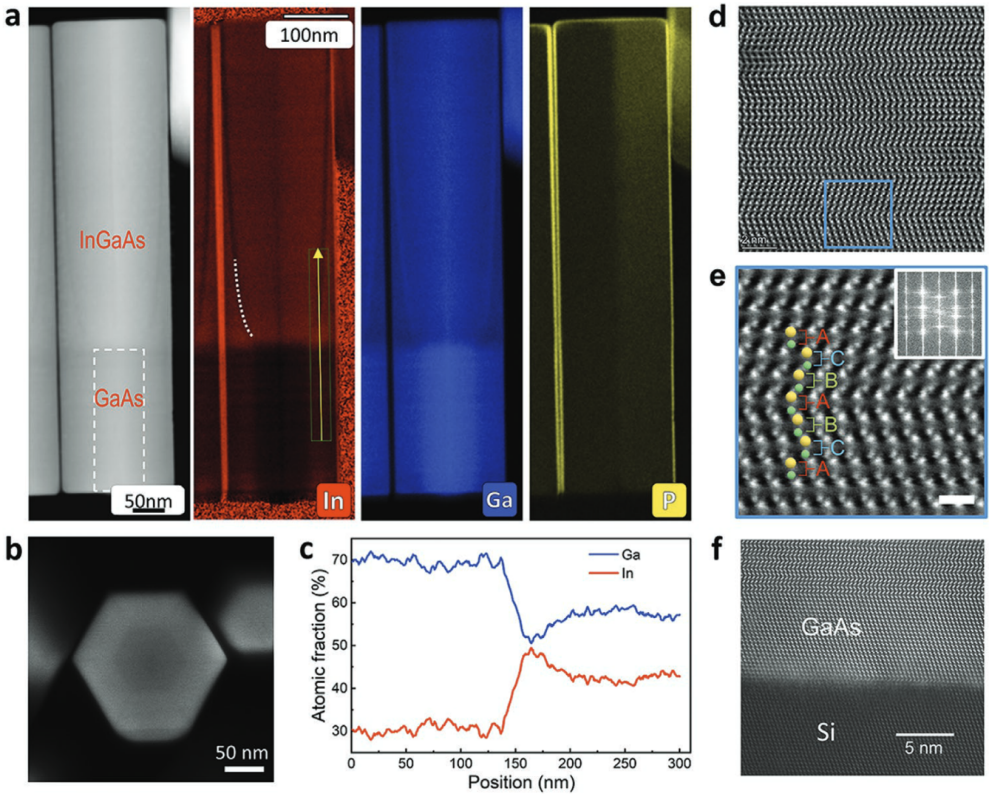

Figure 4.3: TEM characterization. (a)STEM-HAADF image taken in the $\langle 1\,1\,2 \rangle$ direction and EDX elemental maps. (b) STEM-HAADF image viewed at the nanowire base. (c) Line profile of the In and Ga composition from EDX at the InGaAs shell. The scanned region is indicated by the yellow arrow in the In map in (a). (d) STEM-HAADF image acquired in the$\langle 1\,1\,0 \rangle$ direction at the InGaAs region of the nanowire. (e) Magnified image of the blue box in (d) showing a microtwin. Scale bar, 1 nm. The yellow sphere represents group III atoms and green represents As atoms. The inset shows an FFT image of the nanowire. (f) STEM-HAADF image acquired in $\langle 110 \rangle$ zone axis at the Si/GaAs interface.

Figure 4.3 shows the main findings of the TEM study. The side view EDX in (a) and (b) shows the intended nanowire structure was successfully grown. The GaAs seed is clearly visible in the STEM and the In and Ga EDX maps. The top of the nanowire is

shown to have an uniform InGaAs composition. InGaAs grown laterally from the GaAs seed is uniform, but has a different composition from the top InGaAs. The indium incorporation is different in radial and axial growth. This results in a composition of around 30% In for laterally grown material and 45% for vertically grown material, shown in Fig.4.3 (c) as a line scan in the direction of the arrow in the indium EDX map. A difference in incorporation rate can also be seen at the corners of the wire. The dotted line in the indium EDX, Fig. 4.3 (a), shows a dark trail left behind by the corner as it grew vertically and laterally. The dark trail implies a significantly lower indium incorporation at the high order facets found at the corner of the wire. This effect has been reported in other similar selectively grown structures [122, 123]. The InGaP shell is shown in the phosphide EDX map uniformly covering the whole nanowire.

The nanowire structure has very dense micro twins and stacking faults, shown in Fig. 4.3 (d) and (e). The ABCABC stacking sequence is disrupted, showing ABCBA for twins or ABCBCA for stacking faults. The high density of these defects has an effect on the diffraction pattern, shown in the inset, adding additional vertical diffraction lines over the crystalline diffraction pattern. The crystalline diffraction pattern also overlays the diffraction from both the normal and twinned crystal phases. Stacking faults and twin boundaries are not charged defects, nor do they act as nonradiative recombination centres. The stacking faults terminate at the surface of the nanowire, which means that there are no partial dislocations inside the wire. However, stacking faults do influence the local electronic band structure, creating small quantum wells that can trap carriers and decrease the electrical conductivity [124]. A proposed mechanism for the creation of these stacking faults is the lowered fault nucleation energy at the edges of the wire due to a difference in atomic bond length, for flat top nanowires [125]. Another proposed mechanism is the lowered stacking fault nucleation energy for triangle-topped nanowires [126, 127]. Once nucleated, twins will self-replicate due to the attractive interactions mediated by surface strain [128]. The GaAs/Si interface shows $7\mathrm{nm}$ defect free crystal. No threading dislocations were observed in any of the TEM images.

4.3 Nanowire honeycomb photonic crystals

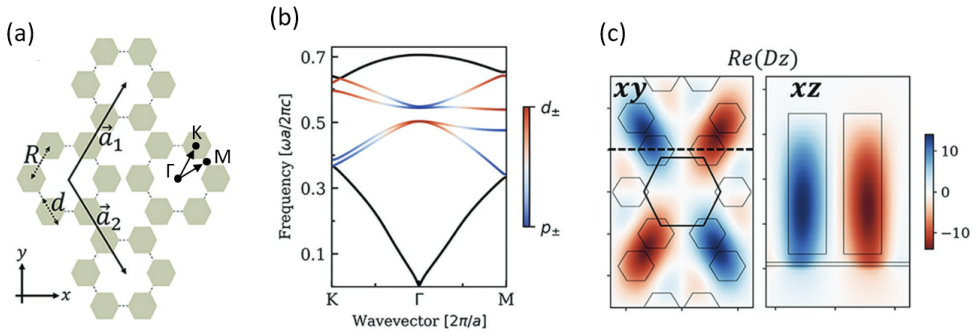

Figure 4.4: Honeycomb photonic crystal structure. (a) Cross-section of a honeycomb pattern of lattice constant a. The nanowires of diameter d are arranged into hexagonal unit cells of edge length R. (b) Photonic band structure of the expanded honeycomb lattice for transverse-magnetic (TM) modes. The dipole and quadrupole bands are shown in blue and red, respectively. (c) Quadrupole-like electric field profiles in the xy and xz planes, calculated at the bottom band-edge.

Honeycomb PhC design. The nanowires are arranged in a honeycomb pattern formed of tiled hexagons, as shown in Fig. 4.4 (a). The honeycomb pattern is defined by lattice vectors $\vec{a_1}$ and $\vec{a_2}$. In this case, the lattice constant $|\vec{a_1}| = |\vec{a_2}| = a$ is set to 630 nm to create a band edge around 1300nm. The nanowire diameter can be controlled by the size of the nanohole. For our samples, the nanowires had diameters d between 160 and 180nm for nanoholes of sizes between 30 and 50nm. The hexagon side length, R, can be changed independently of the lattice constant. For a perfect honeycomb pattern, $R = a/3$. For a perfect honeycomb, the band structure has a double Dirac cone at the Γ point, meaning that the band edge is not flat. To open a band gap in the Dirac cone, and thus flatten the band edge, R can be changed to expand or compress the honeycomb pattern without changing the lattice constant. The band gap for our expanded honeycomb photonic crystal, with $R = 230\mathrm{nm}$, is shown in Fig. 4.4 (b). The lower band edge has a wavelength of 1280 nm. In a typical photonic crystal, the first band

edge has a dipole field profile, with higher modes increasing the symmetry order of the mode profile. This is the case for the compressed honeycomb pattern. However, for expanded honeycomb patterns this is different. The lower band has a dipole mode profile, however, close to the Γ point the mode profile becomes a quadrupole mode. The second band edge will show the dipole mode profile instead. This effect is called band inversion and is represented by the colour bar of Fig. 4.4 (b). The lower band edge quadrupole mode profile is shown in 4.4 (c). The top-down view shows the symmetry of the quadrupole mode and confirms the overlap with the gain material of the nanowires. The cross-sectional view shows the mode is confined within the nanowires with minimal mode leakage through the silicon layer underneath. The field overlap with the gain material is as high as 40%.

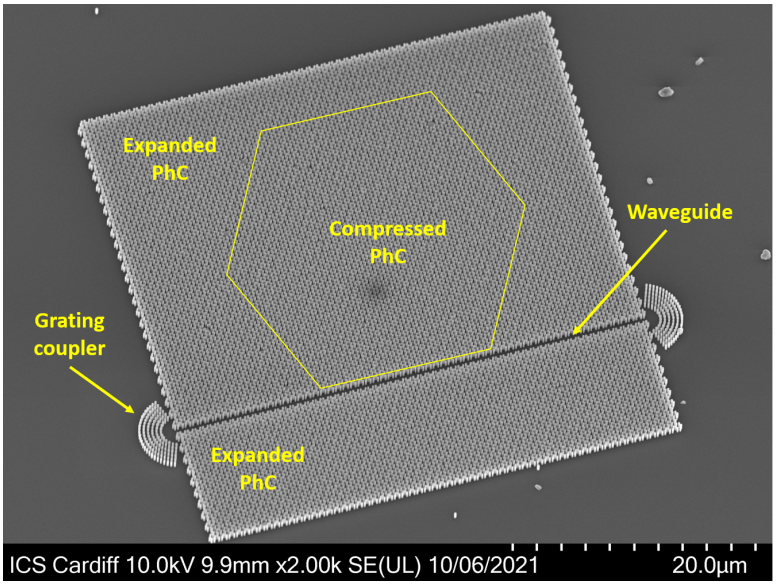

Figure 4.5: SEM image showing the full nanowire device structure

Full device structure. The expanded and compressed honeycomb photonic crystals are only part of a larger device shown in Fig. 4.5. This device makes use of the topological resonant modes at the edge between expanded and compressed lattices [129]. This resonant mode is coupled to the air-mode waveguide, which leads the laser output to a grating coupler. This topological device is outside of the scope of the thesis,

but is presented here for completeness, as parts of the device are investigated in the thesis. The existence of the topological mode could not be verified due to limitations in our measurement setup. Further work is needed to selectively pump the interface with a hexagonally shaped beam.

Optical characterization. The emission characteristics of the nanowire honeycomb arrays are studied using our room temperature micro-photoluminescence setup with the pulsed laser as light source. Lasing is observed at around 1300 nm from the expanded honeycomb lattice, matching the simulation prediction for the lower band edge energy. To verify this lasing peak comes from the band edge, the patten is pumped selectively with a beam spot of around 6$\mu\mathrm{m}$ diameter. The pattern shows the same lasing wavelength and intensity when pumped at various positions on the expanded honeycomb region, as shown in Fig. 4.6. This indicates that the underlying lasing mechanism is the same for all positions, and is not induced by small defects in the lattice such as missing or merged nanowires. The multiple peak spectrum coming from pumping the coupler region will be discussed in the following chapters, and is not part of the honeycomb photonic crystal.

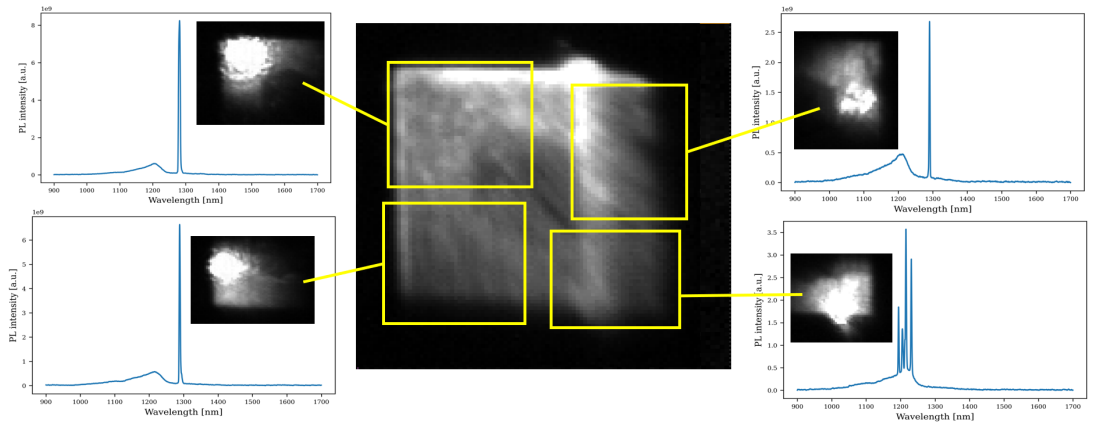

Figure 4.6: Lasing spectra of the expanded honeycomb array taken at different positions on the sample. The single mode lasing spectra all come from the honeycomb photonic crystal cavity, while the multimode spectrum comes from the grating coupler cavity.

The lasing characteristics of one such expanded honeycomb array is further studied in more detail. For these measurements, a pulsed laser with a $5\mathrm{MHz}$ repetition rate and a beam size of $6\mu\mathrm{m}$ diameter is used. At very low excitation powers, the spontaneous emission spectrum is observed, Fig. 4.7 (a). The broad spectrum is due to inhomogeneities in the InGaAs material. The peak at 1179 nm corresponds to a bulk composition containing 27% indium. When the pumping power is increased, a single sharp lasing peak appears at 1252 nm, Fig. 4.7. There is a slight blue shift effect in the spontaneous emission of 5 nm due to band filling. The integrated spontaneous and stimulated emissions, along with the FWHM of the spectrum, are shown in Fig.4.7. The lasing threshold is found to be 1.25 $\mu\mathrm{J\,cm^{-2}}$. This value is among the lowest reported values for nanowire photonic crystal lasers [35, 130–132]. Further work could lower the threshold by improving the overlap between the gain spectrum and the resonant wavelength. To further confirm the lasing resonance comes from the bottom band edge of the photonic crystal, a comparison is made of the lasing wavelength of patterns with different nanowire diameters with the simulated band edge frequency. Fig. 4.7 (d) shows the correlation between the simulated and measured resonant wavelengths. The offset between simulation and measurement can be caused by fabrication differences or imprecise effective refractive index approximations in the simulation.

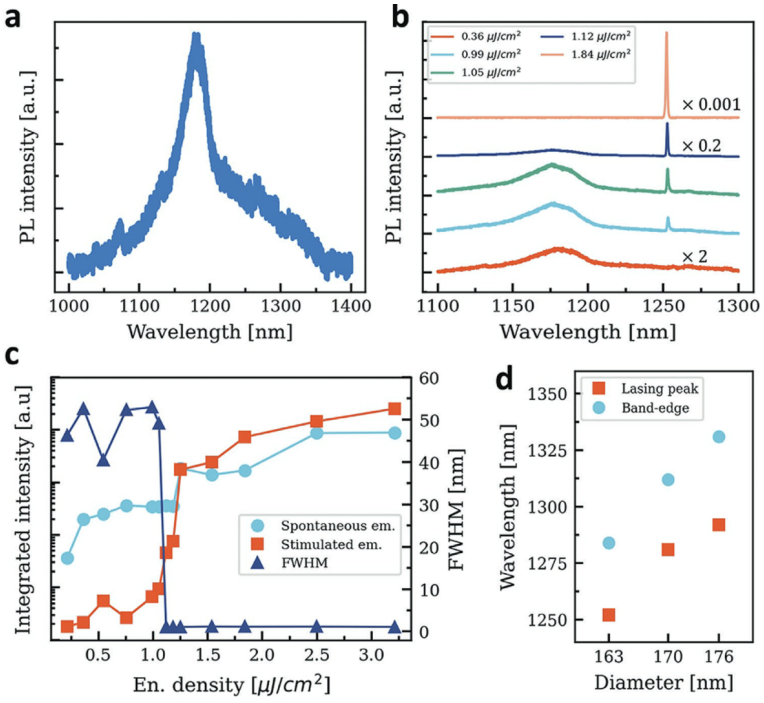

Figure 4.7: Optical characterization of expanded honeycomb lasing. (a) Spontaneous emission spectrum of the nanowires. (b) Optical emission spectrum at increasing pumping powers, showing the evolution of the lasing mode at 1252 nm. (c) Integrated emission intensities of the stimulated emission (red squares), spontaneous emission (cyan circles), and peak FWHM (blue triangles). (d) Lasing frequency for arrays with different nanowire diameter compared to the simulated band edge.

The compressed honeycomb lattice was shown to lase as well, at a slightly longer wavelength of 1300 nm. The lasing threshold is higher as the gain spectrum overlap is smaller at this wavelength. Using the photoluminescence mapping shown in Fig.4.8, significant scattering from the edge between the compressed and expanded honeycomb arrays is observed. The scattering shows that the two photonic crystals are successfully separated, and the edge abruptly disrupts the band diagram. This implies that the topological edge modes can exist in these samples.

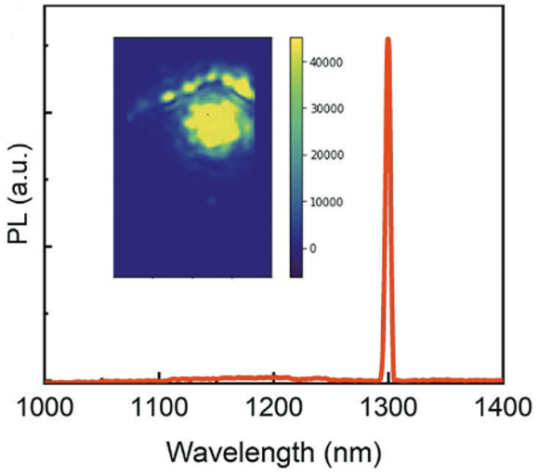

Figure 4.8: Compressed honeycomb lattice lasing spectrum and emission pattern

4.4 Curved cavity nanowire laser

To test the topological mode lasing of our nanowire devices, the micro-PL setup is used to pump one of the grating couplers. While the topological mode lasing could not be verified, it was found that the grating couplers themselves lased very easily. This chapter describes our model for the coupler lasing modes and explores the possibility of using curved array photonic crystals for laser devices.

Previously, curved cavity PhCs such as micro-disk lasers and PhC micro-ring lasers have been proposed and demonstrated using top-down fabricated air-holes PhC structures [133–137]. This type of curved circular structures takes advantage of high Q factor whispering gallery modes and gain enhancing PhC slow light effects to achieve high-efficiency devices. Such designs have not been realized in the bottom-up nanowire platform yet.

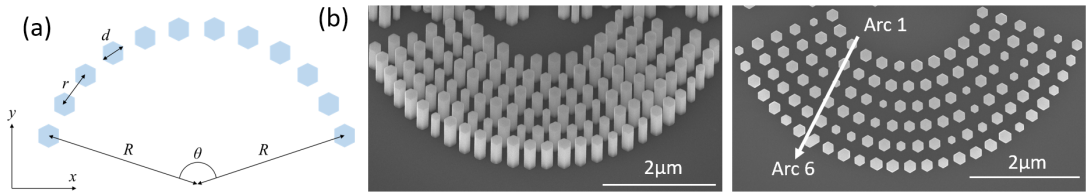

Figure 4.9: (a) Diagram of a single curved nanowire array with the relevant properties labelled. (b) Tilted and top-down SEM images of the curved array nanowire device.

The nanowire grating coupler device is formed of six circular arcs along which equidistant nanowires are placed as shown in Fig. 4.9. The number and period of nanowires is different for each arc. A nanowire arc is defined by a radius of curvature R, central angle θ, period r, nanowire diameter d.

Cavity design and simulation. To study the resonant properties of curved nanowire cavities, 3D FDTD simulations were performed using the Ansys Lumerical software. The nanowire array was meshed using a conformal mesh method with a minimum accuracy of 18 mesh points per wavelength. This is sufficient resolution, as increasing the mesh accuracy further does not change the results. The simulation region boundaries used PML boundary conditions on all sides, which were placed far enough away from the structure to not couple to the resonant cavity. To calculate the Q factors,the slope of the envelope of the decaying signal is used, computed using the high-Q monitor provided by Lumerical FDTD. To ensure travelling wave modes are excluded from the calculations, an apodization of 2500 femtoseconds is used to allow sufficient time for scattering to occur.

First, the full nanowire array structure is simulated, corresponding to the fabricated structure shown in Fig. 4.9 (b). Fig. 4.10 shows the electric field profile of resonant modes taken at the plane half the height of the nanowires, indicating increasing resonant wavelength from arc 2 (1295 nm) to arc 6 (1340 nm). The increase of resonant

wavelength is due to the increase of both the spacing between nanowires and the cavity size defined by the arc length.

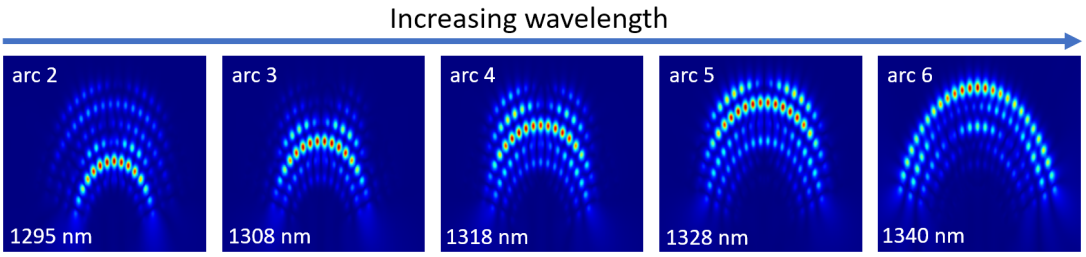

Figure 4.10: FDTD simulation showing the electric field magnitude at the resonant modes of the curved nanowire array device. The field profile is shown at a cross section through the array taken at half the nanowire height.

To understand the origin of the resonances, additional 3D FDTD simulations were carried out for each individual arc separately, and the simulated spectra are shown in Fig. 4.11 (a). Interestingly, the resonant wavelengths from arc 1 to arc 6 shows excellent agreement with the resonance frequencies of individual arc structures in Fig. 4.11 (a). This suggests that the interactions between resonant modes in arcs are very small, and the radiation from non-active arcs can be negligible when one of the modes is lasing. This can be understood from the weak electric field profiles in non-active arcs in Fig. 4.11. Note that arc 1 could not form a visible resonant mode in the full array structure because it has a very low Q factor, as manifested by the broad peak, due to its short cavity length. While arcs 2, 3 and 4 show single mode resonances, arcs 5 and 6 show multimode resonances due to their larger arc length.

Q-factor simulations. Next, the effect of the radius of curvature on the Q factor is investigated by simulating a single curved array with different radius of curvature values. All other parameters are kept the same, including nanowire number, nanowire dimension, spacing, and cavity length. Note that for the data set shown in Fig. 4.11(b), all simulations were done in two dimensions due to computational time constraints.

Although this 2D FDTD simulation setup eliminates the vertical loss both into the substrate and the air, leading to a constant increase in the Q factor for all radius values, the couplings between the nanowires are well described. As one can expect, the curvature of the array has negligible impact on the lateral losses at large bending radii, resulting in the Q factor very close to that of a straight array. Interestingly, in the opposite limit when the value of bending radius is very small, the Q factor increases significantly due to the coupling between the fields at both ends of the array. The curved array eventually bends into a full circle which acts similarly to a micro-ring, leading to very large Q factors. The oscillating behaviour at small bending radius around 1-3 μm, shown in the Fig. 4.11 (b) inset, can be correlated to the distance between the two ends of the array. The coherent laser light exits the structure through the ends of the arrays, as shown in Fig. 4.13 (b). At smaller values of radius of curvature, the two ends will be close enough to each other to be coupled together. Light exiting one end of the array can then be absorbed by the other end and recycled. As the emitted light is coherent, the distance between the two ends determines whether the absorbing end lies at a node or antinode of the emitted wave. If the absorbing end is placed at an antinode, the coupling strength between the ends of the array will be higher. If the absorbing end is placed at a node, the coupling strength will be lower. As the distance between the ends changes due to the change in radius of curvature, the ends go through peaks and troughs, causing the coupling, and thus the Q factor to oscillate.

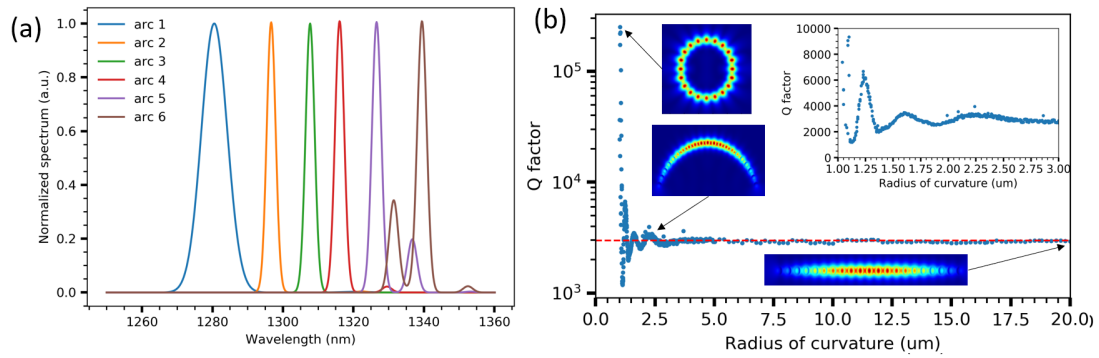

Figure 4.11: (a) FDTD simulation results showing the normalized resonances of each individual nanowire arc. (b) the relationship between Q factor and the radius of curvature of an arc along with representative E-field mode profiles and a dashed line indicating the Q factor value of a straight nanobeam, with an inset showing Q factor oscillations in greater detail.

A complete nanowire microring circle has been simulated to have a Q factor on the order of 105. This resistance to bending losses showcases the ability of nanowire arrays to be bent into shapes similar to their hole-based PhC counterparts for applications such as microring lasers [133–137]. Although the Q factors for curved arrays are low compared to a full circle, they could be greatly improved by including nanowire-based reflectors at the two ends of the beam, tailoring the spacing between nanowires or decreasing the thickness of Si layer [123, 138, 139].

Nanowire uniformity study. Due to the physics of nanowire growth, some variation of nanowire diameter is expected even for 100% yield runs. Previous simulations assumed all nanowires are identical; however, it is of interest to know the limit at which the resonant cavity stops functioning. A series of simulations of a single nanobeam with random nanowire diameters was performed. The array contains 21 nanowires. The nanowire diameter follows a normal distribution, with a mean of 190 μm. The variance is taken to be between 0 and 30% of the mean. Two simulations are done for each variance value with different random number generator seeds, and the Q factors

are averaged. This limits the effect of randomly created defect mode resonances and scattering points.

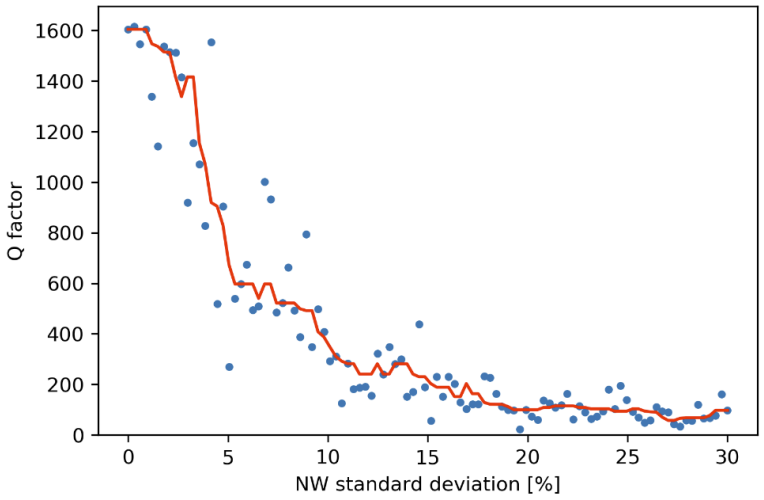

Figure 4.12: Nanowire Q factor vs diameter standard distribution. A moving average mean is shown as a red line to highlight the trend.

Figure. 4.12 shows the results of the simulations. For very uniform nanowires, with a standard deviation of less than around 3% of the nanowire diameter, the Q factor remains constant. Nanowire with large scattering potential can still occur even at high uniformity as seen by the outliers in this region. A large threshold is reached at around 5%. The threshold represents the point at which the fundamental mode of the cavity stops functioning. There are many outliers in this area, as the positioning of the scattering nanowires is important. As more scattering points are added into the nanobeam, the available resonances have increasingly smaller spatial spread, leading to much lower Q factors.

This result shows that a standard deviation of nanowire diameter of less than 3% is required for a 100% nanobeam yield. Our samples have a higher deviation, meaning that not all nanobeams will be functional.

Far field emission simulations. To predict the emission profile of the nanowire array lasers, the free space far field pattern of the resonant modes was calculated using the 3D FDTD method. First, we can expect the most of light is emitted from the ends of the nanowire arrays in the lateral direction (XY plane in Fig. 4.13 (a)) similar to straight nanobeam lasers [17,18]. This can be seen from the Poynting vector plot in Fig. 4.13 (b) which shows the power flux of the electromagnetic field is strongest at the ends of the array. The Poynting vector points tangentially away from the array, showing the light is emitted towards the back of the array, in the + Y direction. There is no field flow towards the front of the array in the -Y direction, indicating that bending losses are negligible for this radius of curvature.

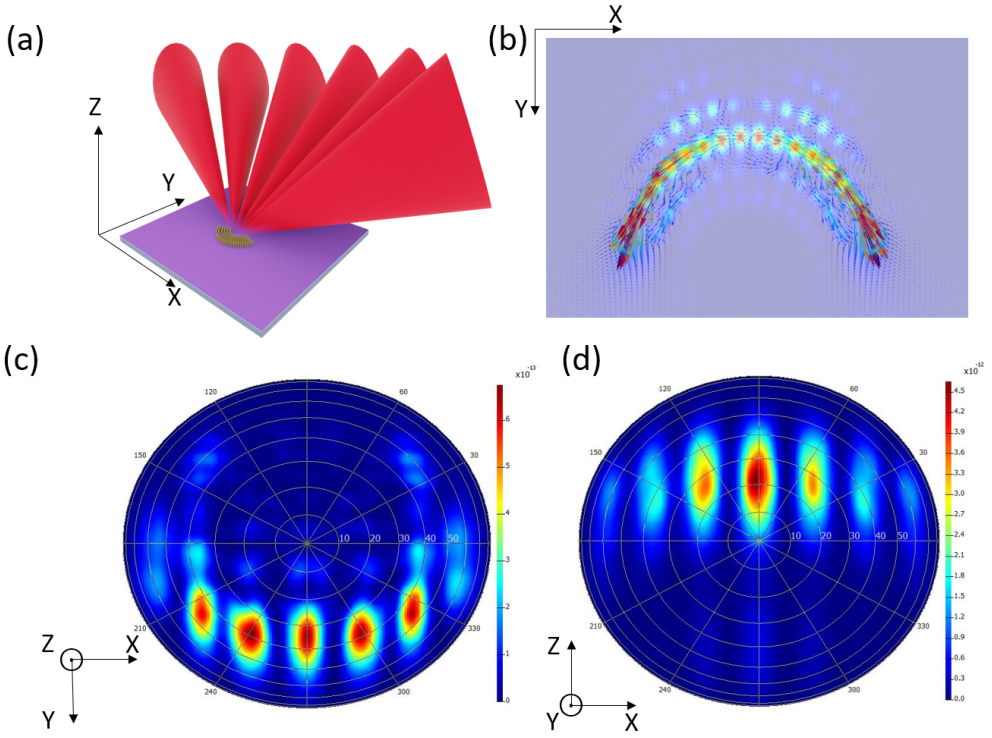

Figure 4.13: Far field emission simulations of the full structure at a representative wavelength of 1318 nm. (a) diagram showing the free space emission of the structure, (b) Poynting vector map overlaid over the |E| field showing the emission direction, (c) polar plot of the far field emission in the vertical (+z) direction and (d) polar plot of the far field emission in-plane (+y).

Because of the small cavity size, the two output beams have relatively large divergence. In the far field, the emission from the two ends will overlap and interfere. This is shown in Fig. 4.13 (c) and (d), where multiple lobes can be seen. Figure 4.13 (c) shows the far field emission as seen from the top of the array, confirming the preferentially directional emission towards the back of the array. The in-plane emission is shown in Fig. 4.13 (d) where the same interference pattern can be seen again. The interference pattern azimuthal divergence angle is approximately 100° and the polar divergence angle is approximately 20°. Since the two ends of the array are not parallel to each other, the azimuthal divergence is large. This can be improved by aligning the ends of the array to point in the same direction, ensuring the emitted beams propagate parallel to each other. The radius of curvature was found to have a small impact on the polar divergence angle, giving a tuneability range of between 10°-30°.

Optical characterization. To verify the observed modes match the simulated resonant modes shown in Fig. 4.10, the array is selectively pumped and the lasing threshold is measured. A lower threshold signifies a higher overlap between the pumping spot and the resonant mode. The results are shown in Fig. 4.14 (a). When pumping on the side of the array, the threshold is significantly higher, implying that the resonant mode is confined mainly to the centre of the array, as expected from the simulation.

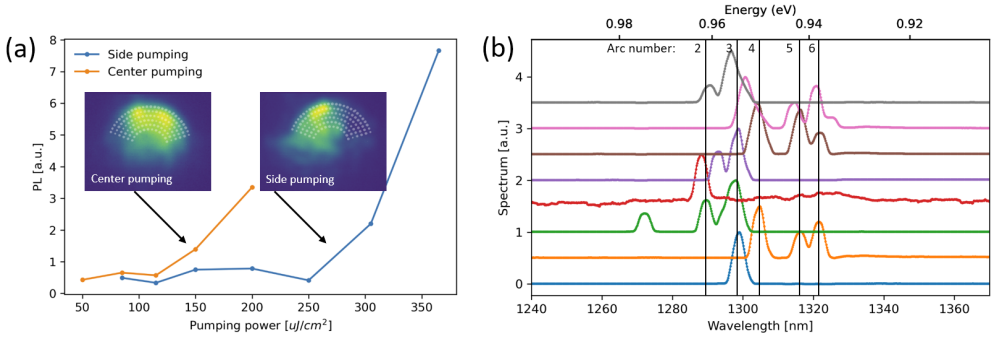

Figure 4.14: (a) LL curves of the array pumped selectively in the centre and on the side of the cavity, along with images showing the two pumping positions. (b) Lasing spectra of a few nominally identical nanowire arrays showing common lasing wavelengths.

Eight nominally identical nanowire arrays on the same sample were measured, their lasing spectra shown in Fig. 4.14 (b). Although no device showed lasing from all curved arrays, five common lasing wavelengths can be identified, suggesting that the lasing mechanism is that described by simulations. The lasing lines at 1288 nm, 1297 nm, 1305 nm, 1324 nm and 1328 nm are assigned to arcs 2, 3, 4, 5 and 6 respectively. Arc 1 is unlikely to lase due to its very low Q factor. Some lasing lines appear outside of the five common wavelengths. These can be attributed to other resonant modes introduced by the nanowire non-uniformity. There is a slight discrepancy between the measured and simulated lasing wavelengths, which can be attributed to experimental factors such as the change in local effective refractive index due to non-uniformity in nanowire size or in the InGaAs composition, and to simulation related factors such as imperfect meshing. The jump in wavelength from the first four arcs to the last two can be explained by the nanowire diameter being slightly larger on the outside of the array. This is due to the larger diffusion area available for the nanowires to draw precursors from. The previous simulations have shown arc 1 to be very lossy due to its short cavity length. For the other arcs, a major factor that can impede lasing is the non-uniformity in the nanowire size, which leads to a decrease of Q factor and increase of the lasing threshold. It's possible that the pumping power was not high enough to cause lasing in

the less uniform arcs. Moreover, the position of the outlier nanowire is important, as the impact of the NW on the mode increases with mode overlap. A single non-uniform nanowire in the centre of the array will cause much more scattering than one placed at the ends.

The lasing properties of one representative array are measured in more detail. The measured emission spectrum from the full nanowire array structure is shown in Fig. 4.15 (a). At low pumping powers, the lasing spectrum is single mode around 1305 nm. At increased pumping power, multiple lasing modes emerge at different lasing thresholds and slope efficiencies. This difference is likely due to the difference in their Q factors caused by the non-uniform nanowire diameters. The nanowires show a reasonably uniform gain spectrum around 1300-1330 nm, which is unlikely to have a noticeable effect on the lasing threshold. The gain spectrum is broadened by InGaAs compositional changes at the edges of the nanowire, shown in Fig. 4.3 (a).

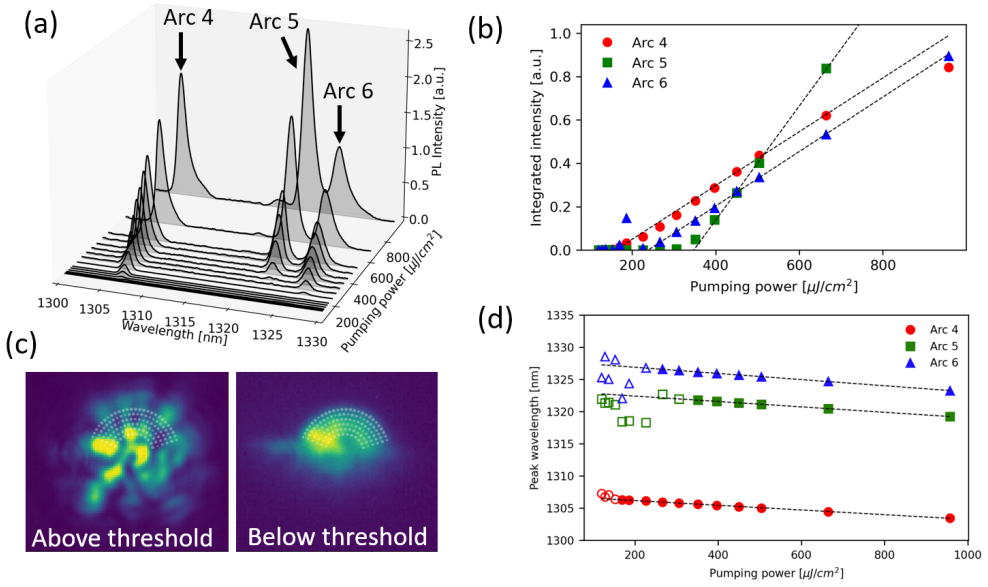

Figure 4.15: Optical characterization of a representative nanowire array structure. (a) Power dependent PL emission showing the evolution of the lasing spectrum. (b) L-L curves of the three lasing peaks along with linear fits in the above threshold regions. (c) Near field emission of the array before and after the lasing threshold, showing characteristic interference patterns, along with a transparent SEM overlay of the array structure. (d) Peak wavelength as a function of pumping power, along with fits in the above threshold region. The hollow markers represent data points below the threshold.

The L-L curves of the three lasing peaks are shown in Fig. 4.15 (b). A threshold power density of 157 μJ/cm2 is extracted for arc 4. Arcs 5 and 6 show thresholds of 347 and 238 $\mu J\,cm^{-2}$ respectively. These values are in line with other thresholds of III-V nanowire photonic crystal lasers at room temperature [108, 123, 131]. The Q factor can be approximated using the full width at half maximum of the lasing peaks immediately after the threshold. This method overestimates the Q factor, however the comparison between different arc is still meaningful. From the measurement, arcs 4, 5 and 6 have Q factors of around 2300, 1100 and 1400 respectively. The Q factor is well correlated with the lasing threshold for each arc, showing the importance of nanowire uniformity.

Figure 4.15 (c) shows the near field emission images captured by the InGaAs focal plane array detector at below and above lasing thresholds. The speckle pattern is oriented towards the back of the array, indicating that light is preferentially emitted towards the back of the array. This agrees with the results of the simulations presented in Fig. 4.13. The lasers show good wavelength stability with no mode hopping at increased pumping powers as seen in Fig. 4.15 (d). The slight redshift can be attributed to the self-heating of the laser, causing a change in the effective refractive index of the cavity. Both the refractive index of the nanowire, and the nanowire diameter increase with temperature, leading to an increase in wavelength. The refractive index dependence on temperature is two orders of magnitude higher than the thermal expansion index, indicating that refractive index change is the main redshift mechanism.

4.4.1 Contributions

Significant contributions to the work presented in this chapter have been made by a number of people. Dr. Oumaima Abouzaid and Dr. Qiang Li helped with sample growth by operating the MOCVD reactor for the samples presented. Cristian Messina did initial honeycomb simulations and wrote the manuscript parts of this chapter are based on. Dr. Tim Grieb and Dr. Andreas Rosenauer did the TEM imaging for the NW samples. Cristian Messina and Balthazar Temu assisted in the initial curved array simulations. The mask for the nanowire was fabricated by the Institute of Compound Semiconductors and designed by Dr. Yongkang Gong. Analysis of the data measured by others was done by the author, as well as all work not highlighted here.

Chapter 5

Tunnel epitaxy

A promising way to reduce defects in heteroepitaxy on silicon is to make use of patterned substrates. Selective area epitaxy makes use of dielectric materials such as silicon oxide or nitride which have very low sticking coefficients. Unlike the nanowire approach, in this chapter the possibility of large-area epitaxy using selective epitaxy is investigated, by means of changing the growth direction from vertical to lateral.

5.1 Introduction

Aspect ratio trapping. Since threading dislocations propagate upwards at an angle in the $\langle 1\,1\,1 \rangle$ direction, and they can only terminate at a surface, we can use vertical walls to stop the dislocations from climbing to the active region. Using long stripes of oxide with exposed silicon surfaces in between has proven to reduce surface defect density [140, 141]. This technique is called aspect ratio trapping (ART). The trench height must be sufficiently tall in relation to the width to be able to effectively intercept defects. Fig. 5.1 shows the trapping mechanism for threading dislocations and planar defects propagating parallel and perpendicular to the trenches. The only type of defects that can not be trapped are planar defects propagating parallel to the trench. Additional defects can be nucleated when the III-V grows out of the trenches and coalesces [142]. If the silicon substrate has a no-offcut (001) surface, antiphase boundaries could appear, and they would not be completely removed by the ART mechanism.

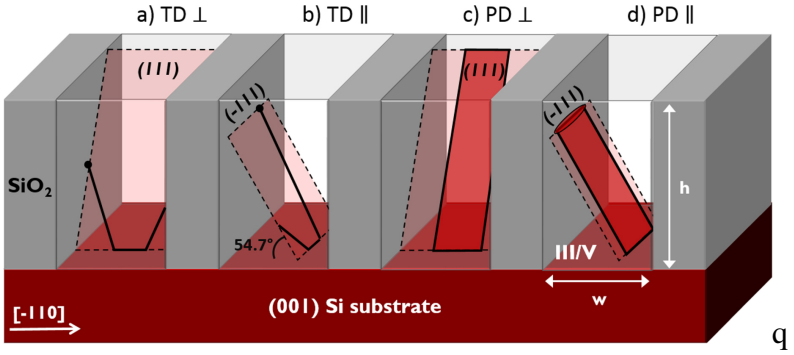

Figure 5.1: Aspect ratio trapping diagram showing the defect reduction mechanism. All threading dislocations can be trapped, but planar defects parallel to the trench can propagate upwards. [140] .

V-grooves. To remove issues with ABP it is common to etch the exposed silicon to expose $(1\,1\,1)$ surfaces. Monolayer steps on the $(1\,1\,1)$ surface do not cause antiphase boundaries, unlike $(0\,0\,1)$, as shown in Fig. 5.2. This type of structure is called a v-groove. Combining v-grooves and ART has been used to create defect nanoridges structures. Nanoridges have been used to create CMOS-integrated electrically pumped lasers [143]. Integration with silicon photonics can also be accomplished, though high coupling efficiency requires large device footprints [144].

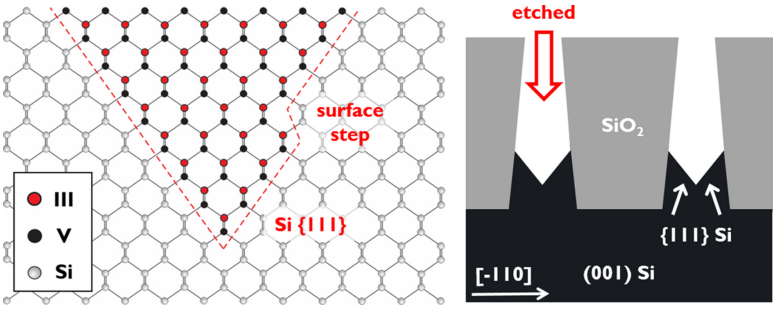

Figure 5.2: V-groove diagram showing that antiphase boundary do not nucleate on $(1\,1\,1)$ surface steps. [145].

Using v-grooves on their own, without ART, has also been used to reduce defect density. The undercut under the mask creates a small 'tiara' around the edges of the v-

groove, which is effective at intercepting threading dislocations [68, 75, 146].

5.2 Review of recent lateral selective area growth

Lateral selective area epitaxy uses the same concepts as aspect ratio trapping and v-groove patterning, but changes the growth direction from vertical to lateral. This approach has the potential of creating large area, planar, thin sheets of III-V on silicon with no dislocations. Many groups have implemented such a technique using various approaches.

The lateral selective area epitaxy approach has other benefits, aside from the defect free integration. By lithographically defining the growth areas, we solve the alignment challenges of bonding and transfer-printing techniques. Moreover co-fabrication of III-V and Si can be performed as the active region is in plane with the waveguide. Additionally, the thermal expansion mismatch challenge in traditional thick buffer heteroepitaxy is solved by fabricating the tunnels to be much less thick than the crack formation thresholds. The thermal budget constrains are also relaxed, as the high temperature III-V growth happens before passive SiPh device fabrication and metallization steps.

A selection of recent results is shown in Table. 5.1, showcasing the different materials and structures available and the largest areas achieved. A collage of the recent results is shown in Fig. 5.3, showcasing the various III-V shapes that can be achieved with lateral epitaxy.

The first applications of lateral epitaxy were a proposed solution for the creation of silicon-on-insulator substrates in the 90s [147]. Recent research focuses on the growth of III-V on SOI. University of California Santa Barbara has done research in lateral epitaxy both on native InP and silicon, studying the physical mechanisms of growth [148, 149]. Additionally, they found a method to remove parasitic deposition on the

growth mask, which is a common issue with such selective area epitaxy techniques [150].

IBM Zurich and ETH Zurich, et al. have investigated the use of lateral epitaxy for thin nanowire structures which can be integrated with electrical and photonic components [122, 151, 152]. They have also demonstrated that lateral growth can produce very high-quality crystal, equal to wafer bonding techniques [153]. Recently, they have also demonstrated the possibility of defect-free coalescence from multiple silicon seeds in confined epitaxy [154].

Hong Kong University of Science and Technology (HKUST) has investigated the possibility of large area III-V on SOI using longer tunnels. Initial experiments used very long Si seeds and short tunnels [155]. Further research used shorter tunnels and wider tunnels to increase the total epitaxy area [156]. More recently, they realized defect-free regrowth from III-V on SOI template [157], and long cavity DBR lasers [158].

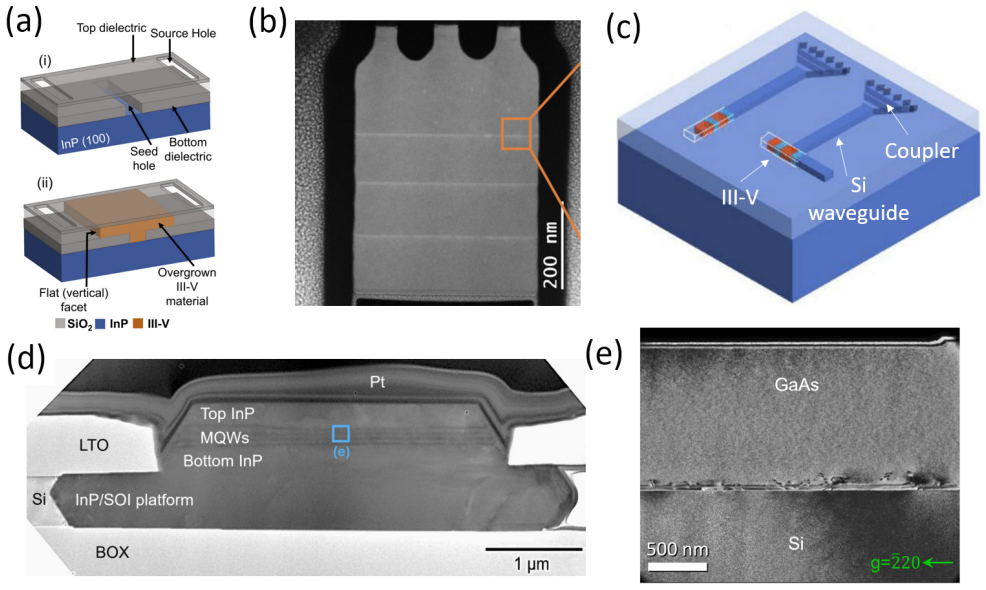

Figure 5.3: Review of recent lateral area growth. (a) Template-Assisted Selective Epitaxy of InP on InP wafers. [159] (b) Selective Epitaxy in Templates of InP on Si showing merging from multiple Si seeds. [154] (c) Template-Assisted Selective Epitaxy of InP/Si photodiodes showing integration with SiPh passive elements. [98] (d) Large area InP/SOI template with regrown microring. [157] (e) Lithographically defined tunnel epitaxy of long InP/SOI stripes (this work) [160].

Table 5.1: Review of recent lateral selective area growth by different research groups, showcasing the materials and areas achievable.

	Year	Substrate	Epilayer	Area
University of California Santa Barbara [159]	2019	InP	InP/InGaAs	1x1 µm
IBM Zurich [98]	2022	Si	Doped InP/InGaAs Photodetector	1000x500 nm
Hong Kong University of Science and Technology [157]	2023	Si	InP + InP/InGaAs QW	5x7 µm
Cardiff University [160] (this work)	2023	Si	GaAs	2.5 µm x 200 µm

5.3 Defect trapping mechanism

The diagram in Fig. 5.4 shows the propagation and confinement of dislocations in tunnel epitaxy. The setup is similar to that of vertical ART presented before, the main

difference being that the Si surface shows a $\{1\,1\,1\}$ surface. The strain crates dislocation half loops consisting of misfit dislocations propagating along the $\{1\,1\,1\}$ Si surface. Threading dislocations and planar defects such as twinning boundaries or stacking faults lie on $\{1\,1\,1\}$ planes as well. TDs will glide along one of the three available $\{1\,1\,1\}$ planes. Since all $\{1\,1\,1\}$ planes that intersect the Si surface intersect the nitride, all TDs will propagate into the SiN and terminate close to the Si seed. This is shown in Fig. 5.4 (a) and (b). One $\{1\,1\,1\}$ plane was omitted since it is horizontally symmetric to (b). in $[0\,0\,1]$ direction) and will finally hit the top SiN layer. The trapping distance of TDs relies on the crystalline planes and is generally 1.4 times the thickness of the Si device layer, similar to aspect ratio trapping [161]. The 220 nm Si device layer here (or the height of the growth cavity) translates into a dislocation trapping distance of 310 nm, which reasonably agrees with the observed distance of 250 nm in our plan-view TEM.

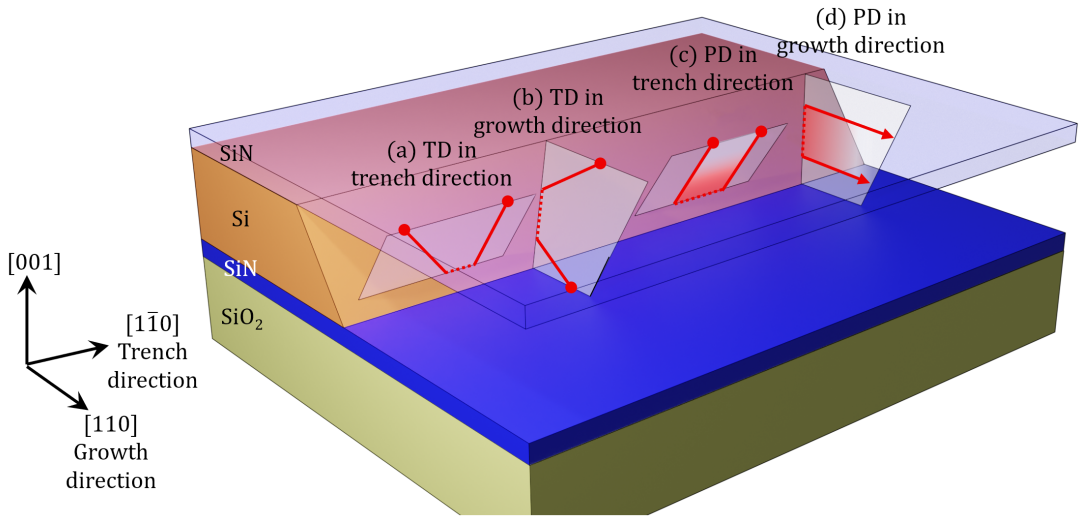

Figure 5.4: Schematic showing the confinement of threading dislocations (TD) and planar defects (PD) in lateral tunnel epitaxy. Circle line ends represent trapped defects, arrows represent untrapped defects. TDs propagating in the $\{1\,1\,1\}$ plane parallel to the Si trench direction (a) and in the $\{1\,1\,1\}$ plane parallel to the growth direction (b) can be trapped. Planar defects in the $\{1\,1\,1\}$ plane parallel to the Si trench direction (c) can be trapped. Planar defects at the $\{1\,1\,1\}$ plane parallel to the growth direction (d) cannot be trapped.

Planar defects propagating in the plane shown in (c) are also trapped and terminate at the SiN interface. However the two remaining planes, shown in (d), are not trapped and can propagate infinitely through the crystal in the growth direction. Different from stacking faults in conventional III-V buffers on silicon which are often accompanied by two partial dislocations at both ends, the planar defect in Fig. 5.4 (d) tends to terminate at the free surface of the dielectric layer and thus avoids introducing additional dislocations the III-V material [161]. As a result, their impact on device performance could be less severe.

5.4 Pattern fabrication

As shown by the schematic in Fig. 5.5, a front-end patterning and epitaxy process is developed on a standard 220 nm SOI substrate that allows the selective growth of GaAs prior to the formation of Si waveguides or metallization. The fabrication was done in collaboration with the University of Southampton.

Starting from an 8-inch 220 nm (001) SOI substrate, etching Si trenches was carried out in step 2 (Fig. 5.5). A 40 nm SiN layer was deposited and patterned to open a Si seed at one side of the trench (step 3). A thick amorphous Si (a-Si) layer was then deposited and planarized by chemical mechanical polishing (CMP). Note that the pre-deposited 40 nm SiN can be used here as an etch stop layer for the CMP process in step 5. Afterwards, another 200 nm SiN layer was deposited, and the growth openings in the SiN layer were defined at the other side of the Si trench (step 6). The a-Si sacrificial layer was then removed by TMAH wet etch. This was then followed by a hydrofluoric acid (HF) cleaning step to remove any native oxide present between the a-Si and the crystalline Si layer. A further TMAH etch was performed to produce smooth 111-orientated Si facets at the Si seed (step 7), which is important to prevent antiphase boundaries (APBs) in III-V/Si heteroepitaxy [162, 163]. Finally, the lateral tunnel epitaxy of III-Vs was carried out in MOCVD (step 8). To employ the III-V layer for practical device applications, the top SiN layer can be removed by either HF wet etching or dry etching methods, such as inductively coupled plasma (ICP). Figure 5.5 (b) displays the top-view SEM photo of the fabricated SOI pattern. The top SiN layer is transparent and the Si trench and Si seed underneath are visible. As indicated by the blue arrow of growth direction, III-V lateral tunnel epitaxy will initiate from the Si seed and grow in the lateral direction parallel to the substrate surface.

As this was the first attempt at fabricating tunnel structures, the process steps were not fully optimized and the resulting patterns had significant variations. Tunnel length and shape varied between chips, and some tunnels were collapsed. The samples presented in this chapter were grown on the successful chips, with similar tunnel lengths and

window spacing. A notable difference is that some patterns had single-sided tunnels while others had double-sided, resulting in a reduced growth rate.

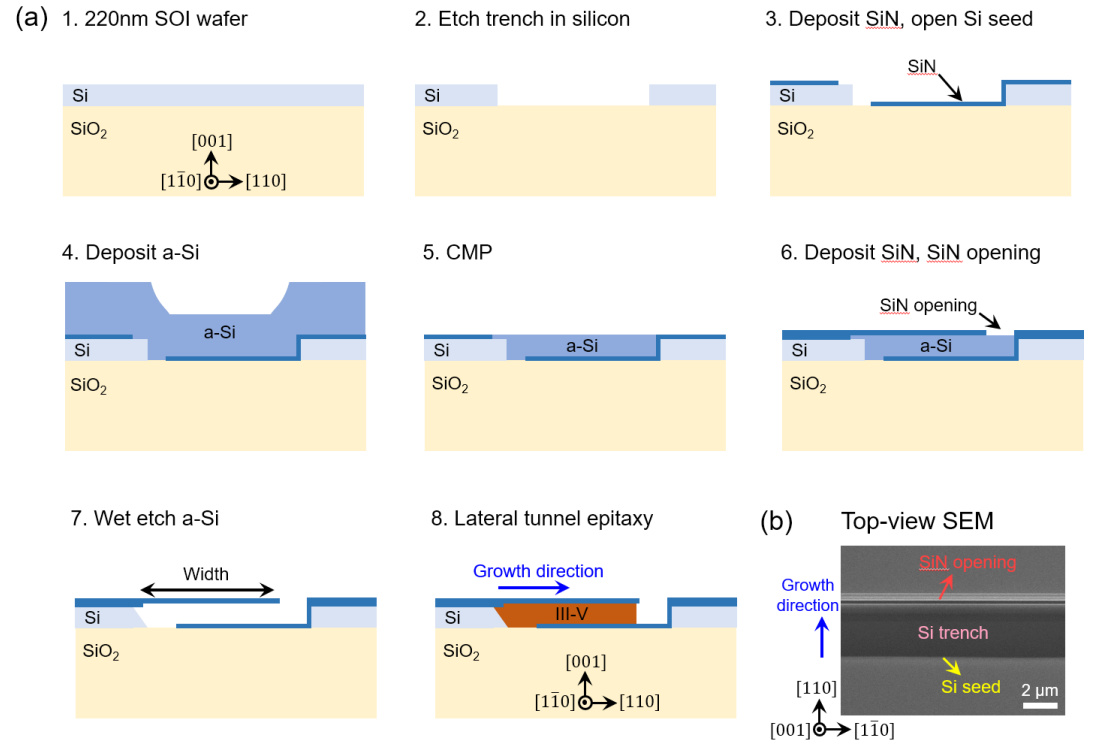

Figure 5.5: Process flow of the front-end process for lateral tunnel epitaxy on a 220 nm SOI. (b) Top-view SEM photo of fabricated SOI patterns. The top SiN layer is transparent under top-view SEM.

5.5 Growth studies

Selectivity studies. Using MOCVD with hydrogen as the carrier gas and TEGa and TBAs as growth precursors, GaAs is grown directly on the patterned chips. Prior to growth, the sample was dipped in diluted HF to remove the native oxide on the Si seed surface and then immediately loaded into the MOCVD reactor. The growth process started with 800 °C annealing for 20 min for thermal deoxidation. Various precursor flow rates, durations and temperatures were used for the growth studies.

Initial growth runs on the tunnel epitaxy template had very poor selectivity. Despite the high desorption rate on SiN, the precursors nucleated on the mask, rather than inside the tunnel on the silicon seed. As growth continues precursors would diffuse and find nucleated sites on the mask quicker than the Si seed, thus drawing the precursors away from the seed and on the mask deposited crystals.

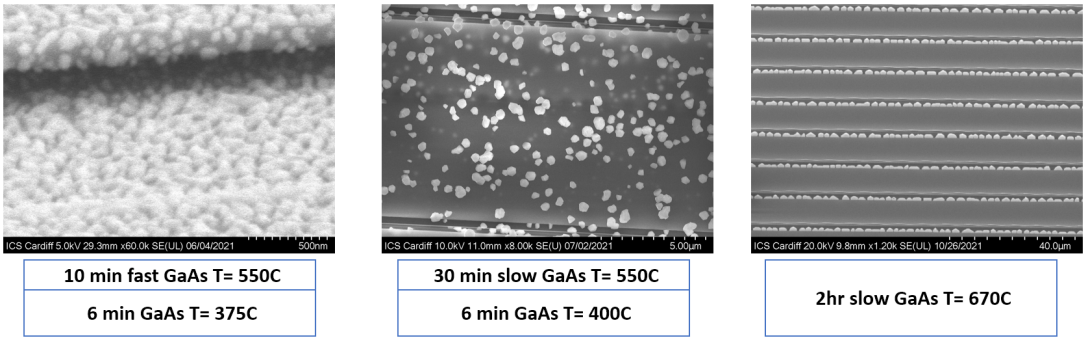

Figure 5.6: Selectivity issues of GaAs showing three growth runs with different growth parameters. Best results at high temperature with very slow growth rates.

Three GaAs samples grown with different parameters are shown in Fig. 5.6. Initial growth runs used parameters similar to that of planar GaAs on Si, using high precursor flows and with a low-temperature nucleation layer. This yielded very poor selectivity. The mask was covered in deposition and very little precursors entered the tunnel. Inside the tunnel, the deposition rate quickly decreased with distance from the window, with no visible growth on the silicon surface. Decreasing the precursor flow by a factor of 10 improved the selectivity. Nucleation requires multiple adatoms to stick to each other, so the lower flow decreases the probability of nucleation. This enabled the precursors to diffuse into the tunnel, however, the growth rate at the silicon seed was still too low. The biggest improvement was achieved by increasing the temperature by 120 °C and removing the low-temperature nucleation step. This set of parameters is very similar to that used for nanowires. The desorption off the mask is strongly dependent on temperature [164] resulting in much higher growth selectivity. There was very little deposition on the mask, which allowed the precursors to find and grow from the silicon

seed inside the tunnel. The deposition on the mask was largely in areas with no open tunnels.

Nucleation studies. After achieving good selectivity the the nucleation and growth of GaAs inside tunnels is further studied. GaAs was grown at a single temperature of 670°C for two hours. Three samples with different growth rates are grown, using the precursor flows shown in Fig. 5.7. As shown in Fig. 5.7 (a), GaAs islands are nucleated along the silicon seed surface. By increasing the growth rate, denser GaAs islands emerge with well-developed crystalline facets, shown in Fig. 5.7 (b)). The two vertical $\{1\,1\,0\}$ facets are formed at both sides of the GaAs islands as indicated by the white dotted line in Fig. 5.7 (b), similar to other selective growth of III-V nanoridges and vertical III-V nanowires with six $\{1\,1\,0\}$ side-facets [40]. By further increasing the growth rate, a continuous GaAs layer could be obtained, as indicated by Fig. 5.7 (c). The coalesced GaAs layer shows portions of both smooth growth, as well as rough portions, indicating that there are defects in the crystal structure.

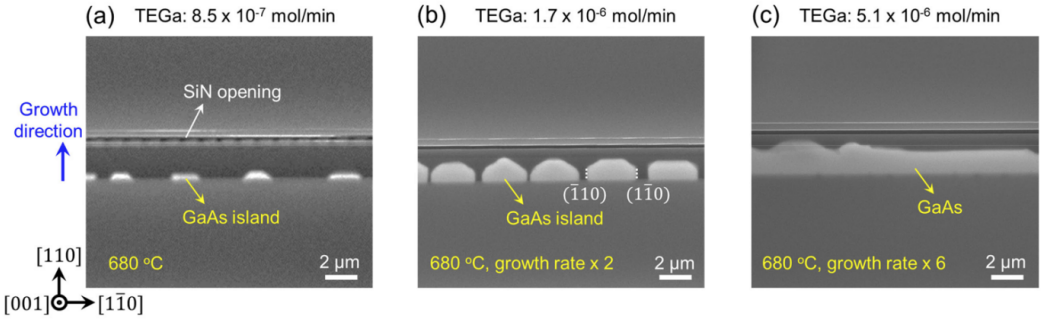

Figure 5.7: Top-view SEM photos of as-grown GaAs inside the tunnel without the low temperature GaAs nucleation layer. The top SiN layer is transparent under top-view SEM. (a) Tiny GaAs islands deposited at a slow growth rate. (b) Larger GaAs islands with clear faceting are formed. The GaAs islands exhibit two $\{1\,1\,0\}$ facets on both sides. (c) GaAs grown inside the tunnel at an increased growth rate. The GaAs growth front formed both straight and bumpy end facets.

Diffusion length study. The maximum width of the tunnel is given by the diffusion length of the precursors. More precisely, the growth rate is proportional to the amount of group III precursor at the growth interface. The amount of group III precursor at the Si seed will be dependent on a number of factors such as tunnel width and height, precursor species, temperature, mask surface roughness and reactor pressure.

To estimate the diffusion length into the tunnel, a staircase pattern was used, Fig. 5.8. The width of the tunnel is large so that the difference in width will not significantly bias the results. For our patterns, using TEGa as group III precursor, with a growth temperature of 670°C we find nucleated islands up to 50 µm away from the window. The growth rate decreases linearly as expected. This result suggests that it should be possible to grow very wide area slabs, larger than the current record of about 10 µm [157].

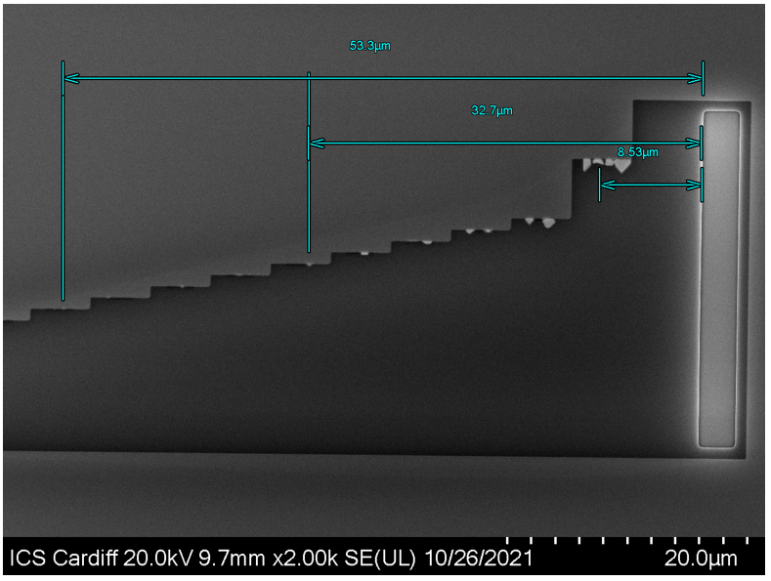

Figure 5.8: Top-down SEM image showing the precursor diffusion length inside the tunnel. The sample is GaAs grown with $1.7 \times 10^{-}6\ \mathrm{mol/min}$ **TEGa flow at 670** °C **for two hours.**

5.6 Material characterization

GaAs epitaxy. We prepared plan-view GaAs/Si TEM lamella by using focused ion beam milling. The schematic of Fig. 5.9 (a) illustrates the orientation of the TEM lamella, which includes both the Si layer and the in-plane GaAs layer. The thickness of the TEM lamella was approximately 400 nm. During the ion milling process, intended to thin the TEM lamella, the SiN layer was still present as well as oxide on the opposite face. As such, the TEM lamella incorporates nitride and oxide on both sides and the epitaxial GaAs in the middle. This is quite thick for TEM but still yields acceptable images, aided by the anomalous transmission effect when a two-beam diffraction condition is used. The TEM montages in Fig. 5.9 (b) and (c) present paired bright-field and dark-field images taken in the $g = 220$ diffraction condition. GaAs regions with both straight and bumpy growth fronts can be observed. The bumpy growth front likely results from the coalescence of two adjacently situated, non-$\{1\,1\,0\}$-orientated side-facets of GaAs islands. The dark area near the bumpy growth front in Fig. 5.9 (c) suggests it has a twinned orientation different from the surrounding GaAs, which could be associated with the planar defects in this same area. A cross-sectional-TEM analysis of a similar twinned section will be presented later. Despite this problematic coalescence region, Fig. 5.9 (a) shows a clean GaAs membrane region with a length of several microns that is completely free of any crystalline defects, which is not feasible in conventional thin film heteroepitaxy.

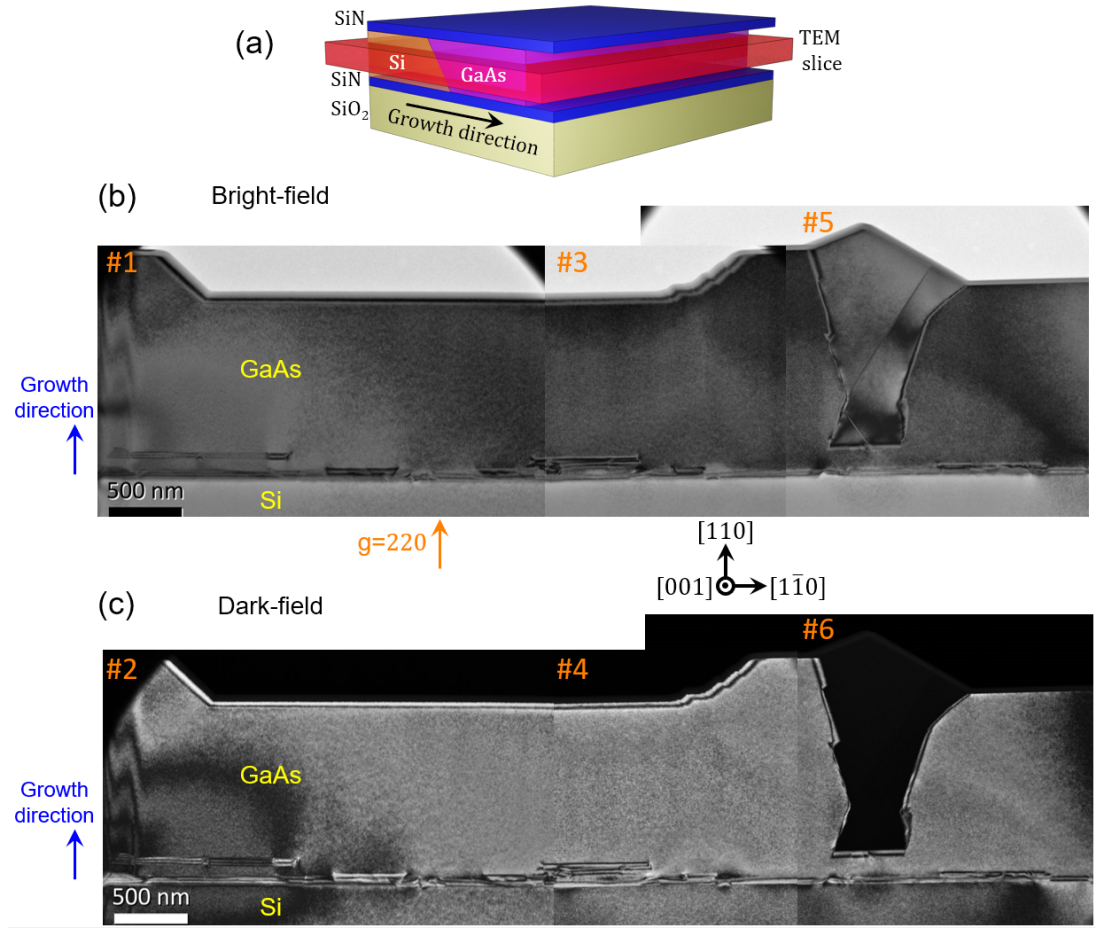

Figure 5.9: Plan-view TEM of tunnel epitaxy GaAs. a) A schematic illustrates the orientation of the plan-view TEM lamella along the [001] zone axis. The TEM lamella incorporates the entire GaAs layer. (b) Bright-field and (c) dark-field TEM montages, including both the Si and GaAs layer. The original TEM images 1-6 were acquired under a $g = 220$ diffraction condition.

More TEM investigations were conducted near the Si interface to understand the defect trapping effect from the lateral tunnel epitaxy. Using the same $g = 220$ condition, Fig. 5.10 (a) and (b) shows zoomed-in plan-view TEM images where planar defects close to the Si region were observed. These planar defects are stacking faults (SFs) and twins running parallel to the $\{1\,1\,1\}$ planes, and they terminate at the top SiN layer and buried oxide layer a short distance from the Si seed. Fig. 5.10 (c) and (d) present the similar

region but using the perpendicular $g = \bar{2}20$ diffraction condition. Dislocations, which were invisible under the previous $g = 220$ diffraction condition in Fig. 5.9 and 5.10 (a), now become visible with bright and dark contrast on the dislocation lines. As indicated by the red arrow in Fig. 5.10 (d), this contrast is due to the dynamical diffraction of electron beams in the TEM and indicates the dislocation lines are inclined through the TEM lamella [165]. In the same region, uniform moiré fringe can be seen due to the overlap between Si and GaAs lattices. The clearly distinguished moiré fringe indicates relaxation of the GaAs layer. In both $g = 220$ and $g = \bar{2}20$ conditions, all these crystalline defects are well confined within $250\ \mathrm{nm}$ distance from the Si seed. Beyond this localized defective interface, the GaAs main layer is free of any threading dislocations. The crystalline quality of the epitaxial GaAs was further examined by selective diffraction patterns taken from the GaAs and Si/GaAs interface along the $[0\,0\,1]$ zone axis, as shown in Fig. 5.10 (e) and (f). The kinematically forbidden 002 reflections which are absent in the Si diffraction pattern appear dim in GaAs due to the two sublattices being occupied by group III and group V elements [166]. At the Si/GaAs interface, both the Si and GaAs diffraction spots are noticeable, accompanied by some double diffraction, which manifests a little grid at each g-vector.

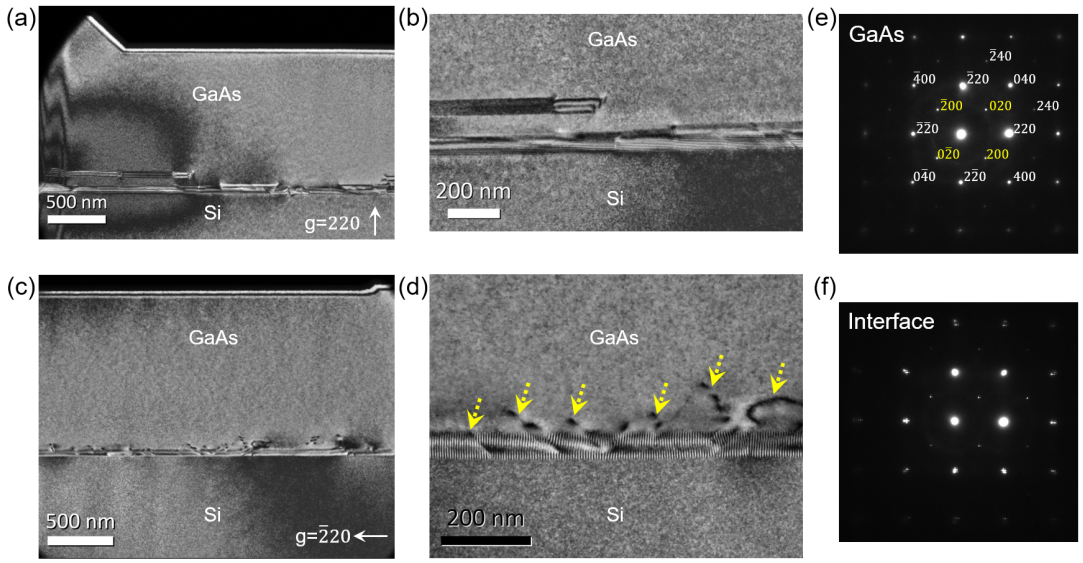

Figure 5.10: Plan-view TEM analysis for the confinement of dislocations and planar defects in laterally grown GaAs on SOI. (a) Dark-field plan-view TEM image ($g = 220$) encompasses both Si and GaAs regions. (b) An enlarged TEM image reveals planar defects confined near the Si region. (c) Dark-field plan-view TEM image ($g = \bar{2}20$) showing the confinement of dislocations near the Si interface. (d) A zoomed-in TEM image to show the propagation and effective trapping of dislocations. Plan-view electron diffraction patterns of the (e) GaAs and (f) Si/GaAs interface, respectively.

Fig. 5.11 (a) shows a cross-sectional TEM image along the lateral growth direction, where planar defects are present. A further zoomed-in image near the GaAs-Si interface is given in Fig. 5.11 (b). In this particular sample, an unintentional over-etch from HF resulted in an uneven SiO_2 surface beneath the GaAs. The yellow arrow in Fig. 5.11 (a) indicates a step at the bottom surface of the upper SiN layer, a structural imperfection from pattern fabrication. Planar defects appear to form near this area, a phenomenon often observed in other selective area heteroepitaxy [167, 168]. In Fig. 5.11 (b), the over etch of the buried oxide created a silicon corner (indicated by the white arrow in Fig. 5.11 (b)) and an undercut region. As a result, GaAs was able to grow under the bottom $(0\,0\,1)$ Si plane. Planar defects form at the tip of the Si corner,

running parallel to the 111 Si surface and terminating at the top SiN and bottom buried oxide layer. These observations highlight the impact of structural and morphological irregularities of growth patterns on generating new defects during lateral epitaxy, particularly stacking faults and twin defects. Fig. 5.11 (c) shows an electron diffraction image at the GaAs/Si interface with the Si and GaAs diffraction spots marked along with the associated orientation of crystal planes, confirming the zinc-blende phase of the epitaxial GaAs.

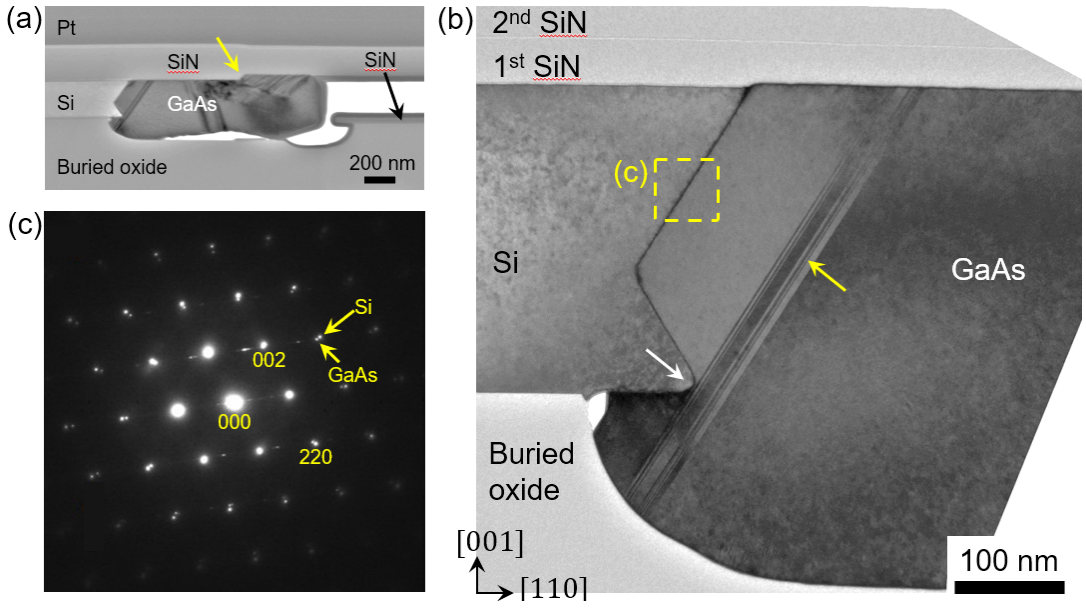

Figure 5.11: Cross-sectional TEM images of GaAs laterally grown on SOI. (a) Global-view and (b) zoomed-in TEM images. (c) Electron diffraction patterns showing both the Si and GaAs lattices, indicating the zinc-blende phase of GaAs.

InP epitaxy. The best InP sample was grown using a low-temperature nucleation layer followed by a higher temperature and flow step. The nucleation layer was grown at 460°, with a flow of 1.5 $\mu\mathrm{mol/min}$ for 12 minutes. The temperature is then ramped to 730°C for the next step. The flow is set to 25 $\mu\mathrm{mol/min}$ for 20 minutes. These growth parameters are similar to those found in literature [36, 169].

An SEM of the image is shown in Fig. 5.12. The growth front is not uniform implying

the nucleation is not uniform, or that there are different grains coalesced into a slab.

Selectivity is still not perfect, with deposition appearing mainly at the growth windows. On the planar SiN there is very little deposition, so we attribute the selectivity issues to fabrication related issues. We believe this to be mainly due to SiN roughness due to the window etch process and possibly exposed silicon close to the window due to etch mask misalignment.

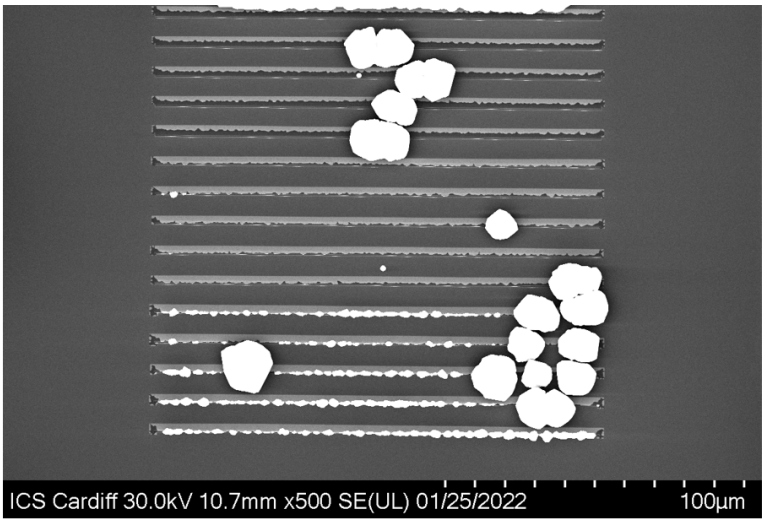

Figure 5.12: SEM image of InP laterally grown on SOI. Deposition on the mask is still visible. The InP can be seen growing out of the window for shorter tunnel lengths.

Cross-sectional TEM is used to investigate the growth of InP inside tunnels as well. A representative image is shown in 5.13. The growth time for this sample was too long, causing the epilayer to grow out of the tunnel through the window.

Due to the larger lattice mismatch between InP and Si, threading dislocations are observed appearing at the silicon seed interface. Due to the aspect ratio trapping mechanism, the dislocations do not propagate more than 500 nm from the silicon seed. One dislocation can be seen halfway through the tunnel, nucleated from the SiN tunnel wall. Most likely, this was caused by dust or debris left from the fabrication process.

Additionally, an untrapped planar defect can be seen propagating throughout the whole tunnel. The diffraction patterns show the crystallinity of different points in the structure. At the end of the tunnel, the InP diffraction pattern shows highly crystalline material, without stacking faults, grains or twin defects. Close to the silicon seed, the diffraction pattern is messier, implying the existence of multiple grains slightly rotated from each other. The silicon seed shows perfect crystallinity as expected, and shares an orientation with the epitaxial InP layer.

Another difference from the GaAs growth is the lack of microtwins close to the silicon seed. Because of this, the InP is epitaxially aligned with the silicon seed. This is confirmed by the dark field image, showing both InP and Si as bright, and the diffraction patterns showing the same orientation.

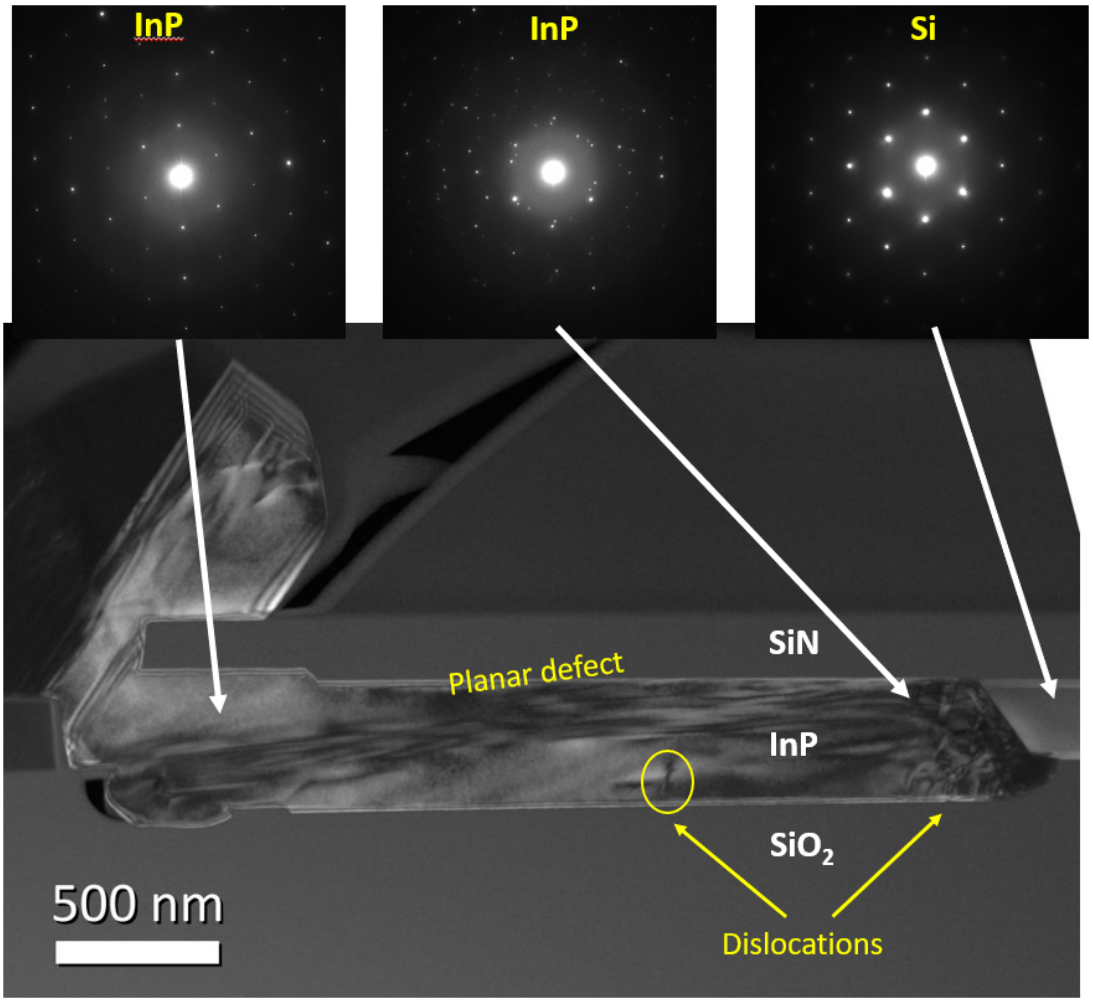

Figure 5.13: Cross-sectional dark field TEM images of InP laterally grown on SOI along with selective area diffraction patterns taken at the silicon seed, at the InP close to the Si interface and at the InP close to the end of the tunnel.

Optical characterization. Optical characterization of the epitaxial GaAs is measured using room temperature micro-photoluminescence. A continuous-wave 660 nm laser with a 10 µm diameter spot was used as the excitation source. The PL emission from the coalesced GaAs (as shown in the SEM photo in Fig. 5.7 (c)) appears to be very dim, likely attributed to regions with grain boundaries or twinning misorientations. Instead, PL spectra of the uncoalesced GaAs (as shown by the SEM photo in Fig. 5.7 (b)) were measured. Fig. 5.7 (a) shows the comparison of normalized

PL spectra from the GaAs on SOI and a reference semi-insulating (SI) undoped GaAs substrate at a low pumping power. The unintentionally doped (UID) GaAs grown via MOCVD typically exhibits n-type background doping, which could induce a blue shift in the PL peak due to the change in Fermi energy level [170, 171]. With the PL of the GaAs on SOI exhibiting a longer tail on the low-energy side, the extracted FWHM (60 nm) is larger than the value (22 nm) measured from the reference GaAs wafer. The broader PL is attributed to the presence of planar defects and associated type II band transitions near the GaAs/Si interface. As shown by the power-dependent PL of GaAs on SOI in Fig. 5.7 (b) , as the pumping density increases and the peak wavelength blue-shifts, the tail of the PL peak on the long-wavelength side gets more pronounced. Upon reaching a high pumping power of 46.1 $\mathrm{kW\,cm^{-2}}$, a saturation of the PL peak intensity is observed. Simultaneously, a side-peak at a more extended wavelength of 890 nm started to emerge. We associate this side-peak at the longer wavelength, particularly noticeable under high pump power, with the presence of planar defects near the Si interface [172].

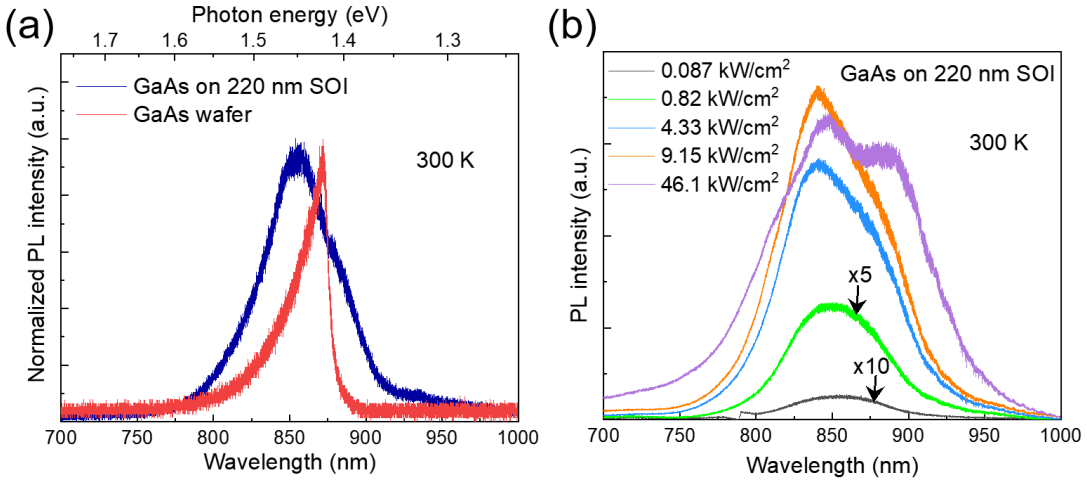

Figure 5.14: Optical characterization of laterally grown GaAs. (a) Normalized PL spectra of the uncoalesced GaAs on SOI, as shown in Fig. 5.7 (b), and commercial semi-insulating GaAs wafer. (b) Room temperature power-dependent PL spectra of the uncoalesced GaAs on 220 nm SOI.

Given the different material volume between the GaAs on 220 nm SOI and the GaAs wafer, an extremely low pumping power is used to probe the unintentionally doped (UID) GaAs on a 220 nm SOI as well as the reference semi-insulating (SI) GaAs substrate, as illustrated in Fig. 5.15 (a). Comparative analyses at increasing pump powers are presented in Fig. 5.15 (b-e). Interestingly, under low pump power, the GaAs on SOI manifests a substantially elevated PL intensity in comparison to the GaAs wafer (Fig. 5.15 (a)). As the pump power increases, the difference in the PL intensity between the GaAs on SOI and GaAs wafer decreases (see Fig. 5.15 (b-e)). This phenomenon could be attributed to two potential reasons: First, the n-type background doping in UID GaAs grown by MOCVD can contribute to enhanced PL intensity [169, 173]. Second, the distinct structural differences between the GaAs on SOI and the GaAs wafer can result in different pumping conditions. In the case of GaAs on SOI, it is feasible that multiple round-trip reflections of the pump light within the GaAs may occur. Such reflections are characterized by the pump light oscillating within the GaAs structure, facilitated by strong reflection at both the top GaAs/SiN and bottom GaAs/SiO_2 interfaces. This could be advantageous for the PL intensity of GaAs on SOI, especially when the pump power is low.

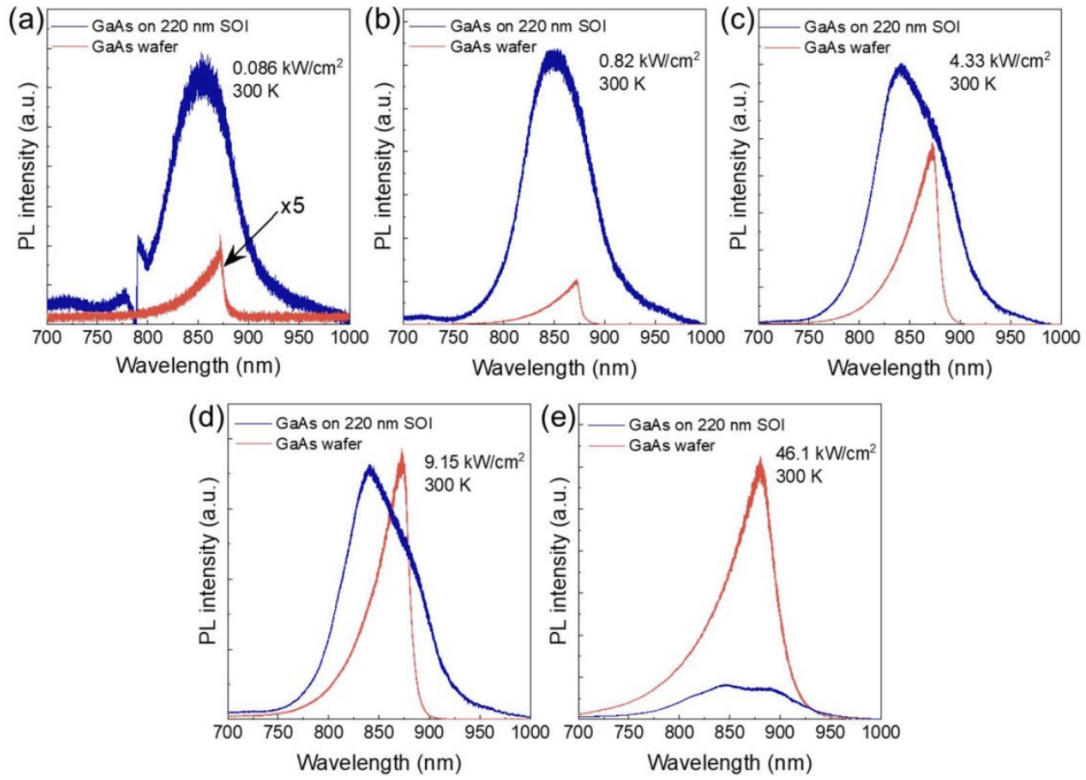

Figure 5.15: Power-dependent comparison between GaAs wafer and laterally grown GaAs.

5.7 Second generation tunnel epitaxy

To improve the uniformity of the growth inside tunnel patterns we needed a way to increase the uniformity of the nucleation layer, without losing selectivity. The second generation of tunnel epitaxy structure uses v-grooves as nucleation spots. V-grooves have been shown to yield very uniform growth even for very long structures [143, 167]. Work is still ongoing, but preliminary results show this technique is successful in improving the uniformity of InP epitaxy inside tunnel patterns.

A smooth nucleation for long trenches was achieved, as shown in Fig. 5.16 (a). Following the nucleation, uniform slabs of a few microns were grown, Fig. 5.16 (b), but good growth front uniformity was achieved only for shorter tunnels.

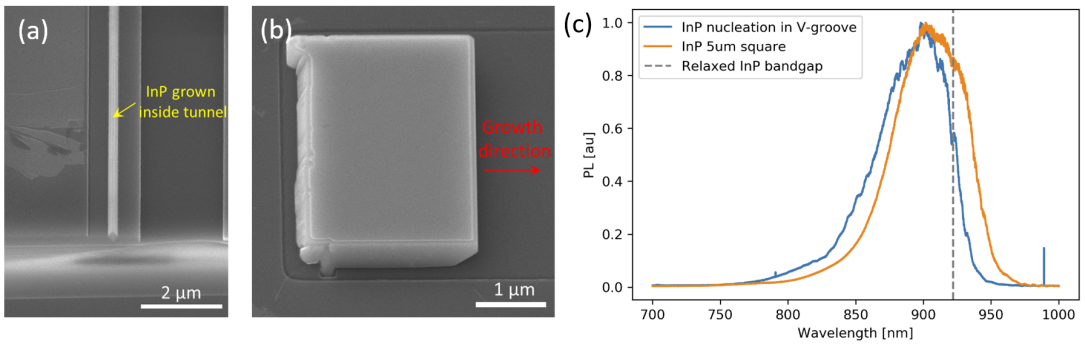

Figure 5.16: Second generation tunnel epitaxy showing (a) the v-groove nucleation and (b) the following confined in-plane growth. PL from the v-groove and the laterally grown InP is shown in (c).

Using a micro-PL setup, we measured the emission at different points on the sample, as shown in Fig.5.16. The emission is blue-shifted compared to the expected value for unstrained InP of around 922 nm. Compressive strain leads to a shifting of the electronic bands and to a widening of the band gap [174, 175]. The nucleation region is more blue-shifted, implying that it is more compressively strained. As the InP continues to grow laterally, the strain is relaxed, leading to less blueshift. However, even after a few microns of growth, the strain does not appear to be completely relaxed.

5.7.1 Contributions

Significant contributions to the work presented in this chapter have been made by a number of people. Dr. Oumaima Abouzaid and Dr. Zhao Yan helped with sample growth by operating the MOCVD reactor for the samples presented. The tunnel epitaxy patterns were fabricated at the University of Southampton, with Dr. David Thomson, Prof. Graham Reed, Dr. Martin Ebert and Dr. Weiwei Zhang, Dr Qiang Li, and Dr. Zhao Yan collaborating on the design and fabrication. Dr Zhao Yan proposed and did initial design for the second generation tunnel epitaxy. TEM measurements were done by Dr. Richard Beanland. Parts of this chapter are based on a manuscript written by

Dr. Zhao Yan.

Analysis of the data measured by others was done by the author, as well as all work not highlighted here.

Chapter 6

Conclusions and future work

To address the industrially relevant problem of integrating telecom-wavelength lasers to silicon photonics cirtuicts, this thesis investigated three different ways of epitaxially integrating III-V lasers on an SOI silicon photonics platform. The advantages and disadvantages of each technique were presented, both from a materials and device perspective.

Using a novel thick InAsP defect filter layer, a low threading dislocation density of $7.3 \times 10^7 \mathrm{cm}^{-2}$ using a total buffer thickness buffer of under 2 $\mu\mathrm{m}$. A new technique for increasing the gain and decreasing the spectral width of quantum dots was investigated, showing that stopping the arsenic flow during the self assembly process has the potential of improving dot quality.

Surface emitting photonic crystal lasers are fabricated using inherently TD-free InGaAs nanowires. By deforming the perfect honeycomb lattice, the photonic band edge flattens at the Γ point, resulting in increased gain. A low threshold of 1.25 $\mu\mathrm{J}\,\mathrm{cm}^{-2}$ is achieved through a combination of high nanowire unfiformity, low optical substrate losses and increased gain due to the flat band edge mode. Additionally, curved photonic crystal laser are demonstrated for the first time. Due to whispering-gallery modes, the Q-factor of the resonant cavity is largely independent of the bending radius, allowing for arbitrarily shaped laser cavities and high Q ring resonators with small footprint.

By changing the growth direction from horizontal to lateral and employing an aspect ratio trapping technique, large area III-V layers are grown on SOI. Extensive charac-

terisation is performed to verify the defect trapping mechanism using TEM and PL.

Applications. While neither approach provides a perfect solution to the III-V on SOI integration problem, each approach has particular suitable use cases. For high power lasers coupled to a waveguide, the most suitable approach is growth in pockets, using defect filter layers and quantum dots. This method is not limited by area, like tunnel epitaxy, and can easily be pumped electrically, unlike nanowires. The biggest downside for this application is the low lifetime due to the dislocations, and the relatively low coupling coefficient to the waveguide. For free-beam applications such as LIDAR, a surface emitting photonic crystal nanowire integration approach would be favourable, if electrical pumping can be achieved. There is no area limitation, with entire wafers covered in nanowire being possible. Beam quality and cavity Q-factor increase with higher area. The main advantage over pocket growth is the lack of defects, increasing the lifetime and efficiency of the laser. A pocket approach would also require multiple additional processing steps to fabricate a photonic crystal. For high efficiency coupling with silicon photonics waveguides, a lateral growth approach would be best. Tunnel epitaxy places the defect-free III-V layers in direct contact with the silicon waveguide layer, allowing for very high coupling efficiencies. Applications include energy efficient lasers and high speed modulators. Pocket growth has low coupling efficiency due to the air gap between the III-V and the waveguide, and nanowires suffer from height mismatch with the silicon surface. However, nanowires could perform well for these applications in a fully photonic crystal based circuit.

6.1 Future work

To bring these techniques to an application-ready stage, where they are efficient and reliable enough for industrial adoption, further research is required. The future work presented in this chapter focuses more on short-term research into improving the ma-

terial quality. Once the material quality is at an acceptable level, more detailed studies on the large scale integration and manufacturing can be performed.

6.1.1 Large area epitaxy

Defect filter layers. Further optimization of the defect filter layers is possible. Growth temperature variation, DFL composition and thickness variation, and DFL stacking studies are all promising routes to achieving lower defect densities. Quantum dot defect filter layers are another possible avenue of progress.

In the shorter term, cross-sectional TEM studies are required to confirm the defect filtering and creation mechanisms. This could provide information to explain why going from two to three DFLs does not change the TDD. Moreover, the stacking fault formation mechanism and preferential directionality could be investigated using TEM.

Quantum dots. The next steps are investigating the defect resistance of the optimised QD sample by growing it on our InP/Si template. By combining a defect resistant gain medium with an effective defect filter layer we expect to be able to fabricate electrically driven lasers on silicon wafers. Initial study began in this area, but issues with surface roughness and stacking faults affecting the dot nucleation occurred. Possible solutions involve optimising the DFL to decrease surface roughness or adjusting the QD growth recipe to account for the new surface.

Silicon photonics integration. For these techniques to be useful they must be integrated on a silicon photonics platform. The thick DFL buffers make evanescent coupling impossible for planar growth. Selective area epitaxy can be used to define sunken pockets on SiPh wafers, which makes it possible to grow the gain material level with the waveguide layer. This technique has shown good results in recent years [68–70].

Through collaboration, we received templates of MBE grown III-V on Si in patterned sunken pockets. Future work on this platform includes optimising our defect filter layers and quantum dots for this novel selective area epitaxy approach.

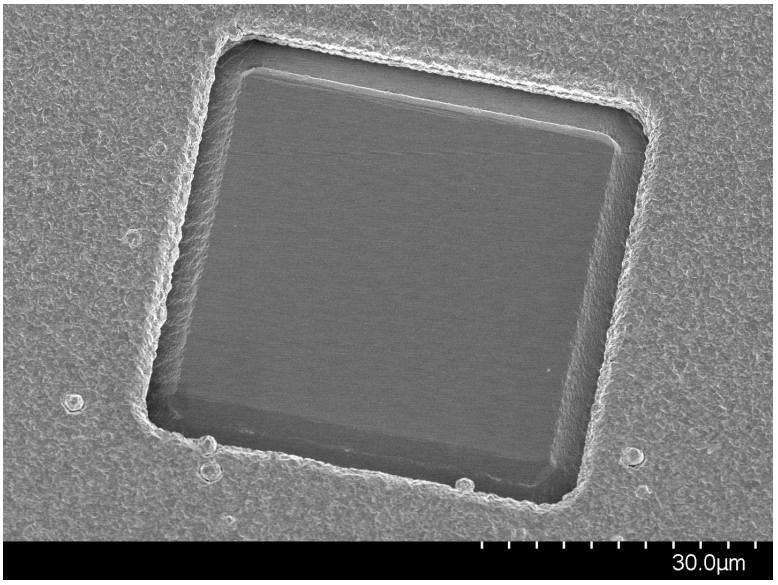

Figure 6.1: MBE grown selective area epitaxy sunken pocket template for silicon photonics integration.

6.1.2 Nanowires

Epitaxy. Further optimisation of the epitaxy procedure is needed to improve nanowire uniformity. Possible improvement routes include variation studies of growth temperature and growth rate of the GaAs and InGaAs layers, variation of indium composition or use of high indium content quantum confining structures. Using surfactants such as antimonides can also be investigated as a means of controlling the growth.

Device opportunities. Future work on this topic can make use of the lack of bending losses to create microring lasers with very small footprint and high Q factor. Arbitrary cavity shape lasers could also be developed for use in interferometers or microfluidic biosensing.

Topological devices. Studies are ongoing on the topological laser devices shown in Fig. 4.5. We have proven that scattering occurs at the edge between the two PhC, but we were unable to prove the existence of the topological edge mode. Moreover, we were unable to prove the air-mode nanowire waveguide or the coupler function. Improvements can be made by further simulation studies to design better patterns that take into account the larger nanowires due to the pattern edge growth rate difference. Moreover, individual devices should be fabricated so they can be tested individually, independent of the larger system. Improvements in the photoluminescence setup are also required for better characterization.

Optical characterization. Two upgrades to the optical table setup are currently ongoing. A laser divergence measurement can be done by measuring the Fourier plane of the tube lens. At the Fourier plane, the position of a beam spot can be precisely correlated to a propagation direction, making it possible to measure the divergence of a surface emitting laser. Difficulties in setting this up involve compatibility issues with the inner optics of the spectrometer. Possible solutions involve using an external detector simultaneously with the spectrometer, or integrating a motorized fibre collection system which can raster scan through beam space.

The second upgrade involves integrating a spatial modulator beam shaper into the setup. By shaping the pumping beam to match the shape of the topological edge mode, we can selectively excite it to confirm its existence and measure its properties. Difficulties lie in the live modelling of the beam shape to match the rotation and scale of the hexagon. These issues could be tackled by use of an automated script which makes it easy for the user to change the beam shape.

6.1.3 Tunnel epitaxy

Epitaxy. Finding the right parameters for good nucleation is crucial in achieving large-area defect-free growth. Growth studies involving variations of growth temper-

ature, growth rate and V/III ratio can be used to find an optimised recipe. The use of antimonide surfactants or various low-temperature nucleation materials such as InAs, AlAs, or GaP can also be investigated as a means to increase growth selectivity and improve nucleation uniformity.

Quantum confining structures such as quantum wells or quantum dots could be grown on this platform. Vertical overgrowth of quantum dots is a particularly promising research direction, as this type of structure has never been achieved before.

XRD studies. To better understand the strain relaxation mechanism inside the seed and the lateral growth, reciprocal space mapping using XRD can be used. By sampling the reciprocal space at various points on the sample, and at different points during growth, we can investigate how and where the relaxation occurs.

TEM studies. The threading dislocation termination of the second generation epitaxy has not been yet verified using TEM. Moreover, TEM can provide further insights into the types of defects present in the second generation, making a comparison with the first generation possible.

Simulations. Simulations can be used to understand and find the best device parameters for this new platform. Possible progress paths include resonant cavity simulations, electrical pumping and current flow simulations and thermal simulations. These simulations can inform device design for lasers and modulators, and open the door to new applications such as photodetectors and transistors.

Device opportunities. Small, optically pumped devices such as microrings could be achieved using the second generation platform. Vertical overgrowth can be investigated as a means of expanding the available III-V volume for better optical confinement. Electrically pumped lasers and modulators are the natural progress paths for further research.

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