Active Thermal Sharing Control for a Cascaded Converter in Medium-Voltage Applications

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***Abstract* — The cascaded three-level neutral-point-clamped (C3L-NPC) converter has been adopted in practical projects for power transmission in medium-voltage distribution networks. However, this type of converter comprises multiple submodules (SMs) in which thermal imbalance may occur due to a mismatch between component parameters of the SMs. This may lead to decreased system reliability. To address this shortcoming, an active thermal sharing control strategy for C3L-NPC converters is presented in this paper. A thermal control loop is incorporated into the inner current controller within each SM. Active and reactive power regulation is conducted based on the individual junction temperature of each SM. A high-level controller is used to regulate the total power and to calculate the temperature reference. The control strategy enables decoupled thermal and power regulation, and each control loop can be independently designed. The effectiveness of the approach has been experimentally validated using a testbed down-scaled from the ANGLE-DC project—the first operational medium-voltage dc link in Europe. It is shown that the junction temperature of the SMs is effectively balanced without affecting the output power under cooling system failures.**

***Index Terms* — medium-voltage direct-current, cascaded three-level neutral-point-clamped converters, junction temperature, active thermal sharing control.**

I. Introduction

POWER electronic converters are key components of medium-voltage direct-current (MVDC) distribution networks. They connect distributed generators and energy sources to the grid, offering high efficiency, high power quality, and fault-ride-through capabilities. However, reliability is an important performance criterion affecting converter design and control [1], [2]. Around 55% of the failures in power electronic converters are caused by temperature-related issues [3]. High mean temperatures and temperature fluctuations can cause fatigue and damage in the packaging of the semiconductor materials—leading to bond wire lift-off and solder crack.

Power converters are normally connected in parallel to achieve high current ratings or in series for high voltage ratings. Even when all submodules (SMs) within a converter may operate at even loading or under voltage sharing control, the thermal stress for each SM may be different. This may be due to a mismatch in component parameters and/or to different individual cooling system conditions [4]. Given that the lifetime of converter systems is determined by the first failed SM, temperature imbalance may result in premature damage of certain SMs—decreasing, in turn, the overall lifetime of the system [5].

Active thermal control addresses the reliability issues just discussed. Active thermal control methods are categorized into device-level, converter-level, and system-level approaches [6], [7]. For a single SM, an often-adopted device-level approach is to modify the switching modulation by using discontinuous pulse-width modulation (D-PWM) [8] and injecting zero-sequence current [9]. The current flow path is changed so that the semiconductor device with the highest temperature is not switched on and does not conduct. Through this approach, the thermal stress is distributed to other switching components within the same SM. However, by incorporating D-PWM, the harmonic performance of the output current and voltage may be affected [8]. In addition to D-PWM and zero-sequence injection, an active gate driver can be used to regulate junction temperature. In [10], a two-step gate driver was designed to actively adjust the device's switching and conduction losses, thereby minimizing thermal cycling of the solder. For the converter-level control, junction temperature is controlled by modifying the switching frequency and limits of the current controller, with junction temperature being estimated through a Luenberger closed-loop observer [11]. These control structures typically use proportional-integral (PI) based closed-loop controllers, which do not allow for precise regulation of thermal stress in specific semiconductors for H-bridge or three-phase converters [11], [12]. To achieve more accurate junction temperature control, finite control-set model predictive methods are employed [13]. These methods enable optimal selection of the switching vector to reduce thermal stress in specific semiconductors.

An effective method, named power routing, redistributes the power among different SMs according to their thermal conditions [14], [15]. The SM with the highest temperature is allocated the least power and vice versa, enabling thermal stress to be shared equally. The device junction temperature is estimated based on its power losses and thermal impedance [16]. The conduction loss is mainly related to the current and

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voltage drop across the device, whereas the switching loss is related to the switching frequency and dc voltage [17].

Power routing has been widely adopted in cascaded H-bridge (CHB) converters and interleaved dual-active-bridge (DAB) dc/dc converters [18], [19]. The power references sent to the SMs are inversely proportional to their individual accumulated damage, which represents the product life consumption. The accumulated damage is first estimated using the rain flow-counting algorithm and Miner's rule. It is then updated after a fixed period. A virtual resistor, whose resistance is a function of the accumulated damage, is then used to distribute the power references to the SM controller. This method also applies to smart transformers, where the SMs for CHB and DAB converters are in a series connection [20], [21].

Given it is not sufficient to address thermal issues only when the overheated SMs of CHB and DAB converters are in different paths, power routing may be also used in combination with D-PWM [22]. The overheated SM in a CHB converter is thermally compensated by adjusting the clamped phase angle of the D-PWM to reduce the switching losses, while for a DAB converter, the SM is compensated by adjusting the power reference.

In the literature, the concept of power routing has been extended to the thermal management of grid-connected converters in microgrids [23]-[25]. Since these converters always adopt decentralized control without communication, temperature–power based droop control strategies are used to achieve an equal thermal distribution [23], [24]. In [23], the droop coefficient of the converter is adjusted through online monitoring of the line-frequency component of junction temperature ripples. Thus, reliability is enhanced compared with conventional decentralized power sharing strategies. In [24], a lifetime-oriented droop controller is developed based on the relationship between the temperature and output power.

In an MVDC link connecting to distribution networks, modular multilevel converters (MMC) and cascaded three-level neutral-point-clamped (C3L-NPC) converters constitute two candidate technologies to build up the dc voltage. The C3L-NPC converter was adopted in the first MVDC demonstration project in Europe, the ANGLE-DC project [26], [27]. It has a significantly lower cost compared with an MMC, although at the expense of slightly lower efficiency and reliability [28]. For MMCs, thermal imbalance among SMs could be more than 20% [1]. In [29], an active thermal balancing algorithm is proposed for MMC, demonstrating effective performance in SM capacitor voltage balancing while also reducing the computational burden. To optimally balance the thermal stress among SMs, a sorting method can be used considering a weighting trade-off between the capacitor voltage and thermal balancing control loops [30]. By using this method, the lifetime of the first failed power semiconductor device may be increased by 50%. In [31], PI control is used to balance the junction temperature of SMs in an MMC. A control loop is superposed on the capacitor voltage controller to adjust the dc voltage of the SMs, hence adjusting the power losses. However, the conduction losses in MMCs are dictated by the arm current magnitude and these are nearly equal in all SMs, so only the switching losses can be adjusted by regulating the dc voltage.

To date, suitable thermal control strategies for C3L-NPC converters have not been yet investigated. The existing active

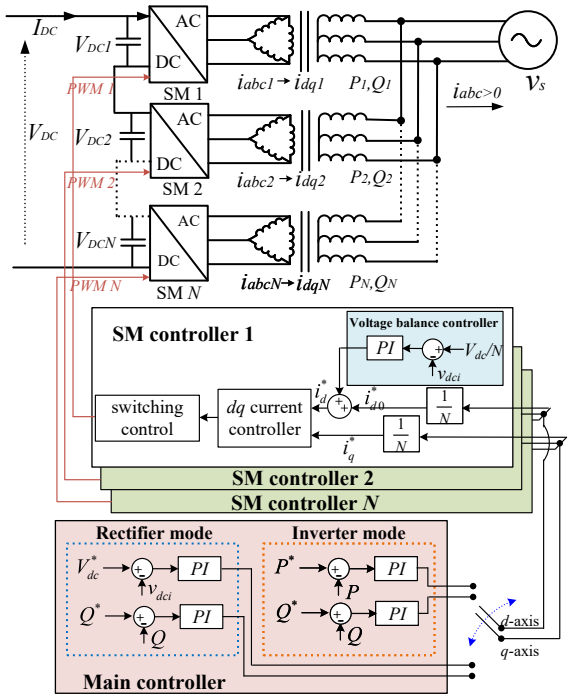


Fig. 1. Traditional dc voltage and power control of C3L-NPC converters.

thermal control methods cannot be directly adopted in the C3L-NPC converter due to the following key aspects. Firstly, the control structure differs because each SM in the C3L-NPC operates as an independent ac/dc converter requiring a dc voltage controller to regulate active power due to the series connection of the dc link. Secondly, the minimal dc voltage margin requirement is unique. Each SM must maintain a minimum dc voltage, and if the dc voltage of one SM increases, the dc voltage of another SM must decrease to maintain the total dc link voltage constant. This requirement differs from other topologies and needs careful reassessment to avoid instability. Thirdly, the simultaneous control of both active and reactive power has been achieved for the C3L-NPC converter, unlike prior references that primarily focused on active power regulation. This additional degree of freedom in reactive power control adds complexity and requires specialized considerations.

This paper presents an active thermal sharing control scheme for C3L-NPC converters. A PI-based thermal controller is embedded in each SM to adjust active and reactive power concurrently. A high-level main controller is used to set the mean temperature of the SMs as the reference to SM controllers. In addition, the thermal control capability is considered. To ensure the stable operation of the system, the main controller modifies the temperature references once the outputs of the SM's PI controllers reach the upper or lower boundary. To facilitate control design, an electro-thermal model of the system was developed. Tuning of the thermal controller was conducted using the frequency response of the system.

The main contributions of the paper are threefold and are detailed as follows:

1) The method allows flexible control of both active and reactive power to redistribute thermal stress among

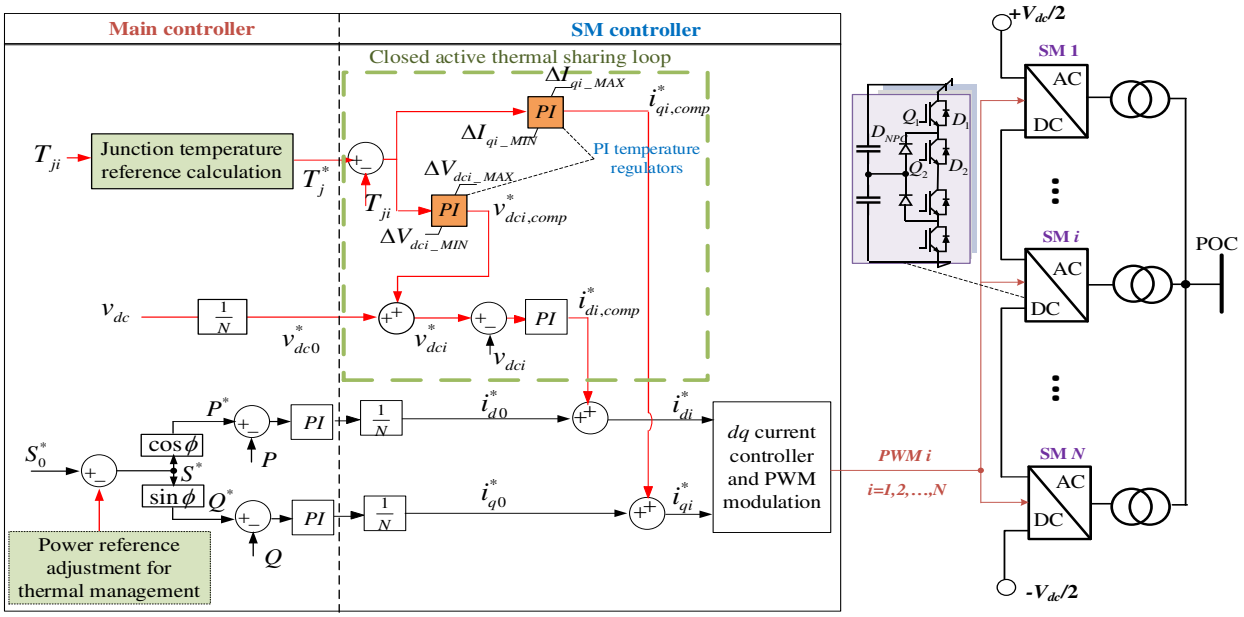


Fig. 2. Thermal sharing control schematic of the MVDC system with N cascaded SMs.

SMs. This is achieved through specific design of the active and reactive regulation control loops, with active power regulated by controlling the dc voltage of the SMs and reactive power directly regulated by controlling the reactive current.

2) The method ensures power redistribution among SMs without affecting the total output power, thereby achieving decoupling between thermal sharing control and power control.
3) The minimal dc voltage margin of a SM is considered. When this margin is reached, decoupling performance deteriorates, potentially leading to instability. To address this, the temperature reference is selected as the mean temperature of the remaining SMs instead of the mean temperature of all SMs.

The control strategy was experimentally validated using a laboratory-scale MVDC testbed down-scaled from the real ANGLE-DC project. It is shown that the junction temperature of the SMs is effectively balanced when cooling system failures occur in the SMs.

II. Control of Medium-Voltage C3L-NPC Converters

A C3L-NPC converter system consists of N three-phase individual SMs. The dc terminals of the SMs are connected in series to build a medium-voltage (MV) level dc voltage, and the ac sides are connected in parallel. Fig. 1 shows the main circuit and the conventional control schematic of the power control station. The dc link voltage is controlled by the dc voltage control loop in the other converter station.

The control scheme contains both SM controllers and a main controller. The SM controller regulates dq components of each SM's current (i_d and i_q) and generates PWM switching signals. The reference currents (i_d^* and i_q^*) are the sum of the outputs of an embedded dc voltage balancing controller and the main controller. The voltages of the SMs are balanced using the voltage balancing controller. The main controller regulates the total dc voltage and reactive power or the total active and reactive power of the system. The outputs of the main controller are divided by N to ensure an equal sharing of loads ($P_1 = P_2 = \cdots = P_N$) and dc voltages ($V_{dc1} = V_{dc2} = \cdots = V_{dcN}$) [32].

III. Active Thermal Sharing Control Method

In ideal conditions, the equal sharing of power and voltage balances the current and voltage of the SMs and, thus, the thermal stress will also be evenly shared. However, in practice, the thermal stress may be unbalanced due to mismatched component parameters or cooling system failures. This will further lead to different degradation rates of SMs, large maintenance times, and a reduction in system reliability.

To relieve the consequences caused by the thermal imbalance, a novel active thermal sharing control method is presented. The method consists of three components. Firstly, an active thermal sharing loop is used to achieve thermal balance. Secondly, considering the control limitations arising from the required minimum dc voltages of SMs, the junction temperature reference is modified according to the operating conditions. Thirdly, in the event of overheating, the amount of power that should be reduced is selected based on the thermal model to guarantee that the temperatures of all SMs are regulated below a maximum allowable value (i.e. 150 °C).

A. Active thermal sharing control loop

1) Control loop structure: The active thermal sharing control loop is enclosed by the green dashed block in Fig. 2. The junction temperature reference T_j^* is calculated by the main controller and sent to the thermal sharing control loop of each SM. T_j^* is the average junction temperature of all SMs. T_{ji} traces T_j^* through a closed loop, where T_{ji} is the junction temperature of the i^{th} SM. The error between T_j^* and T_{ji} is eliminated by two PI controllers, which generate compensating references for active and reactive power. As the active power of each SM is proportional to its dc voltage, the d-axis variable $v_{dci,comp}^*$ is added as a compensation term to the dc voltage

controller to regulate active power. Similarly, the q-axis variable $i^*_{qi,comp}$ is added as a compensation term to the q-axis current control loop to regulate reactive power. Through this configuration, thermal stress is equally distributed for all SMs.

The lifetime of a converter is restricted by the most severely heated components. Thus, T_{ji} may be selected as the junction temperature of the most heated component of the i^{th} SM [31]. However, as each SM is formed by 30 individual devices (4 IGBTs and 6 diodes per phase), it would take significant time to calculate all junction temperatures to identify the device exhibiting the highest temperature. For simplicity, a three-phase balanced condition and no drift in the neutral-point voltage are assumed. In this case, the devices of one bridge arm only (Q_1, Q_2, D_1, D_2 and D_{NPC} in Fig. 2) are sufficient to represent the thermal condition of an SM due to the symmetrical structure of the converter. Thus, T_{ji} is obtained as:

$$T_{ji}=\max\{T_{Q_1}i, T_{Q_2}i, T_{D_1}i, T_{D_2}i, T_{D_{NPC}}i\} \quad (1)$$

where $T_{Q_1}i$, $T_{Q_2}i$, $T_{D_1}i$, $T_{D_2}i$ and $T_{D_{NPC}}i$ are the junction temperatures of the five devices.

2) Modeling of power loss and junction temperature: The IGBT module F3L75R07W2E3_B11 is used and its parameters at 25℃ are given in Table I [34]. T_{ji} is determined based on the device's power losses, which include both the conduction and switching losses.

TABLE I.
PARAMETER OF IGBT MODULE F3L75R07W2E3_B11 [34].

IGBT	Value	Diode	Value
V_{ce0}	0.772 V	V_{f0}	0.83 V
R_{ce}	3.29 mΩ	R_f	2.22 mΩ
$E_{on}+E_{off}$	3.5 mJ	E_{rec}	5.9 mJ
$R_{th,1,Q}$	0.051 K/W	$R_{th,1,D}$	0.097 K/W
$\tau_{th,1,Q}$	5×10^{-4} s	$\tau_{th,1,D}$	5×10^{-4} s
$R_{th,2,Q}$	0.117 K/W	$R_{th,2,D}$	0.219 K/W
$\tau_{th,2,Q}$	5×10^{-3} s	$\tau_{th,2,D}$	5×10^{-3} s
$R_{th,3,Q}$	0.426 K/W	$R_{th,3,D}$	0.576 K/W
$\tau_{th,3,Q}$	0.05 s	$\tau_{th,3,D}$	0.05 s
$R_{th,4,Q}$	0.506 K/W	$R_{th,4,D}$	0.508 K/W
$\tau_{th,4,Q}$	0.2 s	$\tau_{th,4,D}$	0.2 s

The real-time power loss calculation $P_{loss,x}$ of device x (for Q_1, Q_2, D_1, D_2 or D_{NPC}) over a fundamental period is given in [33]. For simplicity, $P_{loss,x}$ is represented by a 2nd order polynomial as a function of active and reactive power, given as:

$$P_{loss,x} = a_{1,x}P_i + a_{2,x}P_i^2 + a_{3,x}P_iQ_i + a_{4,x}Q_i + a_{5,x}Q_i^2 = f_{loss,x}(P_i, Q_i) \quad (2)$$

Vector $\mathbf{a}_x = [a_{1,x}, a_{2,x}, a_{3,x}, a_{4,x}, a_{5,x}]$ is formed with the coefficients in (2), which in turn result from polynomial fitting.

The thermal impedance network shown in Fig. 3 is suitable for both IGBTs and diodes. There are four layers of impedance, each with a different time constant, and the thermal capacitance is calculated as $C_{th,i} = \frac{\tau_{th,i}}{R_{th,i}}$. Since the thermal impedance from the case to the heatsink $R_{th,CH}$ is significantly smaller compared to that from the junction to the case $R_{th,JC}$, $R_{th,CH}$ is not taken into account.

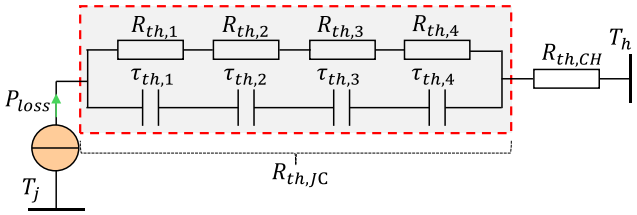


Fig. 3. Thermal impedance network of semiconductors.

At steady-state, the junction temperatures of the IGBTs and diodes are calculated based on a 1-D lumped thermal network with the thermal capacitance being omitted [31], given as

$$T_{j,x} = P_{loss,x}(R_{th,JH,x} + R_{th,HA}) + T_{jA} \quad (3)$$

where $R_{th,JH,x} = (R_{th,1,x} + R_{th,2,x} + R_{th,3,x} + R_{th,4,x})$ is the total thermal resistance from junction to heatsink, $R_{th,HA}$ is the thermal resistance of the heatsink to the ambient air, and T_{jA} is the ambient temperature.

B. Thermal control limitation analysis

1) Thermal control limitation: Thermal regulation is limited to the adjustable range of active and reactive power among SMs. Assuming some SMs are overheated by ΔT_j, their junction temperature ($T_{j,oh}$) will be equal to that of normal SMs ($T_{j,nom}$) after applying the thermal sharing control method. Based on (3),

$$P_{loss,nom}R_{th,nom} = P_{loss,oh}R_{th,oh} + \Delta T_j \quad (4)$$

where $P_{loss,nom}$ stands for the power losses of the most heated components in the normal SMs and $P_{loss,oh}$ in the overheated SMs. $R_{th,nom} = R_{th,JH,nom} + R_{th,HA}$ and $R_{th,oh} = R_{th,JH,oh} + R_{th,HA}$ are the thermal resistances of junction to the ambient air of the corresponding components. $P_{loss,oh}$ has a lower boundary $P_{loss,min}$ which is determined by the minimum allowable power of an SM, $P_{i,min}$ and $Q_{i,min}$. As the remaining power is redistributed equally to the normal SMs, their active and reactive power are $\frac{P-mP_{i,min}}{N-m}$ and $\frac{Q-mQ_{i,min}}{N-m}$, where m is the number of overheated SMs, and $P = \frac{3}{2}V_dI_d$ and $Q = \frac{3}{2}V_dI_q$ are the active power and reactive power of the converter. As the reactive power of each SM can be reduced to zero, the minimum reactive power and minimum current, $Q_{i,min}$ and $I_{qi,min}$, are then zero. The minimum active power $P_{i,min}$ is proportional to the minimum dc voltage $V_{dci,min}$ of the SM, and this is given as:

$$P_{i,min} = V_{dci,min}I_{dc} = V_{dci,min}\frac{P}{V_{dc}} \quad (5)$$

where $V_{dci} = \frac{V_{dc}}{N}$ is the dc voltage of the i^{th} SM and V_{dc} is the total dc link voltage. $V_{dc,min}$ should be no less than the peak ac voltage, but it should provide sufficient margin for the required power. Thus, $V_{dc,min}$ is expected to provide a voltage of $V_s = 1.2$ p.u. to satisfy Grid Code requirements [35]. The maximum value of ΔT_j to meet the condition for temperature equal sharing is obtained by combining (2)−(5) as:

$$\Delta T_{j,max} = f_{loss,nom}\left(\frac{\left(N-m\frac{V_{dc,min}}{V_{dc}}\right)^P}{(N-m)N}, \frac{Q}{N-m}\right)R_{th,nom} - f_{loss,oh}\left(\frac{V_{dc,min}{}^P}{NV_{dc}}, 0\right)R_{th,oh} \quad (6)$$

where $V_{dc,min} = 1.2 \times 2 \times \sqrt{2}NV_s^{sec}$ and V_s^{sec} is the ac voltage at the secondary side of the isolation transformer at the converter side (i.e. low voltage rating). In (6), $f_{loss,nom}$ and $f_{loss,oh}$ are the polynomial functions used for fitting the power losses of the normal and overheated SMs. The equation indicates that if the increased temperature of the overheated SMs exceeds $\Delta T_{j,max}$, the thermal sharing control limit has been reached. Thus, equal temperature sharing cannot be achieved. This unequal sharing condition should be considered in the reference calculation of the junction temperature.

2) Reference calculation of junction temperature: If $\Delta T_j \leq \Delta T_{j,max}$, the saturation of the temperature PI controller of an SM is not reached and the controller output is proportional to the error between the junction temperature and its reference. In this condition, T_j^* is selected as the mean value of T_{ji} $(i = 1,2,\dots,N)$ to avoid interfering with the dc voltage and power. Assuming identical proportional and integral gains for all PI controllers, the sums of the compensation terms are:

$$\mathbf{X}_{comp,sum} = \mathbf{G}_{th,sum}(s)\left(T_j^* - T_{ji}\right) = \mathbf{0}_{1\times 2} \quad (7)$$

where $\mathbf{X}_{comp,sum} = \left[\sum_{i=1}^{N} v_{dci,comp}^* \quad i_{qi,comp}^*\right]$ is a vector with the sums of the compensation terms. $\mathbf{G}_{PI,th,dq}(s) = \left[\sum_{i=1}^{N} G_{PI,th,d}(s) \quad \sum_{i=1}^{N} G_{PI,th,q}(s)\right]$ is a vector with the sums of transfer functions of the PI controllers as entries. $\mathbf{0}_{1\times 2} = [0 \quad 0]$ is a vector with zero entries. From (7), it can be seen that the sums of $v_{dci,comp}^*$ and $i_{qi,comp}^*$ are zero, which implies that the thermal control does not influence the dc link voltage or the total power.

As discussed previously, when ΔT_j is greater than $\Delta T_{j,max}$, the thermal control limit is reached. Under this condition, the output of the temperature PI controller of the overheated SMs will decrease to its lower limit. Thus, if T_j^* were still set as the mean value of T_{ji}, the sums of $v_{dci,comp}^*$ and $i_{qi,comp}^*$ in (7) would be non-zero and the thermal control would interfere with the dc voltage and total power regulation. To prevent this, T_j^* is selected as the mean temperature of the remaining (N-m) SMs instead of the mean temperature of all SMs. The temperature reference is thus modified as:

$$T_j^* = \frac{\sum_1^{N'} T_{jm}}{N'} \quad (8)$$

where T_{jm} is the temperature of the m^{th} SM that meets either $v_{dci,comp}^* \geq \Delta V_{dci,MIN}$ or $i_{qi,comp}^* \geq \Delta I_{qi,MIN}$, and N' is the number of SMs that meet such a constraint. Here, $\Delta V_{dci,MIN}$ and $\Delta I_{qi,MIN}$ are the limit values of the temperature PI controllers as shown in Fig. 2. In turn, $\Delta V_{dci,MIN} = V_{dci,min} - V_{dc0}^*$ and $\Delta I_{qi,MIN} = I_{qi,min} - I_{q0}^* = -I_{q0}^*$, and their values are selected according to the allowable minimum active and reactive power. To ensure $v_{dci,comp}^*$ and $i_{qi,comp}^*$ reach their minimum values at the same time, the ratio of the gain of the d-axis and q-axis PI controllers is selected as $\frac{G_{PI,th,d}(s)}{G_{PI,th,q}(s)} = \frac{|\Delta V_{dci,MIN}|}{|\Delta I_{qi,MIN}|}$.

C. Thermal management by power adjustment

In the event of severe overheating, the highest temperature among SMs $T_{ji,max}$ may exceed the maximum allowable junction temperature $T_{j,MAX}^*$ even if a thermal control scheme is implemented. Thus, the power output of the cascaded converter must be reduced to avoid damaging the SMs. This is achieved by decreasing the apparent power setpoint S^*. To do this, T_{ji} of all SMs is firstly sent from SM controllers to the main controller to identify the SM with the highest temperature. Then, an appropriate power reduction $\Delta S^*$is calculated based on (2) and (3). Details for this process are given in the flowchart in Fig. 4.

The process starts by initializing the setpoint S_0^*. The main controller receives T_{ji} from the SMs and uses (8) to calculate reference T_j^*. Meanwhile, the maximum temperature $T_{ji,max}$ is found. In the next step, $T_{ji,\max}$ is compared with a predetermined threshold value $T_{j,MAX}^*$. Considering a thermal time constant, a time delay $T_{delay} = K_{\tau,thermal}T_{PWM}$ is considered, which is the time interval for calculating ΔS^*, where T_{PWM} is the switching period. T_{delay} was selected as 200 ms in this paper by considering the time constant of the thermal impedance in Table I. If $T_{ji,\max} > T_{j,MAX}^*$ after T_{delay}, $S_{n+1}^* = S_n^* - \Delta S^*$ is updated for the next iteration. ΔS^* is iteratively obtained using (2) and (3) until the condition $T_{ji,\max}^{cal} < T_{j,MAX}^*$ is met, where $T_{ji,\max}^{cal}$ is the theoretically calculated value of the maximum junction temperature which dictates whether S_n^* should be further decreased. If $T_{ji,\max}$ has been limited below $T_{j,MAX}^*$, S_n^* remains unchanged (i.e. $S_{n+1}^* = S_n^*$) and the algorithm proceeds to the next iteration. An allowable minimum power S_{MIN}^* could be also set according to practical requirements. If $S^* < S_{MIN}^*$, system operation should be shut down.

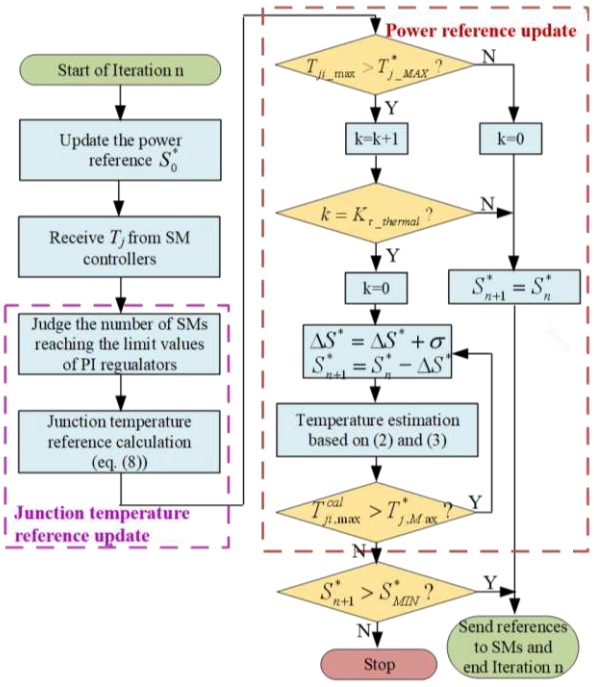


Fig. 4. Thermal management within the main controller.

IV. Small-signal Modeling and Thermal Controller Parameter Design

A. Small-signal modeling

1) Small-signal model of a single SM: The dynamic equations of the *dq* current loop are:

$$\dot{\hat{\mathbf{i}}}_{dqi} = \frac{1}{L}\left[K_{p,I}\left(\hat{\mathbf{i}}^*_{dq0} + \hat{\mathbf{i}}^*_{dqi,comp} - \hat{\mathbf{i}}_{dqi}\right) + K_{i,I}\hat{\mathbf{x}}_{I_{dqi}}\right] - \frac{R\hat{\mathbf{i}}_{dqi}}{L} \quad (9)$$

$$\dot{\hat{\mathbf{x}}}_{I_{dqi}} = \hat{\mathbf{i}}^*_{dq0} + \hat{\mathbf{i}}^*_{dqi,comp} - \hat{\mathbf{i}}_{dqi} \quad (10)$$

where $\mathbf{i}_{dqi} = [i_{di} \quad i_{qi}]$ is the *dq* current, and $\mathbf{i}^*_{dq0} = [i^*_{d0} \quad i^*_{q0}]$ and $\mathbf{i}^*_{dqi,comp} = [i^*_{di,comp} \quad i^*_{qi,comp}]$ are the references produced by the power and thermal controllers. $\mathbf{x}_{I_{dqi}} = [x_{I_{di}} \quad x_{I_{qi}}]$ is the output of the integral action of the current PI controller, $K_{p,I}$ and $K_{i,I}$ are the proportional and integral gains of the controller, and L and R are the transformer leakage inductance and ac circuit resistance. In this notation, '$\hat{x}$' stands for the perturbed value of variable x and an uppercase notation is used to denote RMS values of ac variables (or average values of dc variables).

The equations of the dc voltage PI controller are:

$$\hat{\imath}^*_{di,comp} = K_{p,u_{dc}}\hat{\dot{x}}_{V_{dci}} + K_{i,u_{dc}}\hat{x}_{V_{dci}} \quad (11)$$

$$\hat{\dot{x}}_{V_{dci}} = -\hat{v}_{dci} + \frac{\hat{v}_{dc}}{N} + \hat{v}^*_{dci,comp} \quad (12)$$

where $v^*_{dci,comp}$ is the dc voltage reference generated by the thermal controller, $K_{p,u_{dc}}$ and $K_{i,u_{dc}}$ are the proportional and integral gains of the controller and $x_{V_{dci}}$ is the output of the integral action. The dynamic equation of the dc voltage of the SM is obtained from the power relationship between the ac and dc sides of a converter as

$$\hat{\dot{v}}_{dci} = \frac{I_{dc}\hat{v}_{dci}}{C_{dci}V_{dci}} + \frac{\hat{\imath}_{dc}}{C_{dci}} - \frac{3V_{di}\hat{\imath}_{di}}{2C_{dci}V_{dci}} \quad (13)$$

where i_{dc} is the dc link current and C_{dci} is the dc capacitance. Assuming v_{dc} is fully regulated by the dc voltage control station, $\hat{v}_{dc}$ is considered zero for simplicity.

For modeling the dynamics of the thermal network, a four-layer thermal impedance with different time constants is normally considered ($\tau_{th,i}$). The time constants are shown in Table I. However, to facilitate the analysis, the first-order transfer function $\left(\frac{R_{th,JH}}{\tau_{th}s+1}\right)$ was used instead to represent its dynamics, where τ_{th} is an equivalent time constant defined as the time when the output of the system is approximately equal to 0.63 times the steady value following a step input. A time-domain simulation was conducted to illustrate temperature variations, utilizing both actual impedance and equivalent impedance. Fig. 5 presents the comparison, revealing a minor discrepancy. Therefore, the equivalent impedance is adequate for representing the dynamics of thermal behaviors.

By linearizing (2), the dynamic equation of the thermal network is then

$$\hat{\dot{T}}_{ji} = \frac{-\hat{T}_{ji} + \hat{\mathbf{W}}_i\mathbf{F}_{loss}}{\tau_{th}} \quad (14)$$

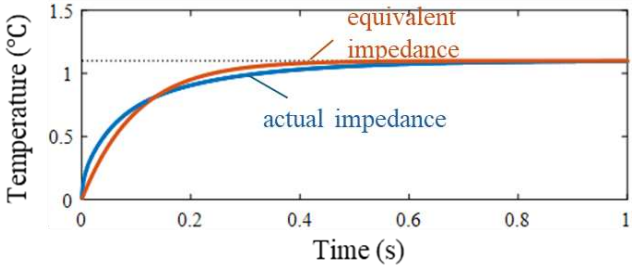


Fig. 5. Comparisons of dynamics of junction temperature using equivalent impedance and actual impedance.

where $\mathbf{F}_{loss} = [a_1 + 2a_2P_{0i} + a_3Q_{0i} \quad a_3P_{0i} + a_4 + 2a_5Q_{0i}]^T$ and $\mathbf{W}_i = [P_i \quad Q_i]$. It is noted that only the dynamics of the impedance of junction to heatsink are considered. The dynamics of the impedance of heatsink to the ambient air are not modeled due to their very large time constant (of around tens of seconds [31]). Hence, the temperature variation of the heatsink during an updating period of the thermal control loop is considered unchanged. Combining (9)−(14), the state-space representation of a single SM without controllers is:

$$\dot{\hat{\mathbf{x}}}_{SMi} = \mathbf{A}_{SMi}\hat{\mathbf{x}}_{SMi} + \mathbf{B}_{SMi}\hat{\mathbf{u}}_{SMi} \quad (15)$$

$$\hat{\mathbf{y}}_{SMi} = \mathbf{C}_{SMi}\hat{\mathbf{x}}_{SMi} \quad (16)$$

where $\mathbf{x}_{SMi} = \left[\mathbf{i}_{dqi} \quad \mathbf{x}_{I_{dqi}} \quad T_{ji} \quad v_{dc} \quad x_{V_{dci}}\right]^T$ is the state vector, $\mathbf{u}_{SMi} = [v^*_{dci,comp} \quad i^*_{qi,comp} \quad \mathbf{i}^*_{dq0}]^T$ is the input vector and $\mathbf{y}_{SMi} = [T_{ji} \quad \mathbf{W}_i]^T$ is the output vector. $\mathbf{A}_{SMi}$, $\mathbf{B}_{SMi}$ and $\mathbf{C}_{SMi}$ are provided in the Appendix. The transfer matrix representation of (15)-(16) is obtained as

$$\hat{\mathbf{Y}}_{SMi}(s) = [\mathbf{C}_{SMi}(s\mathbf{I} - \mathbf{A}_{SMi})^{-1}\mathbf{B}_{SMi}]\hat{\mathbf{U}}_{SMi}(s) = \begin{bmatrix} G_{1,th}(s) & G_{2,th}(s) & G_{3,th}(s) & G_{4,th}(s) \\ G_{1,P}(s) & G_{2,P}(s) & G_{3,P}(s) & 0 \\ G_{1,Q}(s) & G_{2,Q}(s) & 0 & G_{3,Q}(s) \end{bmatrix}\hat{\mathbf{U}}_{SMi}(s) \quad (17)$$

The outputs of the temperature and power PI controllers are given, respectively, by

$$\hat{v}^*_{dci,comp} = G_{PI,th,d}(s)\left(\hat{\delta}^*_i - \hat{\delta}_i\right) \quad (18)$$

$$\hat{\imath}^*_{qi,comp} = G_{PI,th,q}(s)\left(\hat{\delta}^*_i - \hat{\delta}_i\right) \quad (19)$$

$$\hat{\boldsymbol{\imath}}^*_{dq0} = \frac{1}{N}G_{PI,W}(s)\left(\hat{\mathbf{W}}^* - \hat{\mathbf{W}}\right) \quad (20)$$

where $G_{PI,th,d}(s) = \frac{K_{P,th}s + K_{i,th}}{s}$, $G_{PI,th,q}(s) = \frac{0.2V_{dc}}{I_q}G_{PI,th,d}(s)$ and $G_{PI,W}(s) = \frac{K_{P,W}s + K_{i,W}}{K_{i,W}s}$ are the transfer functions of the thermal and power PI controllers (see Fig. 2). In (20), $\mathbf{W}^*$ is the power reference and $\mathbf{W}$ is the output power ($\mathbf{W} = \sum_{i=1}^{N}\mathbf{W}_i$), whereas in (18) and (19), δ_i is the difference between T_{ji} and the mean value (i.e., $\delta_i = T_{ji} - \frac{\sum_{i=1}^{N}T_{ji}}{N}$), and δ^*_i is the reference of δ_i. To achieve equal thermal sharing, δ^*_i is set to zero.

2) Small-signal model of the C3L-NPC converters: Assuming the parameters for each SM are identical, the temperature equations for an *N* SM-cascaded system are:

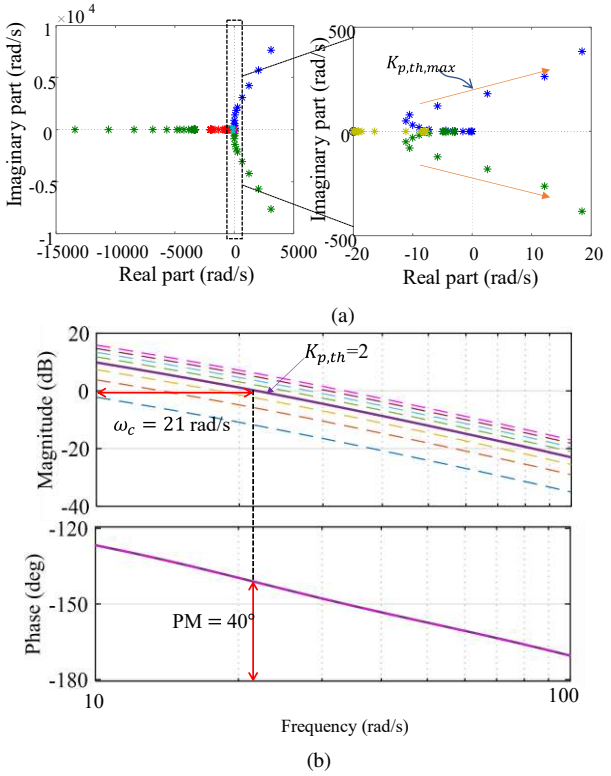


Fig. 6. Frequency-domain analysis. (a) Closed-loop poles' trajectories as $K_{p,th}$ increases. (b) Bode plot of $G_{\delta,th}(s)$ for values of $K_{P,th}$ ranging from 0.5 to 4.

$$\begin{cases} \hat{T}_{j1} = G_{\delta,th}(s)\left(\hat{\delta}_1^* - \hat{\delta}_1\right) + \mathbf{G}_{W,th}(s)\left(\widehat{\mathbf{W}}^* - \widehat{\mathbf{W}}\right)^T \\ \hat{T}_{j2} = G_{\delta,th}(s)\left(\hat{\delta}_2^* - \hat{\delta}_2\right) + \mathbf{G}_{W,th}(s)\left(\widehat{\mathbf{W}}^* - \widehat{\mathbf{W}}\right)^T \\ \vdots \\ \hat{T}_{jN} = G_{\delta,th}(s)\left(\hat{\delta}_N^* - \hat{\delta}_N\right) + \mathbf{G}_{W,th}(s)\left(\widehat{\mathbf{W}}^* - \widehat{\mathbf{W}}\right)^T \end{cases} \quad (21)$$

where $G_{\delta,th}(s) = \left(G_{1,th}(s) + \frac{0.2V_{dc}}{I_q} G_{2,th}(s)\right) G_{PI,th,d}(s)$ and $\mathbf{G}_{W,th}(s) = \left[\frac{1}{N} G_{PI,W}(s) G_{3,th}(s) \quad \frac{1}{N} G_{PI,W}(s) G_{4,th}(s)\right]$. From (21), the following expressions are obtained:

$$\begin{cases} \hat{T}_{ji} - \hat{T}_{j1} = G_{\delta,th}(s)\left[\left(\hat{\delta}_i^* - \hat{\delta}_i\right) - \left(\hat{\delta}_1^* - \hat{\delta}_1\right)\right] \\ \hat{T}_{ji} - \hat{T}_{j2} = G_{\delta,th}(s)\left[\left(\hat{\delta}_i^* - \hat{\delta}_i\right) - \left(\hat{\delta}_2^* - \hat{\delta}_2\right)\right] \\ \vdots \\ \hat{T}_{ji} - \hat{T}_{jN} = G_{\delta,th}(s)\left[\left(\hat{\delta}_i^* - \hat{\delta}_i\right) - \left(\hat{\delta}_N^* - \hat{\delta}_N\right)\right] \end{cases} \quad (22)$$

Letting $\delta_N^* = -\sum_{i=1}^{N-1} \delta_i^*$ and adding all equations in (22) yields

$$\hat{\delta}_i = G_{\delta,th}(s)\left[\hat{\delta}_i^* - \hat{\delta}_i\right] \quad (23)$$

Solving for $\hat{\delta}_i$ results in

$$\hat{\delta}_i = \frac{G_{\delta,th}(s)}{1+G_{\delta,th}(s)} \hat{\delta}_i^* \quad (24)$$

Equation (24) shows that when the constraint $\delta_N^* = -\sum_{i=1}^{N-1} \delta_i^*$ is met, the difference between the temperature of each SM and the mean temperature can be independently controlled. In fact, the control system has *N* degrees of freedom: one for the control of total power and the remaining $N-1$ for temperature control between the *N* modules. The thermal

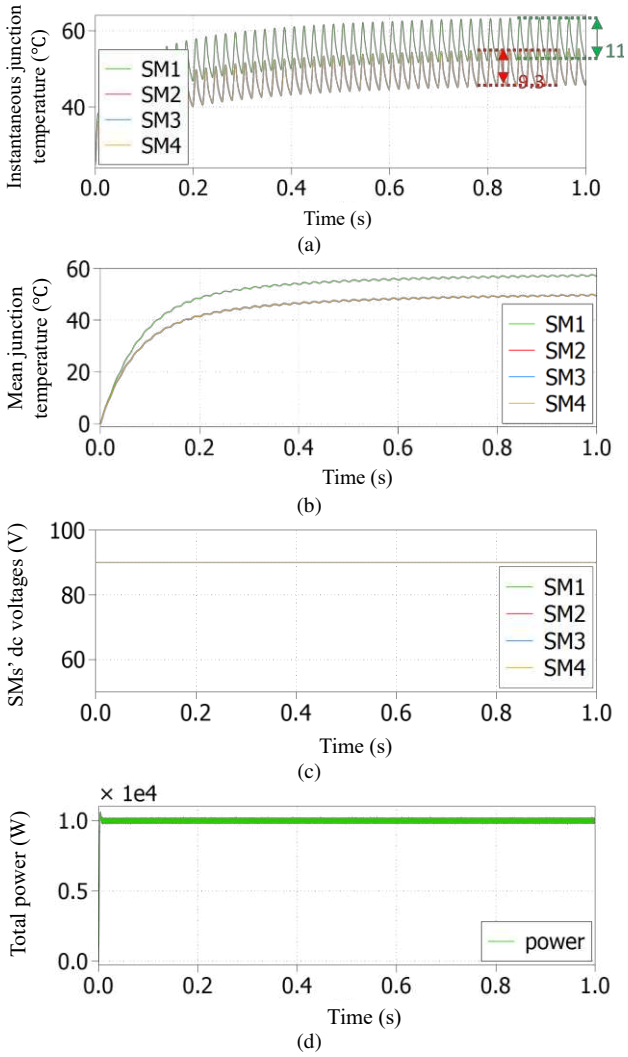


Fig. 7. Results for C3L-NPC converters without the implementation of active thermal control. (a) Instantaneous junction temperature. (b) Mean temperature after low-pass filtering. (c) SMs' dc voltages. (d) Total power.

balancing control (i.e. $\hat{\delta}_i^* = 0$) is a special case as $\hat{\delta}_i^*$ can be selected arbitrarily to regulate the temperature difference between any neighboring SMs. As the thermal control loops are decoupled from each other and from the power controller, $G_{PI,W}(s)$, $G_{PI,th,d}(s)$ and $G_{PI,th,q}(s)$ can be tuned separately. Verification can therefore be conducted with a smaller number of SMs without compromising the generality of the conclusions.

It is noted that even though communication between the main controller and the SMs' controllers may introduce a slight time delay, this delay typically amounts to approximately 3.05 ms with Modbus-based communication. This duration is about 10 times shorter than the time constant of the outer control loops. Therefore, the communication delay is disregarded in the derivation of the mathematical models.

B. Controller parameter tuning

The procedure for tuning $G_{PI,W}(s)$ was conducted as in [36], with the reader referred to that reference for further details. Only the tuning of $G_{PI,th}(s)$ is discussed in this paper to prevent duplication of information. The zero of $G_{PI,th,d}(s)$ was selected

to cancel out the pole of the transfer function of the equivalent thermal impedance $\frac{R_{th,JH}}{\tau_{th}s+1}$, which has the largest time constant in the control system. Thus, $K_{i,th}$ is selected as $K_{i,th} = K_{P,th}/\tau_{th}$. $G_{\delta,th}(s)$ is the open loop transfer function of the thermal sharing loop defined after (21). The root locus of its closed-loop transfer function and the open loop frequency response plot (Bode diagram) of $G_{\delta,th}(s)$ for different values of $K_{P,th}$ are shown in Fig. 6.

The control parameters for the dc voltage, current and power controllers in Fig. 2 are summarized in Table II, where $K_{p,x}$ and $K_{i,x}$ represent their proportional and integral gains, respectively. The relevant circuit parameters are listed in Table III. Four dc series-connected 3L-NPC SMs are used to achieve a dc voltage of ±180 V. These SMs are connected to an isolation transformer with a Yd11 vector group connection, where the high-voltage winding is star-connected, and the low-voltage winding is delta-connected with a 30-degree phase lead.

According to the trajectories of the eigenvalues in Fig. 6(a), it is found that all the closed-loop poles locate in the left-half s plane when $K_{p,th}$ is less than the threshold gain value $K_{p,th,max}$, which indicates that the system is stable. If $K_{p,th}$ is larger, the system may become unstable since a pair of complex conjugate poles move to the right-half s plane. Both the divergence rate and the oscillation frequency will increase as the $K_{p,th}$ increases. To select a suitable value for this gain, the Bode diagram of $G_{\delta,th}(s)$ is analyzed in Fig. 6(b). The bandwidth of the thermal control loop increases as the value of $K_{P,th}$ increases, whereas the phase margin is reduced. To obtain a suitable dynamic performance, $K_{P,th}$= 2 is chosen, for which the cut-off frequency is 21 rad/s and the phase margin is 40º.

TABLE II. CONTROLLER PARAMETER.

current controller		dc voltage controller		power controller	
$K_{p,I}$	10	$K_{p,u_{dc}}$	6.8	$K_{p,W}$	0.2
$K_{i,I}$	200	$K_{i,u_{dc}}$	1000	$K_{i,W}$	20

TABLE III. MVDC CONVERTER PARAMETERS.

Power rating	4 kW	DC link voltage	± 180 V
AC voltage (RMS of v_s)	415 V	Transformer rating	10 kVA, Y-415 V/Δ-41.5 V
Filter inductance (per SM)	0.5 mH	DC capacitance (per SM)	5400 μF
Power factor	0.9	Switching frequency	10000 Hz

V. SIMULATION AND EXPERIMENTAL VALIDATION

A. Simulation results

The simulation is conducted using PLECS, with four SMs cascaded together. The $R_{th,JH}$ of SM1 is chosen to be larger than that of the other three SMs to create a mismatch in component parameters. In Fig. 7, the $R_{th,JH}$ of SM1 is doubled, and the system operates without thermal sharing control. As shown in Fig. 7(a) and (b), the dc link voltage is equally shared among the SMs. However, due to the mismatched thermal resistance, the junction temperature swing of SM1 is 11 °C,

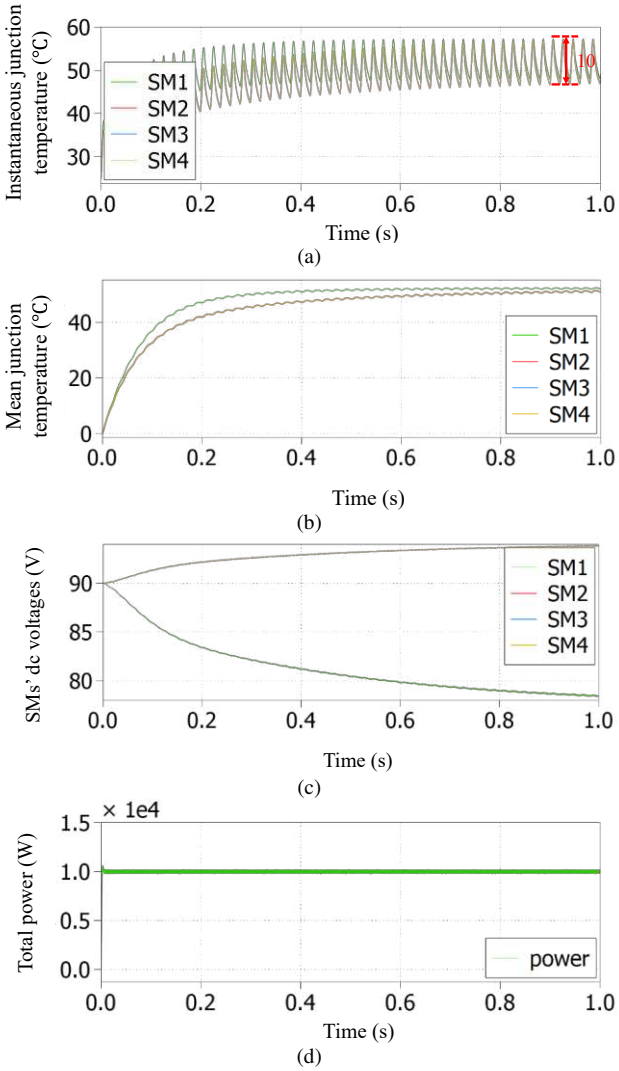


Fig. 8. Results for C3L-NPC converters with the implementation of active thermal control. (a) Instantaneous junction temperature. (b) Mean temperature after low-pass filtering. (c) SMs' dc voltages. (d) Total power.

which is 1.7 °C higher than those of the other SMs. Additionally, the mean temperature of SM1 is around 10 °C higher than that of the others.

Fig. 8 illustrates the case when thermal sharing control is implemented. As shown in Fig. 8(a) and (b), the junction temperatures of the four SMs are evenly distributed. Through the automatic regulation of the thermal control loop, the dc voltage of SM1 decreases to around 80 V, while the others increase to 95 V (see Fig. 8(c)). Since power control is decoupled from thermal sharing control, the total power remains unaffected (see Fig. 8(d)). As both the swing and mean junction temperatures of the overheated SM are lowered, the accumulated damage is reduced according to the lifetime model [37]. Consequently, the overall reliability of the system is enhanced.

Fig. 9 and Fig. 10 illustrate the scenario where the $R_{th,JH}$ of SM1 is increased to be four times larger than that of the other SMs, simulating a more severe overheating condition. In Fig. 9, the temperature reference is set to the average junction temperature of the four SMs. After 0.3 seconds, the thermal control capability reaches its limit, and then the thermal PI

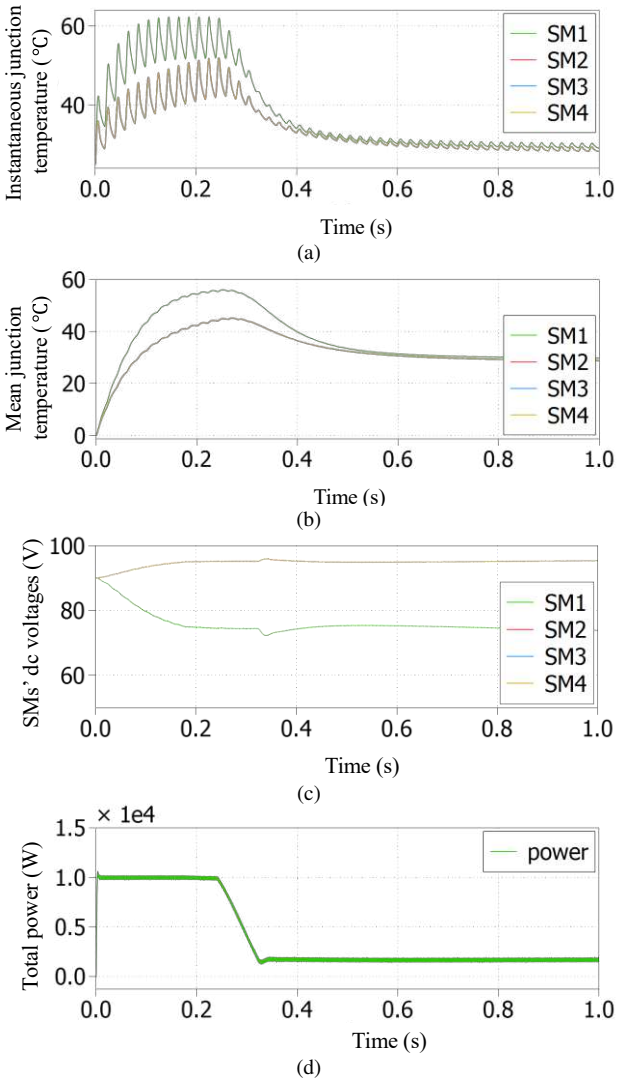


Fig. 9. Results for C3L-NPC converters when maximal thermal control capability is reached without applying thermal management in Fig. 4. (a) Instantaneous junction temperature. (b) Mean temperature after low-pass filtering. (c) SMs' dc voltages. (d) Total power.

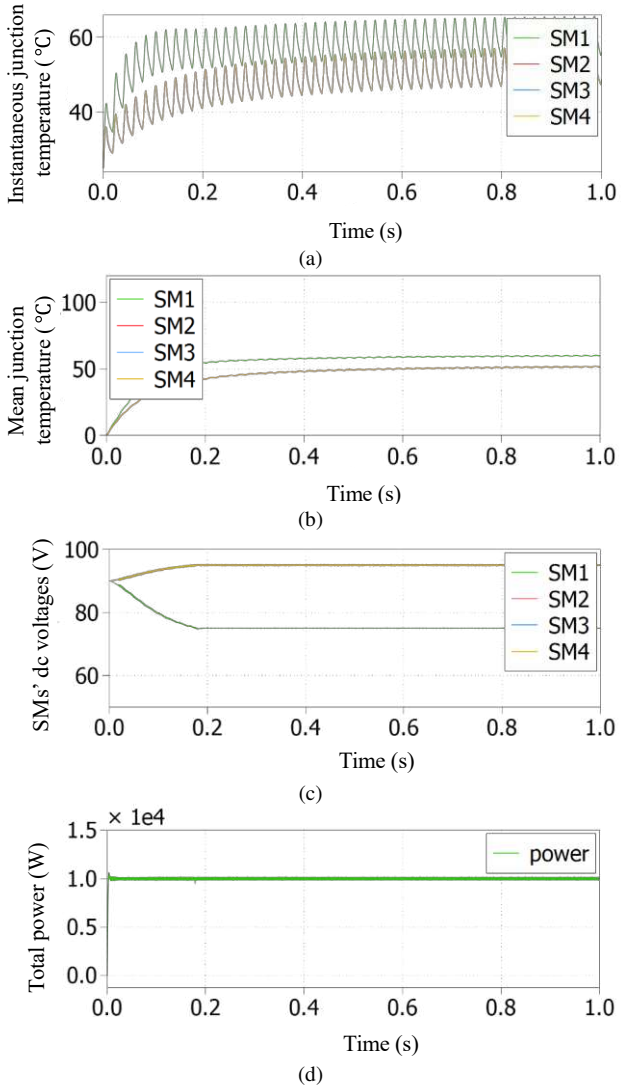


Fig. 10. Results for C3L-NPC converters when maximal thermal control capability is reached with applying thermal management in Fig. 4. (a) Instantaneous junction temperature. (b) Mean temperature after low-pass filtering. (c) SMs' dc voltages. (d) Total power.

regulator of SM1 becomes saturated. As a result, the thermal sharing control is no longer decoupled from the power control. As shown in Fig. 9(d), the power control is affected, leading to a significant decrease in power after 0.3 seconds.

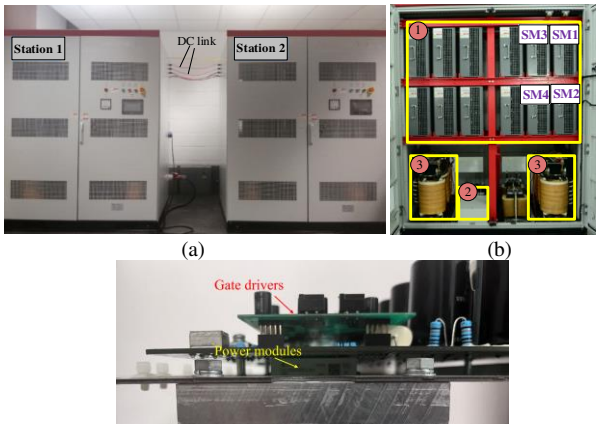
In Fig. 10, once the thermal control limitation of SM1 is reached, the temperature reference shifts to the mean value of the junction temperature of the remaining three SMs (SM2, SM3, and SM4). Consequently, the decoupling between power control and thermal sharing control remains intact, and the output power is sustained, as depicted in Fig. 10(d). Since the maximum thermal control capability is reached, the temperature of SM1 does not completely align with that of the others. There remains a temperature difference of approximately 8°C between SM1 and the other SMs, as shown in Fig. 10(a) and (b).

B. Experimental results

The effectiveness of the thermal balancing approach was validated through a laboratory-scale MVDC testbed down-scaled from the ANGLE-DC project [32]. The experimental facilities are shown in Fig. 11(a). Fig. 11(b) shows the detailed internal structure of each converter station, including the twelve 3L-NPC cascaded SMs and the main controller. Station 1 is in power control mode while Station 2 operates in dc link voltage control mode. The communication between the main controller and the SMs' controllers is based on an RS-485 cable and the Modbus protocol. Two power amplifiers (PA-3*3000-AB/260/2G) were connected to the MVDC testbed to emulate the ac grids from the distribution networks.

As the power rating of the power amplifiers is limited to 9 kVA, four cascaded SMs were used for the experimental validation only instead of the twelve available. However, since the thermal control scheme does not depend on the number of SMs, this does not affect the verification of the method.

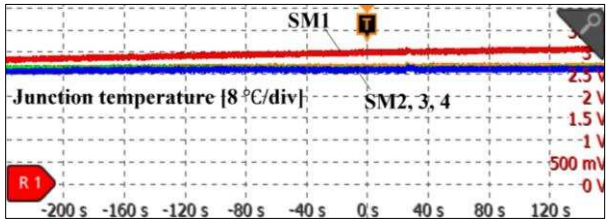
The circuit and controller parameters are the same as in Section IV-B. The negative-temperature-coefficient thermistor inside the power module package was used to measure the heatsink temperatures of the SMs. Each SM is installed with a cooling fan to dissipate the heat of the power devices. The estimated junction temperature is obtained using a digital-to-



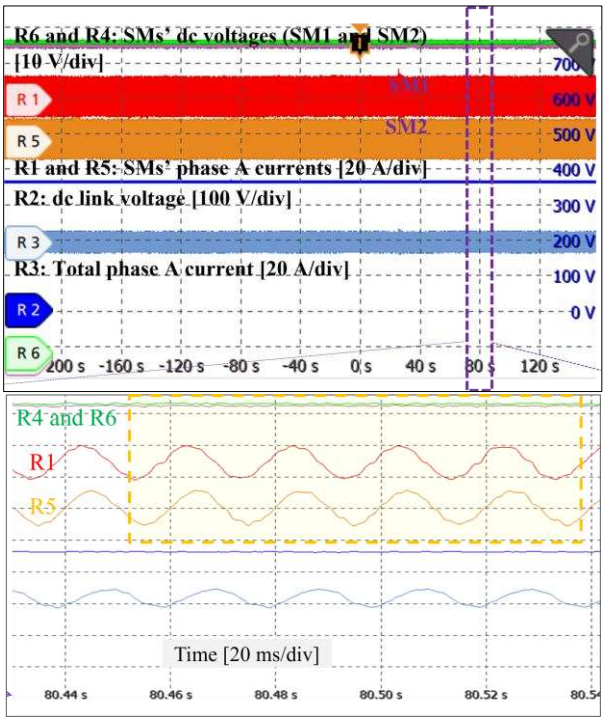
(a) (b)

(c)

Fig. 11. Lab-scaled MVDC platform: (a) back-to-back converter station. (b) internal structure of each converter station including (1) twelve 3L-NPC SMs, (2) high-level central controller and (3) isolation transformers. (c) Power module and gate drivers.



(a)

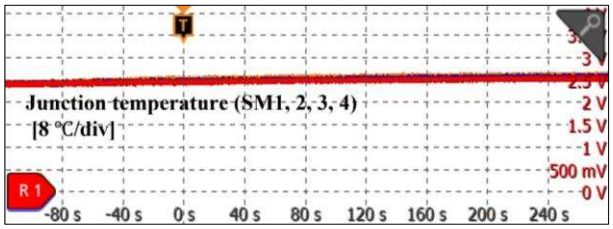


(b)

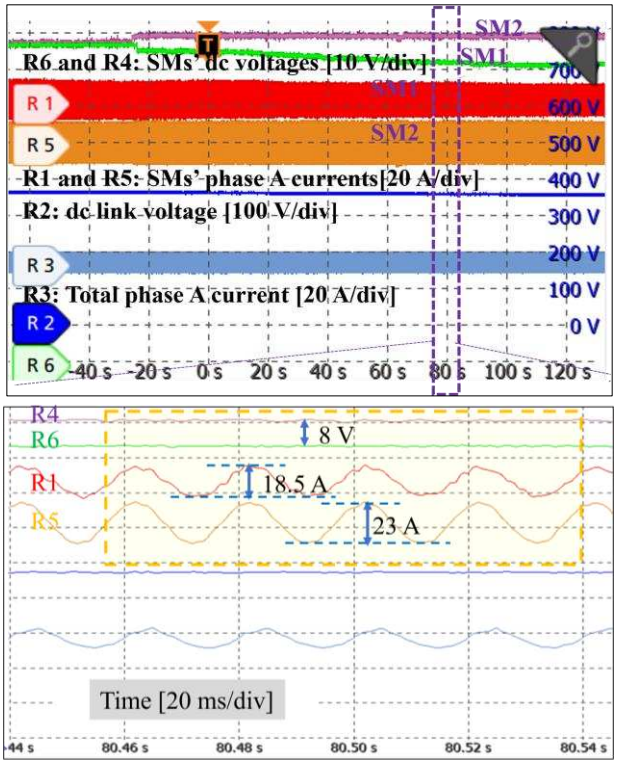
Fig. 12. Junction temperatures of SMs without thermal sharing control (the fan of SM1 is at 60% rated speed and the others at 100% rated speed): (a) junction temperatures of SMs; (b) SM and total ac current and dc voltage (the bottom plot shows a zoomed-in view).

analog (DAC) device, which consists of a PWM chopper and a low-pass filter. The DAC device has a sensitivity of 63 mV/K. In practice, the air-cooling system may encounter failures due to issues caused by electronic parts, such as the power supply and power drives, and mechanical parts, such as the bearings, lubricant, shaft, and fan blades [38]. These may lead to a reduction in air flow rate or even complete failure of the cooling system. In the experimental tests, the fan speed was regulated from zero to the rated speed (3000 rpm) to mimic cooling conditions.

Fig. 12 shows the typical voltage balancing control while the fan of SM1 is operated at 60% rated speed to mimic partial failure conditions. The remaining three SM fans operate at 100% rated speed. It is seen that there is a temperature difference of around 8℃ between SM1 and the remaining SMs (i.e. SM2, 3 and 4) in Fig. 12(a). The dc voltages of the SMs and currents of phase A of SM1 and SM2 and the total dc voltage and current of the four SMs are given in Fig. 12(b). As seen from traces R4, R6, R1 and R5 within the yellow dashed rectangle, the SMs' currents and dc voltages are equally shared.



(a)



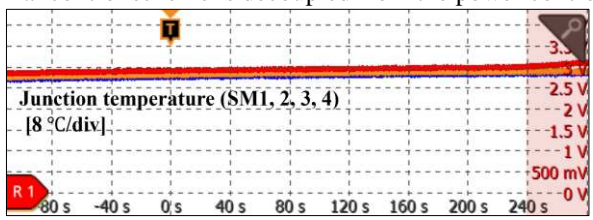
(b)

Fig. 13. Junction temperatures of SMs with thermal sharing control (same thermal conditions as in Fig. 12): (a) junction temperatures of SMs; (b) SM and total ac current and dc voltage (the bottom plot shows a zoomed-in view).

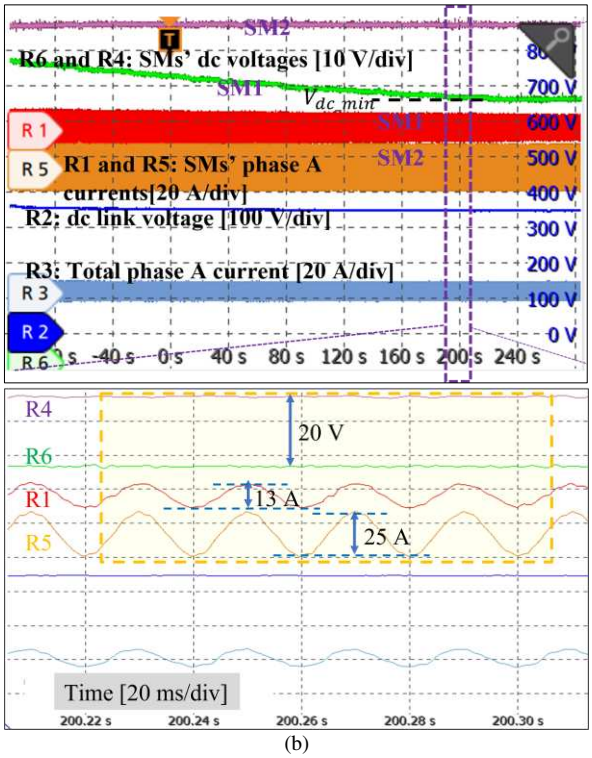
Fig. 13 shows the waveforms when the thermal sharing control is implemented for the same cooling system failure conditions as in Fig. 12. The temperature difference between SM1 and the other SMs is effectively reduced (see Fig. 13(a)). Balancing the junction temperature is achieved by the closed-loop regulation afforded by the thermal controller shown in Fig.

2. The dc voltage and current of SM1 are decreased to eliminate the overheating, and conversely, the dc voltage and ac current of SM2 are increased. As seen from the zoomed-in view in Fig. 13(b), the dc voltage difference between traces R6 (SM1) and R4 (SM2) is around 8 V and the difference of peak-to-peak ac current between traces R1 (SM1) and R5 (SM2) is around 5.5 A (obtained by calculating the value of R5 minus R1).

Fig. 14 shows that the dc voltage further decreases to the minimum limit value when the fan speed is zero to mimic the full cooling system failures of SM1. At a time ~220 s, the dc voltage of SM1 has reached its minimum value set as 75 V (see Fig. 14(b)). With the thermal balancing control, the differences in dc voltages and ac currents of SMs at this severe condition are increased to 20 V and 12 A (obtained by subtracting the values of R5 minus R1), which are larger than those in Fig. 14(b). Meanwhile, the temperature reference changes automatically to the average temperature of SMs 2, 3, and 4 according to (8). Since the thermal control capability has been reached, a slight temperature imbalance appears after 240 s (see the pink rectangle in Fig. 14(a)). It is seen that the total output power in Fig. 13(b) and Fig. 14(b) is not influenced by implementing the thermal controller, which verifies that the thermal control scheme is decoupled from the power control.



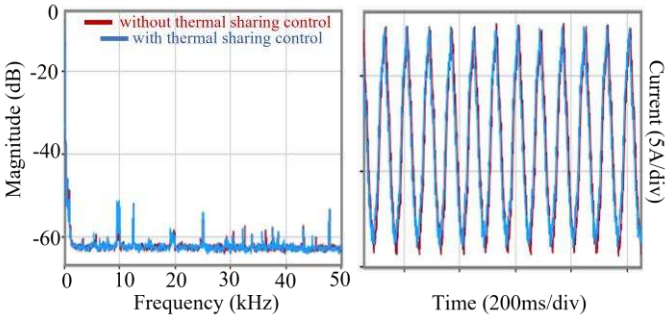
(a)



(b)

Fig. 14. Junction temperatures of SMs with thermal sharing control (the fan of SM1 is at zero speed and the others at 100% rated speed): (a) junction temperatures of SMs; (b) SM and total ac current and dc voltage (the bottom plot shows a zoomed-in view).

As the SMs work at different operating points, there is a risk of deteriorating the harmonic performance of the total current [31]. To investigate this point, the fast Fourier transform (FFT) for the system under a conventional power balancing control was compared with that under the presented thermal sharing control. The spectra of the currents of phase-A under both control strategies are shown in Fig. 15(a). Fig. 15(b) shows the zoomed-in total phase-A currents displayed in Fig. 12(b) and Fig. 13(b), respectively. The harmonics for both control methods within the range of 0 to 50 kHz present similar characteristics. Hence, the presented control strategy has little impact on the current distortion.



(a) (b)

Fig. 15. FFT analysis of ac harmonics with and without thermal sharing control.

VI. Conclusion

For C3L-NPC converters, thermal stress may be distributed unequally among their SMs, thus influencing system reliability while increasing maintenance costs. The active thermal sharing control method presented in this paper is able to balance the thermal stress by concurrently regulating active and reactive power. Based on a temperature PI controller in each SM, the junction temperature difference between SMs can be effectively balanced.

A unique issue exhibited by the C3L-NPC converter topology is the limitation of the thermal regulation which is constrained by the minimum dc voltage of the SM. In the event of a severe temperature imbalance, the thermal control limit can be reached. In this case, the temperature reference is modified by the main controller to maintain the system operation. To facilitate the controller design, a small-signal system model was developed. It was found that the power and thermal control loops are decoupled so that the thermal and power controller can be independently designed.

The presented thermal sharing control scheme was experimentally validated through a laboratory-scale MVDC testbed, which was developed from the technical specifications of the ANGLE-DC project. Converters consisting of four cascaded SMs at 360 Vdc/ 2 kVA were tested at different temperature conditions to mimic partial cooling system failures of SMs, which were achieved by adjusting the cooling fan speed. By implementing the presented thermal control, the junction temperature has been effectively balanced under cooling system failures.

Appendix

Matrices of the small-signal model of equation (17) are:

$$\mathbf{A}_{SMi}=\begin{bmatrix} k_1 & 0 & k_2 & 0 & 0 & k_3 & k_4 \\ 0 & k_5 & 0 & k_6 & 0 & 0 & 0 \\ k_7 & 0 & 0 & 0 & 0 & k_8 & k_9 \\ 0 & k_{10} & 0 & 0 & 0 & 0 & 0 \\ k_{11} & k_{12} & 0 & 0 & k_{13} & 0 & 0 \\ k_{14} & 0 & 0 & 0 & 0 & k_{15} & 0 \\ 0 & 0 & 0 & 0 & 0 & k_{16} & 0 \end{bmatrix}$$

$$\mathbf{B}_{SMi}=\begin{bmatrix} \frac{K_{p,I}K_{p,u_{dc}}}{L} & 0 & \frac{K_{p,I}}{L} & 0 \\ 0 & \frac{K_{p,I}}{L} & 0 & \frac{K_{p,I}}{L} \\ K_{p,u_{dc}} & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}$$

$$\mathbf{C}_{SMi}=\begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ \frac{3V_{di}}{2} & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & \frac{3V_{di}}{2} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

where $k_1=k_5=-\frac{K_{p,I}+R}{L}$, $k_2=k_6=\frac{K_{p,I}K_{i,I}}{L}$, $k_3=\frac{-K_{p,I}K_{p,u_{dc}}}{L}$, $k_4=\frac{K_{p,I}K_{i,u_{dc}}}{L}$, $k_7=k_{10}=-1$, $k_8=-K_{p,u_{dc}}$, $k_9=-K_{i,u_{dc}}$, $k_{11}=\frac{3V_{di}(a_1+2a_2P_{0i}+a_3Q_{0i})}{2\tau_{th}}$, $k_{12}=\frac{3V_{di}(a_3P_{0i}+a_4+2a_5Q_{0i})}{2\tau_{th}}$, $k_{13}=\frac{-1}{\tau_{th}}$, $k_{14}=-\frac{3V_{di}}{2C_{dci}V_{dci}}$, $k_{15}=\frac{I_{dc}}{C_{dci}V_{dci}}$, $k_{16}=-1$.

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