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# Large-area uniform III-V membranes grown on silicon-on-insulator by lateral tunnel epitaxy

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***Abstract*— Lateral tunnel epitaxy of InP and InAs membranes on silicon-on-insulator (SOI) substrates is demonstrated. The near dislocation-free III-V membranes exhibit smooth growth fronts and are precisely positioned atop silicon (Si) waveguides or the Si device layer.**

***Keywords—Silicon photonics, III-V membrane integrated photonics, Epitaxy***

## I. INTRODUCTION

Selective heteroepitaxy using aspect ratio trapping has been developed to realize monolithic integration of III-V lasers on 300 mm silicon (Si) substrates.[1] The confined growth along with the defect necking mechanism minimizes the buffer layer thickness, allowing for close proximity between III-V lasers and Si. However, arising from the growth in vertical direction, there are limits in the achievable volume of III-V materials for electrically injected lasers and challenges in device fabrication.[2, 3] Recently, a novel photonic integration technology, based on an InP membrane-on-insulator platform using bonding techniques, has emerged.[4] Benefited from the strong optical confinement and a lateral current injection configuration, lasers with direct modulation rates >100 GHz and power consumption <1 pJ/bit have been demonstrated,[5] offering a competitive advantage over off-chip electrical interconnections. Compared to the bonding techniques, direct epitaxy removes the need of costly III-V native substrates and offers greater scalability to large silicon substrates. Here, we present a lateral tunnel epitaxy platform (Figure 1a) for III-V membrane on SOI photonic integration. [6] Large-area, near dislocation-free InP and InAs membranes can be directly placed atop the Si waveguides. Incorporating InGaAs multi-quantum wells (MQWs) within the InP membranes results in photoluminescence (PL) detection at the telecom wavelength of 1.5 µm. This material platform offers new opportunities for seamless integration of various active and passive components as well as novel device designs for lasers and modulators.

## II. RESULTS AND DISCUSSION

The scanning electron microscope (SEM) image displayed in Figure 1b illustrates the fabricated SOI pattern before III-V growth. Compared to the mainstream Si waveguide on SOI used in current Si-photonics platform, we mainly implemented two modifications for our lateral tunnel epitaxy: 1, We created the Si V-groove in the Si device layer using anisotropic TMAH wet etch, a technique that has been well-established and documented; 2, We fabricated a lateral tunnel between the Si device layer and the top silicon nitride (SiN) by using an amorphous silicon sacrificial layer. This growth pattern was fabricated on 8-inch SOI substrates, yielding uniform tunnels with lengths ranging from tens to several hundred micrometers.

Lateral tunnel epitaxy was performed using selective area metal-organic chemical vapor deposition (MOCVD). The growth process of the InP membranes consists of two stages: initially, InP grows from the Si V-grooves surface, serving as a seeding layer with uniform morphology; subsequently, the InP evolves laterally into large-area membranes guided by the tunnel. The cross-sectional SEM image in Figure 2a shows the InP growing inside the tunnel, evolving from the Si V-groove and sandwiched between the Si device layer and the top SiN. The optical microscope images in Figure 2d and 2e reveal that the InP membranes exhibit uniform, smooth growth fronts. Electron channelling contrast imaging (ECCI) characterization demonstrates the InP membranes are nearly free of dislocations (not shown here). Growth of uniform InP and InAs membranes

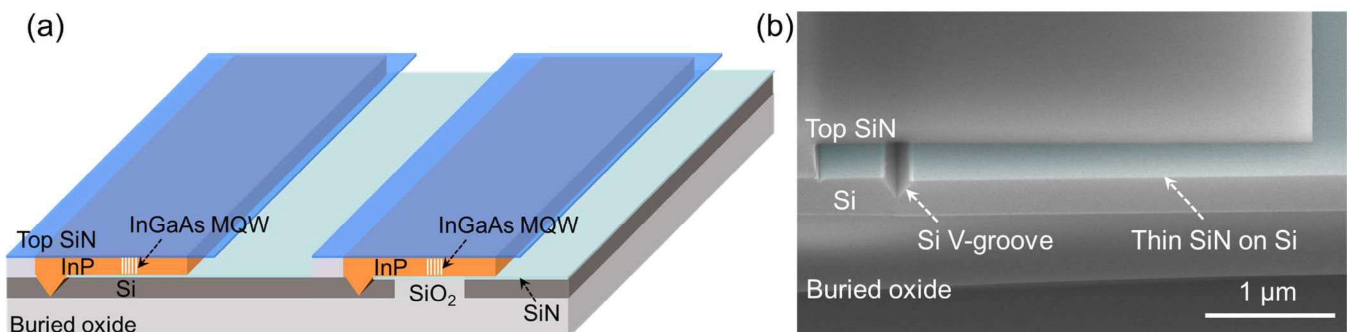


Figure 1. (a) Schematic showing the lateral tunnel epitaxy of III-V membranes on SOI substrates. (b) Tilted SEM photo showing the fabricated SOI pattern before III-V growth. The false-color SEM shows the thin SiN layer on Si.

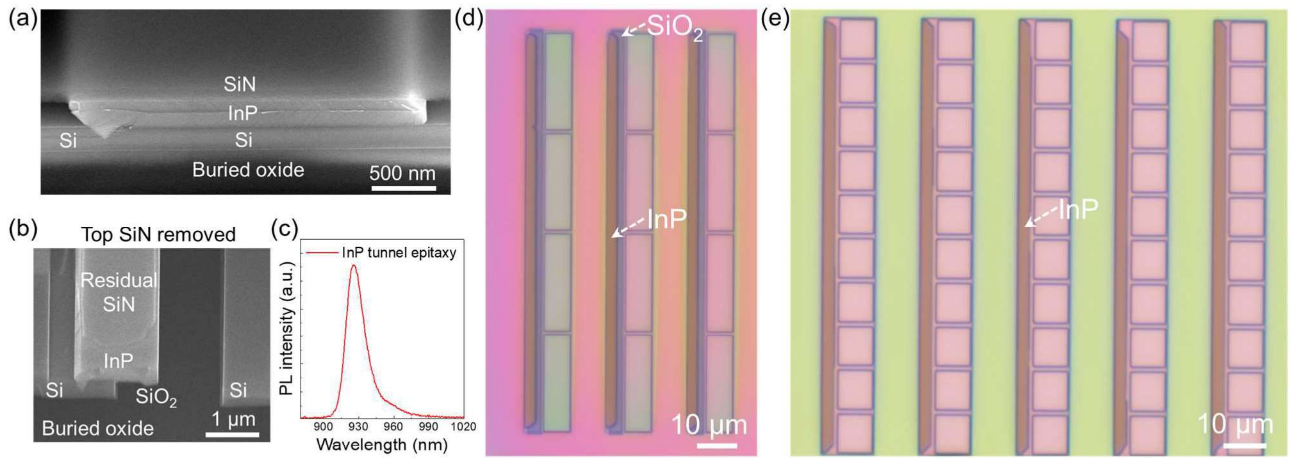


Figure 2. (a, b) Tilted SEM image depicting InP laterally grown on SOI. (c) PL of InP by lateral tunnel epitaxy. (d, e) Optical microscope images showing the smooth growth front of InP membranes with 100 µm length, placed atop $SiO_2$ and Si, respectively.

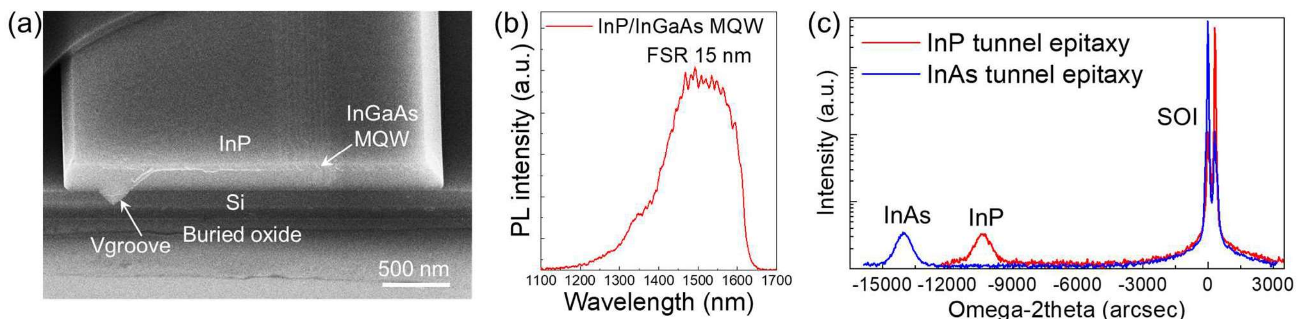


Figure 3. (a) SEM showing the InGaAs MQW insertion inside the InP membranes. (b) PL of the InP/InGaAs MQW by lateral tunnel epitaxy. (c) XRD ω-2θ scan of the InP and InAs lateral tunnel epitaxy.

in cavities with lengths of several hundred micrometers and widths up to 5 µm has been achieved. Notably, the III-V membranes can be positioned on top of the Si device layer (Figure 2a and 2e) or placed on $SiO_2$ or Si waveguides (Figure 2b and 2d), depending on the pattern design. This flexibility offers opportunities for the co-design and co-integration of various active and passive photonic devices.

After optimizing the large-area, uniform InP and InAs membranes, we inserted InGaAs MQW within the InP membranes (Figure 3a). Efficient photoluminescence emission was detected at the telecom wavelength of 1.5 µm (Figure 3b). The fine peaks observed in the PL curve are attributed to in-plane Fabry-Pérot (FP) resonances within the InP membranes. Despite the thin membranes selectively grown on SOI, X-ray diffraction (XRD) ω-2θ scan clearly detected the InAs and InP peaks (Figure 3c), indicating the excellent crystal quality of the epitaxial membranes.

## III. Conclusions

In summary, we have successfully grown large-area, uniform InP and InAs membranes on SOI substrates, showing excellent crystalline and optical quality. The III-V membranes are positioned directly atop Si waveguides, resembling III-V bonded onto SOI substrates. This approach offers a new route for integrating efficient lasers and modulators onto current silicon photonics platforms.

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