3-MHz High-Voltage Pulse Generator With Novel Multilevel LC Resonant Network for Adjustable Pulse Width

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***Abstract*—Voltage pulses with high repetition rates and short rise times exhibit promising prospects in applications of electroporation induced by nanosecond pulsed electric fields, owing to their unique intracellular effects. Generators using diode opening switch (DOS) can generate ultrashort nanosecond pulses with high voltage gain. However, the inherent semi-controlled nature of diodes presents challenges to the adjustability of pulse width in DOS generators. Moreover, the maximum achievable repetition frequency is theoretically limited by the resonant period. In this article, a novel modulator comprising multi-stage linear resonant loops is proposed. This topology enables the adjustment of pulse duration in diode-based LR discharging circuits. Furthermore, the developed approach of multiple modules frequency superposition not only surpasses the theoretical upper limit of repetition rate, but also exhibits improved energy conversion efficiency when compared to traditional DOS circuits. The experimental results indicate that the prototype outputs pulses with amplitude of 2.8 kV and duration ranging from 6.5 ns to 20.3 ns, while achieving a 55.6% improvement in energy transfer efficiency compared to conventional structures.**

***Index Terms*—Nanosecond pulse, semiconductor diode switches, pulse width modulation, modular multilevel frequency superstition.**

I. Introduction

PULSED power technology has found widespread application in various industrial fields, including material modification, biomedicine, and environmental protection [1, 2]. Among them, the utilization of nanosecond pulsed electric fields stands out, drawing significant interest due to its unique advantages in targeting more specific needs. Specifically, shorter rise times in nanosecond pulses enable plasma jets to produce more high-energy electrons, enhancing activation reactions [3, 4]. In our target field, tumor ablation through electroporation, shifting the pulse duration from microseconds to nanoseconds targets organelle membranes instead of cells, a phenomenon referred to as the 'window effect.' The intracellular effects are regulated through the manipulation of pulse width at the nanosecond scale, a process that facilitates apoptosis and triggers immune responses [5]. Due to the brief duration of nanosecond pulses, achieving the energy threshold necessitates an increased repetition frequency of pulse delivery [6, 7]. Besides, high energy conversion efficiency is essential for maintaining the reliability and compactness of pulse generators operating at such elevated frequencies. To meet these application requirements, our objective is to develop an adjustable, high-repetition nanosecond pulse generator with high energy conversion efficiency.

Conventional generators employing gas switches are limited in their ability to output voltage pulses at lower repetition frequencies [8]. In recent years, the advent of semiconductor technology has facilitated the development of solid-state pulse generators, which can operate at relatively high repetition frequencies, in the kHz range[9]. However, due to solid switch performance limitations, pulse rise times are typically greater than several tens of nanoseconds [10, 11]. Achieving shorter rise times often requires specialized circuit topologies for further energy compression and transformation [12]. The Blumlein line can generate pulses with durations of 10 nanoseconds, provided the load impedance is matched. However, due to the fundamentally low output/input voltage gain of traditional Blumlein lines resulting from their voltage division design, these systems struggle to generate high-amplitude pulses at low input voltages [13].

To investigate the biological effects induced by ultrashort pulses, researchers have employed diodes as opening switches to generate nanosecond pulses. Tang et al. developed a DOS-based high-voltage nanosecond pulse generator for electroporation applications, achieving pulses with an amplitude of up to 7.5 kV and a duration of 5 ns under a 1000 V charging voltage. This is attributed to resonant voltage boosting and rapid diode reverse cutoff [14]. Pric et al. constructed an 8x8 diode matrix, generating an 8 ns pulse with an output/input voltage ratio nearing 9 [15]. However, the inflexibility of diodes relative to fully controllable switches leads to a fixed output pulse width in the DOS circuit, posing challenges in studying window effects during nanosecond electroporation.

For effective induction of electroporation, ultrashort nanosecond pulses are typically required to be delivered at a higher repetition frequency. In the study by Sanders et al., a linear resonant network, utilizing commercially available diodes, is presented as an alternative to the magnetic compression stage that requires an expensive specialized diode [16]. This configuration provides DOS circuits with the potential for enhanced high-frequency performance. In our previous research, when operating with a high-power DC

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supply, the maximum repetition frequency achieved by linear DOS circuits reached 1 MHz, surpassing this threshold proved to be exceedingly challenging [17]. This difficulty is primarily attributed to the LC oscillation duration and the theoretical maximum charging speed of the RC charging circuit. Besides, the high-frequency performance of DOS circuits is significantly influenced by energy conversion efficiency [18-20]. During the circuit charging/discharging cycle, significant energy from the DC supply is dissipated due to losses in charging resistors and switches. Specifically, increased frequency typically leads to elevated switching and resistive losses, along with a rise in DC supply output power, reducing pulse generator reliability and efficiency [21].

In this paper, the underlying principles of the proposed multi-resonant loop DOS circuit are first examined. This is followed by circuit-level theoretical analyses, aimed at selecting resonant network parameters that facilitate pulse width modulation. Subsequently, the theoretical maximum repetition frequency of traditional DOS circuits is calculated. To exceed this limit, a topology for a multi-stage modular DOS circuit utilizing frequency superposition is introduced. Additionally, the energy conversion efficiency of the charging circuit is analyzed to validate the superiority of the proposed circuit in high-frequency operation. The feasibility of the multilevel circuits is then evaluated through PSpice simulations. Finally, a 3-stage prototype is constructed to experimentally validate both the theoretical and simulated analyses.

II. Operational Principles of Single-Modular Circuits for Adjustable Pulse Width Output

Fig. 1 shows the proposed DOS circuit, comprising n resonant loops connected to the same DC supply. Each loop consists of a charge/discharge switch S_1, an energy storage capacitor C_1, and inductors L_1 and L_2. Charging occurs when S_1 is off, allowing the DC supply to charge C_1 via R_c and L_1. Once C_1 is charged to U_{dc}, S_1 turns on to start discharging. Independent control of switches S_{11} to S_{1n}, through timing adjustments of control signals V_{11} to V_{1n}, enables adjustable pulse widths. With C_1 and L_1 serving dual roles in both charging and resonant circuits, Section A calculates their parameters in the discharge state. After determining C_1 and L_1 values, Section B analyzes the circuit's charging dynamics.

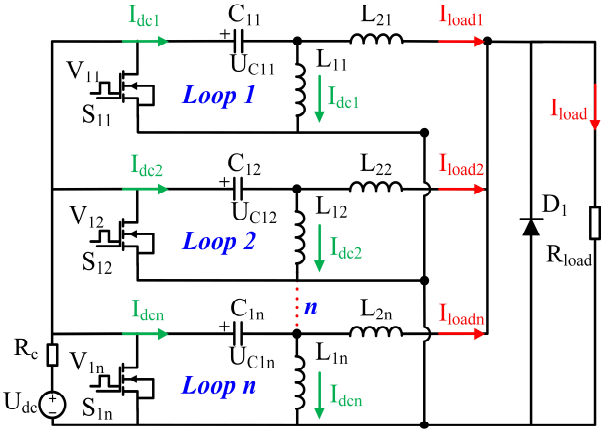

Fig. 1 Schematic of multi-stage loops for adjustable pulse width output.

A. Parameter design for resonant network with adjustable pulse width output

The analysis starts with switch S_1 turned on, focusing on a 2-stage loop where capacitor C_1 is charged to DC supply voltage U_{dc}. The circuit operation is categorized into resonant oscillation and load discharge, based on the diode's state.

1) *resonant oscillation*. The circuit with diode D_1 in the on-state is depicted in Fig. 2, where R_{on} is the forward resistance of the diode D_1. The value of the total current, I_{D1}, in the resonant network, plays a pivotal role in determining the output voltage U_{out}. It is derived from the summation of the resonant network current I_{L21} in Loop 1 and I_{L22} in Loop 2.

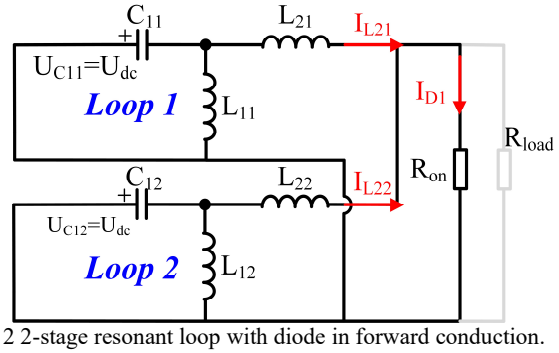

Fig. 2 2-stage resonant loop with diode in forward conduction.

The calculation of I_{L21} is first undertaken and its expression in the s-domain is given as follows:

$$
\begin{aligned}
I_{L21} &= -\frac{U_{dc}\begin{pmatrix} C_{11}C_{12}L_{11}L_{12}L_{22}s^3+\left(C_{11}L_{11}L_{12}+C_{11}L_{11}L_{22}\right)s \\ +C_{11}L_{11}R_{on}-C_{12}L_{12}R_{on}\end{pmatrix}}{\begin{pmatrix} a_1s^5+a_2s^4+a_3s^3+a_4s^2+a_5s \\ +L_{11}R_{on}+L_{12}R_{on}+L_{21}R_{on}+L_{22}R_{on}\end{pmatrix}} \\
a_1 &= C_{11}C_{12}L_{11}L_{12}L_{21}L_{22} \\
a_2 &= \left(C_{11}C_{12}L_{11}L_{12}L_{21}R_{on}+C_{11}C_{12}L_{11}L_{12}L_{22}R_{on}\right) \\
a_3 &= \left(C_{11}L_{11}L_{12}L_{21}+C_{11}L_{11}L_{21}L_{22}+C_{12}L_{11}L_{12}L_{22}+C_{12}L_{12}L_{21}L_{22}\right) \\
a_4 &= \begin{pmatrix} C_{11}L_{11}L_{12}R_{on}+C_{11}L_{11}L_{21}R_{on}+C_{11}L_{11}L_{22}R_{on} \\ +C_{12}L_{11}L_{12}R_{on}+C_{12}L_{12}L_{21}R_{on}+C_{12}L_{12}L_{22}R_{on}\end{pmatrix} \\
a_5 &= \left(L_{11}L_{12}+L_{11}L_{22}+L_{12}L_{21}+L_{21}L_{22}\right)
\end{aligned}
\tag{1}
$$

Directly solving such a high-order Laplace equation to obtain an analytical solution is evidently challenging. Here, by dividing both the numerator and denominator by s^3 and neglecting the terms with negative powers for time-domain analysis, the expression for I_{L21} can be derived as:

$$
I_{L21}(t)=\sinh(\omega_a\cdot t)\cdot e^{\frac{-\left(\frac{1}{L_{22}}+\frac{1}{L_{21}}\right)R_{on}\cdot t}{2}}\cdot V_m \tag{2}
$$

The oscillation period of the current is determined by ω_a, while its amplitude is decided by V_m. These parameters are respectively given as follows:

$$
\omega_a=\frac{\sqrt{C_{11}C_{12}L_{11}\begin{pmatrix} C_{11}C_{12}L_{11}L_{21}^2R_{on}^2+2C_{11}C_{12}L_{11}L_{21}L_{22}R_{on}^2 \\ +C_{11}C_{12}L_{11}L_{22}^2R_{on}^2-4C_{11}L_{11}L_{21}^2L_{22} \\ -4C_{12}L_{11}L_{21}L_{22}^2-4C_{12}L_{21}^2L_{22}^2\end{pmatrix}}}{2L_{21}L_{22}C_{11}C_{12}L_{11}} \tag{3}
$$

$$V_{\mathrm{m}}=\frac{2U_{\mathrm{dc}}L_{22}\sqrt{C_{11}C_{12}L_{11}\begin{pmatrix}C_{11}C_{12}L_{11}L_{21}^2R_{on}^2\\+2C_{11}C_{12}L_{11}L_{21}L_{22}R_{on}^2\\+C_{11}C_{12}L_{11}L_{22}^2R_{on}^2\\-4C_{11}L_{11}L_{21}^2L_{22}\\-4C_{12}L_{11}L_{21}L_{22}^2\\-4C_{12}L_{21}^2L_{22}^2\end{pmatrix}}}{\begin{matrix}-C_{11}C_{12}L_{11}L_{21}^2R_{on}^2-2C_{11}C_{12}L_{11}L_{21}L_{22}R_{on}^2\\-C_{11}C_{12}L_{11}L_{22}^2R_{on}^2+4C_{11}L_{11}L_{21}^2L_{22}\\+4C_{12}L_{11}L_{21}L_{22}^2+4C_{12}L_{21}^2L_{22}^2\end{matrix}} \tag{4}$$

Due to the relatively low on-resistance, R_{on}, of the diode, formula 2-4 can be simplified, yielding the resonant current I_{L21} in Loop 1 as follows:

$$I_{\mathrm{L21}}(t)=\sinh\left(\sqrt{\frac{-L_{22}\left(L_{11}+L_{21}\right)C_{12}-C_{11}L_{11}L_{21}}{L_{21}L_{22}C_{11}C_{12}L_{11}}}t\right)\mathrm{e}^{-\frac{\left(\frac{1}{L_{22}}+\frac{1}{L_{21}}\right)R_{\mathrm{on}}t}{2}}\sqrt{-\frac{L_{22}C_{11}C_{12}L_{11}}{L_{21}\left(L_{22}\left(L_{11}+L_{21}\right)C_{12}+C_{11}L_{11}L_{21}\right)}}U_{\mathrm{dc}} \tag{5}$$

Similarly, the resonant current I_{L22} in Loop 2 can be derived as follows:

$$I_{\mathrm{L22}}(t)=\sinh\left(t\sqrt{\frac{-\left(L_{22}+L_{12}\right)L_{21}C_{11}-C_{12}L_{22}L_{12}}{L_{21}L_{22}C_{11}C_{12}L_{12}}}\right)\mathrm{e}^{-\frac{\left(\frac{1}{L_{22}}+\frac{1}{L_{21}}\right)R_{\mathrm{on}}t}{2}}\sqrt{-\frac{L_{21}C_{11}C_{12}L_{12}}{L_{22}\left(\left(L_{22}+L_{12}\right)L_{21}C_{11}+C_{12}L_{22}L_{12}\right)}}U_{\mathrm{dc}} \tag{6}$$

Synchronizing the oscillation times of Loop 1 and Loop 2 with the diode D_1's reverse recovery time is crucial for achieving maximum reverse peak cutoff and generating high-amplitude pulses. When L_{21} and L_{22} vastly exceed L_{11} and L_{12}, and the products of $C_{11}L_{11}$ and $C_{12}L_{12}$ match T_{w}, the formulae can be combined to calculate $\mathrm{I_{D1}}$ through D_1.

$$I_{\mathrm{D1}}=U_{\mathrm{dc}}\sinh\left(\sqrt{-\frac{1}{T_{\mathrm{w}}}}\cdot t\right)\mathrm{e}^{\frac{(L_{21}+L_{22})R_{\mathrm{on}}\cdot t}{2L_{21}L_{22}}}\left(\sqrt{-\frac{T_{\mathrm{w}}}{L_{21}^2}}+\sqrt{-\frac{T_{\mathrm{w}}}{L_{22}^2}}\right) \tag{7}$$

Therefore, under a constant charging voltage U_{dc}, the frequency of the total resonant current I_{D1} is primarily determined by the T_{w}, while its amplitude is mainly dictated by L_{21} and L_{22}.

2) *resonant network discharging*. The circuit with diode D_1 in the off-state is depicted in Fig. 3.

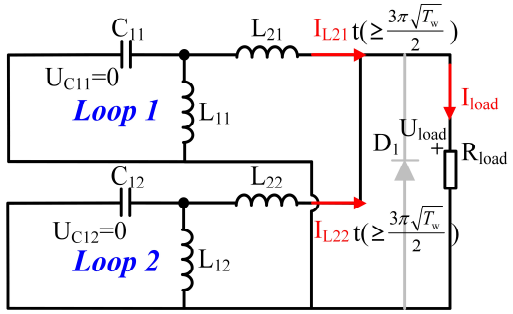

Fig. 3 2-stage resonant loop with diode in reverse cutoff

When the diode recovery time (t_{rr}) equals one-fourth of the resonant period, as expressed by the following equation:

$$t_{\mathrm{rr}}=\frac{\pi\sqrt{T_{\mathrm{w}}}}{2} \tag{8}$$

At this point, the diode loses its conductivity, and the currents I_{L21} and I_{L22} reach their maximum reverse values. L_{21} and L_{22} begin discharging to the load at these values:

$$I_{\mathrm{L21(trr)}}=\sqrt{\frac{T_w}{L_{21}^2}}U_{\mathrm{dc}} \tag{9}$$

$$I_{\mathrm{L22(trr)}}=\sqrt{\frac{T_w}{L_{22}^2}}U_{\mathrm{dc}} \tag{10}$$

As I_{load} is the sum of I_{L21} and I_{L22}, the calculation of I_{L21} is initially undertaken here. The expression in the s-domain, after eliminating the lower-order terms, is given as follows:

$$I_{\mathrm{L21}}(s)=\frac{C_{11}L_{11}\sqrt{\frac{T_w}{L_{21}^2}}U_{\mathrm{dc}}C_{12}L_{21}L_{22}L_{12}s^5}{C_{11}C_{12}L_{11}L_{21}L_{22}L_{12}s^6+\begin{pmatrix}C_{11}C_{12}L_{11}L_{12}L_{21}R_{\mathrm{load}}\\+C_{11}C_{12}L_{11}L_{12}L_{22}R_{\mathrm{load}}\end{pmatrix}s^5} \tag{11}$$

The time-domain expression is as follows:

$$I_{\mathrm{L21}}(t)=\sqrt{\frac{T_w}{L_{21}^2}}U_{\mathrm{dc}}\mathrm{e}^{-\left(\frac{1}{L_{22}}+\frac{1}{L_{21}}\right)R_{\mathrm{load}}\cdot t} \tag{12}$$

The time-domain I_{L22} expression can be similarly obtained as:

$$I_{\mathrm{L22}}(t)=\sqrt{\frac{T_w}{L_{22}^2}}U_{\mathrm{dc}}\mathrm{e}^{-\left(\frac{1}{L_{22}}+\frac{1}{L_{21}}\right)R_{\mathrm{load}}\cdot t} \tag{13}$$

By summing formulas 12 and 13, I_{load} can be obtained. Since U_{load} is the product of I_{load} and R_{load}, U_{load} can be expressed as:

$$U_{\mathrm{load}}(t)=\left(\sqrt{\frac{T_w}{L_{21}^2}}+\sqrt{\frac{T_w}{L_{22}^2}}\right)U_{\mathrm{dc}}R_{\mathrm{load}}\cdot\mathrm{e}^{-\left(\frac{1}{L_{22}}+\frac{1}{L_{21}}\right)R_{\mathrm{load}}\cdot t} \tag{14}$$

Consequently, the time t_{hf} for the output voltage U_{load} to decrease to half of its peak value is given as:

$$t_{\mathrm{hf}}=\frac{0.69315}{\left(\frac{1}{L_{22}}+\frac{1}{L_{21}}\right)R_{\mathrm{load}}} \tag{15}$$

Therefore, in the 2-stage loop configuration, the duration of the output voltage U_{out} is primarily determined by the sum of the reciprocals of inductances L_{22} and L_{21}. Assuming there are n loops, where the following conditions are satisfied:

$$L_{2i}=\frac{1}{k_i}L\left(i\geq 1,i\in\mathrm{N}^+\right) \tag{16}$$

The variable i represents the index of the ith Loop, L is the inductance value of L_{21} in Loop 1, and k_{i} is the ratio of inductance $L_{2\mathrm{i}}$ in Loop i to L_{21} in Loop 1, satisfying the following relationship:

$$k_1\leq k_2\leq\ldots\leq k_n \tag{17}$$

Since Loops 1 to Loop n can operate independently, based on formula 15, the achievable range of output pulse width adjustment on the load side is:

$$\frac{0.69315L}{R_{\mathrm{load}}\left(k_1+k_2+\ldots+k_n\right)}\leq t_{\mathrm{hf}}\leq\frac{0.69315L}{R_{\mathrm{load}}\cdot k_1} \tag{18}$$

The corresponding maximum output amplitude, V_{max}, is:

$$\frac{R_{\mathrm{load}}k_1\sqrt{T_{\mathrm{w}}}U_{\mathrm{dc}}}{L}\leq V_{\mathrm{max}}\leq\frac{R_{\mathrm{load}}\left(k_1+k_2+\ldots+k_n\right)\sqrt{T_{\mathrm{w}}}U_{\mathrm{dc}}}{L} \tag{19}$$

D_1 uses the CN25M diode with a 50ns reverse recovery time. For electroporation with 5-20 ns pulses and a 100 Ω load, formula 8 sets C_{1i} at 33nF and L_{1i} at 90nH. With n=3, calculations yield an inductance L of 2885 nH, and output characteristics are in Table I.

TABLE I
3-STAGE RESONANT LOOP NETWORK

Number of Closed Switches	Loop i	k_i	V_{max}	t_{hf}
1	1	1.00	1.89 U_{dc}	20 ns
1	2	1.33	2.51 U_{dc}	15 ns
1	3	2.00	3.78 U_{dc}	10 ns
2	12	2.33	4.40 U_{dc}	8.5 ns
2	13	3.00	5.67 U_{dc}	6.6 ns
2	23	3.33	6.29 U_{dc}	6.0 ns
3	123	4.33	8.18 U_{dc}	4.6 ns

B. Theoretical calculation of maximum repetition frequency for DOS charging circuit

Following the resonant network parameter calculations, this section analyzes the charging circuit, focusing on the maximum repetition frequency. Given the uniformity of capacitors (C_{11}=C_{12}=C_{13}) and inductors (L_{11}=L_{12}=L_{13}), Loop 1 is analyzed in detail with its s-domain representation provided.

$$I_{dc}=\frac{C_{11}U_{dc}}{s^2\cdot L_{11}\cdot C_{11}+s\cdot R_c\cdot C_{11}+1} \tag{20}$$

After the inverse Laplace transform is performed, the following expression is obtained:

$$I_{dc}=\frac{2e^{-\frac{R_c\cdot t}{2L_{11}}}\sqrt{C_{11}(C_{11}\cdot R_c^2-4L_{11})}\cdot U_{dc}}{C_{11}\cdot R_c^2-4L_{11}} \cdot\sinh\left(\frac{t\cdot\sqrt{C_{11}(C_{11}\cdot R_c^2-4L_{11})}}{2L_{11}\cdot C_{11}}\right) \tag{21}$$

The damping ratio of the circuit is largely influenced by the value of the charging resistor R_c. When R_c is less than $\sqrt{4L_1/C_1}$, the charging circuit is in an underdamped state. The current I_{dc} reaches its maximum value $I_{dc\_m}=U_{dc}\sqrt{C_1/L_1}$ at $t_{I\_m}=\pi\sqrt{L_1C_1/4}$. In this case, U_{C11} is

$$U_{C11}=U_{dc}\{\frac{1}{C_{11}\cdot R_c^2-4L_{11}}[-R_c\sinh(\frac{t\cdot\sqrt{C_{11}(C_{11}\cdot R_c^2-4L_{11})}}{2L_{11}\cdot C_{11}}) \cdot\sqrt{C_{11}(C_{11}\cdot R_c^2-4L_{11})}+\cosh(\frac{t\cdot\sqrt{C_{11}(C_{11}\cdot R_c^2-4L_{11})}}{2L_{11}\cdot C_{11}}) \cdot(-C_{11}\cdot R_c^2+4L_{11})\cdot e^{-\frac{R_c\cdot t}{2L_{11}}}]+1\} \tag{22}$$

Hence, the time t_{U_m} at which U_{C11} reaches its maximum value is $\pi\sqrt{L_{11}C_{11}}$. Given that C_{11} is 33 nF and L_{11} is 90 nH, the value of the time t_{U_m} is 171 ns. In underdamped conditions, this time value is relatively independent of the charging resistance R_c and represents the shortest charging time for the capacitor C_{11}. Considering that the time t_{osci} for the resonant circuit current to reach its reverse maximum value is $3\pi\sqrt{T_w}/2$ =257 ns, the minimum cycle time for the DOS circuit T_p is $t_{osci}+t_{U\_m}$=428 ns. Therefore, the maximum achievable operating repetition frequency f_{max} ($1/T_p$) is 2.3 MHz.

For $R_c \geq \sqrt{4L_{11}/C_{11}}$ (overdamped circuit state), the shortest charging time (t_{sc}) for capacitor C_{11} is defined when the voltage (U_{C11}) reaches 99% of the charging voltage (U_{dc}). Since the charging time should be less than the circuit operation cycle, the charging resistance must be satisfied:

$$R_c\leq\frac{1}{5\cdot f_{max}\cdot C_{11}} \tag{23}$$

When the charging resistance reaches its minimum value, the time t_{sc} also attains its minimum, which is calculated to be 330 ns according to formula 22. Therefore, T_p is

$$T_p=t_{osci}+t_{sc}=587\text{ ns} \tag{24}$$

The maximum repetition frequency f_m is

$$f_{max}=1/T_p=1.7\text{ MHz} \tag{25}$$

The DOS circuit achieves maximum frequencies of 2.3 MHz under zero damping and 1.7 MHz with overdamping. The higher frequency is theoretical, ignoring power and loss limits, while the lower accounts for practical constraints like charging resistance. This result indicates that enhancing the repetitive operating frequency of the DOS circuit by reducing R_c is subject to limitations.

III. Operating Principles of Multi-Stage Modular Frequency Superposition Circuits

To surpass the repetition frequency constraints of DOS circuits, a novel modular topology based on frequency superposition is developed (Fig. 4). Each module, consisting of three Loops, is connected through isolation circuits.

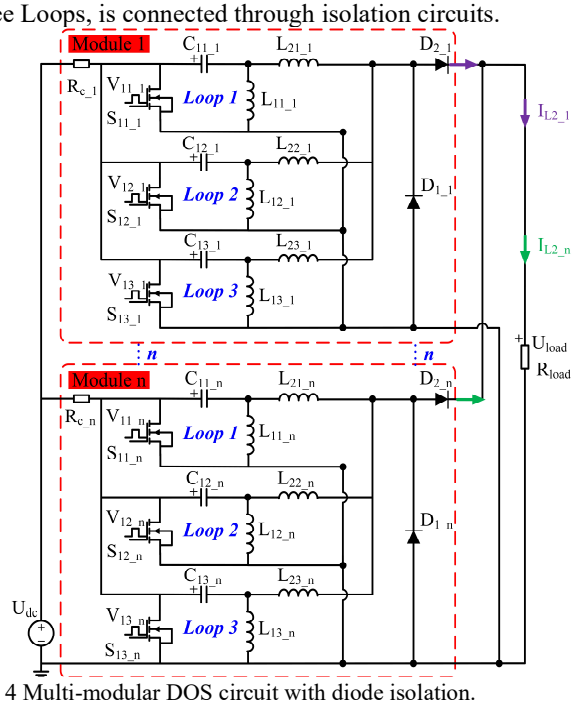

Fig. 4 Multi-modular DOS circuit with diode isolation.

Section A explains the control and timing of the multi-module circuit to boost frequencies. Section B compares its energy efficiency to single-stage DOS circuits at the same frequency. Section C examines how parasitic components in isolation circuits affect output. The analysis focuses on systems with only Loop1 active per module for clarity.

A. Basic principles of multi-modular frequency superposition

Initially, all switches are off and capacitors are charged to U_{dc}. Fig. 5 illustrates the timing for frequency superposition across multiple modules.

1) At t=0, the switch in Module 1 is turned on, placing the module in a discharge state. At t=t_{osci}, the current I_{L2} reaches its maximum reverse value, coinciding with the diode undergoing reverse cutoff, which leads to the generation of pulses with a fast rise time at load side. At t=t_{on}, the switch in Module 1 is turned off, transitioning the module into a charging state. Since the capacitors in the other modules are already fully charged at t=0, only one module is charging in the circuit at this time.

2) At t=t_{delay}, the switch in Module 2 is turned on, triggering the discharge process. A nanosecond pulse is subsequently produced at the load end at t=t_{delay}+t_{osci}. The time interval between the two discharges for the load is t_{delay}. At t=t_{delay}+t_{on}, the switch in Module 2 is turned off. At this moment, the number of charging modules increases to two, and Module 1 has been charging for a duration of t_{charg}=t_{delay}.

3) At t=(n-1)t_{delay}, the switch in Module n is turned on, initiating discharge. A pulse is then generated at t=(n-1)t_{delay} + t_{osci}. At this point, the load has received the nth pulse, with t_{delay} as the interval between pulses. At t=(n-1)t_{delay}+t_{on}, Module n finishes discharging and begins to enter the charging state. Consequently, all modules are in a charging state. The charging time t_{charg} for Module 1, Module 2, up to Module n-1 is (n-1)t_{delay}, (n-2)t_{delay}, and t_{delay}.

4) At t = nt_{delay}, Module 1 is poised to close again, marking the end of Cycle 1 and the commencement of Cycle 2. At this juncture, the multi-level modular circuit begins its repetitive operation, following the steps outlined in 1-3.

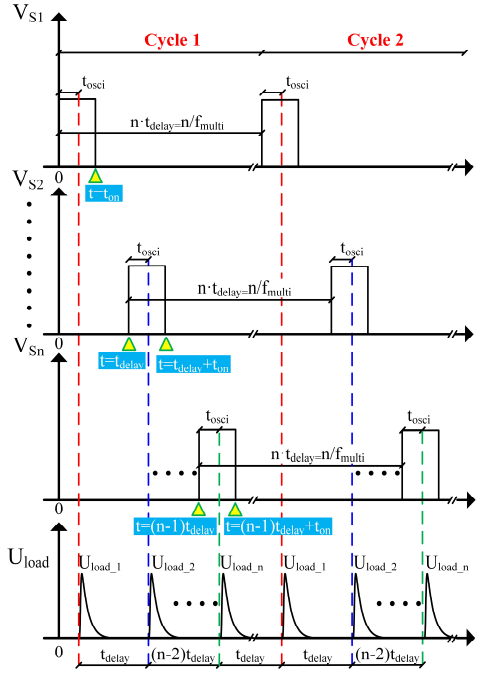

Fig. 5 The time diagram of modular frequency superposition.

For continuous and uniform pulse output, the operating frequency f_s of each individual module must satisfy the following conditions:

$$\begin{aligned} f_s &= f_{multi} / n \\ t_{delay} &= 1 / f_{multi} \end{aligned} \tag{26}$$

f_{multi} is the desired repetition operating frequency of the multi-level modular circuits. n (assumed to be an even number) *is* the number of DOS modules used in the proposed topology.

B. Analysis of energy conversion efficiency

A multi-stage DOS circuit employing frequency superposition is utilized to exceed traditional DOS circuits' theoretical repetition frequency limits. Besides, this circuit also shows enhanced energy conversion efficiency in charging compared to standard structures. Charging efficiencies of both architectures will be compared at equivalent repetition frequencies in subsequent analysis.

The theoretical frequency limit of DOS circuits, excluding semiconductor power limits and parasitic parameters, is set at 1 MHz from prior research [17]. Energy transfer efficiency differences between traditional single-stage and 3-stage frequency superposition DOS circuits are calculated under these conditions.

In Cycle 1, the average output power of the DC power supply gradually increases over time, stabilizing at its maximum value at (n-1)t_{delay} + t_{on}. Therefore, the time interval for efficiency comparison calculations is set between [nt_{delay}, (n+1)t_{delay}] in Cycle 2. The average energy transfer efficiency in the charging circuit, E_A, is defined as the ratio of the increase in energy stored in the capacitor C_1 over a specified time interval to the energy output by the DC supply.

$$E_A = \frac{\Delta W_c}{\Delta W_{dc}} \tag{27}$$

Where ΔW_c represents the increase in energy stored in capacitor C_1 after a duration of t_{delay}, and ΔW_{dc} denotes the energy provided by the DC supply during t_{delay}. This can be further rewritten as:

$$E_A = \frac{W_c}{W_c + W_s + W_R} \tag{28}$$

W_s and W_R represent the switching loss and resistive energy dissipation, respectively.

1) Capacitor C_1 stored energy W_c. In the multi-stage modular circuit, capacitors within the circuit undergo charging during this period. The changes in stored energy for capacitors C_2 and C_3, located in modules 2 and 3 respectively, are quantified as follows:

$$\begin{aligned} \Delta W_{cn} = \frac{1}{2}\sum_{n=2}^{3} C[U_{dc}(1-e^{-\frac{nt_{delay}-t_{on}}{R_cC}})]^2 - \\ \frac{1}{2}\sum_{n=2}^{3} C[U_{dc}(1-e^{-\frac{(n-1)t_{delay}-t_{on}}{R_cC}})]^2 \end{aligned} \tag{29}$$

For module 1, the increase in stored energy in capacitor C_1 is determined as:

$$\Delta W_{c1} = \frac{1}{2} C[U_{dc}(1-e^{-\frac{t_{delay}-t_{on}}{R_cC}})]^2 \tag{30}$$

Therefore, the sum of the increases in stored energy in the capacitors on modules 1-3 is calculated as:

$$W_{c\_m}=\sum_{n=1}^{3}W_{cn}=\frac{1}{2}C[U_{dc}(1-e^{-\frac{3t_{delay}-t_{on}}{R_cC}})]^2 \quad (31)$$

For a single-stage DOS circuit operating at 1 MHz, it is

$$W_{c\_s}=\frac{1}{2}CU_{dc}^2 \quad (32)$$

2）Switching losses. Following linearization of the current or voltage during the conduction/turn-off period of switch S_1, the calculated switching loss is:

$$\begin{aligned}P_s=2f_s[&\int_{t_1}^{t_2}U_{dc}\times\frac{U_{dc}}{R_c}(\frac{t-t_1}{t_2-t_1})dt\\&+\int_{t_2}^{t_3}\frac{U_{dc}}{R_c}[U_{dc}-\frac{U_{dc}}{t_3-t_2}(t-t_2)]dt]\\&=f_s\frac{U_{dc}^2}{R_c}[t_3-t_1]\end{aligned} \quad (33)$$

t_1 to t_2 and t_2 to t_3 represent the conduction delay time and the rise time of the switch, respectively. Based on formula 23, the relationship between P_s and the repetition frequency is as follows:

$$P_s=5U_{dc}^2f_m^2C_1(t_3-t_1) \quad (34)$$

Therefore, from the above formula, it is evident that the loss is directly proportional to the square of the frequency. When a three-stage circuit is employed, the loss of each module's switch can be reduced to one-ninth of that in a traditional DOS circuit.

3）resistive energy dissipation W_s. For the DOS circuit, it occurs during both turn-on and turn-off phases of the switch, represented by the following formula:

$$W_R=\frac{U_{dc}^2}{R_c}t_{on}+\int_{t_{on}}^{T_p}(\frac{U_{dc}}{R_c}e^{-\frac{t}{R_cC_1}})^2R_cdt \quad (35)$$

T_p is the operating period of the circuit. Clearly, a reduction in resistance and an increase in turn-on time t_{on} of switch lead to an increase in resistive losses.

Substituting formulas 29-35 into formula 28, the charging efficiencies for multi-stage modular and traditional single-stage DOS circuits can be derived as follows:

$$E_{Am}=\frac{\frac{1}{2}C[U_{dc}(1-e^{-\frac{3t_{delay}-t_{on}}{R_{cm}C}})]^2}{\begin{aligned}&\frac{1}{2}C[U_{dc}(1-e^{-\frac{3t_{delay}-t_{on}}{R_{cm}C}})^2+\frac{U_{dc}^2}{R_{cm}}t_{on}\\&+f_s\frac{U_{dc}^2}{R_{cm}}(t_3-t_1)+\int_{t_{on}}^{T_{pm}}\left(\frac{U_{dc}}{R_{cm}}e^{-\frac{t}{R_{cm}C_1}}\right)^2dt\end{aligned}} \quad (36)$$

$$E_{As}=\frac{\frac{1}{2}CU_{dc}^2}{\begin{aligned}&\frac{1}{2}CU_{dc}^2+f_{multi}\frac{U_{dc}^2}{R_{cs}}(t_3-t_1)\\&+\frac{U_{dc}^2}{R_{cs}}t_{on}+\int_{t_{on}}^{T_{ps}}\left(\frac{U_{dc}}{R_{cs}}e^{-\frac{t}{R_{cs}C_1}}\right)^2dt\end{aligned}} \quad (37)$$

From formulas 23 and 26, it follows that $f_{multi}=3f_s$, $T_{pm}=3T_{ps}$, and $R_{cm}=3R_{cs}$. Therefore, at $t_{on}=200$ ns and $U_{dc}=400$ V, E_{Am} and E_{As} are 35.0% and 22.5%, respectively. Utilizing a DOS circuit based on three-stage frequency superposition results in a 55.6% improvement in charging efficiency, compared to the traditional structure.

C. Isolation between modules

The diode-isolated 2-stage DOS circuit is shown in Fig. 6. For investigating the impact of introducing diodes D_{2_1} and D_{2_2} on the output characteristics of Module 1, Module 1 is in the discharging circuit state, while Module 2 is in the fully charged circuit state. To simplify the calculation of the KVL equation, Fig. 6(a) could be modified as Fig. 6(b), in which the diode D_{2_2} and D_{1_2} connected in series are reduced to a diode D_{1+2_2}.

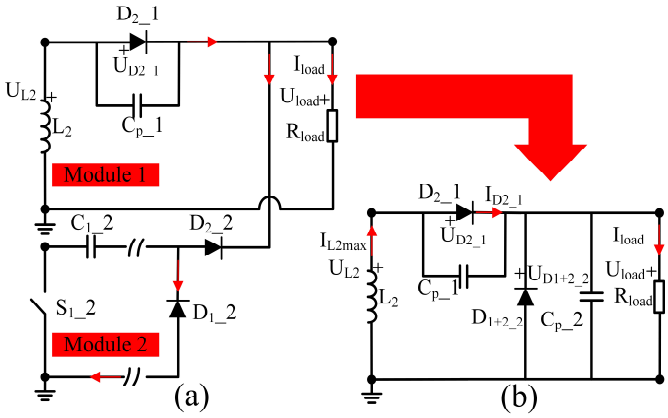

Fig. 6 The diode-isolated 2-stage DOS circuit. (a) Discharging equivalent circuit of 2-stage DOS at t≥t_{osci}. (b) Simplified equivalent circuit of Fig. 6 (a).

The KVL equation for the simplified equivalent circuit is as follows:

$$L_2\cdot(C_{p\_1}\cdot\frac{d^2U_{D2\_1}}{dt^2}+\frac{I_s\cdot\frac{dU_{D2\_1}}{dt}e^{\frac{U_{D2\_1}}{N\cdot V_T}}}{N\cdot V_T})=U_{D2\_1}+U_{D1+2\_2} \quad (38)$$

$$\begin{aligned}&I_{s2}\cdot e^{-\frac{U_{D1+2\_2}}{N_2V_{T2}}}+C_{p\_2}\cdot\frac{dU_{D1+2\_2}}{dt}+\frac{U_{D1+2\_2}}{R_{load}}=\\&C_{p\_1}\cdot\frac{dU_{D2\_1}}{dt}+I_s(e^{\frac{U_{D2\_1}}{N\cdot V_T}}-1)\end{aligned} \quad (39)$$

U_{D2_1} and U_{D1+2_2} are the voltages of diode D_{2_1} and D_{1+2_2}. C_p, I_s, N, and V_T are the parasitic capacitor, reverse saturation current, emission coefficient, thermal voltage of the diode respectively, where $U_{D2\_1(t=0)}=0$, $I_{load(t=0)}=I_{L2max}$, $U_{D2\_1(t=0)}=V_2$, and $U_{D1+2\_2(t=0)}=0$, $diffU_{2\_1(t=0)}=V_1$. The approximate Taylor series is used to solve the formula 38-39:

$$\begin{aligned}U_{load}(t)=&\frac{C_{p\_1}V_1+I_se^{\frac{V_2}{N\cdot V_T}}-I_s-I_{s2}}{C_{p\_2}}\cdot t+\frac{1}{2}\frac{1}{L_2C_{p\_2}^2N_2V_{T2}R_{load}}\omega\cdot t^2\\&-\frac{1}{6}\frac{1}{L_2C_{p\_2}^3N_2^2V_{T2}^2R_{load}^2}\xi\cdot t^3+\frac{1}{24}\frac{1}{NV_TC_{p\_1}L_2^2C_{p\_2}^4N_2^3V_{T2}^3R_{load}^3}\upsilon\cdot t^4\\&-\frac{1}{120}\frac{1}{N^2V_T^2C_{p\_1}^2L_2^2C_{p\_2}^5N_2^4V_{T2}^4R_{load}^4}\psi\cdot t^5+O(t^6)\end{aligned} \quad (40)$$

ω, ξ, υ and ψ are the coefficients of the second, third, fourth and fifth terms of the Taylor expansion, respectively. Overall, the introduction of diode D_{2_1} has a minor effect on the output pulse amplitude but results in a slight increase in the width of the

output pulses. The additional isolation diode D_{2_2} in module 2 causes not only an increase in the pulse width of module 1, but also a decline in the output amplitude. A smaller value of V_T and C_p could effectively mitigate these negative effects.

IV. Simulations Results

To validate the theoretical analysis, the PSpice circuit simulation model is constructed. The modular 3-stage circuit with frequency superposition used in the simulations is shown in Fig. 4, and the traditional single-stage DOS circuit is shown in Fig. 7 [16].

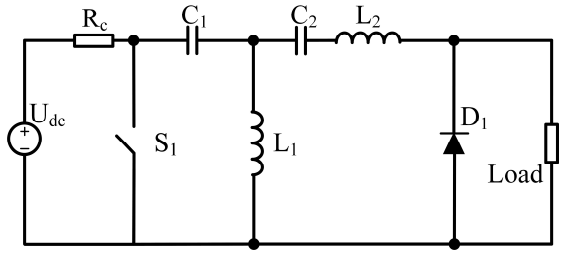

Fig. 7 Conventional single-stage DOS circuit structure

In the simulation setup with a 1 MHz repetition frequency, switch S_1 is closed at t=5 μs, marking the start of cycle 2 at t=8 μs. Therefore, the simulation results presented start from t=8 μs. Fig. 8 shows adjustable pulse widths for Loops 1, 2, 3, and 123, with corresponding U_{dc} values of 1756 V, 1321 V, 863 V, and 400 V. This result validates the previous analysis presented in Section A of Part II.

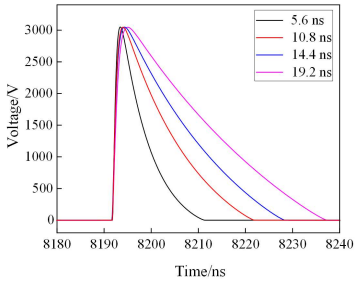

Fig.8 Simulation results of adjustable pulse width.

To verify the increased charging efficiency E_A of the proposed multi-stage modular frequency superposition compared to the traditional DOS circuit, simulations of both circuits at the same frequency are performed. Since the output energy of the DC source can be easily obtained in simulations, the original formula 28 for calculating the charging efficiency E_A can be updated as follows:

$$E_A=\frac{\frac{1}{2}CU_{dc}^2}{\int_0^{Tp} P_{DC}(t)dt} \tag{41}$$

Fig. 9 shows the simulated output power of the DC source at different operating frequencies. A higher output power DC source is needed for the conventional single-stage DOS circuit compared to the 3-stage DOS circuit at the same frequency. This indicates that the proposed structure reduces the associated costs of high-frequency operation, including high-capacity power supplies and energy consumption.

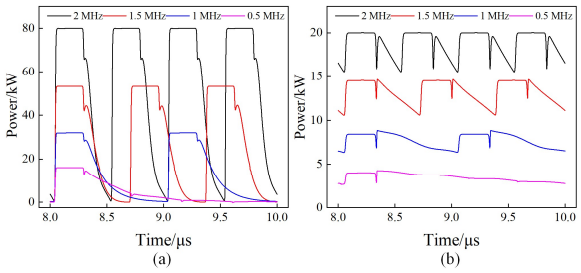

Fig. 9 The simulated waveforms of DC source output power P_{DC} under different operation frequencies. (a) Conventional single-stage DOS circuit. (b) The 3-stage modular DOS circuit with frequency superposition.

According to formula 41, the charging efficiency of the two circuit structures is shown in Fig. 10. The charging efficiency is significantly improved in the modular 3-stage DOS circuit compared to the conventional single-stage DOS circuit at the same operating frequency. Simulated results validate the theoretical analysis of formulas 27-37.

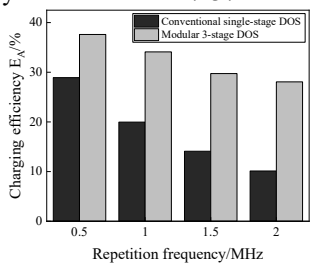

Fig. 10 Comparison of the charging efficiency between the conventional and proposed structures.

Figure 11 illustrates the attainment of a 3 MHz repetition frequency pulse output at the load side under the condition where the operational period (T_p) of each module is set to 990 ns, and the inter-module delay is configured at 330 ns. To enhance the quality of the output pulse, it is advisable to opt for a fast recovery diode with minimal junction capacitance.

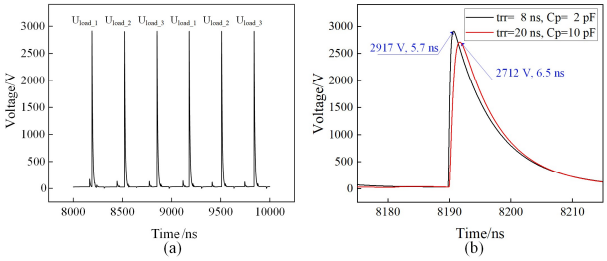

Fig. 11 Simulation waveforms of output voltage U_{load} in the 3-stage module with diode isolation at 3 MHz. (a) Output voltage U_{load}. (b) Impact of parasitic parameters of Diode D_{2_2} on U_{load_1}.

V. Experimental Results

A 3-stage prototype of DOS generators with diode isolation is constructed to validate the theoretical and simulated analyses. The trial prototype is depicted in Fig. 12, and key parameters of the proposed structure are presented in Table II. Experimental waveforms are captured using an oscilloscope (WaveSurfer 510; Lecroy, USA) equipped with a voltage probe (PPE 4 kV; Lecroy, USA) and Pearson current monitor (Model 6600; Pearson Electronics, USA).

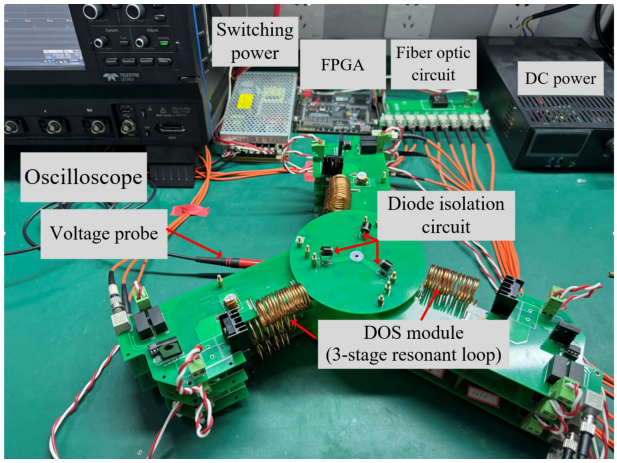

Fig. 12 The experimental prototype of three-module DOS circuit based on diode isolation.

TABLE II
MAIN SPECIFICATIONS

Symbol	Value
SiC MOSFET	IMZ120R030M1HXKSA1
Input voltage	400 V
R_c	5 Ω, 20 Ω
R_{load}	100 Ω[15, 17]
Driver	IXDN609
Resonant diode	CN25M
Isolation diode	FR2040
C_{1i}	33 nF (C1812C333KCRACTU)
L_{1i}	90 nH (1212VS-90NME)
T_p	990 ns
t_{delay}	330 ns
Loop *i*	Loop 123

Fig. 13 displays the output voltage of a single module containing three resonant loops. It is evident that voltage pulses with a pulse width ranging from 20.3 ns to 6.5 ns can be obtained on the load side.

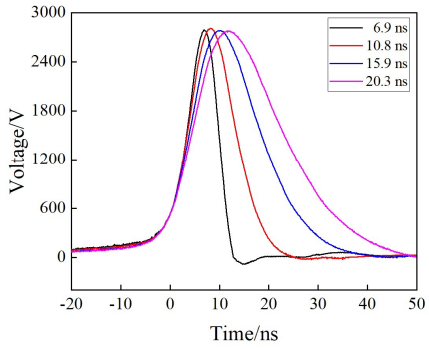

Fig. 13 Experimental waveforms of output voltage U_{load} with adjustable pulse width. The charging voltages for Loop 1, 2, 3, and 123 are 1700V, 1300V, 900V, and 400V, respectively.

Fig. 14 shows the differences in the DC source output characteristics between the conventional single-stage circuit and the 3-stage modular circuit. Experimental results indicate that at the same repetition frequency of 1 MHz, the 3-stage modular structure with frequency superposition consumes less energy from the DC source and has improved charging efficiency compared to the conventional single-stage circuit.

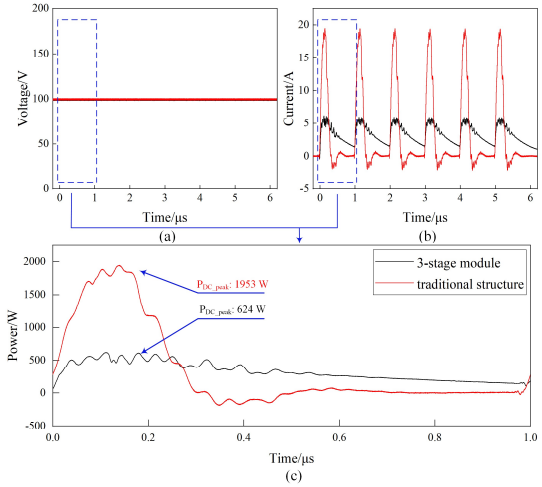

Fig. 14 The experimental waveforms of the DC source output in the 3-stage modular DOS circuit and traditional single-stage structure at 1MHz repetition frequency. (a) DC source output voltage U_{dc}. (b) Charging current I_{dc} to capacitor C_1. (c) DC source output power P_{DC}. P_{DC_peak} is the peak output power of the DC source, calculated as the maximum value of the product of U_{dc} and I_{dc}.

For the electroporation application in vitro experiments, the resistance of solution is equal to 104 Ω according to the $R_L=L^2/(V\cdot\sigma_L)$ (L is the electrode gap with 2×10^{-3} m, σ_L is the conductivity of the solution with 0.32 S/m, and V is the volume of the solution with 120 μL). Therefore, the load resistance R_{load} for the DOS circuit in this paper is set to 100 Ω. Fig. 15 demonstrates that pulses with an amplitude of 2.8 kV and a repetition frequency of 3 MHz are delivered to a 100 Ω resistive load. To the best of our knowledge, this achieves the highest operating frequency reported for DOS circuits based on commercially available linear resonant networks.

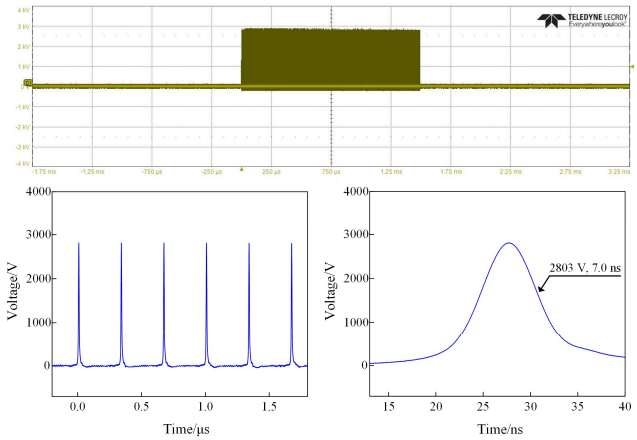

Fig. 15 Experimental waveforms of the output voltage U_{load} in a 3-stage modular DOS circuit at 3MHz repetition frequency within 1.5 ms burst, applied to the resistive load.

To demonstrate that the developed generator could be used for wider applications, an RC series-parallel load [22] is used to test the output characteristics of the proposed pulse generator. The experimental results in Fig. 16 show that nanosecond pulses with an amplitude of nearly 4 kV are obtained, further demonstrating the versatility of the pulse generator.

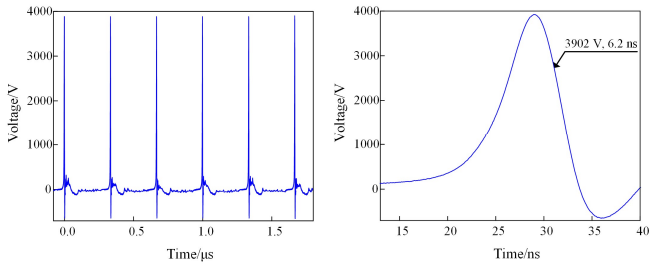

Fig. 16 Experimental waveforms of the output voltage U_{load} in a 3-stage modular DOS circuit at 3MHz repetition frequency within 1.5 ms burst, applied to the RC series-parallel load, consisting of a 2.2 kΩ resistor and a 1.5 nF capacitor in parallel, then in series with a 1 kΩ resistor.

In order to assess the suitability of this circuit topology for other nsPEF applications, such as plasma treatment, output tests were performed under RC parallel load conditions. The resistor and capacitor in the test are set at 1 MΩ and 15 pF, respectively. Fig. 17 shows that higher amplitude outputs are achieved under resistive-capacitive load at the same input voltage, compared to purely resistive conditions. This highlights the potential of the proposed structure for broader nsPEF applications.

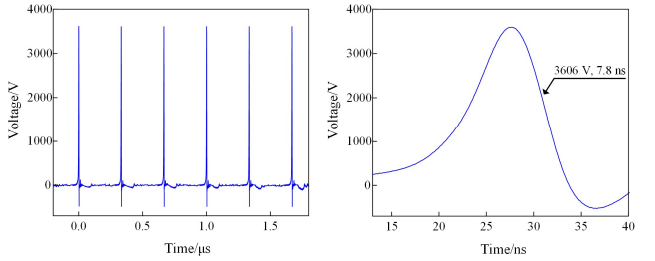

Fig. 17 Experimental waveforms of the output voltage U_{load} in a 3-stage modular DOS circuit at 3MHz repetition frequency within 1.5 ms burst, applied to the resistive-capacitive load.

VI. Conclusion

A novel DOS-based circuit with multi-stage resonant loops based on modular frequency superposition is proposed. It is capable of generating high-voltage pulses with adjustable nanosecond pulse widths at a 3 MHz repetition frequency, while operating at relatively high energy conversion efficiency. Theoretical analysis, simulation calculations, and experiments have been conducted, yielding the following results:

1) A DOS circuit composed of three resonant loops has been designed. By controlling the charging/discharging states of each loop, it is possible to generate seven sets of voltage pulses ranging from 6.9 ns to 20.3 ns. This marks a significant advancement in DOS circuit design, introducing the ability to generate pulses with adjustable pulse widths.

2) Due to limitations imposed by the oscillation time and recharge time of energy storage capacitors, the theoretical maximum operation frequency of traditional DOS circuits is 2.3 MHz. To surpass this threshold, a modular frequency superposition topology has been introduced. It can allow each module to deliver pulses to the load in sequence, achieving a multi-fold increase in the output repetition frequency.

3) The high-frequency performance of traditional DOS circuits is significantly affected by energy conversion efficiency. With the adoption of a modular frequency superposition topology, switch losses and resistive losses in the pulse generator are reduced, leading to a decrease in the required DC supply output power. This results in a notable enhancement of charging efficiency by 55.6 % when compared to traditional structures at the same operating frequency. This novel circuit approach showcases its potential and adaptability for high-frequency pulsed power designs.

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