Dual-Gate RF HEMT Based on P-GaN/AlGaN on Si Technology for Future X-Band On-Chip RF and Power Electronics

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Abstract

This paper presents dual-gate (2 × 0.5 µm) RF high electron mobility transistors (HEMTs) on P-GaN/AlGaN on Si substrate for next-generation airborne applications. The dual-gate architecture enhanced switching performance and reduced power loss, achieving a 77% reduction in off-state gate leakage current (0.3 mA/mm at V_{GS} = -6V) and improving the I_{ON}/I_{OFF} ratio by 1.9 orders of magnitude (5.45 × 10⁴) over single-gate devices. DC characterization revealed a current density (I_{DS}) of 712 mA/mm, on-resistance (R_{ON}) of 3.12 Ω.mm, peak transconductance (G_M) of 223 mS/mm, and pinch-off voltage (V_P) of -2.4 V. S-parameter measurements showed a cut-off frequency (f_T) of 7.12 GHz and a maximum oscillation frequency (f_{MAX}) of 24.18 GHz. These results support the integration of the proposed RF devices with existing E-mode power devices on a single P-GaN/AlGaN HEMT on Si platform, paving the way for integrated transceiver modules.

Introduction

Modern on-chip GaN transceivers surpass traditional GaAs designs, potentially reducing costs by up to 40% per module [1]. Fully integrated AlGaN/GaN transceiver front ends with high-power amplifiers and integrated power switches also achieve significant size and weight reductions [2]. Among the various GaN-based device architectures, normally off P-GaN/AlGaN high electron mobility transistors (HEMTs) have attracted considerable attention due to their improved reliability and robustness compared to other enhancement-mode (E-mode) HEMTs [3]. These devices offer high breakdown voltage, low on-resistance, and enhanced thermal stability, making them suitable for both RF and power switching applications. For the full realization of integrated transceivers, development of RF-capable P-GaN/AlGaN HEMTs on Si substrates is crucial. This approach leverages the cost benefits and scalability of Si while maintaining the high-performance characteristics of GaN technology.

Recent advancements have demonstrated RF P-GaN-gated HEMTs on Si with a cut-off frequency (f_T) of 6.0 GHz and a maximum oscillation frequency (f_{MAX}) of 9.8 GHz for devices with a gate length (L_G) of 1 µm, indicating the potential for high-frequency operation [4]. However, the presence of P-GaN under the gate results in increased gate-to-source capacitance (C_{GS}), thereby limiting RF performance.

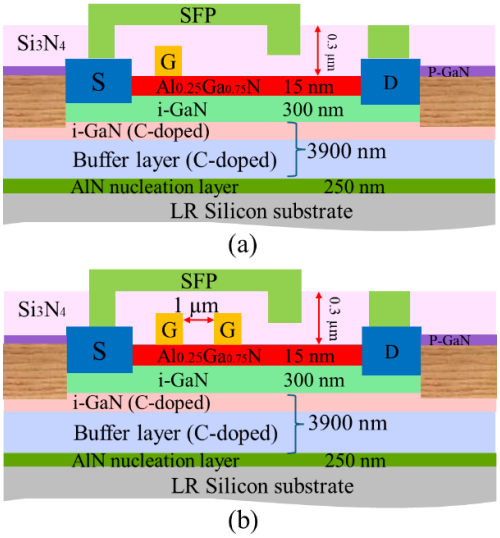


Fig. 1. Cross-sectional view of the fabricated (a) single-gate, and (b) dual-gate RF HEMTs on Si.

This paper presents a dual-gate RF HEMT based on P-GaN/AlGaN technology on a low-resistivity (LR) Si substrate, featuring an L_G of 2 × 0.5 µm. The device was evaluated against a single-gate HEMT on the same substrate, demonstrating superior switching performance, reduced power loss, and enhanced channel control. Notably, the dual-gate design suppressed off-state gate leakage current by 77%, reducing it to 0.3 mA/mm at V_{GS} = -6 V, thereby improving reliability and power efficiency. Additionally, the I_{ON}/I_{OFF} ratio increased by 1.9 orders of magnitude to 5.45 × 10⁴. S-parameters analysis showed an f_T of 7.12 GHz and an f_{MAX} of 24.18 GHz, indicating suitability for next-generation airborne applications.

Material and Device Fabrication

The study used commercial P-GaN/AlGaN HEMTs on 6-inch LR Si (σ < 0.03 Ω.cm). The structure included from top to bottom a 3.9 µm buffer layer, a 300 nm undoped GaN layer,

and a 15 nm undoped $Al_{0.25}Ga_{0.75}N$ barrier layer, topped with a 60-70 nm P-GaN doped with Mg at 3×10^{19} cm^{-3}, as shown in Fig. 1.

Single-gate and dual-gate HEMTs were fabricated simultaneously for accurate comparison. The process began with alignment markers using a two-step method to ensure precise photolithography and e-beam lithography alignment. Inductively Coupled Plasma Reactive-Ion Etching (ICP-RIE) with Ar/Cl_2 was used to etch the GaN epitaxial layers to ~1.5 µm before metal patterning. The developed marker technology is compatible with both dark and transparent GaN substrates, including sapphire and SiC, enabling broader material integration.

The top P-GaN layer was selectively etched in active areas using low-damage ICP-RIE with $BCl_3/Cl_2/SF_6$ prior to depositing Ti/Al/Ni/Au Ohmic contacts and annealing at 790°C in an N_2 atmosphere. Device isolation was achieved via ion implantation to a depth of ~200 nm, followed by Ni/Au Schottky gate deposition. A 100 nm plasma-enhanced chemical vapor deposition (PECVD) Si_3N_4 layer was used for passivation, reducing surface states and improving device stability. Si_3N_4 windows were etched using RIE with SF_6 before final bond-pad and source-field plate (SFP) deposition.

Fig. 2 details the fabrication steps, highlighting critical processing stages. Scanning electron microscopy (SEM) images of the dual-gate HEMT are shown in Fig. 3. The device gate width (W_G) and L_G were 2×50 µm and 0.5 µm, respectively. The source-to-drain distance (L_{SD}) and gate-to-source distance (L_{GS}) were 5 µm and 1.5 µm, respectively.

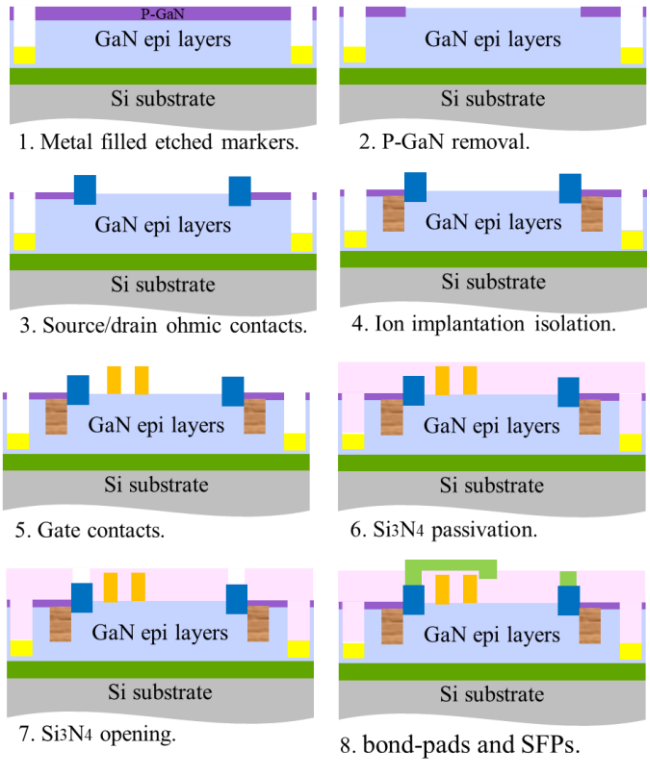


Fig. 2. Fabrication steps of RF dual-gate HEMT on Si substrate.

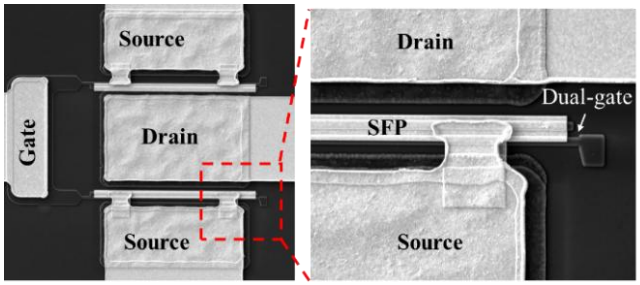


Fig. 3. SEM image of the fabricated dual-gate RF HEMT on Si substrate.

RESULTS AND DISCUSSIONS

A. DC Characteristics

Fig. 4 presents the transfer characteristics of both devices, showing a pinch-off voltage (V_P) of approximately -2.6 V for each. Both devices exhibit similar trends as the drain-to-source voltage (V_{DS}) increases, where transconductance (G_M) and drain-to-source current (I_{DS}) decrease due to self-heating effects. Compared to the single-gate HEMT, the dual-gate HEMT demonstrated significant enhancements in I_{ON}/I_{OFF} (from 6.2×10^2 to 5.4×10^4) and gate leakage (I_{GS}), reducing

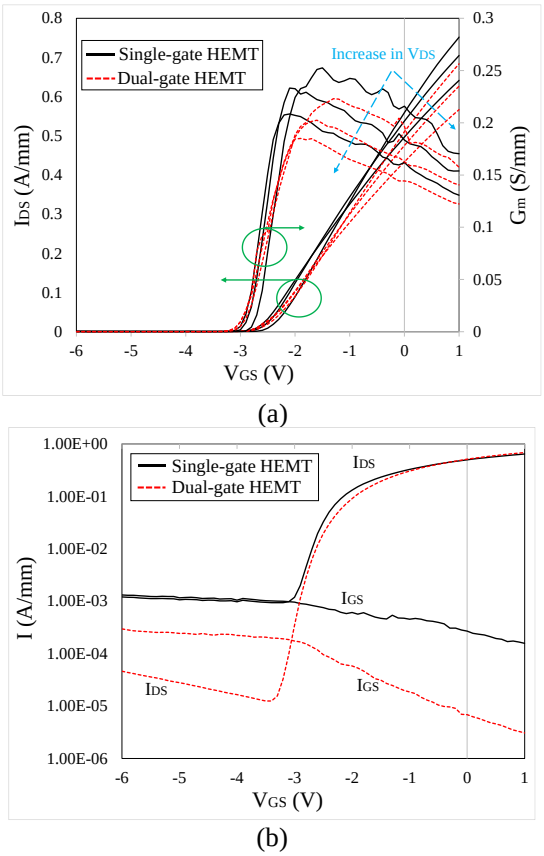
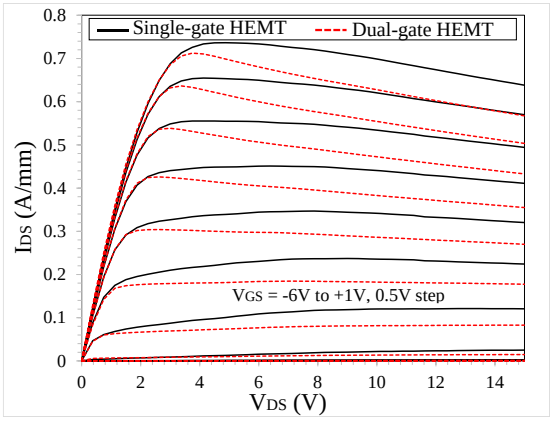
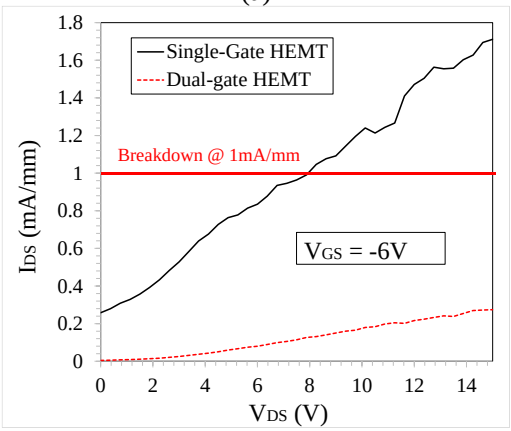


Fig. 4. (a) Transfer, and (b) pinch-off and gate leakage characteristics of the fabricated devices.



(a)



(b)

Fig. 5. (a) output characteristics, and (b) OFF-state current leakage of the fabricated devices.

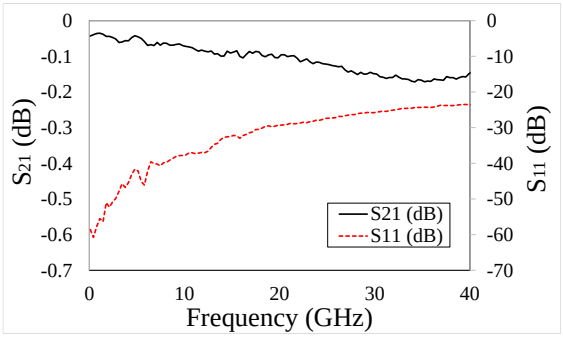
by 77% at V_{GS} = -6 V. Additionally, the peak G_M remains high at 223 mS/mm with minimal degradation.

Fig. 5a presents the output characteristics of both devices up to V_{DS} = 15 V. No compromise in on-resistance (R_{ON}) was observed, with R_{ON} = 3.12 Ω·mm. Comparing the two devices, the dual-gate HEMT is more susceptible to self-heating effects, where the output current begins to degrade at voltages above 2 V, though it achieved a maximum I_{DS} of 0.712 A/mm at V_{GS} = 1 V. Additionally, in Fig. 3, the off-state output current leakage at V_{GS} = -6 V was reduced by 84% at V_{DS} = 15 V.

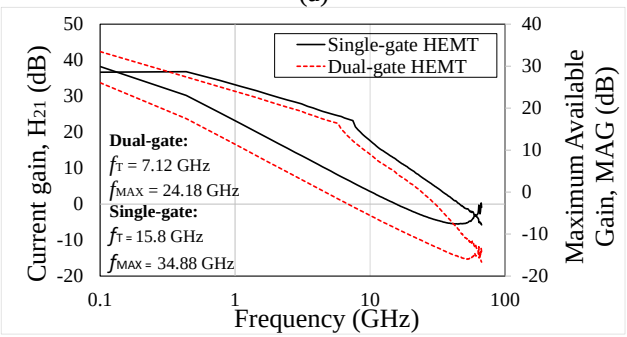
B. RF Characteristics

On-wafer small-signal S-parameter measurements were performed using a vector network analyzer (Agilent E8361A). The system was calibrated with an off-wafer calibration impedance standard substrate (ISS), using a Short-Open-Load-Thru (SOLT) calibration technique. Fig. 6 illustrates the small-signal S-parameter characteristics.

In Fig. 6(a), the RF losses of a 0.3 mm-length 50 Ω CPW line show an insertion loss of 0.17 dB at 35 GHz. Additionally, a good impedance match was observed, with S_{11}



(a)



(b)

Fig. 6. (a) CPW loss, and (b) |H21| MAG for the fabricated HEMTs.

remaining below -20 dB up to 40 GHz, indicating minimal signal reflection. This suggests that the thick GaN buffer (~3.9 µm) provided excellent RF isolation from the lossy Si substrate, thereby enhancing transmission characteristics and minimizing substrate-induced losses for high-frequency applications.

Fig. 6(b) presents the current gain |H_{21}| and Maximum Available Gain (MAG) of the fabricated single-gate and dual-gate RF HEMTs. The f_T and f_{MAX} of both devices were measured at maximum G_M under V_{DS} = 15 V and V_{GS} = -1 V. A noticeable degradation in f_T (by 54%) and f_{MAX} (by 31%) was observed in the dual-gate device, primarily due to the increased total L_G, which doubled from 0.5 µm to 1 µm. This increase in L_G results in higher gate resistance (R_G) and parasitic capacitance (C_{GS}), thereby limiting high-frequency performance. However, further enhancement in f_T by more than 50% is feasible by reducing L_G to 0.25 µm, following an optimized aspect ratio of 1:15 [5]. These results highlight the trade-offs between improved gate control and high-frequency performance in dual-gate designs.

CONCLUSIONS

This study demonstrated the feasibility and advantages of a dual-gate RF HEMT based on P-GaN/AlGaN technology on a LR Si substrate. Compared to its single-gate counterpart, the dual-gate device exhibited significantly improved switching characteristics, enhanced channel control, and reduced power losses. The suppression of off-state gate leakage by 77% and the substantial increase in the I_{ON}/I_{OFF} ratio highlight its

potential for reliable high-power applications. Although the increased gate area led to a trade-off in high-frequency performance, further optimization, such as reducing L_G, could mitigate these effects. With an f_T of 7.12 GHz and an f_{MAX} of 24.18 GHz, the dual-gate RF HEMT demonstrates strong potential for on-chip power and RF integration in advanced transceiver applications.

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