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PAPER

AlGaAs VSCELs grown on thin 150 mm germanium substrates

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Abstract

To reduce material usage and minimise device cost the use of reduced substrate thickness is considered in high volume vertical-cavity surface-emitting laser (VCSEL) manufacturing. For large-diameter VCSEL wafers, germanium (Ge) is emerging as an alternative substrate solution. In this work, VCSEL structures designed for 940 nm emission are grown by metal–organic vapour-phase epitaxy on 150 mm (6 inch) germanium substrates of thickness 675, 450 and 225 μm. Using on-wafer testing of fabricated devices, threshold current density, differential resistance, and emission wavelength are compared across the three substrate thicknesses, with results demonstrated for the first time on a Ge wafer thickness of 225 μm. These results underline the potential of thin Ge substrates for reduced material usage in VCSEL manufacturing.

1. Introduction

Vertical-cavity surface-emitting lasers (VCSELs) emitting in the 800–1000 nm range are today a commercialised technology playing a significant role in short-reach data communication as well as 3D sensing applications [1]. The large expansion in the VCSEL market in 2017, driven by the consumer smartphone demand, necessitated the scale-up to 150 mm (6 inch) diameter substrates. Since then, billions of chips have been shipped worldwide. In more recent years, work has been done to transition to 200 mm (8 inch) production [2], motivated by the promise lower cost and enhanced sustainability. The increase of substrate diameter in the production of VCSELs is the natural progression towards enhanced throughput and reduced cost per chip, however, scaling GaAs substrate sizes beyond the conventional 150 mm diameters introduces significant technical and material challenges. As the substrate diameter increases, it becomes increasingly difficult to achieve uniform epitaxial growth across the entire wafer surface resulting from the unavoidable spatially varying deposition rate within an MOVPE reactor. This non-uniformity can result in gradients of layer thickness, composition, and doping concentrations, which are critical parameters for the performance and reliability of VCSELs. Variations in these parameters lead to non-uniformity in lasing wavelengths and device efficiencies which can affect overall yield relative to target specifications. Furthermore, given that VCSELs are comprised of on the order of 200 epitaxial layers, the slight lattice mismatch between AlAs (or high-Al containing AlGaAs) and GaAs (0.16% [3]) compounds into a large compressive strain which bows/warps the VCSEL wafer, adding further complexity in subsequent lithography and etching. This issue worsens as the substrate diameter is increased, with a bow of approximately 150 μm for a 150 mm wafer and $\sim$200 μm for a 200 mm wafer [4].

It has been suggested that germanium (Ge) is the ideal substrate for volume VCSEL production [5] due to some favourable properties relative to GaAs, previously reported in [2, 4]. Ge has a lattice constant that sits between GaAs and AlAs meaning that the strain-induced wafer bow issue which exists with GaAs is reduced for Ge substrates. Additionally, Ge is mechanically stronger and more resistant to warp. As such, the maximum height variation across a 150 mm, 675 μm thick, Ge-substrate VCSEL wafer is typically $<$20 μm and is driven by the surface height fluctuations of the bare substrate before growth. Moreover, the higher thermal conductivity of germanium compared to GaAs has been shown to enhance the thermal performance of VCSELs [6], which is important for maintaining performance stability and prolonging lifetime,

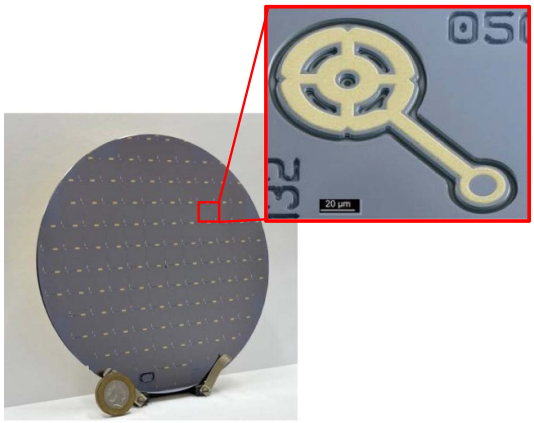

Figure 1. 150 mm-diameter 675 μm-thick Ge substrate wafer fabricated with a stripped back VCSEL process. The inset shows an image of an individual device used in this study. Each 150 mm wafer contains over 150 000 individual VCSEL devices.

particularly in high-power and high-temperature applications. Previous work has demonstrated parity in the electro-optical performance of Ge and GaAs-substrates VCSELs and the advantages of improved uniformity on Ge [2, 7, 8]. There have also been reports detailing the growth of AlGaAs-based structures (distributed Bragg reflector (DBR) and half-VCSEL structures) on bulk Ge substrates utilising epitaxial nucleation layers [9–11].

As with all consumer markets, a main priority is the VCSEL average selling price (ASP) and cost per wafer. Increasing GaAs substrate diameters $\geqslant$200 mm allows for a reduction in ASP somewhat but is hindered by the high-cost point of the superior substrate quality required for laser devices. Ge, on the other hand does not suffer in this way as high-quality substrates are commercially available up to 300 mm [12] for already-established supply chains. Another possibility for a reduction in cost per wafer is to grow on a thinner substrate, increasing the number of possible wafers from a single boule. VCSELs on Ge have, so far, been grown on 625–725 μm thick substrates at 150 mm, equivalent to those on GaAs, but recent research has also demonstrated successful growth on 425 [13], 375 [10], and 330 μm [14] thick Ge on 100 mm (4 inch) wafers. Moreover, the substrate makes up more than 98% of the total material of a VCSEL and, prior to packaging, more than 75% of the substrate will be removed, usually by mechanical grinding. Growing on thinner substrates can significantly reduce the amount of material wasted, but this is not an option for GaAs wafers due to the strain and subsequent wafer bow. Ge, on the other hand, is more tolerant to the strain effects driven by the VCSEL epi-layers and have been widely used in the production of III–V solar cells on substrates $<$200 μm thick [15]. If VCSELs, which are more difficult to manufacture, can be demonstrated successfully on thinner substrates the advantages of a reduction in cost due to a reduction in material required for epitaxy and a reduction in material usage can be realised.

In this paper, we assess the performance of VCSEL devices processed from nominally identical epitaxial structures grown on varying Ge substrates thicknesses, over 150 mm. An example is shown in figure 1. This study is concerned with the impact of substrate thickness on both individual device performance and wafer-scale variation. As such, each wafer is compared in terms of key figures of merit: threshold current density, lasing wavelength, series resistance, optical power, external differential efficiency, and also thermal performance. These quantities and their on-wafer variations are compared for each growth substrate thickness.

2. Materials and methods

2.1. Epitaxial structures and device fabrication

The MOVPE-grown structures used are generic *p–i–n* layout, designed and produced by IQE plc, for 940 nm emission wavelength. The active region is a multi-quantum well centred in a λ-thick separate confinement heterostructure (SCH). The optical cavity is formed by sandwiching the SCH between an upper p-type AlGaAs DBR mirror and lower n-type AlAs/AlGaAs DBR mirror. A buried $Al_{0.98}Ga_{0.02}As$ layer is included in the top DBR for optical confinement and current funnelling following selective oxidation. This structure was grown simultaneously on 150 mm Ge substrates of 675, 450, and 225 μm thickness to enable a representative comparison. Growth conditions were optimised for the 225 μm substrate to account for temperature gradients between the thickest and thinnest substrates. These substrate thicknesses are commercially available from Umicore N.V. and were not thinned specifically for this study.

The devices fabricated for this study are Quick VCSEL (QuickSEL) structures, which employ a stripped-back fabrication process designed to minimise time-to-result with minimal impact on device performance. Details of the design is given in [16]. The mesas are defined by an inductively coupled plasma etch to just below the active region to allow the selective oxidation to take place. Selective wet thermal oxidation was carried out using a single-wafer conduction heated furnace, with an infrared camera for *in-situ* monitoring across the wafer. The nominal oxidation length is 15 μm, measured at the centre of the wafer. The furnace makes use of differential pressure across the wafer to negate the temperature effects of wafer bow on oxidation rate [6, 17]. *P*-contacts and bond pads are formed via a liftoff process of a Ti/Pt/Au stack, and a back-side blanket-coating of standard n-contact metal for GaAs and Ge provides a global contact for each wafer. Ohmic contacts are formed as the final step by a combined annealing process for both p and *n*-contacts.

2.2. Experimental procedure

For the assessment of device performance, the power-current-voltage (PIV) characteristic and optical spectra are measured across the intact 150 mm wafers using a semi-automated probe station. The probe station is equipped with an integrating sphere and calibrated power meter for true optical power measurements. A small portion of the light is tapped off from the sphere and fibre-coupled to a high-resolution spectrometer for fast mapping of the peak lasing wavelength. The substrate temperature is 25°C for all measurements except where thermal performance investigating, where the substrate temperature is raised between 25 and 75°C.

The oxidation extent at 96 different points across each 150 mm wafer was subsequently determined from electrical test structures. Measurements of conductance versus mesa diameter and fitting with a relevant model allows the oxidation extent to be inferred from the x–intercept. The uncertainty in the oxidation length is given as $\pm$ 0.5 μm from the error of the fit.

3. Device results & discussion

3.1. Threshold requirement

Raw PIV data is presented in figure 2(a) for ~10 μm aperture devices measured at the centre of each wafer. The threshold current, I_{th}, is extracted from the *P–I* data and the mapping of the local oxidation extent is used to calculate the threshold current density, J_{th}. This is shown in figure 2(b) for oxide apertures ranging ~1–14 μm in diameter, with the points corresponding to the raw data in figure 2 circled. Locally, at the wafer centres, we find J_{th} on the 225 μm substrate to be higher than that of the 450 and 675 μm substrates, with an increase of ~0.3 kA cm^{-2} for large aperture devices. However, the full distribution of J_{th} for all devices on the wafer presents a modified picture. A histogram of J_{th} for 43 μm mesa diameter devices (~10 μm aperture) for each substrate thickness is shown in figure 3. The histograms are fit with lognormal distributions of mean 1.59, 1.62, and 1.64 kA cm^{-2} for the 675, 450, and 225 μm wafers, respectively. However, we observe an elongated tail for the 225 μm wafer tending to high values of J_{th}. This is reflected in the corresponding variance of the distributions which are 0.14, 0.15, and 0.35 kA cm^{-2} for the 675, 450, and 225 μm wafers, respectively. The origin of the high J_{th} tail for the 225 μm wafer is a variation in the oxidation extent at particular regions. At the bottom right of the wafer, the oxidation extent is longer, leading to smaller aperture sizes for a given mesa size which results in an increase of J_{th}. At the top edge of the wafer, the oxidation extent is significantly shorter which results in a leakage path due to the incomplete oxidation of the contact pad region of the QuickSEL devices. Therefore, at the top edge, the assumptions made when calculating the oxidation extent using the electrical method are not valid, hence skewing the values of *J*th. This can be seen more clearly in the contour plots of figure 4, which show the wafer-scale variation of J_{th} for each wafer, with cross-hatched regions used to indicate areas with these skewed higher J_{th} values removed, that are visible in the tail of figure 3. Investigation into potential temperature non-uniformities creating oxidation length variation, show that there is less than 1.2 °C in substrate temperature measured by an *in-situ* pyrometer during the oxidation process. This temperature variation does not provide sufficient variation to cause the differences in oxidation rates seen and the corresponding J_{th}. On the other hand, the threshold current density of the 675 and 450 μm wafers in terms of mean, variance, and spatial distribution match very well. Some explanation of possible causes for the observed difference in J_{th} is given in section 3.7.

3.2. Electrical resistance

VCSELs inherently have high electrical resistance due to the large number of epitaxial interfaces. Minimising this resistance is desirable for limiting Joule heating and is addressed with high doping levels and compositional grading at interfaces. For our devices, we characterise the electrical differential resistance, R_d, from the slope of the I–V characteristic. This is shown for ~10 μm oxide aperture devices of each substrate

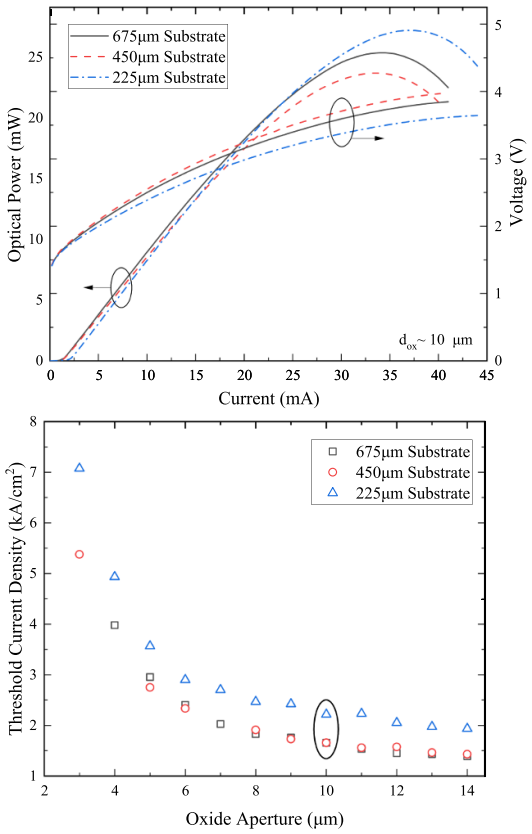

Figure 2. PIV curves for ∼10 μm diameter oxide aperture VCSELs measured at the centre of each 150 mm wafer of varying substrate thickness (a). Extracted threshold current densities as a function of oxide aperture for the same local region (b).

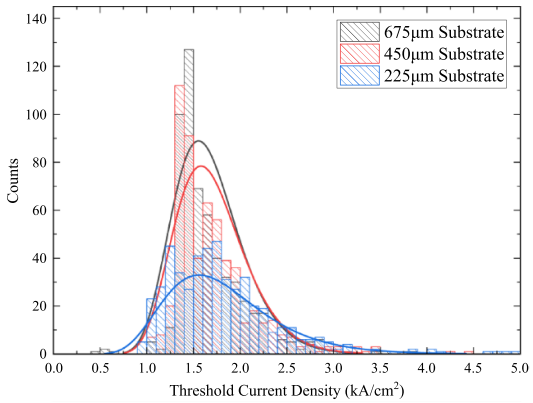

Figure 3. Histogram of threshold current density for 43 μm mesa devices across 6 inch wafer, fit with a lognormal distribution (solid lines).

thickness in figure 5, the same devices as figure 2(a). We observe a reduced R_d above turn-on, in the linear region of the I–V, for the 225 μm substrate device. We extract and compare values of R_d (slope of the linear region of the I–V between 2.0 and 2.4 V) and the reduction is more clearly seen when plotted as a function of oxide aperture, as in figure 6(a). This is observed to be the case across the whole wafer, as shown in the histograms of figure 6(b). The 675 and 450 μm wafers are fit with a Gaussian distribution of mean of 91.6 and 91.9 Ω, respectively. The distribution of the 225 μm has a mean of 74.6 Ω, but is negatively skewed unlike the 450 or 675 μm, with a large tail towards lower resistance values. Unlike for J_{th}, the differential resistance is found to be consistently lower for the 225 μm wafer relative to the 675 and 450 μm wafers. To better understand this, circular-transfer length method (CTLM) measurements were performed for the p-ohmic contact. All wafers have comparable specific contact resistances with mean values of 9.2×10^{-7}, 3.6×10^{-6}, and 8.8×10^{-7} Ω cm^{-2} for the 675, 450, and 225 μm wafers, respectively—comparable to

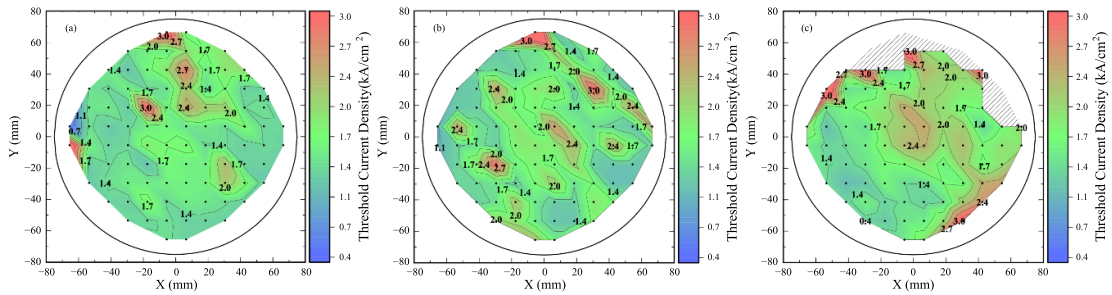

Figure 4. Contour plots for threshold current density of 43 μm mesa diameter VCSELs across (a) 675, (b) 450, and (c) 225 μm thick Ge substrate wafers.

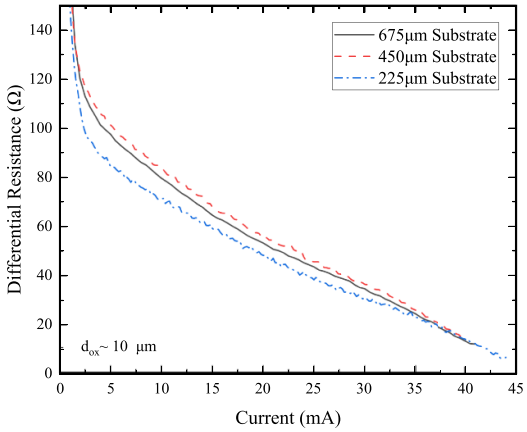

Figure 5. Measured differential resistance characteristic of 43 μm mesa diameter VCSELs on 675, 450, and 225 μm substrate VCSELs.

previous work on Ge substrate wafers [6]. The wafer-scale sheet resistance, R_{sheet}, of the highly p-doped GaAs cap layers are extracted from the same tests and plotted in figure 7. The mean sheet resistance value across each substrate thickness wafer is 55.4, 56.2, and 45.7 Ω □ for 675, 450 and 225 μm respectively. The variance of the distribution is >12 times higher for the 225 μm wafer and the driver of this can be seen in the contour plots of figure 7(c)—there are large regions with considerably lower sheet resistances relative to the 675 and 450 μm wafers, which would suggest higher levels of p-doping in the cap layers. The lowest sheet resistances are seen at the top and right-hand outer edge, which correlate again to the regions of slower oxidation previously mentioned. The values at the centre of the wafer in figure 7(c) are however, consistent with those seen across both 675 and 450 μm wafer in figures 7(a) and (b). Although the sheet resistance represents the topmost layers of the epitaxial structure, it can be used as an indicator of general doping concentration throughout the full stack. As such, these results would suggest that the rate of dopant incorporation is significantly higher for the 225 μm wafer, likely driven by temperature effects relating to the reduced thermal mass relative to the 675 and 450 μm substrates.

3.3. Differential efficiency

The external differential efficiency, η_{d}, is calculated from the slope of the P–I curve, and, in figure 8(a), this is plotted as a function of bias current for ∼10 μm aperture devices, measured at the centre of the wafer. The peak differential efficiency, $\eta_{\text{d,peak}}$, is then extracted and plotted against the oxide aperture diameter for each substrate thickness, shown in figure 8(b). For apertures>6 μm, $\eta_{\text{d,peak}}$ is observed to plateau (with some scatter) and values range from ∼0.97–1.07 W A^{-1} . We find $\eta_{\text{d,peak}}$ to be uniform across the 675 and 450 μm wafers, however, the values at the top edge and bottom right edge of the 225 μm wafer diverge, which can be seen in the contour plots of figure 9. The central region of the 225 μm wafer produces higher differential efficiencies than that of the 675 and 450 μm wafers, but at the edge regions this drops significantly. Again, this is correlated with the previously discussed variations in the oxidation extent.

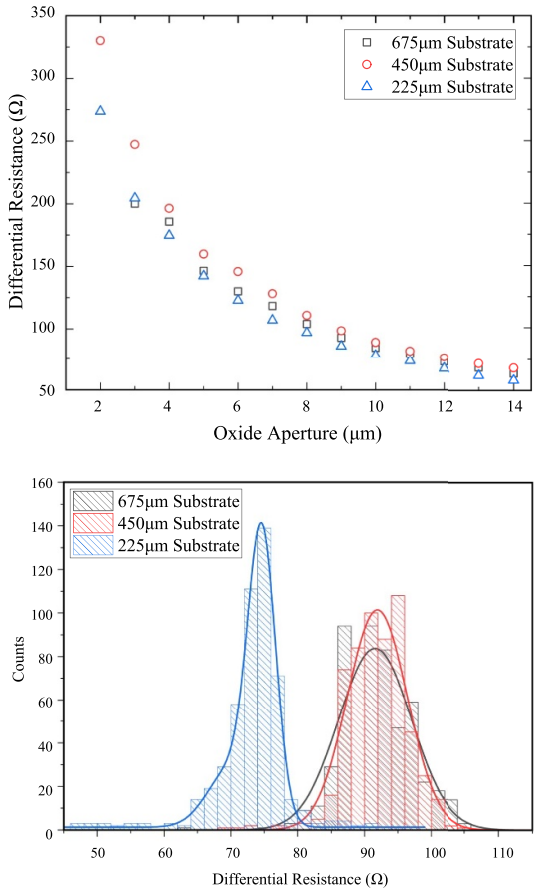

Figure 6. (a) Differential resistance measured between 2.0 and 2.4 V as a function of oxide aperture diameter for devices on 675, 450, and 225 μm substrates. (b) Histogram of differential resistance for 43 μm mesa devices across 6 inch wafer. Histograms are fit with a lognormal distribution (solid lines).

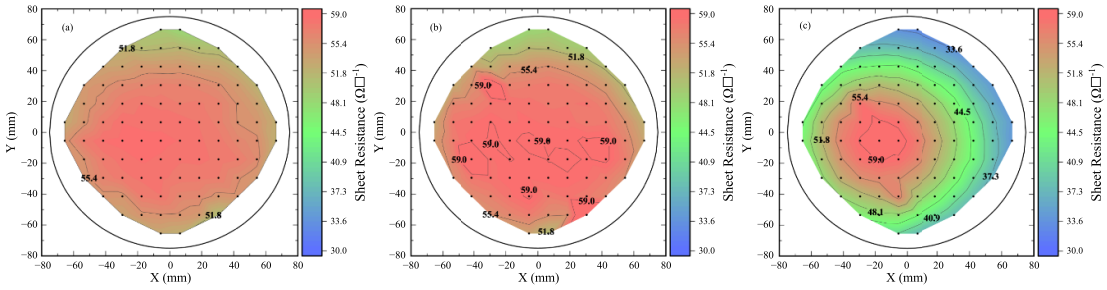

Figure 7. Contour plots of the sheet resistance variation across (a) 675, (b) 450, and (c) 225 μm substrate thickness wafers, extracted from CTLM measurements.

3.4. Peak wavelength

We also consider the peak lasing wavelengths of devices produced on each wafer. The lasing wavelengths at 5 mA for 49 μm ($\sim$14 μm aperture) devices are mapped across the wafers and histograms showing the distributions of each is shown in figure 10. Larger aperture devices are chosen so that the aperture-dependent confinement effects are minimised. From the Gaussian fits, the mean wavelengths are 935.8, 935.1, and 936.8 nm and the variances 4.0, 12.2, and 7.8 nm for the 675, 450 and 225 μm wafers, respectively. The spatial variation for each wafer is shown in figure 11. For the 675 and 450 μm wafers, there is a typical radial distribution with longer wavelengths in the centre, decreasing towards the edge. This is the result of typical MOVPE growth rate variation for a rotating wafer. There is a significant centre-to-edge variation for the 450 μm wafer, which results in the elongated tailed distribution and high variance. The 225 μm wafer also shows longer lasing wavelengths at the centre, however, again at the top and bottom right edge, there is a region that diverges from the trends of the 675 and 450 μm wafers, this time red shifting the emission to a similar value to that of the centre. The redshift is indicative of an increased optical path length in the optical

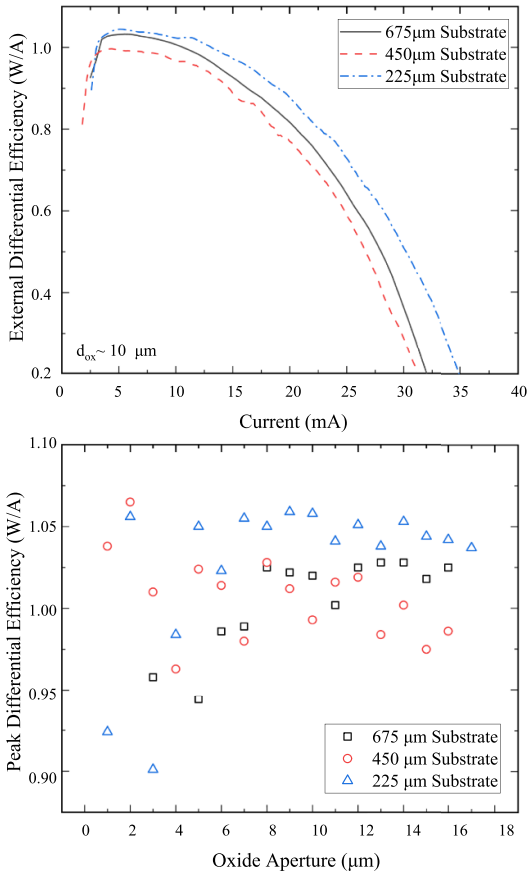

Figure 8. (a) External differential efficiency as a function of bias current for single ∼10 μm oxide aperture diameter devices on 675, 450, and 225 μm substrates respectively. (b) Peak external differential efficiency as a function of oxide aperture diameter devices on 675, 450, and 225 μm substrates.

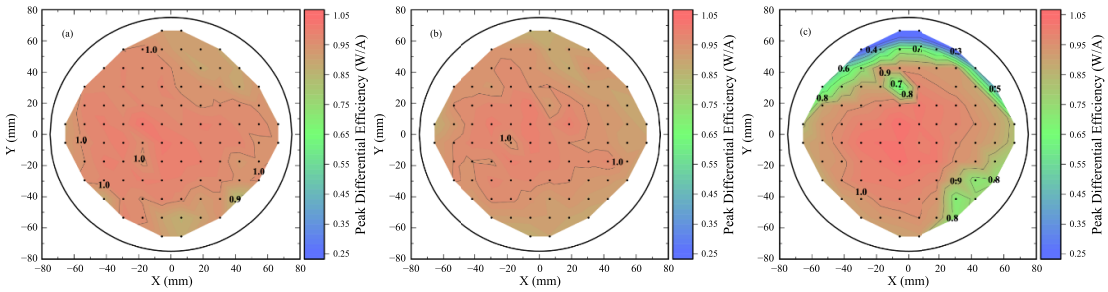

Figure 9. Contour plots of the peak external differential efficiency of 43 μm mesa diameter VCSELs across (a) 675, (b) 450, and (c) 225 μm thick Ge substrate wafers. The regions of low differential efficiency at the top and right edge of the 225 μm wafer corresponds to regions of slow (short) oxidation.

cavity of the stack. In general, we do not observe a significant shift in emission wavelength for the 450 and 225 μm wafers with respect to the 675 μm, however, we do find more prominent wafer-scale variations.

3.5. Temperature dependence

The temperature dependence of J_{th} was measured for individual devices at the centre of the wafer, with∼10 μm diameter oxide apertures, for each substrate thickness, and this is shown in figure 12. From a polynomial fit, the temperature of the minima in threshold current density, T_{min}, which occurs when the gain peak and cavity mode wavelengths align, is found to be 50.0, 52.5, and 56.0 °C for the 675, 450, and 225 μm wafers, respectively. This corresponds to a room temperature gain peak—cavity mode wavelength detuning of 1.8, 1.9, and 2.2 nm. With minimal difference in the detuning between the wafers, we do not attribute this to be a significant driver for the increased J_{th} of the 225 μm wafer devices. We observe an offset in the minimum achievable threshold current density, $J_{th,min}$, which is independent of the alignment of the

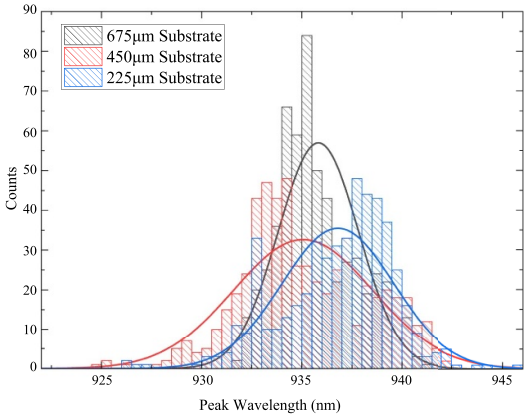

Figure 10. Histogram of peak emission wavelength for 49 μm mesa diameter VCSELs across wafers of 675, 450, and 225 μm substrate thicknesses.

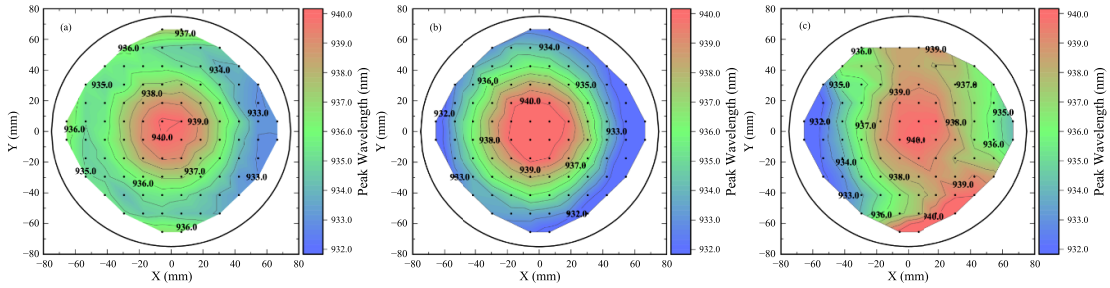

Figure 11. Contour plots showing the variation of the peak emission wavelength of 49 μm mesa diameter VCSELs, at 5 mA, across 675 (a), 450 (b), and 225 (c) μm thick Ge substrate wafers.

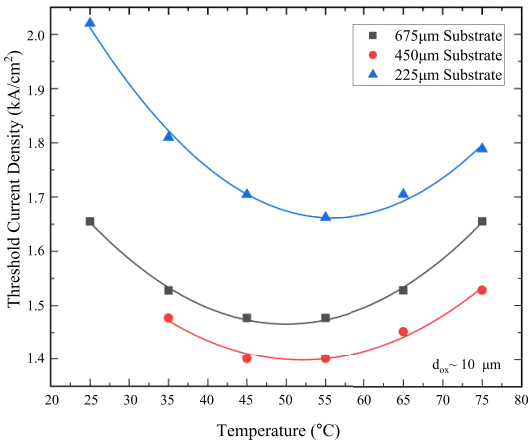

Figure 12. Threshold current density as a function of temperature (data points), between 25 and 75 °C with a polynomial fit (solid line) for each wafer.

gain spectrum with the cavity mode, and this is in line with those made in section 3.1, that is, with the 225 μm wafer producing devices with the highest threshold requirement.

The temperature dependence of J_{th} results from the different temperature shifts of the gain spectrum and the cavity mode wavelength. We also consider the temperature-dependence of the optical power, measured up to thermal rollover, and raw curves are plotted in figure 13 for each substrate thickness. All three substrates show a reduction in power output with an increase in temperature. At 25 °C, the peak optical power is highest for the 225 μm substrate device, at around 33 mW (figure 13(c)), this is consistent with the increased differential efficiency also observed on the 225 μm wafer.

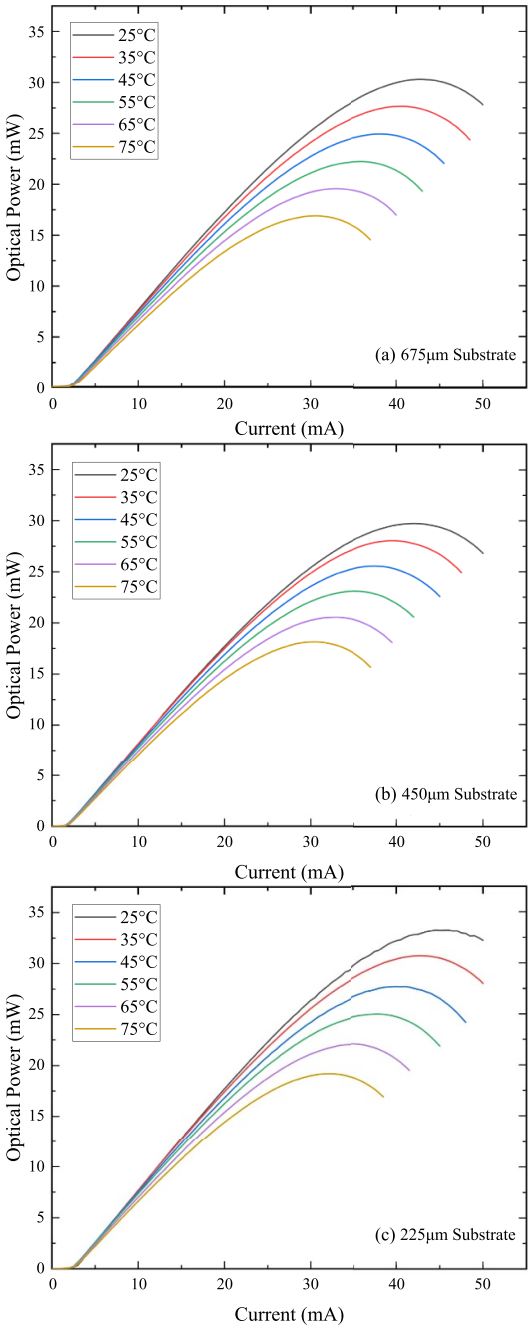

Figure 13. Temperature dependent *P–I* measurements of a single ∼10 μm oxide aperture device, from the centre of the wafer, on (a) 675, (b) 450 and (c) 225 μm thick Ge substrate wafer.

In comparison, both the 675 and 450 μm substrate devices, figures 13(a) and (b) respectively, show similar performance, with an output power of around 29 mW. This difference remains consistent with increasing temperature, up to 75 °C.

3.6. Discussion

Here, we discuss the implications of the experimental data presented in sections 3.1–3.6. To further understand the wafer-scale variations, we correlated the device performance data with measured bow/warp of each wafer using the autofocus function on a maskless lithography tool. The measured surface height variation of the 225 μm wafer shows a sharp increase in the warp at the top and right-hand edges of the wafer. These peaks correspond to regions on the wafer with longer Fabry-Pérot cavity mode wavelengths and variations in oxidation rates. Even with growth conditions optimised for the thinnest substrates used in this study, temperature fluctuations at these points are likely to affect composition, layer thicknesses, and/or doping incorporation. It is unclear whether the height fluctuations are as pronounced pre-growth or caused by the growth itself. Additionally, comparison to pre-processing reflectance measurements shows a similar

trend in the extracted Fabry-Pérot cavity mode wavelength which also coincides with a large peak in surface height variation. On the other hand, the maximum surface height variation for the 675 μm wafer was found to be greater than that of the 225 μm wafer. The key difference is that the change in height is gradual for the 675 μm wafer, increasing approximately linearly when moving from the top to the bottom edge of the wafer. Despite this, the wafer-scale variation in device performance is not correlated with the surface height variation for the 675 μm wafer. This would suggest that is a combination of multiple factors (thermal properties of the substrate, relative prominence of bow/warp peaks) that drives fluctuations in the properties of epitaxial layers, which ultimately leads to the non-uniformity in device performance observed for the 225 μm wafer. Conversely, the warp of the 450 μm wafer is negligible in comparison to both the 225 and 675 μm wafers.

A definite cause of the increased J_{th} for the 225 μm wafer is unclear, however, substrate temperature variations, likely to occur during growth across different Ge thicknesses, may lead to variations in material composition, layer thickness, and doping incorporation in the DBR layers. Any impact on the mirror reflectivity will have a significant effect on the threshold gain requirement. Available growth data indicates that the 225 μm wafer has a lower stopband height compared to the other two wafers, furthering the idea that a lower reflectivity (higher mirror loss) is a cause of the higher J_{th}. This is also consistent with the slight increase in the external differential efficiency observed and the higher optical powers of devices produced on the 225 μm wafer. The reduced differential resistance and sheet resistance, suggests an increased doping incorporation in the p-DBR, which would increase the rate of free carrier absorption and increase the internal optical losses.

Irrespective of that, successful growth is demonstrated on 150 mm 450 μm Ge substrates, producing high-performance devices comparable to that of a standard substrate thickness and with comparable distributions across the wafer. We demonstrate that a 450 μm Ge substrate can work as a drop-in replacement for our previously-qualified 675 μm (150 mm diameter) Ge substrates, thus reducing the required substrate material by one third. Moreover, although wafers of 225 μm thickness do not provide devices of identical performance and with identical wafer-scale uniformities, some promise is shown for the future. Large regions of the wafer produced devices with comparable performance to that of a standard substrate thickness, which, with further optimisation may yet yield improvements whilst requiring only a third of the substrate material.

4. Conclusion

In summary, the successful growth, fabrication, and characterisation of 450 and 225 μm thick Ge substrates over 150 mm diameter wafers has been demonstrated. This is the first of its kind for a AlGaAs-based VCSEL structure on 225 μm thick Ge. Comparable performance of both 675 and 450 μm thick substrate wafers has been shown across performance metrics including threshold current density, differential resistance, peak differential efficiency and peak wavelength, highlighting its suitability as a drop-in replacement if a thinner substrate is required. Devices across 225 μm thick wafers show an increase in J_{th} of $\sim$0.3 kA cm^{-2} compared to the other two, as well as a decrease in differential resistance. Comparison to available photoluminescence growth data suggests this is due to compositional and thickness changes, likely caused by differences in substrate temperatures during growth. More work is required to investigate growth of VCSEL structures on 225 μm thick Ge, but some promise is shown for reducing cost and waste of the end product.

Data availability statement

The data that support the findings of this study are openly available at the following URL/DOI: https://doi.org/10.17035/cardiff.28755134.

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Device fabrication was carried out in the Institute for Compound Semiconductors (ICS) at Cardiff University.

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