A Hybrid electron beam lithography approach to wafer scale up of 150 mm InP ridge lasers

Tomas Peach, Ben Salmond, Tyrone Jones, Elizabeth Beaumont, Stuart Thomas, Angela Sobiesierski, and Samuel Shutts

***Abstract*—The utilization of electron beam lithography (EBL) as a wafer scale technique for the fabrication of compound semiconductor devices provides unique challenges in terms of both application and throughput. We report on wafer scale EBL in the context of fabricating edge emitting lasers on 150 mm indium phosphide (InP) substrates. A hybrid electro-optical lithography process is used to pattern typical ridge waveguide (RWG) laser structures, while overcoming some of the practical challenges associated with fabricating these devices on large wafer platforms. This technique is demonstrated to reduce patterning times by up to a factor of 20 compared to conventional EBL processes. Moreover, we motivate the application of hybrid lithography by considering the loading effect of etching 150 mm InP wafers and the benefit of transitioning to a 'low open area' mask geometry.**

***Index Terms*—Electron beam lithography, 150 mm wafer processing, InP.**

I. Introduction

ELECTRON beam lithography is a powerful technique which has vast applications in the fabrication of complex semiconductor device architectures. This spans numerous material platforms, and multiple scientific disciplines [2], [3]. One such application is compound semiconductor (CS) optoelectronics where EBL is often used to realize novel devices such as ridge waveguide (RWG) lasers or optical amplifiers [4], photonic crystals [5], [6] and grating coupled devices [7]–[9]. Due to the serial nature of focused electron beam exposure, EBL is often considered a slow process technique which usually requires relatively long writing times [10]. This is not a inhibitor for an academic or development environment because sample materials, and therefore patterning areas, are generally quite small which makes the slow writing speeds more manageable. However, it does pose a challenge when scaling up to wafer level processing. In the mass production of semiconductor devices, e.g. the complementary metal-oxide-semiconductor (CMOS) industry, this challenge has been overcome via the utilization of deep ultraviolet (DUV) and extreme ultraviolet (EUV) lithography [11]. However, the current throughput requirements of CS is significantly less than CMOS, and therefore does not justify the vast expense of adaptation to these production-scale techniques at this time. This means EBL is still the foremost technique for fabricating nanoscale devices on this material platform.

In recent times, the increased demand for fast data communication platforms, and the subsequent growth of the technologies that underpin them, has led to a significant scale up in the production of compound semiconductor optoelectronic devices. One of the foremost motivators for this growth is the evolution of the photonic integrated circuit (PIC) within which InP photonics has been positioned as a key contributor [12], [13]. As a result, a significant effort has been made to scale up the manufacture of InP substrates, including the now commercial availability of photonics grade 150 mm wafers and development of wafer scale III-V quaternary epitaxy [14]. Therefore, the ability to fabricate high quality InP photonic device architectures on larger wafers is becoming increasingly valuable. One key device architecture in InP optoelectronics is the RWG edge emitting laser [15]. Indium phosphide RWG lasers, operating in the O- and C-band wavelength range (1.3 μm and 1.55 μm respectively) [16], [17], have been crucial for the commercialization of broadband telecommunication technologies and have, until now, been limited to fabrication using 75 mm and 100 mm wafers. The performance of these devices is very well understood which therefore positions them as the natural choice for the initial qualification of new 150 mm InP material. For reliable device operation, there are several strict fabrication requirements for a RWG laser, such as well defined device dimensions and straight sidewall profiles [18], which has positioned EBL as a commonly used technique.

In addition to the increased exposure times of EBL, one of the key challenges to scaling the fabrication of InP RWG lasers to larger wafer diameters is achieving a uniform etch depth during the ridge definition. This becomes challenging due to the significant increase of material reactants being removed during the dry-etch process to define the waveguide [19], [20]. This loading effect results in a decrease in etch rate that, in turn, contributes to a higher degree of mask degradation and therefore a reduction of sidewall quality and profile. Furthermore, achieving a well-defined and uniform etch stopping position becomes more challenging as the longer runtime amplifies the inherent etch process non-uniformities. One solution to combat these challenges is to reduce the amount of the wafer surface area that is exposed to the etch chemistry during the ridge definition. This can be achieved by switching to using a 'low open area' (LOA) trench-based architecture in the device mask design. However, this then poses a challenge to the process compatibility of EBL.

T. Peach (email: peacht@cardiff.ac.uk), T. Jones, E. Beaumont, S. Thomas and A. Sobiesierski are affiliated with the Institute for Compound Semiconductors, Cardiff University. B. Salmond and S. Shutts are affiliated with the School of Physics and Astronomy, Cardiff University. This work is a highlight paper from CS-MANTECH 2025 [1]

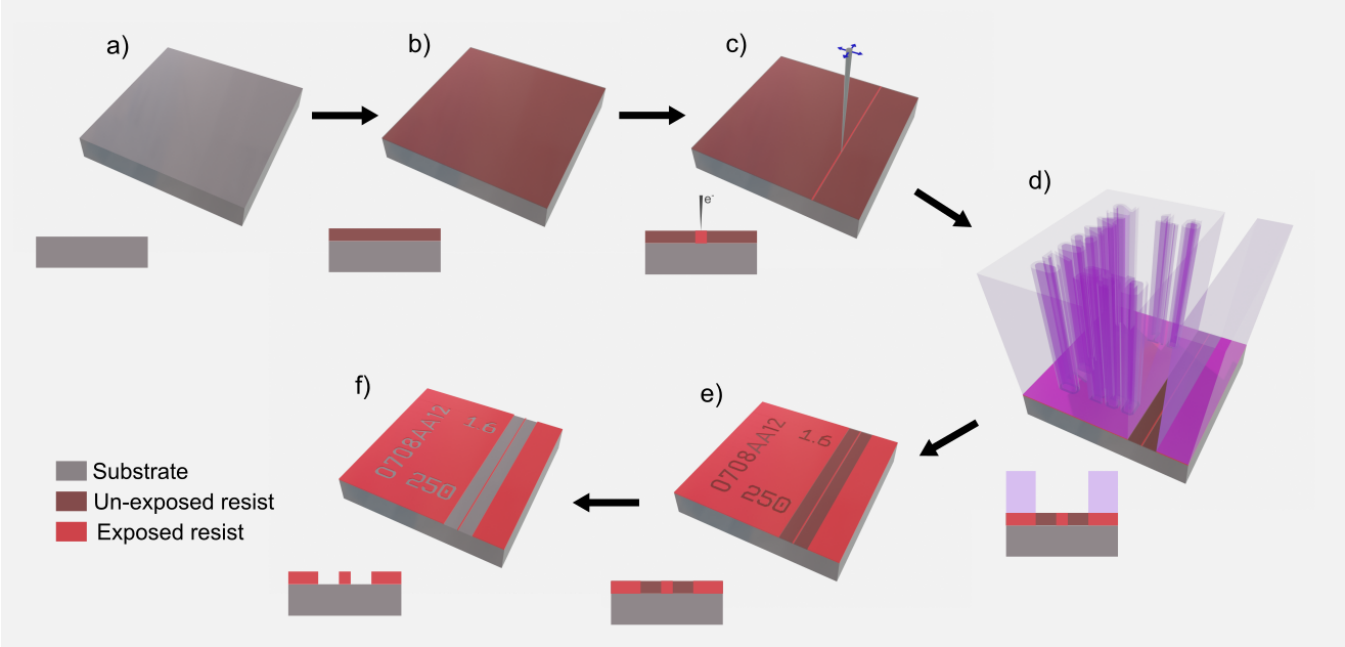

Fig. 1. Schematic illustration of hybrid electro-optical lithography process. a) Substrate b) Resist deposited on wafer. c) EBL exposure of high-resolution RWG features. d) Optical exposure of low-resolution trench features. e-f) Single development step. Also included is cross sectional depiction of each step.

Conventional 'high open area' (HOA) ridge patterning would involve using a negative tone resist and only exposing the area where the ridge is to be defined. The obvious approach to converting to a trench geometry would involve switching to a positive resist and exposing the trench while leaving the central ridge un-exposed. This would lead to an approximate increase in patterning area of a factor of 10, depending on ridge/trench widths. An alternative approach to achieve this could be to use multiple lithography and mask etch steps, however this will also lead to an increase in process time and complexity. It would therefore be valuable to establish a single layer lithography process to pattern these structures such that the key attributes of EBL are maintained, but without significantly hindering potential throughput. In this work, an electro-optical hybrid lithography process is presented with a view to provide a wafer scale InP ridge/trench etch mask within a reasonable processing window [1]. Hybrid "mix and match" lithography was first reported in the field of CMOS manufacturing [21], [22] and is still an active area of process development today [23]. All fabrication work in this study has been performed at the Institute for Compound Semiconductors (ICS) at Cardiff University. EBL was achieved at 100 kV using a Raith EBPG5200plus system. Maskless optical lithography was performed using a Heidelberg MLA150.

II. Fabrication

We use a single negative resist layer (AZ® nLOF™ 2000) and a hybrid electro-optical exposure process to achieve high-quality ridge/trench geometries, on 150 mm InP wafers. Other resists are theoretically possible, provided that they have suitable electron beam and optical sensitivities. Prior to lithography, a dielectric layer is first deposited onto the wafer to act as a hard mask during the semiconductor etch process. Figure 1 displays a process flow of the hybrid process. Resist is first spun onto the wafer at an appropriate thickness to pair to the hard mask, and to allow for the desired feature resolution and pattern transfer. The wafer is then exposed using a 100kV electron beam to define the high resolution device structures. For this simple RWG application, resist is spun to a nominal thickness of 1.5 μm however we have tested different resist dilutions to achieve films down to 200nm. Thinner resists allow for higher resolution patterning due to a reduction in electron forward scattering. We find that it is possible to achieve $\simeq$ 300 nm pattern resolution at a resist thickness of 1.5 μm and $<$ 100 nm at a thickness of approximately 500 nm. The high aspect ratio profiles that are achievable with this resist process are extremely useful for definition of various device architectures within optoelectronics. In the immediate context of this work, EBL is used to pattern the linear RWG structures which typically range from 1 μm to 2 μm in diameter. While these dimensions are typically within the capability of conventional optical lithography systems, we find that EBL allows for a significantly greater control over resist sidewall angle, line edge roughness, and nanoscale uniformity of critical dimensions. Furthermore, EBL allows for the integration of more complex nanoscale device architectures such as Bragg gratings. At a resist thickness of 1.5 μm, a dose of 80 μCcm^{-2} is used to resolve the RWG structures. The beam current for this exposure was set to be 10 nA with a step size of 10 nm.

Immediately after EBL, the wafer is then loaded into the MLA150 for optical exposure whereby the trench geometry, and any other non-process-critical features are defined. This includes process control structures and devices labels. The MLA150 uses an 8 W, 375 nm laser to project the pattern directly onto the resist without the requirement of a pho-

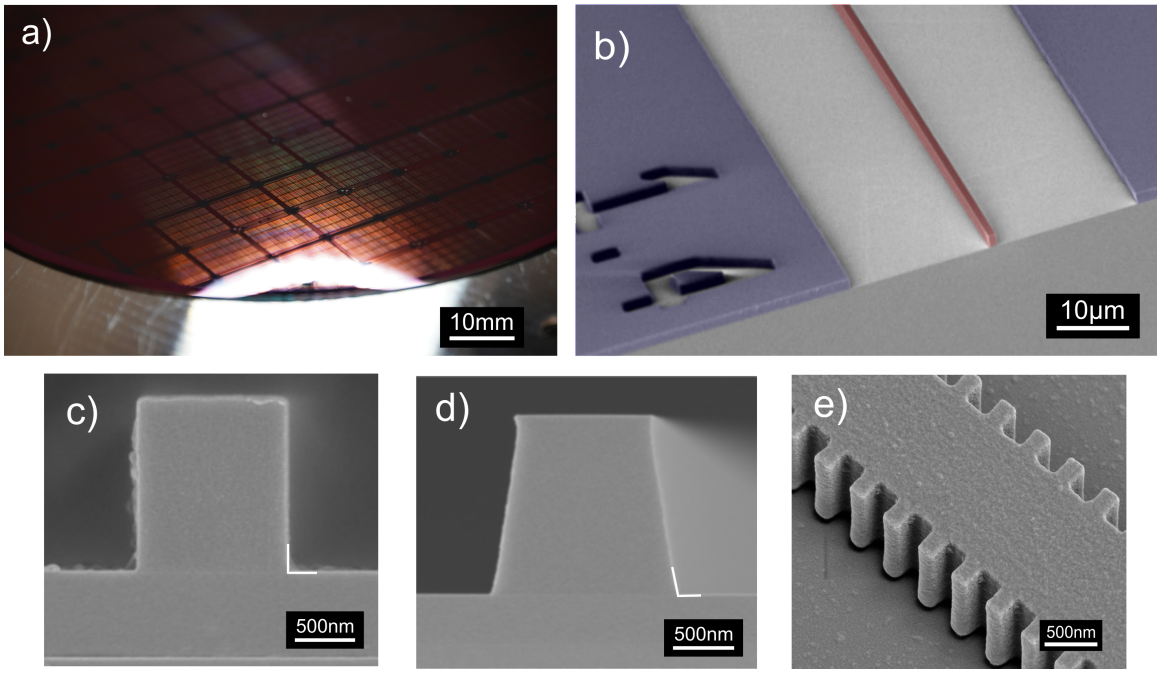

Fig. 2. a) 150 mm InP wafer patterned using hybrid lithography process. b) Image of ridge (red) and trench (blue) geometries. c) Cross section of typical EBL RWG resist profile, indicated sidewall angle is 90 °. d) Cross section of typical optical lithography RWG resist profile, indicated sidewall angle is 83 °. e) An example SEM image of a 3rd order DFB resist mask patterned using hybrid lithography.

tomask. After the second exposure, the resist is then developed in a single step where both EBL and optical features are resolved simultaneously. It is therefore crucial to correctly balance the exposure doses of each lithography system to achieve the desired feature resolution. Typical structure resist sidewall angles are found to be 90 degrees (Figure 2c), which is essential for high quality ridge definition. For the sake of comparison, an identical ridge defined solely by optical lithography is displayed in figure 2d, with a side wall angle of 83 degrees. Alignment between the two exposures is achieved using temporary contrast alignment markers that are exposed during the EBL step and identifiable during the optical lithography process. This therefore necessitates the EBL process preceding the optical exposure however, if the sample has pre-existing alignment fiducials, then the exposures can happen in either order. In both cases the alignment accuracy is found to be better than 500 nm which is the standard operational limit of the MLA150 system. The wafer is then passed on to etch and subsequent device processing steps. Figure 2e) includes an example SEM image of a typical 3rd order DFB ridge architecture to demonstrate the application of hybrid electron beam lithography in high resolution nanoscale patterning. Naturally, increasing the pattern complexity of the high resolution EBL step will result in longer exposure times however the comparative benefit of the hybrid process remains the same.

To validate the effectiveness of the hybrid process, we compare the cumulative exposure time of the two lithography steps with a conventional approach using a positive resist EBL and an inverted pattern design. Here we assume a sensitivity of 300 μCcm^{-2} which is typical of a resist of this nature. The results of this comparison are displayed in table I. For completeness we also include the HOA negative EBL resist process. Schematic representations of each exposure regime are displayed in figure 3. For the sake of comparison, we have assumed an identical mask design across the three exposures. This includes process control structures and device labels. The total exposure time of the hybrid lithography is slightly over 2 hours, whereas the equivalent positive resist exposure exceeds 30 hours. Therefore the implementation of hybrid lithography has reduced the total exposure time by a factor of 15.

TABLE I
A COMPARISON OF THE PATTERN AREAS AND EXPOSURE CONDITIONS FOR THE HYBRID (LOA), POSITIVE EBL (LOA) AND NEGATIVE EBL (HOA) LITHOGRAPHY PROCESSES.

	Negative Hybrid		Positive	Negative
	EBL	Optical	EBL	EBL
Pattern Area (%)	0.42	82.32	17.26	2.34
Exposure Dose (Various)	80 (μCcm^{-2})	200 (mJcm^{-2})	300 (μCcm^{-2})	80 (μCcm^{-2})
Exposure Time (hh:mm)	01:24	0:44	30:48	06:35

Naturally, the removal of non critical structures from the positive resist mask layout, such as device labels, would decrease the overall exposure time however these structures would then need to be defined at a later stage in the processing. Additionally, the exposure time could be brought further down by reducing the widths of the trench itself. This would need to be carefully considered as it could have an effect on the subsequent device processing steps. Removal of device labels,

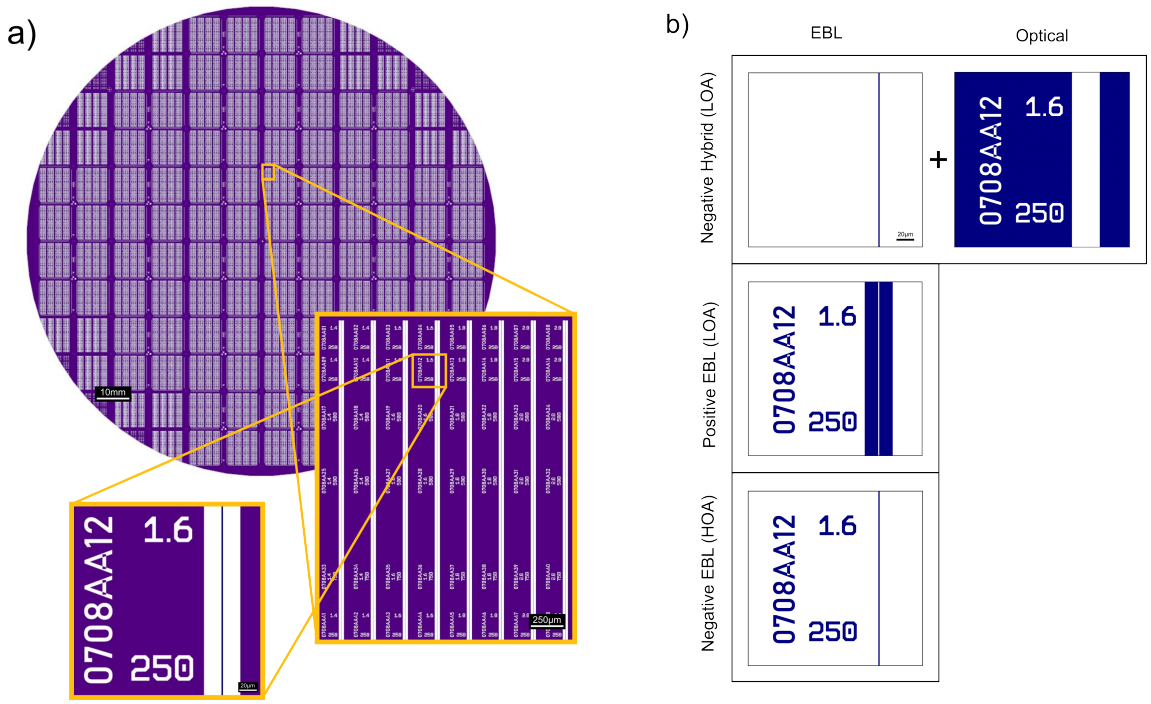

Fig. 3. a) A schematic mask layout for a full 150 mm InP wafer RWG design. Device ridge widths vary from 1.4 μm to 2.0 μm and cavity lengths from 250 μm to 1 mm. b) Exposure layouts for the hybrid (LOA), positive EBL (LOA) and negative EBL (HOA) lithography processes. Blue patterned shapes correlate to exposed areas. A device with 1.6 μm width, 250 μm cavity length is used as an example.

and various reductions of the trench width have been simulated resulting in optimised exposure times ranging from 15 to 20 hours which remains significantly longer than the hybrid exposure. It is also worth commenting that the "Negative EBL" example presented in table I also includes labels and process control structures. This is the main point of difference with the Hybrid EBL step, and the primary contributor to the much greater exposure time. It would naturally be possible to increase the beam current and step size for these features however the utilisation of hybrid lithography would be significantly more efficient for patterning device labels. While this is certainly not device critical, it is quite convenient to identify devices at this stage of the process flow, particularly in a development environment where in-line testing can be crucial. The presented hybrid lithography process time could be further reduced by using a contact aligner as the optical exposure tool rather than a mask-less projection system. However, the flexibility of mask-less optical projection is quite beneficial for a development environment. In addition, a higher level of current and pattern optimisation in the EBL process is also possible to further reduce exposure times.

While the time benefit is clear, the further effectiveness of this technique is inherently linked to the process benefits of reducing the open area amount of the InP semiconductor etch. As such, a comparison of HOA and LOA wafer etches has also been included in this study. Here, we process two identical 150 mm InP wafers, each with a 500 nm thick dielectric hard-mask. For both wafers, RWG laser structures are identically patterned using the EBPG (1c). The LOA wafer is then exposed for a second time using the hybrid technique to mask off a larger percentage of the wafer area (1d). The total amount of open area to be etched in the HOA wafer is 97.66 % whereas LOA is 17.26 %.Therefore, there is a total reduction of over 80 % of the material surface. Both wafers are then identically etched, first to define the dielectric hard-mask and then to etch the InP. After the semiconductor etch, the remaining dielectric is removed. Both materials are etched in an Oxford Instruments PlasmaPro Cobra 300 ICP using fluorine and chlorine chemistry respectively. In a RWG laser device fabrication, the stopping depth would be determined by targeting a specific epitaxial layer within the material heterostructure. This would usually be monitored in-situ using an endpoint technique, to determine etch time. However, for this study, InP substrate wafers were used so there are no specific layers to target. Therefore, both wafers were etched for an identical process time of 330 seconds in an effort to directly compare how the etch rate of the InP is affected by open area amount. This duration was selected to target an approximate etch depth of between 1-2 μm. This would be typical of etching down to the active layer of a shallow-etched ridge laser. For both wafers, etched ridges were characterised using a scanning electron microscope and stylus profilometer to measure widths and etch depths respectively.

III. Results

Comparative etch characteristics between the HOA and LOA wafers are displayed in Table II. As expected, increasing the amount of open area has the effect of significantly reducing the material etch rate. This is such that, after 330 s of etching, the final average RWG depth across the LOA wafer is almost twice that of the HOA equivalent. This can be explained by a saturation of the reactive interaction between the ICP process

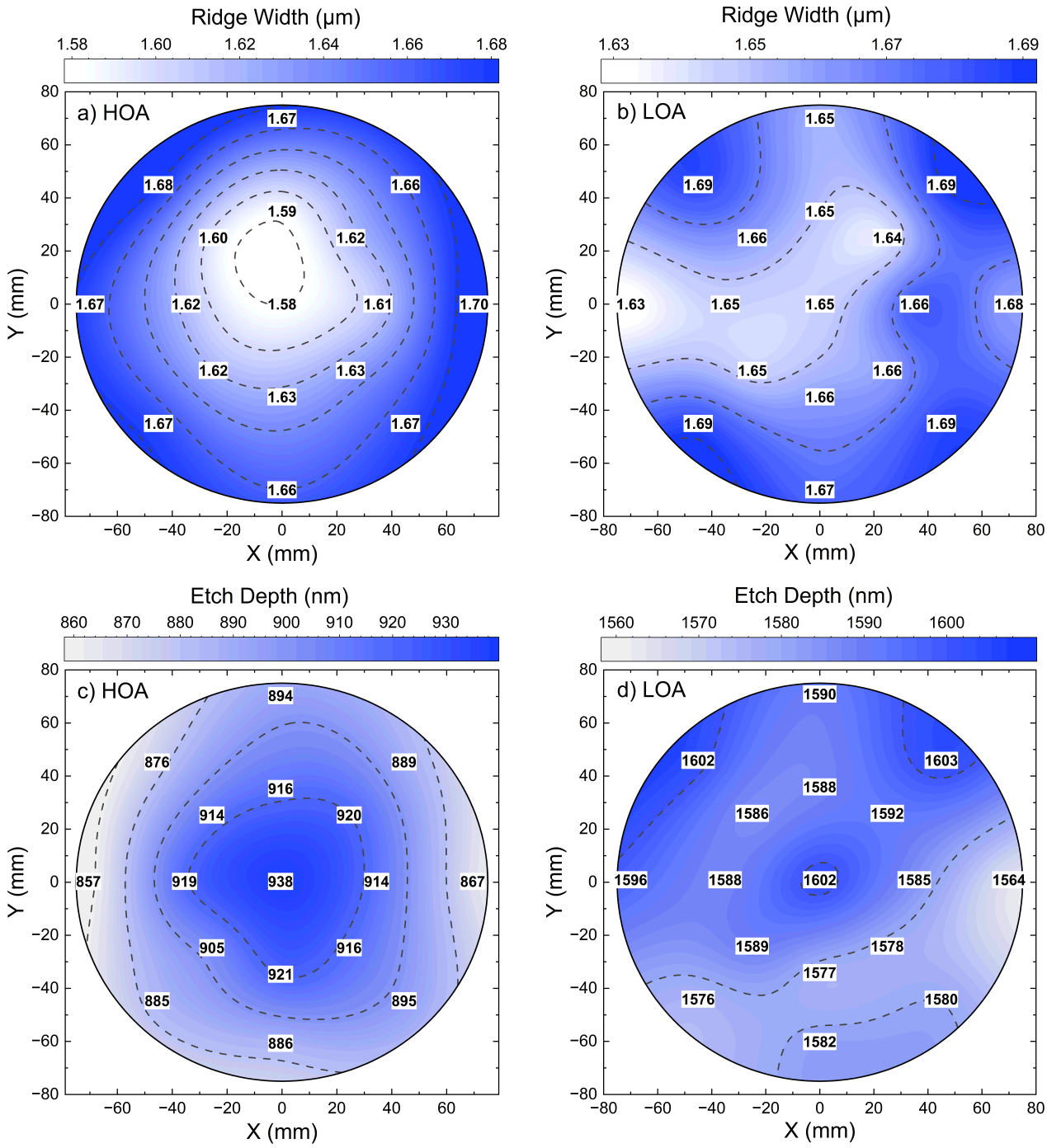

Fig. 4. a & b) 17-point, 150 mm maps of etched RWG width uniformity for HOA and LOA (hybrid) wafers, as indicated. c & d) 17-point, 150 mm maps of RWG etch depth uniformity for HOA and LOA (hybrid) wafers, as indicated. Measurement points are indicated as solid circles and dashed contoured lines correspond to variations of 20nm.

chemistry and the material being removed due to the much larger open surface area. While this decrease in etch rate is not necessarily a problem in a small-scale development cleanroom, it could be critical in a manufacturing environment. In additon to the data presented in table II, figure 4 displays 17-point uniformity maps of the etched InP RWG structures for both wafers. a & b) compare the uniformity of ridge widths whereas c & d) compare etch depths. For the LOA wafer b) we find a mean width of 1.660 $\pm$0.004 μm, a uniformity of 1.8% and 3σ value of 53.7nm. 3σ is defined as the statistical range within which 99.7 % of a given normal data set would lie, i.e. 3 times the standard deviation (σ) from the mean. Therefore, in this context it is used to quantify the total variance in fabricated RWG widths across a 150 mm InP wafer. Measurements were taken using scanning electron microscope images of patterned ridges, therefore it is possible that some variance in measured linewidth is caused by the limitations in inspection methodology. For example, we were

TABLE II
A COMPARISON OF VARIOUS ETCH PROPERTIES FOR THE HIGH-OPEN-AREA AND LOW-OPEN-AREA WAFERS.

	HOA	LOA
Etched Area (%)	97.66	17.26
Average Etch Depth* (nm)	900±6	1587±3
Etch Rate (nm/min)	164±1	288.5±0.5
Etch Rate Standard Deviation (nm/min)	4.1	1.9
Etch Depth Uniformity (%)	4.7	1.2

* After 300 seconds of etching

unable to accurately measure the uniformity of the resist mask for either wafer do to the variances in line width being beyond the resolvable limits of the microscope. However, we did not observe any significant difference in patterned widths between HOA and LOA wafers. We therefore attribute the variation in ridge width, to the etching processes which could result from both the mask opening and semiconductor etches. InP etch processes were not specifically optimised to favour either HOA or LOA wafer layouts. By comparison, the HOA wafer RWGs has a mean width of 1.638 ±0.004 μm, a uniformity of 3.5 % and 3σ value of 107.3 nm. The target design ridge width for both wafers was 1.6 μm. It is clear that there is a greater variance in ridge widths in the HOA wafer which is likely linked to the overall decrease in etch rate and increase in etch rate non-uniformity and associated mask degradation [19]. It is commonplace to apply a corrective bias factor to designed patterns to account for process factors such as etch pattern transfer. Therefore, while there is a greater variance in the HOA wafer, it is trivial to account for this at the design stage. Comparing figure 4 c & d), it is also apparent that the HOA wafer has clear radial distribution in etch depth, from centre to edge, which is not seen to be present in the LOA sample. This distibution is also consistent with the ridge widths of the same wafer. Radial distributions in etch rate are typical of a ICP wafer process and are often attributed to a combination of plasma density nonuniformies, wafer temperature nonuniformites and additional wafer loading effects. Both wafers were processed in identical ICP conditions therefore it is wholly possible that a radial distribution would be present in the LOA wafer as well, however it may not have been resolved in the profilometer measurement. However what is clear, is that the decrease in etch rate observed in the HOA wafer has exacerbated this distribution. Moreover, increasing the amount of open area has the effect of significantly decreasing the material etch uniformity. This is such that the LOA wafer has a calculated uniformity of 1.2 % whereas the HOA wafer has an equivalent value of 4.7 %. It is likely that the vast increase in material being removed during the HOA wafer etch is significantly changing the properties of the process conditions. It could be possible to alter the recipe in an attempt to optimize for HOA geometries, however using a LOA design removes the need for introducing any additional process complexities.

Using the measured standard deviation in etch rates, it is

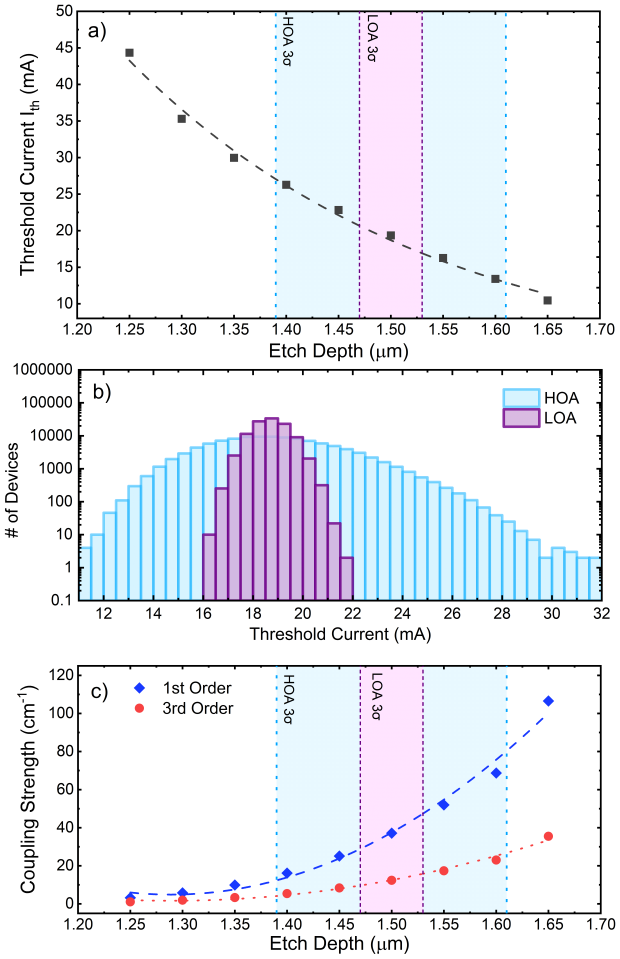

Fig. 5. a) Simulated RWG laser device threshold currents for varying etch depths. 3σ variations for LOA and HOA etches are indicated as shaded regions. b) Histogram showing spread in calculated threshold currents for 100,000 devices based on LOA and HOA wafer etching. c) Simulated coupling strength of typical 1st and 3rd order latteral DFB lasers (blue diamonds and red circles respectively) as a function of etch depth.

possible to estimate what the 3 σ distribution in etch depth would be if both wafers were etched to the same targeted depth. Using the example of a typical shallow etched laser, of 1.5 μm ridge depth, we can calculate that a LOA mask geometry would result in a 3 σ value of 30 nm, and 112 nm for HOA. For the sake of comparison, we have calculated, using Photon Design's PICWave time domain simulation software, what effect these process variances would have on the threshold current (Ith) of a typical InP RWG laser architecture, figure 5. Here we simulate a width of 1.5 μm and cavity length of 500 μm. We see that, a more shallow device etch would result in a higher Ith which would be detrimental to the overall performance of the laser. In addition, using the determined 3 σ values in HOA and LOA etch depths, we can estimate the effect of patterning area on resultant yield in device Ith, figure 5b. This is such that the total spread in Ith for the LOA wafer is predicted to be within only 6 mA whereas for the HOA wafer is greater than 20 mA.

Furthermore, in the context of DFB laser devices, variance

in etch depth can have a significant e ffect o n t he coupling strength between the periodic grating structure and the light mode. An example of this type of device geometry is displayed in figure 2 e). Therefore, we have simulated the effect of RWG etch depth on coupling strength for typical 1st and 3rd order latterly coupled DFB lasers, figure 5 d). 3 σ v alues i n etch depths for the HOA and LOA wafers are included for the sake of comparison. Using this simulated range in coupling strength, and assuming a typical device cavity length of 300 μm, it is possible to calculate the range in coupling coefficient (κL) for the different wafer etch uniformities. This is such that, for a first order DFB laser, the LOA wafer has a calculated κL range of 0.86 to 1.42 whereas the HOA varies from 0.37 to 2.43. A similar trend is also observed in the 3rd order DFB however it is calculated to be more robust to variances in etch depth. A low κL will result in poor single mode stability and low side mode suppression in fabricated DFB lasers and therefore close control over this parameter is critical for laser production.

IV. Conclusion

The now commercial availability of 150 mm photonic quality InP wafers has motivated the scale up of fabrication processes that were previously suited to smaller sample sizes. A key example of this is electron beam lithography, which has many established applications within optoelectronics but has conventional limitations with regards to wafer scale up due to slow writing speeds. In this work, we present a single resist layer hybrid electro-optical lithography process to define conventional InP RWG laser architectures in a significantly reduced timescale. Further motivation for this technique comes when considering the additional process challenges centred around etching large InP wafers. One solution to relieve some of these challenges is to switch to a 'low open area' etch mask design however this will significantly i ncrease the patterning areal of the EBL process step. Hybrid lithography is an ideal solution to this problem as it allows to retain the high resolution patterning of EBL whilst receiving the process benefits o f o ptical l ithography. T his i s s uch t hat a f ull wafer design containing over 100,000 RWG laser structures were patterned using a LOA design in approximately 2 hours. The process benefits o f u sing a L OA e tch m ask h as a lso been demonstrated such that a critical width uniformity of 1.8 % and an etch depth uniformity of 1.2 % has been achieved. By comparison, a 'high open area' mask achieved width and depth uniformities of 3.5 % and 4.7 % respectively. Variances in devices geometries will have a significant e ffect o n end of line device performances which would be inherently problematic for the mass-production of desirably identical laser die. We have demonstrated hybrid lithography specifically in the context of InP optoelectronics however this technique has many other applications in the wider context of the wafer scale up of established device architectures and in other areas of semiconductor fabrication.

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