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Hybrid balanced frequency doubler up-converting from 2.45 to 4.9 GHz using packaged GaN HEMTs and a Moore space-filling coupler design approach

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Research Paper

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Abstract

A hybrid Balanced Frequency Doubler working up-converting from 2.45 to 4.9 GHz using packaged GaN HEMTs and with no amplification stage, was designed and its performance validated with measurements. The design procedure is detailed, including a brief study of the HEMT optimum bias point. Moore space filling curves are used in the design of the input hybrid coupler, to reduce its size at the fundamental frequency. A maximum measured conversion gain of 11.5 dB with a second harmonic output power of 26.3 dBm was obtained, while fundamental and third harmonic suppression exceeds 40 dBc.

Introduction

Frequency multiplication can be achieved using microwave diodes, as varactors [1] and Schottky ones ([2] and [3]), however, with conversion losses. On the other hand, the use of transistors in non-linear regime can provide both frequency multiplication and conversion gain [4].

Balanced circuit topologies are often used in active microwave circuits due to the advantages in performance they present, e.g. enhancing the RF output power (P_{out}) and matching of an amplifier. In active frequency multiplier design, transistor-based balanced frequency doublers (BFDs) exhibit both higher fundamental signal suppression, crucial to attenuate this powerful signal, and higher P_{out} in comparison to the single-ended (SE) architecture.

Recent works that present active frequency doublers (FD) using different transistor technologies and working at different frequency bands have been studied. Some active doublers working at MW and millimeter wave bands found in the literature use Si CMOS [5], InP HBT [6] or Si RFSOI ADNFET [7] transistors, among others. In the case of [5], nonlinear transmission lines are used to generate the second harmonic, and a distributed power amplifier (PA) is added to obtain conversion gain. Regarding [6], the novelty of the presented FD resides in the Marchand balun used at its input, that present low losses and low imbalances, required for a high fundamental signal suppression. A push-push doubler is proposed in [7], that adds a differential PA at its output. Some common features of these circuits are the use of PAs and the wide bandwidth they present. Another push-push FD working at lower frequencies (input $f_0 = 15$ GHz) is presented in [8], where GaN/SiC HEMTs are used. It also uses a Marchand balun and, in this case, conversion gain is achieved without the use of an amplifier.

Regarding hybrid SE FDs working at closer frequencies to that used in this work, we found [9] and [10]. The doubler in [9] ($f_0 = 4.65 - 4.95$ GHz) includes a low-pass filter (LPF) at the input, to select the fundamental signal, and a band-pass filter (BPF) at the output, to reject the fundamental and harmonics signals above the 2nd. It presents losses in the operating bandwidth, however, the fundamental rejection is around 47 dBc. In [10] two doublers are presented. One using a SiC MESFET working at input $f_0 = 2$ GHz and another using a GaN HEMT at $f_0 = 3.33$ GHz. Although the transistors are different, the design procedure is similar. No bias networks are included in the design and in addition to the input and output matching networks, reflector stubs at $2f_0$ at the input, and at f_0 at the output, are presented.

Most of the published research works on the design of high frequency BFDs are related to GaAs-based MMIC technology. Regarding broadband BFDs using this semiconductor, in [11] (input $f_0 = 6-11$ GHz) and [12] (input $f_0 = 3-23$ GHz), power amplifier stages are required to

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Table 1. Comparison of the state-of-the-art FDs working in similar frequency bands.

Ref.	Technology	Topology	Input f_0 [GHz]	Max G_{c2f_0} [dB]	Pout [dBm] (@max G_{c2f_0})	Min f_0 suppression [dBc]
[9]	GaAs MESFET (CFY25-20P) Hybrid MIC	SE FD + LPF (in) + BPF (out)	4.65 - 4.95	-4.29	-2.29	47
[10] (1)	SiC MESFET (CRF2410-10W) Hybrid MIC	SE FD (no bias networks) + $2f_0$ reflec. (in)+ f_0 reflec. (out)	2	10	≈ 30	39.5
[10] (2)	GaN HEMT (CGH40010-10W) Hybrid MIC	SE FD (no bias networks) + $2f_0$ reflec. (in)+ f_0 reflec. (out)	3.33	14.8	≈ 30	36.5
[12]*	GaAs HEMT MMIC	BFD + March. balun + Pre-PA + PA	3 - 23	14	≈ 15	15
[14]	GaAs HEMT MMIC	BFD + Active balun + BPF out	4	-4	-7	25
This Work SE FD	**GaN/SiC HEMT (TGF2799-SM 6W) hybrid MIC**	**SE FD + $2f_0$ reflec. (in)+ f_0 reflec. (out)**	**2.45**	**12.2**	**20.5**	**23.2**
This Work BFD	**GaN/SiC HEMT (TGF2799-SM 6W) hybrid MIC**	**BFD + compact Rat-Race (Moore space-filing curves)**	**2.45**	**11.5**	**26.3**	**40**

*Data including the Pas.

obtain conversion gain, while in [13] (input $f_0 = 15-25$ GHz) the conversion gain is negative, with losses around 5-7 dB. The same happens in [14] (input $f_0 = 4.4$ GHz), where the BFDs conversion losses are around 4 dB. Regarding the input couplers used in these works, a variety of options are presented. In [11] and [13] reduced size rat-race couplers are designed, using in the first case $\frac{\lambda}{8}$ lines and MIM capacitors, and inductors and MIM capacitors in the second case. In [12] a Marchand balun is used and in [14] an active balun.

In the framework of GaN technology, which exhibits higher output power levels and efficiency, two BFDs were found using GaN HEMTs. In [15], one SE FD, one BFD, and a frequency tripler are presented in MMIC technology. In particular, the BFD operates at an input f_0 from 45 to 50 GHz and presents a maximum 2nd harmonic conversion gain (G_{c2f_0}) of 3.8 dB and fundamental signal suppression greater than 55 dBc. In [16], the BFD is used in series with a balanced frequency tripler to build a MMIC sixtupler.

A comparison only of the mentioned doublers at frequencies close to this work is shown in Table 1.

In this work, a hybrid BFD circuit using packaged GaN HEMTs and working at $2f_0 = 4.9$ GHz with no amplification stage, is designed and its performance validated with measurements. This paper extends the BFD research presented on a previous conference paper by the authors [17], in which other FDs were also designed and discussed. In Section 2, the detailed design methodology of the SE FDs that integrate the balanced structure is included, as well as its performance evaluation through the design and measurements of a prototype. Next, in Section 3, the procedure to design the BFD is described, in particular, the design of the input coupler, that presents a compact structure not applied before in this type of circuits. In Section 4, the measured performance of the designed BFD prototype is evaluated and compared with the predictions in simulation. Finally, Section 5 shows a comparison between the SE FD and the BFD, that shows the output power and fundamental signal rejection improvements using the balanced topology.

Single-ended frequency doubler

Initially, a SE FD working at $2f_0 = 4.9$ GHz was designed, in order to use it in the balanced structure. The Qorvo GaN TGF2977-SM transistor was selected due to its bandwidth, gain and power performance. The model provided by Modelithics was used in the ADS simulations.

The first step is to choose the most adequate bias point for this HEMT, enhancing even harmonics generation under nonlinear behavior. Since our goal is to maximize the 2nd harmonic signal in an efficient manner, fundamental signal needs to be suppressed. In the literature, a class B bias point is suggested for FD design. Therefore, a study to find the best bias point was carried out using both simulations and measurements. Several DC gate voltage (V_{GS}) values around class B and input powers (P_{in}) were swept to find the conditions providing the maximum G_{c2f_0}. This conversion gain is the figure of merit optimized in this step, since it will impact both the circuit power added efficiency (PAE) and self-heating, while the power delivered by the GaN HEMT will be doubled using the balanced topology. A higher G_{c2f_0} with enough RF power will avoid the need for a booster amplifier. For these simulations, fundamental load was short-circuited, the perfect load to reject the fundamental signal. In Fig. 1, the G_{c2f_0} contours show that the maximum is achieved at V_{GS}=-3 V and $P_{in} = 10$ dBm. In addition, in Fig. 2, the G_{c4f_0} contours in the same conditions are shown. We can conclude that, in simulation, $V_{GS} = -3.2$ V seems an adequate bias point to design the FD, since a high G_{c2f_0} is obtained, as well as low G_{c4f_0} and high P_{in}, allowing in this case higher 2nd harmonic output power (P_{out2f_0}). A similar study was performed with measurements using an VSA (Vector Signal Analyzer), providing equivalent results.

To design the bias networks (shown in Fig. 8), decoupling capacitors were used to block the DC, and $\frac{\lambda}{4}$ lines with a radial stub (which acts as a short circuit at 2.45 GHz at the input and at 4.9 GHz at the output) to minimize RF losses. In addition, several parallel RC branches are added to filter out low-frequency spurious signals and enhance out-of-band stability. A series resistor in the input is added to further improve stability.

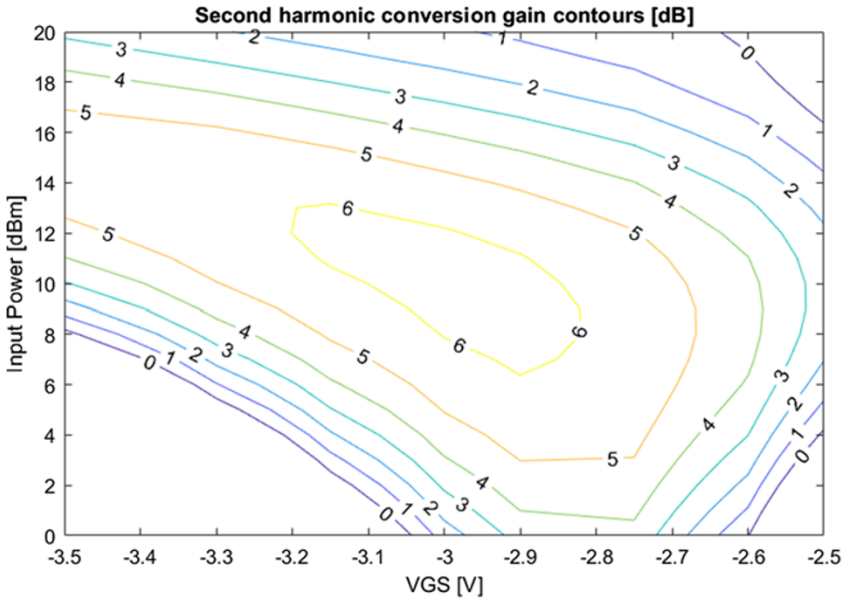

Figure 1. G_{c2f_0} simulated contours sweeping both P_{in} and V_{GS}.

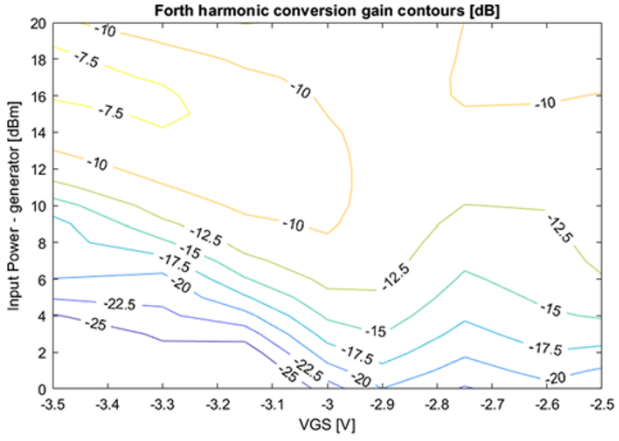

Figure 2. G_{c4f_0} simulated contours sweeping both P_{in} and V_{GS}.

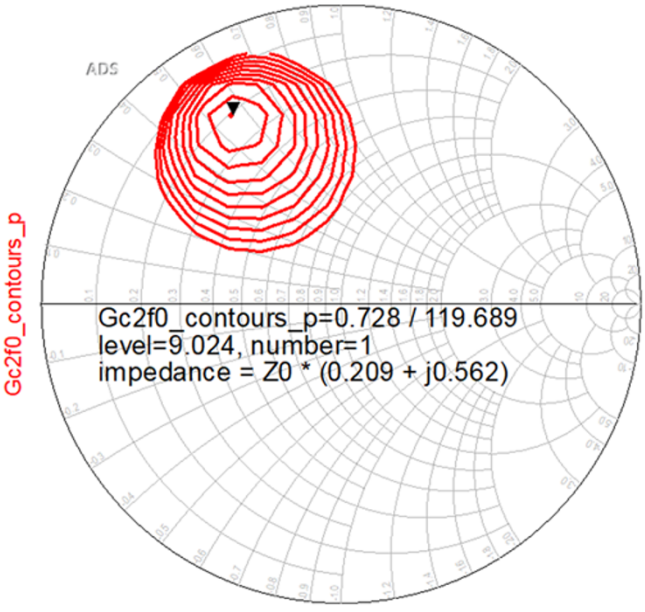

Figure 3. G_{c2f_0} simulated contours obtained at P_{in}=10 dBm with second harmonic LP, showing the impedance that maximizes G_{c2f_0}.

The next step is to find in simulation the second harmonic output impedance (Z_{L2f_0}) that provides, at the chosen P_{in}, the maximum G_{c2f_0} by using 2nd harmonic load-pull (LP), shown in Fig. 3. This impedance, $Z_{L2f_0} = 50(0.209 + 0.562j) = 10.45 + 28.1j$, is the one used to design the output matching network (OMN), shown in Fig. 4. Then, accessing to the transistor intrinsic nodes, available in the Modelithics model, the intrinsic 2nd harmonic FET impedance ($Z^{int}_{L2f_0}$) is computed. This step is crucial since that will be the target impedance in the doubler design. The OMN network includes a single transmission line (TL) resonator to force a high reflective load in Z_{Lf_0} at transistor's drain. We decided to also add another one for Z_{L4f_0}, since the $4f_0$ signal becomes stronger when P_{in} increases, as shown in Fig. 2. No additional suppression is added for the 3^{rd} harmonic, since at the chosen bias point it is relatively small compared to the even harmonics. For matching the Z_{L2f_0}, two $\frac{\lambda}{4}$ TLs, each line with different characteristic impedance, have been added after the drain bias network. That is why part of the drain bias network is also included in Fig. 4. In Fig. 5 it can be seen that this OMN presents 0.65 dB of losses at the 2nd harmonic. The effect of the $\frac{\lambda}{4}$ stubs at f_0 and $4f_0$ can also be seen in the high losses, as well as in the high reflective impedances achieved at these frequencies. Moreover, it is noticeable that there is no need to tune Z_{L3f_0} since the 3^{rd} harmonic is highly suppressed.

At the input, conjugate matching at f_0 is used and a short-circuit for Z_{S2f_0} using a single resonator is added, in order to reflect the 2nd harmonic signal towards the FET input. The extrinsic source impedance is $Z_{Sf_0} = 21 + 20\text{j}\,\Omega$, achieved using a single 20 Ω TL. This network presents the performance shown in Fig. 6, where we can highlight its low losses, that contribute to maintain the G_{c2f_0} values.

Simulation results vs input power for the FD circuit are shown in Fig. 7, where the conversion gains for the fundamental and

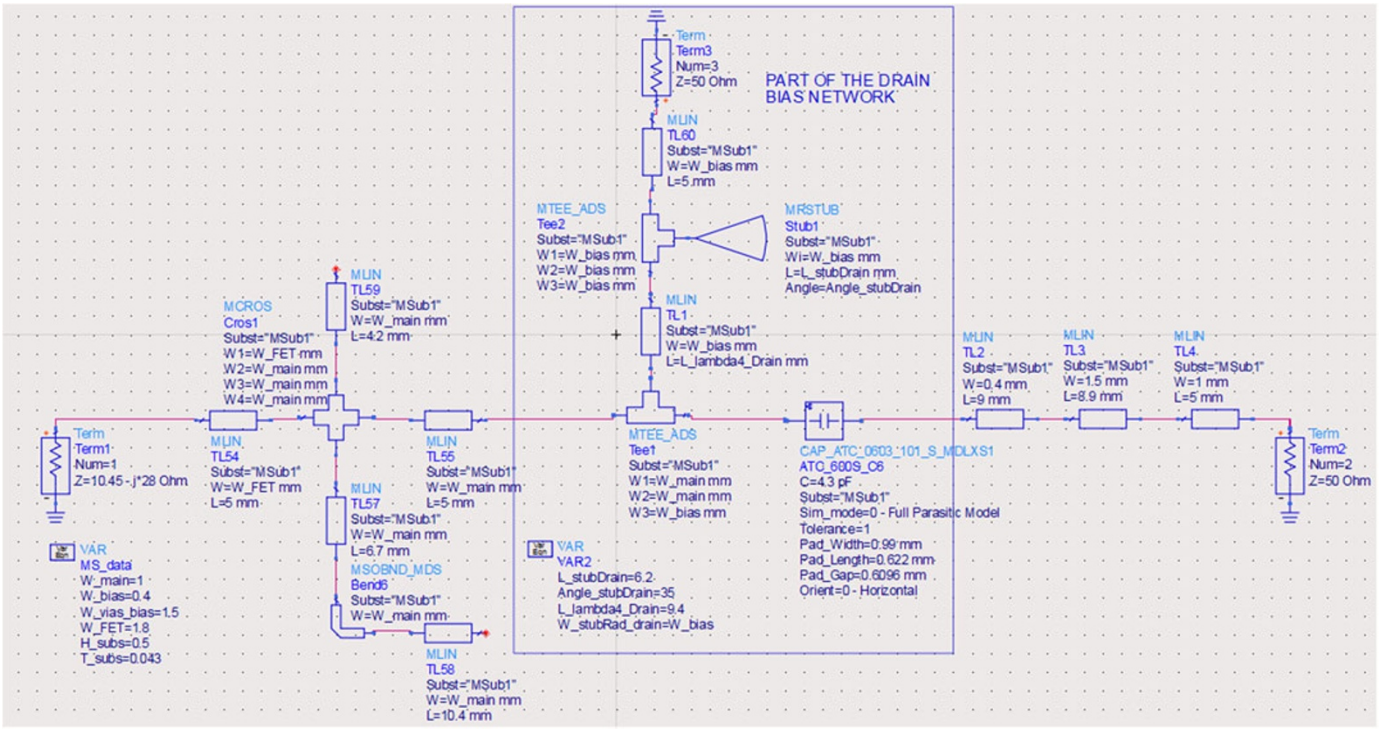

Figure 4. Output matching network design. Part of the drain bias network and decoupling capacitor are shown in the box.

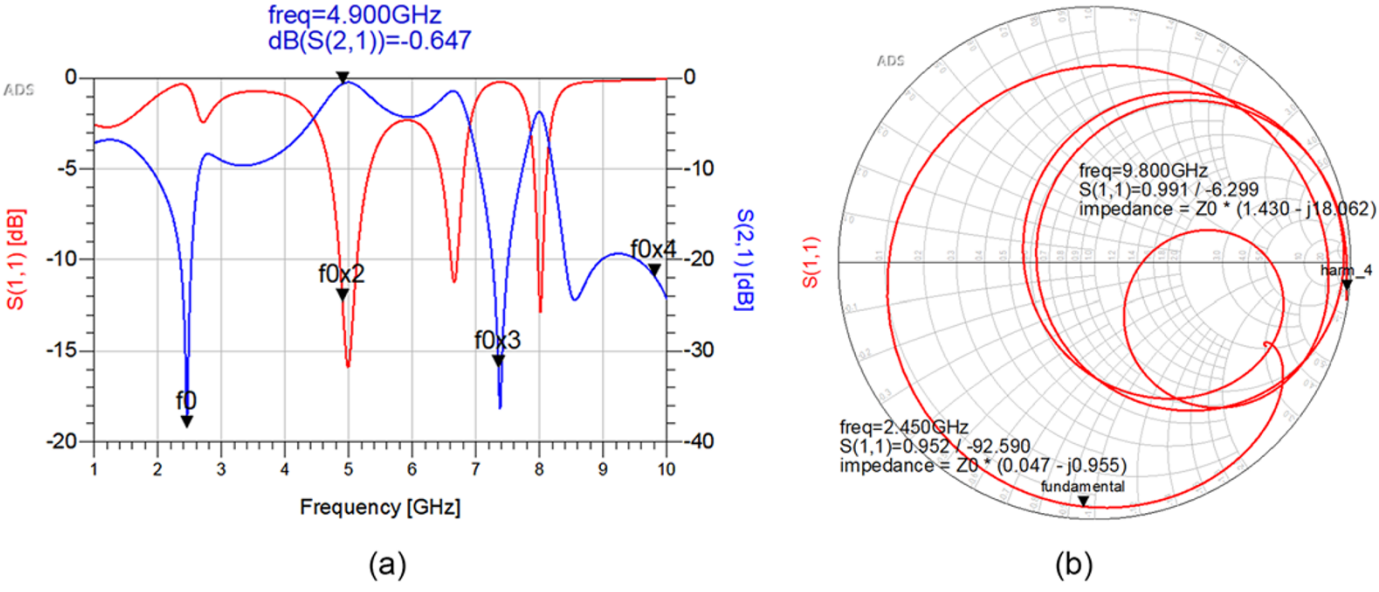

Figure 5. Simulated output matching network (a) S_{11} and S_{21} magnitude in dB. (b) S_{11} magnitude and phase.

harmonics up to the 4th are shown. The maximum predicted G_{c2f_0} is 12.3 dB, and the harmonic suppression is around 30 dBc for the fundamental and larger for the undesired higher harmonics.

Single-ended prototype

The microstrip FD prototype PCB (RO4003C substrate) was processed by laser milling. The circuit was assembled and attached to a copper heat sink. In Fig. 8 the hybrid SE FD prototype is shown.

Small-signal measurements

Using a VNA P9377B, broadband S-parameter measurements were performed. In Fig. 9, the measured S_{11} is shown in comparison to the simulated one. At the fundamental frequency, S_{11} is below −12.5 dB, hence good matching was obtained at the input, including good suppression of the 2nd harmonic.

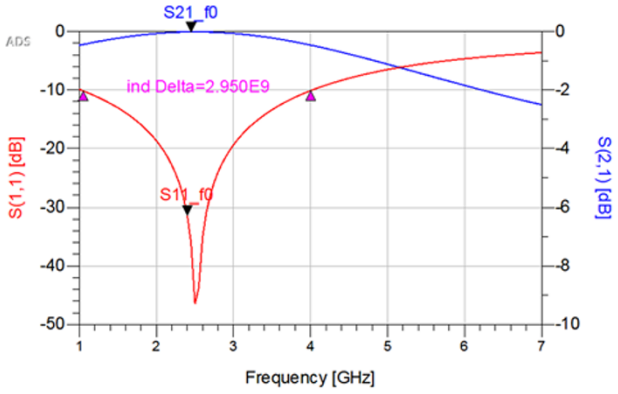

Figure 6. Input matching network simulated S_{11} and S_{21} parameters.

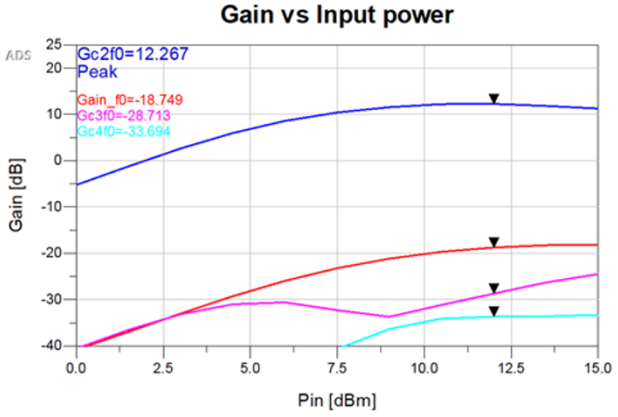

Figure 7. SE FD simulated conversion gains up to the 4th harmonic.

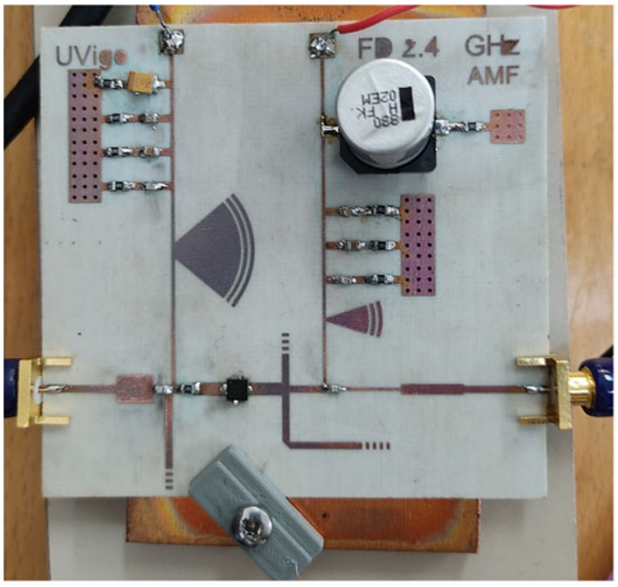

Figure 8. Photo of the designed SE 4.9 GHz FD prototype.

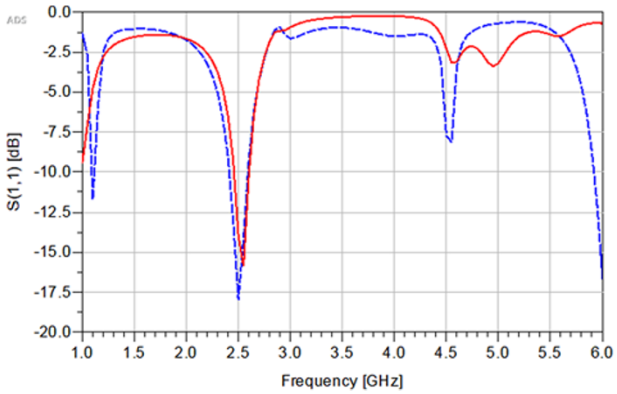

Figure 9. Measured (blue dashed line) and simulated (red continuous line) SE FD prototype S_{11}.

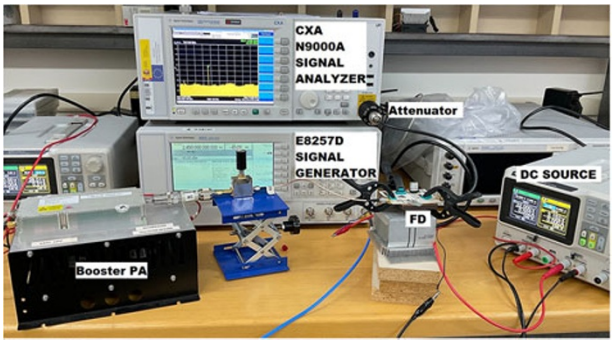

Figure 10. Measurement set-up used to perform large signal measurements.

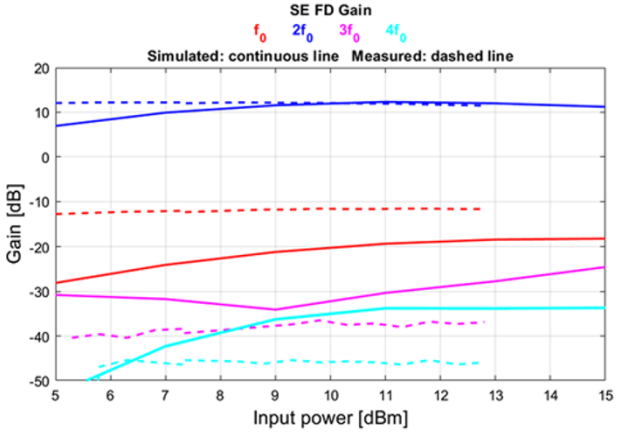

Figure 11. Measured (dashed line) and simulated (continuous line) single-ended FD prototype conversion gains up to the 4th harmonic.

Large-signal measurements

Figure 10 shows the set-up used in this work to perform large-signal measurements. A DC source is used for biasing the HEMT at $V_{DS} = 32$ V and DC drain current (I_{DS}) $= 0.5$ mA. Moreover, a booster amplifier was placed after the E8257D signal generator to provide the desired P_{in}. The receiver (VSA CXA N9000A) bandwidth was capable of measuring above the 4th harmonic, and this instrument was protected using an attenuator. Figure 11 shows the FD prototype power sweep measurements in comparison with simulations. Fundamental signal suppression is around 20 dBc in measurements, while reaching 30 dBc in simulation. Regarding 3rd and 4th harmonics, measured suppression is close to 50 dBc or higher. Measured maximum G_{c2f_0} was 12.2 dB, similar to the simulated one.

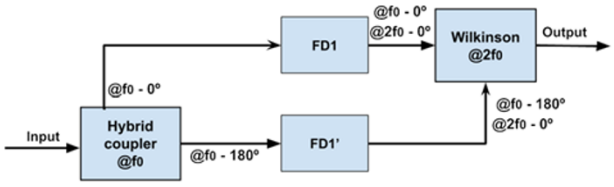

Figure 12. Balanced FD block diagram from [17].

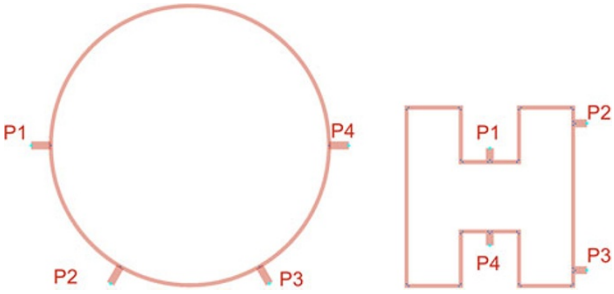

Figure 13. Left side: rat-race ring coupler at 2.45 GHz. Right side: equivalent coupler using Moore space-filling curves (from [17]).

Balanced frequency doubler design

Figure 12 shows the designed BFD block diagram. As indicated before, with this configuration we should expect higher f_0 signal rejection and increased P_{out2f_0} over the single-ended case. For this purpose, the SE FD designed in the previous section was used as the two *FD1*. At the input, a 180° hybrid coupler is required to split and phase-shift the input signal. At the output, a combiner must be used to add in phase both output signals delivered by the SE FDs.

Input 180° hybrid coupler design

A rat-race hybrid coupler is a conventional passive structure used to split a signal into two with a 180° shift. However, its area can be significantly large at low microwave frequencies, such as 2.45 GHz, due to the use of $\frac{\lambda}{4}$ and $3\frac{\lambda}{4}$ sections and conventional substrates. Thus, its miniaturization using space-filling curves, as proposed in [18] and [19], was applied in this work to aid in circuit compactness. In particular, we used Moore curves at its first iteration, since increasing the iteration implies increasing the number of segments and hence, line coupling could happen. In our design, this curve contains 16 segments of 7 mm length each, computed using equation 1 from [19]:

$$a_n = \frac{\pi R}{2(4)^n}, \tag{1}$$

where R is the standard rat-race radius and n is the iteration. Once designed, the obtained total area in this work was 390 mm^2, much reduced in comparison to the equivalent standard rat-race area, 994 mm^2. The difference in size can be appreciated in Fig. 13.

Single-ended FDs output combiner

A Wilkinson hybrid coupler was used to combine the P_{out} of both SE FDs. This coupler was designed at $2f_0$, hence was compact enough. Since several TLs were required after the input coupler to aid separating both SE FDs, bent microstrip transmission lines were also placed at the input of the Wilkinson coupler, providing the proper phase-shift correction for f_0 and the 2nd harmonic in a small space.

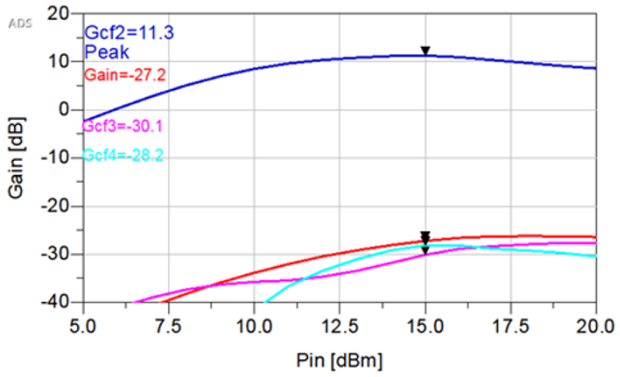

Figure 14. BFD simulated conversion gains up to the 4th harmonic.

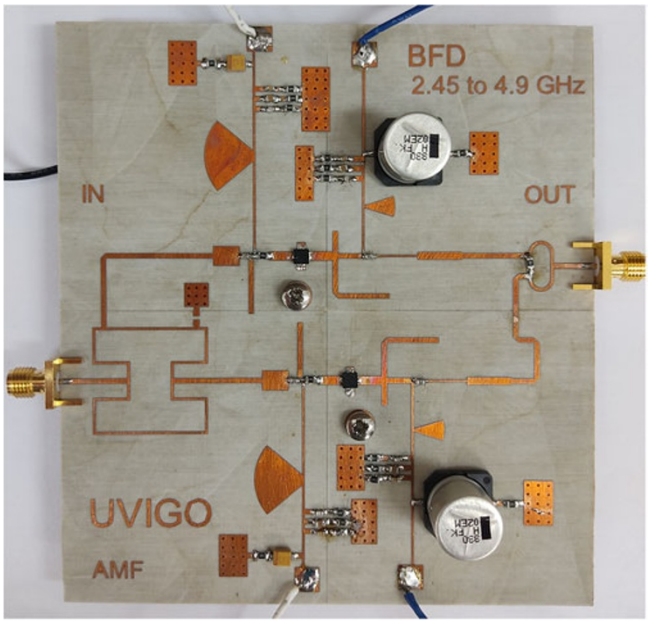

Figure 15. This work BFD prototype working at $2f_0 = 4.9$ GHz.

Balanced frequency doubler simulations

In Fig. 14, simulated conversion gains for the BFD are presented. It is shown that, although the maximum G_{c2f_0} is 1 dB below the simulated SE FD, the P_{in} at this point is 4 dB higher, hence P_{out} has increased in 3 dB. Moreover, the f_0 suppression has improved around 10 dB, achieving almost 40 dBc for f_0 and harmonics up to the 4th.

Balanced frequency doubler experimental results

A photo of the BFD prototype is shown in Fig. 15. It can be seen that both SE circuits are not completely symmetrical. TLs were added at the input of one of the circuits and at the output of the other one, to make feasible the connection to the input and output couplers, respectively. In addition, those TLs lengths are chosen in order to maintain the harmonics phase relationship needed to take advantage of the balanced structure. This relationship is shown in Fig. 12. Similar manufacture and test procedures as with the SE

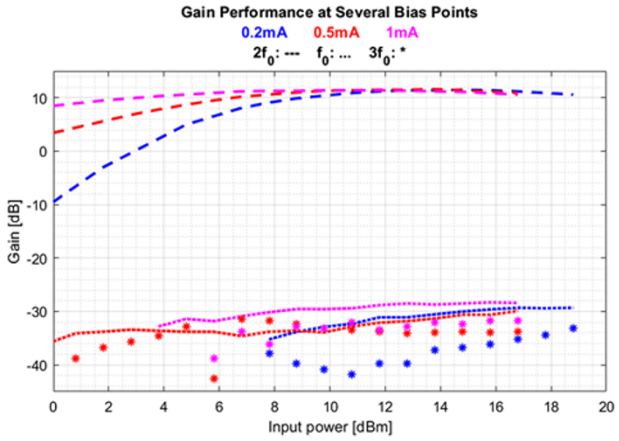

Figure 16. Measured BFD conversion gains, up to the 3rd harmonic, at different bias points: $I_{DS} = 0.2$ mA (blue), 0.5 mA (red) and 1 mA (magenta).

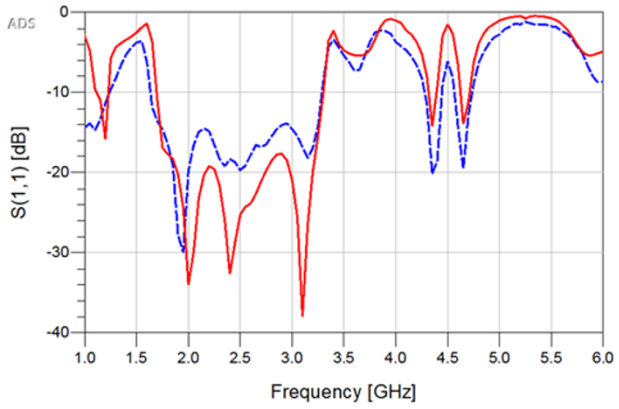

Figure 17. Measured (blue) and simulated (red) BFD prototype S_{11}.

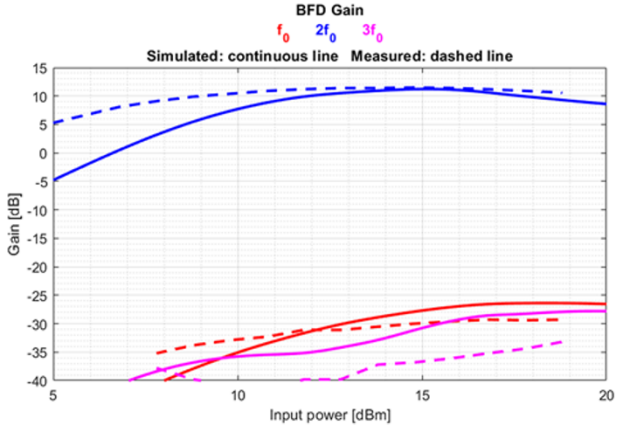

Figure 18. BFD prototype conversion gains simulated (continuous line) and measured (dashed line) vs P_{in}.

FD prototype were applied to the BFD. The small and large-signal set-ups were the same but including an extra DC power supply to bias both HEMTs. All results in this section are for an input $f_0 = 2.45$ GHz.

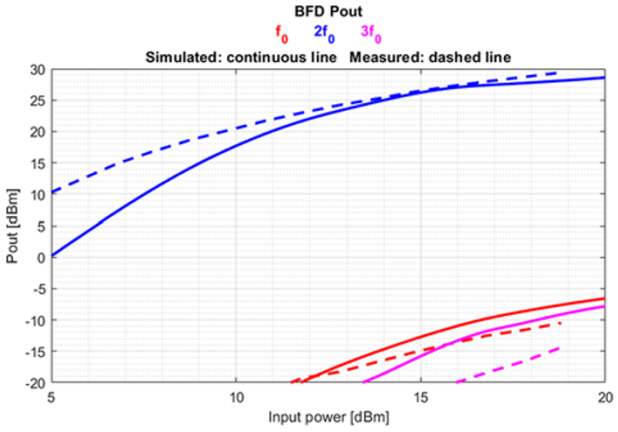

Figure 19. BFD prototype P_{out} from simulations (continuous line) and measurements (dashed line) vs P_{in}.

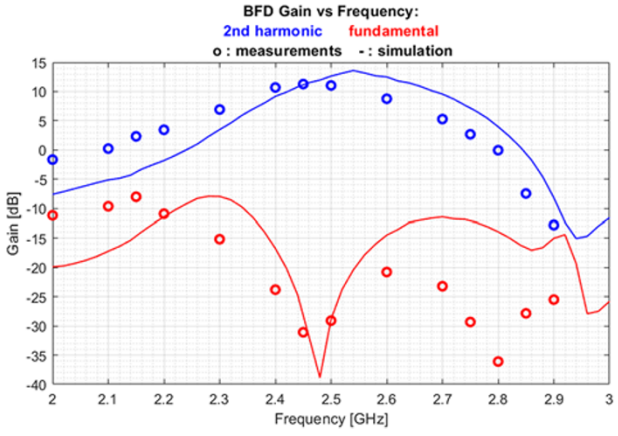

Figure 20. BFD simulated (continuous line) and measured (dots) fundamental gain (red) and 2nd harmonic conversion gain (blue) at the P_{in} for maximum G_{c2f_0} vs f_0.

Measurements at different bias points

Several transistor bias points close to the one used in simulation were tested, in order to analyze which of them provided improved performance, to account for slight inaccuracies in the HEMT model, not optimized for sharp class B. Figure 16 shows a comparison of the BFD conversion gain when I_{DS} is 0.2, 0.5 and 1 mA. It can be seen that the obtained maximum measured G_{c2f_0} is 11.5 dB, achieving also good fundamental and other undesired harmonics suppression. Moreover, when $I_{DS} = 0.2$ mA, the maximum G_{c2f_0} is achieved at higher P_{in}, which implies higher P_{out2f_0}. Therefore, next measurement tests are performed at this specific bias point.

Small-signal measurements

In Fig. 17, S_{11} is shown from 1 to 6 GHz. It can be seen that the bandwidth has increased significantly in comparison to the SE FD, due to the input coupler design, that presents more than 1.5 GHz of bandwidth, measured at a return loss of 10 dB. At f_0, S_{11} is around -20 dB, which provides a good input match.

Large-signal measurements

In Figs. 18 and 19, measured conversion gains and P_{out} up to the 3rd harmonic, respectively, vs P_{in} are shown. Fourth harmonic not shown for clarity, its measured suppression level higher than the 3rd

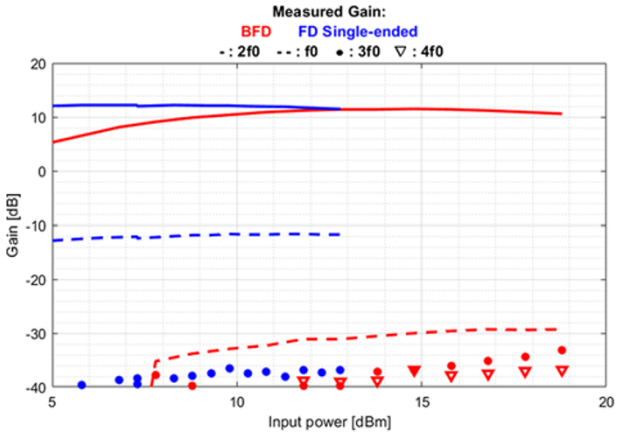

Figure 21. Comparison of the measured conversion gains between the SE FD (blue) and the BFD (red) of this work.

one. The maximum measured G_{c2f_0} is 11.5 dBm and it is achieved at $P_{in} = 14.8$ dBm. At this power, P_{out} is 26.3 dBm. Moreover, f_0 and $3f_0$ suppression exceeds 40 dBc in all the measured range, which is one of the main advantages using the balanced topology.

Next, in Fig. 20, measurements of G_{f_0} and G_{c2f_0} vs f_0 are compared with the results in simulation. If we consider the region in which the G_{c2f_0} is above 5 dB, we obtain a bandwidth for input frequencies from 2.3 to 2.7 GHz, which means 400 MHz. This is equivalent to a 16% fractional bandwidth, hence in the onset of wideband. Moreover, although in simulation the maximum G_{c2f_0} is found at a slightly higher frequency, the prototype achieves its best performance at $2f_0 = 4.9$ GHz.

To our knowledge, this is the first published BFD designed and validated experimentally in hybrid technology using packaged GaN HEMTs.

Comparison of the single-ended and balanced frequency doublers

In this section, the measured figures of merit of the SE FD and BFD are compared in order to show the enhancement in the performance using the balanced configuration. It should be noted that the SE FD measurements were performed at a bias point of $I_{DS} = 0.5$ mA, while in the BFD, $I_{DS} = 0.2$ mA was the bias DC current, determined after the study of different bias points with the BFD prototype, shown in the previous section.

In Fig. 21 it can be observed that the maximum G_{c2f_0} is similar in both designs. However, it should be noted that it is achieved at a higher P_{in} in the BFD, due to the input hybrid coupler, since it implies the need of a P_{in} at least 3 dB higher than in the equivalent SE FD, and due to the differences in the bias points between both prototypes. Moreover, the f_0 signal rejection is approximately 20 dB higher in the BFD, as expected. Regarding the P_{out}, shown in Fig. 22, the reached P_{out2f_0} at the point of maximum G_{c2f_0} is higher at the BFD, since the RF power of the two implied transistors is added.

Conclusion

In this paper a balanced frequency doubler working at $2f_0 = 4.9$ GHz using GaN packaged HEMTs is designed in hybrid technology and validated with measurements. From a careful selection of the HEMTs bias point, the validation of a preliminary single-ended design and the design of a Moore-space-filling curves-based

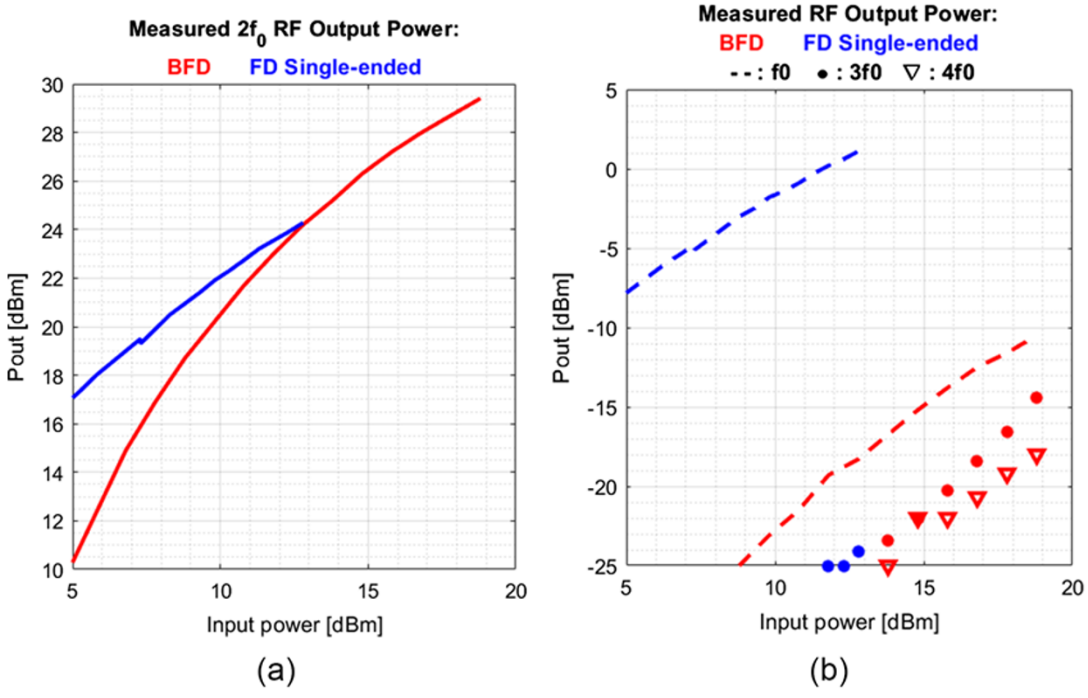

Figure 22. (a) Comparison of the measured P_{out2f_0} between the SE FD (blue) and the BFD (red) of this work. (b) Comparison of the measured P_{out} at other harmonics between the SE FD (blue) and the BFD (red) of this work.

180° hybrid input coupler for compactness, a good RF performance was obtained both in simulations and in measurements of the fabricated prototype. No amplification stage was required, thanks to the performance capabilities of the GaN technology and the adequate selection of matching networks. A maximum measured conversion gain of 11.5 dB with a second harmonic output power of 26.3 dBm was obtained, while fundamental, 3^{rd} and higher harmonics suppression exceeded 40 dBc.

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Competing interests. The authors report no conflict of interest.

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