Development and Implementation of Trap Characterisation and Analysis Techniques for AlGaN/GaN HEMT Technology

by

Wesley Sampson

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Abstract

To advance high-performance AlGaN/GaN HEMTs, understanding and mitigating trapping effects is crucial. In this research, new trap characterisation and analysis methods have been investigated and developed in order to enable detailed investigations into the impact of both fabrication processes and epi-structure variations.

Initially, in collaboration with IQE, this understanding of trap characterisation and analysis was first developed, with a large variety of MIS-HEMT structures fabricated at a commercial foundry. Through the use of DC-IV characterisation, multiple trapping effects were observed and investigated, revealing novel trapping behaviour observable as an output transconductance overshoot. This enabled the development of new characterisation techniques and analysis methods enabling a greater understanding of device topology and the epi-structure on trap effects.

These techniques were then applied to investigate the effect of different fabrication processes and epi-structure variations on traps. When ion implantation was compared with mesa etching for device isolation, ion implantation was found to demonstrate significant advantages over mesa etching, resulting in reduced trapping, improved drain and gate leakage, and improved overall device performance. Furthermore, AlGaN barrier thickness variations were investigated. Here, a 15 nm barrier layer was found to emerge as the optimal thickness, offering a balanced combination of high drain current density, transfer transconductance, and low leakage, while minimising trapping effects. Finally, a low Al concentration AlGaN back barrier on suppressing barrier traps was evaluated. Despite increasing self-heating, the back barrier has been shown to effectively isolate buffer traps, leading to reduced gate and drain-lag current collapse, improved DC-IV characteristics, and enhanced power added efficiency (PAE) at 8 GHz.

This research provides valuable insights into trap characterisation and analysis, enabling the optimisation of AlGaN/GaN HEMT fabrication processes and epi-structures for improved device performance.

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Publications

Conference Presentations

1. **Sampson, W.**, Eblabla, A., Collier, A., Varghese, A., Tasker, P. and Elgaid, K. "Comparison of AlGaN/GaN High Electron Mobility Transistor (HEMTs) on Silicon with GaN cap and In-situ SiN with Trapping Analysis", Presented at: *International Conference on Nitride Semiconductors 14 (ICNS-14)*, Fukuoka, Japan, 12-17 November 2023.

2. Collier, A., **Sampson, W.**, Eblabla, A., Varghese, A., Tasker, P., Patel, J., Tian, L., Asraf, H. and Elgaid, K. "Relative Permittivity Engineering through Amorphous Silicon Nitride PECVD Process Variations for MMIC Applications", Presented at: *International Conference on Nitride Semiconductors 14 (ICNS-14)*, Fukuoka, Japan, 12-17 November 2023.

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4. **Sampson, W.**, Eblabla, A., Collier, A., Hammond, R., Goktepeli, S. and Elgaid, K. "Impact of low Al Concentration AlGaN Back Barrier on Drain Lag in Thin Barrier AlGaN RF HEMTs", *International Workshop on Nitride Semiconductors 14 (IWN-2024)*, Honolulu, US, 3-8 November 2024.

5. Collier, A., **Sampson, W.**, Eblabla, A., Tasker, P., Patel, J. and Elgaid, K. "Stoichiometry Engineering of PECVD Amorphous Silicon Nitride for High

Frequency and High Power Density GaN HEMT Surface Passivation", *International Workshop on Nitride Semiconductors 14 (IWN-2024)*, Honolulu, US, 3-8 November 2024.

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8. Collier, A., **Sampson, W.**, Eblabla, A., Hammond, R., Goktepeli, S., Tian, L., Asraf, H. and Elgaid, K. "AlGaN/GaN MIS-HEMT Kink Effect Attribution to Poole-Frenkel Effect Through Device Topology Analysis," *International Conference on Nitride Semiconductors 15 (ICNS-15)*, Malmo, Sweden, 6-11 July 2025.

9. Papadogeorgos1, S., **Sampson, W.**, Collier, A., Dennis, T., Eblabla, A., Hammond, R., Goktepeli, S. and Elgaid, K. "Output Conductance Overshoot in AlGaN/GaN MIS-HEMTs", *International Conference on Nitride Semiconductors 15 (ICNS-15)*, Malmo, Sweden, 6-11 July 2025.

10. Dennis, T., **Sampson, W.**, Papadogeorgos1, S., Collier, A., Eblabla, A., Hammond, R., Goktepeli, S. and Elgaid, K. "Analysis of Trapping Induced Transconductance Overshoot in the Transfer Characteristics of AlGaN/GaN MIS HEMTs", *International Conference on Nitride Semiconductors 15 (ICNS-15)*, Malmo, Sweden, 6-11 July 2025.

11. Collier, A., Eblabla, A., **Sampson, W.**, Shepphard, D., Harvey, A., Quaglia, R. and Elgaid, K. "Large-signal Performance Comparison of Ion Implant and

Mesa Etch Isolated AlGaN/GaN HEMT Switches on Silicon", Presented at: *20th European Microwave Integrated Circuits Conference (EuMIC)*, Utrecht, Netherlands, 22-23 September 2025.

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1. Goktepeli, S., **Sampson, W.**, Hammond, R., Marchant, H., Collier, A., Eblabla, A., Lees, J., Tasker, P., Quaglia, R. and Elgaid, K. "Analysis of Trapping Induced Transconductance Overshoot in the Transfer Characteristics of AlGaN/GaN MIS HEMTs", *The 2nd IEEE Workshop on Wide Bandgap Power Devices & Applications in Europe (WiPDA Europe)*, Cardiff, United Kingdom, 16-18 Sep 2024.

2. Goktepeli, S., **Sampson, W.**, Collier, A. and Hammond, R. "Deep Traps in GaN-on-Silicon HEMT Devices and Their Effects on RF Performance", *IEEE MTT-S International Microwave Symposium (IMS)*, San Francisco, US, 15-20 June 2025.

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Nomenclature

g_{DS} Output Transconductance

$2DEG$ 2-Dimensional Electron Gas

AlN Aluminium Nitride

BB back barrier

$C-V$ Capacitance-Voltage

CPW Coplanar Waveguide

CZ Czochralski

$DCTS$ Drain Current Transient Spectroscopy

$DIBL$ Drain-Induced Barrier Lowering

DUT Device Under Test

$EB-PVD$ Electron Beam Physical Vapour Deposition

EBL Electron Beam Lithography

$eLRRM$ enhanced Line-Reflect-Reflect-Match

f_t Current Gain Cut-off Frequency

f_{MAX} Maximum Frequency of Oscillation

FET Field Effect Transistor

$GaAs$ Gallium Arsenide

GaN Gallium Nitride

GSG Ground Signal Ground

HBT Heterojunction Bipolar Transistors

$HEMT$ High Electron Mobility Transistor

$HFET$ Heterojunction Field Effect Transistor

ICP Inductively Coupled Plasma

ICS Institute of Compound Semiconductors

InP Indium Phosphide

IPA Isopropyl Alcohol

$LDMOS$ Lateral Diffusion Metal Oxide Semiconductor

LNA Low Noise Amplifer

LOR Lift-Off Resist

MBE Molecular Beam Epitaxy

$MIMO$ Multiple Input Multiple Output

$MIS-HEMT$ Metal-Insulator-Semiconductor High Electron Mobility Transistor

$MMIC$ Monolithic Microwave Integrated Circuits

$MOCVD$ Metal Organic Chemical Vapour Deposition

NQ Non-Quiescent

P_{PE} Piezoelectric Polarisation

P_{SE} spontaneous polarisation

PA Power Amplfier

PAE Power Added Efficiency

$PECVD$ Plasma-Enhanced Chemical Vapour Deposition

PNA Power Network Analyser

Q Quiescent

RF Radio Frequency

RIE Reactive Ion Etching

RTA Rapid Thermal Annealing

$S - Parameters$ Scattering-Parameters

SFP Source Field Plates

Si Silicon

SiC Silicon Carbide

$SiGe$ Silicon Germanium

SMU Source Measure Unit

TRL Thru-Reflect-Line

VNA Vector Network Analyser

FZ Float Zone

Chapter 1

Introduction

1.1 Why GaN HEMTs

There has been rapid growth in the use of high frequency systems in numerous applications such as military, satellite communication, to consumer wireless communication systems such as 5G. One example is with the shift towards 5G where billions of devices will be connected, and high data rates of multi-Gbps is required. These systems consist of multiple components, and due to the requirement of Multiple Input Multiple Output (MIMO) configurations, RF systems are growing in complexity. The RF front end consists of power amplifiers (PA), low-noise amplifiers (LNA), and switches. During transmission, the efficiency of the power amplifier is the most important metric due to both power and thermal constraints [1]. The PA needs constant development to achieve higher power, higher frequency and higher efficiency to meet the demand for future high-frequency RF systems [2].

Since PA technology emerged in the communications market in the 1990s, it has been dominated by silicon (Si) lateral diffusion metal oxide semiconductor (LDMOS) devices. This is still the case for applications with operating frequencies below 2 GHz [1]. Currently in mobile phones, the dominant technology is the GaAs heterojunction bipolar transistor (HBT) [3]. Silicon dominated because of its low cost and highly mature technology. However, Si suffers from several disadvantages such as; low critical electric field, low operating temperature, and low carrier mobility. Whilst

GaAs HBTs offer fantastic RF performance, they suffer also suffer from a low critical electric field.

To overcome these shortcomings and the requirement for higher power densities, the move to a new semiconductor material is required. Wide-bandgap semiconductors have been considered an enabling technology. and of these, Gallium Nitride (GaN) has emerged as one of the most promising options [4] due to its advantages over silicon and GaAs HBTs [5].

The reason GaN is considered ideal for both high-power and high-frequency applications is its unique material properties. This results in GaN having a high critical electric field, high electron saturation velocity, high thermal conductivity, and a low dielectric constant. Therefore, it is likely that GaN will replace all traditional semiconductor materials for 5G communication systems [1].

Its electrical properties can be seen in Table 1.1 taken from [4], compared to the electrical properties of Si, Gallium Arsenide (GaAs), 4H-SiC, $GaN_{(Bulk)}$, and $GaN_{(HEMT)}$. The difference between $GaN_{(Bulk)}$ and $GaN_{(HEMT)}$ is due to the formation of a two-dimensional electron gas (2DEG) in the GaN High Electron Mobility Transistor (HEMT) [6].

Table 1.1: Comparison of material properties of different semiconductors [4]

Material	Bandgap Eg (eV)	Mobility μn ($cm^2V^{-1}s^{-1}$)	Permittivity ϵ	Saturation Velocity (cms^{-1})	Critical Field Ec (Vcm^{-1})
Si	1.12	1400	11.8	1×10^7	3×10^5
GaAs	1.42	8500	12.8	2×10^7	4×10^5
4H-SiC	3.23	260	9.7	2×10^7	2.9×10^6
$GaN_{(Bulk)}$	3.44	900	9	2.5×10^7	3.3×10^6
$GaN_{(HEMT)}$	3.44	1800	9	2.5×10^7	3.3×10^6

The properties of GaN are approximately 3.1 times the energy band gap, 2.7 times the electron saturation velocity, and 11.6 times the critical electric field over Si [7]. GaN also has approximately 5 times the breakdown voltage of any other transistor technology with similar high frequency power gain such as those made from Si, Silicon Germanium (SiGe), Indium Phosphide (InP), and GaAs [8]. This increased breakdown voltage is highly desirable due to the need for devices to operate

at both high temperature (> 250 °C), and high output power at high frequencies (> 100 GHz) [9] [10].

1.2 Current Issues with RF GaN HEMTs - Trapping Effects

During the last 30 years, there has been a significant amount of research on the RF GaN HEMT device with significant success. Table 1.2 taken from [11] highlights the current state of the art for GaN HEMT RF performance. In 2020 the first GaN power amplifier MMIC operating beyond 200 GHz was reported in [12], and in recent years there has been significant success with Monolithic Microwave Integrated Circuits (MMIC) operating above 100 GHz in the W, D and G bands [13] [14] [15] [16] [17] [18].

Table 1.2: An Overview of the Current Commercial Deep Sub-Micron GaN Processes [11].

	L_g (nm)	f_t (GHz)	f_{max} (GHz)	P_{out} (W/mm @ GHz)	Bias (V)
NGC	200/150	65	-	4 @ 38	28
Qorvo	90	115/145	-	1.3 @ 35	13-15
Raytheon	<150	-	200	2.8 @ 95	18
Ommic	100	100	180	3.3	12
HRL T3	40	220	440	-	1-12
HRL T4	20	320	550	-	0.5-4
Cree	150	30/40	>80	3.5 @ 30	28
Fraunhofer	100	110	>320	2 @ 40	15

However, despite this success, GaN HEMTs are plagued with numerous issues. These issues include DC-RF dispersion, poor power-added efficiency (PAE), and linearity [1]. These negative effects are attributed to the presence of trap states in the bulk epi-structure and at the surface of the device. These traps lead to stability and reliability issues. These issues can manifest as current collapse, threshold voltage drift, short-channel effect deterioration, and reduced RF power output. These significantly hinder the performance of GaN HEMTs [19]. The prevalence of these trap states in GaN HEMTs is due to the large lattice mismatch, with the substrate

typically being a non-native substrate such as Si or SiC. This leads to growth defects and dislocations that can become sources of trap effects [20].

1.3 Research Achievements

This thesis has two main Achievements:

1. Develop trap characterisation and analysis techniques that can be used to assess the impact of variations in the fabrication process and epi-structure on the AlGaN HEMT trap states.

2. Apply the developed trap characterisation and analysis techniques to the pre-existing DC and RF characterisation methods that are used in the research group to enable deeper investigations into the effect of alternative fabrication processes and epi-structure variations on device linearity and efficiency.

Achieving both of these has enabled improvements in both the process flow for device fabrication and provided insight into epi-structure variations that can be used to enhance the performance of RF AlGaN/GaN HEMT devices.

1.4 Thesis Outline

This thesis consists of 9 chapters:

Chapter 1 provides an introduction to the current state-of-the-art GaN HEMTs, followed by the current issues and challenges facing GaN HEMTs that prevent their full potential from being realised.

Chapter 2 reviews the basic operating principles of GaN HEMTs at both DC and RF, with important figures of merit discussed and details on how small-signal RF measurements are performed and small-signal equivalent circuit models can be derived.

Chapter 3 discusses the trapping effects in GaN HEMTs, along with the physics that causes these trapping effects, what effect they have on GaN HEMTs, and how they can be characterised and suppressed.

Chapter 4 presents the fabrication process and the techniques required to produce high-performance RF GaN HEMTs. It starts with an introduction into the material properties and material growth, followed by a brief description of all the fabrication steps carried out for this work.

Chapter 5 in collaboration with IQE, aims to develop the capability and DC-IV characterisation methods that can be used to determine the location and the effect of trap states in AlGaN/GaN devices, through a simple epi-structure and a wide variety of metal-insulator semiconductor high-electron mobility transistor (MIS-HEMT) structures. In this section a new trapping effect is observed that has been previously unreported, along with the observation of multiple trapping effects that have been identified and discussed.

Chapter 6 investigates the effect of two different isolation methods on the performance of AlGaN/GaN HEMT that have been fabricated. The effect of mesa etching and ion implantation for device isolation was investigated with regard to the trapping states in the device and, therefore, the effect of the fabrication process on the linearity and efficiency of AlGaN/GaN HEMTs. The DC and RF performance has also been investigated with small signal modelling performed to investigate the effect of device isolation on the intrinsic device parameters.

Chapter 7 assesses the trade-off between the desire to reduce the AlGaN barrier thickness to enable higher frequency operation of AlGaN HEMTs, and the potential negative impact this reduction in AlGaN barrier thickness can have on device properties. To perform this analysis, three different wafers with different AlGaN

barrier thicknesses were used for the fabrication of AlGaN/GaN HEMTs. These were then characterised to determine the effect of barrier thickness in the quantity of trap states. The DC and RF performance has also been investigated for each AlGaN barrier thickness to determine the optimal thickness for the fabrication of short gate AlGaN/GaN HEMTs for high-frequency operation.

Chapter 8 analyses the effectiveness of a low Al concentration AlGaN back barrier in the epi-structure below the channel to determine its effectiveness in reducing the effects of buffer traps. For this, multiple AlGaN/GaN HEMTs were fabricated on two different wafers. One with no AlGaN back barrier and the other with an AlGaN back barrier. Multiple characterisation methods have been used to observe the impact of this AlGaN back barrier in the suppression of trap effects, along with the effect on device performance. These characterisation methods include DC-IV, Pulsed-IV, DCTS, small-signal RF, and a large-signal load pull and power sweep at 8 GHz.

Chapter 9 concludes this research thesis, summarising the findings along with a discussion of the potential for future work.

Chapter 2

Introduction to Gallium Nitride High Electron Mobility Transistors

2.1 History of the GaN HEMT

The High Electron Mobility Transistor (HEMT) was first demonstrated by Mimura et al. at Fujitsu Labs in 1980 in the Gallium Arsenide (GaAs) material space [21]. The first demonstration of a HEMT in Gallium Nitride (GaN) was done by Khan et al. in the early 1990s with the first observation of a 2DEG in GaN in [22], and the first fabrication of a GaN HEMT in [23]. Since then, despite its virtually non-existent high-frequency performance at the time [8], the GaN HEMT has become one of the most powerful and power-efficient RF devices in the 1 to 100 GHz frequency range.

2.2 Operating Principles of GaN HEMTs

2.2.1 Polarisation and Formation of 2DEG channel

The HEMT is a Field Effect Transistor (FET), which can also be referred to as a Heterojunction Field Effect Transistor (HFET). This name is due to the formation of a heterostructure, at the junction between two semiconductor materials with

different band gaps [24]. The conventional AlGaN/GaN HEMT structure, shown in Figure 2.1, leads to the formation of this heterojunction between the AlGaN and GaN layers, due to the dissimilarities in the band gap of AlGaN and GaN. At this heterojunction, electrons will move from the top layer surface due to of the spontaneous polarisation (P_{SE}) that occurs because of the wurtzite-shaped GaN crystal structure. At this heterojunction, the collection of the free carriers leads to the creation of a conducting channel. The electrons confined to this channel are referred to as a 2-Dimensional Electron Gas (2DEG). This 2DEG is confined in the third dimension and can only freely move in two directions. Because of the separation of the electrons from these donor atoms, there is a significant reduction in the Coulomb scattering, which leads to extremely high mobility and thus a high saturation velocity of the electrons.

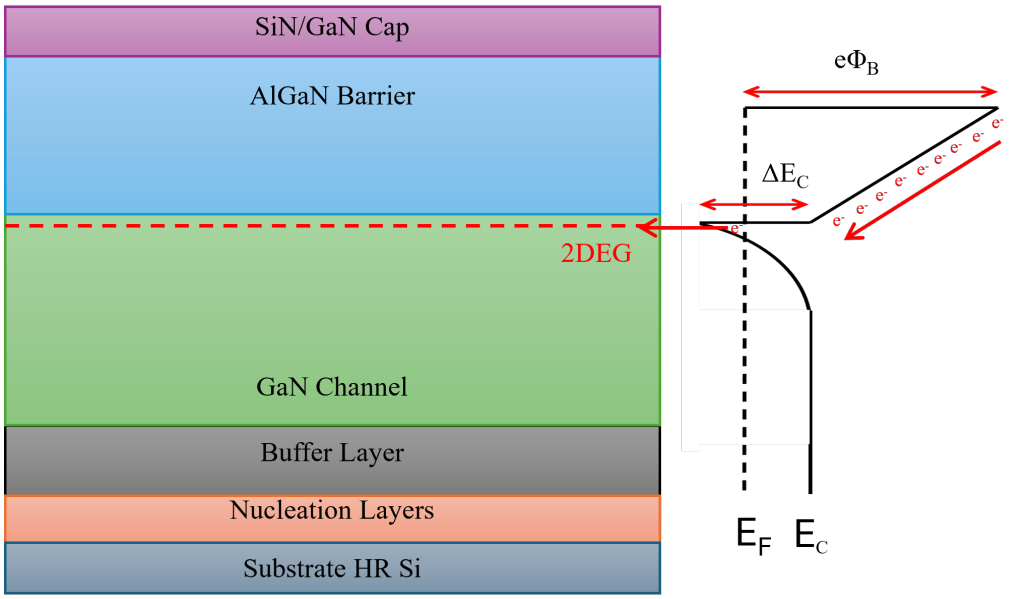


Figure 2.1: A standard HEMT structure is shown with the location of the formed 2DEG. To the right the band structure is shown, highlighting the quantum well that forms below the Fermi level to confine the 2DEG. The movement of electrons from surface donor states to the 2DEG is also highlighted.

The ability of AlGaN/GaN HEMTs to form this 2DEG without any additional doping is due to the P_{SE} and piezoelectric attributes, which originate in the III-Nitrides crystals. This quality is due to the III-nitride wurtzite crystal arrangement. The high variation in electronegativity due to covalent-ionic bonds and the lack of

symmetry along the c-direction lead to this very high P_{SE} in the $< 0001 >$ direction. The other polarisation effect is piezoelectric polarisation (P_{PE}) which is formed due to strain in the epitaxial layers. This originates from the lattice mismatch between the thin AlGaN and the thicker GaN layers. Therefore, the polarisation charges come from these two sources, the piezoelectric effect from strain in the AlGaN layer, and the difference in P_{SE} between AlGaN and GaN. Due to the increased piezoelectric constants and the P_{SE} moving from GaN to AlGaN, the total polarisation in the AlGaN layer is larger than that in the GaN layer. The stress is defined as:

$$P_{PE} = 2\varepsilon_a \left(e_{31} - \frac{e_{33}c_{13}}{c_{33}} \right) \tag{2.1}$$

where ε_a is the lattice constant of AlGaN, e_{31} and e_{33} are the piezoelectric constants and c_{13} and c_{33} are the elastic constants of the AlGaN and GaN material, respectively.

This effect leads to a positive polarisation charge at the AlGaN/GaN interface. This has the effect of pulling the conduction band down as shown in Figure 2.1. This causes the electrons to move from the donor atoms to compensate for this positive charge, resulting in the formation of the 2DEG, confined in the quantum well that forms below the Fermi level (E_F) at the AlGaN/GaN interface. In the GaN material, the conduction band is then pulled up as a result of the polarity shifting as the polarisation shifts the charge to negative.

The formation of the 2DEG due to polarisation is described by:

$$\sigma = (P_{SP,AlGaN} + P_{PE,AlGaN}) - P_{SP,GaN} \tag{2.2}$$

where σ is the sheet charge where the AlGaN and GaN layers meet, P_{PE} and P_{SP} represent the piezoelectric polarisation and the positive spontaneous polarisation, respectively.

The mathematical expression for the 2DEG concentration is:

$$n_s = \left(\frac{\sigma}{q}\right) - \left(\frac{\varepsilon_0 \varepsilon_r}{q^2 t_{AlGaN}}\right)(q\phi_b + E_F - \Delta E_C) \tag{2.3}$$

where ΔE_C represents the energy variation between the AlGaN and GaN material, E_F is the Fermi level with respect to the conduction band of the GaN material, $q\phi_b$ is the barrier height of the Schottky gate, t_{AlGaN} is the thickness of the AlGaN layer, ε_r is the dielectric constant, q is the charge of an electron, σ is the sheet charge where the AlGaN and GaN layers meet, and n_s is the 2DEG current density [25] [26] [27].

2.3 GaN HEMT DC Characteristics

In the operation of a GaN HEMT current is confined in the 2DEG. Current flows between the drain and the source (I_{DS}), and the flow of I_{DS} is controlled by applying a voltage to the gate. Due to the confinement of the current flow to the 2DEG, the quality of this 2DEG has a significant impact on the conductivity of the channel. The quality of this channel is highly dependent on the epilayer structure used to grow the GaN HEMT. The conductivity of 2DEG is defined as:

$$\sigma = q n_s \mu \tag{2.4}$$

where σ is the sheet conductivity in the 2DEG, q is the charge of an electron, n_s the current density of 2DEG and μ is the mobility of electrons. This highlights the dependence of channel conductivity on carrier concentration and mobility [28].

In GaN HEMTs the DC output characteristics can be separated into two regions, the linear region and the saturation region. These regions are shown in Figure 2.2 where the linear region is defined by the point at which the electric field of the drain-source ($E_{(x)}$) is less than the critical electric field (E_c) . This is defined as ($E_{(x)} < E_c$). The saturation region is where the drain-source electric field is greater than the critical electric field ($E_{(x)} > E_c$). The critical electric field is the point at which the electric field has a potential high enough to allow the electrons to travel

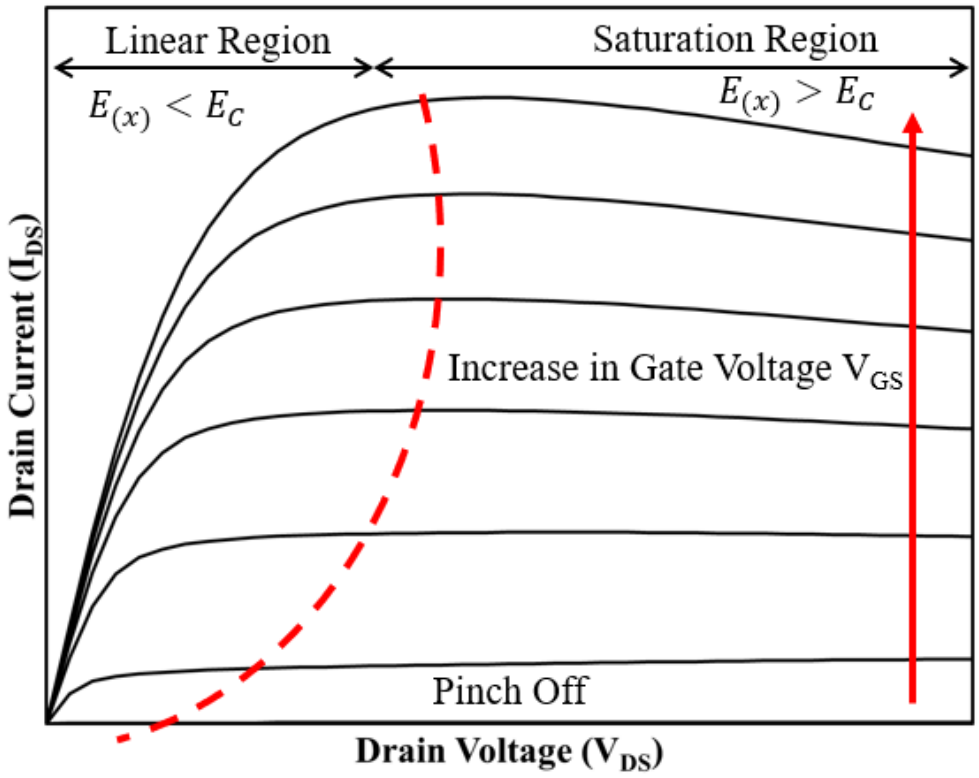


Figure 2.2: DC Output Characteristics of a GaN HEMT, showing the linear region, saturation region, and device pinch off.

at their saturation velocity (v_{sat}).

The velocity of electrons in the linear region is governed by:

$$v = \mu E_{(x)} \tag{2.5}$$

where $E_{(x)}$ refers to the electric field potential, v is the velocity of the electrons, and μ is the mobility of the electron.

For the saturation region, the velocity of the electrons is no longer dependent on the source-drain electric field because their velocity has saturated. This is defined as:

$$v = v_{sat} \tag{2.6}$$

The drain-source current (I_{DS}) flow across the channel is expressed as:

$$I_{DS} = qn_s(x)v(x) \tag{2.7}$$

where q is the charge of an electron, $n_s(x)$ is the 2DEG current density, and $V_{(x)}$ is the velocity of the electrons in the channel. This applies when I_{DS} is normalised to the width of the gate (W_G).

Taking into account the channel potential $V_{(x)}$, the 2DEG charge density is:

$$qn_s = C(V_{GS} - V_t - V_{(x)}) \tag{2.8}$$

where V_t represents the threshold voltage and C represents the gate capacitance normalised to W_g.

Looking at the linear region where $E_{(x)} < E_c$, both Equations 2.5, 2.6, and 2.8 can be substituted into Equation 2.7 to result in:

$$I_{DS} = C(V_{GS} - V_t - V_{(x)}) \cdot \mu \frac{dV_{(x)}}{dx} \tag{2.9}$$

This can then be rearranged to give the differential:

$$\frac{I_{DS}}{C \cdot \mu} dx = (V_{GS} - V_t - V_{(x)}) dV_{(x)} \tag{2.10}$$

This can then be integrated, which when in the linear region, results in:

$$I_{DS} = \frac{\mu C}{x} \left[(V_{GS} - V_t)V_{(x)} - \frac{V_{(x)}^2}{2} \right] \tag{2.11}$$

When a small V_{DS} is applied, this linear region is applied throughout the channel, substituting $x = L_g$ and $V_{(x)} = V_{DS}$, the drain current in this linear region can be described by:

$$I_{DS,lin} = \frac{\mu C}{L_g} \left[(V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2} \right] \tag{2.12}$$

If this $I_{DS,lin}$ is now differentiated with respect to V_{GS}, it allows us to derive the transconductance (g_m):

$$g_{m,lin} = \frac{\mu C}{L_g} V_{DS} \tag{2.13}$$

since transconductance is the rate of change in I_{DS} with respect to V_{GS}.

The equations derived above are only valid when V_{DS} is low and the HEMT is operating in the linear region. Therefore, when V_{DS} increases to a value large enough to introduce velocity saturation at any point in the channel, reaching the saturation region. It becomes important to focus on the point at which the critical electric field occurs. Equation 2.11 therefore needs to be solved for $V_{(x)}$:

$$V_{(x)} = V_{GS} - V_t - \sqrt{(V_{GS} - V_t)^2 - \frac{2I_{DS}x}{\mu C}} \tag{2.14}$$

and $E_{(x)}$:

$$E_{(x)} = \frac{dV_{(x)}}{dx} = \frac{I_{DS}}{\mu C \sqrt{(V_{GS} - V_t)^2 - \frac{2I_{DS}x}{\mu C}}} \tag{2.15}$$

Taking l_c as the point of the critical electric field and setting $x = l_c$, means that the electron saturation velocity must satisfy the below:

$$v_{sat} = \mu E_{(l_c)} = \mu E_c \tag{2.16}$$

Taking Equation 2.15 and substituting into this equation allows us to calculate I_{DS} in the saturation region:

$$I_{DS,sat} = v_{sat} C \left[\sqrt{(V_{GS} - V_{th})^2 + (l_c E_c)^2} - l_c E_c \right] \tag{2.17}$$

Since saturation I_{DS} depends on V_{GS}, the transconductance in the saturation region is obtained by differentiating this equation with respect to V_{GS}, resulting in the following.

$$g_{m,sat} = v_{sat} C \frac{V_{GS} - V_{th}}{\sqrt{(V_{GS} - V_{th})^2 + (l_c E_c)^2}} \tag{2.18}$$

In short gate length devices, l_c becomes small and this allows the two above equations to be approximately reduced for $I_{DS,sat}$:

$$I_{DS,sat} \approx v_{sat}C(V_{GS} - V_{th}) \tag{2.19}$$

and for $g_{m,sat}$:

$$g_{m,sat} \approx v_{sat}C \tag{2.20}$$

These equations only take the intrinsic part of the AlGaN/GaN HEMT, so the extrinsic components must be added, and V_{GS} and V_{DS} need to be redefined to $V_{GS,ext}$ and $V_{DS,ext}$ to indicate that they are applied directly to the source, gate, and drain electrodes directly.

For V_{GS} we get:

$$V_{GS} = V_{GS,ext} - I_{DS}R_s \tag{2.21}$$

and for V_{DS}:

$$V_{DS} = V_{DS,ext} - I_{DS}(R_s + R_d) \tag{2.22}$$

In both of these R_s and R_d refer to the source and drain resistances, respectively. [29]

2.4 GaN HEMTs at RF

2.4.1 The Small Signal Equivalent Circuit Model

At high frequencies, the device is studied in terms of a small-signal equivalent circuit model. Under small-signal conditions, the non-linear characteristics of HEMTs can be linearised and described using a linear small-signal model, using lumped elements. The model used in this work is shown in Figure 2.3 and consists of two sections; Extrinsic parameters, and intrinsic parameters. The extrinsic parameters are parasitic elements that depend on the device layout and tend to degrade RF performance. Each of these elements in the small signal model translates into a physical effect occurring in the device and are listed in Table 2.1.

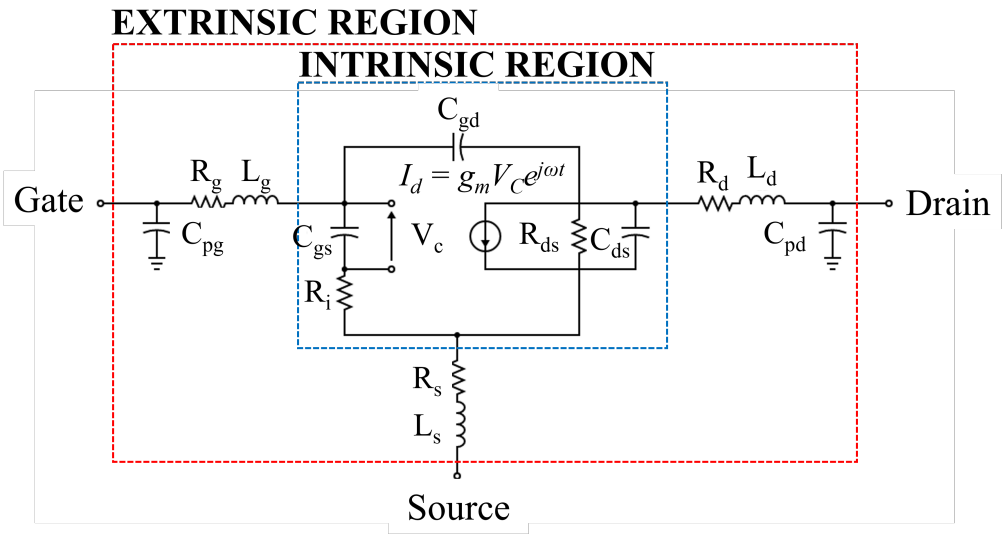


Figure 2.3: HEMT small-signal equivalent circuit model. Elements inside the red dashed lines, refer to the extrinsic parasitics, and inside the blue dashed lines are the intrinsic device parameters.

Intrinsic Equivalent Circuit Parameters

In this HEMT small signal model, I_{DS} is dependent on both V_{GS} and V_{DS}. Changing V_{GS} or V_{DS} results in changes in I_{DS} defined by the transconductance (g_m). When V_{GS} changes rapidly, I_{DS} cannot change immediately due to the time required to charge and discharge the associated gate capacitance in the depletion region. This

	Parameter	Physical description
Intrinsic	C_{gs}	Gate-source capacitance
	C_{gd}	Gate-drain capacitance
	C_{ds}	Drain-source capacitance
	R_i	Input resistance
	R_{DS}	Drain-source resistance
	g_m	Transconductance
	τ	Transconductance delay
Extrinsic	R_g	Gate resistance
	R_g	Gate resistance
	R_d	Drain resistance
	R_s	Source resistance
	L_g	Gate inductance
	L_d	Drain inductance
	L_s	Source inductance
	C_{pg}	Gate Pad Capacitance
	C_{pd}	Drain Pad Capacitance

Table 2.1: Small-signal equivalent circuit components and their physical descriptions.

leads to a time delay τ at high frequencies:

$$g_m(\omega) = g_m e^{-j\omega\tau} \tag{2.23}$$

where $\omega = 2\pi f$ is the angular frequency, f is the operating frequency and j is the imaginary unit.

The gate-source capacitance C_{gs} and the gate-drain capacitance C_{gd} describe the change throughout the depletion region under the gate, when V_{GS} is varied:

$$C_{gs} = \left.\frac{dQ_G}{dV_{GS}}\right|_{V_{DS}=\text{const.}} \tag{2.24}$$

and where V_{DS} is varied:

$$C_{gd} = \left.\frac{dQ_G}{dV_{DS}}\right|_{V_{GS}=\text{const.}} \tag{2.25}$$

here, Q_G refers to the charge at the gate, which is equal but opposite to the

charge induced throughout the depletion region.

Drain-source capacitance C_{ds} represents the capacitance between the drain and the source, after the extrinsic pad capacitance has been removed:

$$C_{ds} = \left.\frac{dQ_D}{dV_{DS}}\right|_{V_{GS}=\text{const.}} \tag{2.26}$$

where Q_D refers to the drain charge.

Of the remaining intrinsic parameters shown in Table 2.1, R_i refers to the input resistance, which affects the gate charging time and R_{gd} is complementary to R_i and reflects the symmetrical nature of the physical device in the linear region [30]. R_{ds} represents the finite output resistance of the device [31].

Extrinsic Equivalent Circuit Parameters

The extrinsic parameters are also shown in Table 2.1. Here R_s and R_d refer to the ohmic contact of the source and the drain, including the bulk resistance, leading to the active channel, respectively. R_g refers to the metallisation resistance due to the formation of the Schottky contact.

L_g, L_s and L_d, refer to the parasitic inductance through the contact pads, for the gate, source and drain, respectively.

C_{pg} and C_{ps} are the parasitic capacitances and represent the electric field distribution, due to contact pads.

Defining f_t and f_{MAX} through the equivalent circuit model

The definition of both f_t and f_{MAX} can be represented by the equivalent circuit model using:

$$f_T = \frac{1}{2\pi[(C_{gs}+C_{gd})(1+\frac{R_s+R_d}{R_{ds}}) + g_m C_{gd}(R_s+R_d)]} \tag{2.27}$$

for f_t and:

$$f_{MAX} = \frac{f_T}{2\sqrt{\frac{R_i+R_g+R_s}{R_{ds}} + 2\pi f_T R_g C_{gd}}} \tag{2.28}$$

f_{MAX} [32].

2.4.2 S-Parameter Measurements

High-frequency characterization of HEMTs relies heavily on scattering parameters (S-parameters). Unlike low-frequency measurements using impedance (Z-parameters) or admittance (Y-parameters), S-parameters are preferred at RF due to their ease of measurement and analysis. S-parameters represent the ratio of incident and reflected power waves at each port of the device, providing valuable information about signal transmission and reflection. These consist of a 2-port measurement system as described in Figure 2.4.

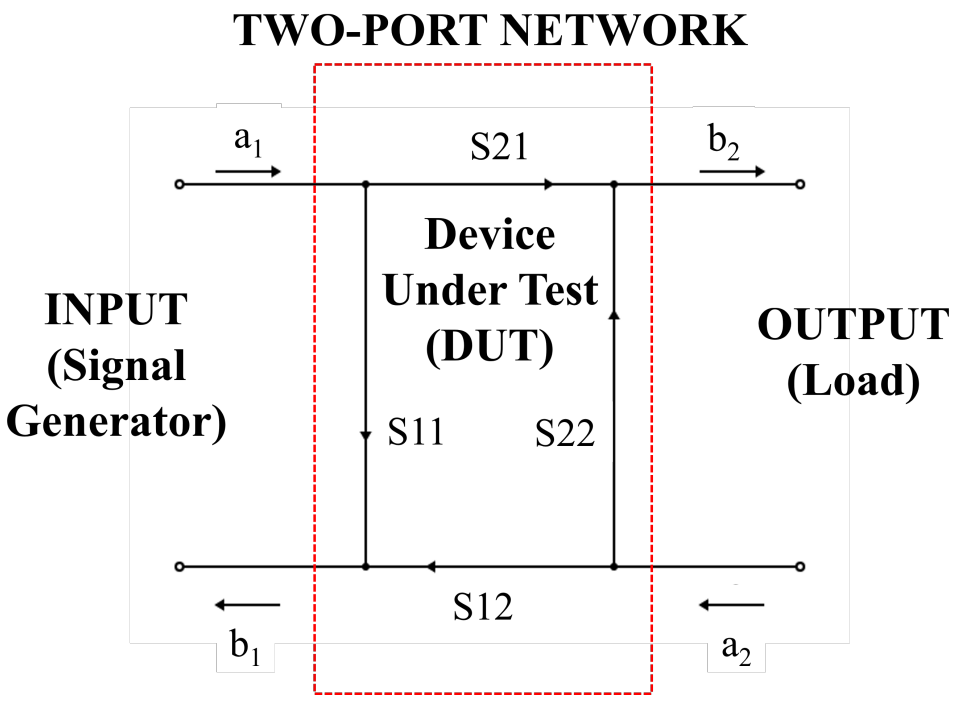


Figure 2.4: Two-Port s-parameter measurement system, with input signal generator and output load for RF characterisation of GaN HEMTs.

In DC measurements, in order to terminate the load for measurements, an open or a short is used to allow for Voltage and Current to be measured; however, at high frequencies, the implementation of an open or short is highly complicated. Therefore,

to measure the s-parameters, either a Vector Network Analyser (VNA) or Power Network Analyser (PNA) will be used. These instruments employ a 50 Ω termination load to eliminate reflections. At high frequencies, it is difficult to implement a 50 Ω load due to parasitic effects. This standardised termination simplifies measurements and ensures consistent results in different setups [33].

The s-parameter matrix describes the relationship between incident (a) and reflected (b) waves, and can be expressed as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.29}$$

From this matrix representation, the individual reflected waves (b_1) and (b_2) can be explicitly written as:

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.30}$$

and

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.31}$$

where S is the s-parameters, and a and b represent the incident and reflected wave components, respectively.

The S parameter input reflectance coefficient is described as:

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2=0} \tag{2.32}$$

the output reflectance coefficient is:

$$S_{22} = \frac{b_2}{a_2}\Big|_{a_1=0} \tag{2.33}$$

the input forward gain is given by:

$$S_{21} = \frac{b_2}{a_1}\Big|_{a_2=0} \tag{2.34}$$

the output reverse gain is given by:

$$S_{12} = \frac{b_1}{a_2}\Big|_{a_1=0} \tag{2.35}$$

During measurements, S_{11} and S_{21} are measured by terminating the output port with the 50 Ω load, where S_{12} and S_{22} are measured by terminating the input port with the 50 Ω load [29].

S-parameter measurements can easily be converted into many other parameter forms to allow further analysis of the measurements such as Z- and Y-parameters [34].

There are two main figures of merit for an RF HEMT, which are the Current Gain Cut-off Frequency (f_t), and Maximum Frequency of Oscillation (f_{MAX}).

f_t is defined as the frequency at which the current gain falls to unity as shown in Equation 2.36. This can be expressed using H-parameters which represent the current in a system:

$$f_T : h_{21}(f_T) = 1 \tag{2.36}$$

This can also be expressed in terms of s-parameters as:

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}} \tag{2.37}$$

f_{MAX} is defined as the frequency at which Masons unilateral power gain (GU) falls to unity shown in:

$$f_{MAX} : GU(f_{MAX}) = 1 \tag{2.38}$$

This can be defined through s-parameters as:

$$GU = \frac{|S_{21} - S_{12}|^2}{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2 - |S_{12}S_{21}|^2 - S_{12}S_{21} - S_{21}S_{12}} \tag{2.39}$$

This manipulation of S-parameters allows for many important insights into device performance to be made [31].

2.4.3 Using S-Parameter Measurements for Equivalent Circuit Modelling

To perform equivalent circuit modelling; the core physics underlying the HEMT needs to be considered. The first criteria is to choose the small signal model. This has been done here by first observing a large signal model for the HEMT shown in Figure 2.5.

This large signal model consists of both extrinsic and intrinsic regions and contains two diodes in the intrinsic region. Linearising the behaviour, by taking measurements in the saturation region, the previously mentioned small signal model can be deduced, repeated here again in Figure 2.6. This has replaced each diode with a capacitor and resistor pair and replaced the large signal current source with the small signal current source, which relies on the transconductance and the angular frequency and time delay.

The equivalent circuit modelling procedure can be broken down into the following steps; extracting pad capacitance; extracting series parasitics; and extracting intrinsic parameters.

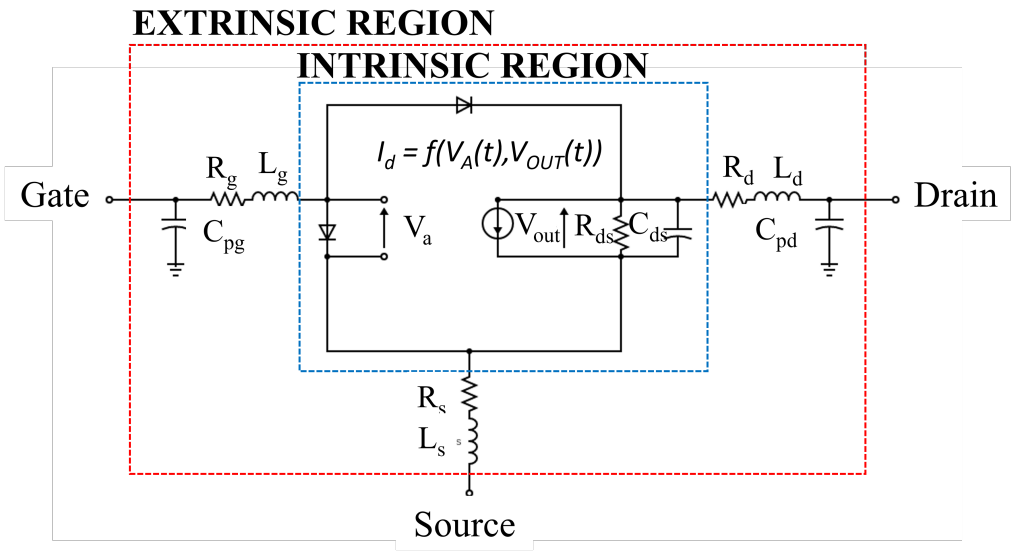


Figure 2.5: HEMT large-signal equivalent circuit model. Elements inside the red dashed lines, refer to the extrinsic parasitics, and inside the blue dashed lines are the intrinsic device parameters.

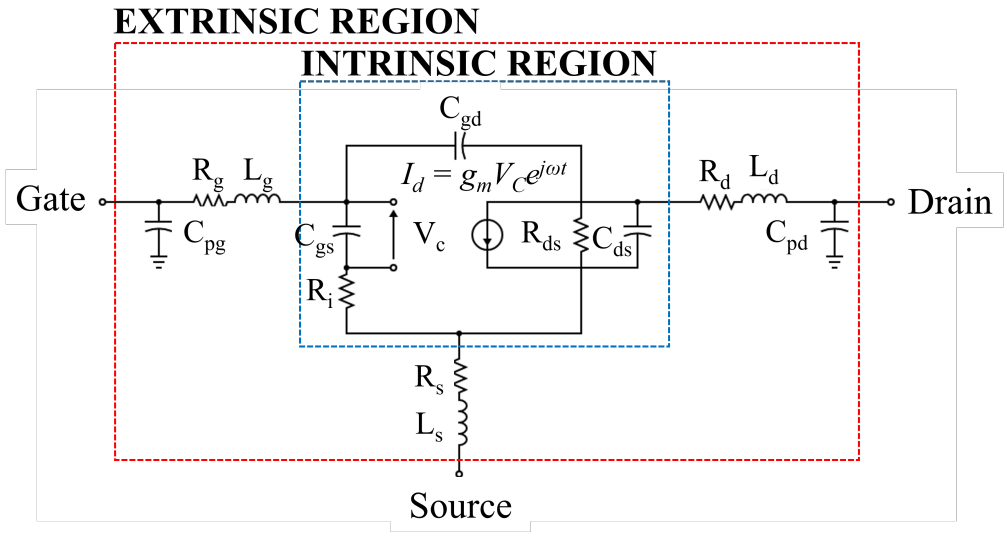


Figure 2.6: HEMT small-signal equivalent circuit model. Elements inside the red dashed lines, refer to the extrinsic parasitics, and inside the blue dashed lines are the intrinsic device parameters.

Pad capacitance

For this measurement, the device is biased in the cold-FET bias, where V_{DS} is set to 0 V. For this measurement, the device is pinched-off, where $V_{GS} << V_t$. This effectively presents HEMT as a block of semiconductor material, with pads as shown in Figure 2.7. This model can be further simplified if only low-frequency measurements are considered, as in Figure 2.8, as resistance and inductive parasitics become negligible compared to capacitance.

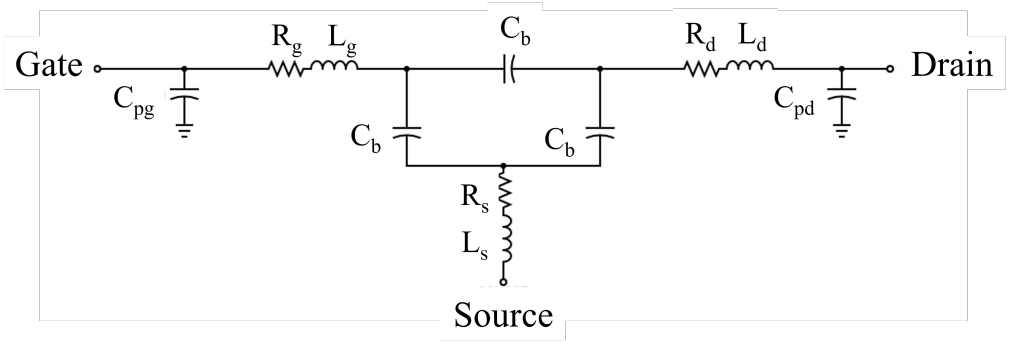


Figure 2.7: Cold-FET configurations small-signal equivalent circuit model. Y1, Y2, and Y3 are labelled to show the capacitance grouping in the π network.

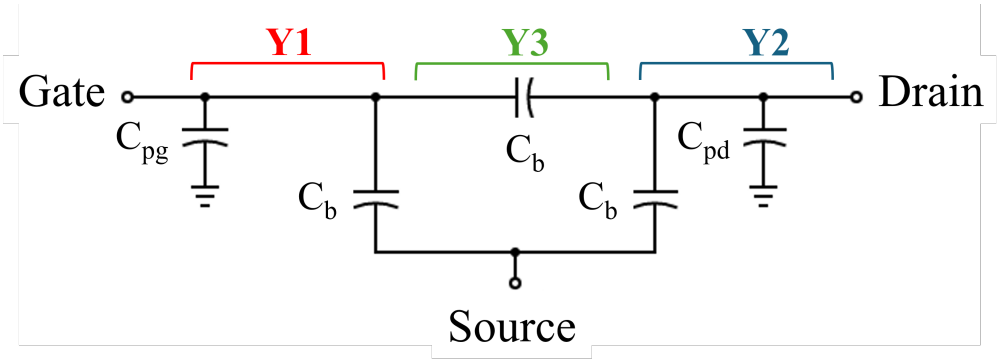


Figure 2.8: Cold-FET configurations small-signal equivalent circuit model. Y1, Y2, and Y3 are labelled to show the capacitance grouping in the π network.

With this circuit model, it can be simplified to a π network, and when the s-parameters, are converted to y-parameters the following describes the network:

$$Y_1 = Y_{11} + Y_{21} = j\omega(C_{pg} + C_b) \tag{2.40}$$

$$Y_2 = Y_{22} + Y_{12} = j\omega(C_{pd} + C_b) \tag{2.41}$$

$$Y_3 = -Y_{12} = j\omega C_b \tag{2.42}$$

These equations can then be rearranged to allow computation of the capacitance values:

$$C_b = -\frac{Y_{12}}{j\omega} \tag{2.43}$$

$$C_{pg} = \frac{Y_{11} + Y_{21}}{j\omega} - C_b \tag{2.44}$$

$$C_{pd} = \frac{Y_{22} + Y_{12}}{j\omega} - C_b \tag{2.45}$$

The pad capacitances can then be de-embedded to allow for the next set of parasitics to be extracted.

Series Parasitics

In order to extract the extrinsic resistance and inductance parasitics, the diodes in the HEMT need to be brought into conduction. This is done by applying a forward bias to the HEMT which consists of a high positive V_{GS}, whilst ensuring V_{DS} is at 0 V. During forward bias, the equivalent circuit can be represented as shown in Figure 2.9. During this measurement, it is best to use a current source for the gate, rather than a voltage source to ensure the current flow through the gate is kept constant. In this work, three bias points were used, which were 200, 400, and 600 μA/mm.

The s-parameter measurements must then be converted into z-parameters:

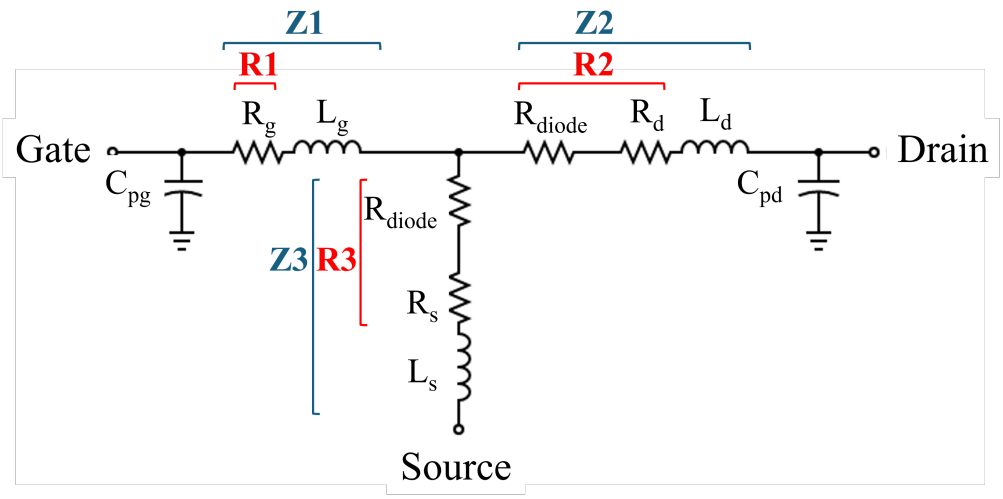


Figure 2.9: Forward bias configuration small-signal equivalent circuit model. Z1, Z2, Z3, R1, R2, and R3 are labelled to show the impedance and resistance grouping respectively.

$$Z_1 = Z_{11} - Z_{21} = R_g + j\omega L_g \tag{2.46}$$

$$Z_2 = Z_{22} - Z_{12} = R_2 + j\omega L_d \tag{2.47}$$

$$Z_3 = Z_{12} = R_3 + j\omega L_s \tag{2.48}$$

which allows the resistor and inductor values to be separated, where the resistance is the real part, and the inductance is the imaginary part of the z-parameters. This allows inductance to be directly calculated; however, for the resistance values R_2 and R_3 these represent both series parasitics R_d and R_s, respectively, along with the resistance of the diode R_{diode}.

Therefore, to extract the diode resistance, the resistance for both R_2 and R_3 should be plotted against $1/I_{GS}$. Then, by linear extrapolation of these plots, R_{diode} can be removed, as $R_{diode} = 0$ at the Y-axis intercept.

Now that the series parasitics have been extracted, they can be de-embedded to allow for the intrinsic parameters to now be extracted.

Intrinsic Device

For extracting the intrinsic parameters, the bias point is now chosen depending on the desired operating points of the HEMT. For this work, the bias points were chosen for V_{GS} = maximum g_m, with $V_{DS} = 15$ V.

At this stage of the small-signal model, we look directly at the intrinsic part of HEMT as seen in Figure 2.3. For the extraction of all of these components, the s-parameters are once again converted into y-parameters. The y-parameters can be directly related with each associated intrinsic parameters using:

$$Y_{11} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_1} + j\omega C_{gd} \tag{2.49}$$

$$Y_{12} = -j\omega C_{gd} \tag{2.50}$$

$$Y_{21} = \frac{g_m e^{j\omega\tau}}{1 + j\omega C_{gs} R_1} - j\omega C_{gd} \tag{2.51}$$

$$Y_{22} = \frac{1}{R_{ds}} + j\omega(C_{ds} + C_{gd}) \tag{2.52}$$

These can then be rearranged and substituted to extract each of the intrinsic parameters.

The intrinsic capacitances are:

$$C_{gd} = -\frac{imag(Y_{12})}{\omega} \tag{2.53}$$

$$C_{ds} = -\frac{imag(Y_{22})}{\omega} - C_{gd} \tag{2.54}$$

$$C_{gs} = -\frac{1}{imag(Y_{11} + Y_{12}) \cdot \omega} \tag{2.55}$$

next, the intrinsic resistances are:

$$R_{ds} = \text{real}(Y_{22})^{-1} \tag{2.56}$$

$$R_i = \text{real}(Y_{11} + Y_{12})^{-1} \tag{2.57}$$

Finally, it is possible to extract the intrinsic transconductance:

$$g_m = |(Y_{21} - Y_{12})(1 + jR_i\omega C_{gs})| \tag{2.58}$$

and the time delay:

$$\tau = \frac{arg((Y_{21} - Y_{12})(1 + jR_i\omega C_{gs}))}{\omega} \tag{2.59}$$

Now that all intrinsic and extrinsic parameters have been extracted, it is important to verify the model works correctly and to further tune and optimise to ensure the parameters, result in a suitable model for the HEMT over the desired frequency range [35] [32].

2.5 RF Measurement Procedure for GaN HEMTs

2.5.1 On Wafer RF Measurements

All measurements were performed on wafer using several different RF S-parameter measurement systems. An example of one system that was used is shown in Figure 2.10. The typical RF measurement system consists of the following:

- VNA or PNA: this is to handle the RF signal generation and measurement.
- DC Power Supply: this is used for the DC bias for the device.

- Bias Tees: these are used to combine the RF and DC signal on the device side, but block RF from reaching the DC power supply and DC from reaching the PNA or VNA.

- RF Range Extenders: These are optional and used to extend the maximum measurement frequency from 67 to 130 GHz. In Figure 2.10 these contain the bias tee.

- RF GSG Probes: these land on the pads on wafer to enable electrical contact for the measurement system.

- RF Cables: these are a high frequency coaxial cable that is used for the connection between the VNA, bias tees, and RF GSG probes.

- DC Cables: these are triaxial cables that run from the bias tee to the measurement system.

- Probe Station: This contains a movable chuck that holds the wafer, manipulators to move the probes with micron precision, and a microscope to view the probes and devices.

Due to the highly sensitive nature of RF measurements, it is crucial to ensure effect of all the cabling and connectors are removed from the measurements. This is done through RF on-wafer calibration.

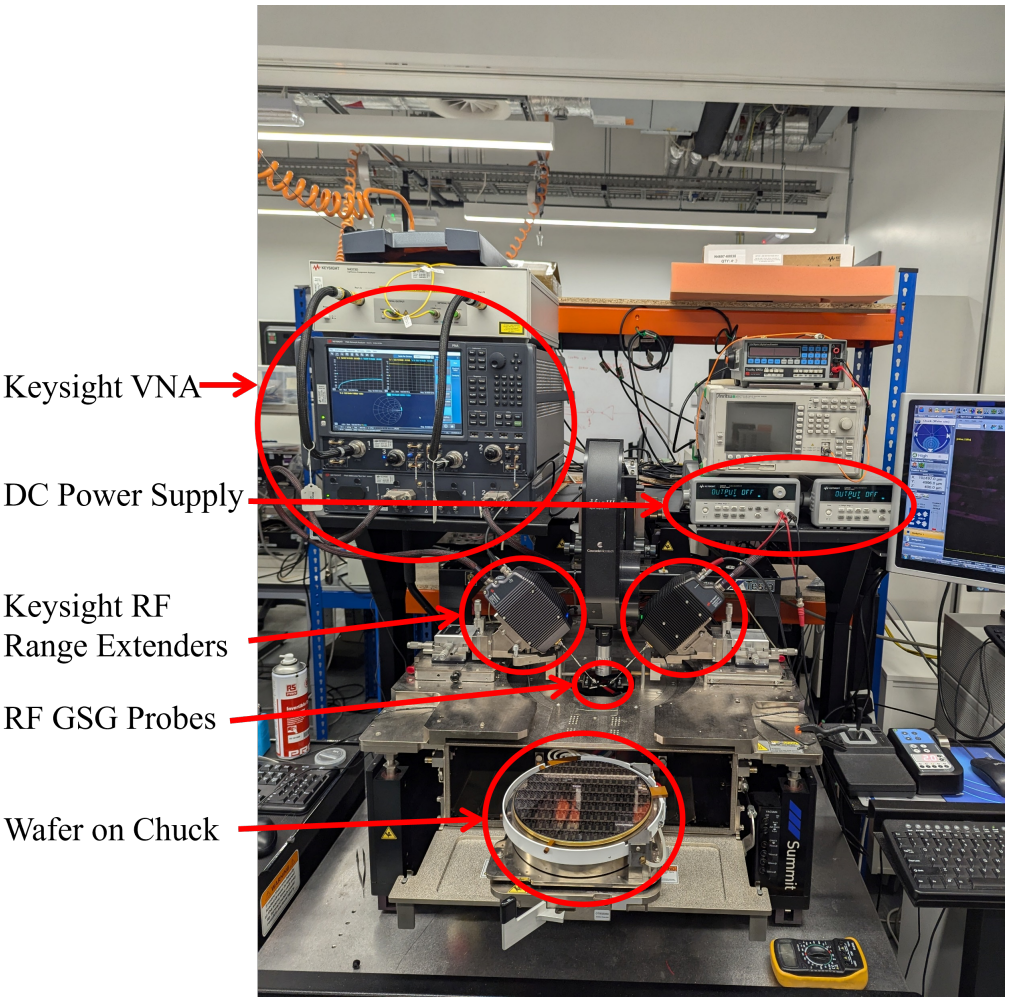


Figure 2.10: Photo of one of the RF systems used in this work, labelled to show the key system components.

2.5.2 Calibration

To ensure accurate measurements, the measurement reference plane needs to be moved from the output ports on the VNA to the probe tips. This ensures that the measurements only incudes the device, the device feeds, and measurement pads. The device feeds are coplanar waveguide (CPW) transmission lines, that connect the device to the measurement pads that the probes land on for the measurement to the device.

This probe tip calibration was performed through Enhanced Line-Reflect-Reflect-Match (eLRRM) using the MPI AC2 calibration substrate. The key structures that need to be measured for an eLRRM calibration are:

- Open: this is an open structure where the signal open resulting in theoretically infinite impedance.
- Short: this is a short where the signal is directly connected to the ground.
- Thru: this is a structure where port 1 and port 2 are directly connected through a 50 Ω transmission line.
- Match: this is a structure with a 50 ohm resistor between the signal and ground.

The eLRRM calibration technique was developed by Leonard Hayden at Cascade Microtech. The eLRRM is based on a standard eight-term error model and two-port ABCD-parameters (voltage-current cascade parameters) are used to describe the measurement configuration of the line. The objective of this calibration method is to compute the terms E_x and E_y which are the error box on port 1, port 2 including half of the line respectively, then using known standards, take the raw measurement and extract the corrected Device Under Test (DUT) behaviour. To do this, the probe tip reference plane error boxes $E_{X'}$ and $E_{Y'}$ are used to perform a measurement of the Thru standard; then they can move the reference plane to the centre of the line. In doing so the error boxes can be moved to include the

Thru standard allowing the E_X and E_Y to include everything except the DUT, as shown in Figure 2.12. It is known that only 7 of the 8 terms need to be known to extract the corrected DUT behaviour as the absolute magnitude, and the phase of the incident and reflected waves is not required just the ratios for s-parameters. The full details of the calibration technique and equations can be found in [36].

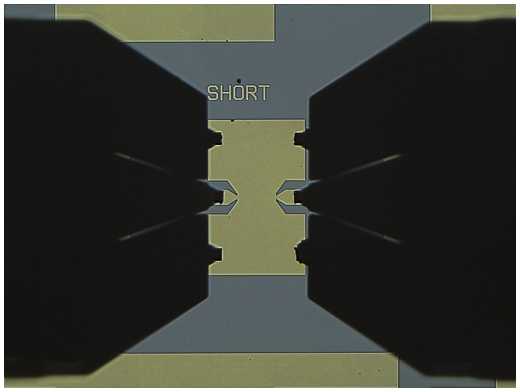


Figure 2.11: GSG probes used for an on-wafer measurement of a short.

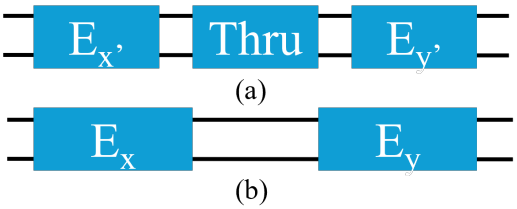


Figure 2.12: Diagram showing the error boxes that are used for the eLRRM. (a) Thru standard is measured with probe tip reference plane error boxes, (b) the reference plane is moved so the error boxes including the centre of the Thru allowing just the DUT to be measured. Figure adapted from [36] ©2006 IEEE.

2.5.3 On-Wafer De-Embedding

For some RF measurements, multi-line Thru-Reflect-Line (TRL) measurements have been performed on-wafer to allow for de-embedding of the device feeds. These measurements are taken during the measurements of the devices, which allows for TRL calibration to be applied as a post-process to eliminate substrate loss and other effects from the DUT, when performing small signal modelling, but still preserving the original measurements, for investigations into behaviour such as substrate loss.

TRL calibration is an eight-term error model similar to the eLRRM mentioned above. However, it differs through the use of uniform transmission line sections, allowing for easy implementation on-wafer, allowing for calibration to be performed on the same substrate as the DUT, which ensures minimal electrical behaviour difference. The on-wafer standards that are used for this TRL de-embedding consist of a 2x Thru, which is both feeds for the device connected together, then 1000, 1500,

and 2000 μm lines. It is important to note that these line lengths exclude the same feeds that are used for the device, to ensure the length is correct after the calibration error boxes has moved to the centre of the 2x Thru. By using these line lengths it allows for a calibration to be performed over a large frequency range. In standard TRL the calibration per line is valid for all frequencies that result in a phase shift of between 20° and 160°, whereas with multiline TRL each line is used for the entire frequency range, but on a weighted scale with more weight for the lines closest to 90°. This allows for a suitable calibration for the entire frequency range that can be used to perform the de-embedding required to develop the small-signal model. The complete details and equations on which the TRL calibration is based can be found in [37] and the exact implementation in our research group is described in [38].

Chapter 3

Characterisation and Analysis of Trapping in Gallium Nitride HEMTs

3.1 Introduction to Trapping Effects

Trapping effects remain the main obstacle to progress in GaN HEMTs. Controlling these trap states and minimising them is the key to allowing improved performance in GaN HEMTs [39]. Therefore, in order to further develop AlGaN/GaN HEMTs, an understanding of the trapping phenomena and the trapping effects is critical. This will allow for the identification of the trapping centres, the activation energy of the traps, and the spatial location of the devices. Therefore, targeted improvements to both the fabrication methods and the epi-structure growth can be performed to reduce the trapping effects in AlGaN/GaN HEMTs.

Defects and impurities introduce localised trap states in semiconductors. GaN is known to contain a large density of defects and dislocations as a result of growth on non-native substrates. It is also understood that ionised donor states are located at the surface of the AlGaN barrier. The localised states can act as charge-trapping

centres in the structure of semiconductor devices, resulting in a diminished device performance.

The main locations for trap states are; surface traps between the passivation and AlGaN barrier; traps in the AlGaN barrier; interface traps at the AlGaN/GaN heterojunction; channel traps in the GaN channel layer; buffer traps in the buffer layer; and substrate traps at the interface between the buffer and substrate. These locations are shown in Figure 3.1. These trap states can be identified by their properties, such as charge state, ionisation energy, and the capture cross section. These can be obtained by analysing the emission rate of the trapped charge [40].

3.1.1 Trap Charge States

Traps with energy levels close to the conduction band are described as donor traps. These are traps that are likely to release an electron into the conduction band during trap emission. Traps with energy levels close to the valence band are described as acceptors and are more likely to trap an electron from the valence band, leading to the production of a hole. These traps occur both on the surface and in the epitaxial bulk layers [41]. When these traps are empty, they maintain a neutral charge, but in the filling process, they can become negatively charged in the case of a donor trap or positively charged in the case of an acceptor trap [42].

3.1.2 Trap Ionisation Energy

Ionisation energy, is the minimum required energy to release the electron from the trap, and it is equated to the energy level of the trap. The ionisation energy can be determined by the relationship between the time it takes for the trap to release, the trap time constant, and the temperature. Due to this relationship, it is possible to deduce the trap ionisation energy through measurements of the trap time constant at various temperatures and using an Arrhenius plot. Traps can be considered either shallow or deep. Shallow traps have a low trap ionisation energy, whereas deep traps have a large trap ionisation energy.

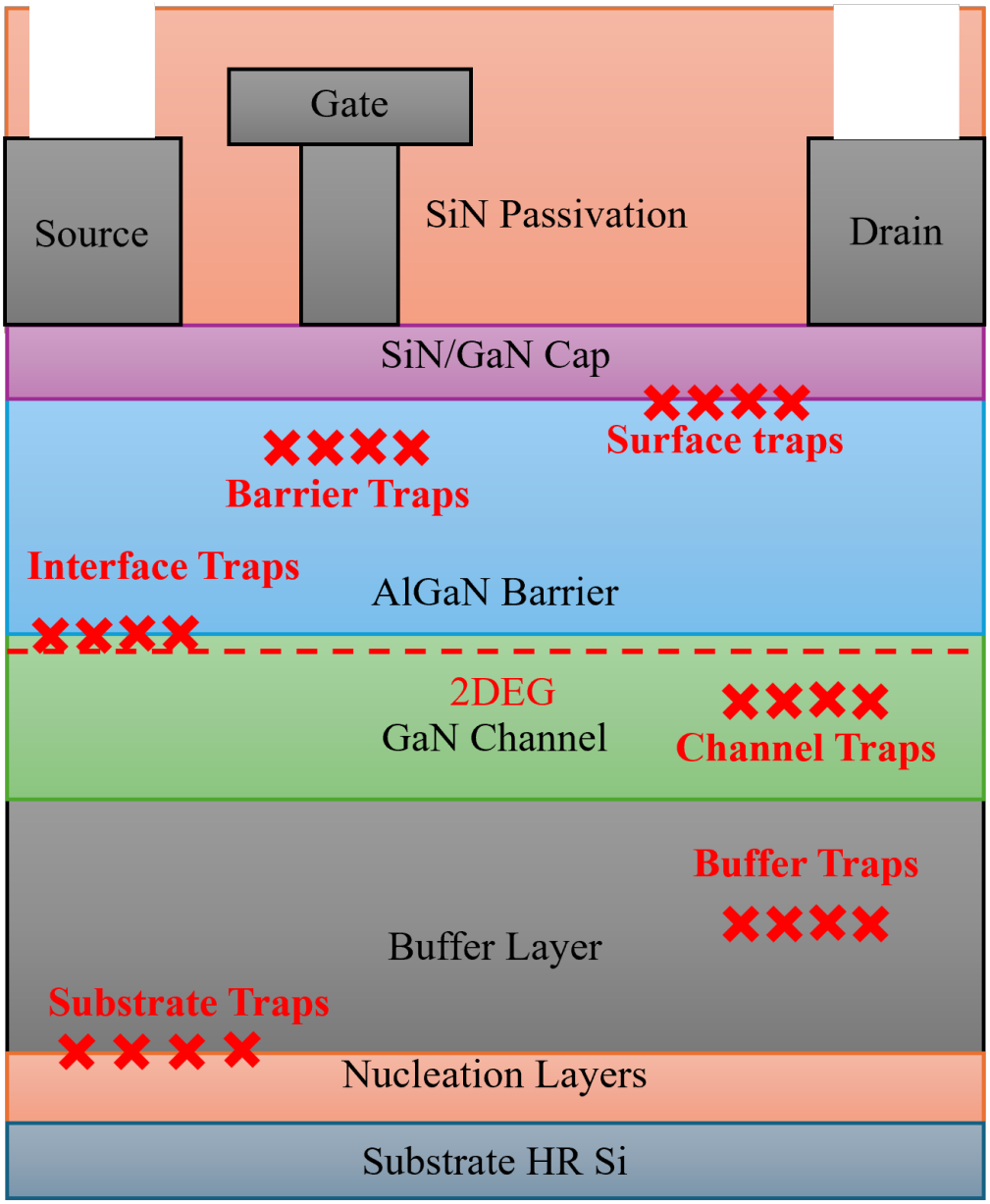


Figure 3.1: Trapping locations in AlGaN/GaN HEMTs.

3.1.3 Trap Capture Cross Section

This refers to the effective area surrounding a trap in which an electron or hole passes through it, which will have a high probability of being trapped.

The capture cross section has a direct relationship with the time constant of a trap, as a larger capture cross section results in a shorter time constant to both fill and release a trap. If the capture cross section is very small, it will result in a longer trap time constant, as the time taken to fill and release will increase [40].

3.2 Trap Types and Locations

3.2.1 Surface State Traps

Surface-state trapping effects were originally thought to be unavoidable in the AlGaN/GaN material system, because of the strong polarisation fields.

In the previous section, the formation of the 2DEG was described; however, for the 2DEG to form, donor states on the surface of the AlGaN barrier are required. These donor states donate their electrons to the 2DEG, and in doing so, this creates a positive sheet charge of ionic donor states. The effect of these surface states leads to an extension of the depletion region in the lateral directions. This indicates that there is an additional negative charge on the surface [39]. This effect leads to the formation of a virtual gate that results in degraded RF performance in AlGaN HEMTs. In the AlGaN barrier traps end up scrambled, since the Fermi level is placed above the surface trap index. This is due to the thin AlGaN barrier, which allows traps to easily move to the channel through the polarisation process in the AlGaN/GaN heterojunction [43]. The AlGaN barrier layer has been considered a weak point in the epi-structure since the excessive intrinsic and extrinsic strain that is induced will result in defects that cause degradation of the 2DEG, and lead to the formation of trap states [44]. There are several areas where traps can arise at the surface; these are dangling bonds, surface growth defects, processed induced surface damage, and foreign contaminants [45]. An example of a contaminant is oxygen,

which can form trapping states on the AlGaN barrier [46] [47].

However, despite these surface trap effects, the effects can be mitigated by passivating AlGaN/GaN HEMTs [48], resulting in a successful suppression of surface trap effects.

3.2.2 Bulk / Buffer Traps

Native buffer traps are introduced during epitaxial growth and, in order to reduce these traps, the growth parameters must be tightly controlled [45].

Dopants are required in the buffer to reduce buffer leakage and punch-through currents. They also enhance the carrier confinement in the 2DEG and increase the breakdown voltage. The use of these dopants leads to the creation of acceptor traps, which, while creating a highly resistive GaN buffer, results in increased trapping effects [49]. It has also been found that as the density of the buffer traps increases, the leakage of the buffer decreases [50].

Iron (Fe) acts as a deep acceptor and typically behaves as an electron trap; carbon (C) is also a deep acceptor, but it typically behaves as a hole trap. This explains why C doping leads to traps with time constants greater than Fe doping in the buffer [51]. However, despite the lower time constant traps due to Fe doping, when compared to C, there are several disadvantages. Fe is not compatible with the CMOS process due to its effect of a contaminant, which leads to Foundries rejecting it. It also has a memory effect, making the doping profile difficult to control with precision when compared to Carbon. Therefore, while C produces larger trapping effects, it is currently the preferred method for buffer doping [52].

The inclusion of the AlGaN back barrier has been shown to reduce buffer trapping effects whilst providing high electron confinement. Due the increased band gap of the back barrier, the buffer traps can effectively be isolated from the channel [53]. This is discussed in more detail in Chapter 8.

There is currently research on the growth of AlGaN/GaN epi-stacks using buffer-free growth to reduce these trapping effects. This has been observed to lead to

reduced bulk trapping [54].

3.2.3 Impurity Traps

Impurity traps occur where there is an impurity in the lattice structure. These impurities can come from contamination or be inserted for a specific purpose, such as the Fe and C dopants used for the buffer layer. In both of these cases, it will lead to impurity traps [55]. These lead to the formation of point defects, where either the Ga or N form a bond with an impurity. This leads to a gallium vacancy (V_{Ga}) or a nitrogen vacancy (V_N). The formation of these states leads to V_{Ga}-*impurity* and V_N-*impurity* bonds such as V_{Ga}-O, V_N-Mg, or V_n-Si-H. The formation of *impurity-impurity* complexes is also possible such as Mg-H [19].

3.3 The Effect of Impact Ionisation on Trapping

Impact ionisation in the channel has multiple effects on device behaviour. For impact ionisation to occur, electrons must enter a large electric field where they pick up significant energy. This leads to the formation of hot electrons, which are electrons that have significant kinetic energy. These electrons will then collide with an atom in the channel or buffer, resulting in the release of an electron into the conduction band and a hole in the valence band. Therefore, after impact an atom has been ionised, and now there are 2 electrons in the conduction band, the original electron and the released electron, and 1 hole in the conduction band [56].

Depending on where these electrons and holes end up in the structure trap states will result in either the creation of a trap state, or can result in assisting trap emission or mitigation of trap effects.

3.3.1 Impact Ionisation and the Formation of Traps

One effect that has previously been attributed to the formation of trap states through impact ionisation is the kink effect. This effect manifests itself when the holes that

are created through impact ionisation are attracted to the gate and the source, where they accumulate, resulting in the decrease of the potential barrier between the source and the channel, resulting in an increase in drain conductance. The electrons themselves do not contribute to this kink effect, as they are just collected by the drain [56].

Breakdown in devices in the off-state can also be attributed to impact ionisation. At drain high voltages whilst the device is pinched-off impact ionisation can occur, which results in the formation of positive holes; if these holes then drift into the buffer, they will be captured by neutral deep donors. This results in a lower barrier, which increases the buffer leakage current and will result in a breakdown event as V_{DS} continues to increase [51].

3.3.2 Impact Ionisation Reducing Trap Effects

Impact ionisation can lead to the reduction in trap effects through either enabling trap emission or counteracting the effects of the traps.

An example of impact ionisation directly releasing traps is where the hot electrons collide with traps that have already captured an electron. This results in the release of the electron emission from the trap [57].

It has been shown that through impact ionisation, the current collapse effect is reduced, because of the generation of the holes. These holes drift to the buffer, where they are captured by neutral deep donors on the source side. This results in the channel current increasing at a rate greater than that of relying on electron emission from the bottom of the gate [51].

3.4 De-trapping methods

De-trapping of trap states in GaN HEMTs, can occur due to multiple different reasons. The most common to use in terms of trap energy level analysis is thermally activated ionisation, where the time constant of the trap decreases as the temper-

ature of the device increases. This relationship between the trap time constant and temperature is taken advantage of through Arrhenius plots to extract trap-time energy levels.

The typical relationship between the trap ionisation energy and thermally activated ionisation is more complicated in GaN HEMTs because of the high electric fields. The presence of these electric fields has an impact on the trap time constant. This leads to additional effects that result in de-trapping. These consist of energy band lowering, direct electron tunnelling, and phonon-assisted tunnelling. These effects are shown in Figure 3.2 taken from [40]. The lowering of the energy band can be attributed to the high electric fields present in AlGaN/GaN HEMTs.

Direct tunnelling is where an electron tunnels through the energy barrier, enabling it to escape a trap without the requirement of any external energy. Direct tunnelling is the prevalent de-trapping method at low temperature.

Phonon-assisted tunnelling occurs when the band is sufficiently tilted due to a strong electric field. The trapped electron absorbs energy from the lattice structure, and then tunnels through a thinner barrier to a higher energy state [40].

3.4.1 Poole Frenkel Effect

In equilibrium, the system of trapping centres will maintain a constant density of localised electrons, with a balance between the emission and capture process. With the assumption that the emission process is thermally activated, the emission rate from the deep levels in the semiconductor band gap (e), is related to the ionisation energy E_i by the Arrhenius equation:

$$e = AT^2 \exp\left(-\frac{E_i}{kT}\right) \tag{3.1}$$

where A is the pre-exponential factor, T is the temperature, and k is Boltzmann's constant.

However, in the presence of an electric field, the efficiencies of the capture and emission processes change, leading to a new equilibrium with a change in the number

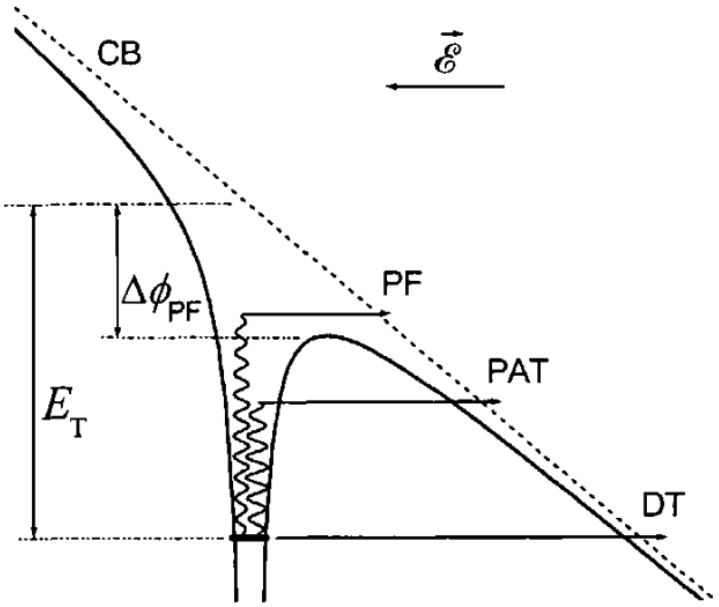


Figure 3.2: "Energy diagram of the trapping centre in the presence of an electric field. Arrows indicate the possible mechanisms of electron emission: thermal ionisation over the lowered barrier (PF effect), direct tunnelling (DT) into the conduction band (CB), and phonon assisted tunnelling (PAT)." Reproduced from [40], with the permission of AIP Publishing

of trapped electrons. In Figure 3.2 the effect of the electric field is shown for a trap described by the Coulomb long-range potential. In the direction of the applied electric field, the potential barrier is lowered, resulting in electrons now requiring less energy to escape the trap. This mechanism of the electric-field-assisted thermionic emission is known as the Poole-Frenkel effect.

In this situation, the potential barrier will decrease by an amount ($\Delta\phi_{PF}$) that is proportional to the square root of the applied electric field (F):

$$\Delta\phi_{PF} = \left(\frac{q^3}{\pi\epsilon}\right)^{1/2}\sqrt{F} = \beta\sqrt{F} \tag{3.2}$$

where q is the charge of an electron, ϵ is the dielectric constant of the material, β quantifies how much the potential barrier for the is reduced in the presence of an electric field.

By substituting in the ionisation energy, the effect of the electric field can be applied to the electron emission rate:

$$E_i(F) = E_i(0) - \beta\sqrt{F}, \tag{3.3}$$

where $E_i(0) = E_T$ is the binding energy of the electron in the trap when no electric field is applied.

Due to this Poole-Frenkel effect when mathematically evaluated, it shows that the energy levels located in regions of high electric field will be smaller than if no electric field is applied. This indicates that the rate of election emission from a trap is strongly enhanced by the electric field:

$$e(F) = e(0)\exp\left(\frac{\Delta\phi_{PF}}{kT}\right) \tag{3.4}$$

and the emission rate will increase exponentially with the square root of the electric field.

Taking the effect of this band bending and the Poole-Fenkel effect the equation can be modified to:

$$e(T,F) = AT^2\exp\left[-\frac{E_T - \Delta\phi_{PF}(F)}{kT}\right] \tag{3.5}$$

where the field-dependent activation energy is considered.

However, the above equations are a simplified representation that only accounts for a single dimension. Since most trapping centres are likely point defects, the 3-dimensional nature needs to be taken into account. The representation of the emission rate supported by an electric field in a spherical case is:

$$\frac{e}{e_0} = \left(\frac{kT}{\beta\sqrt{F}}\right)^2\left\{1 + \left[\left(\frac{\beta\sqrt{F}}{kT}\right) - 1\right]\exp\left[\frac{\beta\sqrt{F}}{kT}\right]\right\} + \frac{1}{2}, \tag{3.6}$$

where e_0 represents the emission rate in the absence of an electric field.

However, when comparing the results found through the 1D and 3D models, it was found that in high electric fields the 1D model approximation is sufficient to determine the trap energy level, without the need for any corrections.

Due to the band bending that occurs and the Poole-Frenkel effect, the probability for the trapped electrons to escape into the conduction band by other methods is also increased. Therefore, Equation 3.1 does not capture all of the physical effects that are occurring. However, through a careful selection of the measurement temperature, specific mechanical methods can be targeted [40].

At low temperatures, the dominant de-trapping method is direct tunnelling, due to its independence on temperature. As the temperature increases, the dominant de-trapping method shifts to phonon-assisted tunnelling, before finally being dominated by pure thermal ionisation, which is most efficient at elevated temperatures, at which point Equation 3.1 accurately describes the emission rate for trapped electrons [40].

3.5 Trap Effects

3.5.1 Gate-lag and Drain-lag

Gate-lag describes the slow transient response of the drain current when the gate voltage is changed. Drain-lag describes the slow transient response in the drain current when the drain voltage is changed. Both of these transient delays in I_{DS} result in current collapse in high-frequency operation.

Gate-Lag is attributed to trap states near the 2DEG channel. This mainly consists of surface trapping effects, which can be mostly mitigated through surface passivation. However, bulk traps have also been reported to have an impact that cannot be mitigated by surface passivation [58].

Drain-lag is mainly caused by traps in the GaN channel and the buffer and remains a significant issue in AlGaN/GaN HEMTs due to the presence of native defect and impurity traps in GaN [59].

3.5.2 Virtual Gate Effect

Because of the presence of negative charge on the surface, the surface potential becomes negative, leading to an increase of the depletion region. This effect acts

like a second gate connected in series with the real gate. The real gate potential is controlled by applying a gate bias, whereas this virtual gate is controlled by the total amount of trapped charge in the gate drain access region. This effect is shown in Figure 3.3 taken from [39].

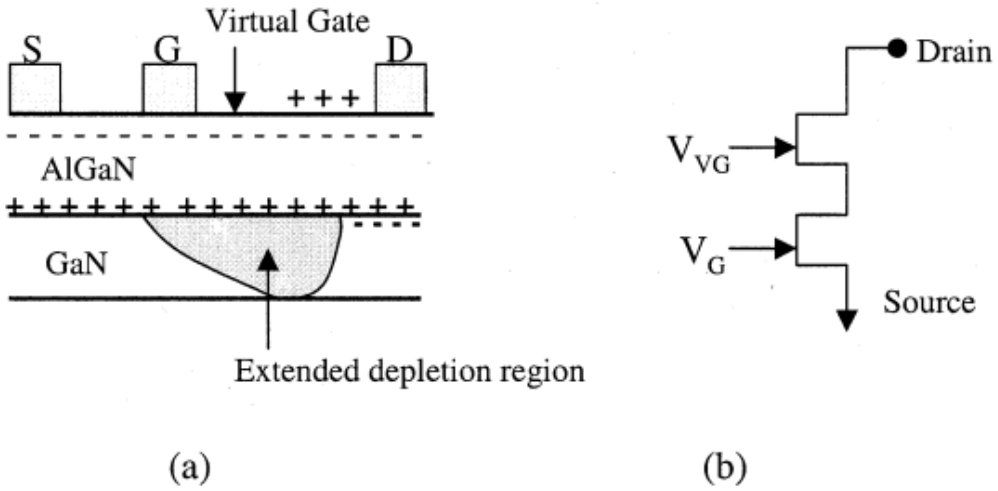


Figure 3.3: "Model of the device showing the location of the virtual gate and schematic representation of the device including the virtual gate." Taken from [39], ©2001 IEEE

Due to the effect of the virtual gate, when bias points are switched, as is typical in a power amplifier operation, the virtual gate potential has to change. This rate of change is restricted due to the time constant of the trap. This de-trapping time results in a transient time period in which the output current is less than during the steady state [39]. Therefore, this virtual gate effect can be directly related to current collapse [60].

3.5.3 Current Collapse

This is the effect in which the output current is reduced compared to the expected current. This, along with an increase in knee voltage, results in a decrease in output power at RF frequencies, and this can be referred to as DC-RF dispersion, current compression, or current slump [39]. This can occur due to both surface-state traps "gate-lag", or traps from the bulk-epistructure "drain-lag". One of the main attributes that cause this is the charging of traps, through hot electrons being

generated. This current collapse translates into a reduction in output power and power-added efficiency (PAE), resulting in lower-efficiency devices [61]. Therefore, this trapping effect results in reduced device efficiency and linearity.

3.5.4 Knee Walkout

Unlike current collapse, where the maximum current in RF is reduced compared to the DC current, knee walkout manifests itself as a decrease in the minimum drain voltage under RF drive compared to DC. This occurs due to an increase in R_{on} during RF operation. This has been directly attributed to trap states in the buffer [62].

Therefore, characterisation of the R_{on} shift allows a good indication of the linearity and efficiency of the device in RF operation.

3.5.5 Kink Effect

A trapping phenomenon previously observed is a dynamic shift in threshold voltage, leading to a kink effect that occurs in the output ($I_{DS}-V_{DS}$) characteristics as shown in Figure 3.4. This is observed as a sudden increase in I_{DS} during a V_{DS} output sweep that leads to a higher saturation current I_{DS}. This kink effect in GaN HEMTs leads to a decrease in transconductance and an increase in output conductance. The kink effect typically leads to a hysteresis in the output characteristics, with kink occurring when V_{DS} is swept from low to high and the kink disappearing when V_{DS} is swept from high to low. The magnitude of the kink will also increase as the maximum V_{DS} increases [63]. This results in a degradation in GaN HEMT performance, as seen in [64]. However, it is important to note that the configuration of the DC-IV measurement system plays an important role in the identification of this effect, as long integration time is required to observe this effect [65] [66].

This kink effect has been reported in multiple papers with many different speculations on the origin. In [67] it was identified that the impact ionisation of shallow traps was the main cause of this kink effect. In [68] an investigation into the impact

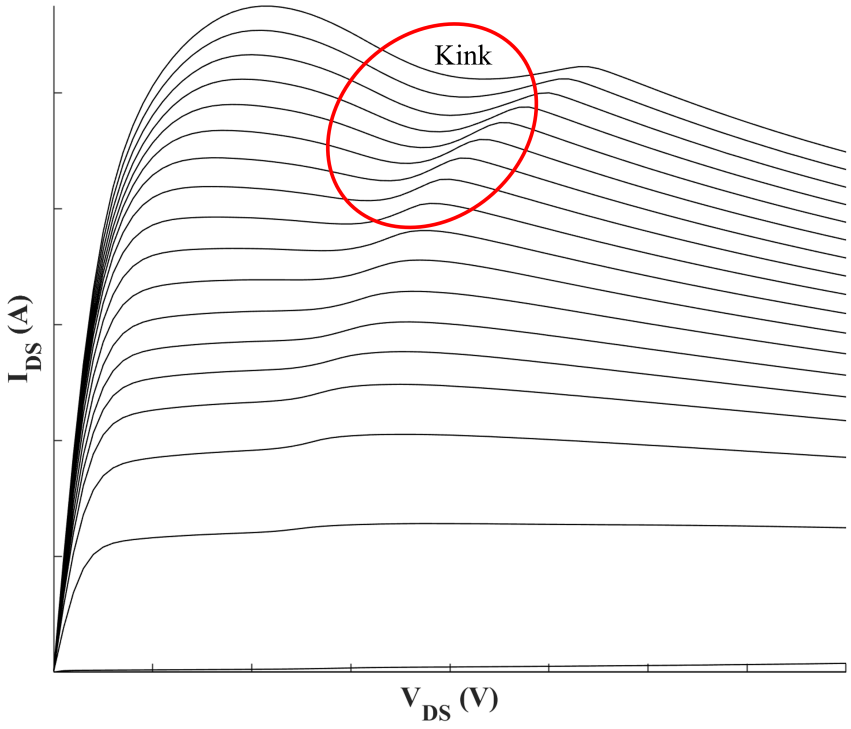


Figure 3.4: Kink effect in the output characteristics of a device.

of temperature variations on the kink and the effect of this impact ionisation found that there is a non-monotonic behaviour of the kink when related to temperature, showing that there is a peak at 75 °C where the kink effect is maximised.

However, in [69], it was previously found that it was due to deep traps in the GaN buffer. During these measurements, gate and drain pumping was performed before sweeping the V_{DS}, indicating that when HEMT is pumped in the off state the kink effect is negligible. This indicates that the traps responsible for the kink effect are empty after resting in the off-state. Therefore, it can be concluded that there is a requirement for a high V_{DS} channel current to fill these traps.

In [63] it was found that this kink effect occurs due to long time constant traps, with a de-trapping time constant of greater than 1 s. As this is significantly longer than the measurement time, it leads to a negative charge under the gate that shifts V_t positive, leading to a decrease in I_{DS}, until the gate drain bias (V_{GD}) increases beyond a specific value, which in the case of this paper is 5 V, where the emission rate of electrons from the donar states in the AlGaN increases exponentially due to

the Poole-Frenkel effect, lowering the activation of the trap energy level to almost zero. This results in the de-trapping time becoming shorter than the measurement time causing this kink effect. When the device is ramped down from V_{DS} high to low, the high V_{DS} ensures that the de-trapping time is kept short so that the de-trapped state is always measured. In addition, when V_{DS} is low, the electric field is insufficient to cause trapping, so the I_{DS} measured for the whole sweep down is high. The kink effect was determined to be attributed to donor traps in AlGaN because the emission time is more sensitive to V_{GS} than to V_{DS}. This work also indicates that these traps are unlikely to be from the C doping in the barrier, as the Poole-Frenkel effect would result in increased negative charge build-up, which is contrary to the findings here. Impact ionisation can also be ruled out because of the long time constant, as impact ionisation is a nearly instantaneous process, unlike what is observed with the kink effect.

3.5.6 V_t shift and V_t Hysteresis in MIS-HEMTs

The threshold voltage of the MIS-HEMT devices is an important factor when determining the performance of the devices. An issue with MIS-HEMT devices is a large V_t shift with large forward gate bias, which is caused by defect trap states induced by the dielectric/III-N interface. These trap states are typically deep acceptor traps [70].

3.6 Advanced Characterisation and Analysis Techniques for Identification of Trapping Effects in GaN HEMTs

3.6.1 Pulsed-IV

Pulsed-IV characterisation is a well established measurement technique to observe the trapping effects on both gate and drain-lag. Through the selection of quiescent

(Q) bias points, and non-quiescent (NQ) bias points, it is possible to observe the trapping effects, and differentiate gate-lag from drain-lag.

Q points refer to the bias at which the device is held before the measurement. NQ points refer to the bias that is applied to the device during the measurement. For this work, the Q points will be notated as (QV_{GS}, QV_{DS}).

Due to the nature of this technique being a pulsed measurement, there is a related pulse width and duty cycle. The pulse width refers to how long the device is held at the NQ bias for measurement, and the duty cycle refers to the percentage of time the device is held at the NQ bias. For this work 1 μs pulse widths were used with a duty cycle of 0.01 %. This means that for each measurement taken at the NQ point, the device was held at the Q points for 10,000 μs. This allows for the self-heating effect to be minimised and ensures that the traps are either empty or full depending on the measurement requirement.

There are three sets of Q point variations that are used:

1. Cold FET: Here, the Q points are set to ($QV_{GS} = 0$, $QV_{DS} = 0$). Due to these bias points, when pulsing to the NQ points for measurements, the gate bias is pulsed down and the drain bias is pulsed up. This results in the trap states filling. Due to the fact that trap states fill extremely fast, it can be stated that the trap state during this measurement is the same as the NQ bias. Therefore, pulsed measurements with Q points of (0,0) result in a measurement of the AlGaN/GaN HEMT in the absence of any trap effects.

2. Gate-Lag: Here, the Q points are set to ($QV_{GS} << Vt$, $QV_{DS} = 0$). Due to these bias points, when pulsing to the NQ points for measurements, the gate bias is now pulsed up, whilst the drain bias is also pulsed up. This results in the trap states under the gate (surface traps) emptying, whilst the traps related to the drain are filling. Due to the slow speed for the traps to empty, this allows the traps dependent on the gate bias to remain in the same state they were in at the Q point. Therefore, this measurement has enabled the gate-lag trap effects to be observed, whilst not observing any effect on device

performance from the drain-lag trap effects.

3. Drain-Lag: Here, the Q points are set to ($QV_{GS} << Vt$, $QV_{DS} = V_{DSHigh}$). Due to these bias points, when pulsing to the NQ points for measurements, the gate bias is pulsed up, whilst the drain bias is now pulsed down. This results in the trap states under the gate (surface traps) emptying, and the traps related to the drain (buffer traps) are also emptying. Once again, due to the slow speed for the traps to empty, this allows the traps dependent on the gate bias and drain bias to remain in the same state they were in at the Q point. Therefore, this measurement has allowed for both the gate-lag trap and the drain-lag trap effects to be observed.

Through comparison of these measurements, it is possible to isolate the gate-lag and drain-lag effects. When determining the effect of the gate-lag trap effects, the cold FET measurement and the gate-lag measurement can be compared. Therefore, when trying to determine the effect of the drain-lag effects, a comparison between the gate-lag and drain-lag pulse measurements can be made.

Through these measurements, it is possible to quantify the current collapse effect and the shift R_{on} due to gate-lag trapping effects and drain-lag trapping effects [71].

3.6.2 Drain Current Transient Spectroscopy

Drain Current Transient Spectroscopy (DCTS) involves the application of a large positive V_{DS} bias, large negative V_{GS} bias, or both to fill the trap states. Once these trap states have been filled, the bias on both the gate and drain will return to steady state, and the change in I_{DS} over time is measured as it returns to steady state current.

The main limitation of DCTS is that the physical location of traps is difficult to determine because of the limited spatial sensitivity. This can be overcome to an extent through the use of multiple different trap filling bias conditions. This allows the trap states in specific regions of the epi-structure to be targeted.

- V_{GS} constant, V_{DS} pulsed high: This allows for drain-lag to be observed as all of the trap states related to the drain bias are filled during this trap-filling bias.

- V_{GS} pulsed $<< V_t$, V_{DS} pulsed high: This causes the surface trap states to fill, which allows the traps under the gate and in the channel to be observed. Due to the V_{DS} also pulsing high, this will also include the drain-lag trapping effects exposed in the above bias conditions, so by comparison of the traps exposed in both methods, the traps causing gate-lag and drain-lag can be individually determined.

The other issue with DCTS is that it is unable to detect trap states with energy levels above 1 eV [19].

Calculating Trap Energy Level and Trap Cross Sections From DCTS Measurement

Current transients are affected by two major factors: self-heating and trapping effects. This is due to self-heating that results in a decrease in I_{DS}. Trapping effects also cause a decrease in I_{DS} due to the effect of traps capturing electrons or holes, but also result in an increase in I_{DS} due to traps releasing captured electrons or holes. Therefore, if the self-heating effect is removed, it is possible to extract detailed information on these trapping effects by observing this transient behaviour.

The I_{DS} transient involves multiple trapping and de-trapping processes, which all decay at an exponential rate with respect to time. Therefore, the transient drain current can be described by:

$$I_{\mathrm{DS}}(t) = \sum_{i=0}^{n} \Delta I_{\mathrm{i}} \exp\left(-\frac{t}{\tau_{\mathrm{i}}}\right) + I_{\infty}, \tag{3.7}$$

where, $I_{\mathrm{DS}}(t)$ represents the transient drain current where, t is the time, τ_{i} is the time constant of the trap, i refers to the i-th trap, n refers to the number of traps with different time constants, ΔI_{i} is the corresponding trap current coefficient, and

I_∞ is the current in steady state.

The assumptions made for this mathematical definition have been shown to fit the experimental results well. However, the next step is to find the time constants of all the traps. This relies on identifying all of the transient responses that occur in the I_{DS} during the recovery period after the pulse.

The first stage is to define a logarithmic variable for time due to the large variations in time constants between different traps:

$$z = \ln t. \tag{3.8}$$

The time constant spectrum can then be expressed as:

$$\Delta I(z) = \lim_{\delta z \to 0} \frac{\text{magnitudes related to the time constants between z and } z + \delta z}{\delta z} \tag{3.9}$$

where $\Delta I(z)$ is the spectrum of time constants.

Now $I_{\mathrm{DS}}(t)$ can be expressed as:

$$I_{\mathrm{DS}}(t) = \int_{-\infty}^{\infty} \Delta I(\tau) \left[\exp\left(-\frac{t}{\exp(\tau)} \right) \right] d\tau + I_\infty. \tag{3.10}$$

Using Equation 3.8 the drain current transient can be expressed through:

$$I_{DS}(z) = \int_{-\infty}^{\infty} \Delta I(\tau) \left[\exp\left(-\exp(z - \tau) \right) \right] d\tau + I_\infty. \tag{3.11}$$

Due to the nature of this as a convolution-type integral equation where $\Delta I(\tau)$ is the unknown, both sides can be differentiated with respect to z:

$$\frac{d}{dz} I_{DS}(z) = -\int_{-\infty}^{\infty} \Delta I(\tau) \left[\exp(z - \tau - \exp(z - \tau)) \right] d\tau. \tag{3.12}$$

Now, since this is still a convolution-type differential, this function is required:

$$W(z) = \exp(z - \exp(z)). \tag{3.13}$$

Applying this to Equation 3.12, allows for $\frac{d}{dz}I_{DS}(z)$ to be expressed as:

$$\frac{d}{dz}I_{DS}(z) = -\Delta I(z) \otimes W(z) \tag{3.14}$$

here $\otimes$ is the convolution operation symbol.

Rearranging for $\Delta I(z)$ gives:

$$\Delta I(z) = \left(-\frac{d}{dz}I_{DS}(z)\right) \otimes^{-1} W(z) \tag{3.15}$$

This method of calculating the numerical differential for the I_{DS} transients is all based on [72].

At this point, deconvolution is required to calculate all of the time constants for each trap. The Bayesian deconvolution method was chosen due to its ability to filter out measurement noise. The equations used to implement the Bayesian deconvolution can be found in [73] [74] [75].

This method has been successfully implemented and Figure 3.5 shows it working on a DCTS measurement performed on an AlGaN HEMT.

Now that the trap energy constants have been extracted, the energy level and cross-section of the traps can be derived through Arrhenius plots, and the equation:

$$\ln(\tau_n T^2) = -\frac{E_a}{kT} + \ln(\sigma_n \gamma_n) \tag{3.16}$$

where the trap time constant is τ_n, σ_n is the trap cross section, γ_n represents the density and thermal velocity of electrons, E_a is the trap activation energy, k is the Boltzmann constant, and T is the temperature.

An Arrhenius plot is shown in Figure 3.6, with the results of a test DCTS measurement that was performed. Through linear extrapolation the trap energy level, and trap cross section can be calculated.

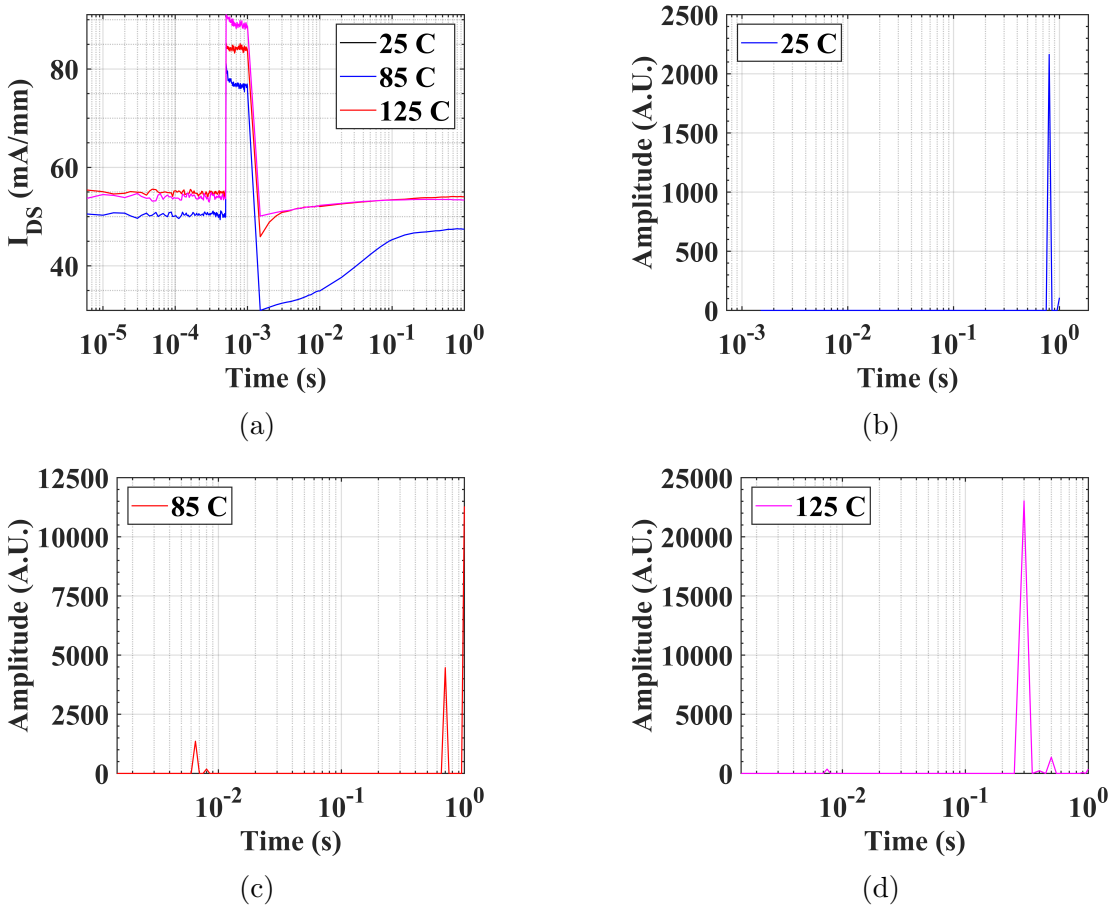


Figure 3.5: (a) Example Drain Current Transient Spectroscopy (DCTS) measurement; and trap time constants extracted after differentiation and Bayesian deconvolution at (b) 25 °C; (c) 85 °C; (d) 125 °C

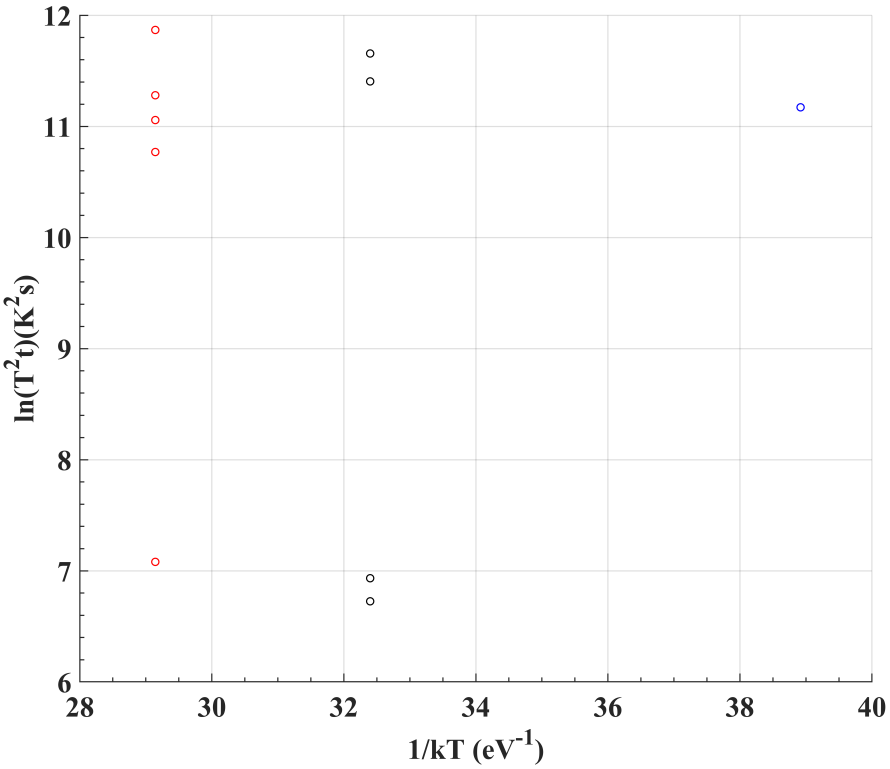


Figure 3.6: Example Arrhenius plot. Here each point refers to a trap time constant. By linear extrapolation of each trap time constant, it is possible to derive the trap energy level and the trap cross section.

3.6.3 Alternative Trap Characterisation and Analysis Techniques

There are numerous alternative trap characterisation methods, each with advantages and disadvantages. Several of these have been summarised in the following.

Low Frequency Output Admittance Measurements (Y-parameters)

This measurement technique characterises traps by measuring the device s-parameters, at very low frequencies ($<$ 10 MHz). These measured s-parameters are then converted into y-parameters, where there is a peak in the admittance at a specific frequency. This peak will shift as the temperature increases, allowing for an Arrhenius plot to be drawn, allowing for extraction of the trap energy level and capture cross section.

This method has the benefits of high dynamic range and fast measurement speed, but it is highly limited in the ability to determine anything other than the trap energy level and capture cross sections.

Low Frequency Leakage Noise

This measurement technique measures the noise signal generated at low frequencies ($<$ 1000 Hz), which reflects the distribution of charge and energy levels in a device. In AlGaN/GaN HEMTs, the presence of traps affects the leakage and conductivity of the device, so that when a small signal is applied, a small current noise is generated by these traps. Through the analysis of these noise signals at multiple different frequencies, the time constants can be extracted for the traps. Then repeating these measurements at different temperatures allows for an Arrhenius plot to be drawn, allowing extraction of the trap energy level and cross section.

The issue with this method is that it is unable to quantify the density of traps or derive their spatial position. However, it does not require high bias points, so this measurement will not result in degradation to the measured device, and it can be applied to small area devices.

3.7 Fabrication Techniques to suppress trapping effects

3.7.1 Surface Passivation

Surface trap stats can be reduced by including a high-quality passivation layer such as Si_3N_4. The use of a SiN cap layer grown in-situ with the AlGaN/GaN epi-structure, has been shown to provide excellent early passivation and prevent strain relaxation [76]. Strain relaxation leads to the formation of additional trap states and leads to device reliability issues [44].

There are several theories on the exact reason that surface passivation leads to reduced surface trap effects.

One theory is that the process of depositing the passivation SiN leads to the incorporation of Si atoms, which act as shallow donor states and which are sufficient to replace the surface donor. [39]

Another theory is that the presence of positive charges at the interface between the passivation and AlGaN barrier is required to prevent the formation of a virtual gate and to aid with the suppression of current collapse. The use of a passivation allows these positive charges to be inserted into the interface because of the presence of the Si^+ ions as dangling bonds in a SiN passivation. This enables both greater 2DEG carrier confinement and suppression of surface trap effects. Therefore, other passivation methods with a larger positive charge density have been developed, such as SiON. This allows gate-lag and current collapse to be reduced [77].

3.7.2 Field Plates

Field Plates attached to either the gate or source have been shown to improve device performance by reducing trapping effects. The longer the field plate, the greater the effect in suppressing the trap states. The use of field plates has been shown to result in a significant reduction in the drain-lag effect by reducing device current collapse

[43].

The field plates result in a reduction to the electric fields peaks, along with a more uniform field. This results in better confinement of electrons in the 2DEG [50].

However, there are issues with field plates, as including a field plate between the source and gate can lead to increased trap states in the gate region [43]. They also lead to significantly higher intrinsic capacitance, which results in significantly deterioration in RF performance.

Chapter 4

Fabrication of Gallium Nitride HEMTs

4.1 Introduction to GaN HEMT and MMIC Fabrication Process

This chapter covers all the steps and theory behind the fabrication of GaN HEMTs and the Monolithic Microwave Integrated Circuits (MMICs) in which these active devices will be used.

All fabrication steps with the exception of material growth, ion implantation, and PECVD were carried out in the Institute of Compound Semiconductors (ICS) at Cardiff University. Ion implantation was performed at the Surrey Ion Beam Centre at Surrey University. PECVD was performed at multiple different partner locations.

4.2 Material Growth

4.2.1 Substrates for High Performance RF GaN HEMTs

There are multiple substrates used for the growth of AlGaN/GaN HEMTs, currently the two most popular substrates are Silicon and Silicon Carbide. Silicon is desired

due to the low cost and large wafer size that is currently possible to produce, due to the robust technology, whereas SiC is preferred due to its superior performance in the three key metrics below:

The substrate material used in this work is high-resistivity silicon. For RF GaN HEMTs, several important properties are required of the substrates:

- **High substrate resistance** is extremely important for RF devices due to the reduced parasitic effects compared to low resistance substrates, leading to degradation of device performance in high-frequency operation [78]. Another benefit is lower substrate loss, which enables higher performance RF GaN HEMTs as it ensures higher efficiency and improved isolation. This is highly important because it allows for improved integrity of the RF signals [79].

- **Thermal conductivity** is important for GaN devices, as they are typically able to operate at much higher temperatures and power levels than competing technology.

- **The lattice constant** is important to ensure a good lattice match with GaN, which reduces stress and dislocations in the material.

Outside of Si and SiC wafers, there are also Sapphire, AlN, and GaN substrates that have been used for the growth of GaN epi-layers. Of these, sapphire was the original material on which the first AlGaN / GaN HEMTs were grown [23]. However, because of the improved thermal conductivity and lattice mismatch of SiC, it is the preferred material for high-performance RF. This leads to improved performance in AlGaN/GaN HEMTs [80].

AlN and GaN substrates have only recently been developed and are currently only available in small wafer sizes of 50 mm. Because the growth of these continues to require significant research, they are still several years away from being viable on a large scale, despite the initial promising results [81] [82].

The final substrate technology under development is GaN-on-Diamond. However, this is a very different process, as the GaN epi-structure is not grown on the

diamond substrate. Instead, the GaN epi-structure was first grown on a silicon wafer. The silicon is then removed, and the diamond substrate is then grown or bonded to the back of the GaN epistack. This has shown very promising results due to the extremely high thermal conductivity of diamond. However, this technology still requires significant development to reach maturity [83].

4.2.2 Silicon Growth

The current industry standard for silicon growth is the Czochralski (CZ) method. This was developed in the 1960's and has constantly been iterated and improved to enable larger diameter wafer growth. Currently, the largest silicon wafers in full-scale production are 300mm, with 450mm wafers available in research. The CZ method is a melt based crystal growth technique, that uses a furnace to heat electronic grade polysilicon in a high purity quartz crucible, to approximately 1420°C just beyond the melting point (1412°C). Then a high purity silicon seed crystal is lowered into the molten silicon, before being slowly lifted out while the seed and furnace are rotated slowly in opposite directions. This leads to large silicon ingots that are then cut to create the silicon substrate [84]. Figure 4.1 describes the CZ process and all the different steps used to ensure that the ingot grows to the correct size and crystal structure. Figure 4.2 shows the grown silicon ingots. Figures 4.1 and 4.2 are taken from [85]. Although this is the optimal growth method for low-cost high-volume manufacturing, this growth method has drawbacks in the purity of the silicon substrates that it is able to produce. This comes from the oxygen impurities contributed from the crucible. Therefore, it is not possible to produce high resistivity silicon substrates, with the CZ method only able to produce silicon wafers with a typical resistance in the range of 100-1000 Ω·cm [86]. Although this is not an issue for most of the CMOS and silicon semiconductor industry, for high frequency GaN-on-Si devices it is extremely important to have high-resistivity silicon substrates (5000 Ω· cm) to minimise any substrate losses.

In the early years of electronic grade silicon substrates (1950's) the predominant

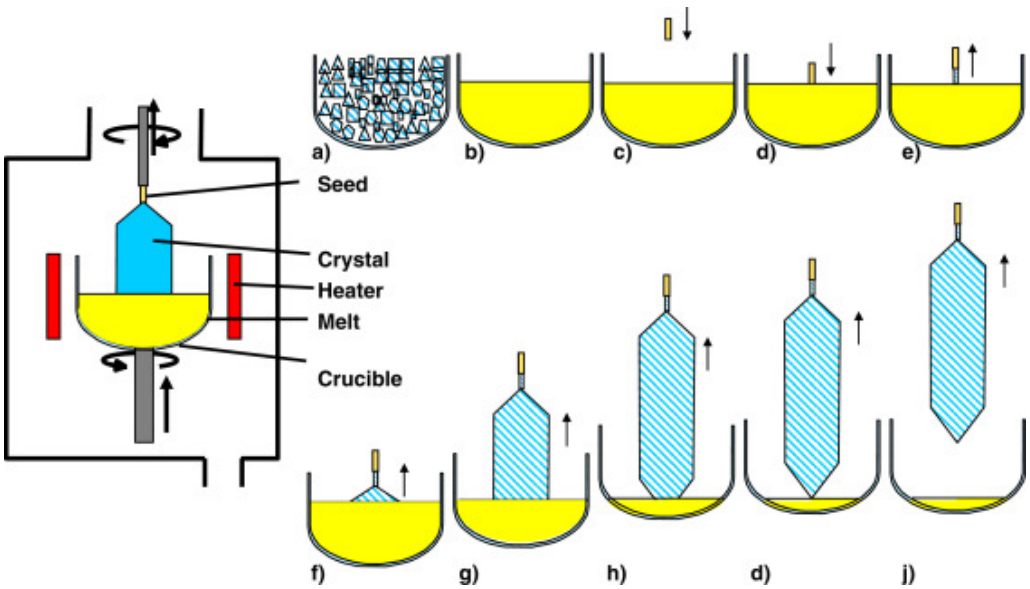


Figure 4.1: Schematic of the Czochralski method process and illustration of the crucible with the different growth steps: (a) The polycrystalline feedstock loaded in the crucible (b) which is then melted, (c) The seed crystal is dipped into the melt, (d) followed by Dash necking (e), shouldering (f), cylindrical growth (g), growth of end cone (h), lift off (i), cooling down and removing of the crystal. Figure taken from [85].

Figure 4.2: Grown silicon ingot with 300mm diameter and weighing over 250 kg. Figure taken from [85].

method of growth used was the Float Zone method. FZ was replaced by CZ for mass production, because FZ was significantly more expensive. Therefore, today the FZ method is only used for very specific applications such as high-resistivity silicon wafer growth $> 1000\ \Omega\cdot$ cm such as those required for GaN-on-Si applications [86]. Currently, it is possible to grow wafers up to 200 mm using FZ with an extremely low oxygen concentration ($<10^{-16}$ cm^{-3}) [85] and a resistivity of up to 20 kΩ [86].

The FZ method is a crucible-free method that places a polysilicon ingot onto a silicon seed crystal; the bottom of the ingot is then melted using inductive heating either in a vacuum or in an argon atmosphere to prevent contamination. The seed crystal is then dipped into the molten polysilicon, then the heating coils are moved to the polysilicon ingot while rotating both the seed crystal and the polysilicon ingot to form the silicon crystal [86]. Figure 4.3 taken from [85] shows the FZ growth method.

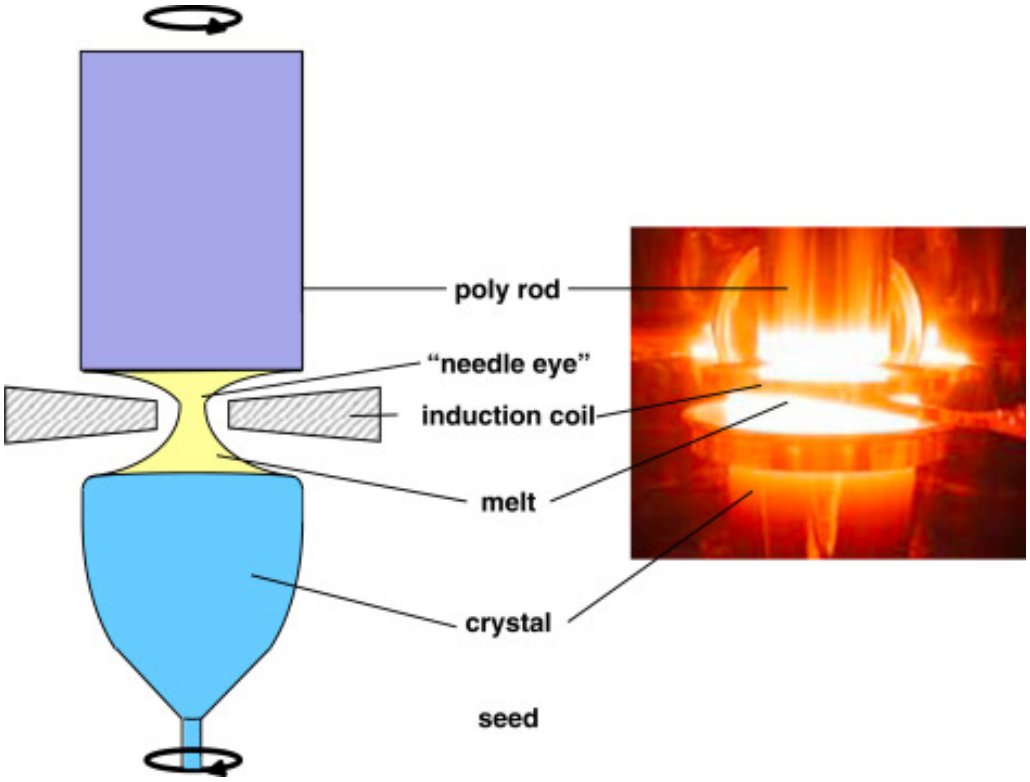


Figure 4.3: Left: Diagram of the FZ growth method. Right: Photograph of FZ growth. Figure taken from [85].

Once the silicon ingot has grown, it is then cut into thin wafers, which are then lapped to the desired thickness, etched to remove any damage from cutting and then

finally polished [86]. At this point, the silicon wafers are ready for the next step of fabrication.

One key factor for silicon wafers is the crystal orientation, the most common being (100) and (111) with the detonation based on miller indices. This has a significant impact on the wafer structure and electrical properties. Whist (100) is ideal for CMOS transistors due to its favourable electronic properties, for use with GaN epi-layers (111) is preferred due to the reduced lattice mismatch as the (111) orientation is similar to the wurtzite structure [87].

4.2.3 Growing the Epitaxial Layers

The growth of high-quality GaN-on-Si is highly challenging because of two main challenges with the growth of GaN on Si. These are the large lattice mismatch of 17 % and a thermal expansion coefficient of 54 % between the wurtzite GaN structure and the silicon (111). Due to this large lattice mismatch, a significant number of dislocations and defects will form, resulting in trapping effects and scattering. The large thermal expansion coefficient leads to large stress across the wafer, which results in wafer bowing, and in severe circumstances cracking during the cooling process.

Due to these issues, thick buffer layers between the GaN and Si substrates are required to allow for a reduction in defects and stress. The first layer is typically a thin AlN nucleation layer, which prevents melt-back etching, where the Ga-Si bonds form as the silicon substrate is etched away. After this nucleation layer, the thick buffer layers can grow on this AlN nucleation layer. The most common buffer structures are graded AlGaN or AlN/GaN superlattice buffer structures.

The graded AlGaN buffer consists of multiple AlGaN layers grown sequentially with a variation in the Al concentration throughout the buffer layer. The AlN/GaN superlattice buffer has been highly successful in terminating the vertically generated defects and dislocations, preventing them from reaching the epi-structure above.

After the buffer structure has grown, the next layer in the epi-structure is the

optional inclusion of an AlGaN back barrier. This structure has been introduced to reduce the buffer trapping effects, by providing increased carrier confinement and raising the conduction energy band reducing the chance carriers can make it to the buffer traps [87].

The high-quality GaN channel layer can then be grown.

An AlN layer is inserted after the GaN channel layer because of its ability to significantly increase the height of the potential barrier, leading to improved confinement and increased 2DEG mobility [88].

Then we have the AlGaN barrier layer. Through adjustments to the Al concentration and the barrier thickness, the properties of the 2DEG can be changed.

The final layer grown is a cap layer to protect the AlGaN barrier from oxidation. This can be either a GaN cap [89] or an in-situ SiN cap layer. The in-situ SiN cap is the currently preferred method as it provides the first few nanometres of passivation, resulting in lower surface trap density [90]. In either case, this cap layer is very thin, typically between 1 and 10 nm.

An example epi-structure for a GaN HEMT is shown in Figure 4.4.

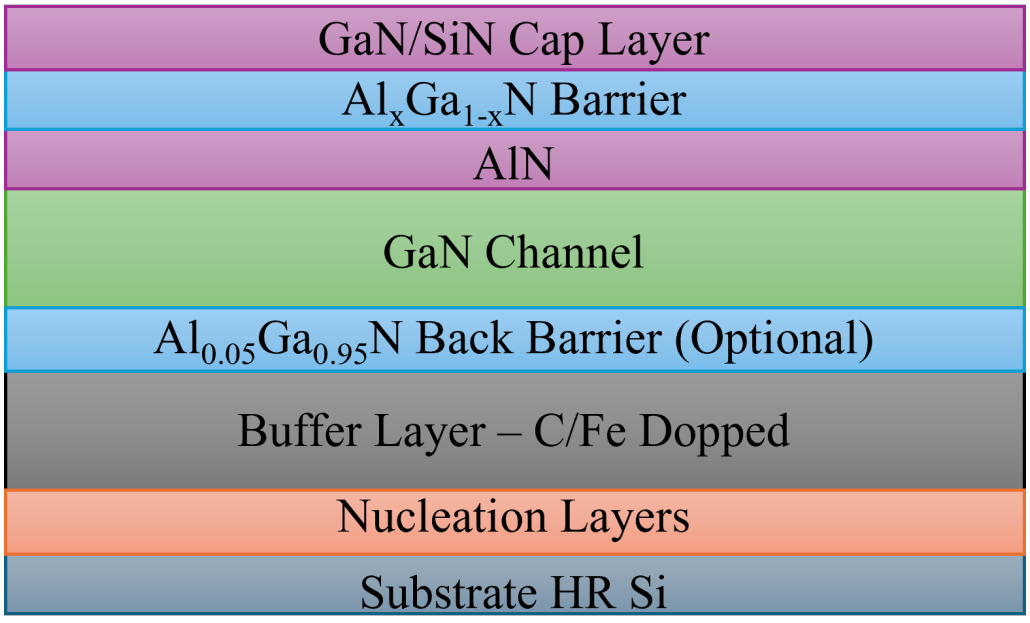


Figure 4.4: Example GaN-on-Si epi-structure.

There are two common methods for epitaxial growth of GaN, these are metal

organic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE).

Because of the slow growth rate of MBE it is typically only used in research for the growth of very high-quality material, where MOCVD is the typical growth method in industry. In [91] using MOCVD for the growth of AlGaN / GaN HEMTs, a growth rate of 4 $Å s^{-1}$ was achieved, while for MBE a had a growth rate of just 1.2 $Å s^{-1}$.

Due to the fact that all of the material used in this work was grown by MOCVD, and MBE is not commercially viable and only used in highly specific applications and research it has not been discussed in this work.

Metal Organic Chemical Vapour Deposition (MOCVD)

For MOCVD growth, a gas stream is passed over the wafer that has been heated. The gas consists of precursors, which are the gases that will be used for growth. Then there are also carrier and purge gases. These are used to control the flow rate of the precursor gas and evacuate the chamber of the toxic precursor gases, when switching to a new epi-layer growth process or finishing the growth process.

A basic MOCVD system consists of the following sections [92]:

- Gas supply and mixing system: this is where the gases are mixed, and the flow rate is controlled to maintain control over the gas flow in the reaction chamber.
- Reactor: this consists of a gas injection shower head, a high-temperature heater (> 1100 °C), and a substrate holder. The gas is flow in injected through the shower head over the entire wafer. This wafer is held in the chamber and heated to the temperature that is required for the process.
- Vacuum system: this is used to evacuate gases from the chamber and to enable control of the specific pressure in the reactor chamber.

- Scrubber unit: this removes the hazardous by products and particulates from the exhaust gases
- Ventilation system: this handles all of the waste gases and removes them from the system.

The growth of the epi-layers, is done through the chemical reactions of the precursor gases on the heated substrate. The gas precursors used for the growth of AlGaN, consist of: $Al(CH_3)_3$, $Ga(CH_3)_3$ and NH_3. These are typically injected into the reactor at low temperature through the shower head along with carrier gases such as H_2 or N_2. These gas precursors then enter the high temperature region, close to the substrate where they react, leading to the single film growth of the desired crystal structure. The by-products from this reaction are then carried away from the surface and removed from the reactor [93]. This process is shown in Figure 4.5.

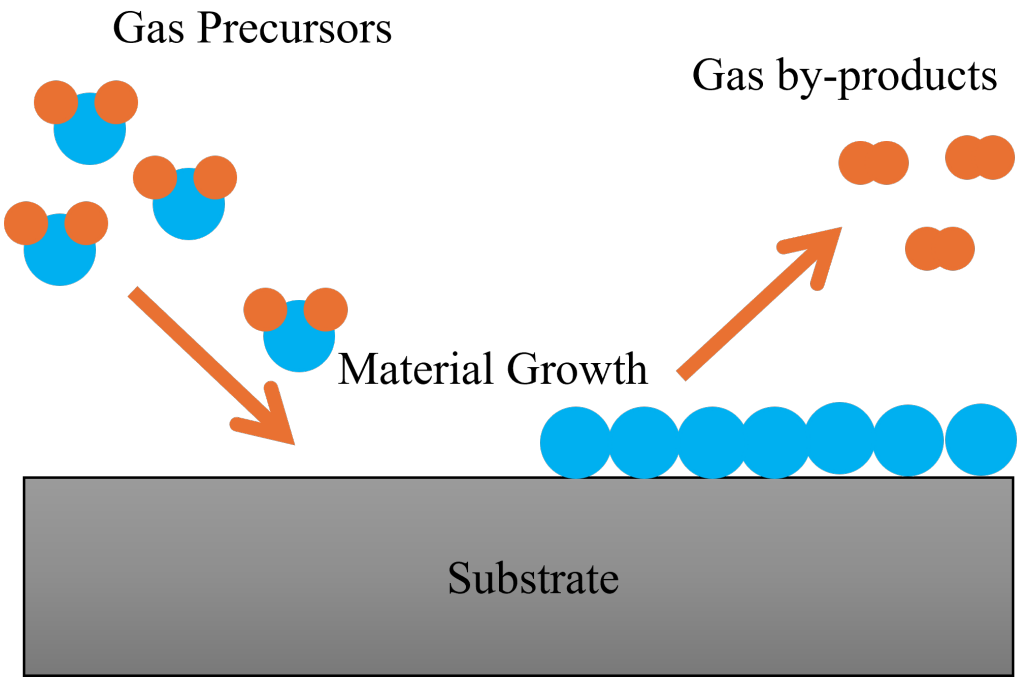


Figure 4.5: Diagram showing MOCVD growth process

4.3 Device Fabrication

4.3.1 Sample Preparation

Sample Cleaving

The first stage before any fabrication begins is sample preparation. The first stage is to cleave the wafers into 25x25mm tokens that will be used for the fabrication. This was done using a diamond-tip scribe. After cleavage, the samples are marked on the back side of the Si for identification.

Sample Cleaning

The cleaning and surface preparation is critical before every fabrication process. The process for cleaning the samples involves the use of the standard organic cleaning process, which consists of 4 stages:

1. First, submerging the sample with acetone and using an ultrasonic water bath for 5 minutes at 50 °C.

2. Then transfer the sample from acetone to methanol and use an ultrasonic water bath for 5 minutes at 50 °C.

3. Next transfer the sample from the methanol to isopropyl alcohol (IPA) and use an ultrasonic water bath for 5 minutes at 50 °C.

4. Finally the sample is rinsed with de-ionised (DI) water and blow dried with a nitrogen (N_2) gun, before performing a dehydration bake at 110 °C.

However, before some process steps, such as metal deposition, it is important to prepare the sample surface by removing any potential contamination, such as oxidation, carbon, and hydrocarbon contamination. To do this, hydrochloric and hydrofluoric acids are diluted in DI water, to effectively remove these surface contaminants [94].

4.3.2 Lithography

Lithography in semiconductor fabrication consists of transferring a pattern onto the sample, and this is one of the most critical processes in semiconductor fabrication. In almost all semiconductor fabrication processes, the sample will pass through this lithography stage multiple times. The lithography stage consists of multiple stages: sample cleaning, application of a resist, baking of the resist, exposing the resist, and development of the resist [95].

In this work, two methods of lithography are used. These are photolithography and electron beam lithography (EBL). For designs where the minimum feature size is > 1 μm, photolithography is the preferred technique due to the fast speed and lower cost, whereas in sub-micrometre designs electron beam lithography is required.

In this work, photolithography was used for all fabrication stages, except for the gates, where the E-beam was used due to the requirement for sub-micrometre gates.

Photolithography is the process of transferring a pattern onto a sample, through the use of light. For semiconductor fabrication, ultra-violet (UV) light is used. There are multiple methods for photolithography, such as methods consisting of a physical mask with a pattern or maskless lithography tools. However, the basic principle remains the same regardless of the patterning technique.

EBL uses the use of a guided beam of electrons to define the pattern onto the sample.

Choosing a Resist, Positive or Negative

In preparation for lithography exposure, the first stage is to choose a resist. In both photolithography and the E-beam, there are two types of resist, positive and negative. In a positive photoresist, the area that is exposed by the UV light is removed, and the area that is protected from the UV light will remain. This is because in the case of a positive resist, during the exposure of the resist, the UV light (or electron beam) results in the breaking of long polymer chains which results in the resist becoming soluble in a developing solution. However, with a negative

resist, the opposite occurs. During exposure to UV light (or electron beam), long polymer chains form in the resist rendering the exposed parts of the resist insoluble in the developer solution, and the protected areas of the resist will remain soluble and can be easily removed. This process is highlighted in Figure 4.6.

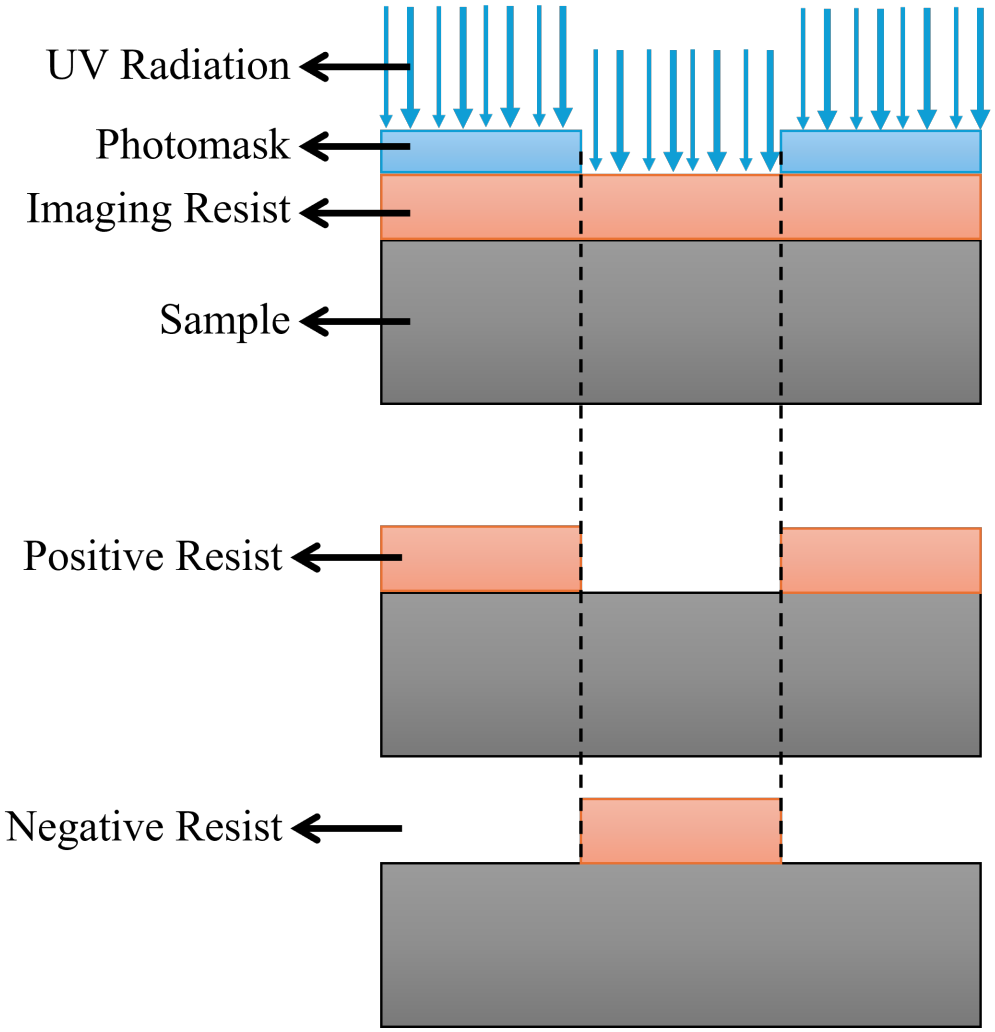


Figure 4.6: Photolithography where the pattern from the mask is transferred to the sample, using either a positive or negative photoresist.

The requirements of the process will determine which resist is best for the specific fabrication purpose.

Spin and Bake of a Resist

Once a resist has been chosen, it needs to be applied to the sample. The best way to ensure a uniform coating is to "spin" the resist onto the sample. This involves the use of a spin coater. The chosen photo resist is carefully applied to the sample using

a pipette to ensure that there are no air bubbles. Once the sample has been coated to the edges, the sample is spun at a high speed. The spin speed, acceleration, and spin time are all chosen based on the desired thickness of the photoresist and can be taken from the resist data sheet. The desired thickness of a resist will change depending on the application.

Once the sample has been spun with the resist, it needs to be baked to evaporate the solvents from the resist and allow the resist polymer to solidify. This can be done either on hot plates or in an oven and should be done according to the recommendations from the photoresist data sheet.

Exposure - Photolithography

Now, the sample is coated with a resist and the lithography process can be performed.

In the case of mask-based lithography. A physical mask with the desired pattern to transfer onto the sample is required. This mask is typically quartz due to the requirement of a high level of transparency to UV light. In this quartz mask, a chrome metal layer is defined with the pattern. This chrome layer prevents UV light from reaching the areas covered in chrome, and where there is no chrome, UV light can pass directly through the quartz to reach the sample.

This mask is placed in hard contact with the sample. This hard contact is required to reach the maximum desired feature resolution, as light will diffuse after passing through a gap. By ensuring a hard contact between the sample and the mask, this diffusion can be minimised. Once the mask and sample are in place and aligned, UV light is focused through the mask, transferring the mask pattern to the resist [96].

Exposure - Electron Beam Lithography

In an E-beam system, because of the nature of an E-beam, where a single beam of electrons is generated, the sample is not exposed all at once. Instead, the electron

beam needs to be focused and moved across the sample to expose specific areas. This means that there is no requirement for a mask as the electron beam will be directed to the areas that are intended for exposure. However, because of the lack of flood exposure and the requirement to expose each area spot by spot, the lithography process is significantly slower than that of photolithography. It also requires a more involved preparation stage as the interaction of the electrons with the resist, substrate, and existing patterns needs to be simulated to ensure that the correct dose is applied to the required areas [96].

Development

Once the sample has been exposed, it needs to be developed. This is where the resist that needs to be removed is etched away. This process is carried out using a specific resist developer solution. The specific solution will change depending on the resist that has been used. This is a highly sensitive process; if the sample is left in the developer solution for too long, it will eventually remove the entire resist, including the areas that should be insoluble. If the sample is left in the developer for too short a time, resist will still remain in places where it is not desired. Therefore, the time needs to be carefully controlled. Once the sample is removed from the development solution, it should be immediately rinsed with DI water to prevent any development from continuing.

At this point, the desired pattern will have been transferred to the sample. This complete process is shown in Figure 4.6, where the cases of a positive and negative resist are shown. After exposure through the mask, the positive photo resist has been removed where it was exposed, and in the case for negative photoresist it has been removed where it was not exposed.

Lithography Alignment

Most semiconductor fabrication processes require more than one lithography stage. Therefore, alignment between each level of lithography is critical. Therefore, align-

ment markers are used to align the different lithography layers. An example of the markers used for photolithography is shown in Figure 4.7. In the first lithography process, a set of markers on the sample has been patterned, then a metal has been deposited to create the markers, which in this case is platinum. The current stage of the sample in Figure 4.7 is that the second lithography level has just been developed. It can be seen that there is both the metal of the markers, and aligned to this marker is the developed photo resist, from the second lithography level. For these alignment markers, verniers are used, which are the ruler-like grid on the side of each marker. These are perfectly aligned for the central pin, then with each pin moving away from the centre the misalignment increases by 0.5 μm. This is to enable the level of alignment accuracy to be determined after the lithography process.

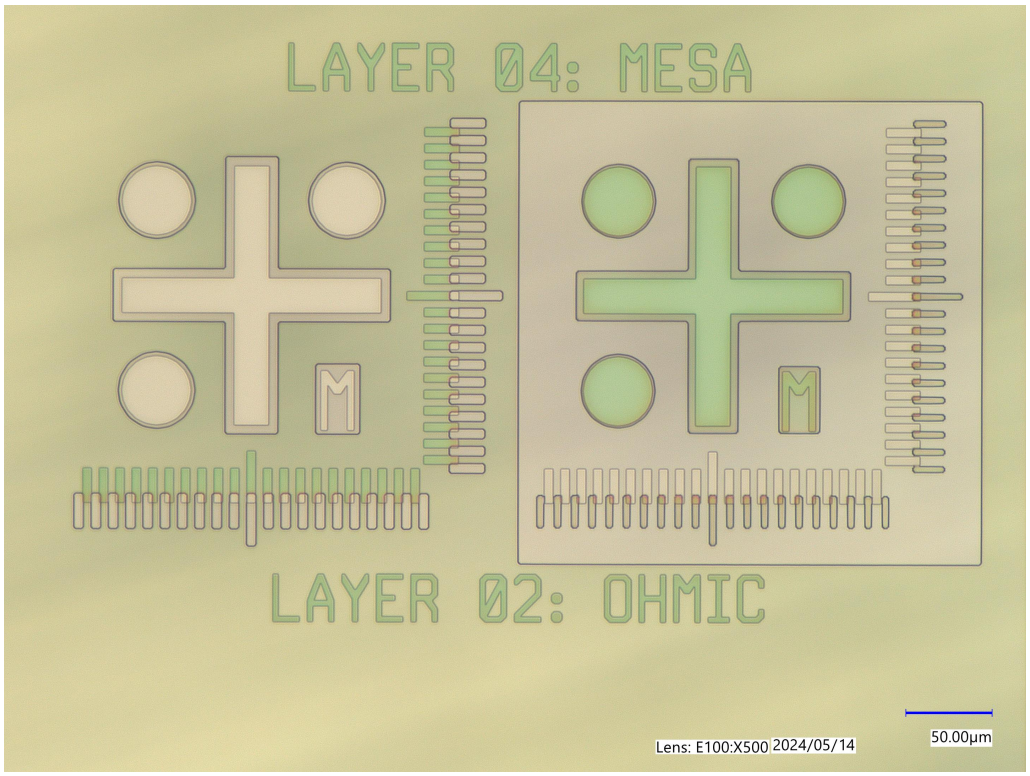


Figure 4.7: Alignment markers from a sample, after the development at the end of the second lithography level.

In order to perform alignment correctly, multiple of these markers are required, to ensure that there is no rotational misalignment across the sample. Therefore, a minimum of two markers are required on the far left and right of the sample, respectively. For processes where a very high alignment accuracy is required, 3

markers can be used with this additional marker at either the top or bottom of the sample.

4.3.3 Metallisation

Metal Deposition

Metal deposition is a critical step because of the requirement of metal-semiconductor contacts. In AlGaN/GaN HEMTs, both Schottky and ohmic metal-semiconductor interfaces are required. Schottky contacts are used for the gate and ohmic contacts are used for the drain. There are several ways to deposit metal onto semiconductors, but in this work electron beam physical-vapour deposition (EB-PVD) has been used for the deposition of all the metals used in this work.

Electron Beam Physical Vapour Deposition

This metal deposition method uses a high-energy electron beam to strike the target metal. This results in the heating of the target until it forms a high temperature molten metal pool. This will then evaporate, resulting in the evaporated atoms gradually condensing on the sample. Due to the requirement for highly pure metals, it is important that this process is performed at a high vacuum in the order of 10^{-6} or 10^{-7}. If the vacuum is not at this level, it will result in the deterioration of the quality of the metal due to the presence of contaminants in the path between the metal source and the sample. Due to the high temperature of the metal evaporation, it is important to ensure that there is a substantial distance between the sample to prevent any burning of the resist. If the resist is exposed to high temperatures, it will deform and round at the ends, resulting in poor metal lift-off, which can result in a poor yield.

Metal Lift-off Technique

This is a critical step for the deposition of metal on a sample. When the metal is deposited on the sample, it will coat the entire surface in a uniform layer. Since

we have a specific pattern with which we wish to define the metal, it is required that the metal can be removed where it is not desired. To do this, a metal lift-off is required.

This process is described in 4.8, where the first step is the use of a bilayer resist. This is where two different resists are used. The first resist is a lift-off resist (LOR). This LOR is not photosensitive, and the development time is dependent on the bake time only. The second resist is the imaging resist. This resist is photosensitive and will have the exact pattern (image) that is required. During the development process, the imaging resist will develop perfectly with the desired pattern, and then the LOR will develop, leading to a resist profile undercut, as shown in Figure 4.8. Now due to this undercut profile, when the metal is deposited, there will be a break in the metal where the sidewalls of the resist is exposed. This sidewall can be attacked by the resist striper solution, which will result in the resist being removed along with the metal deposited on the resist. This leaves only the sample with the metal pattern that was defined in the lithography process.

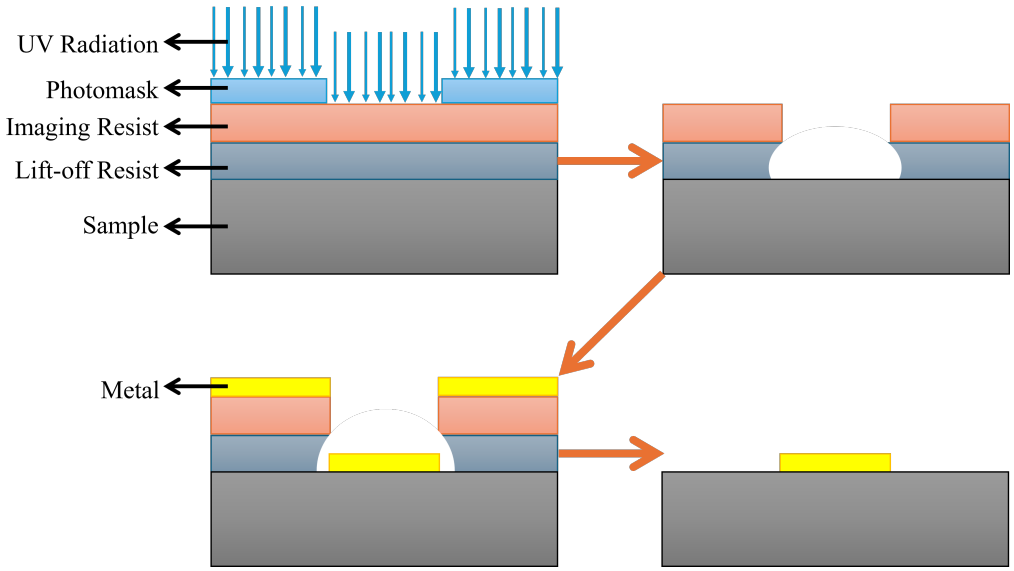


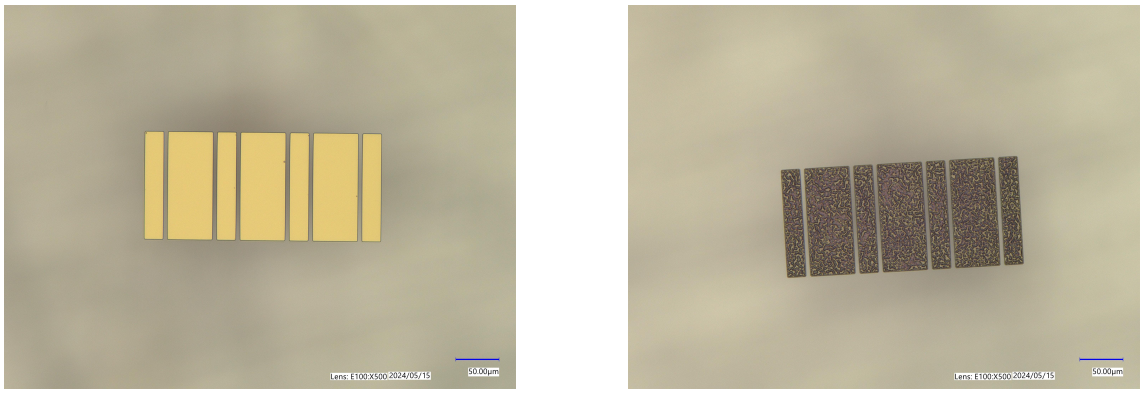
Figure 4.8: The metal lift-off process

Rapid Thermal Annealing (RTA)

Rapid Thermal Annealing (RTA) is a process required for the formation of ohmic contacts.

The RTA process involves rapid heating of the sample to high temperatures (500 to 1200 °C) for a very short time [97]. This leads to the diffusion of the ohmic contacts into the semiconductor AlGaN layer. This results in the formation of an ohmic metal-semiconductor contact [98].

The effect of the RTA process is shown in Figure 4.9, where the ohmic for a 6 finger device is shown after metal deposition and then the effect of RTA for the formation of the Ohmic contacts.



(a) (b)

Figure 4.9: Ohmic contacts for a 6-finger device; (a) before RTA and (b) after RTA.

4.3.4 Dielectric Material Deposition

There are several methods for the deposition of dielectrics. However, for this work plasma-enhanced chemical vapour deposition (PECVD) is the only method used.

Plasma-Enhanced Chemical Vapour Deposition

The PECVD process is a common method for the deposition of dielectric material because of the lower temperature requirements of other methods. The underlying process is similar to that described in the MOCVD, but the deposition rate is significantly increased, along with a significantly lower required substrate temperature. The PECVD deposition process differs from MOCVD in the use of a plasma that converts precursor gases into reactive species that are required for deposition in the sample [99].

Due to the use of this plasma, a lift-off process is not effective, as the resist will be significantly damaged. Therefore, this process is performed as a blanket deposition and will be followed by an etch stage to remove the dielectric where required.

4.3.5 Etching

In this work both wet etching and dry etching has been performed.

Wet Etching

The wet etching process is extensively used in this work for resist development, resist stripping, and metal lift-off. This is the process in which a liquid etchant removes the desired material through the use of chemical reactions. This process is described as isotropic, which means that all directions are etched at the same rate. This is of benefit in the areas described above, but for use in dielectric etching or etching the GaN, this lack of control is problematic [100].

Dry Etch - Reactive Ion Etching

Reactive Ion Etching (RIE) is highly anisotropic, allowing for highly vertical sidewalls. During the etch process, it is possible to rely on just the physical etch process if the plasma species is chemically inert. However, through the introduction of reactive species, it is possible to introduce a chemical etch process. Through adjustments of both of these elements, it is possible to increase the etch rate through the reactive species. Through the use of low RF power and carefully selected reactive species, it is possible to obtain high selectivity between GaN and a dielectric, allowing for the GaN layer to act as an etch stop. This is highly beneficial for the etching of dielectrics in the GaN material space [101], [102].

Dry Etch - Inductively Coupled Plasma

One limitation of RIE is that it has poor etch performance when etching III Nitrides. Therefore, the use of inductively coupled plasma (ICP) etch is preferred when etching

GaN layers. This is due to both the higher plasma density and the ability to reduce the ion energy whilst maintaining a high plasma density. This improved control enables the electron and ion energies to be kept low, improving the anisotropic profile, allowing for improved selectivity, allowing for an improved etch process for GaN [101].

4.3.6 Ion Implantation

Ion implantation is the process of acceleration of a beam of ions from a source to bombard the sample. This process allows for non-native ion species to be inserted into the epi-structure. This process can be used for multiple purposes, such as selective doping [103]. However, in this work, ion implantation has been performed for device isolation using Ar^+ ions.

4.4 Standard HEMT Fabrication Flow

1. Markers: Ti/Pt markers are deposited on the sample. Titanium is used as an adhesion metal to ensure good adhesion between the metals and the GaN Cap layer. Platinum is used because of its high resistance to RTA annealing allowing them to survive the Ohmic Stage.

2. Ohmics: The ohmic contacts consists of a standard Ti/Al/Ni/Au metal stack. The samples are then subjected to Rapid Thermal Annealing (RTA) at 850 C for 30 s in a nitrogen environment. This RTA allows the Titanium and Aluminium to alloy and diffuse into the AlGaN layer creating an ohmic contact to the 2DEG. The nickel acts as a barrier to prevent the diffusion of the gold into this alloy, as gold is required to cap the ohmics due to its resistance to oxidation.

3. Ohmic cap metal: This is a Ti/Au metal deposition that is used to protect the ohmics from any contamination or degradation during the rest of the fabrication process.

4. SiN Deposition: This stage is used to apply the first surface passivation and is used for the definition of the T-Gate foot. 100 nm of SiN is deposited using PECVD at 300 C.

5. Ion Implantation: Ion implantation is performed using Argon Ions, which are used to bombard the sample and disrupt lattice structure. This results in the removal of the 2DEG from this bombarded area. This allows for device isolation to be achieved creating a highly resistive area.

6. SiN Etch: This stage etches the Source and Drain pads using a Cl biased RIE etch stage so that they are exposed to enable electrical connection in a future fabrication process.

7. Gate Trench: This is where the 250 nm gate foot is defined through the use of E-Beam. After the trench is defined the SiN is etched using a Cl biased RIE

etch stage.

8. Gate Head: This is where the gate head is defined using E-Beam, Once this has been defined the gate metal stack Ni/Au is deposited to form the Schottky gates.

9. Bond Pads: This is where a thick metal layer is deposited to connect the ohmics and feeds for the device.

10. 2nd Nitride Deposition: This is an encapsulation Nitride that is used to protect the device from the environment and act as an insulation between metals in the final stage.

11. 2nd Nitride Etch: This is an Cl RIE etch used to expose the measurement pads and the Source contacts. The Source contacts are exposed to facilitate air/nitride bridge fabrication for multi-finger devices if required.

Chapter 5

DC-IV Measurements Investigating Trap Effects In GaN HEMTs

5.1 Introduction

The work in this section was done in close collaboration with IQE plc with extensive discussion and input from Dr. Sinan Goktepeli and Dr. Richard Hammond from IQE.

For this work, a 200 mm GaN-on-Si wafer was grown by IQE, featuring a simple epi-structure intended to facilitate a thorough investigation into characterisation techniques and new methods for trap identification in GaN HEMTs. This wafer was processed at an external foundry to ensure high repeatability across multiple fabrication runs. The mask set was designed in close collaboration between our research group and IQE, with significant MIS-HEMT device variations in both DC and CPW RF topology.

5.2 Trapping Effects Observed in Device Characteristics Using DC-IV Measurements

5.2.1 DC-IV Output Kink Effect

To observe the kink in the device output characteristics, DC-IV measurements were conducted in a dark, temperature-controlled environment using a 200 mm semi-automatic thermal probe station. The Keysight B2902A Source Measure Unit (SMU) was used to perform the DC measurements. All measurements were performed with a 10 ms delay, to enable the long measurement time required to observe the kink effect. Two different measurement setups were used for device measurements. DC device structures were measured using Signatone high isolated coax probes and the RF device structures were measured using 150 μm GSG RF probes through Auriga 67 GHz, 50 V, 1 A Bias tees. A 50 Ω load was connected to the RF port to suppress device oscillations during the measurements.

Before measurement, all devices were first "burnt in" by performing an output measurement with V_{DSMax} = 40 V. After this measurement a permanent threshold voltage shift is observed where V_t decreases by 4 V. At this point, the devices behave in a stable way. It is speculated that this is due to very deep dielectric traps in the MIS-HEMT SiN dielectric under the gate, that are unable to release resulting in this permanent V_t shift.

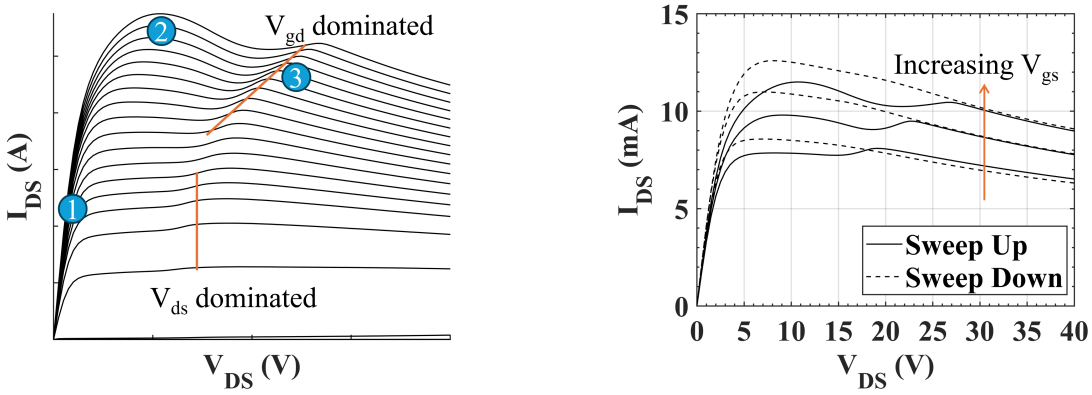
V_{tNorm} has been taken as an approximate value of the threshold voltage after the burn in of the device. This is extracted from a transfer sweep where V_{DS} is set to 10 V.

For the following measurements of the kink, the following DC-IV sweep values were used:

- DC-IV transfer characteristic measurements ($I_{DS}V_{GS}$) were performed with gate voltage (V_{GS}) swept from (V_{tNorm} - 2) to (V_{tNorm} + 9) V steps of 100 mV, with drain voltage (V_{DS}) of 0.1, 2.5, 10, 20, and 30 V.

- DC-IV output characteristics ($I_{DS}V_{DS}$) were then measured with V_{GS} swept from (V_{tNorm} - 2) to (V_{tNorm} + 9) V steps of 0.5 V, with drain voltage (V_{DS}) swept from 0 to 40 V in steps of 0.5 V. This is referred to as the "Sweep Up" measurement.

- DC-IV output characteristics ($I_{DS}V_{DS}$) were then measured with V_{GS} swept from (V_{tNorm} - 2) to (V_{tNorm} + 9) V steps of 0.5 V, with drain voltage (V_{DS}) swept from 40 to 0 V in steps of 0.5 V. This is referred to as the "Sweep Down" measurement.



(a) (b)

Figure 5.1: Output characteristics, (a) shows the kink effect identifying the key points, (1) here the V_t of the device is more positive, (2) shows that V_t is now increasing as V_{DS} increases, (3) Here the V_{DS} and V_{GD} is high enough that through self heating and Poole Frenkel effects electrons are released from the traps allowing the V_t to recover to a more positive value; (b) shows the hysteresis that occurs between the kink in the sweep up and reduced kink in the sweep down of V_{DS}.

The DC-IV measurements results show this kink effect in the output characteristics. The kink effect for one of the devices is shown in Figure 5.1a where 3 different stages in the sweep up (0 to 40 V) measurement are highlighted. These three regions are:

1. The sweep starts with the device at a more positive value V_t.

2. At this point as V_{DS} increases, so does V_t as a result of the long time-constant traps forming the virtual gate, leading current collapse observed as a reduction of I_{DS}.

3. Here, as V_{GD} has reached a critical value, the time constants of these traps have reduced to nearly zero, which removes the effect of the virtual gate, allowing I_{DS} to recover as the original V_t of the device is restored. This reduction of the time constant is likely due to the Poole-Frenkel effect and self-heating in the device.

In Figure 5.1b, it can be seen through the hysteresis that when the device is swept down, V_{DS} high to low, the kink effect is removed from the device's output characteristics. This is due to the high V_{GD} from the start and self-heating of the device, ensuring that the time constant of the traps stays extremely low, leaving them in an empty state, which minimises any impact on I_{DS}. This kink effect is very similar to the kink reported in [63], indicating that this trap is potentially located in the AlGaN layer. However, further measurements and analysis are required to determine the trap time constants to confirm this.

To study the effect of device design on kink, a wide variety of different device structures have been measured, and the effect of device variation on the kink effect is described in Table 5.1 with the respective plots shown in Figure 5.2.

Table 5.1: Impact of device variations on kink effect.

Device Variation	Observation
Increasing Gate Length	Reduction in Kink Effect
Increasing Drift Region	Increases V_{GD} for trap release
Gate Field Plate (Drift Region $\leq$ 10 um)	Increases V_{GD} for trap release
Gate Field Plate (Drift Region $\geq$ 15 um)	Eliminates Kink Effect

When the gate length increases, the kink no longer occurs and a positive increase in the threshold voltage of 4 V is observed for $L_g \geq 2$ μm. This indicates that as the gate length has increased and the electric field has become more uniform, there is significantly less conduction band bending due to the Poole-Frenkel effect due to the reduced maximum electric field magnitude, which prevents the time constant of the deep traps from reducing, this removes the kink effect as the device is unable to recover due traps not releasing the electrons during the measurement sweep. Due to larger gate lengths, there will also be reduced device self-heating, which also leads

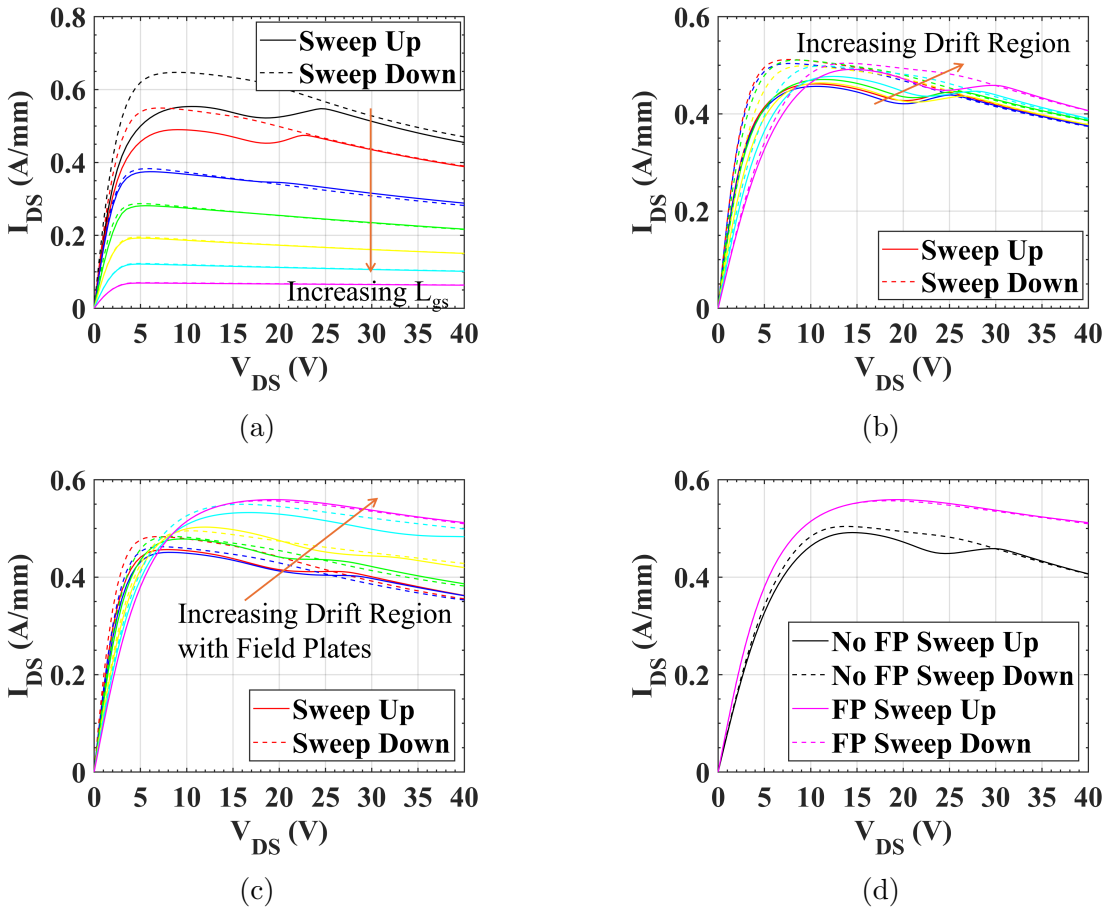


Figure 5.2: The effect of the device design on the kink effect is shown here for V_{GS} = V_tNorm + 7 V; (a) shows the effect of increasing the gate length (0.5 to 20 um) on the kink; (b) shows the effect of drift region (1.6 to 15 um) on the kink; (c) shows the effect of drift region (1.6 to 15 um) with a gate field plate on the kink; (d) shows the effect of the gate field plate with a large drift region (15 um) on the kink effect.

to the reduced chance of electron de-trapping occurring. This is similar to what has previously been seen in [104], where it was observed that as the length of the gate increased, the kink effect no longer occurred.

As the drift region increases, the required V_{GD} for the de-trapping increases. This is due to the decrease in the magnitude of the electric field between the gate and the drain. Due to this a higher maximum V_{DS} is required for the kink effect to be observed as the drift region increases.

The gate field plates improve electron confinement by pushing the electrons away from the surface due to the negative voltage applied. This has the effect of forcing surface trap states to empty more quickly. Therefore, it is assumed that the addition of gate field plates will reduce the kink effect. However, for the short drift regions ≤ 10 μm there is an additional effect at play that causes the V_{GD} required for the electrons to be released to increase. This effect is reduced self-heating in the device because the gate field plate acts as a heat sink. This leads to two conflicting conditions on the device, where the gate field plate pushes electrons deeper into the channel, while reducing the self-heating effect, which leads to a higher V_{GD} being required to release the electrons. The effectiveness of the gate field plate in suppressing trap states only starts to outweigh the effect of reduced self-heating when the drift region is > 10 μm as seen in Figure 5.2d.

5.2.2 Impact of Varying V_{DSMax} on the Output Characteristics

To further investigate the trapping effects in this wafer, additional DC-IV measurements with changes in V_{DSMax} were performed to include the following values: 5, 10, 15, 20, 25, and 30 V. The step size was also reduced to steps of 0.375 V.

Figure 5.3 shows how the output characteristics change as V_{DSMax} increases. Here, it can be seen how there are multiple conflicting trapping mechanisms at play aside from just the kink effect. At low V_{DS} values, there is minority carrier trapping occurring in the barrier, leading to increased V_t, observed through the lower I_{DS}.

As V_{DS} increases above 10 V, electron trapping in the barrier and buffer begins to occur, causing V_t to decrease, resulting in an increase in I_{DS}.

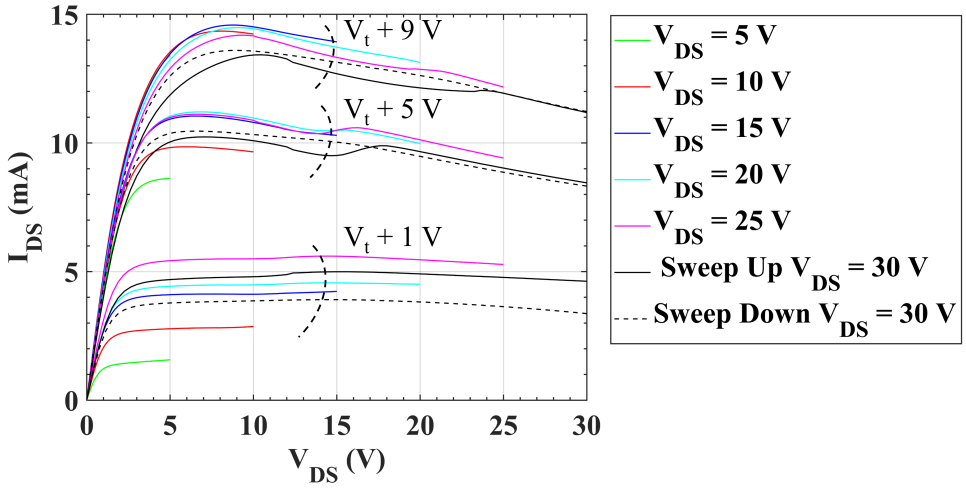


Figure 5.3: The output characteristics for a single device are shown here with the following values for V_{DSMax}: 5, 10, 15, 20, 25, and 30 V. Here the multiple competing trap mechanisms can be observed. At low V_{DS} values, there is minority carrier trapping occurring in the barrier, leading to increased V_t, observed through the lower I_{DS}. As V_{DS} increases above 10 V, electron trapping in the barrier and buffer begins to occur, causing V_t to decrease, resulting in an increase in I_{DS}.

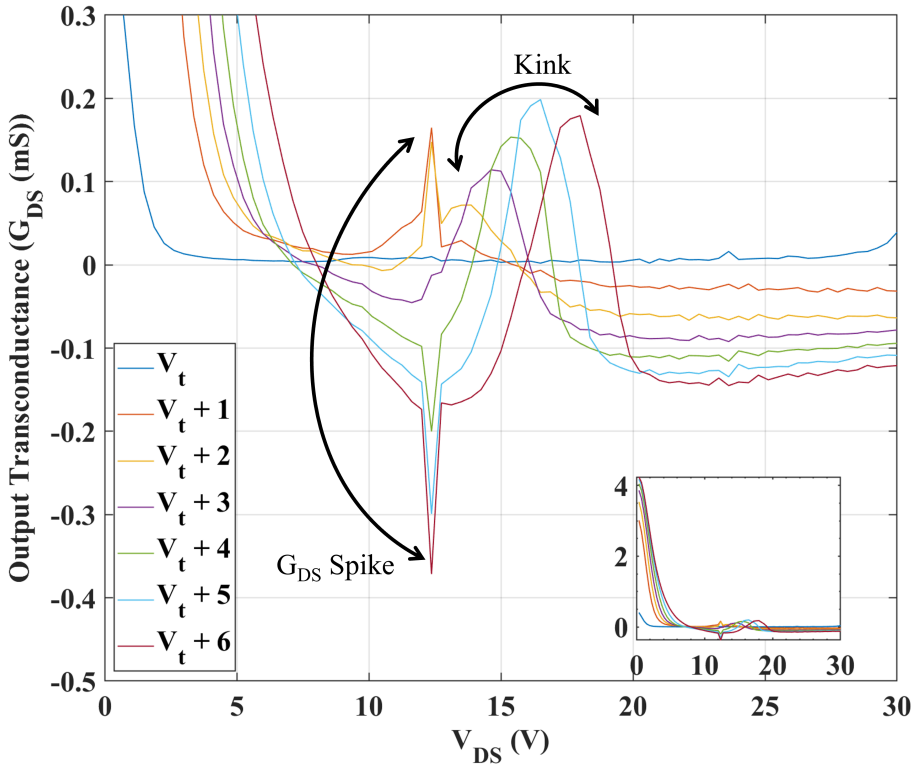
5.2.3 Output Transconductance Overshoot

Here, a new trapping mechanism has been identified that occurs as an overshoot in the output transconductance (g_{DS}). The overshoot is shown in Figure 5.4a with $V_{DS} = 12.375$ V.

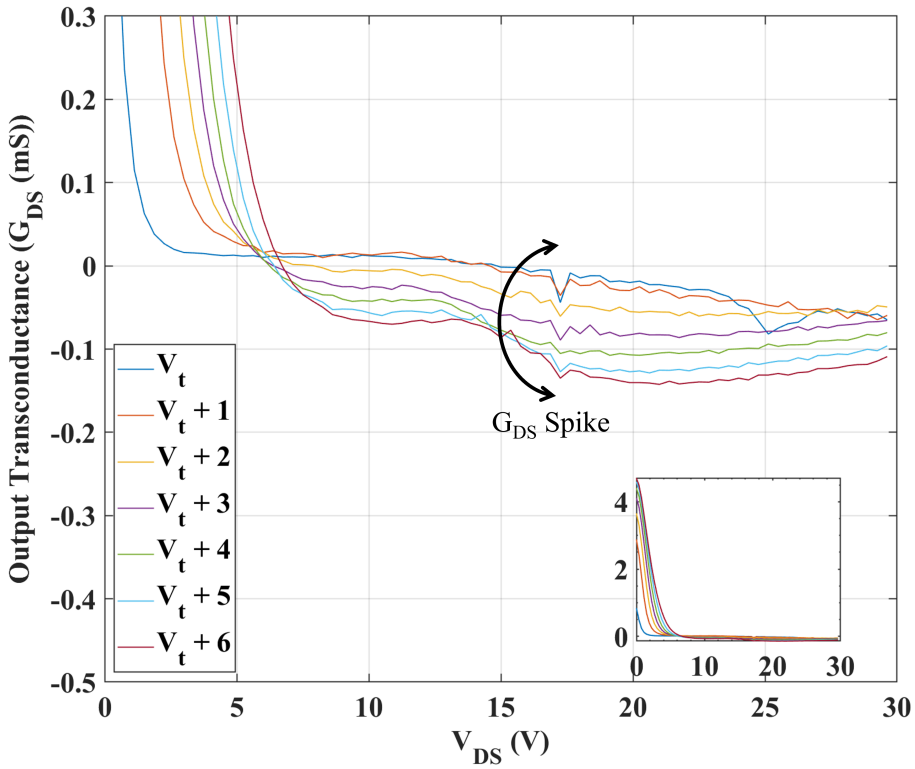
This g_{DS} is well defined and always occurs in the same V_{DS} despite changing V_{GS}. However, the magnitude of the overshoot changes from positive to negative depending on V_{GS}. As V_{GS} increases, the magnitude of the overshoot starts to decrease, from a positive magnitude to a negative magnitude. This indicates that at lower V_{GS} values the trap effect is shifting the V_t more negative and leading to a temporary increase in I_{DS}, however, at higher V_{GS} values the trap shifts to increase the V_t leading to a decrease in I_{DS}. This shift is likely due to an increase in impact ionisation filling the traps, as the device experiences more self-heating, which leads to electron-hole recombination occurring, leading to a temporary reduction in I_{DS}.

This overshoot g_{DS} is also not affected by the drift region or gate field plates. This indicates that this trapping phenomenon is not affected by the gate-drain or gate-source electric field. During a sweep down with V_{DS} swept from high to low, this effect is removed at this V_{DS} location and instead a second location is revealed at $V_{DS} = 17.25$ V, shown in Figure 5.4b. This indicates that a specific V_{DS} is required for trapping and release of traps. Due to the shift of the overshoot location and a significant reduction in magnitude, this indicates that the traps are likely shallow because they are easily affected by self-heating in the device.

The current theory is that these are shallow acceptor traps located in the GaN channel close to the 2DEG, and due to the constant V_{DS}, they are likely well defined in the lattice structure, leading to the trap effect occurring in a highly regular way. This requires further investigation through characterisation and analysis of the trap energy levels through DCTS measurements to allow for the exact cause of this trap effect to be identified.



(a)



(b)

Figure 5.4: Output transconductance (g_{DS}) overshoot; (a) observed at a constant V_{DS} = 12.5 V with the kink shown on sweep up; (b) observed at a constant V_{DS} = 17.25 V. Figure inserts show the full output transconductance sweep.

5.2.4 DC-IV Hysteresis and Transfer Transconductance Overshoot in Transfer Characteristics

For DC-IV transfer characteristic measurements ($I_{DS}V_{GS}$), the gate voltage (V_{GS}) was moved from (V_{tNorm} - 2) to (V_{tNorm} + 9) V steps of 100 mV, with drain voltage (V_{DS}) of 0.1, 2.5, 10, 20, and 30 V. For these measurements, both sweep up and sweep down measurements were performed, to observe any hysteresis.

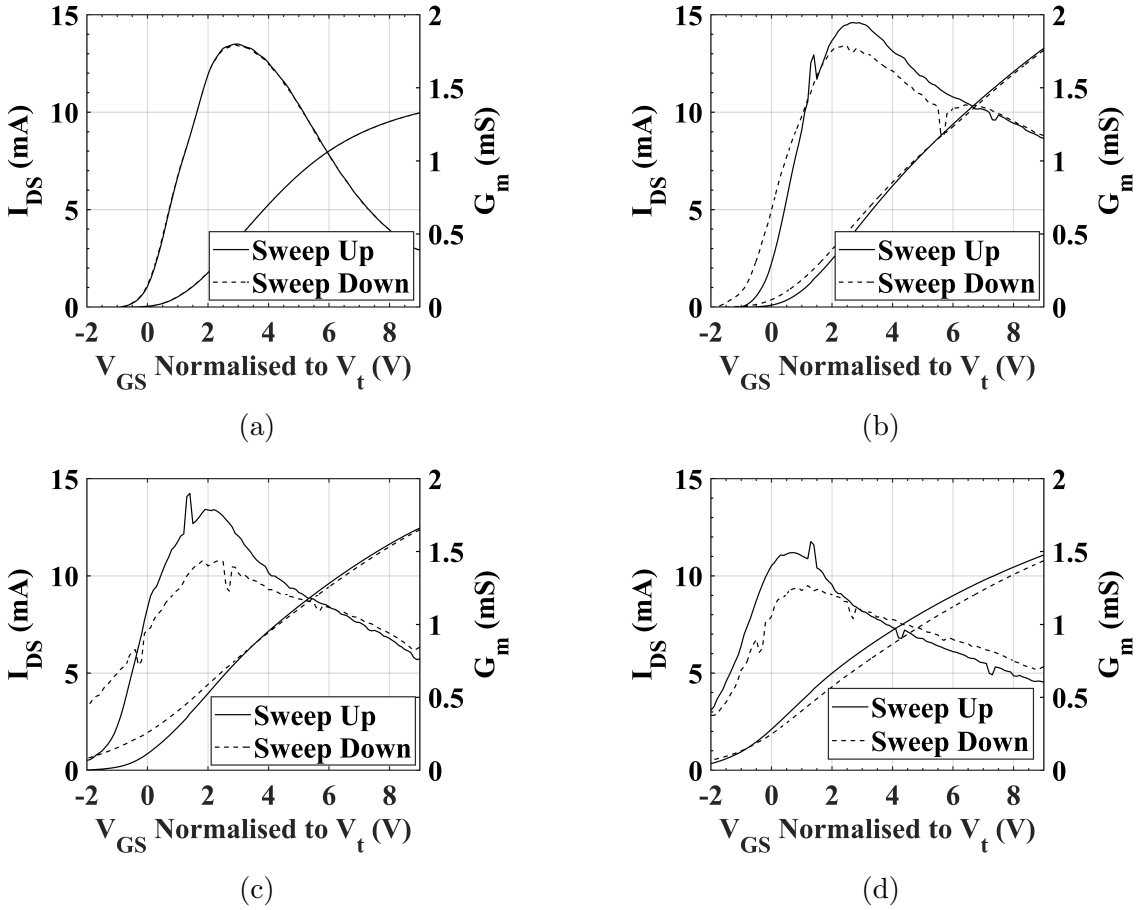


Figure 5.5: Transfer characteristics with both sweep up and sweep down; (a) V_{DS} = 2.5 V; (b) V_{DS} = 10 V; (c) V_{DS} = 20 V; (d) V_{DS} = 30 V. This measurement allows for the hysteresis to be observed in the transfer characteristics between sweep up and sweep down measurements

In Figure 5.5, it can be seen that as V_{DS} increases, there are two noticeable effects on I_{DS}, the first is the appearance of a hysteresis between the sweep up and down, along with a change in the threshold voltage. Hysteresis is not present when V_{DS} = 2.5 V and begins to become apparent as V_{DS} = 10 V. This is closely related to the mechanism that causes the kink effect in the output characteristics. At the

start of the initial sweep up, V_t is more positive due to the presence of the donor traps; As V_{GD} starts to increase, these traps empty, shifting the V_t more negative, as the threshold voltage for the device recovers to its original value. This shift occurs at $V_{GS} = V_t + 4$ V, during the forward sweep where $V_{DS} = 10$ V. This would be related to the point at which the electrons are released from the long time-constant traps because of the Poole-Frenkel effect as the electric field becomes large enough to reduce the time constant of the traps. This results in a hysteresis between the sweep up and the sweep down, since during the sweep down measurement, the donor traps are empty, so they do not lead to an increase in V_t.

However, a second trap mechanism can be observed here, which is the significant shift in V_t dependent on the voltage VDS. This is extremely noticeable with measurement $V_{DS} = 30$ V, where a new trapping mechanism has taken over, leading to a significantly larger V_t change. This is due to the charge and trapping that occurs in the gate dielectric at high V_{DS} values. Although this charging of the gate dielectric results in a reduced V_t it does not impact the kink effect and is instead a separate mechanism that is occurring. This charging effect on the gate dielectric has been shown to be reversible, as after reducing V_{DS} back to a low value, V_t recovers. The exact cause of this trapping effect and its effect on the device need further investigation to identify the exact mechanism occurring here.

5.2.5 Transfer Transconductance Overshoot

The transconductance overshoot highlighted in Figures 5.6a and 5.6b is a trapping effect that has been first published in [57]. In this paper, the trapping effect was attributed to impact ionisation releasing electrons from trap states that then remain empty for the remainder of the measurement, leading to a sudden increase in I_{DS} when V_{DS} is sufficiently high, and hysteresis in the sweep-down measurement where g_m overshoot no longer occurs. These findings are contrary to what has been observed in this section.

For the transconductance overshoots observed in this work, a primary overshoot

is observed at V_tNorm + 1.4 V, with a secondary undershoot occurring at V_tNorm +7.3 V in the forward sweep when V_{DS} = 10 V. When the drain voltage is increased to 30 V, these g_m spikes have not moved in terms of V_{GS} and instead a new undershoot has occurred at V_tNorm + 4.3 V. This indicates that as the drain-source electric field increases, more of these trap effects are becoming observable. When V_{GS} is swept down, the primary overshoot is removed, but the appearance of a new undershoot can be observed at V_tNorm + 5.6 V when V_{DS} = 10 V. Once again, as V_{DS} increases, more of these transconductance undershoots appear at: V_tNorm - 0.4 V, V_tNorm + 2.7 V, and V_tNorm + 5.6 V.

These g_m overshoots are completely independent of the device layout, occurring at the same V_{GS} values for all device variations including: Gate length, Gate Width, Drift Region, Gate Field Plates, and DC and RF configurations. They are also independent of the device threshold voltage and the voltage V_{DS} after a sufficiently large electric field is applied to reveal this effect. To confirm whether there is any temperature dependence, the RF devices were measured at 25 and 175 °C, the results of one of these devices shown in Figure 5.6. It is important to note that this RF device is significantly different to the the DC device in both layout and applied V_{DS} with V_{DS} = 10, and 30 V for the DC device, and V_{DS} = 10, and 20 V for the RF device. This was chosen to emphasise the independence of this overshoot from device layout and demonstrate that heating the device does not affect the location of the g_m overshoot, it does modify the V_{DS} required for it to occur. For example, the primary g_m overshoot at V_tNorm + 1.4 V, at 175 °C is very minor with V_{DS} = 10 V, where for 25 °C it is the first g_m overshoot to occur as V_{DS} increases. Each of the g_m overshoots exhibits different behaviour when heated, for example the g_m overshoot at V_tNorm + 4.3 V, which does not occur at V_{DS} = 10 V at 25 °C, actually becomes the most prominent at 175 °C, indicating that as the temperature has increased, the V_{DS} required for this overshoot has decreased. It has also been accompanied by a change in magnitude from an undershoot to an overshoot as the temperature has increased.

Overall, from these observations, it is currently believed that these traps are generated by the gate source or the gate substrate bias, which pushes thermally generated carriers into deep traps causing the V_t shift. Since this is still present at high temperature, the current assumption is that this is caused by deep traps with very short time constants due to the fast release of traps. Due to the constant V_{GS} of each g_m overshoot location, it is highly likely that the traps are well defined in the lattice structure, due to the consistency found with cross-wafer measurements.

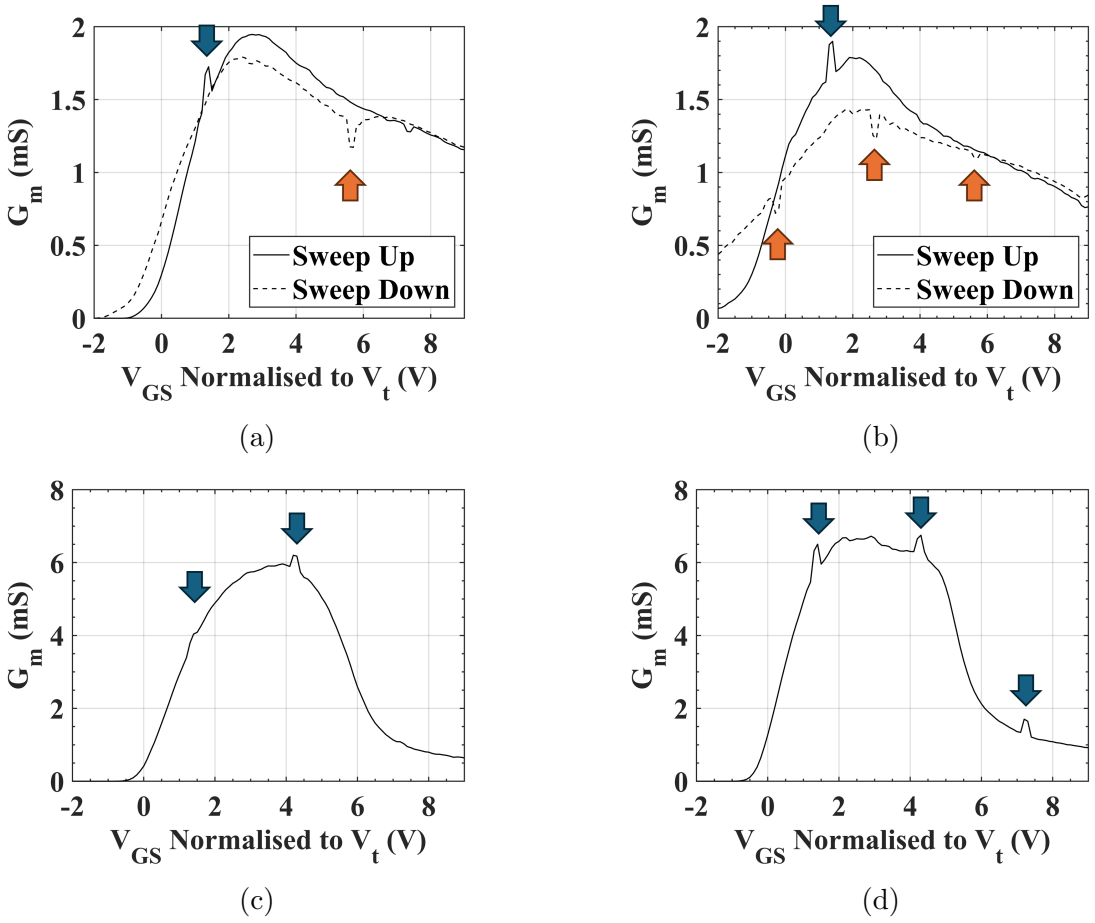


Figure 5.6: Transconductance overshoot at DC device at 25 °C for (a) $V_{DS} = 10$ V; (b) $V_{DS} = 30$ V; and RF device at 175 °C at (c) $V_{DS} = 10$ V; (d) $V_{DS} = 20$ V; where blue arrows indicate overshoot in sweep up, and orange arrows indicate overshoot in sweep down.

5.3 Conclusion

This section has thoroughly investigated the trapping effects observed in GaN HEMTs using DC-IV measurements.

The kink effect was observed in the output characteristics of the device and is attributed to long time-constant traps, causing a dynamic shift in the threshold voltage, leading to hysteresis between sweep-up and sweep-down measurements. This effect is a key indicator of trap stats changing within the device, as after the kink occurs, the device is operating in a state with fewer trapping effects than before the kink. Through observations on the effect of the device layout on the kink effect, it allows for the de-trapping method to be identified as both self-heating and the Poole-Frenkel effect. The self-heating and the Poole-Frenkel effect leads to the time constant of the traps being reduced to nearly zero which allows for the threshold voltage to recover. This results in the restoration of the drain current, which is observed as the kink in the output plots. The location of the traps causing the kink has also been identified as the AlGaN barrier. The effect of device design on the kink effect has also been considered with interesting results for gate field plates, where there are two competing mechanisms with the gate field plates. These are an increased kink due to the gate field plates acting as a heat sink, resulting in reduced device self-heating. This reduced self heating leads to this increased kink, due to the reduced thermal energy to assist the release of the traps. However, the gate field plates also lead to increased electron confinement in the 2DEG which for large drift regions such as 15 μm, results in the elimination of the kink effect as the traps remain empty throughout the measurement. These conflicting properties of the gate field plates lead to decreased device performance for short drift regions ($<$ 10 μ m), but increased device performance for larger drift regions ($\geq$ 10 μ m). This effect has also been observed in the DC-IV transfer measurements, with through hysteresis occurring leading to the dynamic threshold voltage.

The impact of varying the maximum drain-source voltage was also explored, allowing for multiple competing trapping mechanisms to be observed, resulting in

a dynamic threshold voltage, due to minority carrier trapping in the barrier at low V_{DS} values, and electron trapping in the barrier and buffer at high V_{DS} values.

A new trapping phenomenon has been observed in the output transconductance, taking the form of an output transconductance overshoot, which is not dependent on the gate-drain or gate-source electric field. Due to the low V_{DS} required for trapping and release of traps, it indicates that the traps are shallow and easily released by self-heating. These traps are currently assumed to be shallow acceptor traps located in the GaN channel close to the 2DEG.

Additionally a transfer transconductance overshoot has also been observed in the device transfer characteristics. This trapping effect occurs at fixed values of V_{GS} and is independent of the device layout. The temperature dependence leads to changes in the magnitude of the traps and the required V_{DS} to observe the transconductance overshoot, but it has no effect on the V_{GS} at which the overshoot occurs. The current assumption is that this occurs because of deep, short time-constant traps that are well defined in the lattice structure.

Through all of use of these DC-IV characterisation techniques it has been possible to identify multiple trap locations and states, allowing for the development of new understanding of the correlation between trap location and effect on device performance.

Chapter 6

Impact of Isolation Methods on GaN HEMT Performance

6.1 Introduction to Isolation Techniques

Device isolation is a crucial fabrication step in which GaN HEMTs are electrically separated to minimise leakage paths. This allows for improved device efficiency and breakdown behaviour [105].

The two primary isolation methods for GaN HEMTs are the following:

- Mesa Etch Isolation: This method physically isolates the active region of the GaN HEMT by etching away the surrounding material. Typically, this is performed using a Cl_2 plasma etch such as Inductively Coupled Plasma (ICP) etching or Reactive Ion Etching (RIE) [106]. In this work ICP was used for the mesa etch.

- Ion Implantation Isolation: This technique employs high-energy ion bombardment to create defects in the GaN heterostructure, which act as carrier trapping centres, pinning the Fermi level away from the conduction and valence bands. These defects include point defects, ion impurity defects, defect com-

plexes, local lattice disorder, and amorphization. Due to these defects, removing the free carriers, the ion-implanted region becomes electrically insulating, thus allowing the isolation of the device [105]. This can be done with various different ion species ranging from inert species such as Ar^+, Xe^+, Kr^+, and He^+ to reactive species such as H^+, Li^+, B^+, C^+, O^+, F^+, Al^+, Fe^+, N^+, Mg^+, [105], [107], [108], [109] [110].

Mesa etching has a significant advantage in that it is a lower-cost process and is more easily accessible than ion implantation [111].

The main drawback of mesa etch for isolation is that due to the non-planar nature of this method, there is typically increased gate leakage, and premature breakdown due to the gate metal having direct contact with the 2DEG on the mesa sidewall. However, this increased gate leakage can be reduced by expanding the mesa to include the gate feed [111], or mesa burying techniques such as the oxide-filled mesa method developed by [112]. This non-planar nature also leads to reduced device yield compared to planar methods such as ion implantation [109]. Ion implantation is therefore considered a solution to this problem because of the planar nature of the process. This avoids the previously mentioned problems with the mesa etch technique due to the removal of any side walls, and, as shown in [108], it was found that the use of ion implantation resulted in superior breakdown performance compared to mesa etch.

However, there is a significant drawback with ion-implantation isolation in that, through annealing, it is possible for the damaged area to recover and start conducting. Complete recovery typically requires a temperature above 1200 °C [105], however, partial recovery can occur at much lower temperatures of 600 °C [107], which can cause issues for high temperature processes, such as ohmic contacts. In [113], it was identified that the use of ion implantation can result in increased RF leakage compared to mesa isolation.

The following section details an investigation that compared these two meth-

ods of device isolation with the performance of devices using DC-IV, Pulsed-IV, Drain Current Transient Spectroscopy (DCTS) , and RF measurement techniques to determine the best fabrication method for targeted applications.

6.2 Device Fabrication

RF HEMTs were fabricated on a GaN-on-Si wafer purchased from NTT Advanced Technologies. This epitaxial structure was grown on 150 mm Hi-Res Silicon. The complete epitaxial structure and the layout of the devices are shown in Figure 6.1.

The devices were fabricated with 250 nm T-Gates, a Source-Drain spacing (L_{SD}) of 5 μm, a Source-Gate spacing (L_{SG}) of 1 μm, and a Drain Width (L_{WD}) of 32 μm. Multiple device variations were fabricated by increasing the Gate-Width (L_{WG}) and implementing multifinger devices with 2 to 6 fingers using a 300 nm nitride bridge.

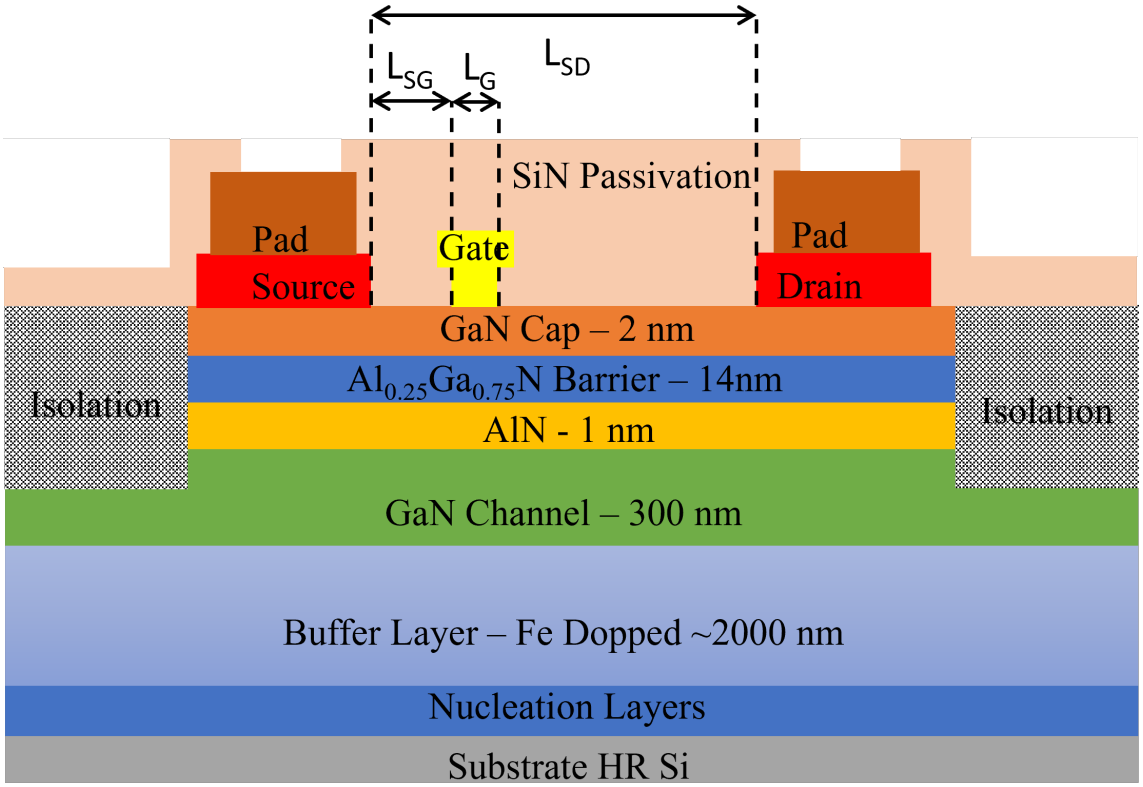


Figure 6.1: Device structure and Epi-Layers used for the isolation study.

Figure 6.2 summarises the complete fabrication process. For this study, a 25x25 mm token was used for fabrication. The upper half (cells 1 and 2) was protected

during the ICP-RIE etch step to prevent any etching, while the lower half (cells 3 and 4) was protected during the ion implantation step. This method allows for a direct comparison between fabrication variations using the same sample, eliminating potential issues related to wafer and fabrication run variability. In our fabrication process, it is important to note that we deposit and anneal the Ohmic contacts prior to device isolation, which ensures that the maximum temperature at which the ion implanted region is exposed to is 300 °C, preventing problems with increased leakage due to annealing occurring in the damaged region.

In this work for the mesa etch, low-damage ICP-RIE was performed using Cl_2 and Ar gases. For ion implantation, Ar^+ ions have been used due to the effect of a heavy mass ion creating displacements in a shallower location with a higher concentration. This leads to increased lattice damage and disorders and allows the ion-implanted region to withstand higher temperature processes than lower-mass ions [114].

The resulting fabricated devices with ion implantation isolation had an ohmic contact resistance of 1.69 $\Omega.mm$ and a 2DEG sheet resistance of 325 $\Omega/\square$.

A completed 4-finger GaN HEMT device with a 25 μm gate width is depicted in Figure 6.3. Detailed SEM images of the mesa etched device (Figures 6.3b and 6.3c) highlight a clear trench encircling the active region. In contrast, the device implanted with ions (Figures 6.3d and 6.3e) does not exhibit this distinct trench, as the isolation process involves the physical damage induced by high-energy ion implantation into the 2DEG channel.

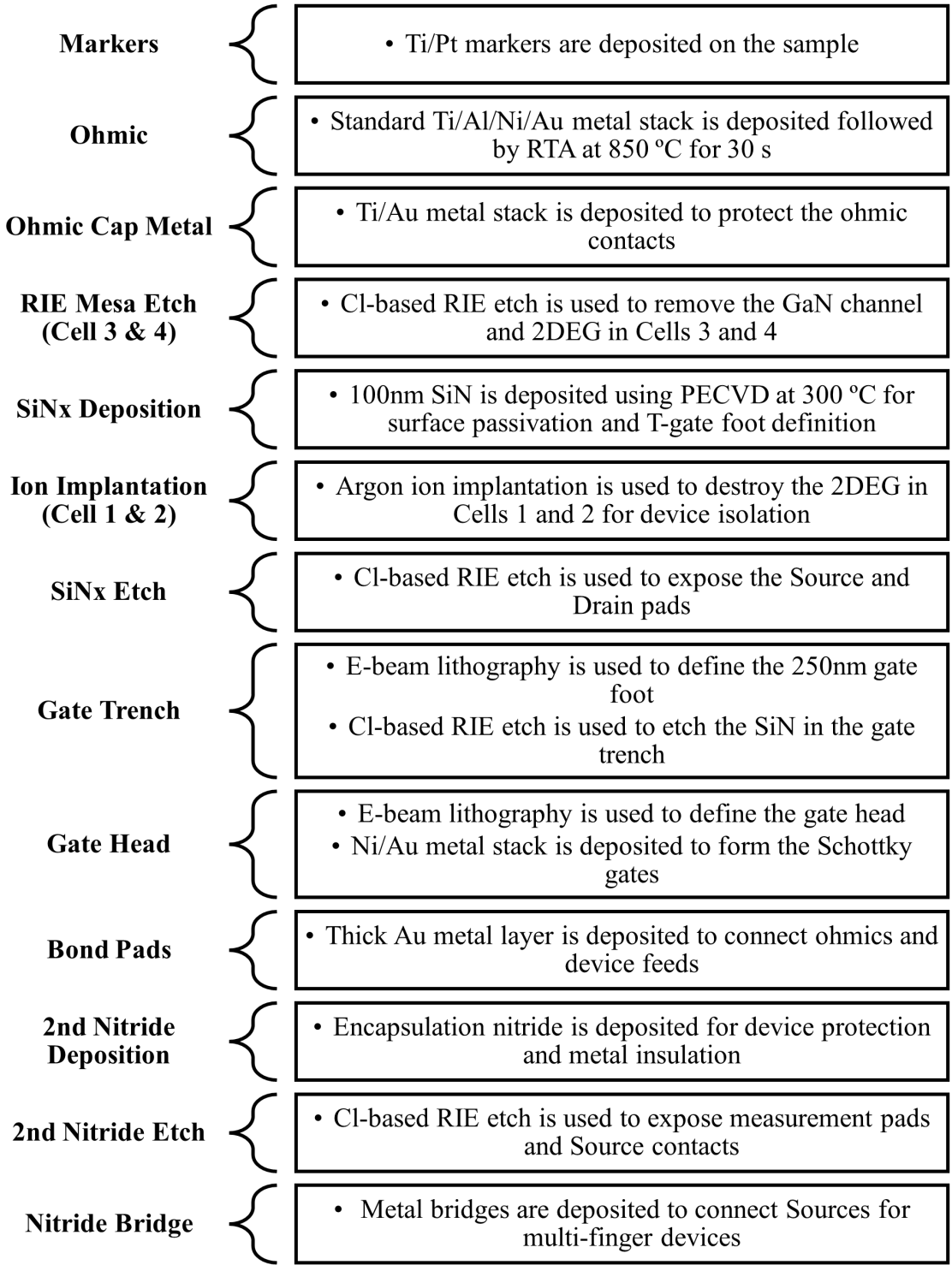
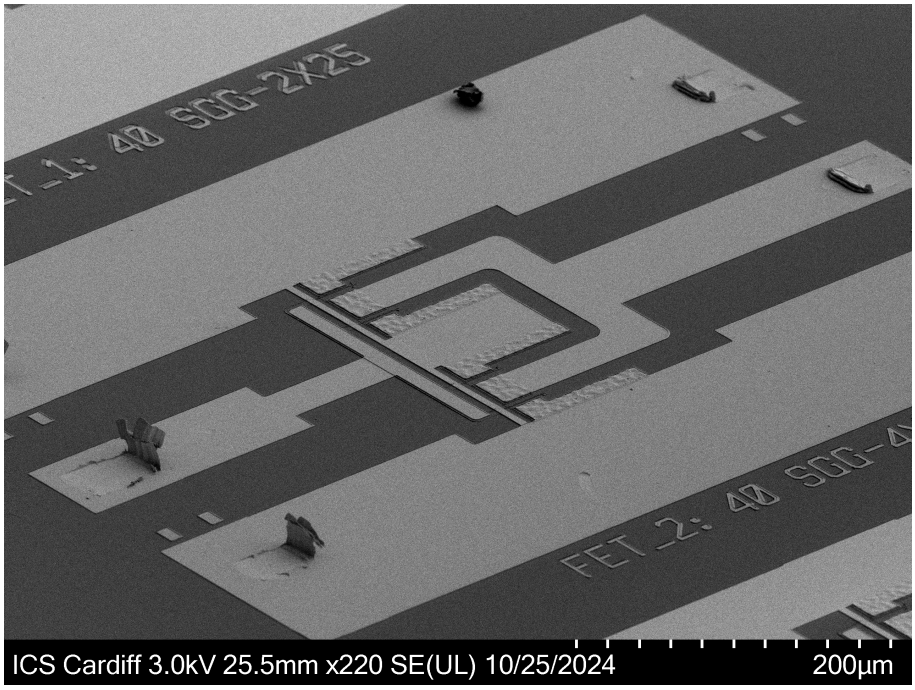
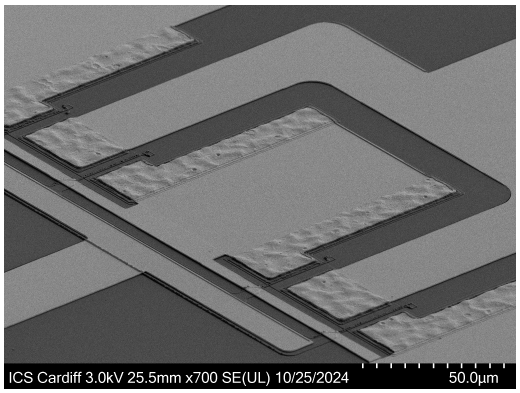


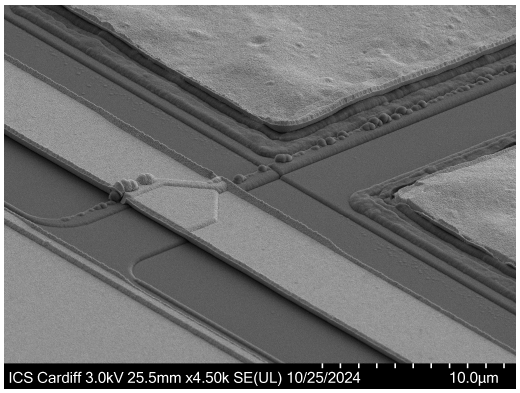
Figure 6.2: Flowchart of the Fabrication Process



(a)



(b)



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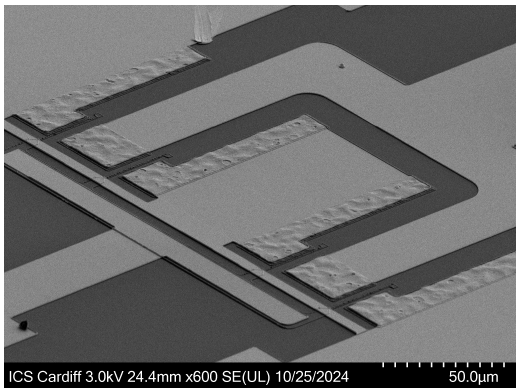
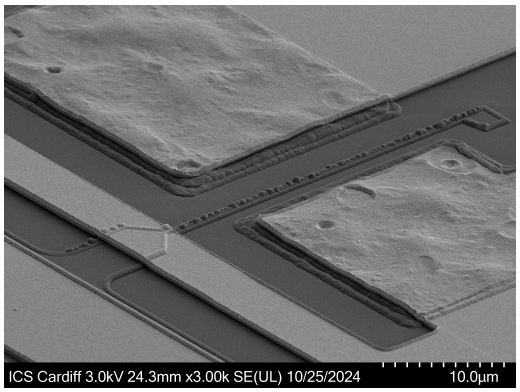


(d)



(e)

Figure 6.3: Scanning electron microscopy (SEM) images of a fabricated 4-finger device with a 25 μm gate width are presented. (a) shows the full device layout with, (b) and (c) showing the device isolated by RIE mesa etch, the core of the device with nitride bridge (b) and close-ups of the gate, source, and drain regions (c). Figures (d) and (e) depict the same device isolated by ion implantation, the core of the device with nitride bridge (d) and with zoomed-in views of the gate (e).

6.3 Device Measurements

6.3.1 DC-IV Measurement Results

DC-IV measurements were performed at 25 °C, 55 °C, and 85 °C to characterise the electrical performance and thermal stability of the devices. This temperature range was selected to simulate the expected operating conditions provided by the industry partner for this project.

The DC-IV measurements were conducted in a dark, temperature-controlled environment using a 200 mm semi-automatic thermal probe station. The Keysight B2902A Source Measure Unit (SMU) was used to perform the DC measurements. The SMU unit was connected to GSG RF Probes via Auriga 67 GHz, 50 V, 1 A Bias tees. A 50 Ω load was connected to the RF port to suppress device oscillations during the measurements.

DC-IV transfer characteristic measurements ($I_{DS}V_{GS}$) were performed with gate voltage (V_{GS}) swept from -4 to 1 V steps of 100 mV, with drain voltage (V_{DS}) held at 15 V.

DC-IV output characteristics measurements ($I_{DS}V_{DS}$) were then performed with gate voltage (V_{GS}) swept from -4 to 1 V steps of 0.5 V, with drain voltage (V_{DS}) swept from 0 to 15 V in 0.375 V steps.

The DC-IV characteristics of a 2-finger, 100 μm device, employing both mesa etch and ion implantation isolation techniques, are presented in Figure 6.4. The key performance metrics extracted from these characteristics are summarised in Table 6.1.

Ion implantation isolation demonstrated significant improvements in several key performance metrics compared to the traditional mesa etch technique.

- Reduced I_{GS} Leakage: A nearly three-order-of-magnitude reduction in gate leakage current was observed at V_{DS} = 10 V, this leads to a significant improvement in device reliability.

- Reduced I_{DS} leakage: A nearly two-order-of-magnitude reduction in the source-drain leakage current was observed, significantly improving the device's off-state characteristics.

- Steep subthreshold slope: The subthreshold slope was reduced by more than four times, which led to improved device pinch-off characteristics.

The improvement in these three key performance metrics results in a significant improvement in device pinch-off behaviour, with reduced off-state current leakage and improved device performance at higher drain voltages and potentially higher breakdown voltage.

Table 6.2 presents the percentage difference in device performance between 25 °C and 85 °C.

Although both isolation techniques exhibited a decrease in performance at elevated temperatures (85 °C), looking at the impact of increased temperature, there are two key parameters where there is a significant deviation between the two methods.

- I_{GS} Leakage: The first is the increase in the gate leakage current, while both have a significant increase in leakage current, the mesa etch shows a huge increase of 276 % compared to 97.0 % for ion implantation. This highlights the key issue with gate leakage in mesa-isolated devices, as this could lead to premature breakdown and device reliability issues.

- I_{DS} Leakage: The second significant deviation is with the source-drain leakage, where the devices with ion implantation demonstrated a larger increase in the source drain current of 55.6 % when compared to the mesa etched devices which had an increase of 32.8 %. However, it is important to note that even at 85 °C, the ion-implanted devices still maintained significantly lower leakage currents than the mesa etched devices.

Overall, the use of ion implantation as an isolation technique leads to an improvement in all aspects of device performance, but the most dramatic improvement

comes in the almost 2 orders of magnitude lower device leakage and over 4 times lower subthreshold slope which lead to vastly improved pinch-off characteristics.

Table 6.1: DC-IV measurement results at 25 °C and 85 °C

DC-IV Measurement Results 25 °C		
Parameter	Mesa Etch	Ion Implant
Threshold Voltage (V)	-2.47	-1.90
Source Drain Leakage (A/mm)	2.04×10^{-3}	1.44×10^{-5}
Gate Leakage (V_{DS} = 10 V) (A/mm)	9.12×10^{-6}	1.01×10^{-8}
Saturation Current (A/mm)	0.44	0.45
Peak Transconductance (mS/mm)	214	240
Subthreshold Slope (mV/decade)	834	192
On-Resistance (Ω/mm)	4.07	3.89
DC-IV Measurement Results 85 °C		
Parameter	Mesa Etch	Ion Implant
Threshold Voltage (V)	-2.55	-1.92
Source Drain Leakage (A/mm)	2.71×10^{-3}	2.33×10^{-5}
Gate Leakage (V_{DS} = 10 V) (A/mm)	3.43×10^{-6}	1.99×10^{-8}
Saturation Current (A/mm)	0.43	0.44
Peak Transconductance (mS/mm)	181	203
Subthreshold Slope (mV/decade)	1040	213
On-Resistance (Ω/mm)	5.81	5.00

Table 6.2: Impact of Temperature on DC-IV measurements, showing the reduction of device performance at 85 °C compared with 25 °C

Parameter	Mesa Etch	Ion Implant
Threshold Voltage Increase	3.24 %	1.05 %
Source Drain Leakage Increase	32.8 %	55.6 %
Gate Leakage Increase	276 %	97.0 %
Saturation Current Decrease	2.27 %	2.22 %
Peak Transconductance Decrease	15.0 %	15.4 %
Subthreshold Slope Increase	25.7 %	10.9 %
On-Resistance Increase	42.5 %	28.4 %

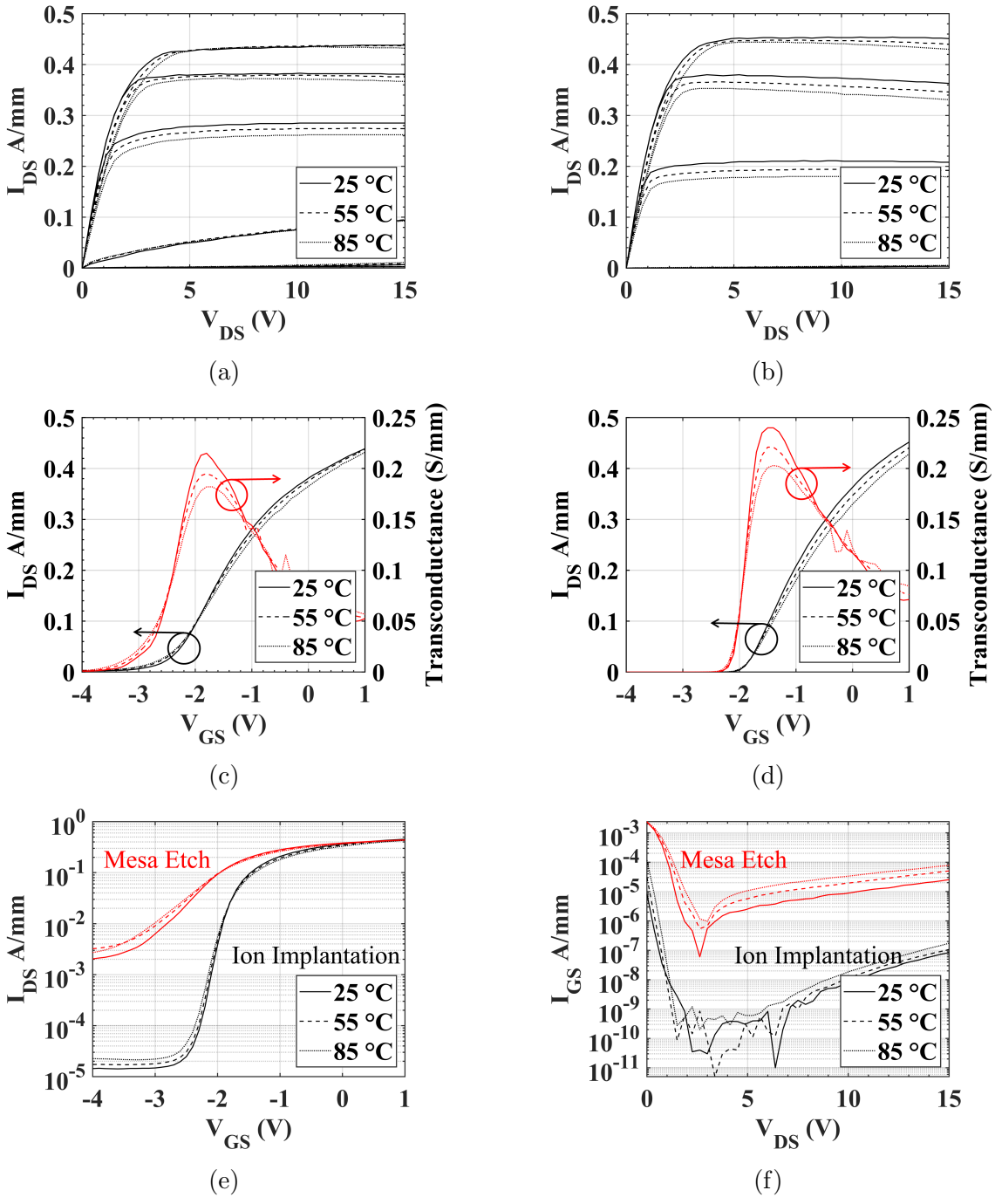


Figure 6.4: Temperature-dependent DC current-voltage characteristics of 2-finger, 100 μm gate width GaN high-electron-mobility transistors (HEMTs): (a) and (b) Output characteristics $I_{DS}V_{DS}$ for mesa etched and ion-implanted devices, respectively; (c) and (d) Transfer characteristics $I_{DS}V_{GS}$ for mesa etched and ion-implanted devices, respectively; (e) Logarithmic scale transfer characteristics for both isolation methods; (f) Logarithmic Gate leakage current for both isolation methods where V_{GS} = 1 V.

6.3.2 Pulsed-IV Measurement

Pulsed-IV measurements were performed to determine the impact of isolation methods on current collapse and R_{on} shift. The Pulsed-IV measurements were conducted in a dark, temperature controlled environment using a 200 mm semi-automatic thermal probe station. The Auriga Tri-State PIV from Focus Microwave was used to perform the pulsed measurements. This system was then connected to GSG RF Probes via Auriga 67 GHz, 50 V, 1 A Bias Tees. A 50 Ω load was connected to the RF port to suppress device oscillations during the measurements. The pulse was set to a 1 μs pulse width, with a duty cycle of 0.01 %. This was chosen to minimise any impact of self-heating on the device performance, along with ensuring a short pulse to enable trap stats to be correctly filled or emptied between measurements.

Pulsed-IV transfer characteristic measurements ($I_{DS}V_{GS}$) were performed with measurement non-quiescent (NQ) points for gate voltage (V_{GS}) swept from -4 to 1 V steps of 100 mV, and drain voltage (V_{DS}) held at 15 V.

Pulsed-IV output characteristics measurements ($I_{DS}V_{DS}$) were then performed with measurement points (NQ) for gate voltage (V_{GS}) swept from -4 to 1 V steps of 0.5 V, and drain voltage (V_{DS}) swept from 0 to 15 V in 0.375 V steps.

For both of these measurement sweeps 4 different sets of quiescent (Q) points are used: (For this section the pulsed measurements, Q points will be notated as (QV_{GS}, QV_{DS}))

- Continuous DC: This is a standard DC measurement and will allow for a comparison between continuous DC-IV and Pulsed-IV measurements (NQ = Q points).
- Cold Pulsed-IV: This is a Pulsed-IV measurement where the Q points are set to (0,0), which removes any electric field across the device and allows the traps to all empty.

- Gate-lag Pulsed IV: This is a Pulsed-IV measurement in which the Q points are set to (-4,0), which will cause the traps dependent on the V_{GS} traps to be filled and the traps dependent on V_{DS} to empty. This will allow the effects of surface-state traps to be observed as a "gate-lag" compared to the cold pulsed-IV measurement.

- Drain-lag Pulsed IV: This is a Pulsed-IV measurement in which the Q points are set to (-4,15), which will cause the traps dependent on both V_{GS} and V_{DS} to be filled. This will allow the effects of bulk-state traps to be observed as a "drain-lag" when compared to the gate-lag Pulsed-IV measurement.

Figure 6.5 shows the pulsed-IV characteristics of a 6-finger, 100 μm GaN HEMT device, comparing the mesa etch and ion implantation isolation techniques. The key performance metrics are summarised in Table 6.3.

Under pulsed-IV stress, the ion-implanted device exhibits significantly superior performance compared to that of the mesa etched device. The ion-implanted device shows minimal current collapse and R_{on} degradation under both gate-lag and drain-lag conditions. In contrast, the mesa etched device suffers from significant current collapse and R_{on} degradation, especially under gate-lag stress.

Looking at the current collapse at $V_{GS} = 1V$ and $V_{DS} = 10V$, the mesa isolated device shows a current collapse of 36.4 % and 27.2 % under gates and drain-lag stress situations, respectively; this compares with 2.73 % and 0.15 % for the ion implantation device. Comparing R_{on}; for mesa isolation we have an increase of 94.7 % and 23.2 % for gate-lag and drain-lag, respectively, and for ion isolation we have an increase of 0.51 % and 8.69 % for gate-lag and drain-lag, respectively. This observed degradation in the mesa etch device indicates a significant increase in trap states in the device that have been directly caused by damage during the mesa etch. The particularly severe pinch-off degradation under cold pulse conditions seen in Figure 6.5e, is attributed to this increase in interface trap states. This shows that the mesa etch process has caused a significant deterioration in the ability to modulate the gate of the device; when the gate voltage is pulsed down for measurements in the

short 1 μs duration.

Table 6.3: Continuous DC-IV and pulsed-IV measurement key parameters. current density and current collapse has been taken from where $V_{GS} = 1V$, and $V_{DS} = 10V$

Parameter	Mesa Etch	Ion Implant
Continuous DC Current Density (A/mm)	0.46	0.47
Cold Current Density (A/mm)	0.52	0.52
Gate-lag Current Collapse	36.4 %	2.73 %
Drain-lag Current Collapse	27.1 %	0.15 %
Continuous DC R_{on} (Ω/mm)	6.58	6.30
Cold R_{on} (Ω/mm)	6.42	5.84
Gate-lag R_{on} (Ω/mm)	12.5	5.87
Drain-lag R_{on} (Ω/mm)	15.4	6.38

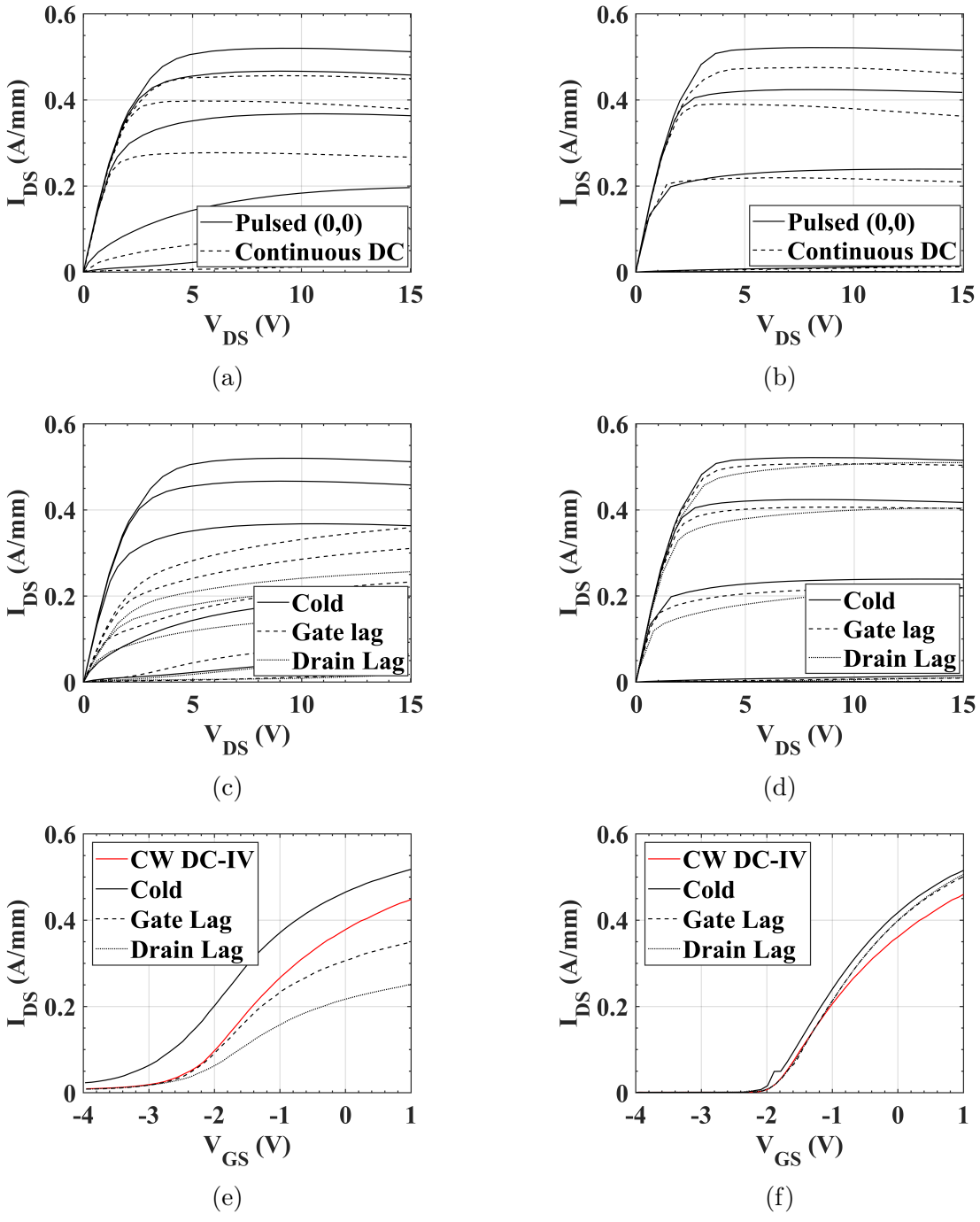


Figure 6.5: Pulsed-IV characteristics of 6-finger, 100 μm gate width GaN high-electron-mobility transistors (HEMTs): (a) and (b) show the CW-DC and cold pulse-IV Comparison for mesa etch and ion implantation respectively; (c) and (d) shows the comparison between cold, gate-lag, and drain-lag pulsed-IV measurements for mesa etch and ion implantation respectively; (e) and (f) shows the comparison between cold, gate-lag, and drain-lag transfer characteristics for mesa etch and ion implantation respectively.

6.3.3 Thermal Dependent Drain Current Transient Spectroscopy Measurements

Drain Current Transient Spectroscopy (DCTS) measurements have been performed at three different temperatures (25, 85, and 125 °C) to compare trap energy levels between isolation methods. These measurements were performed in a dark, temperature controlled environment using a 200 mm semi-automatic thermal probe station. The Auriga Tri-State PIV from Focus Microwave was used to perform the pulsed measurements, using the long-pulse measurement capability. This system was then connected to GSG RF Probes via Auriga 67 GHz, 50 V, 1 A Bias Tees. A 50 Ω load was connected to the RF port to suppress device oscillations during the measurements. The long pulse was set with a span of 1 s, and the sample rate was initially set to 1 MHz and downsampled by 1 order of magnitude every decade after the pulse. After each measurement, the bias of the device was set at $V_{GS} = 0$ V and $V_{DS} = 0$ V, to ensure that the device was in a known state before and after each measurement.

The three key stages of the long pulse measurement are:

- Trap Filling Period: 500 μs filling period.
- Pulse Period: 500 μs pulse width.
- Recovery Period: post-pulse to 1 s.

Two pulsing methods were performed: a single drain pulse, where QV_{DS} is pulsed from a low steady-state value to a high value and QV_{GS} is kept constant above the threshold voltage; and a dual pulse where QV_{DS} is pulsed from a low steady-state value to a high value, and QV_{GS} is simultaneously pulsed from the steady-state value to below the threshold voltage to pinch off the device. The steady-state values are defined as Q points and the values during the pulse period are defined as NQ points. In this study, the Q points were taken as $QV_{DS} = 2$ V, QV_{GS} = -1.93 and -1.63 V for mesa etch and ion implantation, respectively. These Q points are constant

between both pulse methods. For the single drain pulse, the NQ points are: NQV_{GS} = QV_{GS}, NQV_{DS} = 15 V. For the dual pulse, the NQ points are: NQV_{GS} = -4 V and NQV_{DS} = 15 V. The values of QV_{GS} were chosen to set the current in each device to approximately 50 mA/mm when V_{DS} = 2 V, this relates to $V_{GS} = V_t$ + 0.54 V for mesa isolation and $V_{GS} = V_t$ + 0.27 V for ion implantation. This discrepancy between the threshold voltage and the chosen value is due to the worse subthreshold slope and pinch-off characteristics of the mesa etch.

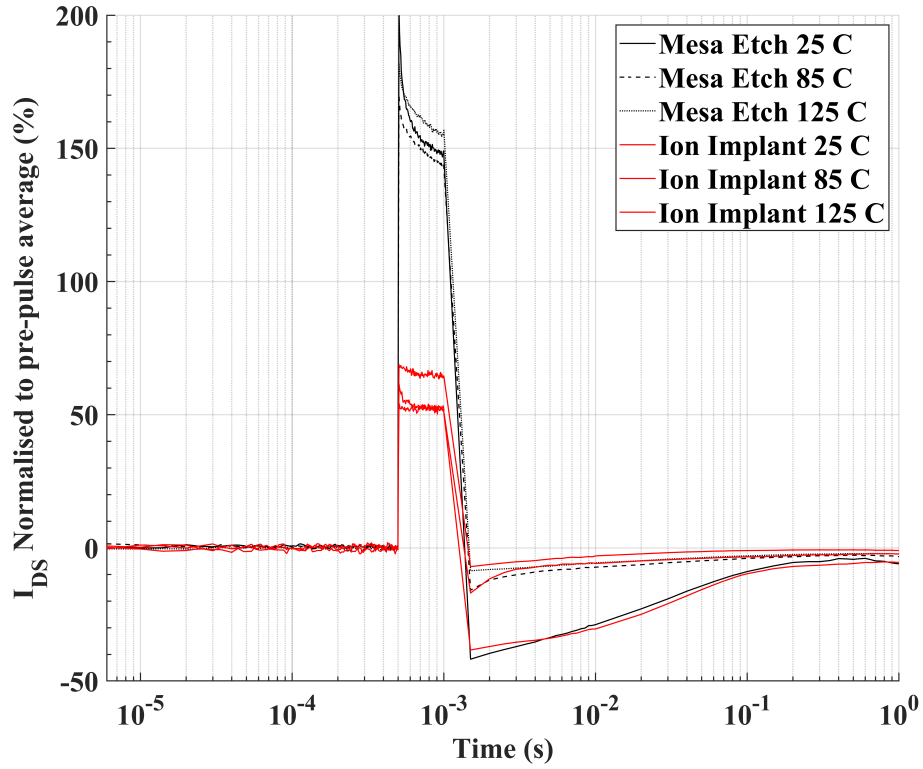
Both pulse methods were performed to determine the location of the traps and the effect of the isolation method on the trap time constants and the maximum drop in drain current after pulsing. Performing these measurements at several temperatures allows us to compare the change in trap time constants and extract trap energy levels.

The single drain pulse is a key indicator of drain-lag, and the dual pulse is a key indicator of both gate and drain-lag. Looking at the results presented in Figure 6.6a, there is a noticeable difference between mesa etch and ion implantation during the pulse stage. The mesa etch exhibits a significantly higher maximum current than ion implantation after V_{DS} is pulsed high. This increase is likely due to the shifting threshold voltage during the pulse, as seen before in Figure 6.5e. The percentage increase of 150 % tracks what would be expected if the threshold shifted as previously seen in the short-pulse measurements. This hypothesis is further supported by the dual pulse measurement Figure 6.6b, where when V_{GS} is pulsed to -4 V, the device does not pinch off correctly, which would be expected if the device pinch-off characteristics have shifted during the measurement in the same way that was observed in the cold FET short-pulse measurements.

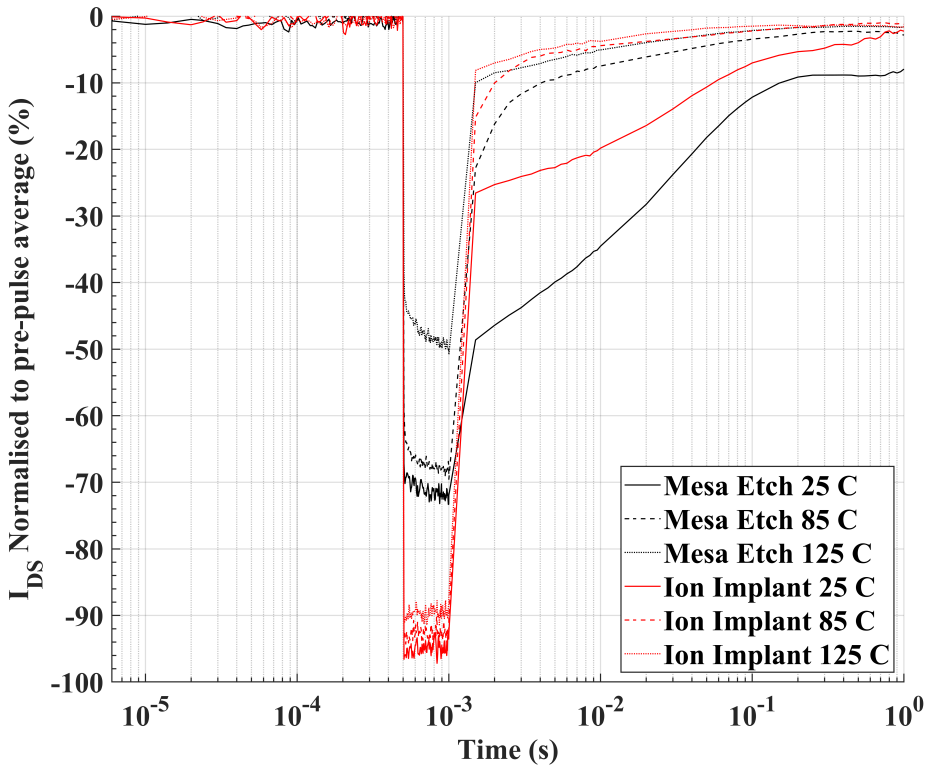
Now looking at the recovery after the pulse, we can see that for the drain-lag measurement, there is minimal difference in recovery between mesa etch and ion implantation, indicating that the isolation methods have not had any impact on the deep-level traps, which are exposed through this measurement technique. However, when examining recovery after dual pulse measurement, there is a significant im-

provement in current recovery with ion implantation. This recovery can be observed in the maximum drop in drain current. At 25 °C, 500 us after the pulse, the drop in current for mesa etch is 48.6 % and 26.6 % for ion implantation. This indicates that there are significantly more trap states generated during the mesa etch process than during the ion implant process. As the overall sum of time constants does not seem to change significantly, it is likely that there are no new additional trap states, but instead a significant increase in surface trap stats that are likely due to the damage to the surface during the mesa etching process.

Due to measurement equipment limitations presenting issues with the noise floor, it is not possible to extract trapping energy states with certainty since Bayesian deconvolution is unable to reliably extract the transients. Any attempted filtering steps applied before lead to obscuring the transients in such a way that they Bayesian deconvolution stage will present a perfectly smooth signal. This will be addressed in future work with modifications to the measurement procedure, such as implementing multiple measurements and averaging to reduce noise, and further improvements to the system to allow for a lower noise floor to complete the analysis to determine the energy level of all traps.



(a)



(b)

Figure 6.6: DCTS measurement results for a 6-finger, 100 μm gate width GaN high-electron-mobility transistors (HEMTs) with two different pulse conditions: (a) V_{GS} held constant V_{DS} pulsed from 2V to 15 V; (b) V_{GS} pulsed to below V_t and V_{DS} pulsed 2 V to 15 V.

6.3.4 Small Signal RF Measurements

Small-signal RF measurements were performed to determine the influence of isolation methods on intrinsic and extrinsic device parasitics, as well as the effect of these isolation techniques on essential RF performance metrics f_t and f_{MAX}. On-Wafer measurements were performed using 150 μm GSG RF probes. The measurements were carried out on a 200 mm semi-automatic probe station, utilising a Keysight Power Network Analyzer (PNA) model N5227B. This was interfaced with the Keysight N5293AX03 range extenders, which extend the range to 0.1 to 120 GHz and incorporate built-in bias tees. In addition, a Keysight B1500a semiconductor device parameter analyser was used for DC biasing and measurements. Both PNA and B1500a were controlled by Keysight IC-CAP software. Probe tip calibration was performed through enhanced Line-Reflect-Reflect-Match Reflect (eLRRM) using the MPI AC2 calibration substrate. After calibration, several de-embedding structures were measured on-wafer to allow for TRL de-embedding to remove the effect of the feed structures from the measurements.

RF measurements were performed from 0.1 to 67 GHz at multiple different bias points to allow for de-embedding and small-signal model extraction:

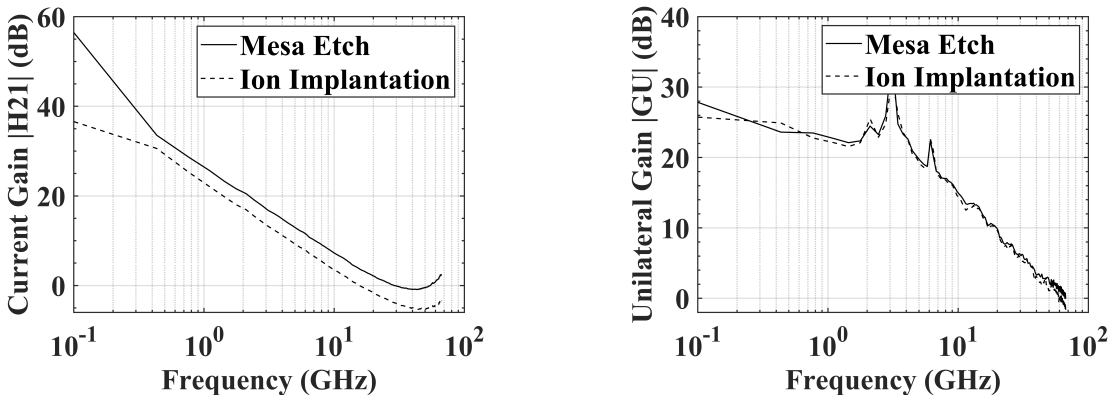
- Pinch Off FET: $V_{GS} << V_t$ Here the gate voltage is set to below the threshold voltage and V_{DS} is set to 0 V, to ensure a cold FET configuration.
- Hot FET: Here, V_{GS} is set for the maximum G_m and V_{DS} is set to 15 V.
- Forward bias: Here we ensure V_{DS} is set to 0 V, and then bias the gate to forward conduction to a specific gate current. For this type of measurement, three measurements are performed with gate current (I_{GS}) set to 200 μA/mm, 400 μA/mm, and 600 μA/mm for each measurement.

The results of the small signal measurements for f_t and f_{MAX} are presented in Figure 6.7 and extracted in Table 6.4 for a device of 4 fingers and 25 um gate width.

The device extrinsic and intrinsic parameters have been extracted and are shown in Table 6.5. There is a notable distinction between mesa etch and ion implantation isolation techniques, with mesa etch demonstrating a considerable advantage in relation to f_t and f_{MAX}. Specifically, the mesa etch exhibits an approximate twofold increase from 15.49 to 28.87 GHz in f_t compared to ion implantation. In f_{MAX}, a more modest enhancement is noted, with the mesa etch increasing to 66.3 GHz, in contrast to the 59.6 GHz observed for ion implantation. This difference in RF performance is due to a decrease of 24 % to intrinsic Gm and a significant increase of 32.17 % in C_{GS}.

Table 6.4: Small signal RF f_t and f_{MAX} for comparing mesa etch and ion implantation

Parameter	Mesa Etch	Ion Implantation
f_t	28.87 GHz	15.49 GHz
f_{MAX}	66.3 GHz	59.6 GHZ



(a) (b)

Figure 6.7: RF S-Parameter measurement results showing (a) f_t and (b) f_{MAX}

Table 6.5: Comparison of extracted values for Extrinsic and Intrinsic parameters for mesa etch and ion implantations

Extrinsic Parameters			**Intrinsic Parameters**		
Parameter	Mesa Etch	Ion Implantation	**Parameter**	Mesa Etch	Ion Implantation
C_{pg} (fF)	8.35	4.09	C_{gd} (fF)	36.7	30.7
C_{pd} (fF)	21.8	49.0	C_{gs} (fF)	143	189
L_s (pH)	11.15	13.2	C_{ds} (fF)	50.1	36.3
L_g (pH)	35.0	34.8	τ (ps)	1.50	2.24
L_d (pH)	49.8	50	G_m (mS/mm)	269	204
R_d (Ω)	1.84	2.95	R_{in} (Ω)	0.645	0.126
R_s (Ω)	0.0210	1.44	R_{ds} (Ω)	566	1070
R_g (Ω)	3.66	3.32			

6.4 Conclusion

The DC-IV measurement results indicate that ion implantation significantly improves key performance metrics over mesa etch, enhancing off-state current control and performance at elevated drain voltages. At higher temperatures (85 °C), both methods showed a decrease in performance, particularly in gate leakage, where the increase in gate leakage for mesa etch devices is greater than the increase for ion-implanted ones. Although source-drain leakage increased more in ion-implanted devices, they still maintained 1 order of magnitude lower leakage compared to mesa etched devices at 85 °C. These findings highlight the benefits of ion implantation in minimising gate leakage and improving device performance and reliability under thermal stress.

Looking at the impact of these two isolation methods on trapping in the device, the comparative analysis of pulsed-IV characteristics between mesa etching and ion-implantation isolation techniques demonstrates that the ion-implanted device exhibits markedly enhanced performance. The ion-implanted device shows minimal current collapse and R_{on} degradation under gate and drain-lag conditions. In contrast, the mesa etched device undergoes considerable current collapse and R_{on} degradation, especially under gate-lag stress. The pronounced pinch-off degradation observed in the mesa etched device under cold pulse conditions is probably attributable to increased interface trap states resulting from the etching process, indicative of significant charge-trapping issues. The DCTS results indicate that mesa etch has issues with shifting threshold voltage observed through an increase in maximum current during the single pulse and the lack of pinch off during the dual pulse, when compared to ion implantation. However, after pulsing, there is a minimal difference in drain-lag recovery between isolation methods, suggesting that there is no impact on deep-level traps. The dual pulse shows an improved drain current recovery with ion implantation, suggesting fewer trap states compared to mesa etch. This improvement is likely due to an increase in the surface trap states caused by damage during the mesa etching process.

When comparing the RF results, it is apparent that there are significant issues with the RF performance of the ion isolated devices. Possibly due to the fact that ion implantation is causing increased RF leakage [113].

However, in previous work in [115] similar results were documented for the DC-IV and Pulsed-IV measurement results, which is consistent with this work, but it was found that with ion implantation there was a 17 % improvement in f_t due to increased intrinsic G_m and reduced C_{GD} and C_{GS}. These RF results contrast with our results and merit further investigation into the cause of this issue with RF performance decreasing with ion implantation over mesa etch.

Chapter 7

Impact of AlGaN Barrier Thickness on GaN-on-Si RF HEMT Performance and Trapping Effects

7.1 Introduction to Barrier Thickness Scaling

To enhance the high-frequency RF performance of AlGaN HEMTs, it is essential to reduce the gate length. Reducing the gate length, reduces the gate-to-drain capacitance (C_{GD}), which leads to an increase in both f_t and f_{MAX} enhancing high-frequency RF performance [116]. However, in making such adjustments, it is crucial to preserve the structural aspect ratio of the gate length to the gate channel distance to mitigate issues such as short-channel effects, which can compromise device performance [117]. Short channel effects lead to pinch-off issues, reduced transconductance (g_m), increased output conductance, and threshold voltage shift. The described ratio (L_g:Barrier thickness) should ideally be within the range of 15:1 [118] [119].

In alternative technology such as GaAs and InP HEMTs, a gate recess fabri-

cation step is performed, where the barrier is etched to position the gate closer to the channel. This allows for aggressive scaling of the gate length. However, in the GaN material space, due to the ceramic-like properties, it is highly resistant to wet etching, and dry etching leads to the formation of significant defects because of the high level of strain in the AlGaN barrier layer. These defects lead to the creation of significant trap states, leading to performance deterioration and reliability issues [116]. Although there have been several examples of successful gate recess techniques for AlGaN / GaN [120] [30], it is generally agreed that to ensure robust fabrication, it is better to focus on planar devices where the aspect ratio is maintained by shrinking the whole barrier layer. This is due to the increased reliability, and avoids the increased surface traps that are caused via the gate recess process. However, reducing the barrier thickness comes with its own challenges, as when the barrier thickness is reduced there is a reduction in channel sheet carrier density. Whilst this can be minimised by increasing the percentage of Al in the AlGaN barrier, this increases the number of defects in the structure and thus the trap states due to the increased strain from the increased lattice mismatch [116].

The study in [117] examined the effect of reducing the barrier thickness from 22 to 18 nm while maintaining a gate length of 100 nm, revealing that a barrier of 22 nm exhibited short-channel effects attributed to the aspect ratio of the gate falling below 5:1. However, attempts to decrease barrier thickness to below 20 nm result in a diminished channel sheet carrier density, which leads to the formation of surface donors and consequently surface trap states. However, this can be mitigated through the application of SiN passivation [121]. A suggested method to maintain the ratio between L_g and the distance to the channel is to etch a gate recess, although this approach has been documented to cause significant complications, including increased gate leakage and damage to the gate access region. The resultant damage to the gate area leads to a substantial increase in surface trapping states, which adversely affects the large signal RF performance of the device [122].

The investigation in [123] on the impact of the thickness of the AlGaN barrier on the linearity of the AM / PM of the device indicates that although reducing the thickness of the AlGaN barrier enhances G_m and the gain, it also poses a trade-off by degrading the linearity of the device. An additional advantage of reducing the AlGaN barrier thickness is the resulting increase in V_t to a more positive value [124]. In [125], it is discussed that reducing the thickness of the AlGaN barrier below the subcritical thickness, estimated at approximately 3 nm, can facilitate the creation of devices in E mode. This is further explored in [126], where a model is developed to increase the critical thickness considering the surface potential. The study in [61] investigates the influence of barrier thickness on current dispersion at RF frequencies in AlGaN/GaN HEMTs, indicating that this dispersion results in reduced output power and power-added-efficiency (PAE) in comparison to DC operation. This dispersion is generally attributed to trapping states that function as acceptors, brought about by threading dislocations and surface states proximal to the gate. The study found that this effect intensifies as the barrier thickness decreases, due to increased electric field within the barrier layer, with the optimal barrier thickness identified as 20 nm.

In this section, an investigation was conducted that compares the effect of three different barrier thicknesses on the performance of devices. The thicknesses of the AlGaN barriers are shown in Table 7.1.

Table 7.1: AlGaN Barrier Thickness Wafer Table.

Parameter	AlGaN Barrier Thickness (nm)
Wafer A	21
Wafer B	15
Wafer C	9

7.2 Device Fabrication

RF HEMTs were fabricated on a GaN-on-Si wafer provided by the University of Cambridge. This epitaxial structure was grown on 150 mm Hi-Res Silicon. The complete epitaxial structure and the layout of the device are shown in Figure 7.1.

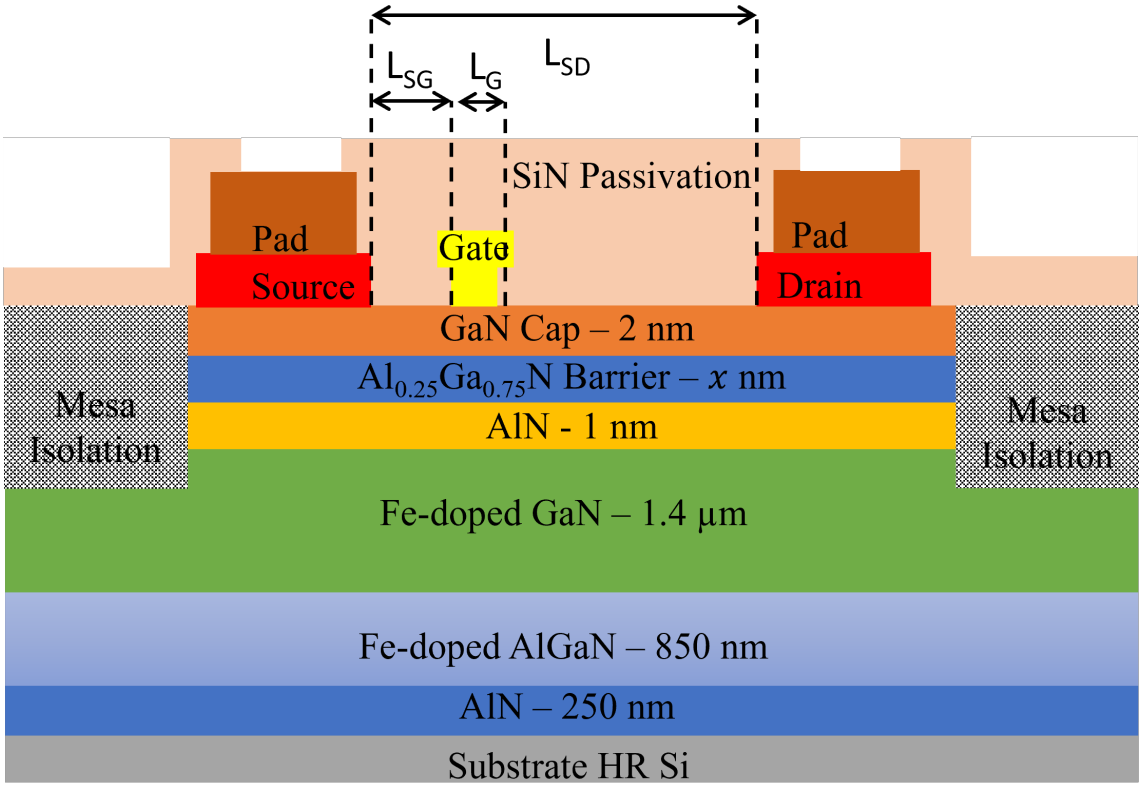


Figure 7.1: Device Structure and Epi-Layers used for this barrier layer study.

The devices were fabricated with fixed 1 μm T-Gates and Source-Gate spacing (L_{SG}) of 1.5 μm. The devices have the following topology variations:

- Source Drain Spacing (L_{SD}) of 4 and 5 μm.
- Drain Width (L_{WD}) of 32 and 52 μm
- Gate Widths of ((L_{GW}) 50, 125, 150, 200, 250, and 300 μm.

The complete fabrication process is summarised in the flow chart in Figure 7.2. For this study, a 25x25 mm token of each wafer was used for fabrication. These samples were fabricated together and put through each fabrication step simultaneously to ensure that the fabrication variation between each sample is minimised.

The resulting fabricated devices ohmic contact and sheet resistance is shown in Table 7.2.

Table 7.2: Ohmic Contact and Sheet Resistance for Barrier Study

Parameter	Ohmic Contact Resistance $\Omega.mm$	Sheet Resistance $\Omega/\square$
21 nm barrier	1.17	310
15 nm barrier	1.44	281
9 nm barrier	1.22	276

A completed 2-finger GaN HEMT device with a 125 μm gate width, 5 um L_{SD} is depicted in Figure 7.3.

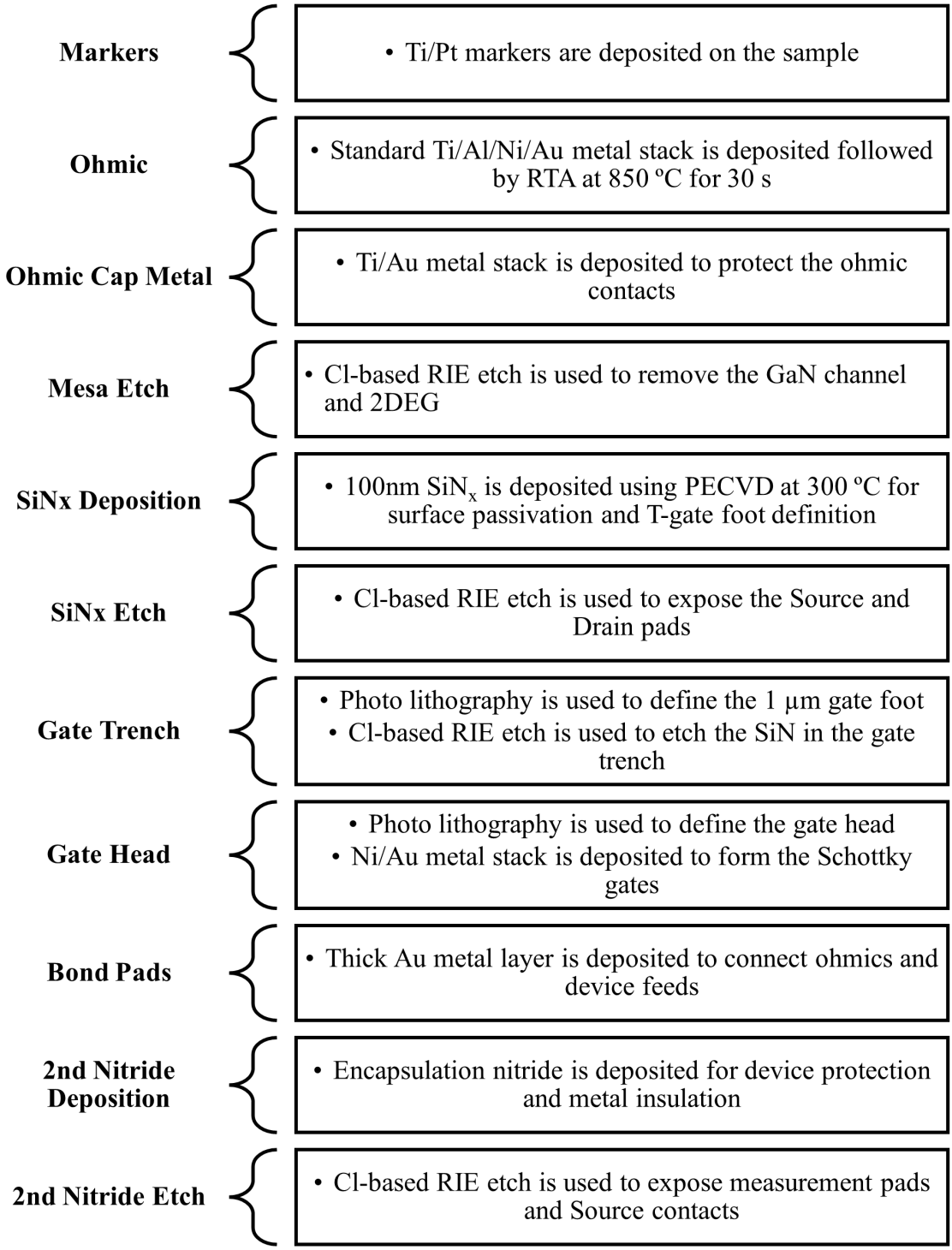
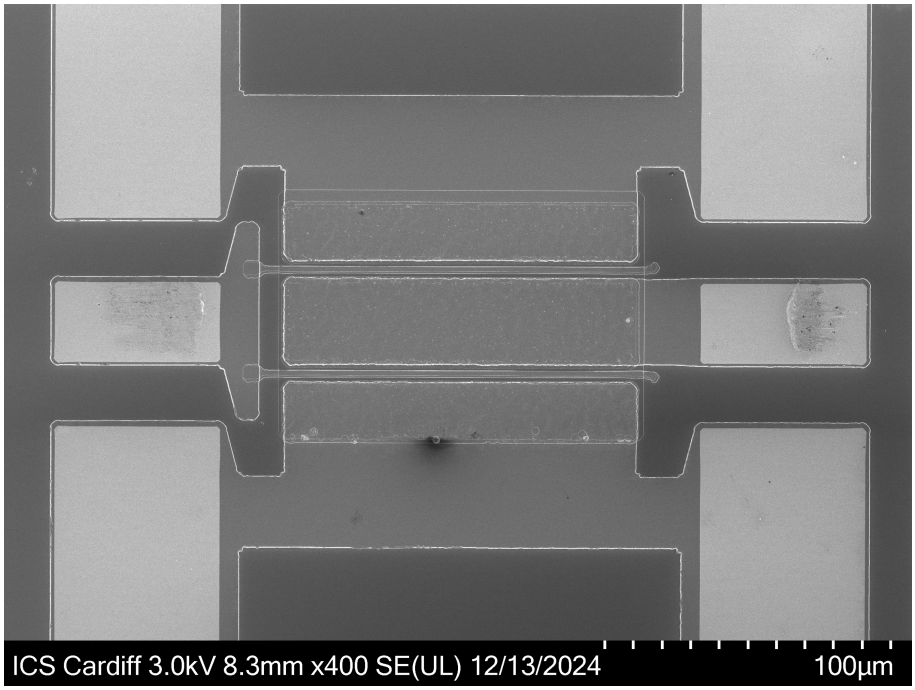
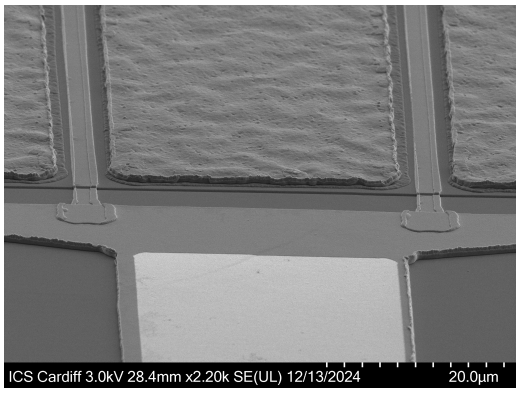


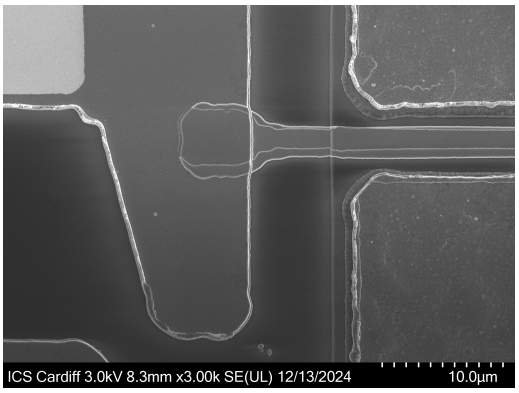
Figure 7.2: Flowchart of the Fabrication Process for the AlGaN Barrier Study



(a)



(b)



(c)

Figure 7.3: Scanning electron microscopy (SEM) images of a fabricated 2-finger device with 125 μm gate width. (a) shows the full device layout; (b) shows the two gates rising over the mesa etch sidewall; (c) shows a zoom in of the gate feed.

7.3 Device Measurements

7.3.1 DC-IV Measurement Results

To characterise the electrical performance of the devices, DC-IV measurements were conducted in a dark, temperature-controlled environment using a 200 mm semi-automatic thermal probe station. The Keysight B2902A (SMU) was used to perform the DC measurements. The SMU unit was connected to GSG RF Probes via Auriga 67 GHz, 50 V, 1 A Bias tees. A 50 Ω load was connected to the RF port to suppress device oscillations during the measurements.

Due to the shifting threshold voltage due to the changing barrier thickness, the DC-IV transfer characteristic measurements ($I_{DS}V_{GS}$) were performed with gate voltage (V_{GS}) swept from $V_t - 1$ to $V_t + 6$ V in steps of 100 mV, with drain voltage (V_{DS}) held at 15 V.

DC-IV output characteristics measurements ($I_{DS}V - DS$) were then performed with gate voltage (V_{GS}) swept from $V_t - 1$ to $V_t + 6$ V steps of 1 V, with drain voltage (V_{DS}) swept from 0 to 15 V in 0.375 V steps.

For these measurements $V_t - 1$ has been approximated as -6, -4, -3 V for the wafers with 21 nm, 15 nm, and 9 nm barriers respectively.

The DC-IV characteristics of a 2-finger, 50 μm device, fabricated on three different Wafers of different AlGaN barrier thickness, are presented in Figure 7.4. The key performance metrics extracted from these characteristics are summarised in Table 7.3.

Upon examination of the output DC-IV results, there is a marked enhancement in current density as the barrier thickness is reduced, increasing from 0.408 A/mm with a 21 nm barrier to 0.940 A/mm with a 9 nm barrier. This is accompanied by a substantial increase in G_m, from 146 to 172, and subsequently to 190 mS/mm as the barrier thickness decreases. In contrast, with regard to G_m, it shows a sharper

rise and fall, which is less desirable compared to the relatively flat profile associated with the 21 nm barrier. However, in relation to R_{on}, there is a considerable improvement in the transition from the 21-nm barrier to thinner ones, with the 15-nm barrier presenting the best value of R_{on} of 3.12 Ω / mm. However, in the context of the DC-IV transfer results, the 9 nm barrier displays a disadvantage, with compromised pinch-off characteristics, manifesting in elevated source-to-drain leakage and subthreshold slope. Although some degradation is also evident with the 15 nm barrier relative to the 21 nm barrier, it exhibits a minor increase to the subthreshold slope, along with a significant increase in leakage current by nearly an order of magnitude. In summary of the DC-IV results, it is evident that the 9 nm barrier presents significant issues in terms of pinch-off performance, and these preliminary DC-IV measurements suggest that a 15 nm barrier provides the most effective balance for optimal device performance.

Table 7.3: DC-IV measurement results for different barrier thickness

Parameter	21 nm barrier	15 nm barrier	9 nm barrier
Threshold Voltage (V)	-5.44	-3.71	-2.59
Leakage Current (A/mm)	1.60×10^{-4}	2.33×10^{-3}	2.18×10^{-2}
Saturation Current (A/mm)	0.408	0.907	0.940
Peak Transconductance (mS/mm)	146	172	190
Subthreshold Slope (mV/decade)	310	471	1260
On-Resistance (Ω/mm)	6.32	3.12	3.61

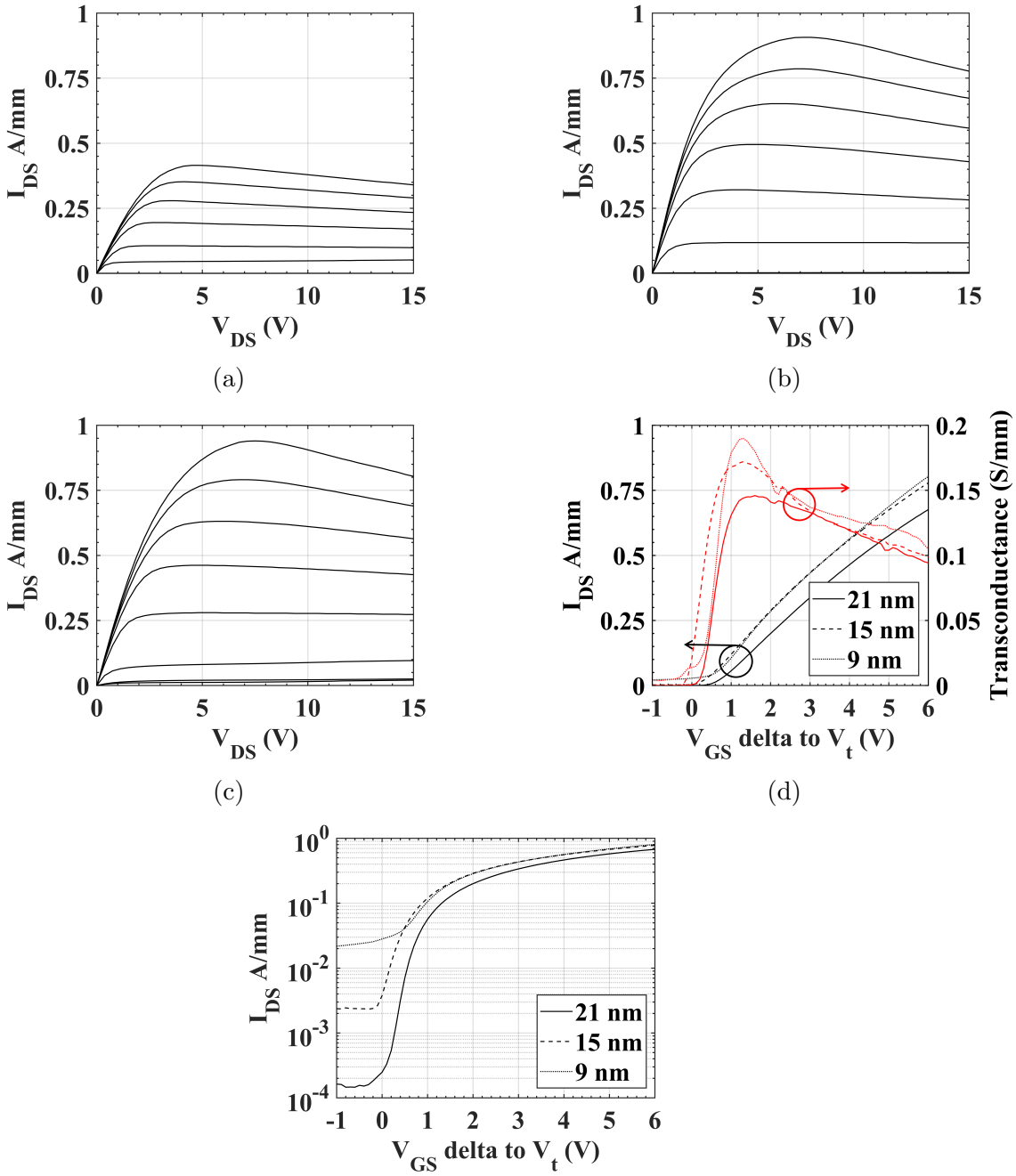


Figure 7.4: DC current-voltage characteristics of 2-finger, 50 μm gate width GaN high-electron-mobility transistors (HEMTs): (a), (b) and (c) Output characteristics $I_{DS}V_{DS}$ for 21 nm barrier, 15 nm barrier, and 9 nm barrier respectively; (d) Transfer characteristics $I_{DS}V_{GS}$ for 21 nm barrier, 15 nm barrier, and 9 nm barrier respectively; (e) Logarithmic scale transfer characteristics for 21 nm barrier, 15 nm barrier, and 9 nm barrier respectively.

7.3.2 Pulsed-IV Measurement

Pulsed-IV measurements were performed to determine the impact of the AlGaN Buffer thickness on current collapse and R_{on} shift. The Pulsed-IV measurements were conducted in a dark, temperature controlled environment using a 200 mm semi-automatic thermal probe station. The Auriga Tri-State PIV from Focus Microwave was used to perform the pulsed measurements. This system was then connected to GSG RF Probes via Auriga 67 GHz, 50 V, 1 A Bias Tees. A 50 Ω load was connected to the RF port to suppress device oscillations during the measurements.

For all Pulsed-IV measurements a 1 μs pulse width was used, with a duty cycle of 0.01 %. This was chosen to minimise any impact of self-heating on the device performance, along with ensuring a short pulse to enable trap stats to be correctly filled or emptied between measurements.

Pulsed-IV transfer characteristic measurements ($I_{DS}V_{GS}$) were performed with measurement points (NQ) for gate voltage (V_{GS}) swept from $V_t - 1$ to $V_t + 6$ V in steps of 100 mV, and drain voltage (V_{DS}) = 15 V.

Pulsed-IV output characteristics measurements ($I_{DS}V_{DS}$) were then performed with measurement points (NQ) for the gate voltage (V_{GS}) swept from $V_t - 1$ to $V_t + 6$ V in 0.5 V steps and the drain voltage (V_{DS}) swept from 0 to 15 V in 0.375 V steps.

For these measurements $V_t - 1$ has been approximated as -6, -4, -3 V for the wafers with 21 nm, 15 nm, and 9 nm barriers respectively..

For both of these measurement sweeps 4 different sets of Q points are used:
(For this section, the pulsed measurements, Q points will be notated as (QV_{GS}, QV_{DS}))

- Continuous DC: This is a standard DC measurement and will allow for a comparison between continuous DC-IV and Pulsed-IV measurements (NQ = Q points).

- Cold Pulsed-IV: This is a Pulsed-IV measurement where the Q points are set to (0,0), which removes any electric field across the device and allows the traps to all empty.

- Gate-lag Pulsed IV: This is a Pulsed-IV measurement in which the Q points are set to ($V_t - 1$,0), which will cause the traps dependent on V_{GS} to be filled and the traps dependent on V_{DS} to empty. This will allow the effects of surface-state traps to be observed as "gate-lag" when compared to the cold-pulsed IV measurement.

- Drain-lag Pulsed IV: This is a Pulsed-IV measurement in which the Q points are set to ($V_t - 1$,15), which will cause the traps dependent on both V_{GS} and V_{DS} to be filled. This will allow the effects of bulk-state traps to be observed as a "drain-lag" when compared to the gate-lag Pulsed-IV measurement.

Pulsed IV measurements showing the collapse of the gate and drain-lag current and the change R_{on} are shown in Figure 7.5 with the key performance metrics summarised in Table 7.4.

Under pulsed IV stress, there are multiple observations that can be identified. The first is that the gate-lag for the 21 and 9 nm barrier is significant with current collapse of 44.8 and 40.9 % respectively compared to the 15 nm barrier which has a current collapse of 28.8 %. This indicates that both the 21 nm, and 9 nm barrier have significantly more surface traps. This is expected for the 9 nm barrier, due to the reduced channel sheet density, which can lead to increased surface state traps. However, for the 21 nm barrier it indicates that there may potentially be more threading dislocations or AlGaN/GaN interface defects due to the thicker barrier. Now when looking at the drain-lag current collapse, it is interesting that 9 nm barrier exhibits significantly less drain-lag than both 21 nm barrier and 15 nm barrier, with 9.79 %, compared to 22.5 and 26 %, respectively. This large difference is likely due to poor carrier confinement due to a shallower quantum well due to the

reduced piezoelectric strain in the 9 nm barrier. This results in a reduction to the bulk trap density. The final observation is that 21 nm barrier shows particularly severe pinch-off degradation under cold pulse conditions Figure 7.6b. This is likely attributed to an increase in trap states at the AlGaN/GaN interface potentially due to additional threading dislocations, indicating a significant trapping effect that prevents the device from pinching off correctly in the short 1 μs duration. This shows a lack of ability to modulate the gate of the device when in pulsed operation.

In summary of these Pulsed-IV results, it once again indicates that the 15 nm barrier provides the best compromise in performance between the 3 barrier thicknesses, due to the significant disadvantages present in the other two wafers.

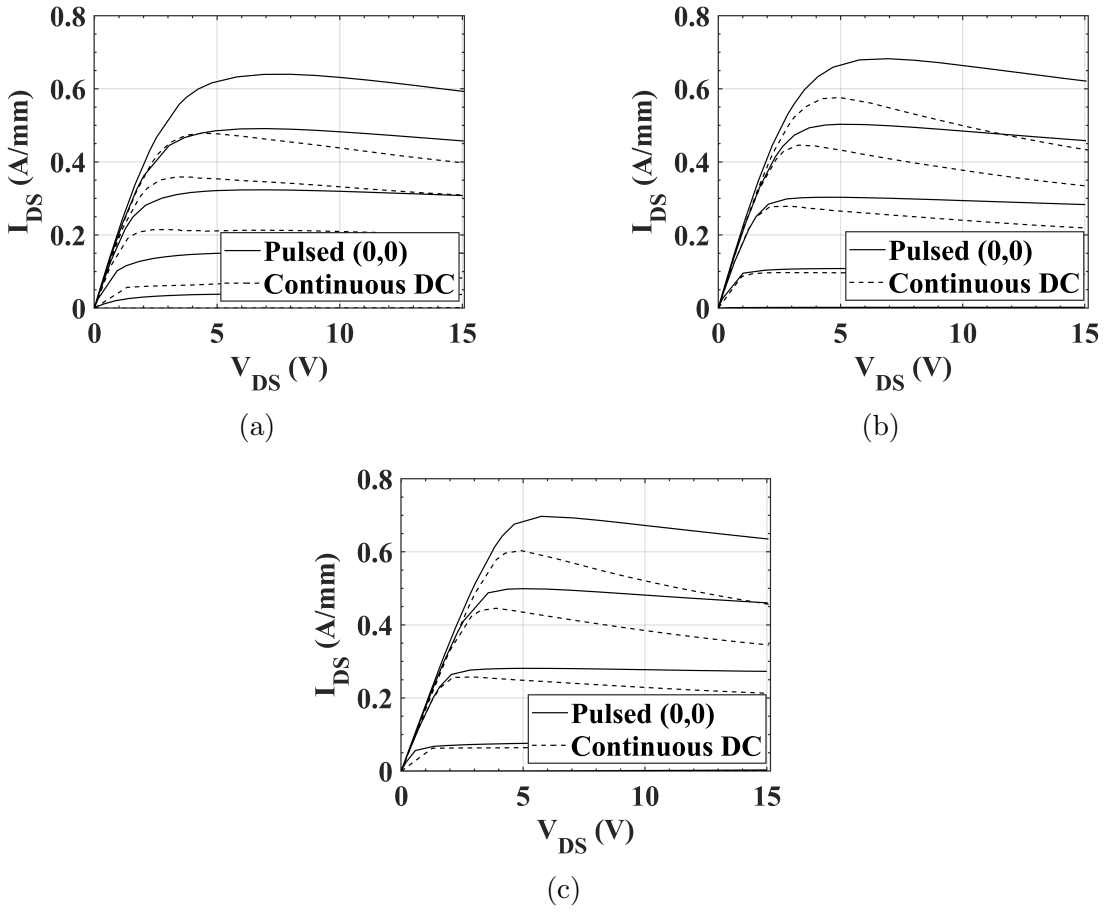


Figure 7.5: Continuous DC and Pulsed-IV characteristics of 2-finger, 300 μm gate width GaN high-electron-mobility transistors (HEMTs): (a) shows the results for 21 nm AlGaN Barrier; (b) shows the results for 15 nm AlGaN Barrier; (c) shows the results for 9 nm AlGaN Barrier.

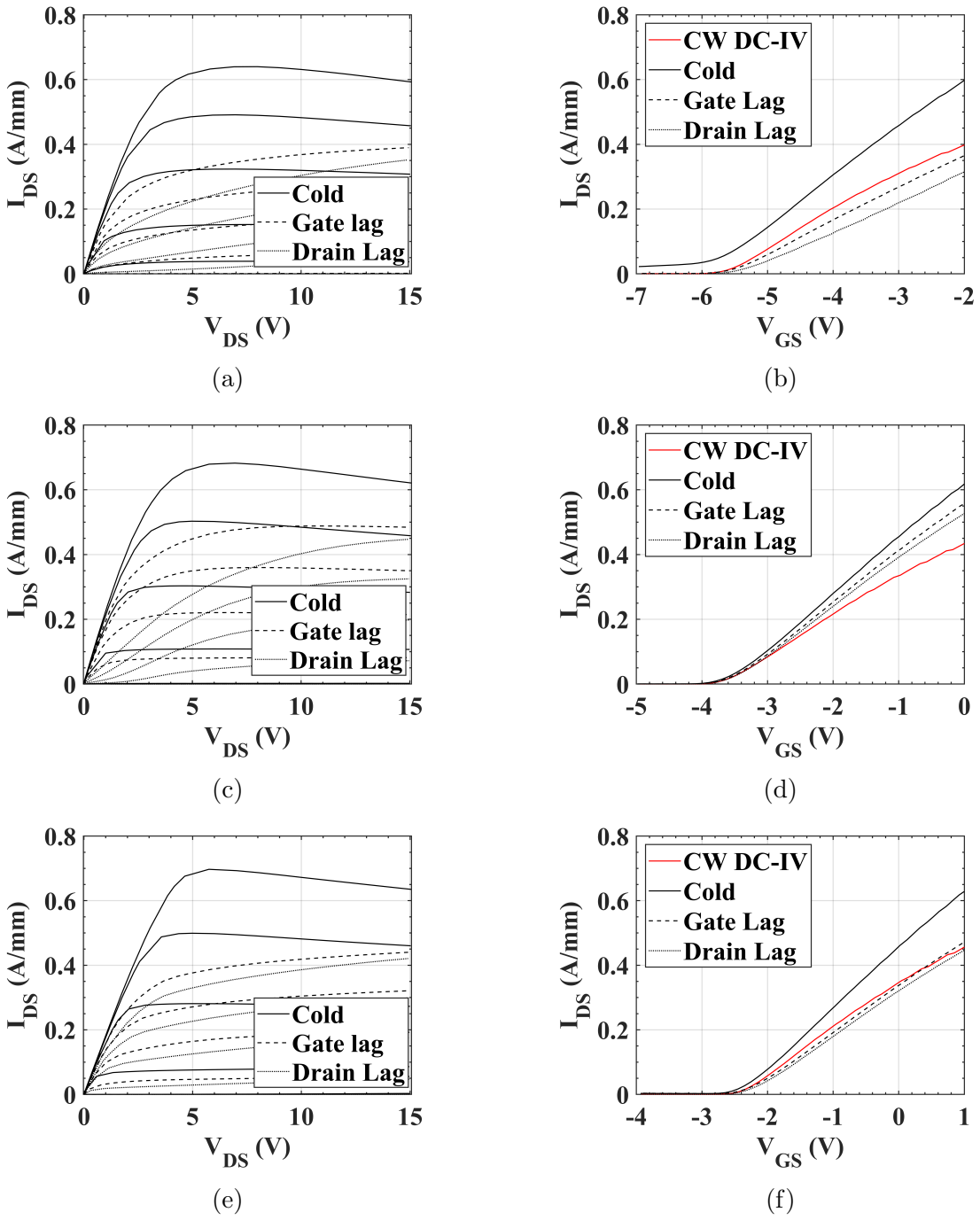


Figure 7.6: Pulsed-IV characteristics of 2-finger, 300 μm gate width GaN high-electron-mobility transistors (HEMTs): (a) and (b) show the Output and Transfer Pulse-IV measurement results respectively for 21 nm AlGaN Barrier; (c) and (d) show the Output and Transfer Pulse-IV measurement results respectively for 15 nm AlGaN Barrier; (e) and (f) show the Output and Transfer Pulse-IV measurement results respectively for 9 nm AlGaN Barrier.

Table 7.4: Continuous DC-IV and Pulsed-IV Measurement Key Parameters. Current Density and Current Collapse has been taken from where $V_{GS} = V_t + 6V$, and $V_{DS} = 10V$

Parameter	21 nm barrier	15 nm barrier	9 nm barrier
CW-DC Current Density (A/mm)	0.437	0.497	0.518
Cold Current Density (A/mm)	0.631	0.663	0.672
Gate-lag Current Collapse	44.8 %	28.8 %	40.9 %
Drain-lag Current Collapse	22.5 %	26.0 %	9.79 %
Continuous DC R_{on} (Ω/mm)	4.96	4.71	5.93
Cold R_{on} (Ω/mm)	4.71	4.54	5.54
Gate-lag R_{on} (Ω/mm)	6.44	5.35	6.64
Drain-lag R_{on} (Ω/mm)	11.0	16.2	7.53

7.3.3 Thermal Dependent Drain Current Transient Spectroscopy Measurements

Drain Current Transient Spectroscopy (DCTS) measurements have been performed at three different temperatures (25, 85, and 125 °C) to compare traps energy levels between the AlGaN barrier thickness variations. These measurements were performed in a dark, temperature controlled environment using a 200 mm semi-automatic thermal probe station. The Auriga Tri-State PIV from Focus Microwave was used to perform the pulsed measurements, using the long-pulse measurement capability. This system was then connected to GSG RF Probes via Auriga 67 GHz, 50 V, 1 A Bias Tees. A 50 Ω load was connected to the RF port to suppress device oscillations during the measurements. The long pulse was set with a span of 1 s, and the sample rate was initially set to 1 MHz and downsampled by 1 order of magnitude every decade after the pulse. After each measurement, the bias of the device was set at V_{GS} = 0 V and V_{DS} = 0 V, to ensure that the device was in a known state before and after each measurement.

The three key stages of the long pulse measurement are:

- Trap Filling Period: 500 μs filling period.
- Pulse Period: 500 μs pulse.
- Recovery Period: post-pulse to 1 s.

Two pulsing methods were performed: a single drain pulse, where QV_{DS} is pulsed from a low steady-state value to a high value and QV_{GS} is kept constant above the threshold voltage; and a dual pulse where QV_{DS} is pulsed from a low steady-state value to a high value, and QV_{GS} is simultaneously pulsed from the steady-state value to below the threshold voltage to pinch off the device. The steady-state values are defined as Q points and the pulse values are defined as NQ points. In this study, the Q points were taken as QV_{DS} = 2 V, QV_{GS} = -5.25, -3.4, and -2.1 V for 21 nm barrier, 15 nm barrier, and 9 nm barrier, respectively. These Q points are constant

between both pulse methods. For the single drain pulse, the NQ points are: NQV_{GS} = QV_{GS}, NQV_{DS} = 15 V, QV_{DS} = 2 V. For the dual pulse the NQ points are: NQV_{GS} = -4 V, and NQV_{DS} = 15 V, QV_{DS} = 2 V. The values of NQV_{GS} were chosen to set the current in each device to approximately 50 mA/mm when V_{DS} = 2 V, this relates to $V_{GS} = V_t + 0.19$ V for 21 nm barrier, $V_{GS} = V_t + 0.31$ V for 15 nm barrier, and $V_{GS} = V_t + 0.49$ V and for 9 nm barrier. This discrepancy between the threshold voltage and the chosen value is due to the worse subthreshold slope as the barrier thickness is reduced.

Both pulse methods were performed to determine the location of the traps and the effect of the AlGaN barrier thickness on the trap time constants and the maximum drop in drain current after pulsing. Performing these measurements at several temperatures allows us to compare the change in trap time constants and extract trap energy levels.

The single drain pulse is a key indicator of drain-lag, and the dual pulse is a key indicator of both gate and drain-lag. Looking at the results presented in Figure 7.7a, there is a noticeable difference between the 21 nm barrier and the other two wafers during the pulse stage. The 21 nm barrier exhibits a higher maximum current than the other two wafers after V_{DS} is pulsed high. This increase is likely due to the shifting threshold voltage during the pulse, as seen before in Figure 7.6b. This hypothesis is further supported by the dual pulse measurement Figure 7.7b, where the device does not pinch off correctly as V_{GS} is pulsed to $V - t$ - 1 V (-7 V), which would be expected if the device pinch-off characteristics have shifted during the measurement, as observed in the cold FET short-pulse measurements.

Now looking at the recovery after the pulse in Figure 7.7, we can see that for the drain-lag measurement, there is a minimal difference in recovery time between the three barrier thicknesses, indicating that changing the barrier thickness does not lead to the creation of new trap locations. However, as the barrier thickness decreases, the quantity of these deep-level traps decreases, revealing that the quantity of traps is significantly affected by the barrier thickness. This result confirms the

findings in the pulsed-IV measurements that increasing the barrier thickness likely leads to an increased amount of threading dislocations and interface issues between the AlGaN/GaN that can cause these additional trap states to form. This trend continues with the dual pulse, where the recovery time remains constant between all three barrier thicknesses, and there is still a significant increase in the number of traps as the AlGaN barrier thickness increases.

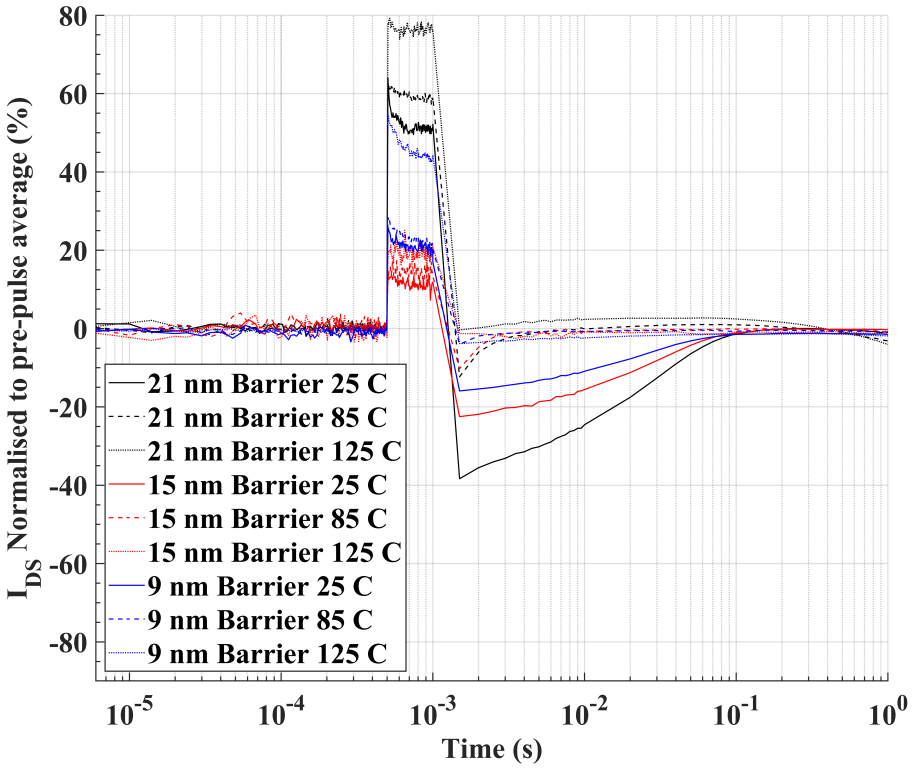
It is also extremely important to note that the recovery time constant decreased significantly as the temperature increased. For the single drain-lag pulse, the recovery percentages are listed in Table 7.5.

Table 7.5: Single pulse drain-lag recovery after 500 μs

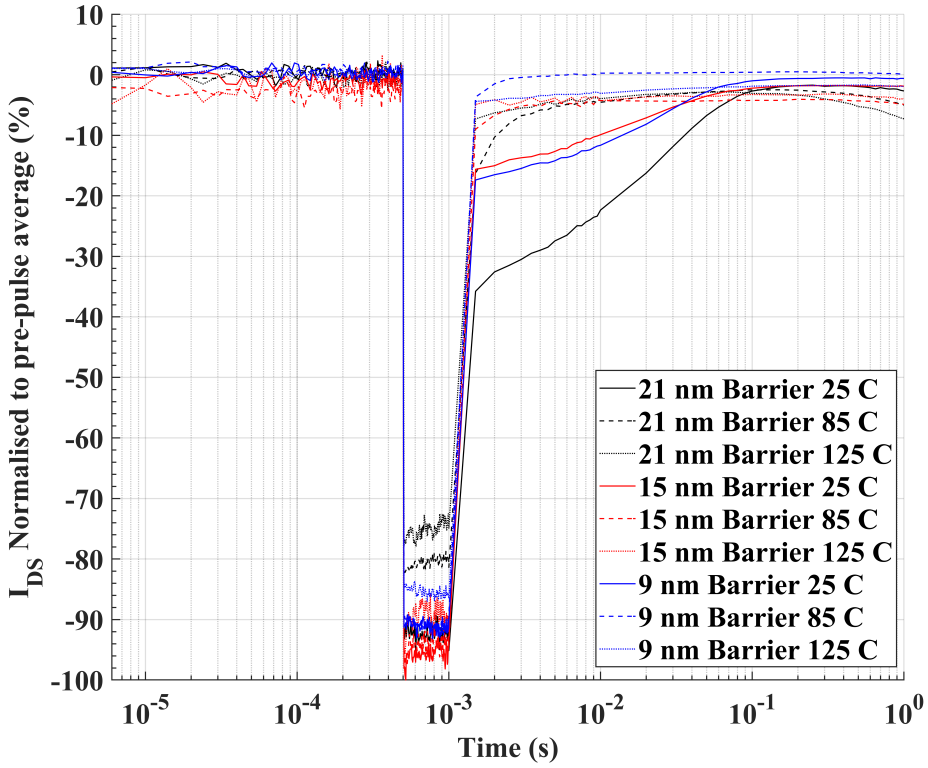
Parameter	21 nm barrier	15 nm barrier	9 nm barrier
25 °C	38.3 %	22.5 %	15.9 %
85 °C	12.3 %	10.2 %	4.01 %
125 °C	0.351 %	1.28 %	3.82 %

The same trend is also shown for the dual pulse measurement. Due to the complete recovery by 125 °C, and significant recovery at 85 °C, it can be concluded that while there are a significant amount of traps in these wafers, they are very shallow traps and can be easily emptied at high temperature.

Due to measurement equipment limitations presenting issues with the noise floor, it is not possible to extract trapping energy states with certainty since Bayesian deconvolution is unable to reliably extract the transients. Any attempted filtering steps applied before lead to obscuring the transients in such a way that they Bayesian deconvolution stage will present a perfectly smooth signal. This will be addressed in future work with modifications to the measurement procedure, such as implementing multiple measurements and averaging to reduce noise, and further improvements to the system to allow for a lower noise floor to complete the analysis to determine the energy level of all traps.



(a)



(b)

Figure 7.7: Drain Current Transient Spectroscopy (DCTS) measurement results for a 2-finger, 300 μm gate width GaN high-electron-mobility transistors (HEMTs) with two different pulse conditions: (a) VGS held constant VDS pulsed from 2V to 15 V; (b) VGS pulsed to below V_t and V_{DS} pulsed 2 V to 15 V.

7.3.4 Small Signal RF Measurements

Small-signal RF measurements were performed to determine the influence of the AlGaN barrier thickness on intrinsic and extrinsic device parasitics, as well as the effect of this AlGaN Barrier thickness on essential RF performance metrics f_t and f_{MAX}. On-Wafer measurements were performed using 150 μm GSG RF probes. The measurements were carried out on a 200 mm semi-automatic probe station, using a Keysight PNA model N5227B. This was interfaced with the Keysight N5293AX03 range extenders, which extend the range to 0.1 to 120 GHz and incorporate built-in bias tees. In addition, a Keysight B1500a semiconductor device parameter analyser was used for DC biasing and measurements. Both PNA and B1500a were controlled by Keysight IC-CAP software. Probe tip calibration was performed through eL-RRM using the MPI AC2 calibration substrate.

RF measurements were performed from 0.1 to 20 GHz at multiple different bias points to allow for small-signal model extraction:

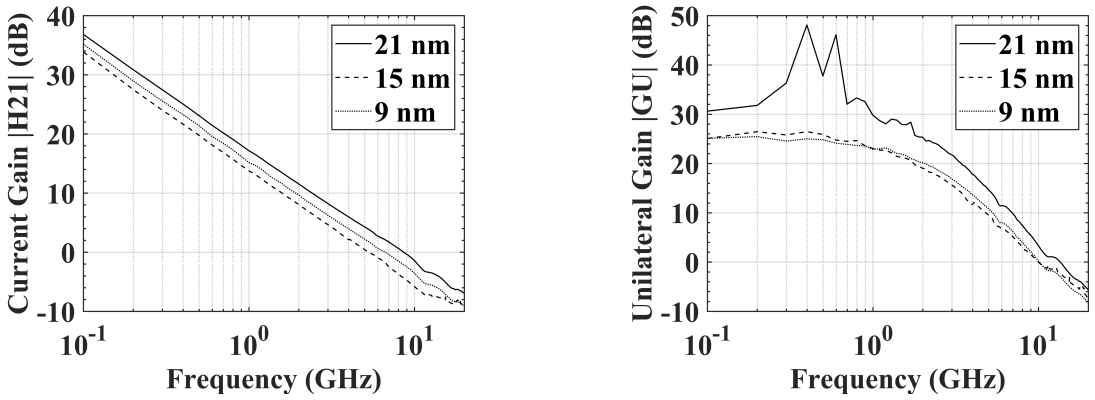
- Pinch Off FET: $V_{GS} << V_t$ Here the gate voltage is set to below the threshold voltage and V_{DS} is set to 0 V, to ensure a cold FET configuration.
- Hot FET: Here, V_{GS} is set for the maximum G_m and V_{DS} is set to 15 V.
- Forward bias: Here we ensure V_{DS} is set to 0 V, and then bias the gate to forward conduction to a specific gate current. For this type of measurement, three measurements are performed with gate current (I_{GS}) set to 200 μA/mm, 400 μA/mm, and 600 μa/mm for each measurement.

The small signal f_t and f_{MAX} for a 2-finger, 5 μm L_{DS}, 125 μm gate width device, fabricated on both wafers, is presented in Figure 7.8 with the extracted values shown in Table 7.6.

The results of the small signal measurements for f_t and f_{MAX} are presented in 7.8. There is a notable difference between the three barrier thicknesses, with the

Table 7.6: Small signal RF f_t and f_{MAX} for 21, 15, and 9 nm AlGaN barrier thicknesses

Parameter	21 nm barrier	15 nm barrier	9 nm barrier
f_t	8.56 GHz	5.27 GHz	6.57 GHz
f_{MAX}	13.5 GHz	9.95 GHZ	10.1 GHz



(a) (b)

Figure 7.8: RF S-Parameter measurement results showing (a) f_t and (b) f_{MAX} for various AlGaN barrier thicknesses

21 nm barrier having the highest f_t and f_{MAX}. This is because while reducing the barrier thickness increases G_m, it also increases the intrinsic capacitances of the device resulting in a reduction in overall f_t and f_{MAX}. The benefits of reduced barrier thickness will only be observed when the gate length has been reduced, which allows improved f_t and f_{MAX} as thinner barrier layers would allow lower gate lengths for a fixed aspect ratio of gate length to gate channel distance.

Table 7.7: Comparison of extracted values for Extrinsic and Intrinsic parameters for AlGaN Barrier Thickness Variations. The extrinsic Parameters have been held constant between wafers.

Extrinsic Parameters			
Parameter	21 nm barrier	15 nm barrier	9 nm barrier
C_{pg} (fF)	113	113	113
C_{pd} (fF)	53.4	53.4	53.4
L_s (pH)	26.3	26.3	26.3
L_g (pH)	131	131	131
L_d (pH)	0.134	0.134	0.134
R_d (Ω)	50.5	50.5	50.5
R_s (Ω)	1.08	1.08	1.08
R_g (Ω)	0.906	0.906	0.906
Intrinsic Parameters			
Parameter	21 nm barrier	15 nm barrier	9 nm barrier
C_{gd} (fF)	61.3	90.4	73.3
C_{gs} (fF)	400	799	638
C_{ds} (fF)	121	83.4	138
τ (ps)	1.21	0.00346	0.00121
G_m (mS/mm)	397	428	449
R_{in} (Ω)	4.89	5.65	7.86
R_{ds} (Ω)	298	434	367

7.4 Conclusion

The results of the DC-IV measurement reveal that reducing the barrier thickness enhances the current density, with values increasing from 0.408 A/mm at 21 nm to 0.940 A/mm at 9 nm. As the barrier thickness decreases, there is an improvement in associated parameters such as G_m, which increases from 146 to 190 mS/mm. The transition from a 21 nm to a 15 nm barrier shows optimal results for R_{on}, with the best value observed at the 15 nm barrier (R_{on} of 3.12 Ω/mm), despite some degradation in the leakage current from the source and pinch characteristics. However, the 9 nm barrier is problematic, as it compromises pinch-off characteristics such as subthreshold slope and increases source-to-drain leakage. Although the 15 nm barrier also shows increased leakage compared to 21 nm, it maintains balanced subthreshold performance and offers more than twice the current density of the 21 nm barrier. Overall, these findings suggest that a 15 nm barrier offers a favourable compromise for device performance, whereas the 9 nm barrier introduces significant issues.

Pulsed-IV measurements have been performed to investigate the effect of barrier thickness on trap formation and recovery time in AlGaN/GaN structures. For the pulsed-IV measurements it is noted that the 21 and 9 nm barriers exhibit a more significant current collapse due to increased surface traps, likely from dislocations or interface defects for the 21 nm barrier, and reduced channel sheet density, which can lead to increased surface state traps in the 9 nm barrier. Interestingly, the 9 nm barrier shows significantly less drain-lag compared to the others, possibly due to poor carrier confinement and increased leakage reducing the bulk trap density. Additionally, the 21 nm barrier demonstrates severe pinch-off degradation under cold pulse conditions, attributed to increased interface trap states, affecting the device's ability to modulate the gate effectively during pulsed operation.

Looking at the DCT spectroscopy measurements, recovery time after a pulse has been found to be relatively unaffected by barrier thickness, suggesting that there are no new trap locations introduced with varying barrier thickness. However,

there is a significant decrease in the number of traps with thinner barriers, which confirms that thicker barriers may lead to more threading dislocations and interface problems, increasing trap formation. A noted pattern is a significant reduction in recovery time as the temperature increases, indicating the presence of mostly shallow traps. At higher temperatures, recovery is nearly instant, indicating that these traps are shallow.

The RF small-signal measurements presented reveal differences in performance depending on the barrier thickness. The 21 nm barrier yields the highest performance measures as a result of having lower intrinsic capacitances than the thinner barriers. Increasing intrinsic capacitance results in a decrease in overall RF performance. The benefits of reduced barrier thickness are apparent only when the gate length is minimised, allowing for improved performance metrics by allowing shorter gate lengths while maintaining a fixed L_g:gate-to-channel distance ratio.

Overall, from this work, it is apparent that the best compromise in barrier thickness is 15 nm, due to the improved DC-IV and trapping performance, the only significant disadvantage being the increased source-drain leakage when compared to the 21 nm barrier. For RF performance, the reduction in the barrier thickness from 21 to 15 nm will allow a 30 % reduction in L_g, which is expected to lead to a significant improvement in RF performance.

Chapter 8

Impact of AlGaN Back-Barrier on GaN-on-Si RF HEMT Performance and Trapping Effects

8.1 Introduction to AlGaN Back Barrier

One of the main drawbacks with AlGaN HEMTs is their efficiency at high frequencies and drain voltages because of the presence of trapping effects, reduced electron confinement, and self-heating in devices. AlGaN HEMTs are currently the most mature GaN HEMTs structure, and there is a strong drive to reduce the barrier thickness, as shown in the above section. In order to overcome several limits with the reduction of the thickness of the AlGaN barrier, changes in the epi-structure are required, with the use of an AlGaN back barrier (BB) among the most promising [127]. The presence of an AlGaN back barrier suppresses short-channel effects, reducing the strict requirement for scaling of the AlGaN barrier thickness for shorter gate lengths [128]. It also provides the additional benefit of increasing the breakdown voltage by ensuring a uniform distribution and reducing the electric field at the edge of the gate [129]. One of the most important uses of the AlGaN back barrier is the suppression of traps in the buffer caused by Fe or C doping. This is

because the increased strain will increase the energy band, preventing hot electrons from being able to reach the deep trap stats in the buffer, preventing the R_{on} shift and current collapse attributed to drain-lag. This has been shown in the following papers that show the significant success that the use of the AlGaN back barrier has had in the suppression of buffer traps [130] [52] [131] [132]. Furthermore, this also has the benefit of increasing the linearity of the device [133].

Figure 8.1 taken from [134] shows the effect of the AlGaN back barrier on suppression buffer traps through because of a sharper electron barrier. This enhanced energy barrier implies that hot electrons are less likely to reach the buffer layer and subsequently be trapped there.

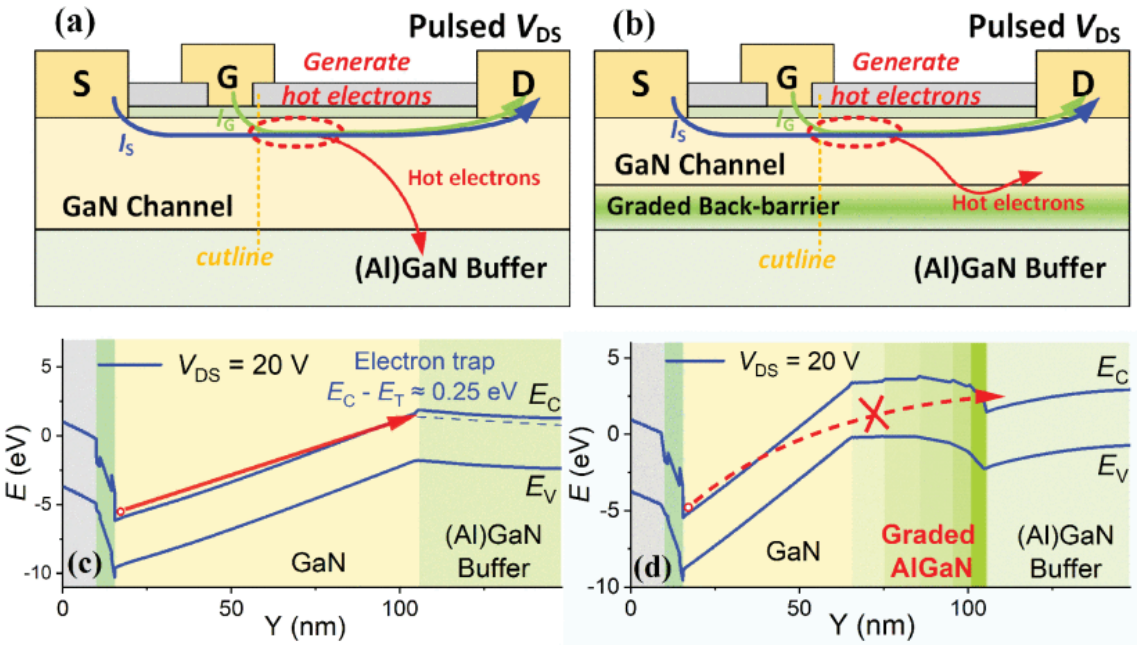


Figure 8.1: "Schematic diagram of hot electrons drifting and trapping by the lectron traps in (Al)GaN buffer (a) without and (b) with graded AlGaN; energy band diagram along the cutline obtained by TCAD simulation of the AlGaN/GaN HEMTs (c) without and (d) with graded AlGaN." Figure taken from [134]

In [127] an investigation on the effect of different Al concentrations in the AlGaN back barrier was performed on GaN-on-SiC, concluding that there were significant issues with Al = 4 % such as increased device leakage and a large Drain-Induced

Barrier Lowering (DIBL) . After increasing the Al concentration to 10 %, there was a four-fold improvement in DIBL and as the concentration increased to a maximum of Al = 25 %, it was found that there were significant improvements in, the leakage current and the DIBL at DC, along with low current collapse under pulsed-IV conditions and a PAE of 70 % at 40 GHz. This indicates that as Al concentration increases, the electron confinement is significantly improving leading to higher-performance devices.

Multiple alternative back barrier structures such as InGaN and AlN have been proposed. In [135] three different back barrier structures were compared; AlGaN, InGaN, and AlN where the AlGaN back barrier was found to provide superior DC and RF performance.

In [136] a graded AlGaN back barrier was grown to completely remove the need for C or Fe doping to prevent the formation of deep acceptor traps. This resulted in successful devices with high performance and good channel control even without the typical barrier structure.

Despite all the advantages of an AlGaN back barrier, there are also several known problems. These consist of lowering the electron density and a reduction in thermal conductivity causing increased heat build-up in the channel [137]. The increased self-heating as a result of the inferior thermal conductivity compared to the binary alloys of GaN or Aluminium Nitride (AlN) [53]. .

In this section, an investigation was conducted that compares the effect of a low-Al concentration AlGaN back barrier on the performance of devices and its effectiveness at suppressing traps in the buffer.

8.2 Device Fabrication

RF HEMTs were fabricated on two GaN-on-Si wafers provided by NTT Advanced Technology, one with no AlGaN back barrier and one with a 5 % $Al_{0.05}Ga_{0.95}N$ back barrier. Both epitaxial structures were grown on 150 mm Hi-Res Silicon. The

complete epitaxial structure and the layout of the device are shown in Figure 8.2.

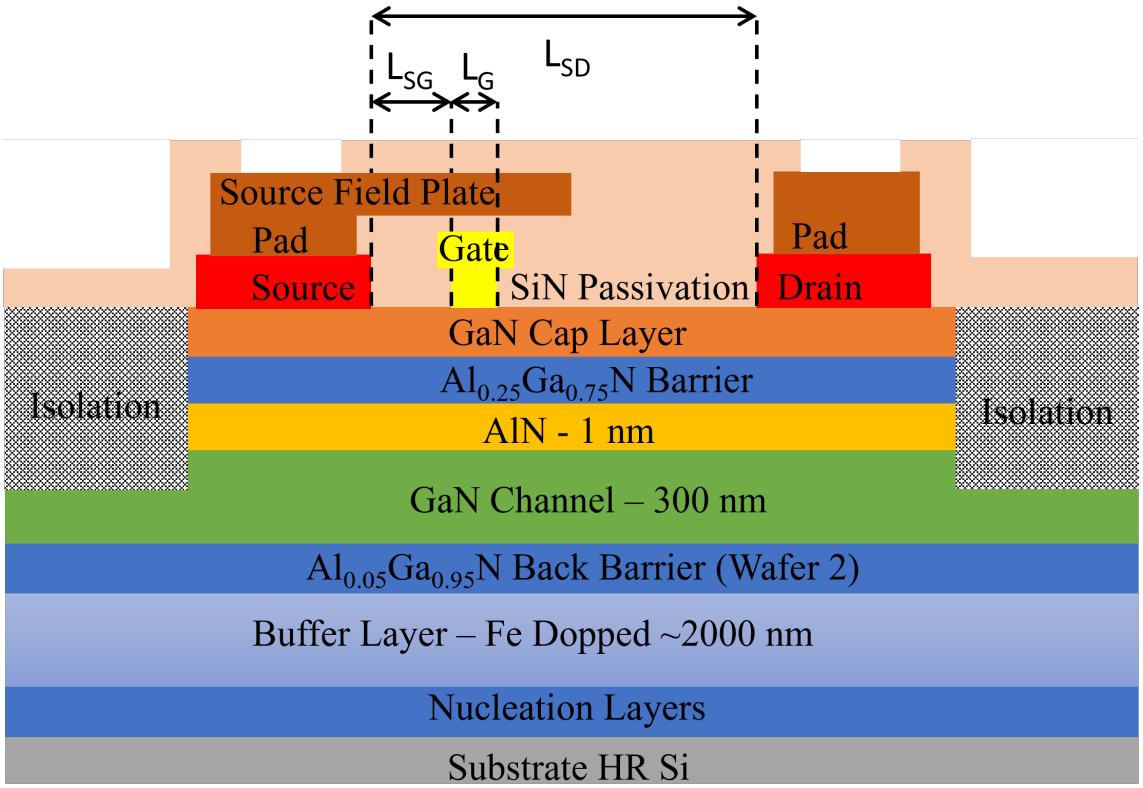


Figure 8.2: Device Structure and Epi-Layers used for this AlGaN back barrier study.

The devices were fabricated with fixed 1.7 μm T-Gates, a Source-Gate spacing (L_{SG}) of 1 μm, and Source Field Plates (SFP) The devices have the following topology variations:

- Source Drain Spacing (L_{SD}) of 5, 10, 15, 20, and 25 μm.
- Drain Width (L_{WD}) of 32 and 52 μm.
- Gate Widths of ((L_{GW}) 125, 150, 200, 250, and 300 μm.

The complete fabrication process is summarised in the flow chart in Figure 8.3. For this study, a 25x25 mm token of each wafer was used for fabrication. These samples were fabricated together and put through each fabrication step simultaneously to ensure that the fabrication variation between each sample is minimised. The ohmic contact and sheet resistance of the resulting fabricated devices is shown in Table 8.1.

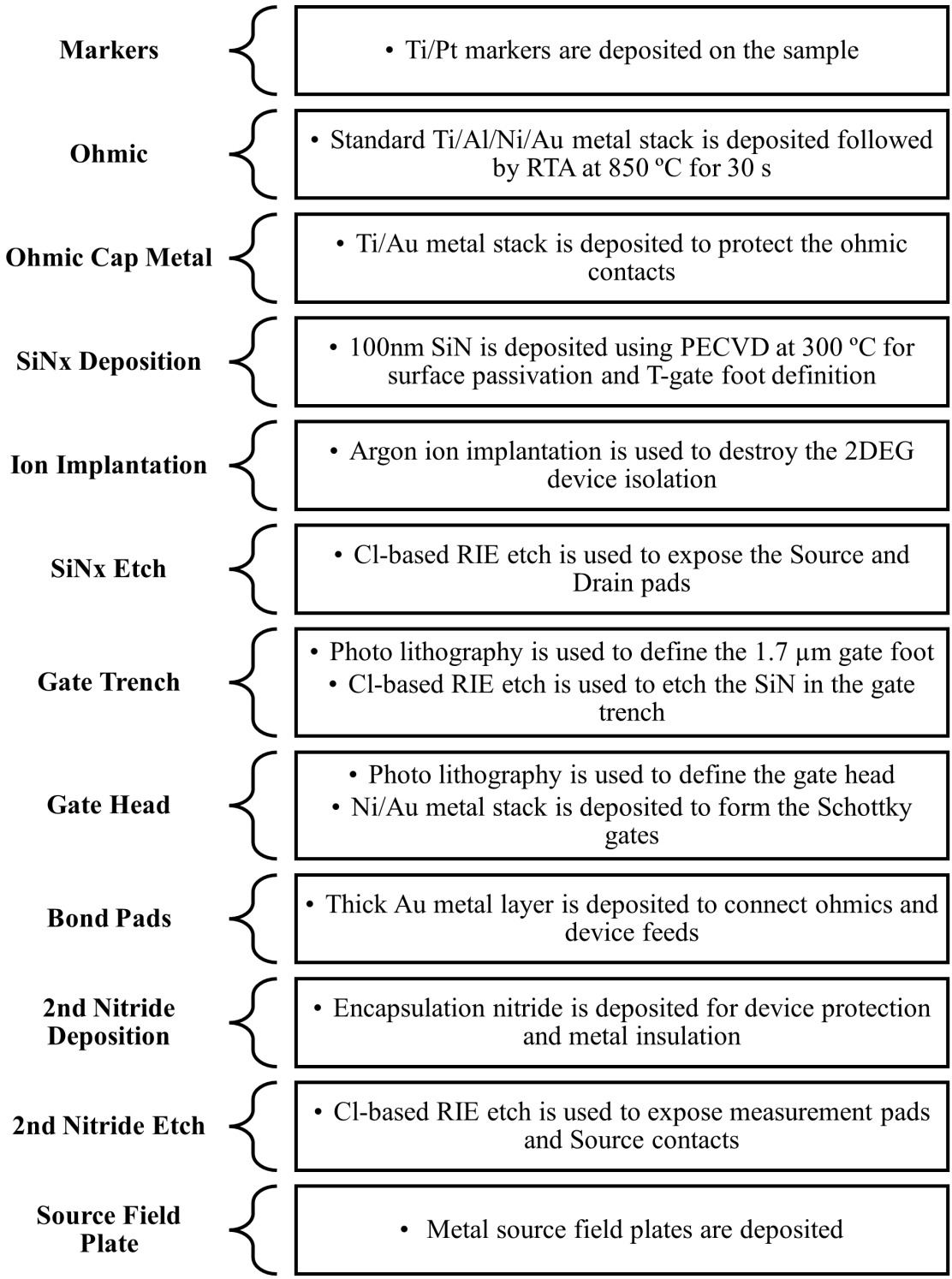
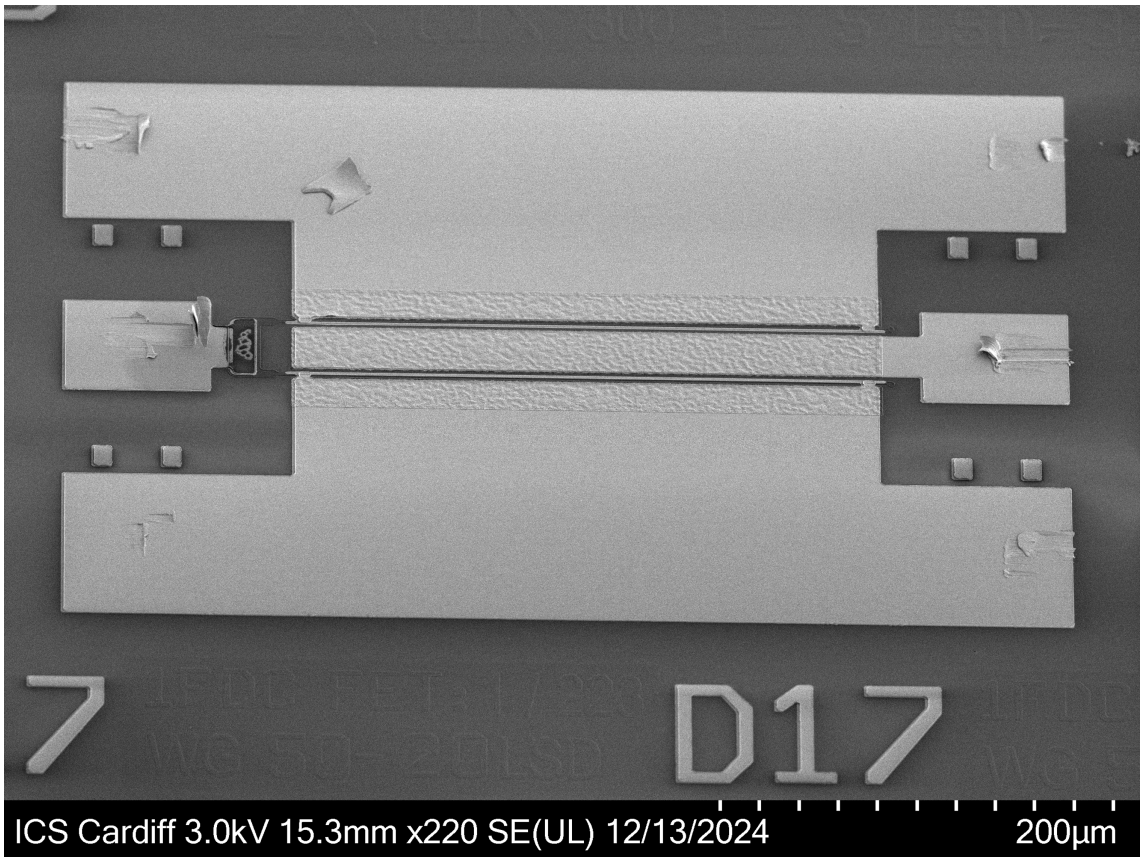


Figure 8.3: Flowchart of the fabrication process for the AlGaN back barrier study

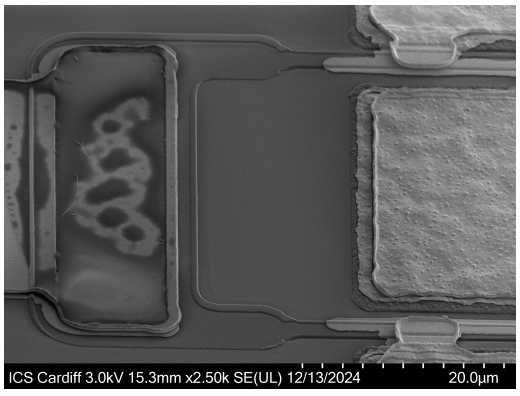
Table 8.1: Ohmic contact and sheet resistance for AlGaN back barrier study

Parameter	Ohmic Contact Resistance $\Omega.mm$	Sheet Resistance $\Omega/\square$
No BB	0.579	320
$Al_{0.05}Ga_{0.95}N$ BB	0.649	313

A completed 2-finger GaN HEMT device with a 125 μm gate width is depicted in Figure 8.4.



(a)



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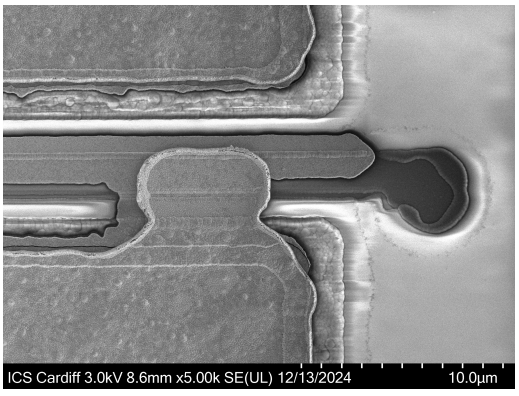


(c)

Figure 8.4: Scanning electron microscopy (SEM) images of a fabricated 2-finger device with 300 μm gate width. (a) shows the full device layout; (b) shows a close up with the two gates; (c) a close up of the source field plate, and how it attaches to the source.

8.3 Device Measurements

8.3.1 DC-IV Measurement Results

To characterise the electrical performance of the devices, DC-IV measurements were conducted in a dark, temperature-controlled environment using a 200 mm semi-automatic thermal probe station. The Keysight B2902A (SMU) was used to perform the DC measurements. The SMU unit was connected to GSG RF Probes via Auriga 67 GHz, 50 V, 1 A Bias tees. A 50 Ω load was connected to the RF port to suppress device oscillations during the measurements.

DC-IV transfer characteristic measurements ($I_{DS}V_{GS}$) were performed with gate voltage (V_{GS}) swept from -4 to 1 V in 100 mV steps, with drain voltage (V_{DS}) held at 15 V.

DC-IV output characteristics measurements ($I_{DS}V_{DS}$) were then performed with gate voltage (V_{GS}) swept from -4 to 1 V steps of 1 V, with drain voltage (V_{DS}) swept from 0 to 15 V in 0.375 V steps.

The DC-IV characteristics of a 2-finger, 5 μm L_{DS}, 300 μm gate width device, fabricated on both wafers, are presented in Figure 8.5. The key performance metrics extracted from these characteristics are summarised in Table 8.2.

Table 8.2: DC-IV measurement results for without and with AlGaN back barrier

Parameter	No BB	$Al_{0.05}Ga_{0.95}N$ BB
Threshold Voltage (V)	2.03	2.23
Leakage Current (A/mm)	5.42×10^{-7}	4.78×10^{-9}
Saturation Current (A/mm)	0.399	0.542
Peak Transconductance (mS/mm)	150	144
Subthreshold Slope (mV/decade)	104	126
On-Resistance (Ω/mm)	5.70	4.17

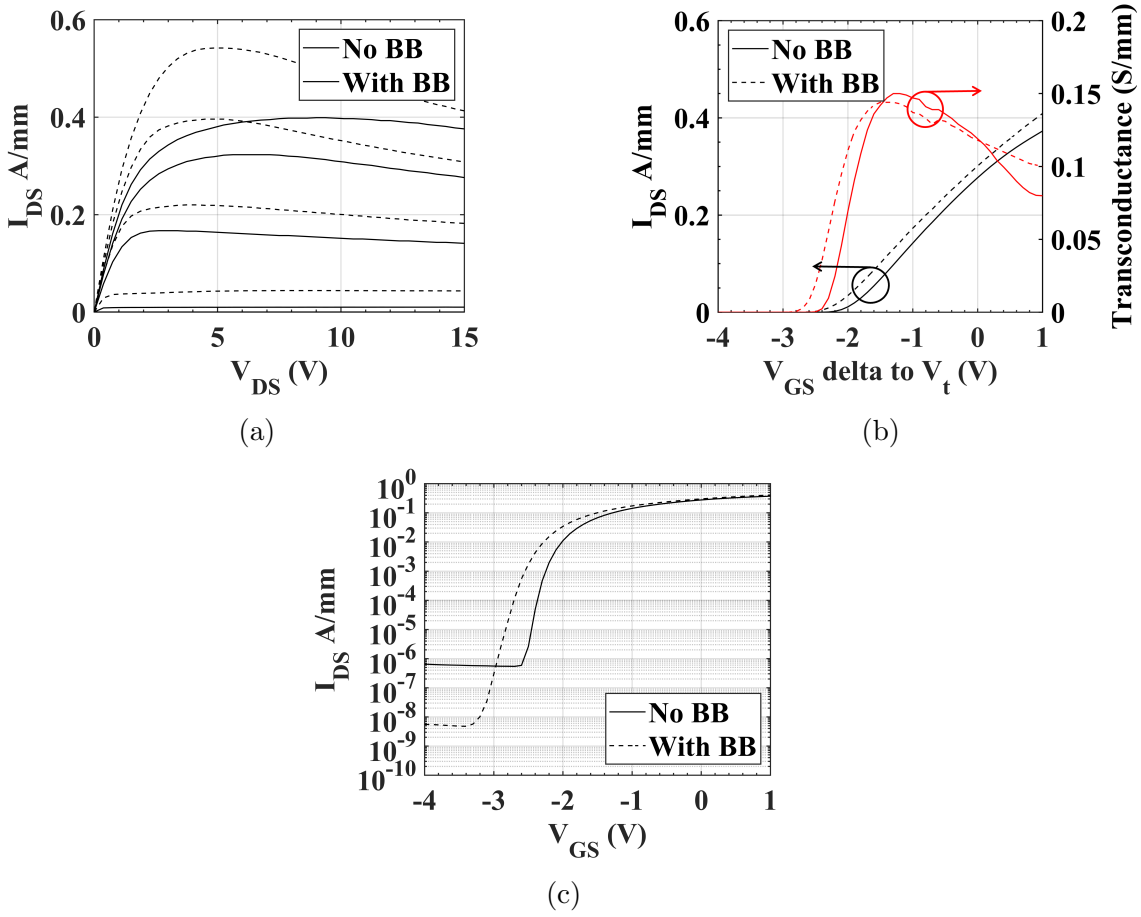


Figure 8.5: DC current-voltage characteristics of 2-finger, 300 μm gate width GaN high-electron-mobility transistors (HEMTs): (a) Output characteristics $I_{DS}V_{DS}$ for wafer with no back barrier and the wafer with $Al_{0.05}Ga_{0.95}N$ back barrier respectively; (d) Transfer characteristics $I_{DS}V_{GS}$ for the wafer with no back barrier and the wafer with $Al_{0.05}Ga_{0.95}N$ back barrier respectively; (e) Logarithmic scale transfer characteristics for the wafer with no back barrier and the wafer with $Al_{0.05}Ga_{0.95}N$ back barrier respectively.

There are two key areas where the presence of the AlGaN back barrier shows significant improvement:

- Reduced Source Drain leakage: A nearly two-order-of-magnitude reduction in I_{DS} was observed, significantly improving the device's off-state characteristics.
- Improved Current Density: There is a significant increase of 35.8 % in the I_{DS} density shown in the output measurements.

The other DC-IV parameters, revealed by the transfer measurements, show a slight deterioration in DC performance. This deterioration is very minor compared to the benefits of increasing the current density and improving the leakage of I_{DS}. However, the most significant issue caused by the addition of the $Al_{0.05}Ga_{0.95}N$ back barrier is the significant increase in self-heating effects in the device. For the wafer with no back barrier at $V_{GS} = 1$ V, there is a drop of 5.71 % from the peak value to $V_{DS} = 15$ V and for the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier under the same conditions the drop is 23.8 %. This is a serious issue that will limit the power density performance of these devices. This self-heating effect will be further investigated in the pulsed-IV section below.

8.3.2 Pulsed-IV Measurement

Pulsed-IV measurements were performed to determine the impact of the $Al_{0.05}Ga_{0.95}N$ back barrier on current collapse and R_{0n} shift. The Pulsed-IV measurements were conducted in a dark, temperature controlled environment using a 200 mm semi-automatic thermal probe station. The Auriga Tri-State PIV from Focus Microwave was used to perform the pulsed measurements. This system was then connected to GSG RF Probes via Auriga 67 GHz, 50 V, 1 A Bias Tees. A 50 Ω load was connected to the RF port to suppress device oscillations during the measurements.

For all Pulsed-IV measurements, a 1 μs pulse width was used, with a duty cycle of 0.01 %. This was chosen to minimise any impact of self-heating on the device performance, along with ensuring a short pulse to enable trap stats to be correctly filled or emptied between measurements.

Pulsed-IV transfer characteristic measurements ($I_{DS}V_{GS}$) were performed with measurement points (NQ) for gate voltage (V_{GS}) swept from -4 to 1 V in steps of 100 mV, and drain voltage (V_{DS}) held at 15 V.

Pulsed-IV output characteristics measurements ($I_{DS}V_{DS}$) were then performed with measurement points (NQ) for the gate voltage (V_{GS}) swept from -4 to 1 V in 0.5 V steps and the drain voltage (V_{DS}) swept from 0 to 15 V in 0.375 V steps.

For both of these measurement sweeps, 4 different sets of (Q) points are used: (For this section, for pulsed measurements, the Q points will be notated as (QV_{GS}, QV_{DS}))

- Continuous DC: This is a standard DC measurement and will allow for a comparison between continuous DC-IV and Pulsed-IV measurements (NQ = Q points).
- Cold Pulsed-IV: This is a Pulsed-IV measurement where the Q points are set to (0,0), which removes any electric field across the device and allows the traps to all empty.

- Gate-lag Pulsed IV: This is a Pulsed-IV measurement in which the Q points are set to (-4,0), which will cause the traps dependent on the V_{GS} traps to be filled and the traps dependent on V_{DS} to empty. This will allow the effects of surface-state traps to be observed as a "gate-lag" compared to the cold pulsed-IV measurement.

- Drain-lag Pulsed IV: This is a Pulsed-IV measurement in which the Q points are set to (-4,15), which will cause the traps dependent on both V_{GS} and V_{DS} to be filled. This will allow the effects of bulk-state traps to be observed as a "drain-lag" when compared to the gate-lag Pulsed-IV measurement.

Pulsed-IV measurements showing gate and drain-lag, quantified through current collapse and shift R_{on} are shown in Figure 8.6 and key performance metrics are summarised in Table 8.3.

Table 8.3: Continuous DC-IV and Pulsed-IV Measurement Key Parameters. Current Density and Current Collapse has been taken from where $V_{GS} = 1V$, and $V_{DS} = 10V$

Parameter	No BB	$Al_{0.05}Ga_{0.95}N$ BB
Continuous DC Current Density (A/mm)	0.397	0.535
Cold Current Density (A/mm)	0.502	0.686
Gate-lag Current Collapse	49.9 %	17.8 %
Drain-lag Current Collapse	31.3 %	18.1 %
Continuous DC R_{on} (Ω/mm)	8.95	6.87
Cold R_{on} (Ω/mm)	8.75	6.74
Gate-lag R_{on} (Ω/mm)	11.0	7.02
Drain-lag R_{on} (Ω/mm)	23.1	8.63

For these measurements a different device layout was used in comparison to the DC-IV measurements. The L_{SD} has been increased from 5 to 15 μm. This will allow for further analysis of the thermal effect to see if the increase in L_{SD} allows the thermal problems to be mitigated.

Looking at the continuous DC measurement it can be seen that for the wafer with no back barrier there is a decrease of 5.79 % compared to 17.06 % for the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier when taking the maximum current density compared to the current density at $V_{DS} = 15$ V. The drop for the wafer with no back barrier

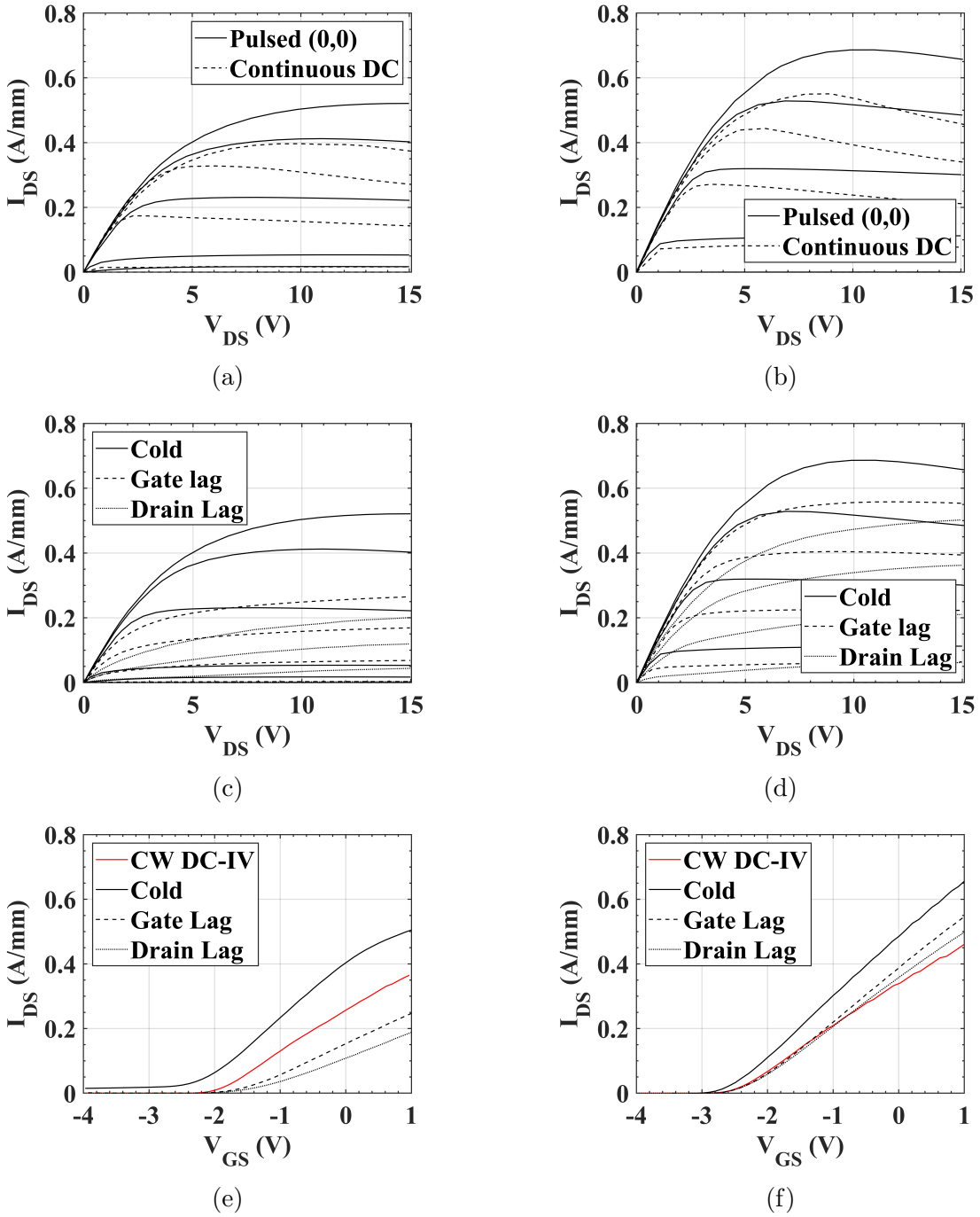


Figure 8.6: Pulsed-IV characteristics of 2-finger, 15 μm L_{DS}, 300 μm gate width GaN high-electron-mobility transistors (HEMTs): (a) and (b) show the DC and cold Pulse Comparison for the wafer with no back barrier and the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier respectively; (c) and (d) shows the comparison between cold, gate-lag, and drain-lag Pulsed-IV measurements for the wafer with no back barrier and the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier respectively; (e) and (f) shows the comparison between cold, gate-lag, and drain-lag transfer characteristics for the wafer with no back barrier and the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier respectively.

is comparable to the thermal effects seen in the previous DC-IV measurements, whilst the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier shows an improvement that is still significantly worse than the wafer with no back barrier. When comparing continuous DC and cold pulsed-IV measurements even with the duty cycle of 0.01 % for pulsed-IV measurements, there is still an observable self-heating effect in the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier after V_{DS} = 12 V under cold pulsed-IV conditions. If we take the point at which V_{DS} = 12 V, before self-heating is obvious with the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier, it can be observed that there is a decrease of 23.6 and 26.7 % for the wafer with no back barrier and the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier, respectively. The fact that there is a significant drop between continuous DC and cold pulsed-IV for the wafer with no back barrier, indicates that in continuous DC measurements there is likely some trapping effect that is either reducing I_{DS} in CW-DC beyond thermal effects or increasing I_{DS} during cold pulsed-IV measurements. The fact that the gap between the wafer with no back barrier and the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier shrinks to such a degree is an indication that the trap effects are more significant in the wafer with no back barrier than in the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier.

Looking at the wafer with no back barrier and the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier under pulsed IV stress, there are several other observations that can be made that support this theory. Looking at the pulsed-IV transfer plot in Figure 8.6e there is a significant deviation between the CW DC-IV and the cold pulsed-IV measurement. This threshold voltage shift and deterioration of pinch-off is likely attributed to a trapping effect that occurs when the gate is pulsed down. This will lead to an increase in current density in cold pulsed-IV and shows the presence of trapping states creating a significant deviation between CW DC-IV and cold pulsed-IV beyond the thermal effects for the wafer with no back barrier.

Continuing to look at these pulsed-IV measurements, a significant improvement in both gate and drain-lag is observed for the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier. The huge improvement is due to the $Al_{0.05}Ga_{0.95}N$ back barrier, improving

the confinement of the 2DEG and suppression of the traps in the buffer. The gate-lag improves from 49.9 to 17.8 % and is due to the suppression of the trap effect that causes the threshold change and poor pinch-off discussed above. drain-lag also improves from 31.3 to 18.1 % for Wafers 1 and 2, respectively. There is also a significant improvement in R_{on} under gate and drain-lag conditions. Under drain-lag conditions, the R_{on} is 168 % higher. This improvement in drain-lag is the specific reduction in trapping effects that was targeted in the study on the $Al_{0.05}Ga_{0.95}N$ back barrier.

In summary of these pulsed-IV measurements, the $Al_{0.05}Ga_{0.95}N$ back barrier is shown to be highly effective in the suppression of trap effects in AlGaN/GaN HEMTs. It has also been shown that with increasing L_{SD}, self-heating can be slightly reduced. This indicates that for high-voltage applications where large L_{SD} is required there are still potential applications where the $Al_{0.05}Ga_{0.95}N$ back barrier will be able to demonstrate significant improvements over no AlGaN back barrier.

8.3.3 Thermal Dependent Drain Current Transient Spectroscopy Measurements

Drain Current Transient (DCT) Spectroscopy measurements have been performed at three different temperatures (25, 85, and 125 °C) to compare trap energy levels between isolation methods. These measurements were performed in a dark, temperature controlled environment using a 200 mm semi-automatic thermal probe station. The Auriga Tri-State PIV from Focus Microwave was used to perform the pulsed measurements, using the long-pulse measurement capability. This system was then connected to GSG RF Probes via Auriga 67 GHz, 50 V, 1 A Bias Tees. A 50 Ω load was connected to the RF port to suppress device oscillations during the measurements. The long pulse was set with a span of 1 s, and the sample rate was initially set to 1 MHz and downsampled by 1 order of magnitude every decade after the pulse. After each measurement, the bias of the device was set at $V_{GS} = 0$ V and $V_{DS} = 0$ V, to ensure that the device was in a known state before and after each measurement.

The three key stages of the long pulse measurement are:

- Trap Filling Period: 500 μs filling period.
- Pulse Period: 500 μs pulse.
- Recovery Period: post-pulse to 1 s.

Two pulsing methods were performed: a single drain pulse, where QV_{DS} is pulsed from a low steady-state value to a high value and QV_{GS} is kept constant just above the threshold voltage; and a dual pulse where QV_{DS} is pulsed from a low steady-state value to a high value, and QV_{GS} is simultaneously pulsed from the steady-state value to below the threshold voltage to pinch off the device. The steady-state values are defined as Q points and the pulse values are defined as NQ points. In this study, the Q points were taken as $QV_{DS} = 2$ V, $QV_{GS} =$ -1.5 and -2.2 V for the wafer with no back barrier and the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier respectively. The

values of QV_{GS} were chosen to set the current in each device to approximately 50 mA / mm when in steady state. These Q points are constant between both pulse methods.

- Single Drain Pulse: NQ points are: $NQV_{GS} = QV_{GS}$ and $NQV_{DS} = 15$ V.
- Dual Pulse: NQ points are: $NQV_{GS} = -4$ V and $NQV_{DS} = 15$ V.

Both pulse methods were performed to determine the location of the traps and the effect of the $Al_{0.05}Ga_{0.95}N$ back barrier on the suppression of bulk trapping effects, through observations of the pulse recovery time, indicating the time constant of the traps and the maximum current drop in drain current after pulsing, indicating the quantity of trap states. Performing these measurements at several temperatures allows us to compare the change in trap time constants and extract trap energy levels.

The single drain pulse is a key indicator of drain-lag, and the dual pulse is a key indicator of both gate and drain-lag. Looking at recovery after pulse Figure 8.7, we can see that for the drain-lag measurement, there is a difference in recovery time at 25 °C, between the wafer with no back barrier and the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier. Since the wafer with no back barrier does not fully recover and appears to have been affected by the pulse, causing a temporary negative shift V_t. This has likely occurred because of the filling of shallow long-time-constant acceptor traps in the GaN channel layer, with time constant greater than that in the post-pulse capture window. The indication that these are shallow traps is that at 85 °C, this trapping effect has decreased significantly. This trapping effect is not apparent in the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier, and is likely due to the increased 2DEG confinement due to the $Al_{0.05}Ga_{0.95}N$ back barrier. Overall in comparison between these two wafers, there is a significant decrease in the trapping time constants for the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier and current drop post pulse. This indicates that the low Al concentration $Al_{0.05}Ga_{0.95}N$ back barrier is highly effective in suppressing deep trap stats in the buffer.

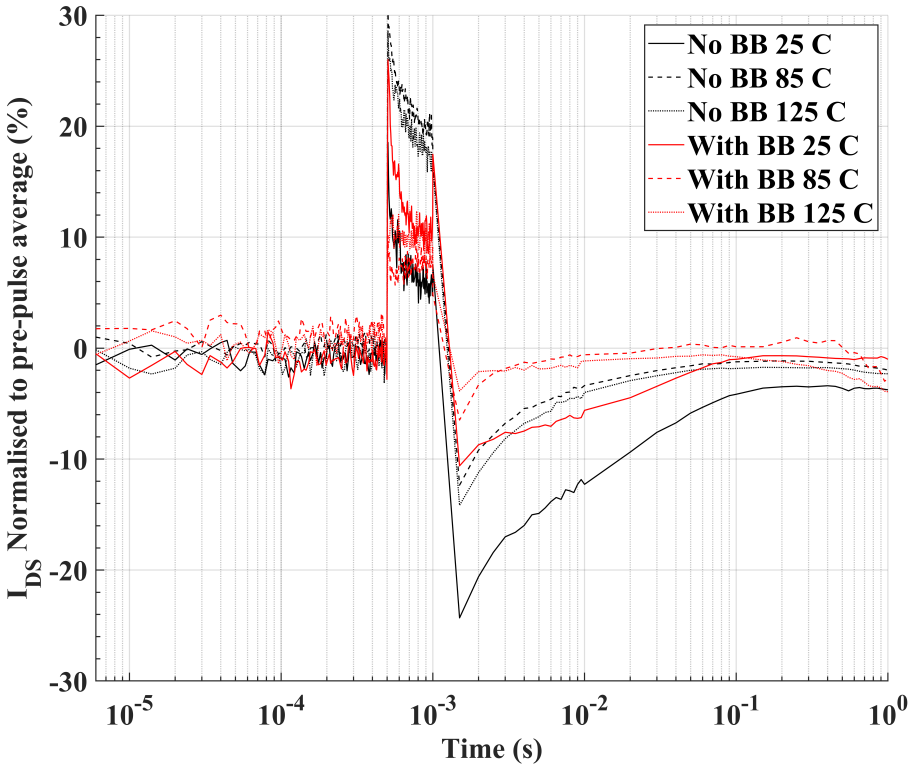
After 500 us, the percentage of current drop for both single-drain and dual-pulse is shown in Table 8.4.

Looking at the current recovery after the duel pulse, there is a very noticeable difference in recovery between the wafer with no back barrier and the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier. The current recovery for the wafer with no back barrier is largely independent of the temperature, which indicates the presence of deep trap states. The reason why the 25 °C measurement is no longer an outlier here is likely because the gate also is pulsed negative, which releases the electrons from the acceptor trap states in the GaN channel. This lack of dependence on temperature on these traps is the reason why the current drop does not change significantly between temperatures. The reason for the increase in current drop at 125 °C is due to other removal of other shallow trap stats, which compete with this trap. The wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier however, is dominated by a long time-constant shallow trap at 25 °C, and has a significant reduction in time constant as the temperature increases. However, when comparing wafer with no back barrier and the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier, it can be seen that the deep trap seen in the wafer with no back barrier has been effectively suppressed by the inclusion of the $Al_{0.05}Ga_{0.95}N$ back barrier proving its effectiveness at suppressing traps originating in the bulk epi-structure.

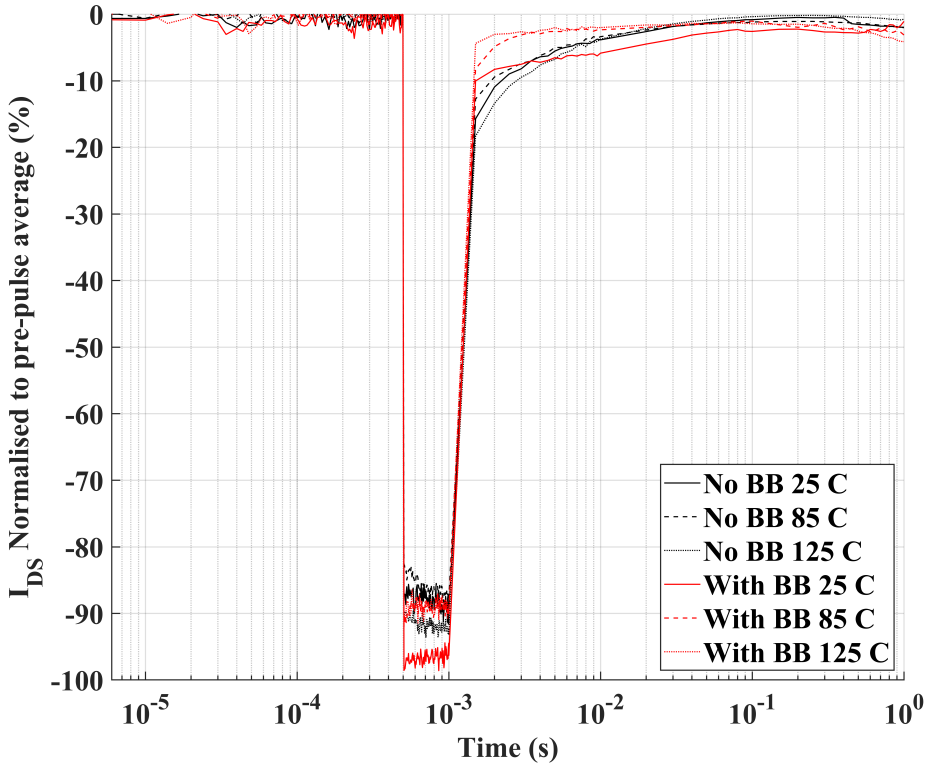
Table 8.4: DCTS current drop after 500 μs

Parameter	No BB	$Al_{0.05}Ga_{0.95}N$ BB
Single Pulse 25 °C	24.3 %	10.6 %
Single Pulse 85 °C	12.3 %	6.48 %
Single Pulse 125 °C	14.2 %	3.85 %
Dual Pulse 25 °C	15.7 %	10.0 %
Dual Pulse 85 °C	12.7 %	8.18 %
Dual Pulse 125 °C	18.3 %	4.38 %

Due to measurement equipment limitations presenting issues with the current noise floor, it is not possible to extract trapping energy states with certainty since Bayesian deconvolution is unable to reliably extract the transients. Any attempted filtering steps applied before lead to obscuring the transients in such a way that



(a)



(b)

Figure 8.7: Drain Current Transient Spectroscopy measurement results for a 2-finger, 300 μm gate width GaN high-electron-mobility transistors (HEMTs) with two different pulse conditions: (a) VGS held constant VDS pulsed from 2V to 15 V; (b) VGS pulsed to below Vt and VDS pulsed 2 V to 15 V.

they Bayesian deconvolution stage will just present a perfectly smooth signal. This will be addressed in future work with modifications to the measurement procedure, such as implementing multiple measurements and averaging to reduce noise and improvements to the system to allow a lower noise floor system to complete the analysis to determine the energy level of all traps.

8.3.4 Small Signal RF Measurements

Small-signal RF measurements were performed to determine the influence of the $Al_{0.05}Ga_{0.95}N$ Back Barrier on intrinsic and extrinsic device parasitics, as well as the effect of the $Al_{0.05}Ga_{0.95}N$ Back Barrier techniques on essential RF performance metrics f_t and f_{MAX}. On-Wafer measurements were performed using 150 μm GSG RF probes. The measurements were carried out on a 200 mm semi-automatic probe station, using a Keysight PNA model N5227B. This was interfaced with the Keysight N5293AX03 range extenders, which extend the range to 0.1 to 120 GHz and incorporate built-in bias tees. In addition, a Keysight B1500a semiconductor device parameter analyser was used for DC biasing and measurements. Both PNA and B1500a were controlled by Keysight IC-CAP software. Probe tip calibration was performed through eLRRM using the MPI AC2 calibration substrate.

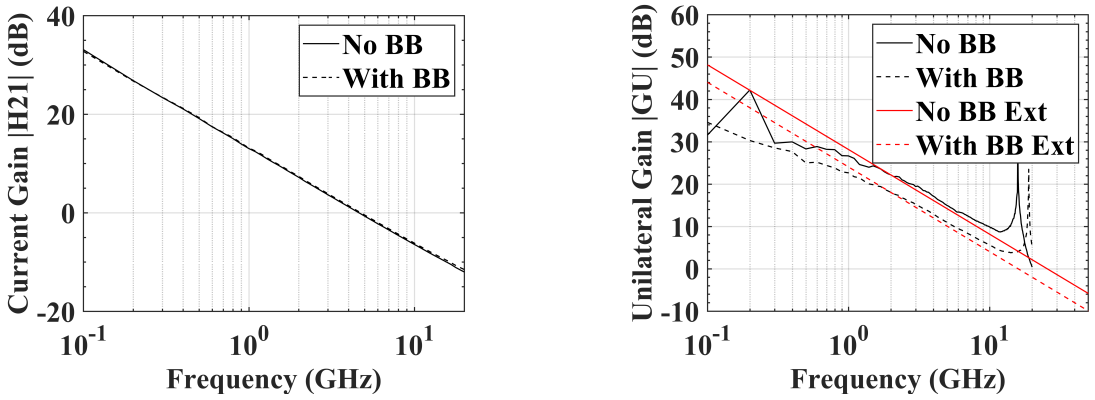
RF measurements were performed from 0.1 to 20 GHz at multiple different bias points to allow for small-signal model extraction:

- Pinch Off FET: Here, the gate voltage is set to below the threshold voltage $V_{GS} << V_t$ and V_{DS} is set to 0 V, to ensure a cold FET configuration.
- Hot FET: Here, V_{GS} is set for the maximum G_m and V_{DS} is set to 15 V.
- Forward bias: Here, we ensure V_{DS} is set to 0 V, and then bias the gate to forward conduction to a specific gate current. For this type of measurement, three measurements are performed with gate current (I_{GS}) set to 200 μA/mm, 400 μA/mm, and 600 μa/mm for each measurement.

The small signal f_t and f_{MAX} for a 2-finger, 5 μm L_{DS}, 125 μm gate width device, fabricated on both wafers, is presented in Figure 8.8 with the extracted values shown in Table 8.5. Due to transients in the raw measurement data, linear extrapolation has been used to determine f_{MAX} with a gradient of -20 dB/decade.

Table 8.5: Small signal RF f_t and f_{MAX} for no BB and with an$Al_{0.05}Ga_{0.95}N$ BB

Parameter	No BB	$Al_{0.05}Ga_{0.95}N$ BB
f_t	4.68 GHz	4.78 GHz
f_{MAX}	25.1 GHz	16.2 GHz



(a) (b)

Figure 8.8: RF S-Parameter measurement results showing (a) f_t and (b) f_{MAX} for no back barrier and $Al_{0.05}Ga_{0.95}N$ back barrier

Table 8.6: Comparison of extracted values for Extrinsic and Intrinsic parameters for no back barrier and with the $Al_{0.05}Ga_{0.95}N$ back barrier

Extrinsic Parameters		
Parameter	No BB	$Al_{0.05}Ga_{0.95}N$ BB
C_{pg} (fF)	67.8	129
C_{pd} (fF)	72.4	93.7
L_s (pH)	21.1	50.4
L_g (pH)	128	103
L_d (pH)	61.1	85.0
R_d (Ω)	131	108
R_s (Ω)	8.54	10.6
R_g (Ω)	0.126	0.126
Intrinsic Parameters		
Parameter	No BB	$Al_{0.05}Ga_{0.95}N$ BB
C_{gd} (fF)	24.0	18.9
C_{gs} (fF)	1670	1680
C_{ds} (fF)	1.00	0.147
τ (ps)	6.18	4.30
G_m (mS/mm)	252	305
R_{in} (Ω)	0.786	0.718
R_{ds} (Ω)	1100	386

The small signal measurements show that whilst the f_t for both wafers is extremely similar, there is a significant deviation with the wafer with no back barrier

having an f_{MAX} of 55 % higher than the the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier. This indicates that the $Al_{0.05}Ga_{0.95}N$ back barrier reduces the high-frequency performance of the device. This contrasts to the findings in the literature in which AlGaN back barriers have been found to increase RF performance by reducing the effects of the short channel [52]. Therefore, this will require further investigation with reduced L_g to verify these results.

8.3.5 Large Signal Measurements

Large-signal RF measurements were performed to determine the influence of the $Al_{0.05}Ga_{0.95}N$ back barrier on the device PAE.

On-wafer load pull was performed using 150 μm GSG RF probes. The measurements were carried out on a 200 mm semi-automatic probe station, utilising a real-time vector-receiver active load-pull system, capable of measurements up to 67 GHz. This system consists of a 67 GHz Rohde & Schwartz (ZVA 67) Vector Network Analyser (VNA), using an external test set based on Marki 2-67 GHz (C-0265) dual-directional couplers. The complete calibration procedure and more details on the system can be found in [38].

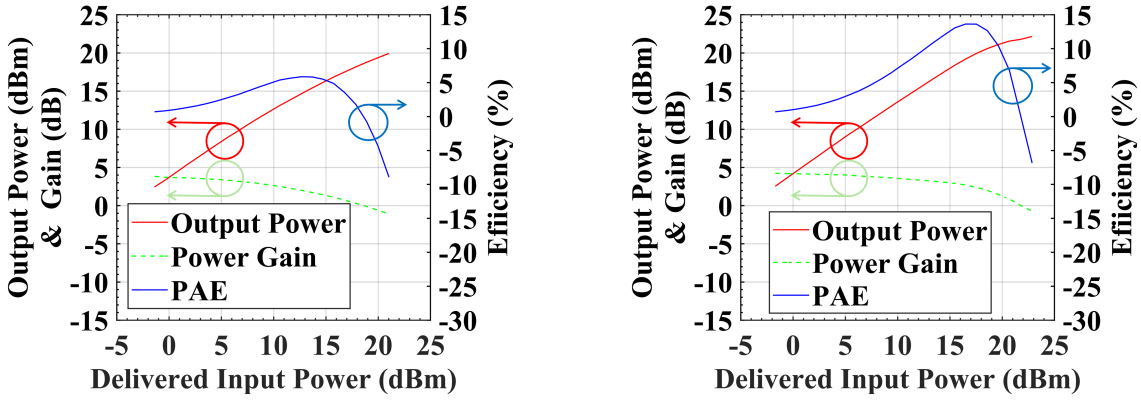


Figure 8.9: RF power sweep from -30 to -5 DBm at load impedance of maximum power for a 2 finger 125 um device with 5 um L_{sd} GaN high-electron-mobility transistors (HEMTs): (a) without back barrier; (b) with $Al_{0.05}Ga_{0.95}N$ back barrier.

The load pull was performed at 8 GHz, to identify the impedance of maximum power. Once this had been found, a power sweep was performed at this impedance from -30 to -5 dBm. The device was biased with V_{DS} = 12 V, I_{DSQ} = 50 mA/mm. The devices measured are the same as those used for RF small signal measurements and is a 2-finger gate width device of 5 μm L_{DS}, 125 μm which was fabricated on both wafers.

Looking at Figure 8.9, the key metric of PAE shows a significant improvement in the wafer with $Al_{0.05}Ga_{0.95}N$ back barrier due to the $Al_{0.05}Ga_{0.95}N$ back barrier compared to the wafer with no back barrier. The wafer with no back barrier had

a maximum PAE of 5.84 % compared to 13.6 % for the $Al_{0.05}Ga_{0.95}N$ back barrier. This shows a significant improvement in the RF efficiency as a result of the suppression of trap states through the inclusion of an $Al_{0.05}Ga_{0.95}N$ back barrier. It is important to note that the measurement at 8 GHz is much higher than the intended operational frequency of devices of this gate length. Typically a frequency of 1 or 2 GHz would be chosen. However, 8 GHz was used in this case to allow for the increased RF performance of the wafer with no back barrier to be taken into account.

8.4 Conclusion

Overall, for DC-IV and pulsed-IV measurements, the inclusion of the $Al_{0.05}Ga_{0.95}N$ back barrier offers a significant improvement in device leakage, current density, and suppression of trap states, but with a significant drawback to the thermal conductivity of the structure. This results in substantially higher self-heating, which could potentially hinder the effectiveness of this structure in applications that require high power density, or where there are significant thermal constraints due to limited cooling budget.

Through the use of DCTS it can be inferred that in the wafer with no back barrier there are shallow acceptor traps in the GaN channel with a long time constant that is greater than the DCTS capture window. This trapping effect is not present in the wafer with the $Al_{0.05}Ga_{0.95}N$ back barrier indicating that this trap is no longer effecting the 2DEG due to the inclusion of the $Al_{0.05}Ga_{0.95}N$ back barrier. However, DCTS also revealed a new trap that is not apparent in the wafer with no back barrier, under the dual pulse. This is a shallow long time constant trap, that is located under the gate. The exact location and cause of this trap requires a deeper investigation.

The small signal RF measurements show a significant decrease in f_{MAX} due to the inclusion of the $Al_{0.05}Ga_{0.95}N$ back barrier. This is contrary to other findings in the literature and will require future investigation.

However, despite the lowered performance for small signal RF, when investigating PAE using large signal RF measurements, it has been found that there is a significant improvement in maximum PAE at 8 GHz due to the $Al_{0.05}Ga_{0.95}N$ barrier.

Chapter 9

Conclusion and Future Work

9.1 Conclusion

Although GaN HEMTs have shown extremely promising performance in high-frequency (>100 GHz) RF applications, they are still affected by poor linearity and efficiency due to trapping effects. Through detailed characterisation and understanding of trapping effects, it is possible to improve GaN HEMT fabrication processes and optimise the epi-structures to enable improved linearity and efficiency of ALGaN/GaN HEMTs.

In this work, the overarching research goals were the development of trap characterisation and analysis techniques, and then the application of these techniques to further improve the analysis that can be performed on device fabrication and material variations. This more detailed understanding of the effects of fabrication and material epi-structure on device performance, will result in the ability for the research group to continue to further develop and improve device fabrication. Both of these goals have been met with the successful development of trap characterisation techniques and analysis methods. The techniques have then been demonstrated to allow for further understanding of the effects of trapping in the performance of the device, allowing for changes in both the fabrication processes and the epi-structure to be compared.

9.1.1 DC-IV Measurements Investigating Trap Effects In GaN HEMTs

DC-IV characterisation was performed to enable the development of trap characterisation and identification capability with close collaboration with IQE, where a simple epi-structure was grown to allow this deep investigation into characterisation techniques and methods for trap identification. Multiple different MIS-HEMT layouts were designed to allow the investigation of device topology and trapping effects. This wafer was processed at an external foundry to ensure high repeatability across multiple fabrication runs. In this investigation multiple trapping effects were observed in the DC-IV characteristics, which has resulted in the development of an understanding of trap location and behaviour in the epi-structure. Through multiple MIS-HEMT devices, it was possible to identify the cause and trap locations of the kink effect. In addition, observe multiple competing trapping mechanisms through DC-IV output measurements with variations of V_{DSMax}. A new trapping phenomenon was also observed in the output transconductance that appeared as an output transconductance overshoot, occurring at a consistent V_{DS} value. Additionally, a trap mechanism was observed in the DC-IV transfer characteristics appearing as a transconductance overshoot, occurring at a fixed V_{GS} value.

Through all of use of these DC-IV characterisation techniques it has been possible to identify multiple trap locations and states, allowing for the development of new understanding of the correlation between trap location and effect on device performance. The device variations also allowed for a deep understanding of the effect of device layout on trapping effects to be developed.

The trap causing the kink effect in these MISHEMTs is assumed to be in the AlGaN layer, and the de-trapping mechanism has been confirmed to be through the Poole-Frenekel effect. This was determined after evaluating the relationship between the kink effect and different device topologies.

Multiple competing trapping mechanisms have also been identified through V_{DSMax} variations, these are minority carrier trapping in the barrier at low V_{DS} values and

electron trapping in the barrier and buffer at high V_{DS} values.

A new trapping mechanism has been discovered that consists of a spike in the output transconductance.This trap has been identified as a shallow acceptor trap in the GaN channel close to the 2DEG.

The trapping effect that causes the transfer transconductance spike has been determined to be a deep, short, time-constant trap that is well defined in the lattice structure.

9.1.2 Comparison of Isolation Methods on GaN HEMT Performance

In this section, GaN HEMTs were fabricated using two different processes to investigate the effect of two different isolation methods on AlGaN/GaN HEMT performance. Through the improved trap-characterisation techniques that have been developed, it has been shown that there is a significant reduction in the trapping effects for ion implantation compared to the mesa etch for device isolation in AlGaN/GaN HEMTs. These results indicate that the mesa etch causes significant damage at the etch surface and leads to a significant increase in trap states in the GaN channel that results in an increase in current collapse under both gate and drain lag conditions. The DC-IV measurement results indicate that ion implantation has improved key performance metrics such as reducing gate leakage and drain-source leakage in pinch-off condition. However, when comparing the RF results, it is apparent that there is an issue with the ion isolation technique used, as significant degradation of 46.35 % and 10.11 % to f_t and f_{MAX} is observed, respectively. This decrease in RF performance is likely due to increased RF leakage caused by ion implantation. However, because f_t is degraded much more than expected, there may also be another effect that has not yet been identified that causes this decrease in RF performance.

Therefore, while the ion implantation isolation method has been determined to result in less degradation in device performance compared to the mesa etch process,

there is still a potential issue with the ion implantation method leading to a degraded RF performance for the device f_t.

9.1.3 Impact of AlGaN Barrier Thickness on GaN-on-Si RF HEMT Performance and Trapping Effects

In this section, GaN HEMTs were fabricated to investigate the effect of variations in the AlGaN barrier thickness on the AlGaN/GaN HEMT performance. Through trapping analysis, it was revealed that both the 21 and 9 nm AlGaN barrier structures exhibited increased surface state trap quantities compared to the 15 nm barrier due to increased threading dislocations and interface defects in the 21 nm barrier structure, and reduced carrier confinement, leading to reduced channel sheet density in the 9 nm barrier. This resulted in the 15 nm barrier displaying the least surface state traps. The bulk trap states were similar for the 21 and 15 nm barrier as expected, however there is significantly less current collapse during Pulsed-IV measurements under drain lag conditions for the 9 nm barrier, due to the increased leakage into the buffer from poor carrier confinement. However, all trap states in these three samples were found to be shallow with almost instant recovery of the device at 125 °C during the DCTS measurements. Through DC-IV measurements, it is apparent that as the barrier thickness decreases, there is an increase in source-drain leakage, along with an increase in the maximum current density and transconductance. However, once again the 9 nm barrier shows significant issues, such as poor pinch-off characteristics. Through the RF small-signal measurements it was apparent that the 21 nm barrier thickness had the highest performance due to the reduced intrinsic capacitance. However, due to the large gate lengths (1 μm) the results do not take into account the advantage of the thinner barriers that can be gained from aggressive gate scaling.

Overall, from this work, it is apparent that the best compromise in barrier thickness for these wafers is 15 nm, due to the improved DC-IV and trapping performance, while for RF performance, the reduction in barrier thickness from 21 to 15 nm will

allow a reduction of 30 % in L_g, which is expected to lead to a significant improvement in RF performance when compared to the 21 nm barrier with a fixed aspect ratio L_g: barrier thickness.

9.1.4 Impact of AlGaN Back-Barrier on GaN-on-Si RF HEMT Performance and Trapping Effects

In this section, GaN HEMTs were fabricated to investigate the effect of a low Al-concentration AlGaN back barrier on the performance of AlGaN / GaN HEMTs. The DC-IV and pulsed-IV measurements show that the use of an AlGaN back barrier offers a significant improvement in device leakage, current density, and suppression of trap states, but due to poor thermal conductivity results in increased device self-heating. Through DCTS measurements, inclusion of the AlGaN back barrier has been shown to remove the effect of the shallow acceptor traps in the GaN channel that were identified. Through small-signal RF measurements, a decrease in device F_{MAX} was observed. However, when looking at large signal power sweep performed at 8 GHz, the inclusion of the AlGaN back barrier and thus the suppression of trap states resulted in an improvement in device PAE, and maximum output power.

In general, it can be determined that the inclusion of an AlGaN back barrier leads to improved device performance, through both increased carrier confinement and the suppression of trap states, resulting in higher-efficiency devices.

9.2 Future Work

The trap characterisation and analysis methods developed in this work will form the base of a new trap characterisation and analysis stage, during the device testing phase. This will This will allow for continued improvements to the fabrication process and result in improved GaN HEMT technology.

9.2.1 Trap Characterisation and Analysis Techniques

The trap characterisation and analysis methods developed in this work require further development to enable trap energy level's, location, and trap capture cross section to be accurately determined. This will require further optimisation of the DCTS measurement process. Either repeating the measurement multiple times and averaging for the result or developing a custom measurement algorithm where a very high sample rate is used for the measurement and then an averaging method is applied in short time windows to replicate the traditional data acquisition method for standard DC-IV or Pulsed-IV measurement techniques. Both of these options will be explored along with other potential solutions.

The use of low-frequency admittance parameters for trap analysis should also be considered as a potential characterisation method because of the ability for very quick measurement and analysis time. This is something that will also be investigated.

Overall, this work has laid the foundation for further development and improvement of the trap characterisation and analysis methods, which will continue to be further developed.

9.2.2 Technology Development

In this work, it has been seen that there are several areas in which further work is required on the development of the technology to enable higher-performance devices.

In the isolation study, the ion implantation method leads to a severe degradation to f_t compared to mesa etch. This will require further investigation as to why the RF performance is so poor. Currently, work is underway to analyse these GaN-on-SiC samples to determine if the substrate has any impact on this RF degradation.

In both the AlGaN barrier thickness and AlGaN back barrier investigation, the use of short gate lengths would allow for a more detailed investigation into the ability to aggressively scale these gate lengths and would provide a more definitive conclusion on the true potential of these epi-structure variations on improved device

performance.

After successful optimisation of the DCTS measurements, it would be beneficial to remeasure and extract the trap energy level, trap cross section, and trap locations, for all investigations to identify the exact change in trapping effects due to the technology variation.

9.2.3 Further DC-IV Trap Investigations

Further investigation should be conducted on the kink effect, with a focus on moving from a qualitative to a quantitative analysis through the development of a technique to assess the full effect of the kink. Further investigation into the effect of more device variations such as gate width, and number of gate fingers on the kink would also provide an interesting insight into this trapping behaviour.

The output transconductance spike is an interesting trapping effect that needs a full investigation to determine the exact cause of this effect. This effect will require an investigation into the effect of device topology and an investigation to determine the traps dependence on temperature.

The effect of the MIS-HEMT dielectric on V_t hysteresis should also be determined through a comparison between the MIS gates and Schottky gates to determine if this effect is due to the gate dielectric.

The transfer transconductance overshoot needs further investigation to determine the exact trap that is causing this effect and the location of this trap. This will require a targeted characterisation, such as capacitance-voltage (C-V) measurements at the specific target voltages. The effect of impact ionisation on this trap should also be investigated by measuring the low current leakage of the gate, to determine whether there is any increase in gate current during the g_m overshoot.

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