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# Principle and Implementation of Active Ground Fault Arc Suppression Based on Hybrid MMC in AC/DC Distribution Network

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**Abstract**—A single-phase-to-ground (SPG) fault in a neutral non-effectively grounded AC distribution network may cause the arc at the fault point and a power supply interruption, permeating the zero-sequence voltage into the DC network and the non-fault AC-side of AC/DC hybrid distribution networks (HDNs). This paper proposes a flexible control method for a modified hybrid modular multilevel converter (HMMC), incorporating an additional full-bridge submodules (FBSM) cluster at its DC side, to deal with SPG faults in HDN. The HMMC includes a modified modular multilevel converter with a zero-sequence current flow path to realize active ground fault arc suppression (AGAS) and an FBSM cluster in its DC side to block the zero-sequence component to the DC grid and the non-fault circuits of HDN. The operation principles of the HMMC that achieves AGAS and zero-sequence voltage transmission suppression (ZVTS) are presented. The HMMC can realize AGAS when there is an SPG fault on the AC side, and ZVTS can be realized on the DC side by utilizing the FBSM cluster. The flexible control method proposed herein can ensure the normal operation of the HMMC under SPG fault conditions, achieve power transfer during fault current suppression, and realize ZVTS during arc suppression. Simulation and experimental results verify the feasibility and validity of the proposed HMMC and its flexible control method.

**Index Terms**—Hybrid modular multilevel converter (HMMC), single-phase-to-ground (SPG) fault, arc suppression, zero-sequence voltage suppression, hybrid distribution networks.

## NOMENCLATURE

|                |                                                              |
|----------------|--------------------------------------------------------------|
| $E_j$          | power supply voltage phasors, $j = A, B, C$                  |
| $U_j$          | phase-to-ground voltage phasors                              |
| $U_{jf}$       | phase-to-ground voltage phasors after SPG fault              |
| $U_0$          | zero-sequence voltage phasor before AGAS                     |
| $U'_0$         | zero-sequence voltage phasor after AGAS                      |
| $U_f^+, U_f^-$ | positive- and negative-sequence voltage phasor               |
| $I_{jG}$       | phase-to-ground leakage current phasor                       |
| $I_f$          | ground fault current phasor                                  |
| $I_Z$          | zero-sequence current phasor provided by HMMC                |
| $I_{jZ}$       | zero-sequence current phasor generated by $j$ -phase of HMMC |
| $\omega$       | angular frequency of AC-side supply power                    |

|                              |                                                                               |
|------------------------------|-------------------------------------------------------------------------------|
| $U_m$                        | rated voltage magnitude of supply power                                       |
| $L_{arm}$                    | arm inductance of HMMC                                                        |
| $C_{dc}$                     | DC-side ground capacitance in HMMC                                            |
| $R_{dc}$                     | DC-side ground resistor in HMMC                                               |
| $Z_{dc}$                     | DC-side ground impedance in HMMC                                              |
| $C_j$                        | total phase-to-ground leakage capacitance                                     |
| $r_j$                        | total phase-to-ground leakage resistance                                      |
| $R_f$                        | ground fault resistance at the fault point                                    |
| $u_{pj}, u_{nj}$             | $j$ -phase upper- and lower-arm voltages                                      |
| $u_{pj}^+, u_{nj}^+$         | $j$ -phase positive-sequence upper- and lower-arm voltages                    |
| $u_{dcp}, u_{dcn}$           | DC-side positive and negative pole-to-ground voltages before the FBSM cluster |
| $u_{dc}^+, u_{dc}^-$         | DC-side positive and negative pole-to-ground voltages after the FBSM cluster  |
| $e_j$                        | instantaneous value of $j$ -phase voltage of power supply                     |
| $u_j$                        | instantaneous value of $j$ -phase to ground voltage                           |
| $i_j$                        | instantaneous value of $j$ -phase current of HMMC                             |
| $I_{pos}, I_{neg}, I_{zero}$ | positive-, negative- and zero-sequence currents of HMMC                       |
| $u_{0\_ctrl}$                | zero-sequence reference voltage controlled by HMMC                            |
| $u_0$                        | instantaneous value of zero-sequence voltage                                  |
| $U_{dc\_ref}$                | DC-side pole-to-pole reference voltage of HMMC                                |
| $Z_{c01}, Z_{c02}$           | zero-sequence impedance of DN1 and DN2                                        |
| $Z_{MMC2}$                   | zero-sequence impedance of HMMC2                                              |
| $Z_{DC1-2}$                  | zero-sequence impedance of DC line                                            |
| $I_{dcz}$                    | DC-side current before the DC-side grounding circuit                          |
| $I_{dc}$                     | DC-side current after the DC-side grounding circuit                           |
| $X$                          | number count of submodules in the FBSM cluster                                |
| $n, m$                       | number count of HBSM and FBSM in each arm                                     |
| $M$                          | voltage modulation ratio of HMMC                                              |
| $U_{max}, U_{min}$           | maximum and minimum output voltages of each HMMC arm                          |
| $U_{c\_ref}$                 | submodule capacitor reference voltage of HMMC arm                             |
| $u_{c\_pj k}, u_{c\_nj k}$   | $k$ th submodule capacitor voltage of $j$ -phase                              |

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|                       |                                                                                                                               |
|-----------------------|-------------------------------------------------------------------------------------------------------------------------------|
|                       | upper- and lower-arm of HMMC                                                                                                  |
| $u_{FBcyx}$           | $x$ th submodule output reference voltage of FBSM cluster positive ( $y = p$ ) and negative pole ( $y = n$ ), $x = 1 \dots X$ |
| $U_{FBc\_ref}$        | submodule capacitor reference voltage of FBSM cluster                                                                         |
| $u_{FBc\_yx}$         | $x$ th submodule capacitor voltage of FBSM cluster positive and negative pole                                                 |
| $\Delta u_{dc0}$      | zero-sequence voltage ripple at the pole-to-ground voltage                                                                    |
| $\Delta U_{dc0 \max}$ | maximum amplitude of the zero-sequence voltage ripple $\Delta u_{dc0}$                                                        |

## I. INTRODUCTION

MEDIUM-voltage distribution networks are closely integrated with the users, distributed renewable energy generators, energy storage devices, and various electrical loads. However, complex environments around power lines can often lead to unintended contacts between power lines and objects such as tree branches, ground or buildings, resulting in single-phase-to-ground (SPG) faults [1]. Medium-voltage distribution networks generally adopt either neutral non-effectively grounded systems or neutral directly grounded systems [2]. Each configuration responds differently to SPG faults, leading to distinct protection challenges. In neutral directly grounded systems, an SPG fault typically results in a significant overcurrent, which can be effectively detected and mitigated using conventional AC protection equipment, such as relays and breakers. These pieces of equipment are therefore well-suited to handling such faults through established protection mechanisms. In contrast, non-effectively grounded systems exhibit a different fault behavior. Rather than producing large fault currents, an SPG fault in this configuration tends to cause overvoltages and the formation of an arc at the fault point, making fault detection and isolation far more complex. This condition significantly increases the risk of equipment damage and safety hazards for personnel [3], [4]. To address this issue, installing a fault arc suppression device helps mitigate these risks by promptly eliminating the arc, thereby minimizing potential damage.

Traditional arc suppression solutions typically rely on passive arc suppression devices (PASDs), such as arc suppression coils (ASCs) and ground fault transfer devices (GFTDs). The ASC can only suppress an arc by injecting an inductive current to compensate for the capacitive current; however, it cannot compensate for active and harmonic components [5], [6]. The GFTD is typically installed at the substation. It mitigates arcs by forcing the fault phase voltage to zero during an SPG fault zero through direct grounding [7]. While this approach helps transfer the fault current to the GFTD, it impacts the whole distribution network considerably. Overall, PASDs generally exhibit poor arc suppression performance. However, with advances in power electronics, PASDs are evolving into active arc suppression devices (AASDs), eliciting more effective and flexible arc suppression strategies.

AASD-based solutions can be categorized into two types based on their operation principles: active current-type arc

suppression (ACAS) and active voltage-type arc suppression (AVAS). ACAS requires the accurate calculation of the suppression current in addition to the precise identification of the harmonic, active, and reactive components of the fault current [8], [9]. Although ACAS can be achieved using different power electronic devices and control methods, the arc suppression performance relies heavily on the measurement of line-to-ground parameters and the accurate localization of the fault point. In case of AVAS, AASDs actively regulate the neutral-to-ground voltage to the opposite of the supply voltage at fault phase. AVAS is not only unaffected by line-to-ground distributed parameters and residual currents but also easy to implement.

With the advancement of power electronic devices, numerous AASD solutions have emerged [10]. A typical configuration consists of a single-phase inverter connected to the neutral-to-ground path to control the fault phase voltage to zero [11]. However, an additional zig-zag grounding transformer is usually required to create a neutral point for most medium-voltage distribution networks. The neutral point may also comprise an ASC combined with a cascaded H-bridge (CHB) inverter [12], or a CHB inverter linked to a grounding transformer [13]. Alternatively, a three-phase configuration [14]–[16] can be directly connected to the distribution network to enable active arc suppression without the need for a grounding transformer [17]. A two-phase T-type CHB inverter without a DC source and its coordinated control scheme has been proposed to reduce the high cost of CHB inverters with DC power supplies [18]. Furthermore, a CHB-based power electronic transformer (PET) with ASC grounding in a Y-connected configuration has been reported to enable coordinated operation of the PET and ASC [19]. Nevertheless, AASD-based solutions require a large-capacity power electronic device to mitigate fault-induced arcs.

All methods described above have a common drawback: the need for specialized inverters and DC power sources at the station. Since these devices are used infrequently, only during arc suppression or partial reactive power compensation, they have very low utilization during non-fault periods, resulting in high investment costs with limited functionality [11]. The rapid development of power electronic technology has resulted in the widespread use of power electronic converters in distribution networks [20]–[22], providing a new approach for ground fault arc suppression with functional reuse of installed devices.

Recently, AC/DC hybrid distribution networks (HDNs) have drawn significant attention for their excellent performance in renewable energy integration. The key equipment in HDNs is the power electronic converter that interconnects the AC and DC networks. Modular multilevel converters (MMCs) show good application prospects in 10-kV HDNs, demonstrating high efficiency, modularity, redundant design, and fault ride-through (FRT) capability [23]–[25]. Recent engineering applications of MMCs include the transformerless MMC-based AC/DC HDN projects in Hangzhou [26], and Zhuhai [27] in China.

The use of transformerless MMCs is an attractive option to reduce costs in AC/DC HDNs [28]–[30]. MMCs can transfer

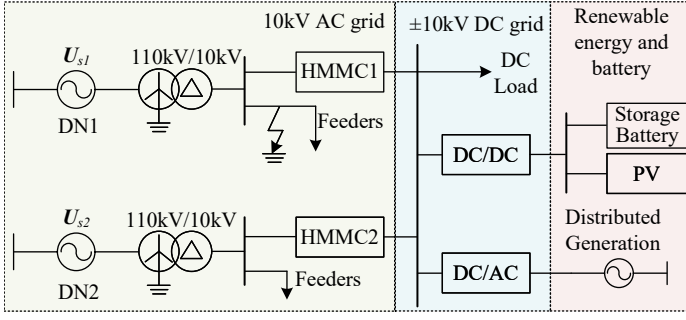


Fig. 1. Architecture overview of AC/DC HDN with HMMC interconnection.

power between AC and DC grids under normal operating conditions. During grid fault conditions, MMCs must switch to the FRT mode to deal with the fault. For example, the authors in [26] proposed an advanced zero-sequence current controller to suppress overcurrent for the FRT control of transformerless MMC, avoiding the shutdown of the MMC. For the valve-side SPG fault in MMC-HVDC station, the authors in [31] proposed an overvoltage suppression strategy based on zero-sequence voltage modulation. Under asymmetrical fault, MMCs in AC/DC HDN should limit fault current [32]. When the SPG fault occurs for the full-bridge MMC (FB-MMC)-based bipolar HVDC, the FRT strategies were also investigated to protect the FB-MMC during the fault, avoiding severe overvoltage in submodule capacitors [33].

Existing FRT strategies typically involve the regulation of MMCs to limit overcurrent, suppress overvoltage in full-bridge submodules (FBSMs), and prevent zero-sequence voltage from entering into the DC network and non-fault side of HDNs [26]. Although various FRT techniques have been studied to enhance the fault tolerance of FB MMCs under AC and DC fault conditions, their implementation under arc suppression conditions has not been investigated adequately.

The difference between FRT and arc suppression is that arc suppression focuses on addressing faults in distribution networks rather than ensuring that the DC side is unaffected by AC faults. If MMC is to be used under arc suppression conditions, they should be modified by constructing a grounding circuit with a zero-sequence current flow path [34]. This way, MMC can actively suppress the ground fault current to zero by controlling the zero-sequence voltage of the bridge arm, achieving active ground fault arc suppression (AGAS). Note that the influence of the zero-sequence voltage transmission between AC and DC HDNs should be considered during the arc suppression period. Furthermore, since AGAS and FRT both handle at the zero-sequence axis, with AGAS aiming to regulate the zero-sequence voltage and FRT aiming to suppress it, their objectives are inherently contradictory. Therefore, the negative effect of the zero-sequence component for arc suppression should be considered carefully to avoid degrading the power quality of the DC grid and the non-fault side of the HDN.

To address these challenges, a novel hybrid modular multi-level converter (HMMC) with AC-side AGAS and DC-side

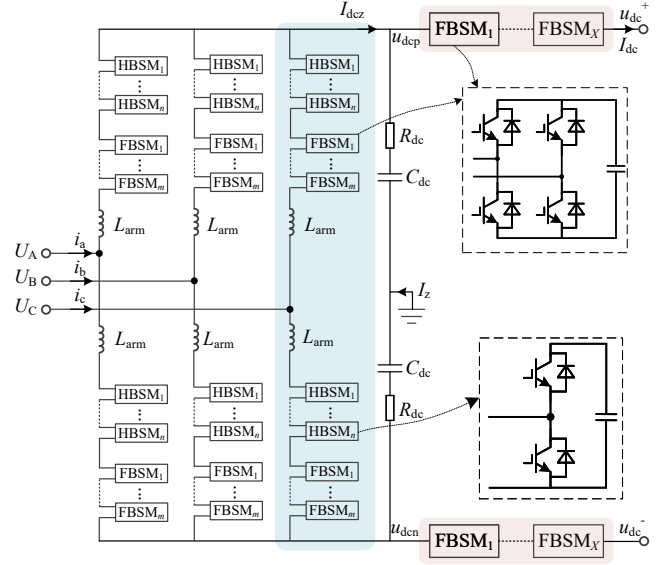


Fig. 2. The modified HMMC topology.

zero-sequence voltage transmission suppression (ZVTS) is proposed to deal with SPG faults in neutral non-effectively grounded systems. The modified HMMC configures the DC grounding circuit with resistors and capacitors to establish a the zero-sequence path. Analytical expressions describing the suppression of the zero-sequence fault current are provided. Then, AGAS control can be achieved by controlling the zero-axis component in the dq0 reference frame. In addition, the principle of zero-sequence voltage transmission between the AC and DC networks during SPG faults is analyzed. An FBSM cluster is configured at the DC-side of the HMMC to block the zero-sequence voltage and ensure the safety and power quality of the non-fault side of the HDN during AGAS. The proposed method is verified via simulations and experiments.

The rest of this paper is organized as follows. In Section II, the HMMC topology is described. Section III discusses the principle of AGAS and ZVTS. The AGAS and ZVTS strategies are elaborated in Section IV. The simulation results are presented in Section V. The experimental results are discussed in Section VI. Finally, Section VII concludes the article.

## II. ARCHITECTURE OF AC/DC HDNs WITH THE HMMC TOPOLOGY

The architecture of AC/DC HDNs with HMMC interconnection is shown in Fig.1. AC/DC HDNs consist of AC and DC sub-networks. Medium-voltage AC distribution network with the neutral non-effectively grounded configuration is developed using an isolation Yg-d transformer (110 kV/10 kV). The line-to-line voltage of the AC network is 10 kV. Transformerless HMMCs are connected to distribution networks 1 and 2. The DC-sides of the HMMCs are connected to form a DC bus with the  $\pm 10$  kV pole voltage. This DC bus can interface with DC loads, storage batteries, photovoltaic power generation, and various distributed power sources.

The modified HMMC is shown in Fig.2. Each arm of the HMMC consists of  $n$  half-bridge submodules (HBSMs) and

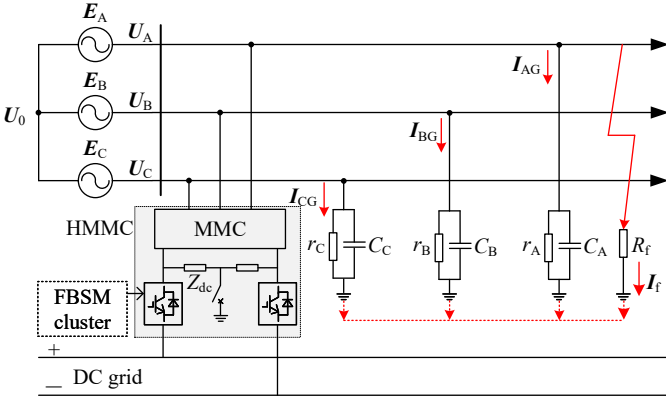


Fig. 3. HMMC without AGAS when the SPG fault occurs.

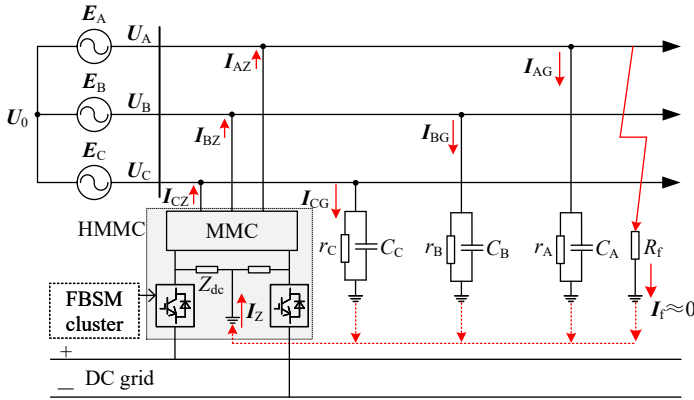


Fig. 4. Equivalent circuit of HMMC-based DN with AGAS when the SPG fault occurs.

$m$  FBSMs. The positive and negative poles of the DC side are grounded through capacitor  $C_{dc}$  and resistor  $R_{dc}$ , forming a grounding path for zero-sequence current during AGAS. The FBSM clusters are added to the positive and negative poles of the HMMC to block the zero-sequence components from entering into the DC network.  $U_j$  represents  $j$ -phase voltage phasor in AC network, and  $L_{arm}$  represents the arm inductance.

### III. OPERATION PRINCIPLES OF AGAS AND ZVTS

#### A. Operation Principle of AGAS using HMMC

Assume that an SPG fault occurs in the A phase of DN1. A simplified distribution network of a neutral point grounded through the HMMC is shown in Fig.3.  $E_A$ ,  $E_B$ , and  $E_C$  denote the three-phase power supply voltage phasors.  $U_A$ ,  $U_B$ ,  $U_C$  denote the three-phase-to-ground voltage phasors.  $U_0$  denotes the neutral zero-sequence voltage phasor, where  $U_j = U_0 + E_j$ .  $C_j$  and  $r_j$  denote the total phase-to-ground leakage capacitance and resistance in DN1.  $R_f$  denotes ground fault resistance at the fault point. HMMC constitutes the grounding circuit by the impedance  $Z_{dc}$ , where the impedance  $Z_{dc}$  includes the grounding capacitance  $C_{dc}$  and resistance  $R_{dc}$ .

As shown in Fig.3, if the DC-side of the HMMC is not connected to the ground when the SPG fault occurs, no current flows through the HMMC to the ground. In this situation, the

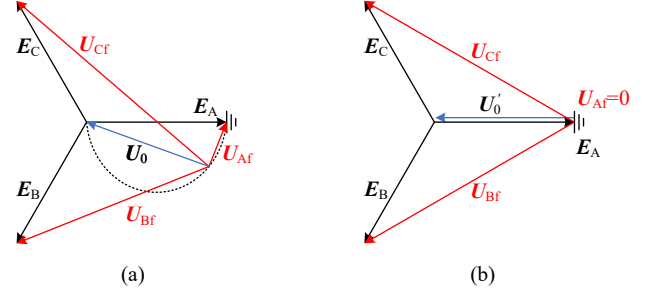


Fig. 5. Three-phase voltage phasors diagram. (a) SPG fault before AGAS, (b) After AGAS.

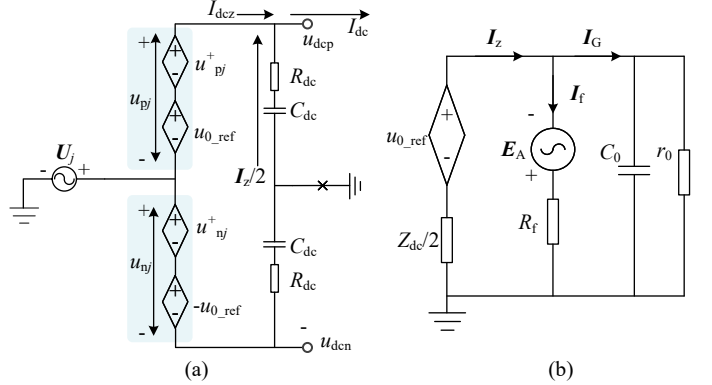


Fig. 6. HMMC equivalent circuit. (a) HMMC single-phase equivalent circuit, (b) Zero-sequence circuit of distribution network based on HMMC with AGAS.

HMMC operates in the FRT mode and blocks the SPG-fault-induced zero-sequence voltage from propagating into the DC network [26]. Without AGAS achieved by the HMMC, the fault current cannot be eliminated at the fault point, which satisfies the equation:

$$I_f = -I_{AG} - I_{BG} - I_{CG} \quad (1)$$

where  $I_{AG}$ ,  $I_{BG}$  and  $I_{CG}$  are the line-to-ground leakage current phasors,  $I_f$  is the ground fault current phasor.

This paper proposes establishing a grounding circuit in HMMC-based AC/DC HDNs to provide a grounding path for the zero-sequence current during AGAS. The circuit includes the capacitance between the positive and negative poles of the DC side of the HMMC. When an SPG fault occurs, the HMMC realizes the function of arc suppression. The HMMC can be considered equivalent to a controllable zero-sequence current source or voltage source used to suppress the ground fault current. A equivalent circuit with the HMMC grounding path is shown in Fig.4.

After an SPG fault occurs in the DN1, a path is formed between the fault point and the earth. Assume that the direction of the current flowing into the earth is positive. A zero-sequence current can be injected to realize the arc suppression. The current equation can be attained as follows:

$$I_{AG} + I_{BG} + I_{CG} + I_f = I_{AZ} + I_{BZ} + I_{CZ} \quad (2)$$

where  $I_{AZ}$ ,  $I_{BZ}$ ,  $I_{CZ}$  are the zero-sequence currents provided by HMMC. Substituting line-to-ground parameters into (2) yields:

$$\begin{aligned} U_A \left( \frac{1}{r_A} + j\omega C_A + \frac{1}{R_f} \right) + U_B \left( \frac{1}{r_B} + j\omega C_B \right) \\ + U_C \left( \frac{1}{r_C} + j\omega C_C \right) - (I_{AZ} + I_{BZ} + I_{CZ}) = 0 \end{aligned} \quad (3)$$

where  $U_j = U_0 + E_j$ ,  $E_A + E_B + E_C = 0$ .

Assume that the DN is symmetrical, i.e.,  $C_A = C_B = C_C = C_0$ , and  $r_A = r_B = r_C = r_0$ . To reduce the fault current  $I_f$  to zero, the zero-sequence current provided by HMMC in (3) can be simplified as:

$$I_Z = I_{AZ} + I_{BZ} + I_{CZ} = 3U_0 \left( \frac{1}{r_0} + j\omega C_0 \right) \quad (4)$$

As shown in (4), when the current provided by the HMMC precisely matches the sum of the ground leakage currents from all feeder circuits, the fault current can be fully compensated. Theoretically, this method can completely compensate the fault current. However, given that the method relies heavily on the accurate measurement of line-to-ground parameters and the precise localization of the fault point, it is difficult to implement in practice. If the voltage at the fault point is suppressed to zero, arc re-ignition conditions will be destroyed, achieving AGAS. Therefore, AGAS with the active control of zero-sequence voltage shows implementation simplicity without of the need for precisely locating the fault point.

According to Kirchhoff's law, current in the zero-sequence net should satisfy (2). Then, (3) can be simplified as follows:

$$3U_0 \left( \frac{1}{r_0} + j\omega C_0 \right) + \frac{(U_0 + E_A)}{R_f} - I_Z = 0 \quad (5)$$

From (4) and (5), it can be seen that if the phase-to-ground voltage at fault phase can be reduced to zero, i.e.,  $U_A = U_0 + E_A = 0$  or  $U_0 = -E_A$ , the total zero-sequence current can be transferred to the HMMC, and the ground fault current reduces to zero, achieving AGAS.

Thus, the HMMC can control  $U_0 = -E_A$  to make the fault phase voltage approach zero. Through zero-sequence voltage regulation using the HMMC, AGAS can be achieved. However, note that using the HMMC for zero-sequence voltage regulation may introduce zero-sequence voltage into the DC network, affecting its operation. Therefore, in the next section, the impact of AGAS on the DC network is discussed and the ZVTS strategy is proposed.

### B. Operation Principle of ZVTS during AGAS

Taking the HMMC topology shown in Fig.2 as an example, assume that the AC-side three-phase voltages ( $U_A$ ,  $U_B$ ,  $U_C$ ) of the HMMC are symmetrical without any zero-sequence component before SPG fault occurrence, which is expressed as follows:

$$\begin{cases} U_A = E_A = U_m \sin(\omega t) \\ U_B = E_B = U_m \sin(\omega t - 2\pi/3) \\ U_C = E_C = U_m \sin(\omega t + 2\pi/3) \end{cases} \quad (6)$$

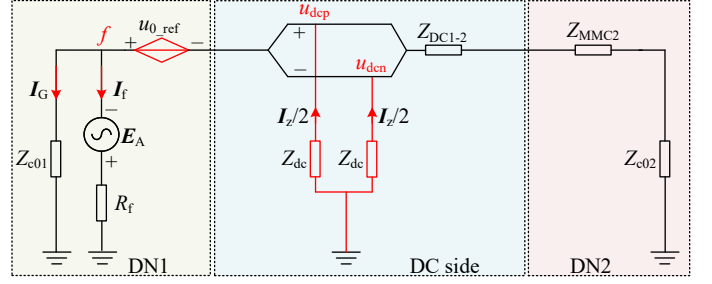


Fig. 7. Zero-sequence equivalent circuit during AGAS without ZVTS.

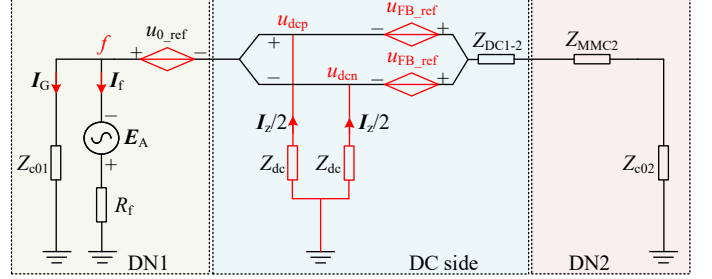


Fig. 8. Zero-sequence equivalent circuit during AGAS with ZVTS.

where  $U_m$  is the voltage magnitude of the supply voltage, and  $\omega$  is its angular frequency. When an SPG fault occurs, the fault phase voltage changes with varying ground resistance  $R_f$ . Assume that an A-phase SPG fault occurs in the feeder of DN1 with a ground resistance  $R_f$ . Then, the three-phase voltage phasor diagram is shown in Fig. 5(a), and the voltage phasor characteristics can be updated according to [35].

Using the symmetrical components method, the three-phase-to-ground voltages after the SPG fault can be decomposed as positive-, negative-, and zero-sequence voltages in (7).

$$\begin{bmatrix} U_f^+ \\ U_f^- \\ U_0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} U_{Af} \\ U_{Bf} \\ U_{Cf} \end{bmatrix} \quad (7)$$

where  $a = e^{j120^\circ}$  is the rotation factor;  $U_f^+$ ,  $U_f^-$  are the positive- and negative-sequence voltages;  $U_{Af}$ ,  $U_{Bf}$ ,  $U_{Cf}$  are the phase-to-ground voltage phasors after the SPG fault. Before and after the SPG fault, the positive- and negative-sequence voltages remain unchanged, and the zero-sequence voltage increases with  $U_0$ , which can be expressed as

$$\begin{cases} U_{Af} = E_A + U_0 \\ U_{Bf} = E_B + U_0 \\ U_{Cf} = E_C + U_0 \end{cases} \quad (8)$$

In the event of an SPG fault with the HMMC not operating in the AGAS mode, there is no zero-sequence voltage in the arm output voltage, i.e.,  $u_{0\_ref} = 0$ . If the DC-side grounding circuit of the HMMC is not closed, no current will flow through the HMMC grounding circuit. The HMMC single-phase equivalent circuit is shown in Fig. 6. The output voltage of the upper- and lower- arms of the HMMC are as follows:

$$\begin{cases} u_{pj} = u_{pj}^+ + u_{0\_ref} = u_{pj}^+ \\ u_{nj} = u_{nj}^+ - u_{0\_ref} = u_{nj}^+ \end{cases} \quad (9)$$

where  $u_{pj}$  and  $u_{nj}$  are the  $j$ -phase upper- and lower-arm output voltages, respectively;  $u_{pj}^+$  and  $u_{nj}^+$  are the positive-sequence upper- and lower-arm voltages, respectively; and  $u_{0\_ref}$  is the zero-sequence reference voltage in the HMMC arm.

As shown in Fig. 6(a), the DC positive and negative pole-to-ground (P2G) voltages can be expressed as follows:

$$\begin{cases} u_{dcp} = u_j + u_{pj}^+ = \frac{U_{dc\_ref}}{2} + u_0 \\ u_{dcn} = u_j - u_{nj}^+ = -\frac{U_{dc\_ref}}{2} + u_0 \end{cases} \quad (10)$$

where  $u_{dcp}$  and  $u_{dcn}$  are the positive and negative pole voltages, respectively;  $u_j$  and  $u_0$  are the instantaneous values of the phase-to-ground voltage and zero-sequence voltage, respectively; and  $U_{dc\_ref}$  is the DC pole-to-pole reference voltage of the HMMC.

Due to  $u_0$  generated by the SPG fault, there is a zero-sequence component in the DC positive and negative P2G voltages. The zero-sequence voltage is transmitted to the DC network and non-fault AC-side of the HDN, potentially deteriorating the safety operation of the non-fault distribution networks.

Notably, the grounding switch device at the DC-side grounding branch is turned off under normal operation without the need for AGAS, and there is no grounding point on the DC-side of the HMMC. When an SPG fault occurs with ground fault resistance, the DC-side grounding circuit is closed for AGAS, providing a path for the zero-sequence current. The HMMC outputs a zero-sequence voltage  $u_{0\_ref}$  in the arm voltage. Consequently, the zero-sequence voltage in DN1 is regulated from  $u_0$  to  $u'_0$ . The fault phase voltage will reduce to zero. This state can be represented by the voltage phasor diagram shown in Fig. 5(b). Then, the three-phase-to-ground voltages after SPG fault occurrence expressed in (8) can be updated as

$$\begin{cases} U_{Af} = E_A + U'_0 \\ U_{Bf} = E_B + U'_0 \\ U_{Cf} = E_C + U'_0 \end{cases} \quad (11)$$

The zero-sequence circuit is shown in Fig. 6(b). When the HMMC operates in the AGAS mode, the zero-sequence voltage is  $U'_0 = -E_A$ , and the fault phase voltage is regulated to zero. The HMMC injects the current  $I_z$ , which is equal to the total line-to-ground current  $I_G$ , resulting in  $I_f$  decreasing to nearly zero.

The HMMC transfers the fault current to the DC-side grounding circuit during AGAS. On the DC side, due to  $I_z$  flowing through the grounding circuit, the DC-side P2G voltage will superpose with a zero-sequence grounding voltage caused by the current  $I_z/2$  and the grounding impedance  $Z_{dc}$ .

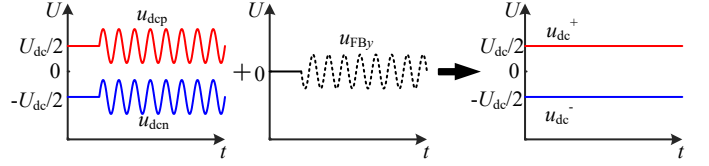


Fig. 9. Operation diagram of FBSM cluster to filter out the zero-sequence voltage.

When the HMMC operates in the AGAS mode, ignoring the voltage drop on the arm inductor, the DC positive and negative voltages in (9) are updated as follows

$$\begin{cases} u_{dcp} = u_j + u_{pj} = U_{dc\_ref}/2 + Z_{dc}i_z/2 \\ u_{dcn} = u_j - u_{nj} = -U_{dc\_ref}/2 + Z_{dc}i_z/2 \end{cases} \quad (12)$$

$$Z_{dc} = R_{dc} + 1/j\omega C_{dc} \quad (13)$$

where  $i_z/2$  is the zero-sequence current flowing to the ground in the DC side per pole and  $Z_{dc}$  is the grounding impedance. Since DC current cannot pass through capacitors, only the AC current  $i_z$  flows through the grounding impedance. The zero-sequence voltage  $\Delta u_{dc0} = Z_{dc}i_z/2$  is the ripple voltage caused by the fault current flowing through the DC-side grounding impedance. The zero-sequence voltage  $\Delta u_{dc0}$  is closely related to  $i_z$  and  $Z_{dc}$ . During AGAS, if the zero-sequence component in the positive and negative P2G voltages is not suppressed, it is transmitted to the DC grid and the non-fault side of the HDN, degrading the power quality.

The zero-sequence equivalent circuit during AGAS is shown in Fig.7, where  $Z_{c01}$  and  $Z_{c02}$  denote the zero-sequence impedances of DN1 and DN2, respectively;  $Z_{MMC2}$  denotes the zero-sequence impedance of HMMC2; and  $Z_{DC1-2}$  denotes the zero-sequence impedance of the DC line.

This article proposes adding an FBSM cluster at the positive and negative ports of the DC side in the HMMC to suppress the zero-sequence voltage being transmitted to the DC grid and the non-fault side of the HDN during AGAS. The zero-sequence equivalent circuit during AGAS with ZVTS is shown in Fig.8.

After SPG fault occurrence in the DN1, the HMMC operates in AGAS mode. The FBSM cluster outputs a zero-sequence voltage, i.e.  $u_{FBy} = -i_z Z_{dc}/2$ , which is reversed to the zero-sequence voltage introduced into DC-side P2G voltage by arc suppression. The operation diagram of FBSM cluster to filter out the zero-sequence voltage is shown in Fig.9. In this process, the DC-side current  $I_{dc}$  flowing through the FBSM cluster is direct current, and the FBSM cluster only outputs zero-sequence voltage. The average power  $\bar{P}$  produced or absorbed by the FBSM cluster in one fundamental period (20 ms) is equal to zero, as shown in (14). Thus, the FBSM cluster can maintain the SM capacitor voltage balance.

$$\bar{P} = \frac{\omega}{2\pi} \int_0^{2\pi/\omega} -\frac{I_{dc} \cdot i_z Z_{dc}}{2} dt = 0 \quad (14)$$

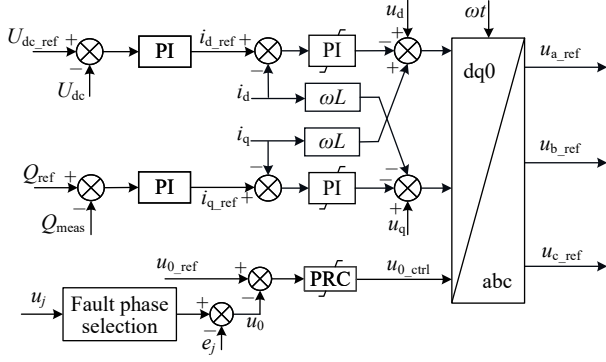


Fig. 10. Block diagram of the HMMC  $U_{dc}Q$  control with AGAS.

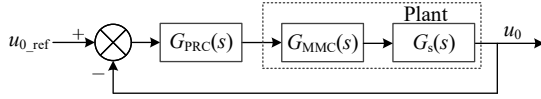


Fig. 11. Block diagram of the AGAS control of the HMMC.

#### IV. HMMC CONTROL STRATEGY

##### A. AGAS Control Method

The AGAS control method of the HMMC aims to achieve arc suppression by actively regulating the neutral-to-ground voltage to track the inverse of the supply power voltage of the fault phase. Based on the analysis of the HDN with the HMMC presented earlier, the dual loop control achieved by controlling the zero-axis component in the dq0 reference frame is shown in Fig.10. After selecting the fault phase, the HMMC outputs a zero-sequence voltage such that the fault phase voltage can be reduced to near zero. Due to the zero-sequence voltage being AC component, it is difficult for traditional PI controllers to track the signal with zero error. Notice that the proportional resonant controller (PRC) can effectively track AC signals at specific frequencies, ensuring accurate tracking and control without errors. Thus, this paper proposes to adopt the AGAS control method based on the PRC. The transfer function of PRC is as follows:

$$G_{PR}(s) = k_p + \frac{2K_r\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \quad (15)$$

where  $k_p$  is the proportional coefficient,  $K_r$  is the resonance coefficient,  $\omega_c$  is the bandpass frequency,  $\omega_0$  is the resonance frequency, and  $s$  is the Laplace operator.

The block diagram of the AGAS control of the HMMC is shown in Fig.11, where  $u_{0\_ref}$  is the zero-sequence reference voltage controlled by the HMMC.  $G_s(s) = 1/(3/r_0 + 3sC_0 + 1/R_f)$  represents the transfer function of the equivalent impedance for the AC-side distribution network.  $G_{MMC}(s)$  represents the transfer function of the HMMC, including the current loop and modulation. Assume that the current controller can track the reference value accurately. The transfer function of  $G_{MMC}(s)$  can be simplified as  $G_{MMC}(s) = e^{-sT_s} \approx (1 - 0.5sT_s)/(1 + 0.5sT_s)$ , considering the sampling and calculation delay. According to Fig.11, the closed-loop

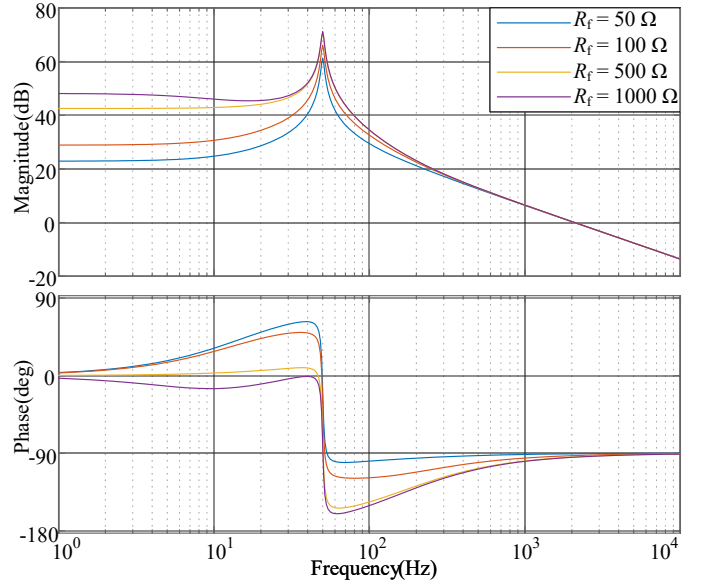


Fig. 12. Bode diagram of the open-loop transfer function with different ground fault resistances.

transfer function of zero-sequence voltage control can be written as

$$G_{AS}(s) = \frac{G_{PR}(s)G_{MMC}(s)G_s(s)}{1 + G_{PR}(s)G_{MMC}(s)G_s(s)} \quad (16)$$

Under different ground fault resistances, the Bode diagram of the open-loop transfer function is shown in Fig.12. The HDN parameters  $r_0$  are 30000Ω,  $C_0$  is 7.14 μF, and the control parameters of the PRC are  $K_r = 24.28$ ,  $k_p = 0.28$ ,  $\omega_c = 6.28$ , and  $\omega_0 = 314$ . At the resonance frequency, the open-loop transfer function has a relatively high gain. Thus, it is proved that the proposed control method can effectively achieve AGAS for different ground fault resistances. With the fault resistance  $R_f = 1000 \Omega$ , it can be seen that the gain is higher under high-impedance, and the arc suppression performance can be better.

##### B. ZVTS Control Method

Previous research [26] has shown that an MMC can achieve the FRT and ZVTS abilities when an SPG fault occurs. However, during AGAS control, the HMMC is already engaged in zero-sequence voltage regulation, which conflicts with the ZVTS operation and hence cannot be realized simultaneously. Hence, ZVTS control should be achieved by the FBSM cluster. Therefore, the ZVTS control of the HMMC aims to suppress the zero-sequence voltage transmitting to the DC grid and the non-fault side of the HDN during AGAS, and balance the cluster submodule capacitor voltages.

During normal operation of the FBSM cluster, voltage balancing is performed in the SM only to ensure its normal operation. On the DC side, since  $I_{dc}$  is direct current, the FBSM cluster can maintain voltage balance by charging and discharging its capacitors, ensuring voltage stability. During AGAS, the fault current is transferred to the DC side and there is a zero-sequence voltage ripple  $\Delta u_{dc0}$  in the P2G

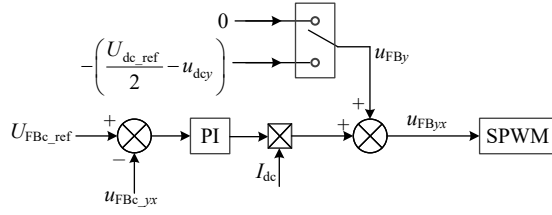


Fig. 13. Control diagram of the  $y$ -pole of FBSM cluster with ZVTS and individual submodule capacitor voltage balancing control.

voltage. The FBSM cluster should be controlled to output a zero-sequence voltage, which is reversed to the zero-sequence voltage ripple  $\Delta u_{dc0}$  introduced into DC-side P2G voltage by AGAS, effectively realizing ZVTS. The output voltage of the positive or negative pole  $u_{FB_y}$  of the FBSM cluster can be obtained as:

$$u_{FB_y} = - \left( \frac{U_{dc\_ref}}{2} - u_{dc0} \right) = -\Delta u_{dc0} = -\frac{i_z}{2} Z_{dc} \quad (17)$$

where the subscript  $y$  denotes the positive pole ( $y = p$ ) or negative pole ( $y = n$ ) of the FBSM cluster.

The zero-sequence voltage in the positive and negative ports on the DC side should be measured to facilitate signal acquisition and control implementation. ZVTS control and individual submodule capacitor voltage balancing control in the  $y$ -pole of the FBSM cluster is shown in Fig.13, where  $u_{FBc\_yx}$  is the  $x$ th submodule capacitor voltage of  $y$ -pole of the FBSM cluster,  $x = 1 \dots X$ ,  $U_{FBc\_ref}$  is the FBSM capacitor reference voltage, and  $u_{FB_yx}$  is  $x$ th submodule output voltage of the  $y$ -pole of the FBSM cluster. Since the FBSM cluster on the DC side does not produce or absorb active power according to (14), the capacitor voltage remains at the rated value with individual submodule voltage balancing control. A feedback controller of individual balancing control provides  $\Delta u_{FBc\_yx}$  from the error between the reference  $U_{FBc\_ref}$  and actual  $x$ th submodule capacitor voltage  $u_{FBc\_yx}$  as follows.

$$\Delta u_{FBc\_yx} = G_{PI} (U_{FBc\_ref} - u_{FBc\_yx}) \quad (18)$$

where  $G_{PI}$  is a proportional-integral controller. Thus, the FBSM cluster can maintain its capacitor voltage and achieve ZVTS.

### C. HMMC Comprehensive Control Strategy

The flowchart of the proposed fault control strategy based on the HMMC is shown in Fig.14. Initially, the HMMC operates in  $U_{dc}Q$  or  $PQ$  control mode, and the zero-sequence voltage is detected in real-time. After detecting the fault phase [36], the HMMC detects the SPG fault and identifies the fault phase. Otherwise, the HMMC operates in the normal control mode. Then, the HMMC operates in the AGAS control to reduce the fault phase voltage to zero, thereby achieving AGAS. Finally, the FBSM cluster outputs a zero-sequence voltage, which is reversed to the zero-sequence voltage ripple  $\Delta u_{dc0}$ .

With the implemented flowchart of the fault control strategy in Fig.14, the comprehensive control strategy of the HMMC

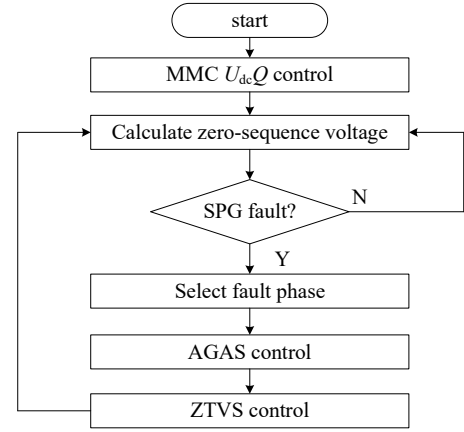


Fig. 14. Flowchart of the proposed fault control strategy.

is presented in Fig.15. The HMMC in DN1 adopts a  $U_{dc}Q$  control mode in  $dq$  axis and realizes AGAS in the zero-axis. The HMMC configures the negative-sequence current controller (NSCC) to ensure that there is no negative-sequence current in the three-phase currents. Additionally, a circulating current suppression controller (CCSC) is also used to eliminate the undesired circulating currents. Due to an SPG fault and AGAS control, the asymmetrical three-phase voltages can lead to an imbalance in three-phase submodule capacitor voltages. The control strategy presented herein adopts a three-layer capacitor voltage balancing control, including leg balancing, arm balancing, and intra-arm balancing control. It ensures that each SM capacitor voltage operates at the rated value during AGAS. Moreover, the FBSM cluster at the DC-side of the HMMC only realizes voltage balancing control during normal operation. After SPG fault occurrence and during AGAS, the FBSM cluster performs ZVTS to inhibit the zero-sequence voltage from entering the DC side. If the HMMC in DN1 adopts the  $U_{dc}Q$  control, the HMMC in DN2 should operate in the  $PQ$  control and realize the power delivery.

### D. Submodule Configuration Principles of the HMMC

In the model analysis of this paper, taking the 10 kV AC grid and the  $\pm 10$  kV DC grid as example, define the voltage modulation ratio  $M$  as [37]:

$$M = \frac{2U_m}{U_{dc\_ref}} \approx 0.82 \quad (19)$$

During the steady-state operation of the distribution network, the MMC does not require additional sub-modules because the three-phase voltages remain symmetrical. During an SPG fault, if the MMC is capable of AGAS control, it is necessary to output negative voltages of the upper- and lower-arms with consideration of the HBSMs and FBSMs ratio configuration within the arm, which is determined according to the maximum and minimum values of the arm output voltages.

During AGAS control, ignoring the voltage drop on the arm inductor, the arm output voltage is as follows:

$$\begin{cases} u_{pj} = U_{dc\_ref}/2 + Z_{dc}i_z/2 - u_j \\ u_{nj} = U_{dc\_ref}/2 - Z_{dc}i_z/2 + u_j \end{cases} \quad (20)$$

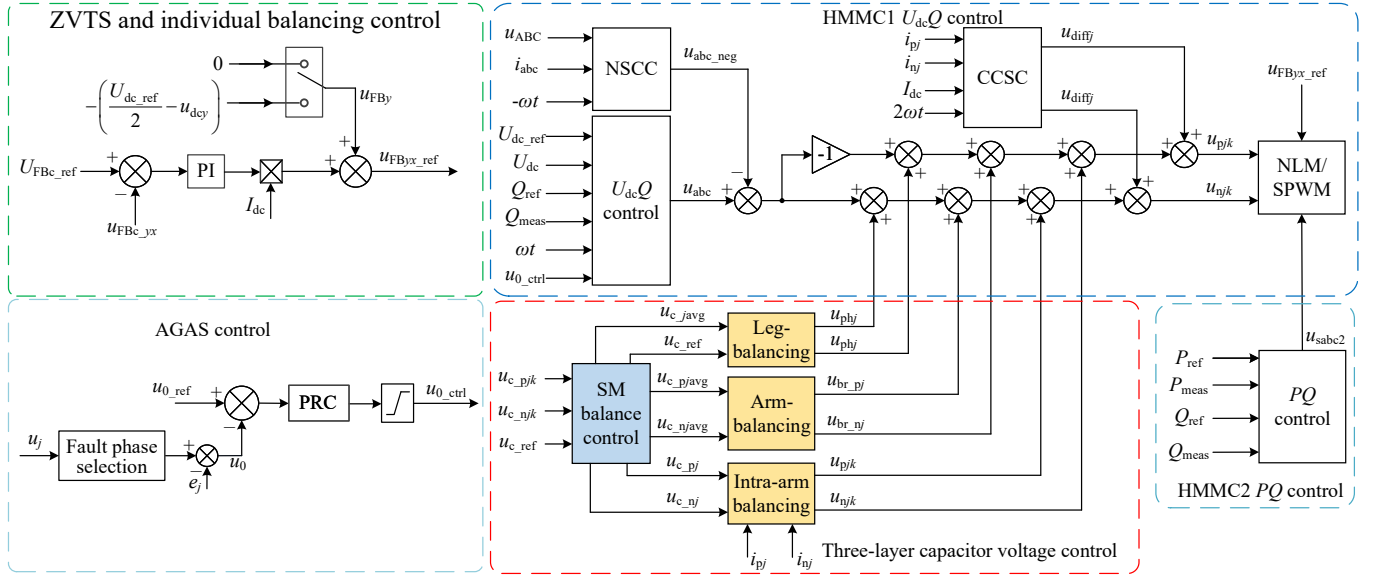


Fig. 15. HMMC comprehensive control strategy.

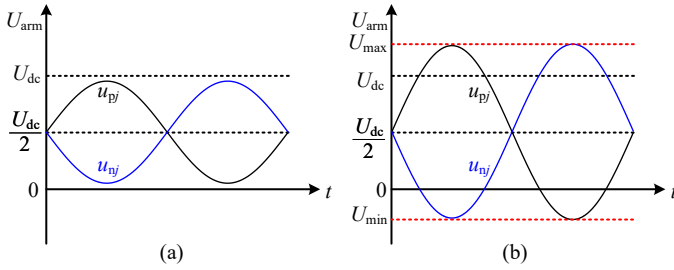


Fig. 16. Schematic diagram of the arm output voltage waveforms in the non-fault phase: (a) normal operation condition and (b) SPG fault with AGAS.

During AGAS, the three-phase voltages are no longer symmetrical. Moreover, the voltage of the fault phase is zero, and the voltage of the non-fault phase rises to the line voltage. This will inevitably lead to an imbalance in the output voltage of each arm. According to (19) and (20), the maximum and minimum output voltages of the non-fault phase arm can be expressed as:

$$\begin{cases} U_{\max} = \frac{1 + \sqrt{3}M}{2} U_{dc\_ref} + \Delta U_{dc0\_max} \\ U_{\min} = \frac{1 - \sqrt{3}M}{2} U_{dc\_ref} - \Delta U_{dc0\_max} \end{cases} \quad (21)$$

where  $\Delta U_{dc0\_max}$  represents the maximum amplitude of the zero-sequence voltage ripple  $\Delta U_{dc0}$  introduced into the DC-side P2G voltage via AGAS. The maximum and minimum output voltages of the non-fault phase arm are shown in Fig. 16.

If the number of HBSMs in each arm of the traditional three-phase MMC is  $n$ , the SM capacitor reference voltage  $U_{c\_ref}$  of MMC arm is obtained as:

$$U_{c\_ref} = \frac{U_{dc\_ref}}{2n} \quad (22)$$

TABLE I  
AC/DC HDN AND HMMC PARAMETERS

| Parameters                                | Value                       |
|-------------------------------------------|-----------------------------|
| Line voltage of AC DN                     | 10 kV                       |
| Grid frequency                            | 50 Hz                       |
| Isolation Yg-d transformer                | 110 kV/10 kV                |
| Phase-to-ground leakage resistance $r_0$  | 30,000 $\Omega$             |
| Phase-to-ground leakage capacitance $c_0$ | 7.14 $\mu F$                |
| Ground fault resistance                   | 50, 100, 500, 1000 $\Omega$ |
| DC voltage of DC DN                       | $\pm 10$ kV                 |
| DC grounding impedance $Z_{dc}$           | 1000 $\mu F$ , 100 $\Omega$ |
| DC load                                   | 3.5 MW                      |
| SM number per arm                         | 28                          |
| HBSM: FBSM                                | 20:8                        |
| Number of FBSM cluster                    | 6                           |
| Arm inductance                            | 15 mH                       |
| SM voltage                                | 1000 V                      |
| SM capacitance                            | 4 mF                        |

To satisfy the output voltage requirements in (21) for AGAS, the total number of SMs (including HBSMs and FBSMs) within the arm of the HMMC must be configured as:

$$n + m \geq \frac{U_{\max}}{U_{c\_ref}} \quad (23)$$

where  $n$  is the number of HBSMs and  $m$  is the number of FBSMs.

Besides, to guarantee the negative voltage output capability in (21) of the HMMC arm during AGAS, the number of FBSMs must be configured as:

$$m \geq \frac{|U_{\min}|}{U_{c\_ref}} \quad (24)$$

The SM configuration principles of the HMMC described in (20)-(24) show that if the zero-sequence voltage ripple on the DC side is neglected, then there should be at least  $1.21n$  SMs within the arm, among which  $0.21n$  should be FBSMs. If the zero-sequence voltage ripple on the DC side is considered, its voltage magnitude is related to the total

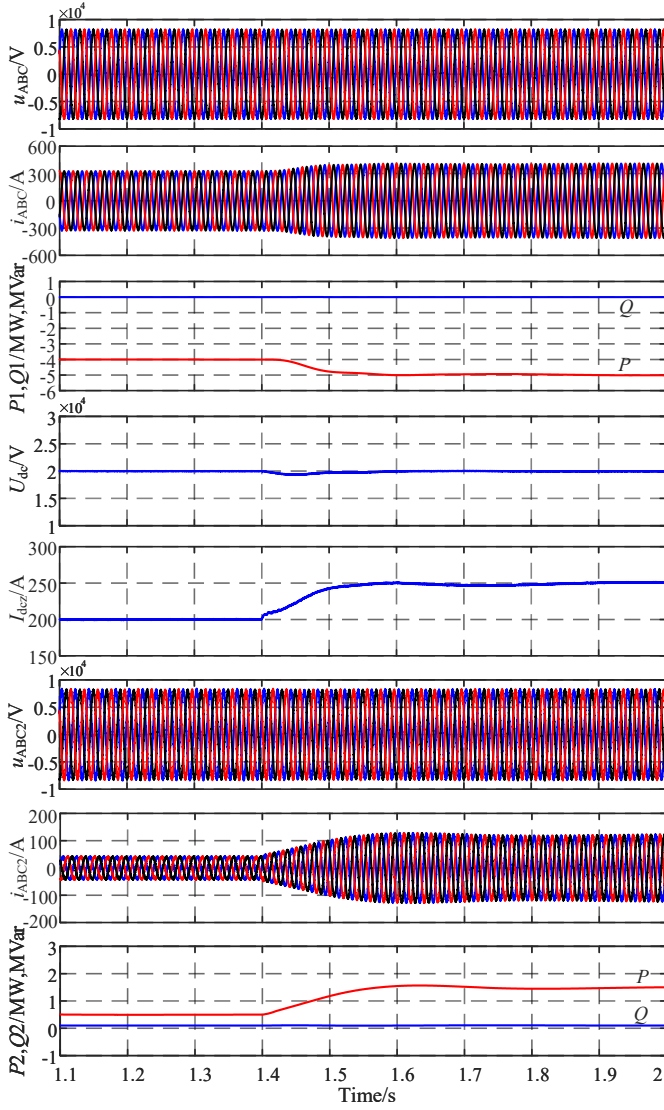


Fig. 17. Simulation waveforms of AC/DC HDN with HMMC under normal operation.

ground capacitance of AC feeders and the impedance of the DC-side grounding branch. It should be designed based on various grid parameters. Herein, the maximum amplitude of the zero-sequence voltage ripple at DC side is considered up to 3 kV. In this paper, the capacitor voltage of SM is chosen as  $U_{c\_ref} = 1$  kV. Therefore, a total of 28 sub-modules consisting of 20 HBSMs and 8 FBSMs were configured in each arm of the proposed HMMC.

The purpose of employing the FBSM cluster was to prevent the zero-sequence voltage from entering into the DC grid during AGAS. As shown in (17), the FBSM cluster has to output a zero-sequence voltage, which is opposite to that of zero-sequence voltage introduced by AGAS. Then, the number of SMs in the FBSM cluster to meet the ZVTS requirements can be determined as follows:

$$X \geq \frac{\Delta U_{dc0\_max}}{U_{FBC\_ref}} \quad (25)$$

where  $X$  is the number of FBSMs, and  $U_{FBC\_ref}$  is the capacitor

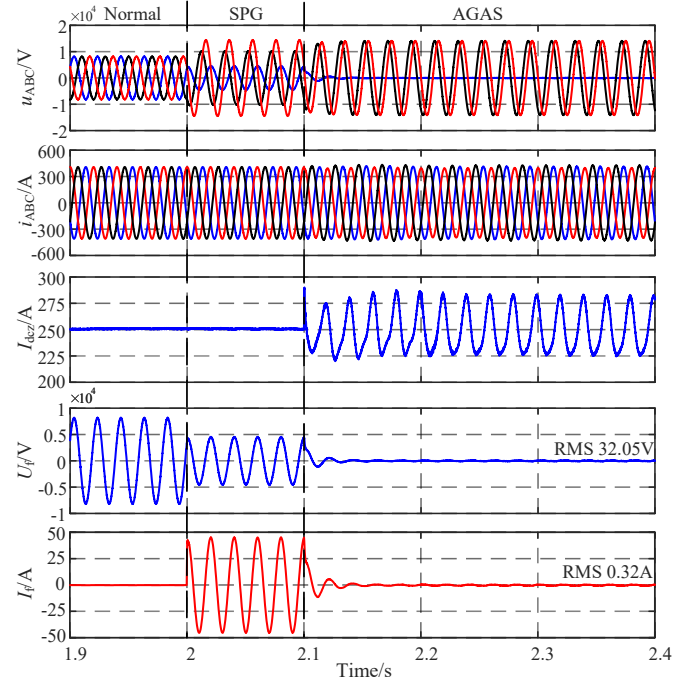


Fig. 18. Simulation waveforms of an SPG fault with/without AGAS control.

reference voltage of the FBSM cluster.

## V. SIMULATION RESULTS

### A. Simulation Model

A 10 kV AC/DC HDN model with HMMC interconnection was constructed using MATLAB/Simulink to verify the feasibility of the HMMC with AGAS and ZVTS capabilities, as shown in Fig.1. Each DN contained transmission lines and loads. There were three feeders in DN1, and DN2. An A-phase SPG fault was set at the feeder of DN1. The specific simulation parameters of the AC/DC HDN and HMMC are presented in Table. I.

### B. HMMC Normal Operation and Power Delivery

In the simulation model, when the system operated in a steady state, the HMMC in DN1 output 4 MW of active power, out of which 3.5 MW was supplied to the DC load and 0.5 MW was transferred to DN2 via HMMC2. At 1.4 s, HMMC2 stepped up its power transfer to DN2 from 0.5 to 1.5 MW. The system quickly reached a new steady state operation. As shown in Fig. 17, during the output power change, the system's three-phase voltages and DC side voltage remained constant, while the output current tracked with the power variation.

### C. AGAS and Fault Current Suppression

The SPG fault was set at the end of a feeder at DN1 (in Fig. 1) at  $t=2$  s with a ground fault resistance of  $100 \Omega$ . After the SPG fault occurred, the A-phase voltage decreased and the voltages of the other two phases increased, resulting in asymmetrical three-phase voltages, as shown in Fig. 18. Due to

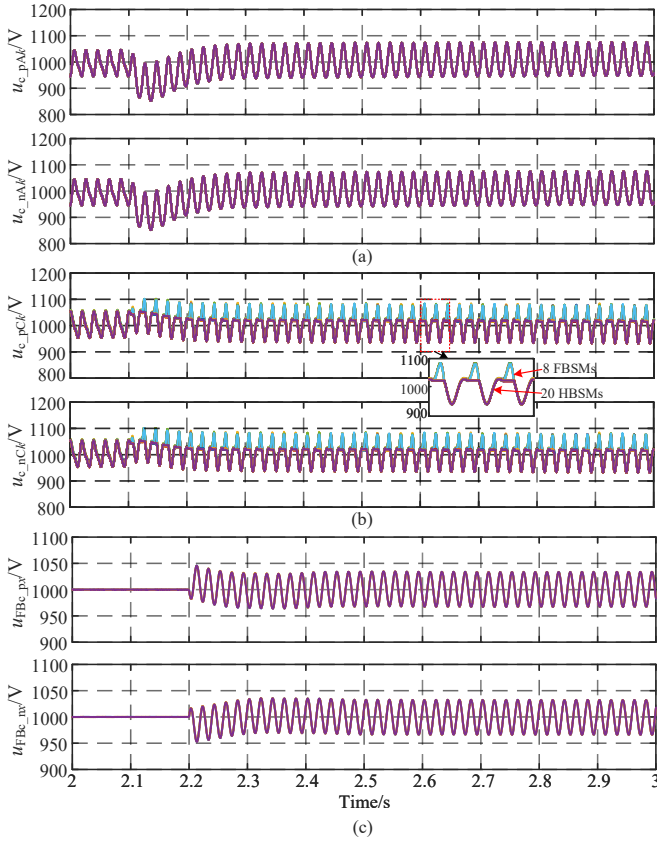


Fig. 19. Simulation waveforms of submodule capacitor voltage after activating AGAS and ZVTS control: (a) the fault phase upper- and lower- arm capacitor voltage; (b) the non-fault phase upper- and lower- arm capacitor voltage; (c) the FBSM cluster capacitor voltage.

the HMMC configured with  $U_{dc}Q$  control, NSCC, and CCSC, as well as three-layer capacitor voltage balancing control, the HMMC can output a three-phase symmetrical currents in the AC-side during 2.0 s-2.1 s. Therefore, the proposed HMMC with control strategy can realize SPG FRT, preventing the AC-side fault from affecting the DC grid. However, during 2.0 s-2.1 s without AGAS control, the ground fault residual current  $I_f$  at fault point was large, as shown in Fig. 18.

The DC-side grounding circuit of the HMMC was put into operation at 2.1 s to reduce the ground fault residual current  $I_f$  caused by the SPG fault. Then, the AGAS mode was activated, transferring the ground fault current to the ground through the grounding circuit constructed on the DC side of the HMMC. As shown in Fig. 18, after the AGAS control was activated, the fault point voltage  $U_f$  was suppressed, and the ground fault residual current  $I_f$  decreased to nearly zero. Note that the three-phase current included the zero-sequence current for arc suppression, resulting in the asymmetry of the AC-side three-phase currents of the HMMC. Furthermore, during the AGAS period, the DC-side current included the arc suppression current flowing through the grounding circuit.

When the HMMC activated the AGAS control, the three-phase-to-ground voltages and currents were asymmetric, affecting the safe operation of the SM capacitor voltage. The

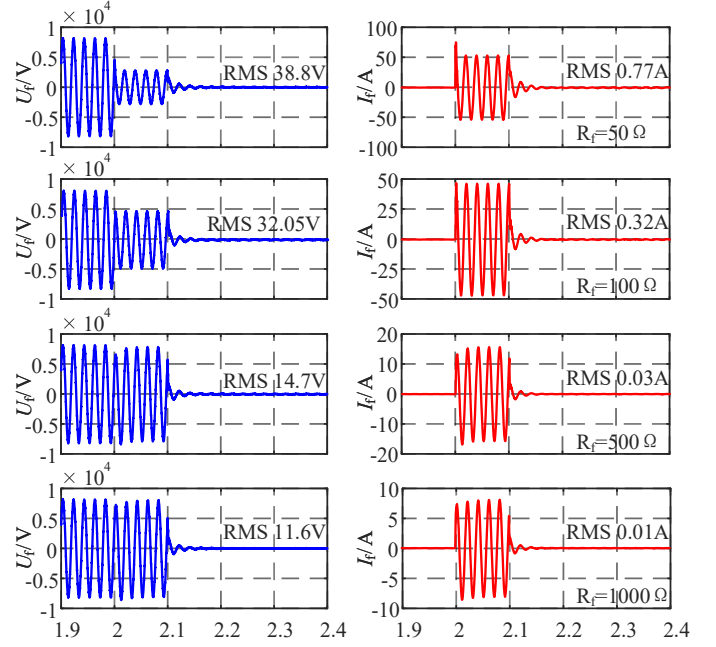


Fig. 20. Simulation waveforms of AGAS in different ground resistances  $R_f$ .

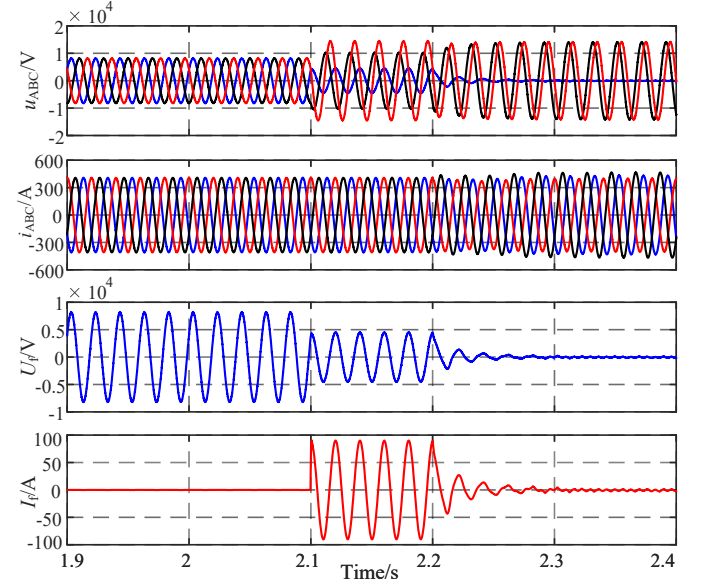


Fig. 21. Simulation waveforms of the SPG fault with AGAS control when the fault current is about 80A.

three-layer voltage balancing control enabled the HMMC to ensure that the three-phase upper- and lower-arm SM capacitor voltages were maintained at their rated values, as shown in Fig. 19, ensuring the safe operation of the HMMC. As shown in Fig.19(a), the fault phase arm does not output the negative voltage, the function of FBSMs is equal to the HBSMs. The capacitor voltage curves of 8 FBSMs were similar to that of 20 HBSMs. However, because the non-fault phase-to-ground voltage increased to the line voltage during arc suppression, the non-fault phase arm output a negative voltage according to (21). At this time, the negative voltage was output by FBSMs

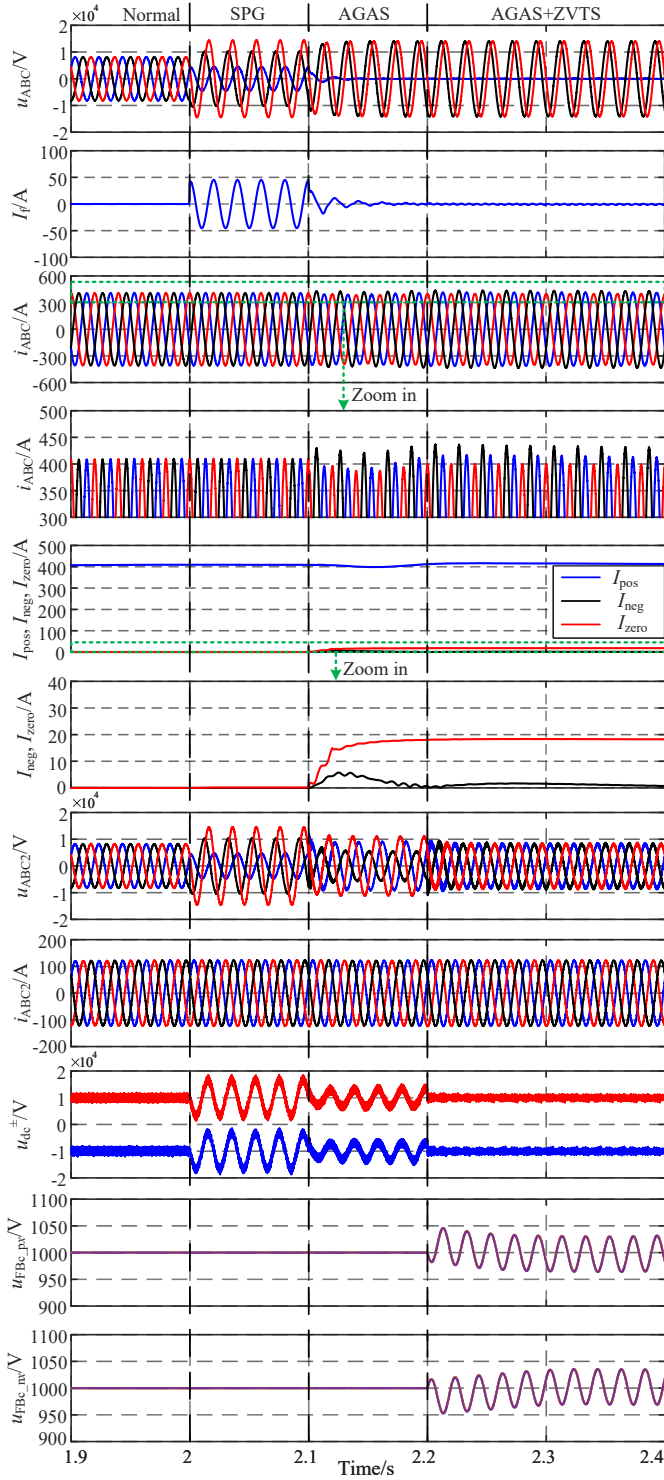


Fig. 22. Simulation waveforms of AGAS with/without ZVTS control.

while the HBSMs were bypassed. Then, the capacitor voltages of FBSMs and HBSMs were different and kept in balance with intra-arm individual balancing control during arc suppression, as shown in Fig. 19(b). During the normal operation, the FBSM cluster only maintained the voltage balance. During ZVTS, the FBSM cluster output a zero-sequence voltage, which is opposed to that of zero-sequence voltage introduced

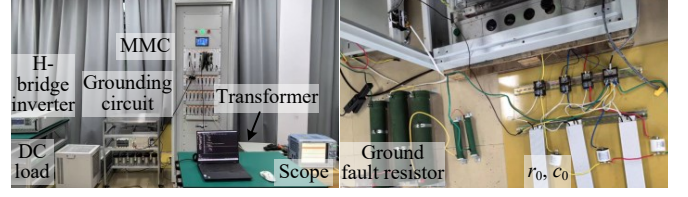


Fig. 23. Photograph of the HMMC experimental setup.

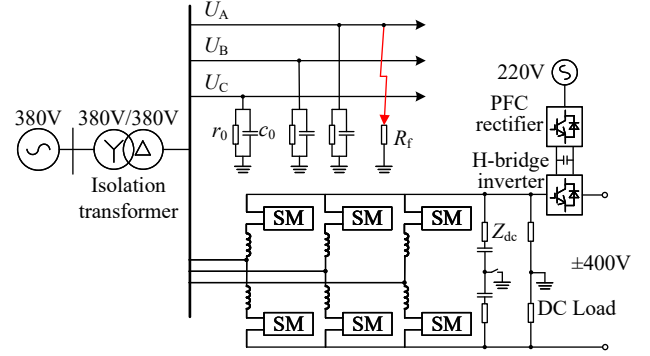


Fig. 24. Schematic wiring diagram of the HMMC experimental setup.

by arc suppression. This caused the generation of ripples observed in the capacitor voltages of the FBSM cluster. With the balancing control method in Fig. 13, the FBSM cluster can maintain voltage balance by charging and discharging submodule capacitors, ensuring voltage stability, as shown in Fig. 19(c).

Fig. 20 shows the simulation waveforms of AGAS in different values of ground fault resistances  $R_f$  (50  $\Omega$ , 100  $\Omega$ , 500  $\Omega$ , 1,000  $\Omega$ ), further verifying the AGAS control performance of the HMMC. During 2.0 to 2.1 s, the SPG fault occurred without AGAS, confirming that the fault phase voltage and current cannot be suppressed. After 2.1 s, the fault phase-to-ground voltage and current were fully regulated within a few microseconds, and the residual voltages and currents at the fault point were suppressed to within 40 V (RMS) and 0.8 A (RMS). The suppression performance on low- and high-impedance faults was effective, contributing to extinguishing the arc.

If the phase-to-ground leakage capacitance was changed, the fault current changed. In this case, the fault current was approximately 80 A. As shown in Fig. 21, the proposed method remained applicable for arc suppression in scenarios where the ground capacitance was increased.

The simulation results demonstrated that after the activation of the AGAS control, the residual voltage of the fault phase decreased significantly, the voltage of the non-fault phase increased to the line voltage, and fault current decreased to nearly zero, confirming effective AGAS achieved using the HMMC.

#### D. Simulation Results of ZVTS

During normal operation in a steady state, DN1 and DN2 generated symmetrical three-phase voltages. The SPG fault

TABLE II  
EXPERIMENTAL PARAMETERS

| Parameters                                | Value                          |
|-------------------------------------------|--------------------------------|
| Line voltage of AC DN                     | 380 V                          |
| Grid frequency                            | 50 Hz                          |
| Isolation Yd transformer                  | 380 V/380 V 12 KVA             |
| Phase-to-ground leakage resistance $r_0$  | 300 $\Omega$                   |
| Phase-to-ground leakage capacitance $c_0$ | 20 $\mu\text{F}$               |
| Ground fault resistance                   | 15, 30, 90, 190 $\Omega$       |
| DC voltage of DC DN                       | $\pm 10$ kV                    |
| DC ground impedance $Z_{dc}$              | 500 $\mu\text{F}$ , 1 $\Omega$ |
| DC load                                   | 2 kW                           |
| SM number per arm                         | 4                              |
| Number of FBSM cluster                    | 1                              |
| Arm inductance                            | 7.5 mH                         |
| SM voltage                                | 250 V                          |
| SM capacitance                            | 2000 $\mu\text{F}$             |
| Switching frequency                       | 2.5 kHz                        |

and AGAS made the three-phase voltage asymmetrical and transferred a zero-sequence voltage through the HMMC to the DC side. The zero-sequence voltage caused fluctuations in the positive and negative P2G voltages of the DC side without ZVTS, transferring them to the DN2. This further led to asymmetrical three-phase voltages in DN2, adversely impacting the HDN.

Fig. 22 shows the waveforms of AGAS with and without ZVTS control. After the SPG fault occurred at 2 s, the zero-sequence voltage was generated in the HDN. The zero-sequence voltage was then transferred to the DC side through the HMMC and then to DN2 without ZVTS control, resulting in the generation of asymmetric three-phase voltage. In the time interval 2.0-2.1 s, when a fault occurred on the AC side but AGAS control was not yet activated, there was no zero-sequence current flowing. During this period, the HMMC delivered active power with only a positive-sequence current of approximately 408 A. After activating AGAS control at 2.1s, zero-sequence current was transferred to the DC-side grounding circuit. Consequently, the fault current was significantly suppressed. During this period, the positive-sequence current  $I_{pos}$  remained constant, negative-sequence current  $I_{neg}$  was maintained at zero, and zero-sequence current  $I_{zero}$  increased to 18.16 A. This confirms the transfer of zero-sequence current to the DC-side grounding path, as evidenced by a noticeable increase in the zero-sequence component. The zero-sequence voltage was still transferred to the DC grid and adversely affected non-fault DN2 side, as shown in Fig. 22. After 2.2 s, ZVTS control was put into operation by activating the FBSM cluster. The FBSM cluster was controlled to output a voltage of the same amplitude and in the opposite direction to the zero-sequence voltage at the DC side, thereby effectively realizing the ZVTS. As shown in Fig. 22, the zero-sequence voltage transmission to the DN2 can be blocked. The capacitor voltage of FBSM cluster fluctuated within a range of  $\pm 50$  V, and was maintained close to the rated value.

## VI. EXPERIMENTAL RESULTS

A scaled-down prototype of the HMMC and its experimental platform were built to validate the effectiveness and

TABLE III  
EXPERIMENTAL RESULTS WITH AND WITHOUT AGAS

| Fault Resistance<br>$R_f/\Omega$ | Fault voltage $U_A/\text{V RMS}$ |       | Fault current $I_f/\text{A RMS}$ |        |
|----------------------------------|----------------------------------|-------|----------------------------------|--------|
|                                  | W/O                              | With  | W/O                              | With   |
| 15                               | 100.4 V                          | 4.0 V | 6.6 A                            | 0.28 A |
| 30                               | 108.2 V                          | 4.3 V | 3.6 A                            | 0.14 A |
| 90                               | 165.5 V                          | 4.2 V | 1.9 A                            | 0.04 A |
| 190                              | 199.3 V                          | 4.2 V | 1.0 A                            | 0.02 A |

feasibility of the proposed HMMC with AGAS and ZVTS abilities. Figures 23 and 24 present the photograph and the schematic wiring diagram of the HMMC experimental setup, respectively. The ungrounded 380 V AC distribution network was formed by an isolation Yd transformer with a capacity of 12 kVA. The leakage capacitance  $c_0$  and resistance  $r_0$  were emulated by three 20  $\mu\text{F}$  capacitors and 300  $\Omega$  resistors. The neutral point of the three-phase capacitors was configured as the ground. The proposed HMMC formed the grounded  $\pm 400$  V DC distribution network. The grounding point on the DC side was connected with the neutral point of the three-phase capacitors. Each arm of HMMC was formed by a stack of four submodules and one arm inductor. The DC-side grounding circuit was constructed with a capacitor, resistor, and switch. The DC-side cluster was configured with one H-bridge inverter. The DC-link capacitor voltage of the H-bridge inverter was supplied by a rectifier with power factor correction function. The H-bridge inverter acted as FBSM cluster and output voltage for implementing ZVTS control, thus filtering out the zero-sequence ripple voltage caused by AGAS, as described in our proposed scheme. Due to limitations of our experimental setup, the H-bridge inverter's role was focused solely on demonstrating ripple suppression. The controller was implemented using Xilinx ZYNQ-7020. The detailed parameters used in the experimental setup were listed in Table II. In the experimental test, each arm of the HMMC had four FBSMs. Therefore, we set the SM voltage to 250 V to meet the target maximum output of each arm as discussed in section IV.D while accommodating hardware constraints. AVAS was then achieved without causing overmodulation. Notably, an SM voltage of 250 V achieved an effect similar to that achieved when the number of SMs is increased (e.g., using five SMs with a voltage of 200 V).

The performance of the proposed control method in experiments under an A-phase SPG fault with different  $R_f$  values is shown in Fig. 25. In the normal operation,  $U_A$ ,  $U_B$ , and  $U_C$  remained symmetrical, and  $U_0$  was zero. When the SPG fault occurred in the A-phase, the fault phase voltage decreased, and non-fault phase voltage increased. The fault current flowed into ground through ground fault resistance  $R_f$ . The residual voltage was different for different ground fault resistance  $R_f$  before activating the AGAS control. After AGAS was activated, the fault-phase voltage was reduced to nearly zero and the zero-sequence voltage increased to  $-E_A$ . As the  $R_f$  values were different, the experimental results of fault phase voltage and residual currents with and without AGAS control were presented in the Table. III. Even for different ground fault resistances, AGAS reduced the residual voltage and fault

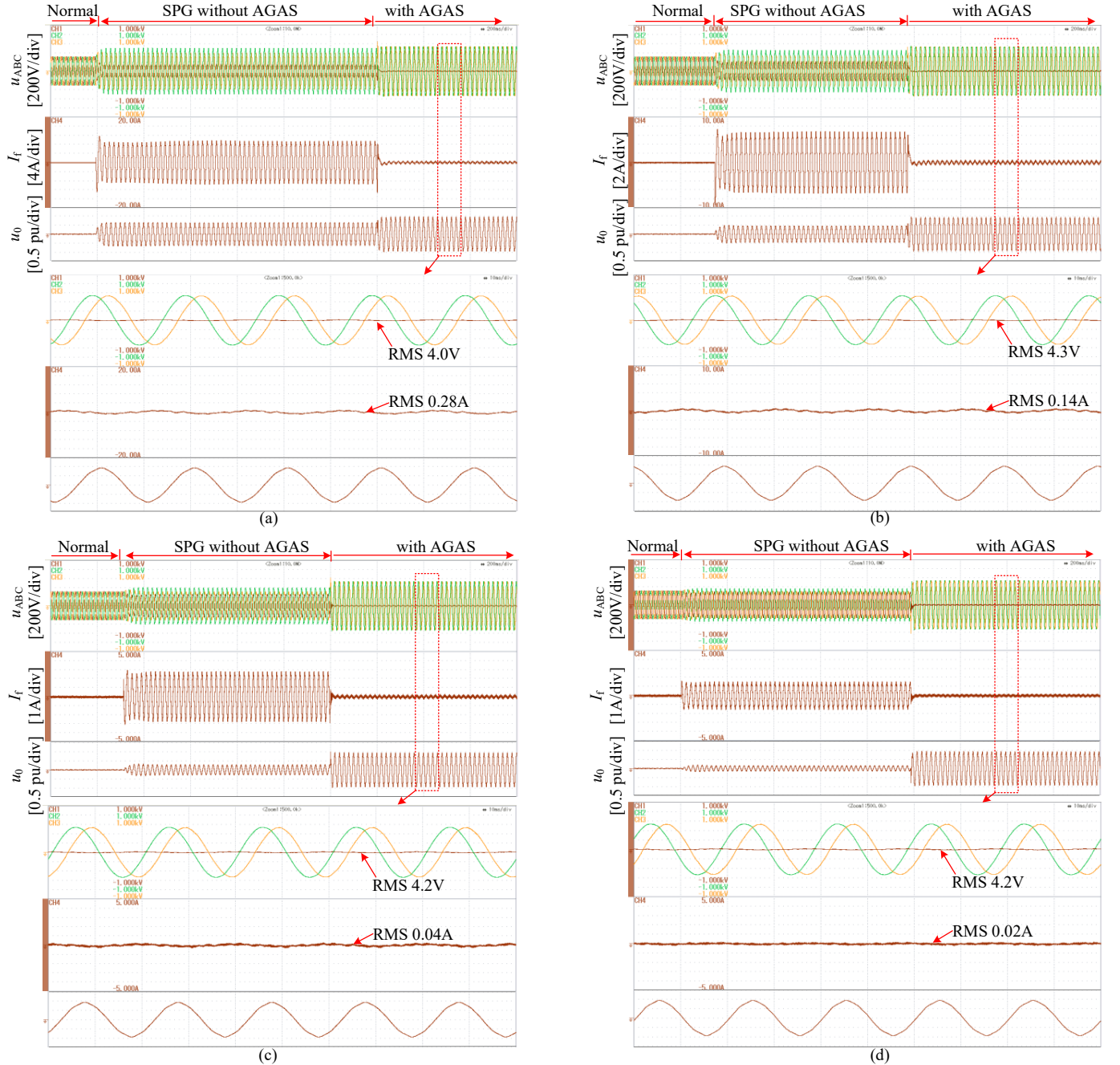


Fig. 25. Experimental results with/without AGAS control: (a) A-phase fault and  $R_f = 15 \Omega$ ; (b) A-phase fault and  $R_f = 30 \Omega$ ; (c) A-phase fault and  $R_f = 90 \Omega$ ; (d) A-phase fault and  $R_f = 190 \Omega$ .

current to nearly zero. Thus, the experimental results indicated that the proposed AGAS method is applicable for different ground fault resistances.

We set an SPG fault in the A-phase with a ground fault resistance of  $190 \Omega$  to verify AGAS and ZVTS control. When AGAS was activated, the fault current was transferred to the DC-side grounding circuit, resulting in the zero-sequence voltage superposing to the P2G voltage at DC grounding circuit. The experimental results of P2G voltage with or without ZVTS control during AGAS are shown in Fig. 26. The DC-side positive P2G voltage before the FBSM cluster always had a large zero-sequence voltage ripple (about 50V)

during AGAS. When an H-bridge cluster on the DC side was controlled to output a voltage with polarity opposite to that of the zero-sequence voltage ripple, this zero-sequence voltage ripple in the DC-side P2G voltage was suppressed to about 8 V by the FBSM cluster after activating ZVTS, improving the power quality of the DC network during AGAS.

## VII. ECONOMIC ANALYSIS AND DISCUSSION

A comparison of the cost and performance of the proposed HMMC and existing configurations, such as the classical HBSM-based MMC with a bulky transformer [24], [38] and a transformerless hybrid MMC [26], [39], is presented in IV.

TABLE IV  
COMPARISON OF DIFFERENT SOLUTIONS

| Scheme                                   | Comparison of topologies |                                             |                  |           | Function comparison |            |      |      |
|------------------------------------------|--------------------------|---------------------------------------------|------------------|-----------|---------------------|------------|------|------|
|                                          | AC Trans-<br>former      | Number count of SM in<br>each arm           | IGBT-<br>modules | Capacitor | Cost/k\$            | SPG<br>FRT | AGAS | ZVTS |
| HBSM-based MMC<br>with transformer [24]  | 1                        | 20 HBSMs                                    | 120              | 120       | 92.943              | Yes        | No   | No   |
| HBSM and FBSM hy-<br>brid MMC [26], [39] | 0                        | 20 HBSMs + 8 FBSMs                          | 216              | 168       | 73.702              | Yes        | Yes  | No   |
| HMMC in this paper                       | 0                        | 20 HBSMs + 8 FBSMs +<br>12 FBSMs in DC side | 240              | 180       | 80.544              | Yes        | Yes  | Yes  |

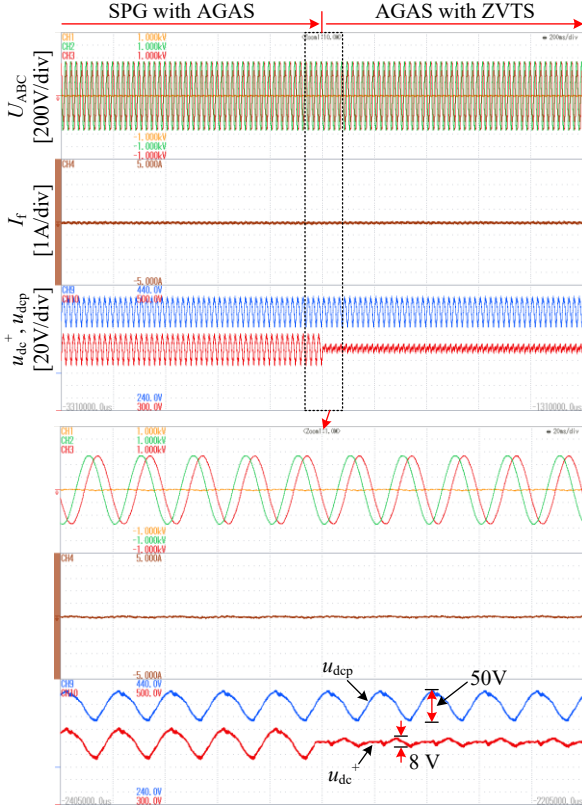


Fig. 26. Experimental results of P2G voltage with/without ZVTS control during AGAS.

In the classical HBSM-based MMC scheme, it is mostly isolated by a transformer before being connected to the distribution network. The zero-sequence component can be blocked by the transformer. The MMC is unaffected by the zero-sequence component, and SPG FRT can be realized without changing the topology and controller. However, this configuration limits the functionality of the MMC. In particular, the MMC only serves to transfer power between the AC and DC DNs and cannot regulate the zero-sequence voltage to achieve arc suppression in the AC DN. Moreover, the transformer is large in size and expensive, which increases the footprint of the equipment and investment cost. Assuming a rated capacity of 5 MW for the MMC, the AC-side voltage is 10 kV and the DC-side voltage is  $\pm 10$  kV. The capacitor voltage of SM is set as 1 kV. A total of 120 HBSMs and a transformer are needed for the classical HBSM-based MMC. Consider a scenario where

the FF450R17ME4 IGBT module that costs \$184.11 is used. The price of the capacitor for each SM will be \$201.99, and the price of the transformer will be \$46,611 for a rated capacity of 5 MW for the MMC. Thus, the total price of the classical HBSM-based MMC with this configuration will be up to \$92,943.

For the transformerless hybrid MMC, the MMC is directly connected to the HDN [26]. Eliminating the transformer significantly reduces the overall investment cost. However, the FRT ability of the MMC needs to be considered in the context of the complex operating conditions of the DN. A certain number of FBSMs need to be used in the MMC arms to achieve FRT. Hence, 20 HBSMs and 8 FBSMs were set in our simulations. This MMC configuration shows the SPG FRT capability and can achieve AGAS under SPG fault conditions. However, considering the impact of AGAS on the DC side, the MMC cannot achieve ZVTS simultaneously.

The proposed HMMC incorporates an FBSM cluster on the DC side and is based on the transformerless hybrid MMC. It achieves AGAS and ZVTS by utilizing the FBSM cluster with a certain increase in cost. As shown in Tab. IV, the cost of the proposed configuration is only 86.6% that of the classical HBSM-based MMC. Compared with the transformerless hybrid MMC [26], [39], the addition of the FBSM cluster in the proposed configuration accounts for only 8.5% additional cost. Although the proposed configuration has a higher initial investment cost, it can provide more comprehensive fault control and economic benefits during operation.

Notably, according to published data on MMC-HVDC station investment structures [40], [41], converter valves and transformers account for approximately 20% and 16% of the total cost, respectively. Other components such as controller and protection systems, filters, civil work and buildings, and auxiliary equipment also contribute to the remaining costs. In our analysis, our cost evaluation focuses specifically on major hardware components, namely IGBT modules, capacitors, and transformers. Since the proposed HMMC removes the need for a bulky and expensive transformer, savings in transformer cost significantly offset the cost of an increased number of semiconductor devices and capacitors. Thus, although the device count is higher, the elimination of the transformer, which accounts for a substantial portion of the conventional MMC cost, makes it reasonable and justifiable that the proposed HMMC results in an overall lower hardware cost.

Therefore, the proposed HMMC saves the bulky transformer

and operates by directly connecting to the distribution network. It can regulate the zero-sequence voltage for AGAS of the distribution network, and realize ZVTS to ensure that the DC grid is not affected by AC grid fault. Moreover, it also has application prospects in DC FRT for DC grids [42].

### VIII. CONCLUSION

This article proposes a novel HMMC with AGAS and ZVTS control abilities for interconnecting the AC and DC distribution networks. The proposed HMMC consists of an MMC, a DC-side FBSM cluster, and a DC-side grounding circuit. The HMMC can flexibly change the operation function of FRT with or without AGAS control. The AGAS control of HMMC is implemented at the zero-axis component to actively regulate the zero-sequence voltage. During AGAS, the fault current is transferred to the DC-side grounding circuit. With the AGAS control, the fault phase voltage and ground fault current are fully regulated within a few microseconds and can be suppressed to within 25 V RMS and 0.5 A in simulation, and 5 V and 0.3 A in a 380 V-12 kVA experimental distribution system. Moreover, during the AGAS and ZVTS, the DC-side zero-sequence voltage ripple is well blocked and decreased from 3.2 kV to near zero in simulation, and from 50 V to about 8 V in an experiment, thereby ensuring the arc suppression in fault AC DN and the power quality of the DC network during AGAS. Thus, the proposed HMMC with AGAS and ZVTS abilities is highly effective at suppressing arcs and inhibiting the zero-sequence voltage from entering into the DC grid under various ground fault conditions. Additionally, the HMMC can transfer power while achieving arc suppression.

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