OPEN ACCESS
IOP Publishing
Semiconductor Science and Technology
Semicond. Sci. Technol. **40** (2025) 115015 (9pp)
https://doi.org/10.1088/1361-6641/ae1c66

Two-waveguide approach for monolithic active/passive photonic integration on GaAs

Laura Michael[1,*], Graham Berry[2], Michael Robertson[2], Giovanni F Cotella[2], Huiyun Liu[3] and Peter M Smowton[1,4]

[1] School of Physics and Astronomy, Cardiff University, Cardiff, Wales, United Kingdom
[2] Ipswich Research Centre, Huawei Technologies Research and Development (UK) Limited, Ipswich, United Kingdom
[3] Department of Electronic and Electrical Engineering, University College London, London, United Kingdom
[4] Institute of Compound Semiconductors, Cardiff University, Cardiff, Wales, United Kingdom

E-mail: michaella1@cardiff.ac.uk

Received 15 July 2025, revised 9 October 2025
Accepted for publication 6 November 2025
Published 18 November 2025

Abstract

Monolithic integration of active and passive photonics is the next step in miniaturisation of semiconductor devices, to streamline their manufacturing and in doing so reduce their cost. However, Si's inefficiency as a light emitter, and the high absorption from quantum wells or dots in III–V materials, requires that the two materials are heterogeneously integrated. This requires either regrowth or additional packaging steps, which add complication in scaling to mass manufacture, as well as high losses at material interfaces. This work proposes a solution whereby a monolithically grown GaAs/AlGaAs platform with both active and passive devices is achieved by using two vertically stacked waveguides, where only one of them contains quantum dots (QDs). In the gain section, where the InAs QDs emit light centred at 1300 nm, the waveguides are decoupled. By changing the relative environment of the two waveguides, light can be made to evanescently couple into the passive waveguide for low loss passive devices. This change can be brought about either by changing the local etch depth, or by the selective oxidation of $Al_{0.98}Ga_{0.02}As$ underlayers. For the correct geometry, 94% of optical power can be successfully coupled between the active and passive waveguide. This coupling is simulated on FIMMPROP by Photon Design Ltd.

Keywords: integration, monolithic, photonic, coupling

* Author to whom any correspondence should be addressed.

1. Introduction

On-chip integration is instrumental in reducing the size of photonic technologies, for more compact sensing [1], communication [2] and imaging devices [3]. Si-on-insulator (SOI) waveguides are the primary choice for passive photonics due to Si's abundance, low cost, compatibility with complementary metal-oxide-semiconductor (CMOS), and well-established manufacturing processes. However, Si cannot efficiently emit light, and so alternative materials are required for active components.

III–V material platforms, such as GaAs, offer high performance lasers and optical amplifiers [4], either through the incorporation of quantum wells [5] or quantum dots [6, 7] (QDs). While III–V materials can also be fabricated into passive devices, light is highly absorbed by these dots or wells. As such, the same material layer cannot be used to make both efficient active and passive devices, without additional processing.

To benefit from the best capabilities of both III–V and Si-based platforms, it is common to assemble a single structure containing parts of each material. This is known as heterogeneous integration.

A common example of heterogeneous integration is flip-chip bonding. In this method, a fully fabricated active device is butt-coupled to (typically) an SOI waveguide by using a 3D alignment technique and an adhesive [8]. An upcoming alternative to this is micro-transfer printing. Again, a fully fabricated device is mounted onto a SOI waveguide, but this time it is deposited on top of the structure. This technique allows for many devices to be integrated simultaneously, as a stamp is used to pick up, align, and deposit many devices at once [9]. Finally, the materials could be combined onto a single platform by regrowth. This involves etching into the SOI (or other passive) waveguide and then initiating a second growth step, where the III–V material is grown in a pre-selected region. A number of challenges must be overcome for successful regrowth [10] and large scale, reliable and reproducible manufacturing has not yet been demonstrated.

Each of these heterogeneous techniques have their own benefits, but all are an additional processing step which would not be required if both the active and passive parts could be grown monolithically. In both flip-chip and micro-transfer printing, large tolerances are required in alignment of the III–V SOA and SOI platforms. For flip-chip bonding the primary losses arise from misalignment of the two waveguides, and the relative mode size in each. Matsumoto *et al* [11] used spot-size converters on an InP/Si platform to achieve 5.1 dB of excess losses due to misalignment and gap. Lin *et al* [12] show that the coupling is more tolerant to alignment variations if the mode field diameter is bigger. In this case 3 dB lower loss was seen by an increase from 1.3×2 μm to 3×3 μm. However, this diameter increase cannot be achieved if the light is to be maintained as single mode, and so the greater loss would have to be accepted for these techniques.

The alternative to the options described above is to procure efficient light generation and low loss optical guiding by using only one material platform. Developments in Si photonics have shown that a Si thin film could be electrically pumped to produce light [13], however this is still in early research and is not in a position to replace the efficient lasing of III–V materials. Conversely, both InP and GaAs have been shown to perform well as passive waveguides and bends [14–16].

Combining high performance GaAs based lasers with GaAs passive structures would allow the monolithic growth of an entire integrated circuit on a III–V platform and will also facilitate the manufacturing of blocks of III–V functions to be transferred as one to the Silicon Photonics platform. The best solution will depend on the final cost and performance of the flip-chip or micro-transfer printing process, the number of active to passive transitions and the performance of any III–V platform. While any photonic device will likely need to be integrated into a CMOS platform during packaging, the larger the photonic circuit that can be monolithically integrated in III–V material, the fewer additional integration processing steps will be required per product, and the easier scalable manufacturing will become. For example, a larger and more complete GaAs based circuit would require fewer pick and place steps with more of the alignment being done lithographically.

In this paper, an active–passive structure is proposed, entirely and monolithically grown on a GaAs/AlGaAs platform. This is achieved by using two vertically stacked waveguides, one for the low loss passive devices and one with InAs QDs to provide gain at 1300 nm [17]. Light is coupled from the gain region into the passive waveguide by changing the relative environment of the two waveguides to induce evanescent coupling between their two TE0 modes. This coupling can be induced through a change in the local etch depth, or by selectively oxidising a layer of $Al_{0.98}Ga_{0.02}As$ beneath the passive waveguide, to change the mode's propagation constant. The coupling expected for each technique is presented, as well as its tolerance to variations in the etching process, which poses the primary challenge in realising these devices experimentally.

The results included in this work are simulated using FIMMPROP software by Photon Design Ltd. Mode profiles in each of the waveguides are calculated using the finite difference method, and these eigenmodes are propagated throughout the coupling region using the eigenmode expansion method. In each case the simulation's mesh and calculation modes are optimised, and the simulation window is chosen to be sufficiently large that the mode powers are negligible at the edges. The GaAs cap and substrate are not included in the mode propagation simulations, to reduce the calculation of radiation modes, because the AlGaAs cladding is sufficiently thick that there is negligible mode overlap with either of these boundaries.

1.1. The active–passive solution using two waveguides

As shown in figure 1, the top waveguide in the ridge structure provides the gain, centred at 1300 nm, due to the inclusion of InAs QDs. The passive waveguide core is just below it and comprises entirely of GaAs. $Al_{0.4}Ga_{0.6}As$ is used around

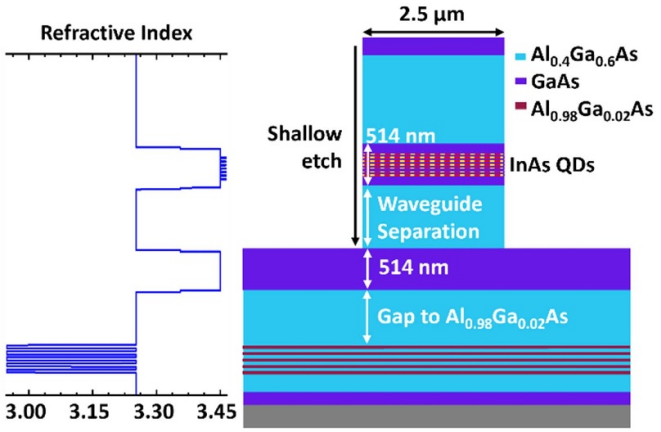

Figure 1. Schematic of the epitaxial layers required for integration using an active and a passive waveguide, and on the left the corresponding refractive index profile. Shown top–down: A GaAs capping layer, $Al_{0.4}Ga_{0.6}As$ cladding, GaAs waveguide with InAs QDs, $Al_{0.4}Ga_{0.6}As$ separating layer, GaAs waveguide, $Al_{0.4}Ga_{0.6}As$ cladding containing 5 repeats of $Al_{0.98}Ga_{0.02}As$, and the lower GaAs contact and substrate. The thicknesses of the cladding and separation layers is varied according to the particular approach used as described subsequently. However, the two waveguide thicknesses are kept at 514 nm in each case.

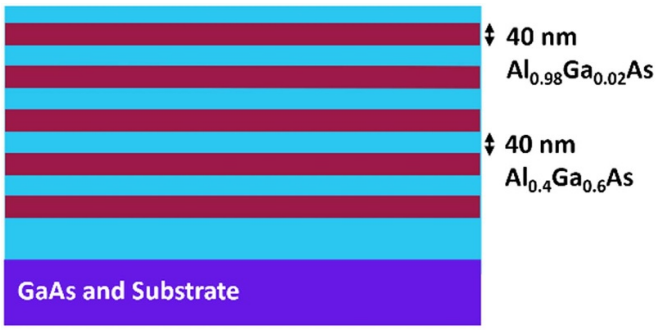

Figure 2. Schema of the $Al_{0.98}Ga_{0.02}As/Al_{0.4}Ga_{0.6}As$ layers included later in two of the three approaches which will be described later, to increase confinement and facilitate mode switching respectively.

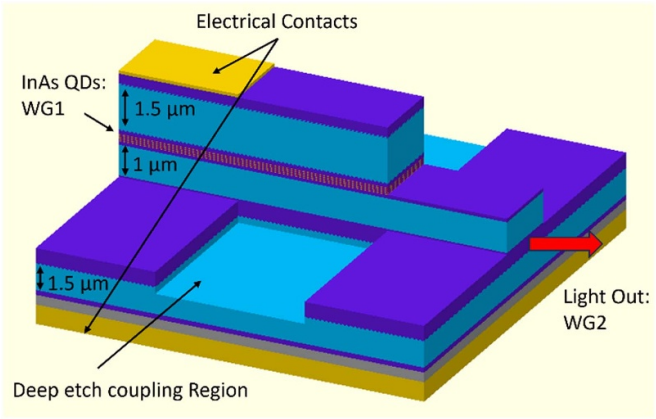

Figure 3. The structure to induce evanescent coupling from the active waveguide (WG1) to the passive waveguide (WG2) by a change in etch depth, using a vertically symmetric epistack, with a waveguide separation of 1 μm. This will be referred to as the 'symmetric stack' henceforth.

each waveguide as the cladding material to provide vertical confinement.

High-Al content layers of $Al_{0.98}Ga_{0.02}As$ can optionally be used beneath the passive waveguide, to increase the confinement and reduce optical losses into the substrate. The layers as used in this work are shown schematically in figure 2. In a similar method to the process in VCSEL fabrication [18], this layer can be oxidised into Al_2O_3. Several thin layers are used to avoid delamination during growth, and the thicknesses and repetition are selected to minimise substrate loss [19].

Due to the shape anisotropy of the QDs, emission is primarily in the TE polarisation [20], and so the focus is on TE modes of the waveguides. The waveguides are designed to be single mode vertically and horizontally, and as such the ridge width is limited to 2.5 μm and the waveguide height to 514 nm. The ridge is mostly 'shallow' etched, which in this work means that the etch depth is less than halfway through the height of the lower, passive waveguide. This provides high confinement to the TE0 mode and causes higher-order modes to be lossy leading to quasi-single mode operation. To induce coupling, this etch can be increased to 'deep', which is greater than halfway through the lower waveguide. For ease of fabrication, preference is given to those etch depths at the interface between layers, as the material change can act as an etch stop or can be readily detected during etching.

To demonstrate different coupling techniques, three approaches based on three different epitaxial structures are simulated. Firstly, as shown in figure 3, the etch-coupling method is demonstrated by choosing a symmetric cladding either side of the two waveguides. Secondly, as shown in figure 4, $Al_{0.98}Ga_{0.02}As$ layers are introduced to reduce the passive loss, and their effect on the etch-coupling scheme relative to the symmetric stack is demonstrated, finally, the oxidation-coupling is shown using the stack in figure 5.

The combination of both active and passive capabilities on one GaAs chip has previously been demonstrated in the literature by using one large GaAs waveguide with offset QDs, which can be selectively etched away to leave passive devices [21]. While this was successful, the small size of the remaining passive waveguide resulted in large mode overlap with the doped materials, leading to an increased loss. If instead, as in this work, two greatly separated waveguides are used, then the overlap with the doped layers can be minimised and the loss avoided.

1.2. Evanescent coupling

The light can be coupled between the active and passive waveguides using evanescent coupling. This occurs when the profiles of two modes overlap, allowing power to pass between

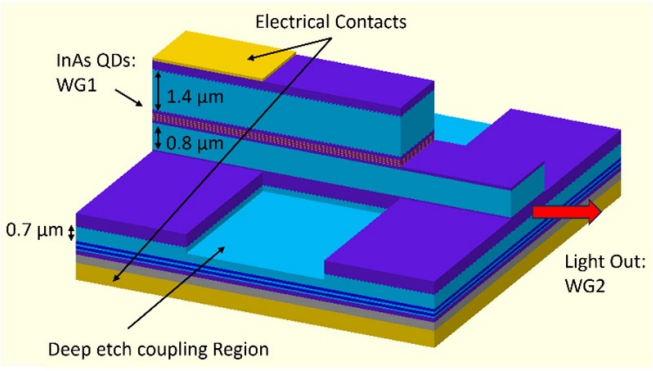

Figure 4. The structure to induce evanescent coupling from the active waveguide (WG1) to the passive waveguide (WG2), by a change in etch depth. The two dark blue layers represent the presence of several repeats of $Al_{0.98}Ga_{0.02}As$ layers, which reduce the loss into the substrate. The waveguide separation is 0.8 μm, and the distance to the $Al_{0.98}Ga_{0.02}As$ layers is 0.7 μm. This will be referred to as the 'etch stack' henceforth.

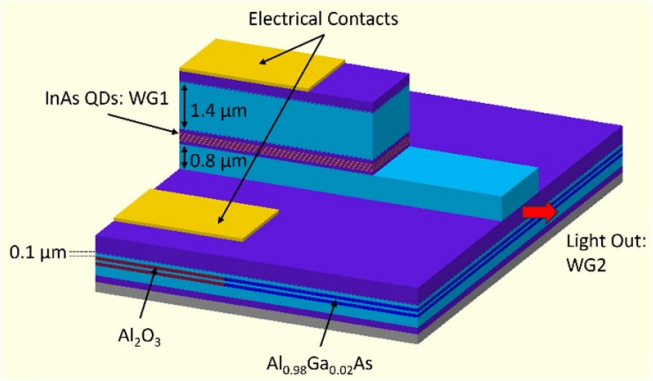

Figure 5. The structure to induce evanescent coupling from the active waveguide (WG1) to the passive waveguide (WG2), by the selective oxidation of $Al_{0.98}Ga_{0.02}As$ layers. The waveguide separation is 0.8 μm, and the distance to the $Al_{0.98}Ga_{0.02}As$ layers is 0.1 μm. This will be referred to as the 'oxidation stack' henceforth.

them. For evanescent coupling to occur, the modes must be close enough together, and also similar in size, propagation constant, and shape [22]. This is demonstrated in figure 6. When the two waveguides are close enough, the modes can overlap, and a large transfer of power is seen between them. If the waveguides are then moved apart, the mode overlap becomes negligible, and no coupling is observed. Finally, if the environment of the two modes is different, such that their mode shape is no longer the same—then much less coupling is seen for the same separation.

Coupling between lateral waveguides is typically achieved by bringing the two closer together over a certain distance, known as the coupling length, before increasing the separation. This is not possible for vertical coupling of an epitaxial structure, as the separation of each layer is fixed. However, the profile and propagation of each mode can be changed, by altering its cladding environment. This changes the amount of

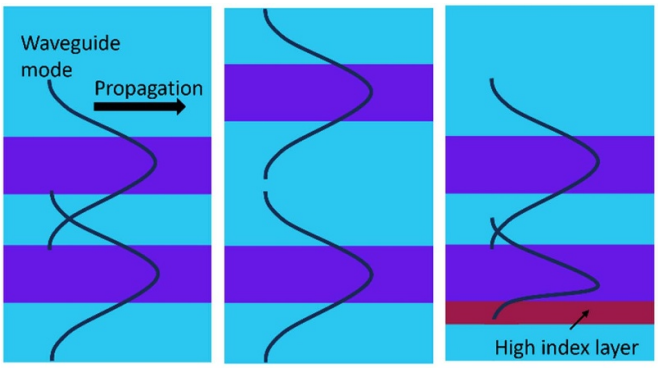

Figure 6. Conditions for evanescent coupling. Left: Two closely spaced waveguides, with coupled modes. Centre: Two separated waveguides, with negligible coupling. Right: Two modes with mismatched mode profile, such that limited coupling occurs.

optical power which is coupled for the same waveguide separation. By selecting this environment to be the same for both waveguides in the coupling region, and very different in other regions, the waveguides can be coupled and decoupled accordingly. The change in propagation is represented in this work by the effective index of each mode.

2. Coupling by etching

The simplest way to change the waveguide environment is to change the etch of the ridge around each of the waveguides. This changes the horizontal confinement of each of the modes, thus changing its mode shape and propagation. When the etch depth is through both the top and bottom waveguides, their environment is the most similar and the coupling is strong. In contrast, reducing this to a shallow etch depth decouples the modes. This effect is shown in figure 7.

As given in figure 3, the light is initially generated in the top waveguide, by electrical excitation from metal contacts placed on the top of the ridge and below the substrate. The light then enters a deeply etched ridge region for an optimised coupling length, to maximise the power coupled into the bottom waveguide. Once the light is in the lower waveguide, the top waveguide can be etched off to stop any coupling back up if further deep etches are needed later in the integrated circuit.

While this method uses only standard etching techniques, the three etch depths required do increase the complexity of fabrication. Depths with the greatest tolerances to unintended variations are used.

2.1. Symmetric stack

For the greatest coupling power, the waveguides should be as identical as possible. This is achieved by a vertically symmetric stack, such that the cladding environment above the top waveguide, and below the bottom waveguide, is identical. The remaining differences between the two waveguides are the presence of the QDs in the top waveguide, and the

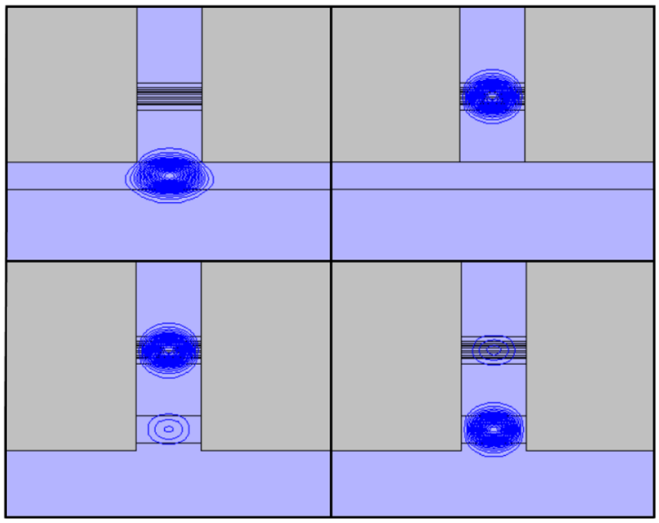

Figure 7. Mode profiles of the two TE0 modes for shallow and deep etch. When deeply etched there is a mode overlap between the two waveguides and power is coupled between them.

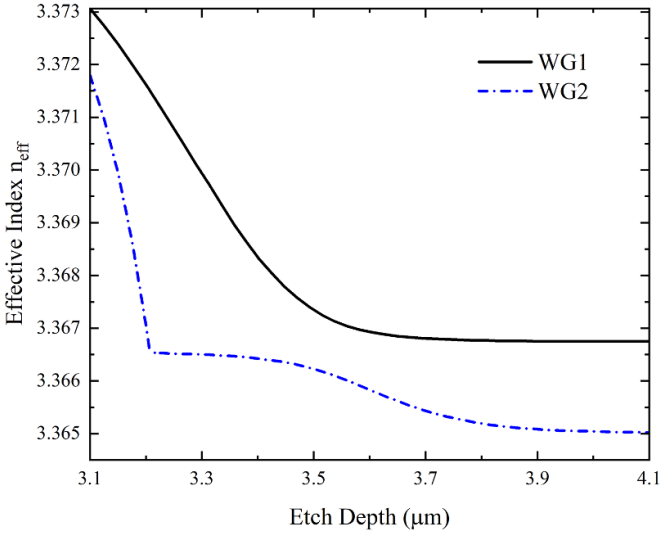

Figure 8. Effective indices of the two waveguides in the symmetric epistack, where WG1 is the top active waveguide, and WG2 is the lower passive waveguide [23].

distant cladding provided by the GaAs-air boundary above the epistack, and the GaAs substrate below it. The cladding thickness is chosen to be sufficiently large to minimise the effect of the top surface (in this case air) or substrate. Figure 8 represents the mode propagation similarities based on the differences in the effective indices of the two modes. At 3.55 μm they are the most similar, and so the strongest coupling effect should be seen. However, the easiest etch depths to consistently reach via fabrication are the top and bottom of the passive waveguide, at 3.3 μm and 3.8 μm. At 3.3 μm, the effective index difference is double that at 3.8 μm.

Figure 9 demonstrates the power output in the bottom waveguide compared to the coupling length, for different etch depths. In contrast to figure 8, the greatest coupling power is actually achieved for an etch depth of 3.6 μm and a coupling length of 592 μm. This is due to the balance between mode shape mismatch and propagation similarity—at this etch depth, the lateral confinement in the two waveguides is not the same. As this etch depth is approximately halfway through the waveguide, at least a $\pm$100 nm fabrication tolerance is needed. With the same coupling length, reducing this etch depth by only 100 nm to 3.5 μm reduces the coupled power from 94% to only 64%. An increase of 100 nm also sees a drop in power to 63%. While a $\pm$100 nm etch tolerance can be expected on a single etch spot, on a 6 inch wafer the difference between, for example, the wafer central and edge could be larger. A 5% tolerance is used to quantify the effect. This corresponds to an etch depth of 3.8 μm. To ensure maximum power coupling across the entire wafer, the coupling length should be chosen to be 404 μm, where the 3.8 μm etch depth has maximum power output of 61%.

If the etch depth is set to be deeper than the bottom of the passive waveguide—at least 3.8 μm—then the power output stabilises at around 54%, with a coupling length of 390 μm. Although the coupling is less efficient, the tolerance

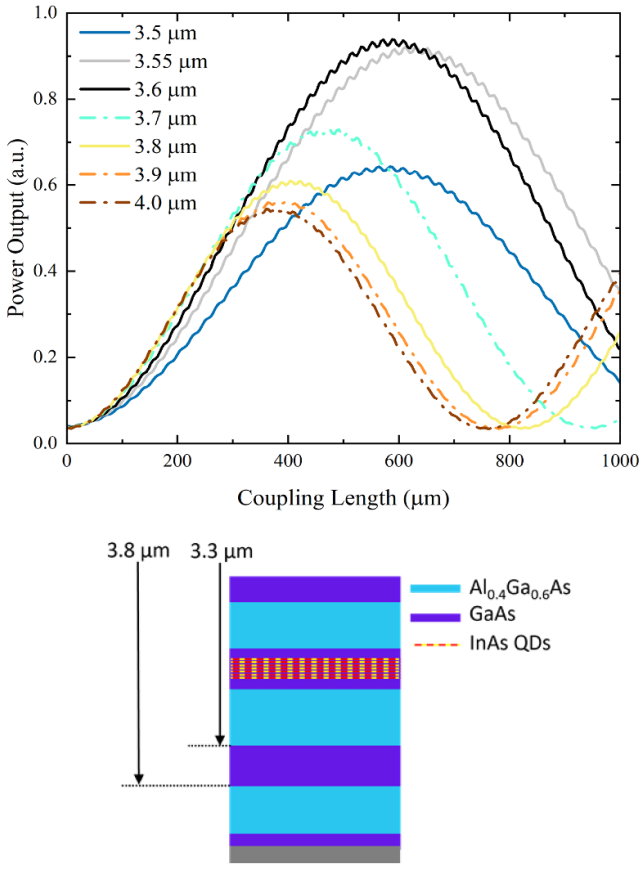

Figure 9. Top: The optical power output in the lower waveguide after evanescent coupling, compared to coupling length and etch depth of the coupling region, for the symmetric epistack. Bottom: A schematic of the layers showing the etch depth to reach the top and the bottom of the lower waveguide [23].

to unintended etch variation would make this a good design choice for devices where the power uniformity is more important than the absolute value. A 54% is equivalent to 2.7 dB of

loss, which is less than what would be expected for flip-chip bonding with misalignment accounted for.

We note that the ripples in figure 9 are due to the multimodality of the coupling section; when deeply etched, both TE0 and TE1 modes can propagate. A small amount of power is coupled between them, as visible in the oscillations.

Light coupled to the lower waveguide in the uncoupled region reduces the mode overlap with the QDs and limits the achievable gain and for the best performance should be minimised. At a coupling length of 0 μm, the 4% power in the lower waveguide represents the light scattered at the etched interface. The power present in the lower waveguide in the 'uncoupled' region is 0.2%. A much larger separation would be needed to reduce this further, due to the exponential tail-off in evanescent mode overlap. As a greater separation also increases the coupling length, the devices would additionally have a much larger footprint. As such a 0.2% coupling is considered to be sufficiently low.

2.2. Inclusion of $Al_{0.98}Ga_{0.02}As$ layers

Adding $Al_{0.98}Ga_{0.02}$ As layers to the cladding beneath the passive waveguide reduces loss into the substrate but also increases the differences in the mode shapes and propagations. Due to this, the two waveguide modes now have less mode overlap for the same separation, and so a smaller separation can, and must, be used to get a high coupling power. Figure 4 shows a schema of the coupling structure for the new epistack, where the $Al_{0.98}Ga_{0.02}As$ layers are represented by the two dark blue lines. Using the same method as in section 2.1, two etch depths can be chosen such that coupling occurs in the deep etched region but not elsewhere. Figure 10 gives the power output in the passive waveguide, again for different etch depths. This time, the depth of the bottom of the lower waveguide is 3.6 μm. Once again, the maximum power is found for an etch depth part-way through the waveguide, at 3.3 μm, with a maximum output power of 88%, but this time for a much lower coupling length of 302 μm. This is due to the reduction in separation between the two waveguides. The most stable etch choice is again found once the etch is entirely through the bottom waveguide; with an etch depth greater than 3.7 μm, the power output becomes very stable at 82%. To allow for etch tolerances, in this case it would be preferred to aim for this more stable value, with a coupling length of 246 μm.

In this structure, again 0.2% of the power is present in the lower waveguide in the uncoupled region. This indicates that the reduced separation is appropriate, due to the higher confinement caused by the presence of the $Al_{0.98}Ga_{0.02}As$ layers.

3. Coupling by selective oxidation

Instead of etching deeper into the ridge, the included $Al_{0.98}Ga_{0.02}As$ layers can be selectively oxidised to change the confinement of the waveguides and therefore make them less similar to each other. As Al_2O_3 has a much lower refractive

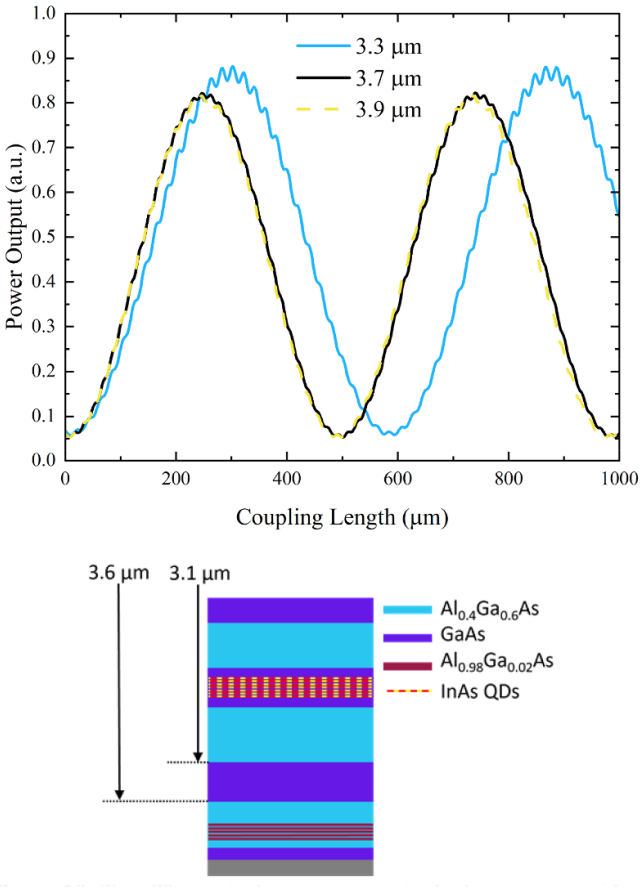

Figure 10. Top: The optical power output in the lower waveguide after evanescent coupling, compared to coupling length and etch depth of the coupling region, for an epistack with the inclusion of $Al_{0.98}Ga_{0.02}As$ layers. Bottom: A schema of the layers showing the etch depth to reach the top and the bottom of the lower waveguide [23].

index than the $Al_{0.98}Ga_{0.02}As$, the effective index of each waveguide mode is increased relative to their distance from it. To maximise this effect, the oxide layer is placed closer to the lower waveguide than the $Al_{0.98}Ga_{0.02}As$ layers are in the etch-coupled stack. This is shown schematically in figure 5.

In this coupling regime there is only one etch depth defining the ridge, and another to remove the top waveguide for the passive sections after coupling. A third etch step is still required to expose the $Al_{0.98}Ga_{0.02}As$ layers for oxidation, but this has more relaxed tolerance for etch depth. The mode profiles of the two TE0 modes in for the oxidation stack are given in figure 11.

For distances of less than 100 nm gap between the bottom of the passive waveguide and the start of the $Al_{0.98}Ga_{0.02}As$ layers, the effect of oxidation on the effective indices are pronounced. Figure 12 shows the effective index change for WG1 (active, top) and WG2 (passive, bottom) when these layers are oxidised and unoxidised. At the 100 nm distance, there is double the effective index difference for the two waveguides when oxidised, compared to unoxidised. The coupling occurs

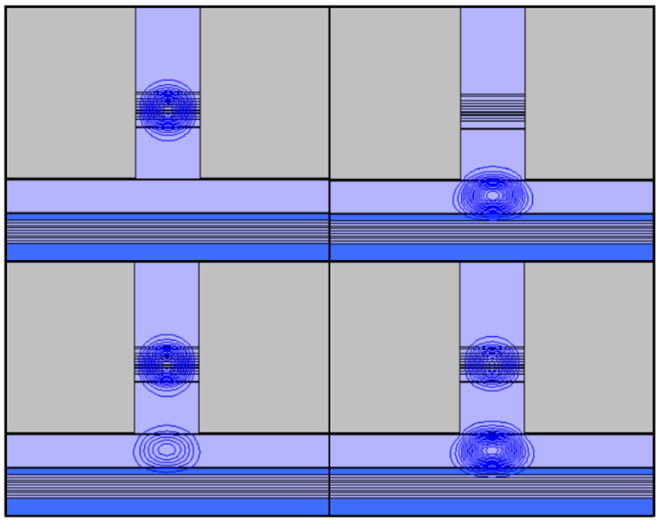

Figure 11. Mode profiles of the two TE0 modes for oxidised (top) and unoxidised (bottom) $Al_{0.98}Ga_{0.02}As$ layers. When unoxidised there is a mode overlap between the two waveguides and power is coupled between them.

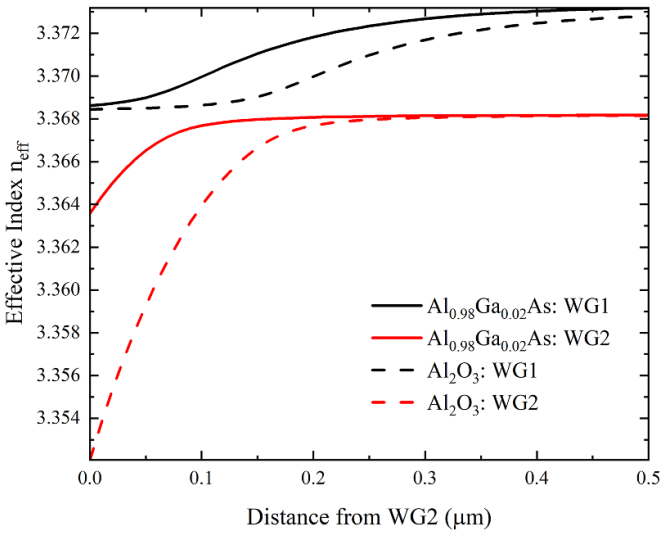

Figure 12. Effective indices of the two waveguides, for oxidised and unoxidised $Al_{0.98}Ga_{0.02}As$, where WG1 is the top active waveguide, and WG2 is the lower passive waveguide [23].

when the $Al_{0.98}Ga_{0.02}As$ is unoxidised and this means that the oxide region needs to be under the gain section. contacts need to be laterally offset instead of above and below the structure, as the oxide is electrically insulating. The ridge etch must be deep enough to expose the lower GaAs waveguide and the contact is placed on the lower GaAs waveguide. While introducing some extra resistance this n-type contact can be sufficiently ohmic.

Calculations are performed to understand the sensitivity of this design to unintended variations in fabrication.

In figure 13, the sensitivity of the ridge etch depth is represented. For the optimum etch depth of 2.9 μm, an optical

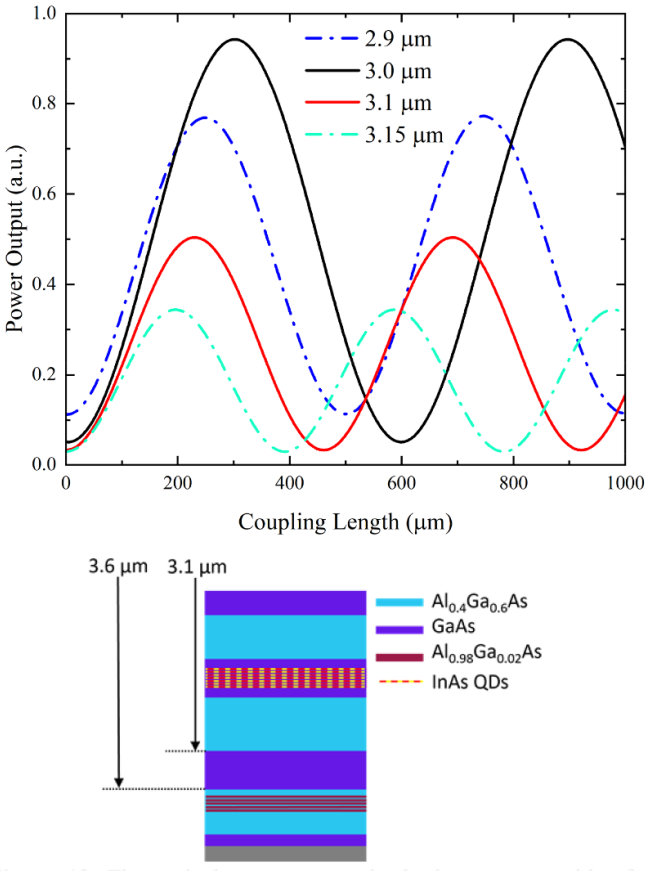

Figure 13. The optical power output in the lower waveguide after evanescent coupling, compared to coupling length and etch depth of the ridge, for the oxidation-coupled epistack. Bottom: a schema of the layers showing the etch depth to reach the top and the bottom of the lower waveguide[23].

power output of 94% is observed, again for a coupling length of 302 μm. This matches that for the etch-coupling case in section 2.2, as their separations are the same. However, this structure is less tolerant to etch variations than either of the etch-coupling methods. A variation of only $\pm$100 nm from the intended etch leads to a coupled power of 54%. This is because this coupling method relies on a bigger effective index change to induce coupling, as the mode shapes in each waveguide are more significantly different. Hence any additional deviation in effective index, as is caused by different etch depths, causes a substantial reduction in coupling efficiency. If a 5% variation, to account for the tolerance across a full-wafer, is used the maximum power output would instead be as small as 34%. Hence this coupling technique is not suitable for wafer-scale fabrication in its current form.

As the coupling region in this oxidation case is entirely shallow etched, only the TE0 mode propagates and so unlike in figures 9 and 10, there are no oscillations in power due to coupling between TE0 and TE1 modes. The optical power in the passive waveguide in the uncoupled region is again 0.2%.

Table 1. A summary of the key performance indicators for each of the three epistacks.

	Symmetric stack	Etch stack	Oxidation stack
Maximum coupled power	94%	88%	94%
Coupling power with an etch tolerance of 5%	61%	82%	34%
Optimum coupling length	404 μm	246 μm	230 μm
Fabrication challenges	2 ridge etches	2 ridge etches	1 ridge etch and oxidation, lateral contacts

4. Summary

This work has demonstrated a two-waveguide structure, where one waveguide is active and the other passive, to provide a platform for monolithic integration. By changing the etch depth around a ridge, or selectively oxidising $Al_{0.98}Ga_{0.02}As$ layers, light can be made to couple between the two waveguides. Three different epitaxial structures have been designed and simulated to present this performance.

The simplest design conceptually is that of a symmetric stack, which uses a deeply etched region to provide the same environment to each waveguide and cause evanescent coupling between them. This has a high maximum coupling power of 94%, but also a much greater coupling length than the other techniques. It does allow sufficient tolerance for a 5% etch variation across a 6 inch wafer, while providing a coupled power of 61% at a length of 404 μm. The other etch-coupled stack, which includes $Al_{0.98}Ga_{0.02}As$ layers to reduce radiative loss, has the lowest maximum coupled power of 88%, but offers significantly more power at an appropriate etch tolerance for wafer-scale processing, of 82% at 246 μm. This combined with its lower-loss passive waveguiding makes it the preferred option for monolithic integration. Both designs require multiple etch steps to define the narrow waveguide ridge but require no uncommon fabrication approaches.

The oxidation-coupled stack also has a maximum coupled power of 94% and a lower coupling length of 302 μm. However, it is the least tolerant to etch depth variations and as such is not appropriate for wafer-scale processing. While this structure only has one etch depth step to define the ridge, it requires additional processing to oxidise the $Al_{0.98}Ga_{0.02}As$. The findings are summarised in table 1.

While the best structure may depend on the scale of fabrication and the functionality to be realised in the integrated circuit, it is the etch stack which offers the greatest overall performance due to its fabrication stability and low coupling length. Future work on fabrication of these devices will provide more insight into the feasibility of each design.

Data availability statement

The data that support the findings of this study are openly available at the following URL/DOI: https://doi.org/10.17035/cardiff.29575019 [23]. Data will be available from 30 September 2026.

Acknowledgment

This work is funded by Huawei Technologies Research and Development (UK) Limited, and also by the UKRI Engineering and Physical Sciences Research Council, Grant Reference Number EPS024441/1.

Author contributions

Laura Michael 0000-0002-9708-054X
Data curation (lead), Formal analysis (lead), Investigation (lead), Writing – original draft (lead), Writing – review & editing (equal)

Graham Berry
Supervision (equal)

Michael Robertson
Supervision (equal)

Giovanni F Cotella
Supervision (equal)

Huiyun Liu 0000-0002-7654-8553
Supervision (equal)

Peter M Smowton 0000-0002-9105-4842
Supervision (lead), Writing – review & editing (equal)

References

[1] Arafin S and Coldren L A 2018 *IEEE J. Sel. Top. Quantum Electron.* **24** 61006121–12
[2] Wang Y, Wang X, Zhu B, Shi Z, Yuan J, Gao X, Liu Y, Sun X, Li D and Amano H 2018 *Light Sci. Appl.* **7** 83
[3] Wang X *et al* 2024 *Chip* **3** 100107
[4] Sobhan A, Anthur A, O'Duill S, Pelusi M, Namiki S, Barry L, Venkitesh D and Agrawal G P 2022 *Adv. Opt. Photon.* **14** 571–651
[5] Mawst L J, Kim H, Smith G, Sun W and Tansu N 2021 *Prog. Quantum Electron.* **75** 100303
[6] Deng H *et al* 2024 *Adv. Phys. Res.* **3** 2400045
[7] Norman J C *et al* 2019 *IEEE J. Quantum Electron.* **55** 2000511
[8] Marinins A *et al* 2023 *IEEE J. Sel. Top. Quantum Electron.* **29** 8200311
[9] Corbett B, Loi R, Zhou W, Liu D and Ma Z 2017 *Prog. Quantum Electron.* **52** 1–17
[10] Shi B, Song B, Taylor A A, Brunelli S S and Klamkin J 2021 *Appl. Phys. Lett.* **118** 122106
[11] Matsumoto T *et al* 2019 *J. Light. Technol.* **37** 307–13
[12] Lin S *et al* 2016 *Opt. Express.* **24** 21454–62
[13] Ma F, Zhou J, Liu K, Yan Z, Dai X, Wu L, Yu L, Sun J, Wang S-Y and Lu M 2024 *Appl. Phys. Lett.* **124** 061101

[14] Montesinos-Ballester M, Jöchl E, Turpaud V, Hillbrand J, Bertrand M, Marris-Morini D, Gini E and Faist J 2024 *ACS Photonics* **11** 62236–2241
[15] Chang L *et al* 2019 *Opt. Lett.* **44** 4075–8
[16] Koester J-P *et al* 2024 *APL Photonics* **9** 106102
[17] Liu H, Hopkinson M, Groom K, Hogg R and Mowbray D J 2008 *Proc. SPIE* **6909** 11–21
[18] Choquette K D, Geib K M, Ashby C I H, Twesten R D, Blum O, Hou H Q, Follstaedt D M, Hammons B E, Mathes D and Hull R 1997 *IEEE J. Sel. Top. Quantum Electron.* **3** 916–26
[19] Albeladi F *et al* 2024 *IEEE* 29*th Int. Semiconductor Laser Conf. (ISLC)* pp 1–2
[20] Humlíček J, Munzar D, Navrátil K, Lorenc M, Oswald J, Pangrác J and Hulicius E 2002 *Physica E* **13** 2–4229–232
[21] Zhang Z, Shang C, Norman J C, Koscica R, Feng K and Bowers J E 2022 *Phys. Status Solidi a* **219** 2100522
[22] Yariv A 1973 *IEEE J. Quantum Electron.* **9** 919–33
[23] Michael L, Berry G, Robertson M, Cotella G F, Liu H and Smowton P 2025 Two-Waveguide Approach for Monolithic Active/Passive Photonic Integration on GaAs *Cardiff University* (https://doi.org/10.17035/cardiff.29575019.v2)