AlGaN/GaN Schottky Barrier Diode Technology for RF Application

Zehao Wu

School of Engineering

Cardiff University

This thesis is being submitted in partial fulfilment of the requirements for the degree of Doctor of Philosophy

Cardiff University August 2025

Acknowledgements

I am deeply grateful to my supervisor, Professor Khaled Elgaid, for his unwavering support, invaluable guidance, and mentorship throughout the course of this research. His expertise and dedication have been instrumental in shaping the trajectory of this thesis.

My sincere thanks go to Dr. Abdalla Eblabla for his exceptional insights, invaluable discussions, and technical guidance. His contributions have been pivotal in enriching and refining this work.

I also extend my appreciation to Dr. Arathy Varghese for her insightful discussions, technical assistance, and constructive feedback. Her contributions have significantly contributed to the advancement of this research.

Heartfelt appreciation goes to my parents, Yuefeng Wu and Guiying Yan, for their constant encouragement, love, and understanding. Their unwavering belief in my abilities has been an enduring source of motivation and inspiration.

I extend my gratitude to all my colleagues and friends for their unwavering support, camaraderie, and enriching discussions that have illuminated my academic journey.

The completion of this thesis was made possible by the collective efforts and support of these exceptional individuals. I consider myself truly fortunate to have had them standing by my side.

Abstract

This thesis investigates AlGaN/GaN Schottky diodes on Si for Ka-band (26.5–40 GHz) nonlinear front-ends. Device-level performance is governed by series/on resistance (R_s/R_{on}), junction capacitance (C_j), and cut-off frequency (f_c). Diodes with 2-/4-finger anodes were fabricated on high- and low-resistivity Si; small-signal parameters were extracted from 100 MHz–50 GHz S-parameters using open/short de-embedding. Representative devices exhibit $C_j \approx 15$ fF at 0 V for a 2-finger high-resistivity sample, falling to ≈ 6.9 fF at −10 V (~54% reduction). For a 25-nm/20%-Al barrier variant, f_c reaches ~163 GHz, providing ample Ka-band margin. Across 26.5–40 GHz, reverse bias consistently improves S11; under −10 V the high-resistivity substrate yields the best overall reflection. Extracted R_s spans ~46–102 Ω depending on layout and epilayer. These results demonstrate the suitability of the reported process and geometries for Ka-band mixers/multipliers and motivate leveraging reverse bias to trade C_j against impedance matching in circuit design.

Table of Contents

Chapter 1

Introduction

Schottky barrier diodes (SBDs) have played a significant role in millimetre and sub-millimetre wave applications since the 20th century, owing to their capabilities in high-frequency operation, fast switching speed, and low forward voltage drop. Over the years, SBDs have undergone continuous advancements in materials, design, and fabrication techniques. Silicon (Si) has been the most commonly used semiconductor material, especially since Gordon Teal's development of the first commercial Silicon device in 1954 [1]. Si's widespread adoption is attributed to its abundance, low cost, and extensive availability worldwide. However, as the demand for higher power handling and operating frequencies grows, the limitations of current Si technology are becoming apparent. Intrinsic material characteristics, such as low breakdown voltage, low electron saturation velocity, and high resistance, have led Si technology to approach its theoretical limits [2]. There is a need for new materials that can surpass these barriers and further enhance device performance.

In contrast to Si technology, III-V compound semiconductor devices exhibit superior characteristics, including higher electron mobilities, which can significantly reduce device resistance. Table 1.1 presents a comparison of key parameters for Si, Gallium Arsenide (GaAs), Gallium Nitride (GaN), and the 2-dimensional electron gas (2DEG) formed at the Aluminium Gallium Nitride (AlGaN) and GaN heterojunction [3]. GaAs and GaN demonstrate higher electron mobility and a larger energy bandgap compared to Si, providing better power handling and potentially higher breakdown voltage.

Apart from electron mobility and saturated electron velocity, the energy bandgap of GaN is significantly larger than that of Si, enabling higher breakdown voltages and better power handling. To support the increasing demands of high-power and high-frequency systems, other wide bandgap materials such as Silicon Carbide (SiC), Gallium Oxide (Ga_2O_3), and Diamond have also drawn considerable attention in recent years. These materials offer a range of advantageous properties including high thermal conductivity, ultra-wide bandgap, and superior breakdown fields.

Table 1.1 presents a comparison of key material parameters relevant to high-frequency Schottky diode applications. GaN offers a good trade-off between manufacturability (especially GaN-on-Si), power performance, and electron transport properties. Although Diamond exhibits exceptional thermal and electrical properties, its fabrication cost and integration challenges remain significant. Ga_2O_3, with an ultra-wide bandgap, shows promise for future generations of high-voltage devices, but its low thermal conductivity currently limits its RF potential.

Table 1.1 Main Parameters of Materials [3]

Material	Electron Mobility ($cm^2/V \cdot s$)	Saturated Electron Velocity ($\times 10^7$ cm/s)	Bandgap (eV)	Breakdown Field (MV/cm)	Thermal Conductivity (W/cm·K)	Wafer Size (inch)	Remarks
Si	1500	1.0	1.12	0.3	1.5	Up to 12″	Mature technology, low cost
GaAs	8500	1.0	1.43	0.4	0.5	≤ 6″	High mobility, fragile
GaN	900	1.5	3.4	3.3	1.3	6–8″ (on Si)	High breakdown, supports 2DEG
SiC (4H)	900	2.0	3.2	3.0	4.9	≤ 6″	Excellent thermal properties
Ga_2O_3	~300	2.0	4.9	>8.0	0.1	2–4″ (lab scale)	Ultra-wide bandgap, poor thermal
Diamond (Bulk)	2200	2.5	5.5	~10	20	<1″ (lab scale)	Ideal material, difficult to process

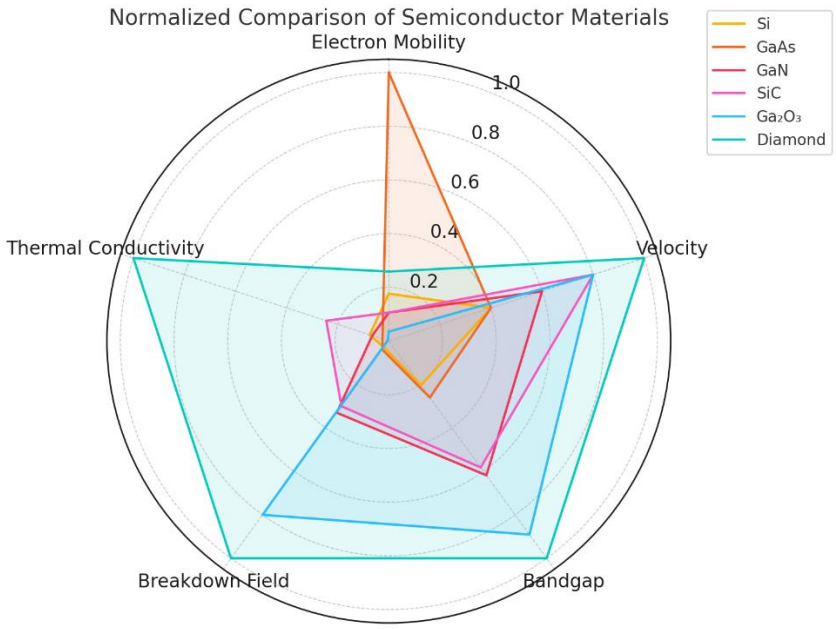


Figure 1.1 Normalized comparison of key semiconductor material properties for high-frequency device applications

GaN, SiC, and Diamond show strong trade-offs between electron mobility, breakdown field, and thermal conductivity, with GaN offering the best balance for manufacturable RF diode platforms.

The discovery and investigation of the two-dimensional electron gas (2DEG) led to the development of a new class of semiconductor devices. The first transistor utilizing a 2DEG was reported in 1980, based on the AlGaAs/GaAs heterojunction, and was termed the high electron mobility transistor (HEMT) [4]. Compared to AlGaAs/GaAs devices, a major advantage of GaN is that a 2DEG can be spontaneously formed at the AlGaN/GaN interface due to strong spontaneous and piezoelectric polarization effects, without the need for intentional doping. This not only simplifies the epitaxial growth process and reduces cost, but also results in significantly higher electron mobility due to the absence of impurity scattering. As a consequence, AlGaN/GaN-based devices exhibit lower sheet resistance, higher current density, and superior high-frequency performance, making them highly suitable for RF and power applications.

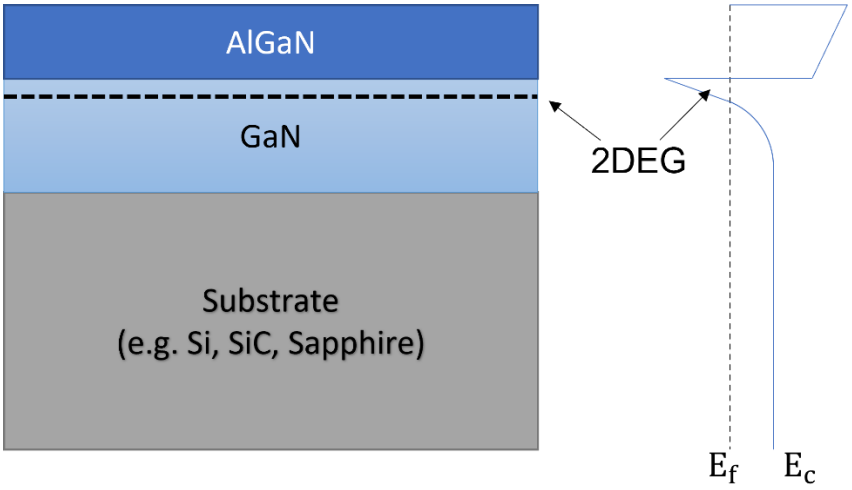


Figure1.2 Cross section of AlGaN/GaN heterojunction and band diagram

Figure 1.2 illustrates the cross-section of the basic AlGaN/GaN heterojunction and its band diagram. Band discontinuity occurs at the interface between two layers when materials with different band gaps are brought together. In the AlGaN/GaN scenario, a quantum well is formed, in which the 2DEG is trapped. Apart from the electron mobility, which has been described in Table 1.1, the 2DEG sheet electron density in AlGaN/GaN heterojunction is approximately $10^{13}/\mathrm{cm}^2$, which is also higher than AlGaAs/GaAs or other III-V materials (approximately $10^{12}/\mathrm{cm}^2$) [5]. Details of AlGaN/GaN heterojunction and 2DEG will be discussed in chapter 2.

1.1 A brief history of GaN and Schottky diode

Gallium Nitride (GaN) is a wide-bandgap semiconductor material that has garnered significant attention and development since its discovery. The early research on GaN dates back to the 1970s; however, substantial progress in the growth and fabrication of high-quality GaN films and devices was not achieved until the 1990s.

In the early stages, GaN was primarily used in optoelectronic devices, such as light-emitting diodes (LEDs) and laser diodes, due to its ability to emit high-intensity blue light. The invention of the blue LED, which earned Isamu Akasaki, Hiroshi Amano, and Shuji Nakamura the Nobel Prize in Physics in 2014,

revolutionized the lighting industry and enabled the development of energy-efficient white LED lighting.

As GaN technology advanced, its potential for high-power and high-frequency applications became evident. One of the most significant breakthroughs was the development of the AlGaN/GaN heterostructure, which allowed for the creation of 2DEG without the need for additional doping. This 2DEG-based AlGaN/GaN heterojunction became the foundation for high-electron-mobility transistors (HEMTs), enabling the creation of powerful and efficient RF amplifiers for wireless communication systems.

The Schottky diode, named after the German physicist Walter Schottky, is a type of metal-semiconductor junction diode that offers fast switching speeds and low forward voltage drop. Schottky diodes made with GaN materials exhibit excellent high-frequency characteristics due to the wide bandgap and high electron mobility of GaN. These attributes make GaN Schottky diodes well-suited for high-power and high-frequency applications, such as RF power amplifiers, microwave circuits, and radar systems.

The combination of GaN's superior material properties and the Schottky diode's advantageous characteristics has led to the development of GaN Schottky diodes for various RF applications. These diodes have found use in power electronics, wireless communication, satellite communication, and military radar systems, among others.

In recent years, ongoing research and advancements in GaN technology have continued to push the boundaries of semiconductor device performance. GaN-based devices are becoming increasingly prevalent in various applications, offering improved efficiency, power density, and reliability compared to traditional silicon-based devices.

1.2 Challenges and opportunities

Despite the significant progress in GaN Schottky diode technology, several challenges remain in realizing their full potential for RF applications. Some of the prominent challenges include:

High Cost of GaN Substrates: Despite the significant progress in GaN device development, the cost of bulk GaN substrates remains prohibitively high, restricting their large-scale deployment. Although GaN-on-Si and GaN-on-SiC technologies have emerged as more cost-effective alternatives, they suffer from challenges such as lattice mismatch, high dislocation density, and thermal expansion differences, which continue to limit device reliability and performance.

Epitaxial Growth and Material Quality: Achieving high-quality epitaxial growth of GaN layers on various substrates is critical for device performance. Controlling defects and dislocations during the growth process remains a challenge.

Thermal Management: GaN-based devices can generate a significant amount of heat during operation. Efficient thermal management techniques are required to ensure device reliability and long-term performance.

Despite these challenges, GaN Schottky diodes offer exciting opportunities for RF applications. Some of the key opportunities include:

Higher Power and Efficiency: GaN-based devices have the potential to handle higher power levels with lower losses, enabling more efficient and compact RF systems.

Wide Frequency Range: GaN Schottky diodes can operate over a wide frequency range, making them suitable for various RF applications, including 5G communication, radar, and satellite communication [6].

1.3 Market and industrial perspectives

The market for GaN-based devices, including Schottky diodes, has been rapidly expanding in recent years. The increasing demand for high-frequency and high-power devices in applications like wireless communication, automotive

electronics, and aerospace is driving the growth of the GaN semiconductor market.

The industrial perspective on GaN Schottky diodes for RF applications is highly positive. GaN-based devices have demonstrated superior performance characteristics, such as higher power density, wider bandwidth, and improved efficiency, compared to traditional silicon-based devices. As a result, industries involved in RF power amplifiers, wireless communication infrastructure, satellite communication, and radar systems are showing interest in adopting GaN Schottky diodes to enhance their products' performance.

1.4 Research Aims and Objectives

The objective of this thesis is to develop and optimise AlGaN/GaN Schottky barrier diodes (SBDs) on silicon substrates for microwave and millimetre-wave applications. Several GaN-on-Si structures have been designed and fabricated to investigate the influence of substrate resistivity, anode geometry, and epilayer structure on device performance. The AlGaN/GaN heterojunction was selected due to its strong 2DEG formation capability and the favourable intrinsic properties of GaN, such as wide bandgap and reasonable lattice compatibility with Si, which enables cost-effective large-area fabrication.

The aims of this research are threefold:

1. **Optimisation of AlGaN epilayer structures**

   This work investigates the influence of AlGaN barrier thickness on diode performance. Two heterostructures with AlGaN thicknesses of 9 nm and 25 nm were selected and fabricated. These structures were designed to study the effect of barrier thickness on parameters such as junction capacitance, leakage current, and breakdown voltage. Silvaco TCAD simulations were used to assist the design phase by estimating electric field profiles and charge distribution across the heterostructure.

2. **Design and fabrication of AlGaN/GaN Schottky diodes with different substrate resistivities**

Devices were fabricated on both low-resistivity silicon ($\rho < 0.03\ \Omega\cdot cm$) and high-resistivity silicon ($\rho > 5000\ \Omega\cdot cm$) substrates. This allowed a systematic evaluation of substrate loss, coupling effects, and their impact on RF performance metrics such as return loss and quality factor (Q). The comparison between the two substrate types provides insights into substrate selection for high-frequency applications.

3. **Evaluation of anode geometry on device performance**

Schottky diodes with varying anode geometries—specifically 2-finger and 4-finger configurations—were designed and fabricated to study their impact on series resistance, parasitic capacitance, and impedance matching. This helped determine the influence of anode layout on both DC and RF characteristics, and provided a basis for layout optimisation in future designs.

1.5 Thesis structure

The organization of the thesis is as follows:

Chapter 1: Introduction

This chapter provides an introduction to the research topic, "AlGaN/GaN Schottky Barrier Diode Technology for RF Applications." It presents the background of SBDs and their significance in high-frequency and high-power applications. Additionally, it introduces the motivation for exploring GaN-based diodes and the potential advantages they offer over conventional Si technology. The research aims and objectives are clearly stated, outlining the focus of the thesis and the areas of investigation.

Chapter 2: Theory of AlGaN/GaN Schottky Diode

In this chapter, the theoretical foundation of AlGaN/GaN Schottky diodes is explored in detail. It covers essential concepts such as the lattice mismatch of materials, the formation of 2-dimensional electron gas (2DEG) at the heterojunction interface, the effects of insertion layers and cap layers on device performance, and the principles of ohmic and Schottky contacts. This chapter provides a comprehensive understanding of the underlying physics and mechanisms governing the behaviour of AlGaN/GaN Schottky diodes.

Chapter 3: Fabrication Process

Chapter 3 describes the fabrication process of the AlGaN/GaN Schottky diodes. It includes the steps involved in the device fabrication, such as epitaxial growth, dielectric deposition, lithography, and metallization.

Chapter 4: Measurement and Analysis of AlGaN/GaN Schottky Diodes on Different Si Substrates

This chapter presents the measurement and analysis of AlGaN/GaN Schottky diodes fabricated on Si substrates with varying resistivity. The impact of different substrate resistivities on the diode's RF performance is thoroughly investigated and discussed. The chapter sheds light on how the choice of substrate material can influence the electrical characteristics and RF performance of the devices, providing valuable insights into optimizing the diode's behaviour for specific RF applications.

Chapter 5: Effect of the Number of Anode Fingers on Device RF Performance

This chapter delves into the effect of the number of anode fingers on the diode's RF performance. The fabrication of two-finger and four-finger devices allows for a direct comparison of how the anode geometry influences the device's characteristics. The extracted parameters and measurement results offer critical observations on the significance of anode finger design in optimizing the diode's RF performance, providing design guidelines for enhanced RF behaviour.

Chapter 6: Effect of AlGaN Layer on Device Performance

Chapter 6 explores the effect of the AlGaN layer on the diode's performance. Two diodes with different AlGaN layer thicknesses are fabricated and characterized to understand the role of this epilayer in shaping the device's RF behaviour. The extracted parameters and comparison of the diodes provide valuable insights into the impact of the AlGaN layer on the diode's electrical properties, helping to optimize the design for improved RF performance.

Chapter 7: Conclusion and future work

Chapter 7 discusses the overall findings from the thesis and provides a comprehensive conclusion. It summarizes the key results and insights obtained from the experimental study on AlGaN/GaN Schottky diodes for RF applications. The chapter highlights the implications of the research in the context of current RF device technology and potential future advancements. Additionally, it discusses any limitations of the study and suggests areas for further exploration. Also presents the recommendations and future prospects for further research and development in the field of AlGaN/GaN Schottky diodes for RF applications. It identifies potential areas of improvement, explores novel device designs, and proposes new avenues for enhancing the performance and efficiency of RF devices based on the findings from the thesis. This chapter concludes the thesis by providing a roadmap for future research in the field of AlGaN/GaN Schottky diodes.

Chapter 2

AlGaN/GaN Schottky diode theory

The typical AlGaN/GaN Schottky diode cross-section structure is shown in Figure 2.1. Several substrates can be used for growing GaN, including Sapphire (used in [7] and [8]), AlN and AlGaN (used as the nucleation layer for GaN on SiC substrate in [9] and [10]), GaN-on-Si technology (recently reviewed in [11]), and GaN-on-diamond devices (studied in recent years [12]).

The choice of substrate plays a critical role in determining the performance, cost, and scalability of GaN-based devices. Several substrate materials are commonly used for GaN epitaxy, including sapphire, silicon carbide (SiC), and silicon (Si). Each of these substrates presents trade-offs between thermal, electrical, and economic factors.

- **Sapphire** offers high resistivity and good lattice compatibility with GaN, but suffers from low thermal conductivity (~0.3 W/cm·K) and limited wafer sizes (typically ≤ 4″). Its brittleness and relatively high cost also limit its scalability.
- **Silicon Carbide (SiC)** provides excellent thermal conductivity (~4.9 W/cm·K) and close lattice matching to GaN, making it ideal for high-power and high-frequency applications. However, SiC substrates are expensive and limited in wafer size (up to 6″), which increases production cost.
- **Silicon (Si)** is the most cost-effective substrate due to its abundance, low bulk cost, and compatibility with large-diameter wafers (up to 12″). Moreover, Si processing benefits from decades of CMOS infrastructure, offering low-cost fabrication tooling and high-volume manufacturing

capability. The main challenges of GaN-on-Si include lattice mismatch, thermal mismatch, and higher dielectric losses, especially at RF frequencies. However, these can be partially mitigated through buffer layer engineering and advanced epitaxial techniques.

The GaN channel layer with a thickness of 1-3μm is positioned above the substrate. The barrier layer, with a higher bandgap compared to GaN, is used to form the 2DEG. $\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}$ is commonly used as the material for the barrier layer, and its properties depend on the aluminum (Al) mole fraction x (ranging between x =0 and x =1). InAlN has also been studied as a barrier layer for InAlN/GaN heterojunction [13]. The anode and cathode are formed by metallization, and there are two types of metal-semiconductor contacts: Schottky contact for the anode and ohmic contact for the cathode.

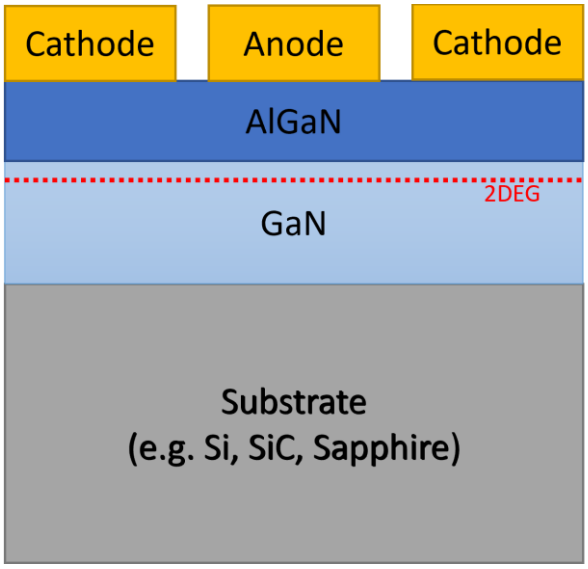


Figure 2.1 Cross session of typical AlGaN/GaN Schottky diode

2.1 Material lattice mismatch and buffer layer

Epilayer growth is a critical process during device fabrication, as lattice mismatch and different thermal expansion coefficients between materials can lead to wafer cracking and bowing due to the high density of dislocations. Table 2.1 displays the lattice and thermal properties of several materials [14]. GaN film exhibits relatively larger mismatch with Si substrate compared to other materials (as shown in Figure 2.2 [15]).

Several approaches have been applied to minimize the mismatch between GaN film and Si substrate to grow the crack-free and high quality GaN film. Another problem of direct growth of GaN on Si is that a Ga–Si eutectic alloy will be formed due to the strong reaction between Ga and Si during the low temperature GaN layer growth [16], also known as melt-back etching.

Table 2.1 Lattice and thermal properties of SiC, sapphire, Si(111), AlN, GaN [2][14][17]

	SiC	Sapphire	Si (111)	AlN	GaN
Lattice constant (Å)	3.08	2.747	3.84	3.112	3.189
Lattice mismatch to GaN (%)	3.5	16.08	-16.9	2.4	none
Thermal expansion ($x10^{-6}/K$)	4.3	7.5	2.4	4.15	5.59
Thermal mismatch to GaN(%)	30	-23	116	34	none

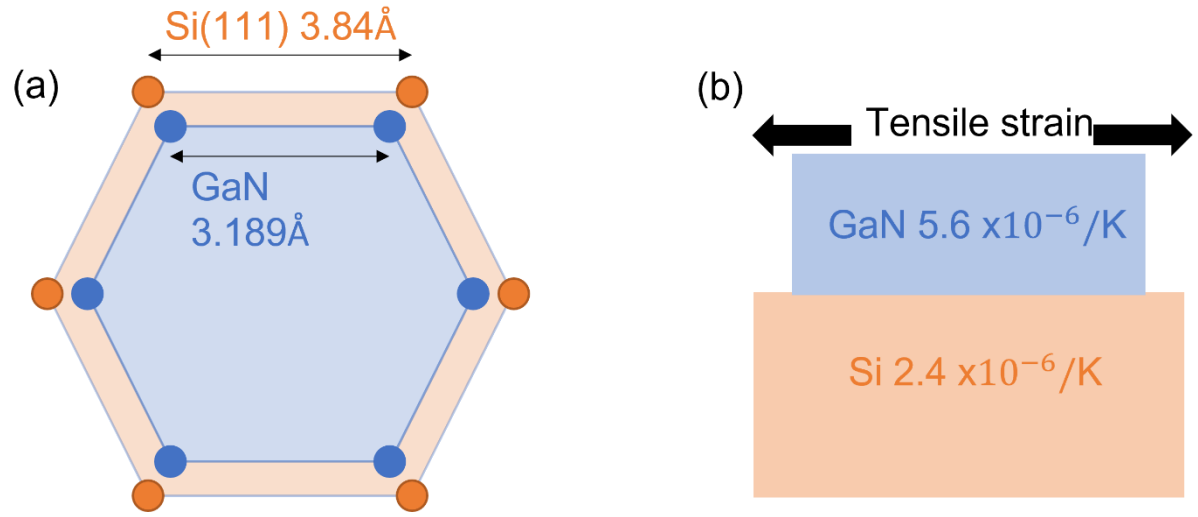


Figure 2.2 GaN on Si (a) lattice mismatch, (b) thermal mismatch

Therefore, a thin film of AlN is widely used as nucleation layer on the top of Si. As can be seen from table 2.1, the lattice and thermal expansion coefficient mismatch between AlN and GaN is significantly smaller than those of Si and GaN. High quality AlN film can be grown on Si (111) due to the lattice matching between Si (111) and wurtzite AlN along certain crystallographic orientation and

through strain relaxation via large number of misfit dislocations at the Si/AlN interface [18], even there is 18.9% lattice mismatch between AlN and Si(111).
A buffer layer is required above the nucleation layer to minimize the effect of mismatch on GaN channel layer to preserve the epilayer quality further. This buffer layer needs to be thick, and highly resistive. Commonly used buffer layer structure includes the graded AlGaN buffer [19, 20], AlGaN/GaN superlattice buffer [21, 22], AlN/GaN superlattice buffer [23, 24], and p-type doped GaN buffer. Mg and Fe are used as dopants in GaN buffer in [25] and [26] respectively, and C-doped GaN buffer is reported in [27, 28]. However, the Mg and Fe-doped buffer suffer from the memory effect. Memory effects in GaN-based devices are typically caused by trap states in the buffer layer or at the heterointerface, leading to delayed or hysteretic electrical responses under bias. These effects can degrade both DC stability and RF linearity, particularly in devices operated at high frequencies. In this work, a carbon-doped buffer layer was used instead of conventional Fe- or Mg-doped buffers. Carbon doping is widely reported to reduce the concentration of deep-level traps and associated memory effects, due to its non-metallic nature and better thermal/chemical stability within the GaN matrix [27]. As such, no significant memory effect was observed during characterisation, and no additional pulsed or transient techniques were required.
This design choice reflects a key trade-off in buffer layer engineering: achieving adequate isolation and resistivity while minimising dynamic trapping effects that compromise high-frequency performance.

2.2 2DEG formation

GaN channel layer is grown above the buffer layer, followed by the barrier layer. As mentioned earlier, the commonly used material for barrier layer to form the 2DEG with GaN is AlGaN. The band gap between GaN and AlGaN is similar due to the electrical and mechanism properties of AlGaN is between those of GaN and AlN. Therefore, the heterojunction can be formed without compromising the crystalline structure of these two materials. The polarization

is generated when a wurtzite crystal symmetry is relaxed [29], it is called spontaneous polarization ($\mathrm{P_{SP}}$). $\mathrm{P_{sp}}$ exists in both AlGaN barrier layer and GaN channel layer and contributes to the formation of 2DEG. As a piezoelectric material, when a film of AlGaN is grown on GaN, the piezoelectric polarization ($\mathrm{P_{PE}}$) occurs due to the strain in AlGaN caused by the lattice mismatch between two layers. Figure 2.3 shows the crystal structure of AlGaN/GaN interface and the polarization in both layers [30]. With more Al composition in AlGaN layer, the electrical and mechanism properties of AlGaN is closer to AlN rather than GaN. This will increase the band gap and lattice mismatch between two layers, and the carrier density in 2DEG consequently. Figure 2.4 shows the sheet carrier density in 2DEG with different Al composition [31-33]. According to [31] an increase of Al composition from 20% to 35% results in a rise in the sheet carrier density from 6.2 x $10^{12}cm^{-2}$ to 13 x $10^{12}cm^{-2}$. A similar trend is observed in another study [32], where an increase in Al composition from 19% to 25% leads to a rise in sheet carrier density from 6.54 x $10^{12}cm^{-2}$ to 9.85 x $10^{12}cm^{-2}$. Moreover, even at a high Al composition of 50%, the carrier density remains substantial, reaching 12 x $10^{12}cm^{-2}$ as reported in [33]. However, in [31] the electron mobility decreases from 1440 $\mathrm{cm^2/VS}$ to 1330 $\mathrm{cm^2/VS}$ when the Al composition increase from 27% to 35%.

The higher 2DEG density at moderate Al composition enhances the screening of impurity and interface roughness scattering, which leads to improved electron mobility. Therefore, an initial increase in Al content can result in mobility enhancement, despite the concurrent presence of alloy disorder scattering.

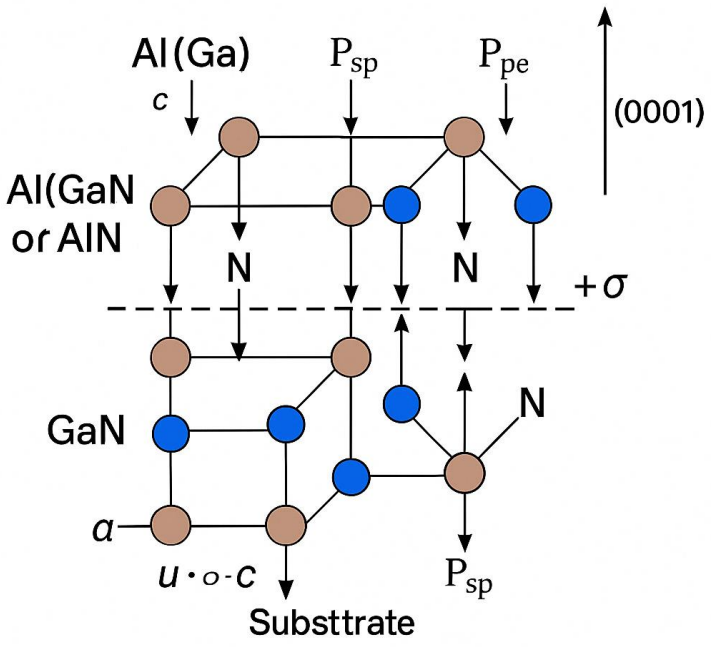


Figure 2.3 crystal structure of AlGaN/GaN and the polarization in both layers

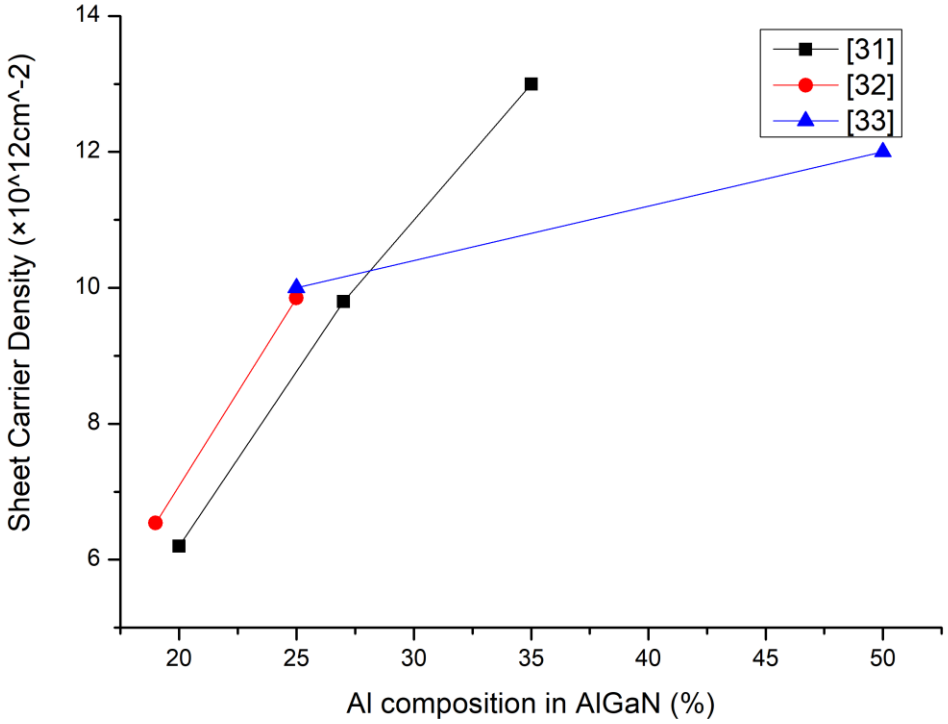


Figure 2.4 Sheet carrier density with different Al composition in AlGaN barrier

The 2DEG mobility is significantly affected by different scatterings, such as interface roughness scattering and alloy disorder scattering [34]. The AlGaN/GaN heterojunction suffer from the alloy disorder scattering, as AlGaN is a ternary compound, this will lead to a dissipation of electron and therefore the decrease of 2DEG mobility [35]. To improve the 2DEG mobility, a AlN spacer layer is applied between AlGaN barrier and GaN channel layer. It is found that HEMTs with AlGaN/AlN/GaN epilayer structure can supply high mobility 2DEG than that without the thin AlN layer [36]. The experiment in [35] shows that the insertion of AlN spacer layer increases the barrier height and therefore suppresses the electron penetration from GaN channel into the barrier, as shown in figure 2.5, the band diagram of AlGaN/GaN and AlGaN/AlN/GaN.

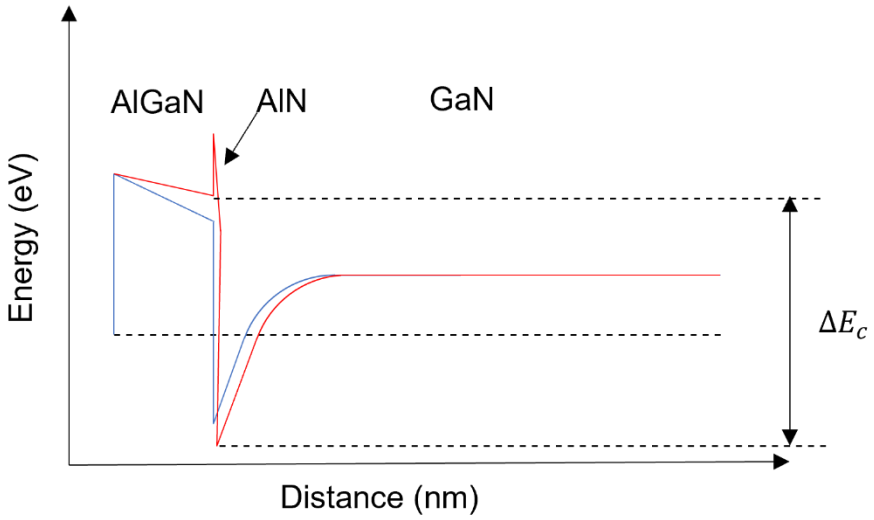


Figure 2.5 Band diagram of AlGaN/GaN (blue) and AlGaN/AlN/GaN (red)

The thickness of AlN spacer layer is critical, as with thick AlN layer, surface roughness scattering is more important than alloy disorder scattering. The experiment result reported in [37] shows that the carrier mobility increases with AlN thickness increases from 0nm to 1nm, while a sharp decrease can be observed when the thickness increased to 2nm. [38] also indicates that the heterojunction with 1.5nm AlN spacer layer has lower carrier mobility than AlGaN/GaN structure, and AlGaN/AlN/GaN with 2 nm AlN has the lowest mobility comparing to other two structures.

2.3 Metal-semiconductor contact

As mentioned above, there are two types of metal-semiconductor contacts, either ohmic contact or Schottky contact. The type of formed contact depends on the work function of the metal (ϕ_m) and the electron affinity of semiconductor (χ). Figure 2.6 shows the energy band diagram for Schottky contact formed by metal and n-type semiconductor.

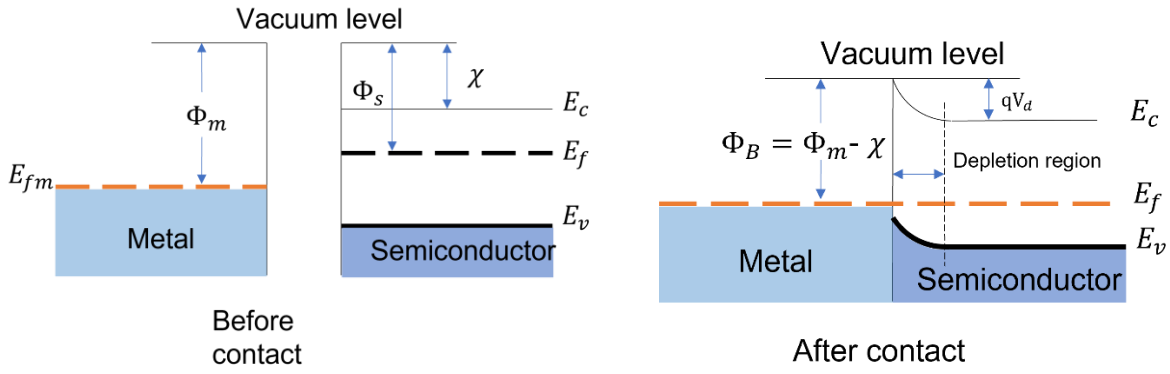


Figure 2.6 Energy band diagram of metal and n-type semiconductor Schottky contact

When a metal is brought into contact with an n-type semiconductor, the alignment of their Fermi levels leads to band bending at the interface. If the metal has a higher work function than the electron affinity plus conduction band edge of the semiconductor, the conduction band bends upward, resulting in the formation of a Schottky barrier with height ϕ_B. This potential barrier limits electron flow from the semiconductor to the metal under equilibrium, and the resulting structure behaves as a Schottky contact.

Conversely, when a low work function metal is used, the conduction band bends downward, and the barrier for electron injection is greatly reduced. In this case, the contact exhibits ohmic behaviour, allowing bidirectional current flow with negligible barrier height.

Figure 2.7 shows the energy band diagrams of an ohmic contact under different biasing conditions. Under forward bias (positive voltage on the metal), electrons can easily move from the semiconductor into the metal. Under reverse bias

(negative voltage on the metal), electrons still encounter only a small barrier, enabling efficient injection from metal to semiconductor.

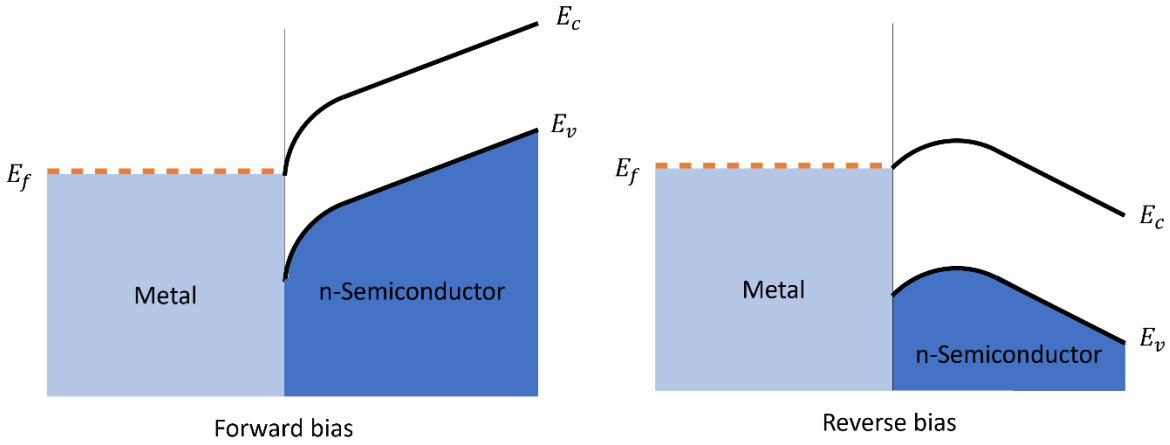


Figure2.7 Ohmic contact energy band bending in bias

Electron transport between metal and semiconductor in Schottky diode can be divided into three main mechanisms, which are thermionic emission, electron tunnelling, and generation-recombination in the depletion region.

2.3.1 Schottky contact

In HEMTs and GaN-based Schottky diodes, the gate contact is typically designed as a Schottky contact. This enables the gate to modulate the 2DEG channel without forming a p-n junction, allowing for depletion-mode operation and low gate leakage under reverse bias. To reduce leakage through the gate, high work function metals are preferred, as they result in a larger Schottky barrier height and hence, lower tunnelling probability.

Table 2.2 shows the work function of several commonly used metals and the ideal Schottky barrier height formed with GaN. As shown in Table 2.2, metals with higher work functions such as Pt, Ni, and Pd form larger Schottky barriers with GaN, which helps suppress reverse leakage current. This is particularly important for Schottky diodes operating at high frequencies, where low leakage and high rectification efficiency are desired.

Table 2.2 Metal work function and Schottky barrier height formed with GaN

	Al	Ti	Au	Pd	Ni	Pt
Work function ϕ_m (eV)	4.28	4.33	5.1	5.12	5.15	5.65
Schottky barrier height ϕ_B (eV)	0.18	0.23	1	1.02	1.05	1.55

Au/n-Gan Schottky contact was formed in [39, 40], and the measured barrier height are 1.02 eV and 0.87 eV respectively. However, Au tends to diffuse into GaN under thermal or electrical stress, creating interfacial states and reducing the effective Schottky barrier height, thereby increasing reverse leakage current [41]. Pt/n-GaN and Pd/n-GaN Schottky barrier were reported in [42], the measured barrier height are 1.27 eV and 1.24 eV respectively. Apart from the work function, metal's adhesion to semiconductor is also critical to metal-semiconductor contact. Ni has better adhesion to GaN comparing to Au and Pt [43]. In these cases, the most commonly used for Schottky contact is Ni/Au. The use of Au is to prevent oxidation and improve the conductivity. Table 2.3 shows the Schottky barrier height and ideal factor of different Ni/Au/n-GaN contact [44].

Table 2.3 Schottky barrier height and ideal factor of Ni/Au/n-GaN contact

Source	[41]	[42]	[45]	[46]	[47]
Ni/Au thickness (nm)	30/50	10/300	40/80	50/300	30/50
Schottky barrier height (eV)	1.3	0.88	0.86	1.18	0.91
Ideal factor n	~1.8	1.18	1.17	1.78	1.52

In addition to diodes, Schottky gates are widely used in GaN-based HEMTs to modulate the 2DEG channel without forming a p–n junction. A high Schottky barrier gate metal such as Ni/Au helps reduce gate leakage under reverse bias, which is essential for achieving high breakdown voltage and stable RF performance.

2.3.2 Ohmic contact

A good ohmic contact requires the metal-semiconductor contact resistance to be low. It can be seen from table 2.2 that the two candidates for ohmic contact forming are Al and Ti, due to their low work function. However, Al-only or Ti-only ohmic contact is not preferred due to the high oxidation propensity and their low reliability on high power and high temperature properties, and the low melting point of Al (600 ℃) causes the thermal stability problem [48]. Ti/Al/metal/Au metal stack is mostly used for ohmic contact with n-GaN, as shown in figure 2.8.

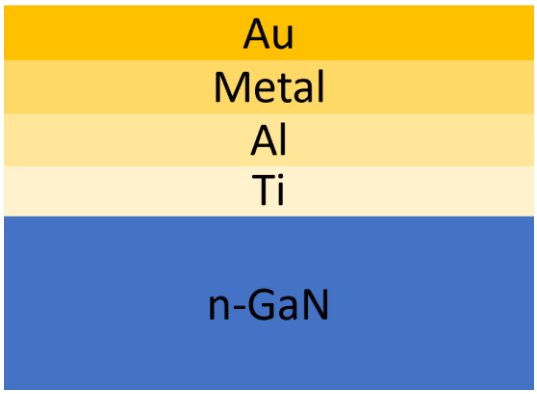


Figure 2.8 Ti/Al/metal/Au metal stack on n-GaN Ohmic contact

When the Ti is used as the first metal layer, the N atoms from n-GaN will be extracted by the Ti atoms and forms TiN compound. The N vacancies in the surface of GaN becomes the electrically active donors. The formation of TiN compound reduces the effective barrier height due to its lower work function (3.74eV) than Ti. The N vacancies leaved in GaN allow electrons flow via tunnelling and therefore reduce the contact resistivity. Experiment in [49] indicates that the strong reaction between Ti and GaN creates the TiN layer, and also a thicker Ti-Ga alloy above the TiN. This strong reaction leaves a large area of void between Ti and GaN, and increases the contact resistance as a result. However, a Al layer above Ti can decrease the Ti-GaN reaction by alloying with Ti. The reason using Au on the top of ohmic contact is the same with Schottky contact, to prevent the oxidation and increase the conductivity. The metal layer between Au and Al is a diffusion barrier to reduce the diffusion

of Au to Al and Ti. Table 2.4 shows the specific contact resistance (ρ_c) of different metal stacks [50-55].

Table 2.4 Specific contact resistance of different metal stacks

	Thickness (nm)	$\rho_c\ (\Omega \cdot cm^2)$	Reference
Ti/Al/Ni/Au	$25/80/20/100$	1.2×10^{-5}	[48]
	$20/20/20/200$	3.15×10^{-5}	[49]
Ti/Al/Ti/Au	$30/100/30/30$	6×10^{-7}	[50]
	$20/170/5/50$	2.2×10^{-5}	[51]
Ti/Al/Pt/Au	$30/100/40/20$	8.4×10^{-5}	[52]
	$25/100/50/200$	8×10^{-6}	[53]

2.3.3 GaN cap layer

The electron affinity (χ) of AlGaN decreases with increasing Al mole fraction[56]. For an n-type Schottky contact, the ideal barrier height follows $\phi B \approx \Phi M - \chi$; hence a lower χ (higher Al content) increases the ideal ϕB . Thicker barriers also reduce tunnelling, typically lowering reverse leakage. (We therefore interpret composition-dependent trends in SBH accordingly in later chapters.). A film of GaN is applied on the AlGaN barrier as the cap layer to improve the effective barrier height, suppress the current leakage [57], due to the lower χ of GaN than AlGaN. The growth of GaN cap layer can also suppress the current collapse caused by the surface state [58].

2.4 Schottky barrier diode operational principle

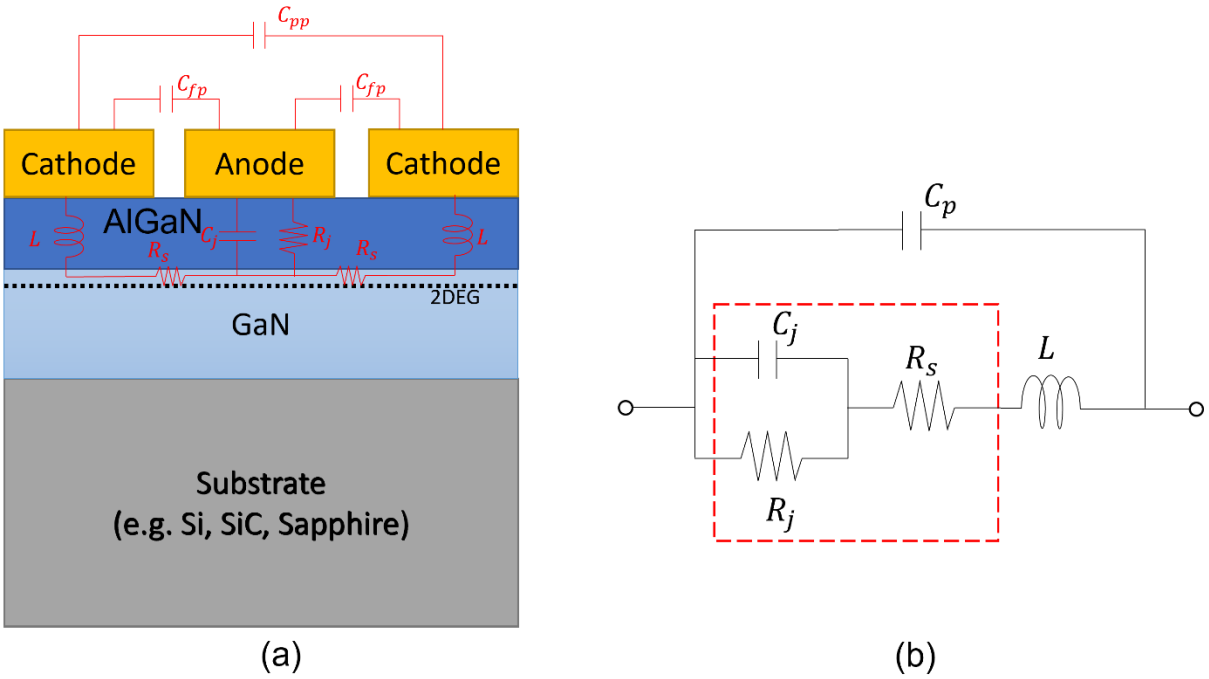
In an AlGaN/GaN Schottky diode, the current flow is primarily governed by the presence of a Schottky barrier at the metal-semiconductor interface and the formation of a 2DEG in the AlGaN/GaN heterostructure. These factors determine the diode's behavior in both forward and reverse bias conditions, making it a valuable component in various electronic devices and circuits.

Figure 2.9 illustrates a comprehensive RF equivalent circuit model for Schottky Barrier Diodes (SBDs), essential for analyzing the diode's operational characteristics in RF applications. The equivalent circuit is an abstraction that simplifies the diode's behavior by representing its physical phenomena with idealized circuit elements, each contributing to the overall performance.

- Parasitic Capacitances (C_{fp}, C_{pp}): These capacitances are due to the physical layout and dielectric properties of the diode's construction. Parasitic capacitances can lead to undesired coupling between different parts of the circuit, causing signal distortion and loss of efficiency, especially at high frequencies where capacitive reactance becomes significant.
- Inductance (L): The inductance symbolized here primarily accounts for the effects of lead and wiring inductances. These inductive components are vital in high-frequency circuits as they can resonate with capacitive elements, affecting the impedance and phase response of the diode.
- Series Resistance ($\mathrm{R_s}$): $\mathrm{R_s}$ is critical in RF diode performance as it contributes directly to insertion loss and can degrade signal-to-noise ratio. Minimizing $\mathrm{R_s}$ is vital for maintaining efficiency, particularly in power-sensitive applications. It is influenced by the materials and the geometry of the diode's construction.
- Junction Resistance ($\mathrm{R_j}$): In a reverse-biased state, $\mathrm{R_j}$ is considered to be very high, effectively isolating the anode from the cathode. This high resistance ensures that the reverse current remains negligible, a desirable property for rectification and switching applications.
- Junction Capacitance ($\mathrm{C_j}$): $\mathrm{C_j}$ at zero bias ($\mathrm{C_{j0}}$) is a function of the depletion region's physical dimensions and the dielectric constant of the semiconductor material. It affects the charging time and, consequently, the speed at which the diode can switch from conducting to non-conducting states.

The cut-off frequency (f_T), representing the maximum frequency at which the diode can effectively operate as a rectifier, is given by equation 2.1:

$$f_T = \frac{1}{2\pi C_{j0} R_s} \tag{2.1}$$



(a) (b)

Figure 2.9 (a) Schematic cross-section of an AlGaN/GaN Schottky barrier diode and (b) its equivalent circuit model

2.5 Schottky diode RF applications

Schottky diodes find widespread applications in radio frequency (RF) circuits due to their unique characteristics and superior performance at high frequencies. Their key attributes make them essential components in various RF applications, providing benefits such as low noise, fast switching speeds, and minimal power dissipation. In this section, we will explore the significant RF applications of Schottky diodes and highlight their advantages in these areas.

2.5.1 Mixer

In high-frequency communication systems, particularly in the W-band (75–110 GHz), Schottky diodes are widely used as mixers due to their fast switching, low capacitance, and nonlinearity. These mixers serve as key components for

up/down-converting RF signals to intermediate frequencies (IF), which is essential in radar, satellite receivers, and point-to-point communication systems. GaN-based Schottky diodes, with their superior breakdown voltage and power handling capabilities, have become strong candidates for future high-frequency mixer designs.

A simplified single diode mixer schematic is shown in Figure 2.10, illustrating the basic configuration. However, practical diode mixers are more complex and often involve multiple diodes and additional circuitry for improved performance. Various mixer designs, such as single-balanced, double-balanced, and single-sideband, are employed to optimize specific applications.

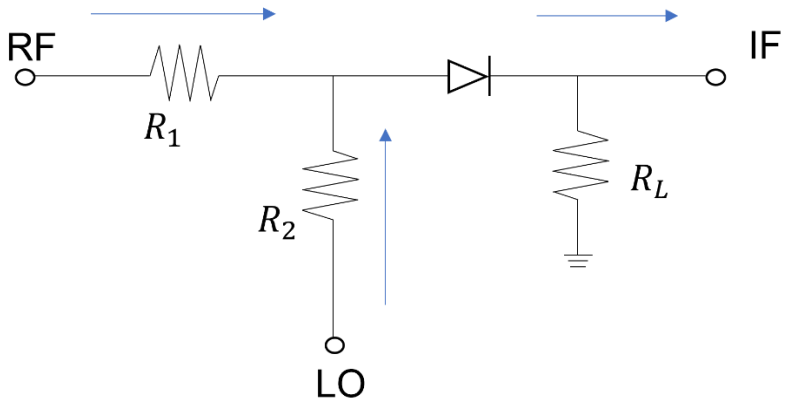


Figure 2.10 Simplified single diode mixer schematic

The power level of the local oscillator (LO) signal plays a critical role in determining the mixer's conversion gain. A higher LO power level can result in a higher conversion gain (lower conversion loss). However, it is essential to ensure proper LO-RF and LO-IF isolation, as well as impedance matching at the LO, RF, and IF ports to maximize the conversion gain. Mismatched ports can lead to signal reflections and loss of power, impacting the overall performance of the mixer.

Table 2.5 compares the reported performance of mixers across a range of frequencies and LO power levels. The goal here is to illustrate the typical conversion loss achievable in real-world designs, as well as the LO drive requirements.

From this table, it is evident that mixers operating in the mm-wave region (e.g., 75 GHz, 91 GHz, 94 GHz) require relatively high LO power (~10–15 dBm) and still suffer from non-negligible conversion losses (>5 dB). This highlights the importance of optimizing the diode parameters—particularly series resistance and junction capacitance—to minimize losses at these frequencies.

Table 2.5 Reported performance of mixer at different operation frequencies

	[59]	[60]	[61]	[62]	[63]
Frequency(GHz)	2.5	94	10	91	75
LO power(dBm)	10	9.5	13	12	15
Conversion loss (dB)	12.9	5.5	8	8.5	11.4

These insights reinforce the motivation behind this thesis: to develop Schottky diodes with low R_on, reduced C_j, and high cut-off frequency, making them suitable for future W-band mixer applications.

The series resistance in the diode is a crucial factor influencing mixer performance. A higher series resistance can lead to increased power losses and reduce the conversion gain [64].

Parasitic capacitance refers to unintended capacitances present in the diode structure due to its physical layout and the presence of other conductive elements. These capacitances can introduce additional reactance into the circuit and reduce the conversion gain, especially at high frequencies [65].

Furthermore, the junction capacitance of the diode also plays a significant role in determining the mixer's performance. The junction capacitance affects the diode's impedance, which is essential for matching the input and output signals to achieve optimal conversion gain. Proper tuning and optimization of the junction capacitance are necessary to maximize the mixer's overall efficiency.

2.5.2 Multiplier

In addition to mixers, Schottky barrier diodes (SBDs) are widely employed as nonlinear elements in frequency multipliers. These circuits generate harmonic signals of the input frequency and are essential for producing high-frequency local oscillator (LO) signals in radar, spectroscopy, and wireless communication systems, particularly in the millimetre-wave and terahertz bands.

GaAs-based SBDs have traditionally been used in commercial multiplier designs due to their high cutoff frequency and mature fabrication technology. However, recent studies have shown that GaN-based SBDs offer promising advantages in terms of higher breakdown voltage, thermal stability, and power handling, which are particularly desirable in high-power mm-wave frequency multipliers.

A basic Schottky diode frequency multiplier configuration is shown in Figure 2.11, where the input signal (f_{RF}) is applied to a single diode that generates output components at harmonics such as 2*f_{RF}, 3*f_{RF}, etc. While the simplified schematic illustrates a basic doubler, practical multiplier designs often incorporate multiple diodes in anti-parallel or balanced configurations, along with resonant circuits and impedance-matching networks to optimise the output power and spectral purity.

Recent works demonstrate the potential of GaN-based multipliers in achieving high efficiency and output power at mm-wave frequencies. For example, Kim et al. [66] reported a 94 GHz GaAs tripler achieving 12.5% efficiency, while Choi et al. [67] demonstrated a GaN-based W-band doubler with an output power exceeding 100 mW. These studies highlight the evolution of Schottky multipliers from low-power designs toward high-efficiency solid-state sources suitable for demanding mm-wave applications.

The development of GaN SBDs with low junction capacitance and high thermal stability is crucial to further improving the performance of frequency multipliers

operating beyond 100 GHz. This motivates the exploration in this thesis of GaN-on-Si diode structures optimised for such nonlinear RF applications.

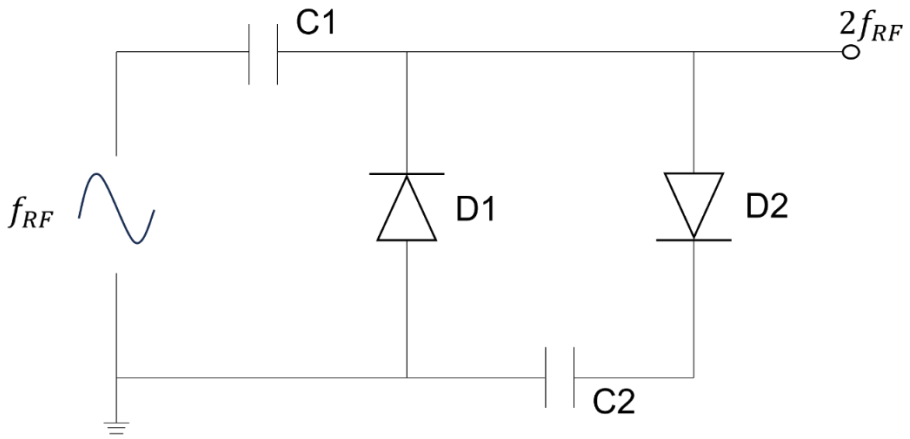


Figure 2.11 Diode doubler circuit

2.6 Conclusion

This chapter provides a detailed exploration of the theoretical and operational principles of AlGaN/GaN Schottky diodes, focusing on the following key aspects:

1. Lattice Mismatch and Buffer Layers: The chapter discusses the significance of lattice mismatch and buffer layers in the fabrication of AlGaN/GaN Schottky diodes. These factors significantly impact the performance and reliability of the devices.
2. Formation of the Two-Dimensional Electron Gas (2DEG): A thorough discussion is presented on the formation of 2DEG in AlGaN/GaN heterostructures. The 2DEG is key to the high performance of these diodes.
3. Types of Metal-Semiconductor Contacts: The mechanisms of Schottky and Ohmic contact formation and their impact on device performance are analysed.
4. RF Applications of Schottky Diodes: The chapter emphasizes the application of Schottky diodes in RF systems, such as mixers and

frequency multipliers, and highlights the importance of proper circuit design and diode characteristics for performance optimization.

The research in this chapter not only provides deep insights into the fundamental theories behind AlGaN/GaN Schottky diodes but also offers significant guidance for their practical applications in RF systems. Through careful consideration of material selection, device structure, and circuit design, the performance and efficiency of these diodes can be further enhanced, playing a vital role in high-frequency and high-power applications.

Chapter 3

AlGaN/GaN Schottky diode fabrication and measurement

3.1 Introduction

This chapter presents a detailed fabrication process of AlGaN/GaN Schottky diodes, which are essential components for achieving efficient and reliable electronic devices in various applications, including high-frequency and high-power circuits. The unique material properties of the AlGaN/GaN heterostructure make it a promising platform for Schottky diodes in RF circuits.

The fabrication process involves a series of carefully optimized steps, including material growth, device structure design, lithography, etching, metallization, and device characterization. Each step plays a crucial role in determining the final device characteristics and performance. This chapter highlights the key aspects of each fabrication step and discusses the influence of process parameters on the resulting device properties.

3.2 Epilayer growth

The first step in the fabrication process is the growth of the AlGaN/GaN heterostructure on a suitable substrate. Epilayer growth is to transport the atoms of material from high purity sources to the substrate wafer surface. The commonly used GaN growth methods are Molecular Beam Epitaxy (MBE) and is metal-organic chemical vapour deposition (MOCVD).

3.2.1 MBE

MBE is a sophisticated and highly controlled method used for the synthesis of thin films and crystal structures layer by layer on a substrate. Conducted in an ultra-high vacuum environment, MBE introduces elemental or compound sources, which are heated to produce a directed molecular or atomic beam towards a substrate. As the particles arrive at the substrate surface, they can migrate, interact, and integrate into the growing film, ensuring precise control over layer thickness, composition, and doping. One of the key advantages of MBE is the precise control it offers, making it possible to grow high-quality epitaxial layers with atomically sharp interfaces [66]. However, the growth rate of GaN using MBE is typically below 1μm/h. The low growth rate has limited MBE's application in the demand for thick GaN and increased production costs [67].

3.2.2 MOCVD

The technique used in this thesis to grow epitaxial structures is MOCVD. The growth parameters should be optimized during this process, such as the growth temperature, and reactant gases flow pattern [68]. MOCVD is a widely used epitaxial growth technique that enables precise control over the material composition and thickness. The growth process involves the decomposition of metal-organic precursors in a heated reactor, resulting in the deposition of crystalline AlGaN and GaN layers on the substrate. In MOCVD, chemicals are vaporized and react with other gases in the reaction chamber to turn the chemicals into desired crystal. Comparing to MBE, the growth rate of GaN epilayers using MOCVD commonly exceeds 1-3μm/h. Figure 3.1 shows the deposition process on substrates surface.

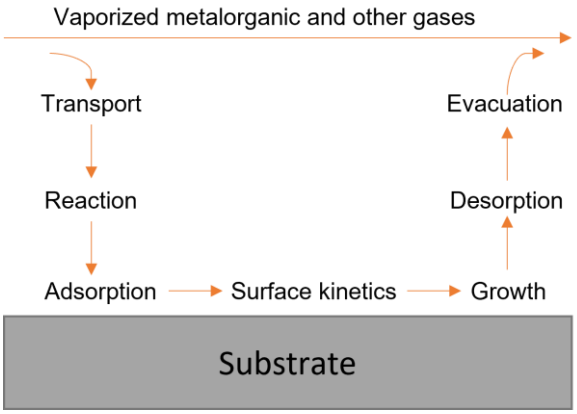


Figure 3.1 Deposition Process on substrate surface

The quality, uniformity, and crystalline nature of the GaN films heavily depend on the choice of precursors. Trimethyl gallium (TMGa) and triethyl gallium (TEGa) are the most commonly utilized gallium precursors, and the nitride precursor is ammonia (NH_3). The typical chemical reaction is shown by equation 3.1, where CH_4 is methane, and C_2H_6 is ethane.

$$TMGa + NH_3 \rightarrow GaN + CH_4 \quad (3.1)$$

$$TEGa + NH_3 \rightarrow GaN + C_2H_6$$

TMGa, being more reactive, typically decomposes at lower temperatures compared to TEGa. NH_3 is the preferred nitrogen source due to its high reactivity and ability to provide the necessary nitrogen atoms for GaN growth [69].

3.3 Lithography

Lithography is a process used in microfabrication to transfer a pattern onto a substrate. The pattern is defined on a mask, which is positioned in close proximity to the substrate, and light is shone through the mask to transfer the pattern onto the substrate. The substrate is then chemically treated to produce the desired pattern. Lithography is a critical step in the device manufacturing process, as it enables the creation of the microscopic features that define the performance and functionality of the resulting device. Two mainly used

lithography are optical lithography, also known as photolithography, and electron beam lithography (e-beam lithography).

3.3.1 Photolithography

Photolithography is a light-based lithography technique that involves projecting light through a mask (photomask) onto a light-sensitive photoresist-coated wafer. The light changes the properties of the photoresist, which is then developed to reveal the desired pattern. Photolithography is a widely used and highly scalable technology, but it has limitations in terms of the minimum feature size that can be achieved.

As illustrated in figure 3.2, the intricate steps of the photolithography process are showcased. In the context of this work, a bilayer photoresist system was employed to enhance the lithography results. This bilayer approach uses two distinct layers: a bottom layer known as a lift-off resist (in this case, LOR 10) and a top imaging layer (S1805). The LOR 10 serves to create an undercut profile, essential for subsequent lift-off processes, while the S1805, being sensitive to light, captures the intricate patterns from the photomask. This combination ensures improved pattern fidelity and simplifies subsequent processing steps, such as metal deposition and lift-off.

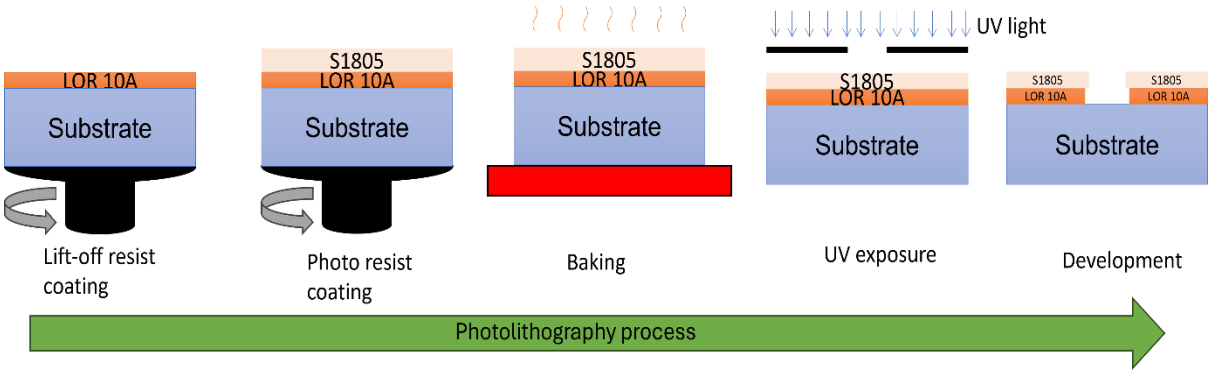


Figure 3.2 Photolithography process used in this study

3.3.2 Electron beam lithography

Electron beam lithography (EBL) is a highly advanced nanofabrication technique that enables patterning at the nanoscale with exceptional resolution

and alignment accuracy. Unlike optical lithography, which relies on light exposure through a mask, EBL employs a focused electron beam, typically within a scanning electron microscope (SEM), to directly write patterns onto an electron-sensitive resist. This technique offers alignment accuracy down to 0.5 nm, making it suitable for sub-micron device fabrication.

In this work, the Raith EBPG 5 system was used for all EBL processes. A bilayer resist scheme comprising PMMA 2010 (bottom) and PMMA 2041 (top) was adopted. PMMA 2010, having a lower molecular weight and higher concentration, serves as the bottom layer to provide structural support. PMMA 2041, with its higher molecular weight and lower concentration, forms the top layer and develops more readily in solvent, enabling an undercut profile favourable for lift-off processes.

In addition, a thin aluminum discharge layer (~30 nm) was deposited on top of the resist. This is crucial when performing EBL on insulating substrates or using non-conductive resists like PMMA. The aluminum layer prevents charge accumulation, which can distort the electron beam trajectory and degrade pattern fidelity. It acts as a conductive path, allowing excess charge to dissipate during exposure.

While Figure 3.2 illustrates the optical photolithography process using S1805/LOR 10A, the overall EBL process follows similar steps in terms of coating, baking, exposure, and development, with the main difference being the resist system and the inclusion of the discharge layer.

3.4 Etching

Etching is a critical step in the fabrication process, used to remove unwanted material and define the diode's active area. Etching techniques in semiconductor fabrication are broadly classified into wet etching, which uses chemical solutions, and dry etching, which relies on plasma-based methods. In this work, only dry etching techniques were used, specifically Reactive Ion Etching (RIE) and inductively coupled plasma (ICP). Wet etching is discussed

here for completeness and comparison. RIE and ICP are commonly used for etching the AlGaN/GaN layers with high precision. The etch depth is carefully controlled to achieve the desired mesa depth, typically around 150nm, which defines the diode's active region.

3.4.1 Wet etching

Wet etching is a fundamental and widely used technique in the field of semiconductor processing and microfabrication. It plays a crucial role in defining precise patterns and structures on semiconductor substrates, allowing for the creation of intricate and complex devices. Wet etching involves the selective removal of material from a substrate using chemical solutions, known as etchants, to achieve the desired pattern or structure. A schematic illustration of the wet etching process is shown in Figure 3.3.

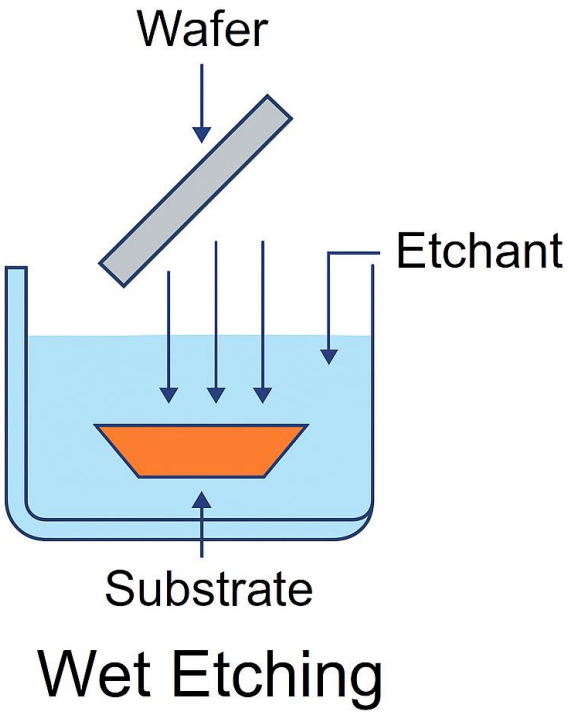


Figure 3.3 Wet Etching

One of the significant advantages of wet etching is its ability to produce smooth and isotropic etch profiles, particularly in comparison to dry etching techniques such as RIE. This capability is crucial in applications where a uniform and

defect-free surface is required, such as in the fabrication of microelectronic devices or microfluidic systems.

Despite its advantages, wet etching does have limitations. It is less suitable for creating sub-micron features and structures with high aspect ratios, as it tends to cause under-etching or lateral material removal. Additionally, wet etching may introduce some surface contamination and produce relatively lower resolution patterns compared to more advanced lithographic techniques.

GaN is a material characterized by its high hardness and chemical stability, which results in a relatively low etching rate and limited etching selectivity during the wet etching process. Various aqueous acid and base solutions were tested for etching of GaN in [70], while no wet etch solutions appreciably etched GaN films. [71] reported that GaN can be etched in sodium hydroxide (NaOH) solution. However, the etching ceased due to the formation of gallium hydroxide ($Ga(OH)_3$).

3.4.2 Dry etching

Dry etching, also known as plasma etching or dry plasma etching, is a vital and widely used semiconductor processing technique for microfabrication and nanofabrication. Unlike wet etching, which uses chemical solutions to selectively remove material from a substrate, dry etching employs plasma, a high-energy ionized gas, to etch materials with exceptional precision and control.

One of the primary advantages of dry etching is its anisotropic etch characteristics. Unlike wet etching, which tends to cause isotropic material removal, dry etching produces well-defined and vertical etch profiles, allowing for the creation of high-aspect-ratio structures and precise patterning. This anisotropic etching capability is crucial for producing sub-micron features and nanoscale structures.

Furthermore, dry etching enables better control over the etching process, offering higher selectivity, uniformity, and repeatability compared to wet etching. The use of reactive gases allows for the customization of etching rates and etch

profiles, making it possible to etch multiple materials selectively and with high accuracy. This level of control is essential in the fabrication of complex integrated circuits and advanced microelectronic devices.

RIE is a dry etching process that employs chemically reactive plasma to remove material deposited on substrates. The plasma is generated by introducing a mixture of gases into a low-pressure chamber and applying a RF power to create a glow discharge. This discharge dissociates the gas molecules into ions, radicals, and other excited species.

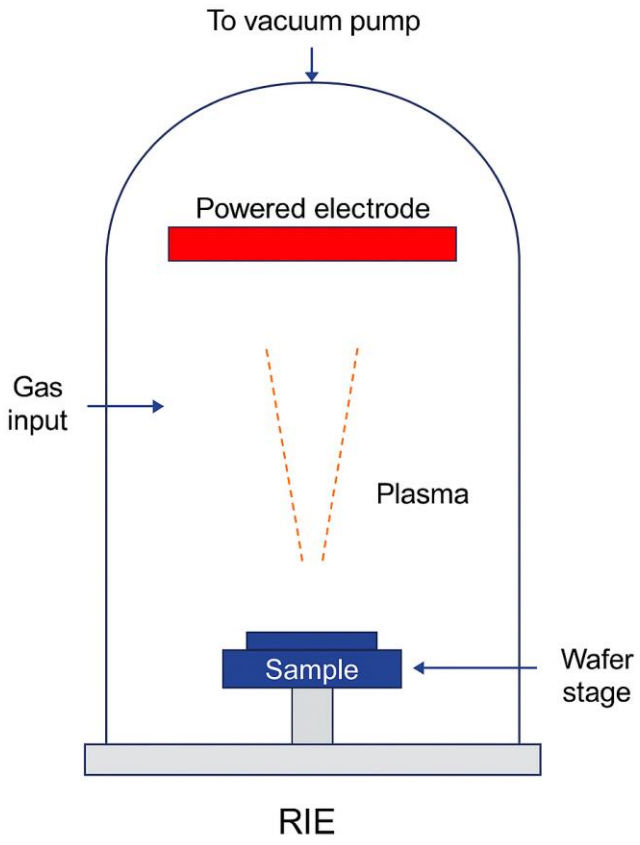


Figure 3.4 RIE dry etching

The fundamental mechanism of RIE involves both physical and chemical etching. Physically, the ions are accelerated by the electric field towards the substrate, where they physically bombard the surface, causing a sputtering

effect. Chemically, the reactive species in the plasma can react with the surface material.

Another commonly used dry etching method is ICP, which is a technology that generates plasma by using an inductively coupled electromagnetic field.

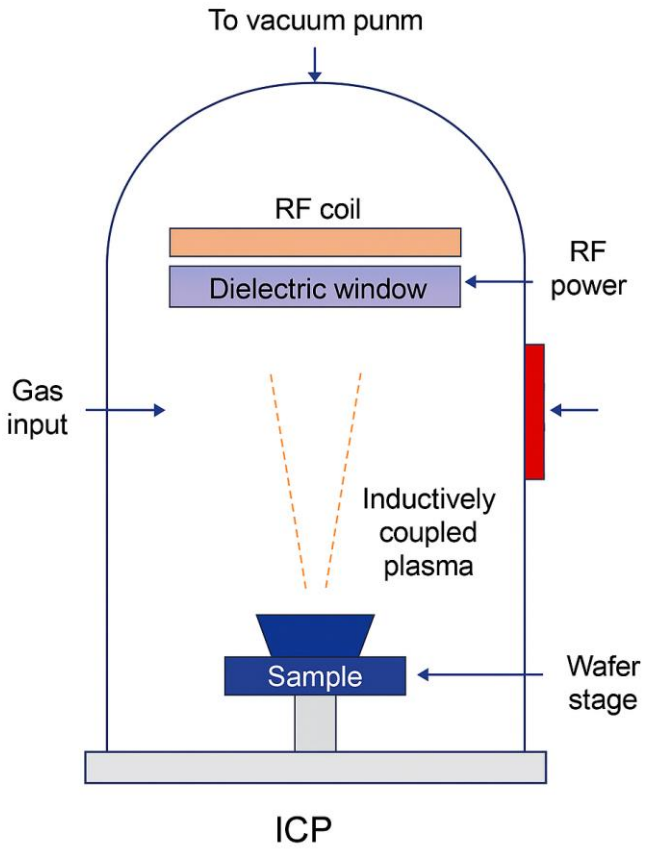


Figure 3.5 ICP dry etching

ICP is known for its high etch rates and the ability to control the directionality of the etch, which is critical for anisotropic profile transfer. The low ion energy also minimizes the physical damage to the substrate, which is particularly advantageous when processing delicate structures.

3.5 Ohmic and schottky metal deposition

Metallization is a crucial step in the fabrication process as it forms the contact to the AlGaN/GaN heterostructure. Metal deposition onto semiconductor wafers or samples can be carried out in several different ways including thermal evaporation, electron beam evaporation and sputtering.

3.5.1 Thermal evaporation

Thermal evaporation is one of the fundamental techniques employed in the deposition of metallic thin films. The core principle of this method revolves around heating the metal in a high-vacuum environment. Upon reaching its evaporation point, the material transforms into a vapor, which subsequently condenses onto a cooler substrate, resulting in a thin film. One of the primary advantages of this technique is its straightforwardness, coupled with the ability to achieve high-purity films. However, thermal vaporization faces challenges when dealing with materials that possess exceedingly high melting points, as the required temperatures might be difficult to attain. Additionally, achieving a uniform thickness, especially over expansive areas, can be problematic. Figure 3.6 shows the thermal evaporation system.

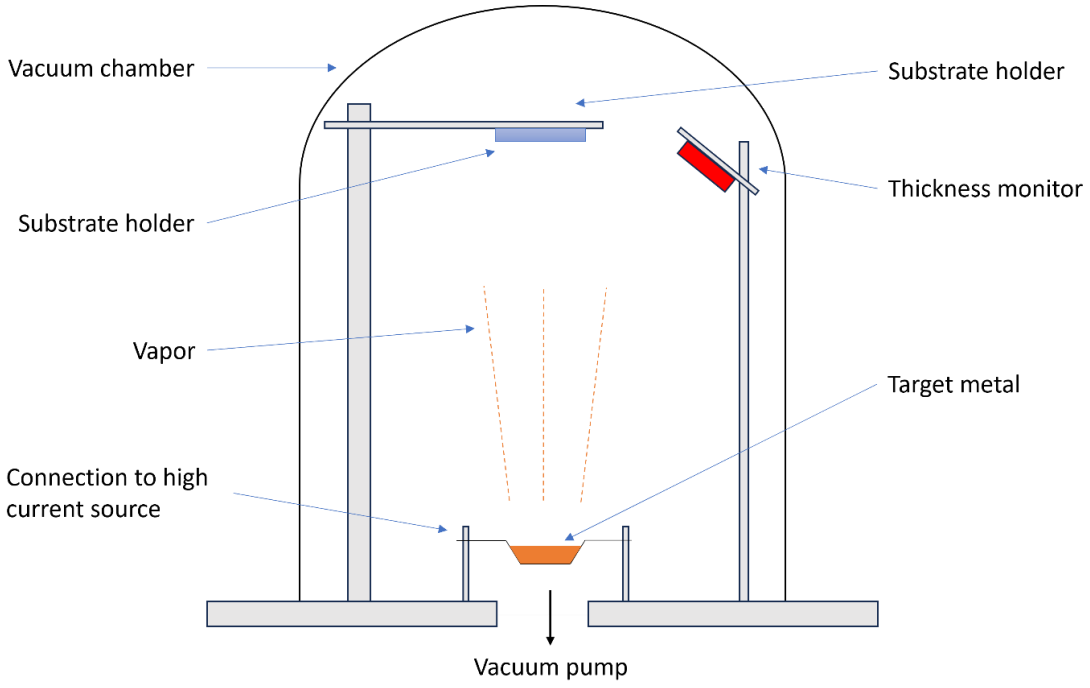


Figure 3.6 Thermal evaporation system

3.5.2 Sputtering

Sputtering stands out as a distinct metal deposition method due to its reliance on ionized gas, primarily argon, to instigate the deposition process. The gas ions, when directed at a target material, result in atomic ejections from the target. These atoms subsequently form a thin film upon encountering a substrate. Sputtering's versatility is evident in its ability to cater to a diverse range of materials, offering excellent step coverage, which makes it exceptionally suitable for substrates with intricate topographies. Moreover, the films generated through sputtering often exhibit commendable adhesion properties to the substrate. However, the deposition rates in sputtering are characteristically slower in comparison to the evaporation techniques. The sputtering process is shown in figure 3.7.

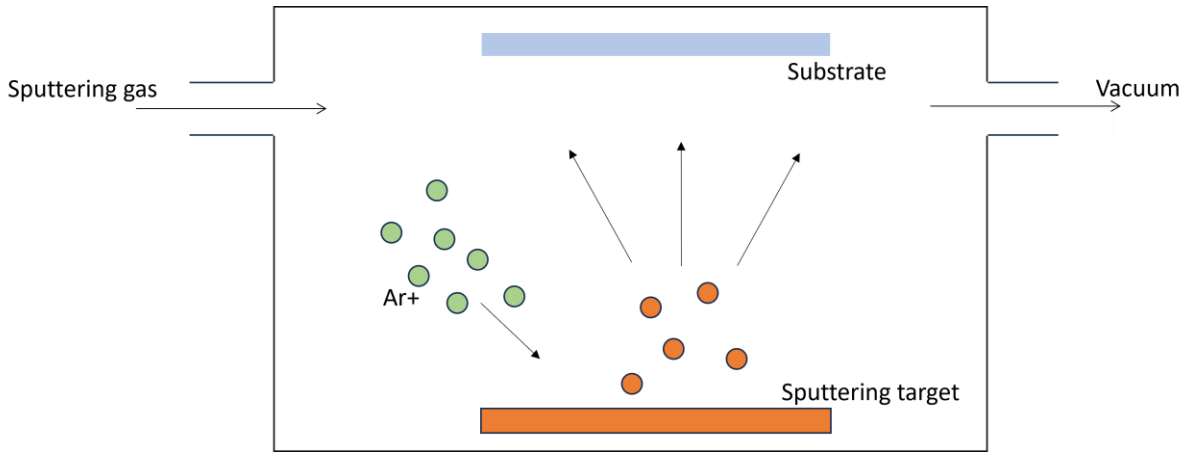


Figure 3.7 Sputtering

3.5.3 E-beam evaporation

A more sophisticated technique, e-beam vaporization, employs an electron beam (e-beam) directed onto the material intended for deposition. The kinetic energy from the electrons results in the heating and eventual evaporation of the target material. This vapor then follows a trajectory similar to thermal vaporization, condensing onto a substrate to form a film. Electron beam evaporation offers a distinct advantage in its ability to evaporate materials that are otherwise resistant to thermal evaporation due to their high melting points. This method also provides enhanced control over deposition rates and is

capable of producing films of superior quality and density. Figure 3.8 shows the e-beam evaporation.

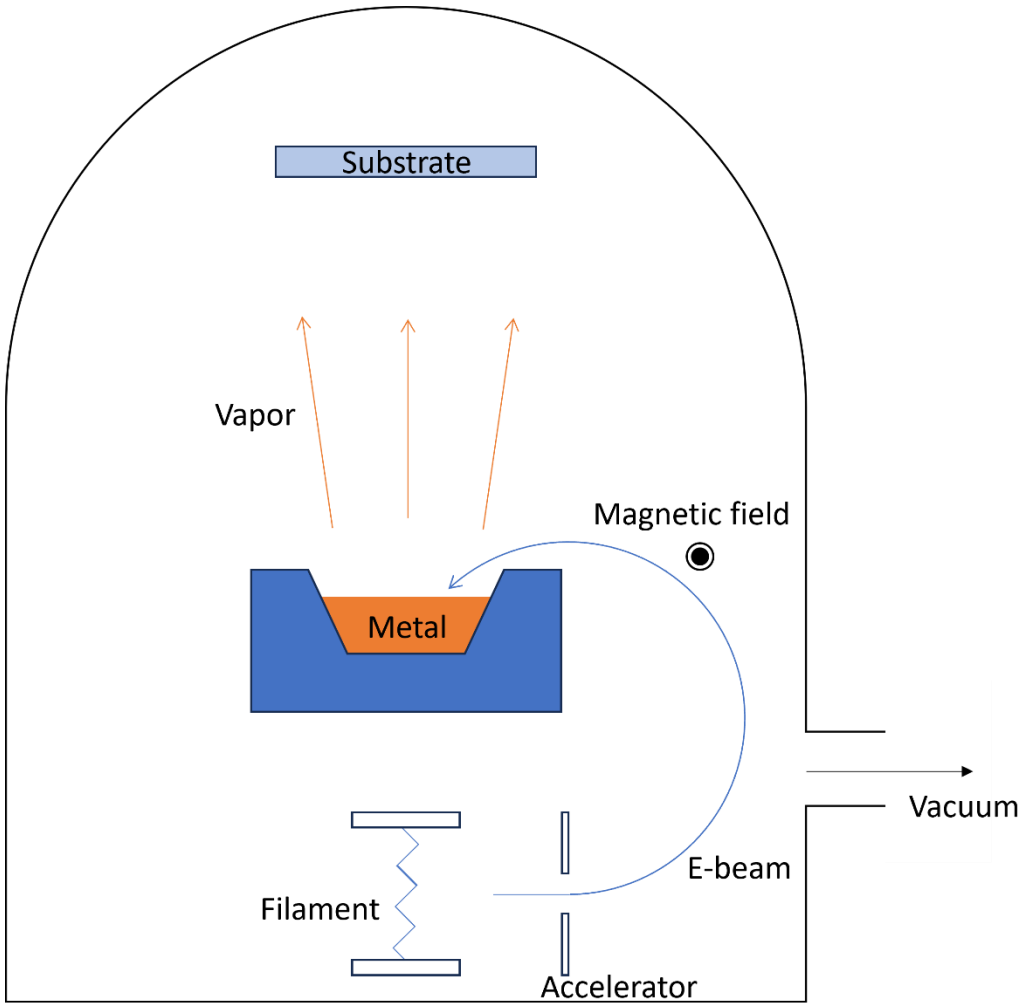


Figure 3.8 E-beam evaporation

For ohmic contacts, a metal stack of Ti(30nm)/Al(180nm)/Ni(40nm)/Au(100nm) is deposited onto the etched surface. The choice of this metal stack is based on its work function and compatibility with the AlGaN/GaN material, enabling low-resistance ohmic contacts.

For Schottky contacts, a metal stack of Ni(20nm)/Au(200nm) is deposited onto the mesa surface. The Schottky metal stack is carefully chosen to achieve the desired Schottky barrier height, a critical parameter in diode performance.

3.5.1 Lift-off technique

The lift-off process is a crucial step in the fabrication of AlGaN/GaN Schottky diodes, enabling precise metal definition without damaging the underlying epilayers. A bilayer resist structure composed of LOR 10A and S1805 was used to facilitate an undercut profile for successful liftoff. During development, the exposed S1805 layer is removed, along with the underlying LOR 10A. Due to the differential solubility and bake conditions, a natural undercut is formed at the interface, which is essential to prevent metal fence formation during liftoff. The metal stack (Ti/Al/Ni/Au for ohmic contacts and Ni/Au for Schottky contacts) is then deposited over the entire wafer, covering both the patterned S1805 and surrounding LOR10. The crucial step is the lift-off process, where the wafer is immersed in a solvent that dissolves the LOR10 layer, causing the overlying metal to lift off and detach from the substrate. This results in the desired metal pattern, precisely defined on top of the S1805 resist, facilitating the fabrication of well-defined metal contacts and interconnections for high-performance electronic devices. This process is illustrated in figure 3.9.

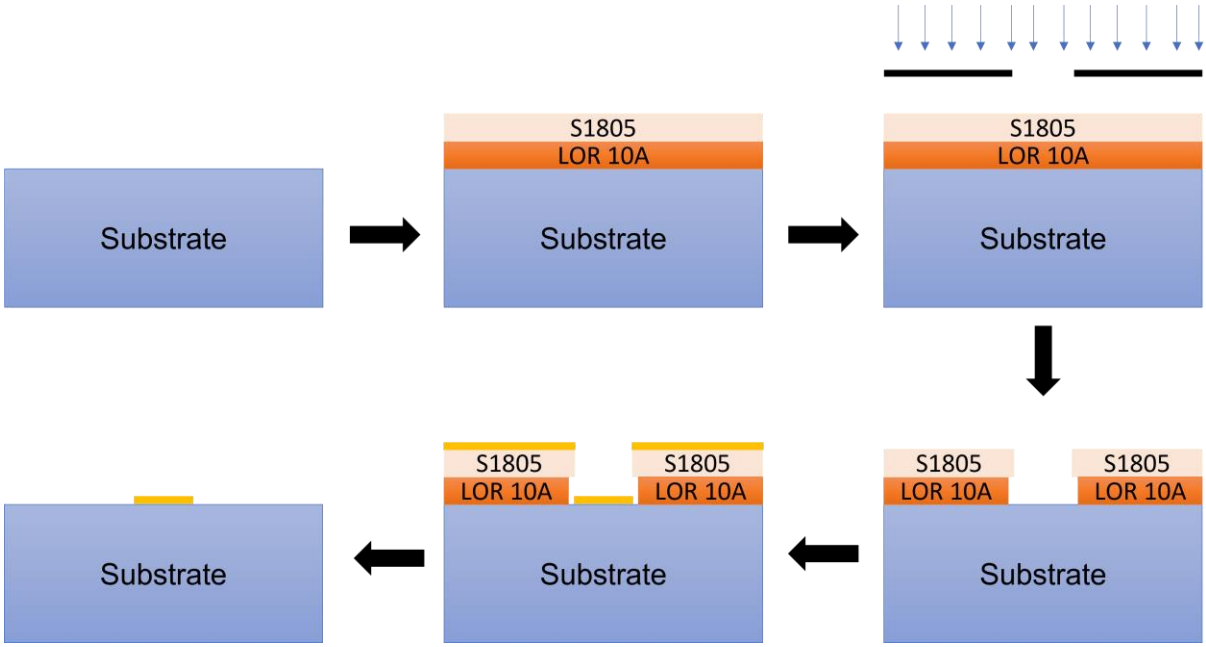


Figure 3.9 Lift-off process

3.6 Annealing

Following metallization, a rapid thermal annealing process is performed to improve the metal-semiconductor interface and reduce contact resistance. The annealing in this work is conducted at a temperature of 830°C for 30 seconds, ensuring the formation of stable and low-resistance contacts.

3.7 Marker metal deposition

In this work, Ti/Pt metal stacks were deposited on the wafer surface as alignment markers to assist in precise alignment during subsequent lithography steps. These markers are essential for multi-step processes such as mesa etching, ohmic metal, and Schottky gate patterning.

Titanium was chosen due to its strong adhesion to GaN, high thermal stability, and low diffusivity, making it ideal for use in high-temperature processes. Platinum, layered above Ti, enhances visibility under optical and SEM inspection. In contrast, alternative metals such as Au are prone to diffusion and contamination during annealing, while Al has a low melting point and poor resistance to standard etchants.

3.8 Diode fabrication flow

The complete device fabrication process is illustrated in Figure 3.5, showing the step-by-step integration of alignment marks, ohmic contacts, mesa isolation, and Schottky gate metallisation.

The process began with the deposition of alignment markers (Ti/Pt) using photolithography and liftoff. Next, the ohmic contact metal stack Ti (30 nm) / Al (180 nm) / Ni (40 nm) / Au (100 nm) was deposited and patterned to form the cathode contacts, followed by rapid thermal annealing.

After ohmic contact formation, a mesa isolation etch was performed using RIE, defining the device active area. A passivation layer of SiN was then

deposited to reduce surface states and leakage current. Via holes were opened in the SiN using photolithography and dry etching.

Finally, a Schottky contact (Ni/Au) was deposited over the AlGaN surface, completing the diode structure. The schematic steps of this process are shown in Figure 3.10.

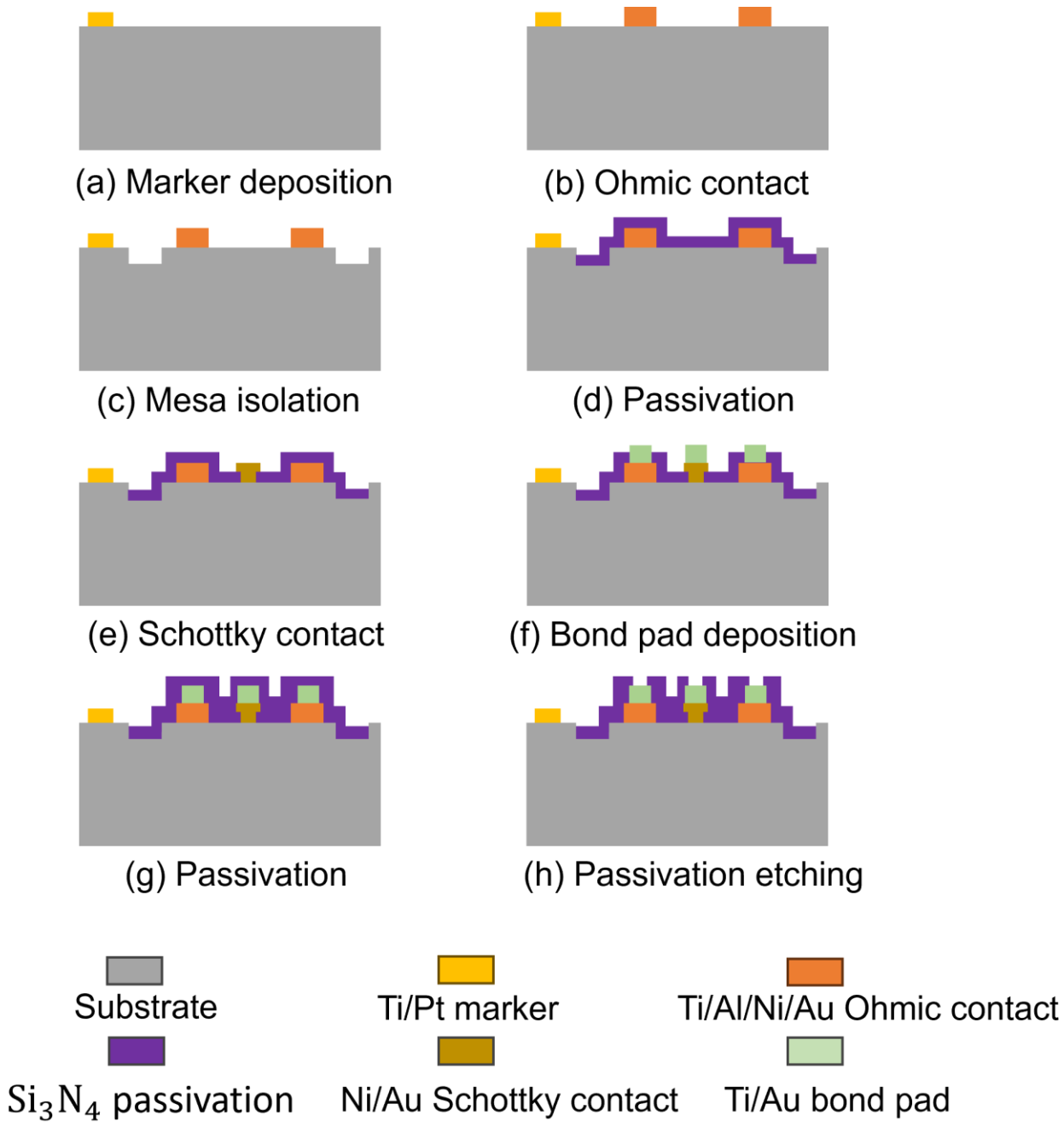


Figure 3.10 Main fabrication steps

3.9 Device characterization

After the completion of the fabrication process, the AlGaN/GaN Schottky diodes undergo thorough device characterization to evaluate their electrical and RF performance. Device characterization is a critical step in the development of electronic devices as it provides valuable insights into the device's behaviour and functionality under different operating conditions.

3.9.1 DC Current-Voltage (I-V) Measurements

One of the primary electrical characterizations performed on the fabricated Schottky diodes is the current-voltage (I-V) measurement. I-V measurements are conducted to understand the diode's electrical behaviour and to determine key parameters such as the ideality factor, Schottky barrier height, series resistance, and reverse breakdown voltage.

I-V measurements are typically carried out using a semiconductor parameter analyzer. During the measurement, a bias voltage is applied across the Schottky diode, and the resulting current is recorded. The process is repeated for different bias voltages to establish the current-voltage characteristic curve.

From the I–V curve, the ideality factor (n) can be extracted, which provides insight into the nature of carrier transport mechanisms across the Schottky diode interface. The ideality factor is also related to the effective barrier height of the device.

Figure 3.11 depicts the I-V curve of the diode. A diode primarily conducts when a forward bias is applied. This conduction starts appreciably at a voltage termed the 'forward voltage' (V_{on}). When reverse biased, an ideal diode would exhibit no current flow. However, in practical diodes, a small reverse saturation current does exist due to minority carriers. As the magnitude of the reverse bias increases, this current remains nearly constant until reaching a point called the 'breakdown voltage' (V_{br}), Beyond this voltage, the diode enters a breakdown region where the reverse current rises sharply. Depending on the nature and

design of the diode, this breakdown might be destructive or a utilized characteristic.

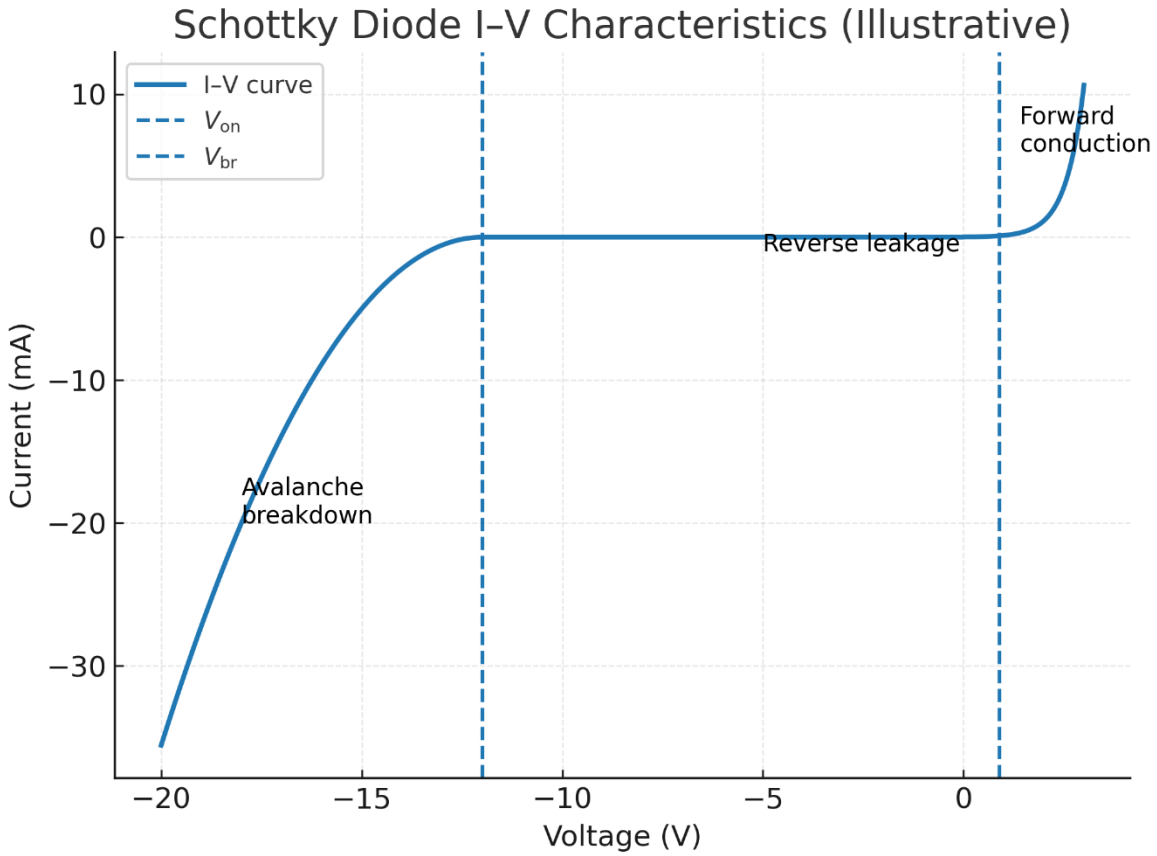


Figure 3.11 Diode I-V curve

3.9.2 RF characterization

RF characterization of the AlGaN/GaN Schottky diodes is essential to assess their performance in high-frequency applications. RF measurements are conducted to determine key parameters such as the S-parameters, cut-off frequency.

S-parameters are crucial for characterizing the diode's RF behaviour, as they describe the relationship between incident and reflected RF waves at the diode's terminals. S-parameters provide information about the diode's transmission, reflection, and scattering characteristics, enabling the design and optimization of RF circuits and systems.

In this work, RF measurements were performed using a Keysight Performance Network Analyzer (PNA) N5227A, covering a frequency range from 100 MHz to 50 GHz. A Short-Open-Load-Thru (SOLT) calibration was carried out at the probe tips. The main purpose of this calibration is to remove the effects of the measurement infrastructure—including cables, probe arms, and connectors—by shifting the reference planes directly to the device terminals. This ensures that the extracted S-parameters accurately represent the intrinsic response of the device under test (DUT).

Figure 3.12 shows the actual calibration standards (Short, Open, Load, and Thru) used in this work, captured under an optical microscope. These standards are patterned on a commercial GSG calibration substrate with a 150 µm pitch, matching the RF probe pitch for minimal mismatch. This ensures high confidence in the accuracy and repeatability of S-parameter extraction across the 100 MHz–50 GHz frequency range.

Figure 3.12 Optical microscope images of the SOLT (Short, Open, Load, Thru) calibration standards used for RF on-wafer calibration

Representative optical micrographs of the fabricated **2-finger** and **4-finger** SBDs are shown in figure 3.13, highlighting the Schottky anode finger array, ohmic cathode pad and CPW pad geometry used for on-wafer S-parameter measurements (100 MHz–50 GHz).

From left to right: the CPW signal feed, the Schottky anode with two fingers (Ni/Au over AlGaN within the passivation opening), and the ohmic cathode pad (Ti/Al/Ni/Au) at the mesa edge. The blue-tinted region corresponds to the passivated/mesa area; fingers were patterned by E-beam lithography and contacted in a 50 Ω CPW layout compatible with 150 µm-pitch GSG probes. Design values used in this work: junction length Lj=4 , anode width W=10 µm.

Figure 3.13 Optical micrograph of 2-finger/ 4-finger AlGaN/GaN Schottky diode (GSG probing)

3.10 On-wafer de-embedding

In the field of RF and microwave engineering, accurate and reliable measurements of device performance are crucial for the design and characterization of high-frequency electronic components and systems. However, when measuring devices using on-wafer or on-chip techniques, the presence of parasitic elements and interconnects can significantly affect the measurement results, making it challenging to extract the true intrinsic performance of the device. This is particularly important when working with small and sensitive devices, such as AlGaN/GaN Schottky diodes, where parasitic effects can be more pronounced.

Calibration and de-embedding are two distinct but complementary steps in RF measurement. Calibration, performed using standards such as Short-Open-Load-Thru (SOLT) or Through-Reflect-Line (TRL), brings the reference plane forward from the VNA port to the probe tips. This process removes the effects of the measurement infrastructure, including cables, connectors, and probes, ensuring that the measured S-parameters are referenced at the probe tip.

De-embedding, on the other hand, extends the reference plane further from the probe tip to the device terminals. This step removes the parasitic effects introduced by contact pads, feedlines, and substrate contributions, thereby isolating the intrinsic response of the device under test (DUT). By combining calibration and de-embedding, the resulting measurements accurately capture

the true high-frequency performance of the DUT, enabling reliable parameter extraction and model validation.

Once the calibration data is acquired, various de-embedding algorithms and techniques can be employed to compensate for the parasitic effects. The most commonly used methods include S-parameter de-embedding, TRL de-embedding, and cascaded de-embedding techniques. These approaches help to remove the systematic errors and accurately extract the device's intrinsic S-parameters, impedance, and other relevant RF parameters.

As mentioned earlier, a pad structure was utilized during the fabrication process to connect the co-planar waveguide (CPW) probe to the device for measurement. Consequently, a de-embedding process is necessary to eliminate the parasitic parameters of the pads from the measurement results, thereby accurately revealing the RF performance of the device. To facilitate this, open and short structures of the pads were fabricated and subsequently measured.

To ensure accurate removal of parasitic effects introduced by probe pads and interconnects, dedicated open and short structures were designed and fabricated alongside the actual device. These structures mimic the layout of the CPW pads without the active device in between (for open) or with a direct metal bridge (for short), thereby enabling precise calibration under identical probing and measurement conditions.

Figure 3.14 presents optical microscope images of the fabricated open and short structures. These calibration references were used in the de-embedding process. Figure 3.15 shows the equivalent circuit of the open and short structures of the pads.

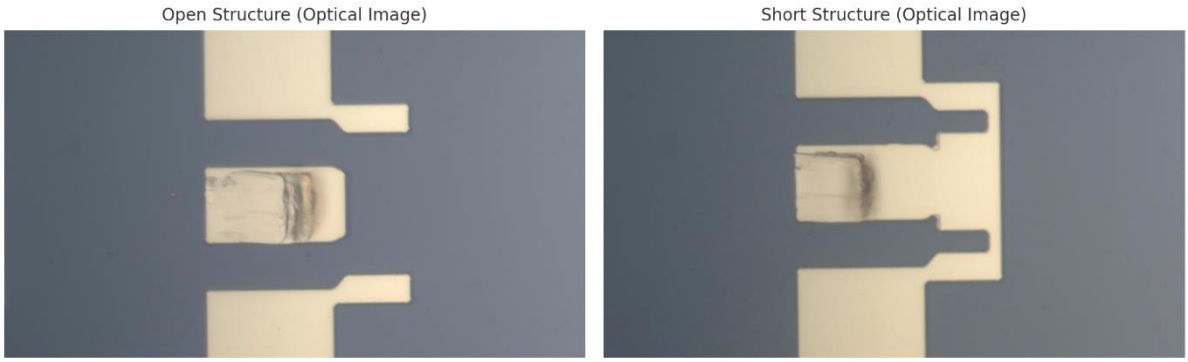


Figure 3.14 Optical microscope images of the fabricated open and short structures

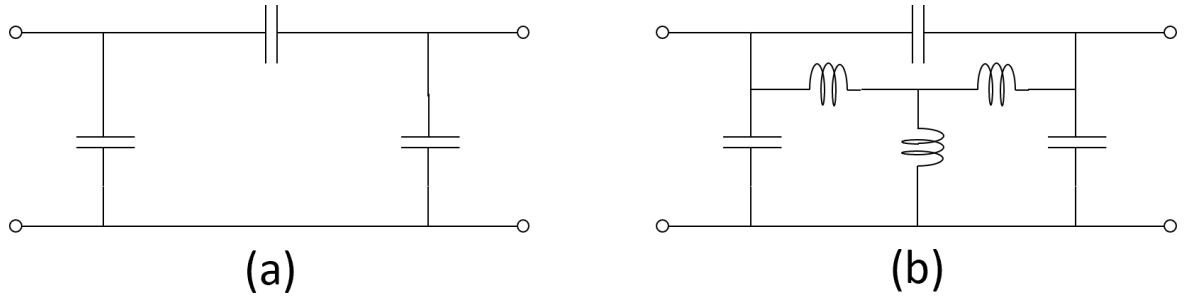


Figure 3.15 Equivalent circuit of (a) open structure, and (b) short structure

Based on the de-embedding technique theory from [72], the schematic principle of that is shown in figure 3.15. In this study, the device and two reference structures (open and short) were measured, and the resulting data were captured in the form of S-parameters. The open structure's measurement aids in the elimination of parasitic capacitance. For this purpose, the S-parameters of both the device and the open structure were converted to admittance parameters (Y-parameters), after which they were subtracted. To mitigate the effects of parasitic inductance, the S-parameters from the short structure and open structure measurements were also converted into Y-parameters and then subtracted. This derived parasitic inductance in Y-parameter form was then transformed into impedance parameters (Z-parameters). Following the removal of parasitic capacitance, the parasitic inductance was further removed in the Z-parameter domain. After these corrections, the true device characteristics were recalculated and converted back to S-parameters for further analysis.

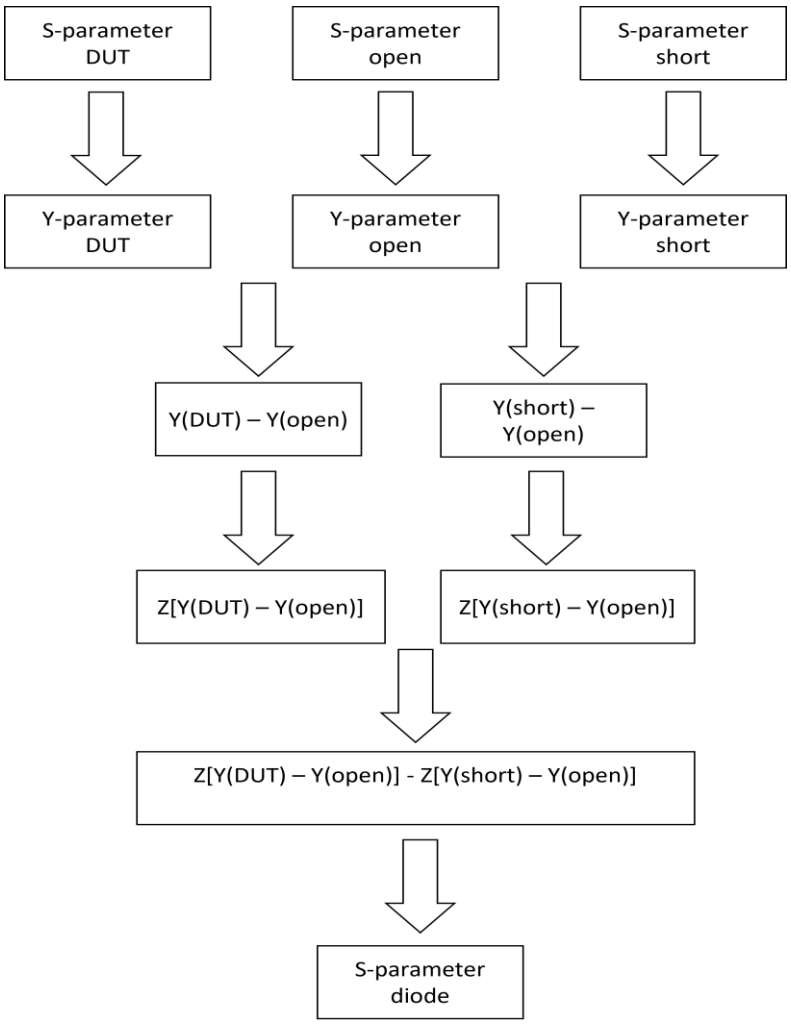


Figure 3.15 Schematic principle of de-embedding

3.11 Conclusion

This chapter has laid out the comprehensive fabrication process of AlGaN/GaN Schottky diodes, highlighting each step's significance in achieving efficient and reliable electronic devices for high-frequency and high-power applications. The integration of advanced epitaxial growth, lithography, etching, metallization, and characterization techniques continues to drive advancements in device design and optimization, leading to enhanced performance and reliability. As research in this field progresses, AlGaN/GaN Schottky diodes hold great promise for the future of electronics and RF engineering, opening up new possibilities for a wide range of applications.

The chapter also highlighted the importance of device characterization, particularly I-V and RF measurements, to evaluate the diode's electrical and RF performance. I-V measurements provided insights into the diode's electrical behavior, while RF measurements, such as S-parameters, offered a comprehensive understanding of its RF characteristics.

Moreover, the chapter discussed the significance of on-wafer de-embedding, a critical technique to remove unwanted effects from test fixtures and interconnects during measurements. De-embedding allowed researchers to accurately determine the intrinsic characteristics of the AlGaN/GaN Schottky diodes, ensuring reliable data for precise parameter extraction and model validation.

Chapter 4

Characterization of Diodes with Different Substrate Resistivity

4.1 Introduction

RF circuits are electronic circuits designed to operate at high frequencies, within which microwave circuits represent an important subset covering frequencies typically from 300 MHz to 300 GHz. These circuits are widely used in various applications, including wireless communication systems, radar systems, satellite communication, and many other electronic devices. The key difference between RF and microwave circuits lies in their frequency ranges and the specific technologies used to design and implement them. These circuits often require special design techniques and components to handle the high-frequency signals efficiently. Due to their unique properties, RF and microwave circuits are crucial for modern communication systems and play a vital role in enabling wireless connectivity and high-speed data transfer.

Diodes are essential components in RF and microwave circuits due to their nonlinear behaviour and frequency mixing capabilities. The performance of a diode is influenced by various parameters, including substrate resistivity, doping concentration, junction depth, and others. Extensive research has been conducted on high-performance transistors fabricated on high-resistivity Si substrates, as documented in [73]. Similarly, investigations on transistors utilizing low-resistivity Si substrates have been reported in previous works ([74] and [75]). However, the impact of substrate resistivity on the RF performance of AlGaN/GaN Schottky diodes remains relatively unexplored.

In this context, understanding the effect of substrate resistivity on the RF performance of AlGaN/GaN Schottky diodes is of paramount importance. The substrate resistivity plays a crucial role in determining the overall electrical characteristics and RF behaviour of these diodes. However, a comprehensive understanding of the relationship between substrate resistivity and RF performance is lacking, creating a research gap in this field.

To address this research gap, this chapter presents a thorough investigation into the RF characterization of AlGaN/GaN Schottky diodes with different substrate resistivity values. The characterization is accomplished through on-wafer S11 measurements, which provide insights into the diode's reflection coefficient and impedance matching properties. These measurements were performed using a state-of-the-art Vector Network Analyzer (VNA) in a controlled microwave probe station environment. The diodes under examination were mounted on a coplanar waveguide (CPW) transmission line with a 50 Ohm characteristic impedance, ensuring consistent and accurate measurement conditions.

The S11 measurements cover a wide frequency range from 100 MHz to 50 GHz, with a step size of 10 MHz. By systematically varying the substrate resistivity and observing the corresponding RF performance parameters, such as insertion loss, return loss, and bandwidth, a comprehensive understanding of the impact of substrate resistivity on the RF characteristics of AlGaN/GaN Schottky diodes can be attained. The obtained results will provide valuable insights for the design and optimization of these diodes for specific RF and microwave applications.

By addressing this research gap and uncovering the influence of substrate resistivity on the RF performance of AlGaN/GaN Schottky diodes, this chapter aims to contribute to the existing knowledge and facilitate further advancements in the field of high-frequency semiconductor devices.

4.2 Wafer and substrate characteristics

To comprehensively investigate the impact of substrate resistivity on the RF performance of AlGaN/GaN Schottky diodes, two different wafers were carefully selected for device fabrication. The choice of substrates played a crucial role in studying the influence of substrate resistivity on the diode characteristics. The first wafer utilized a low-resistivity silicon (Si) substrate with a resistivity of less than 0.03 Ω·cm, while the second wafer used a high-resistivity Si substrate with a resistivity exceeding 5000 Ω·cm. By utilizing substrates with significantly different resistivity values, it was possible to examine the direct correlation between substrate resistivity and the resulting RF performance of the fabricated diodes.

Apart from the substrates, the epitaxial layers of both wafers were identical, ensuring consistent material properties and layer structures. The epitaxial layers began with a base layer of Gallium Nitride (GaN) measuring 2 µm in thickness, providing the foundation for subsequent layers. On top of the GaN layer, a thin layer of Aluminium Nitride (AlN) with a thickness of 1 nm was deposited, serving as an interfacial layer to enhance the quality of the heterostructure. Following the AlN layer, there was a precisely engineered layer of Aluminium Gallium Nitride (AlGaN) with a thickness of 9 nm and an Aluminium content of 32%. This carefully controlled composition of AlGaN allowed for tailoring the material's properties, such as bandgap and carrier mobility, which directly influence the RF performance of the diodes. Finally, a 2 nm thick GaN cap layer was added to serve as a protective coating on the top surface, safeguarding the underlying layers during device fabrication and operation.

The layer structure described above, with its specific material composition and thicknesses, was replicated on both wafers to ensure a comparative analysis of the RF performance while isolating the impact of substrate resistivity. Figure 4.1 visually presents the layer structure of the fabricated AlGaN/GaN Schottky

diodes, illustrating the successive layers from the substrate to the protective cap layer.

By systematically exploring the RF characteristics of diodes fabricated on substrates with varying resistivity, this study aims to provide valuable insights into the relationship between substrate resistivity and the resulting RF performance parameters, such as insertion loss, return loss, and bandwidth. Through a detailed analysis of the experimental data, a comprehensive understanding of how substrate resistivity influences the performance of AlGaN/GaN Schottky diodes can be attained, enabling optimized device design and enhanced performance for various RF and microwave applications.

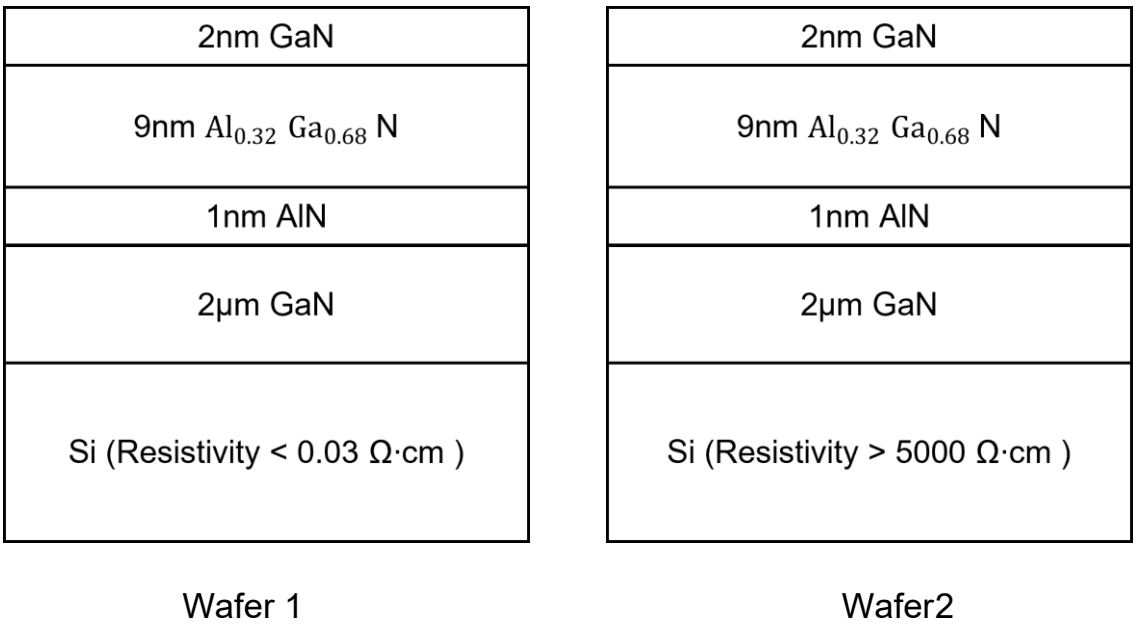


Figure 4.1 Epitaxial wafer structure of compared substrates

Two-finger and four-finger devices were meticulously designed and fabricated on both wafers to assess the impact of the number of anode fingers on the diode's RF performance. Figure 4.2 illustrates a simplified top view of the fabricated devices, highlighting the respective arrangements of the anode fingers in the two-finger and four-finger configurations. The junction length (L_j) was set at 4 μm, ensuring consistent junction characteristics across the fabricated diodes. For both types of devices, the anode length (L_A) was maintained at 250 nm, while the anode width spanned 10 μm.

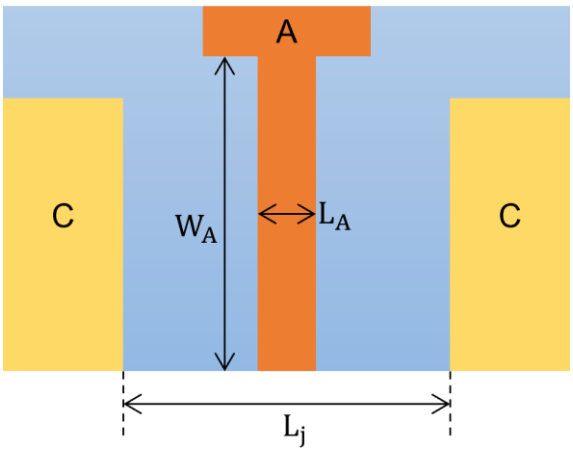


Figure 4.2 Simplified top view of devices

4.3 Measurement result and parameters extraction

Return loss of the open CPW lines was measured as a one-port setup on a PNA after 150-μm GSG SOLT calibration; short/open standards were fabricated on-wafer for de-embedding. The measured |S11| responses (Fig. 4.3) clearly separate the two cases: the high-resistivity Si CPW maintains a reflection magnitude closer to 0 dB across the band, indicating lower substrate loss, whereas the low-resistivity Si CPW shows a progressively more negative |S11| with frequency, consistent with increased dielectric and conduction losses in the lossy substrate. These measurements verify that substrate resistivity has a pronounced impact on the RF scattering behaviour of CPW structures and, by extension, the devices measured through them.

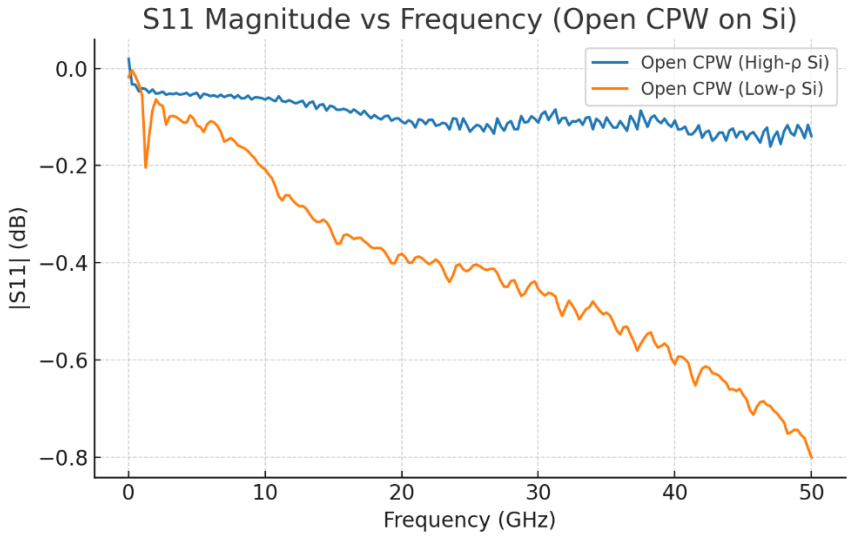


Figure 4.3. Return loss of open CPW transmission line

After confirming the substrate resistivity, it was crucial to ensure the functionality of the fabricated diodes. To achieve this, a comprehensive DC measurement was conducted for all diodes. This step aimed to evaluate the electrical characteristics of the diodes. By performing these DC measurements, we could ascertain the operational integrity and reliability of the fabricated diodes. This thorough assessment provided valuable insights into the diodes' performance and served as a necessary validation step before proceeding with further RF characterization and analysis. And the results are shown in figure 4.4.

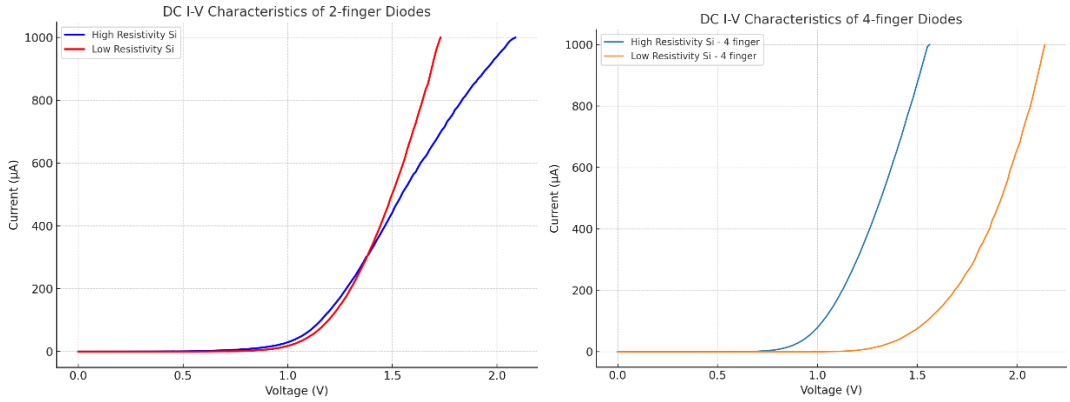


Figure 4.4. DC measurement of fabricated diodes: (a) 2-finger, (b) 4-finger diode

For the 2-finger pair, the faster rise of the low-resistivity-substrate I–V is consistent with a modest reduction in lateral series resistance and a slightly lower effective SBH due to local metal thickness/roughness variations at the Schottky edge; both effects increase forward conduction at a given bias. For the 4-finger pair, the larger turn-on disparity is plausibly driven by cumulative lithographic/overlay variation across the wider anode array (effective area and edge field non-uniformity), together with finger-to-pad parasitic differences that alter current crowding.

On-wafer RF measurements were conducted to assess the RF performance of the fabricated diodes, and the results were obtained. To accurately evaluate the

intrinsic performance of the diodes, the measured data underwent de-embedding to eliminate the influence of the transmission lines and other extraneous elements. This de-embedding process effectively isolated the RF characteristics of the diodes themselves, enabling a more precise analysis of their performance. Figure 4.5 presents the plotted results of the de-embedded RF measurements for the two 2-finger diodes. The parameters of interest, return loss, were carefully analysed.

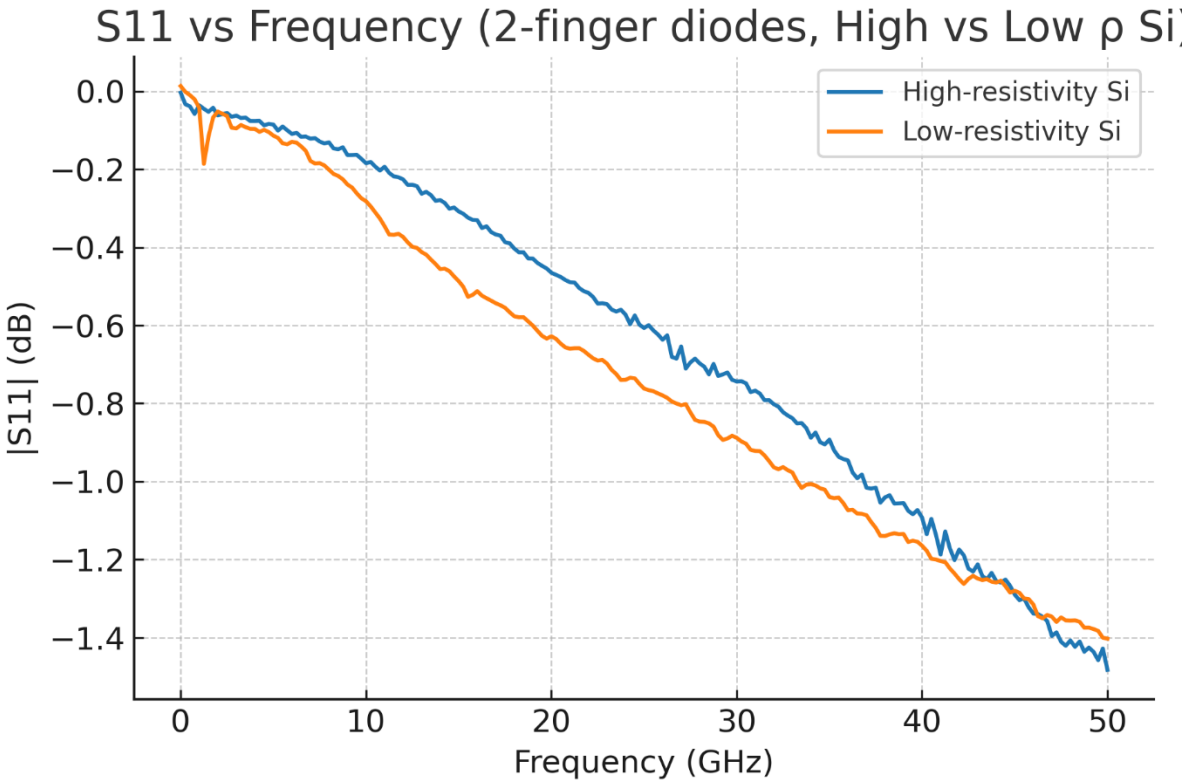


Figure 4.5 Return loss of 2-finger diodes on different substrate

From the observed results in Figure 4.5, a noticeable trend can be discerned regarding the reflection coefficient of the two diodes. Diode 1 (blue line), fabricated on the high-resistivity substrate, exhibits a higher magnitude of reflection coefficient (lower return loss) compared to Diode 2 on the low-resistivity substrate across most of the measured frequency range. However, at

higher frequencies (45 GHz - 50 GHz), Diode 2 shows a higher reflection coefficient than Diode 1.

To delve into the factors influencing these measurement results, an in-depth analysis of the Schottky diode's various parameters is conducted using an equivalent circuit model, as depicted in Figure 4.6. Within this model, it is important to note that C_{sub} and R_{sub} represent parameters associated with the transmission line and will be effectively eliminated during the subsequent de-embedding process. By extracting the remaining parameters, such as junction capacitance, junction resistance, and series resistance, we aim to uncover the underlying factors contributing to the observed RF performance differences between the diodes on high and low-resistivity substrates. The subsequent analysis will shed light on the correlation between these extracted parameters and the diodes' RF performance, aiding in the optimization and design of high-performance Schottky diodes for various RF and microwave applications.

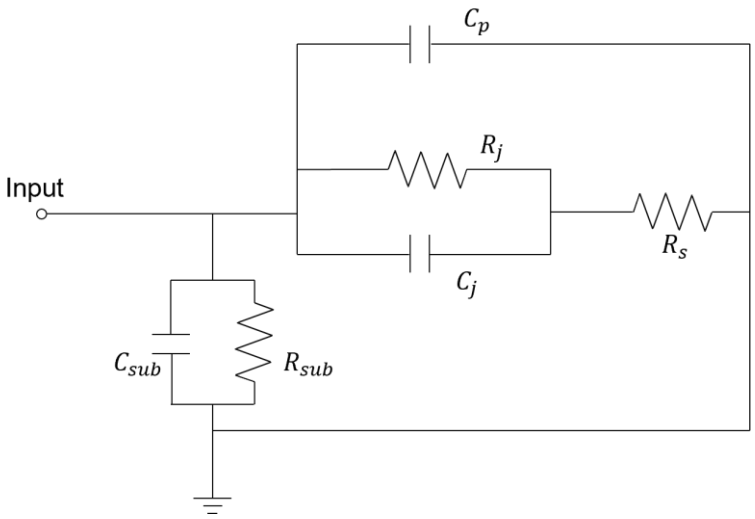
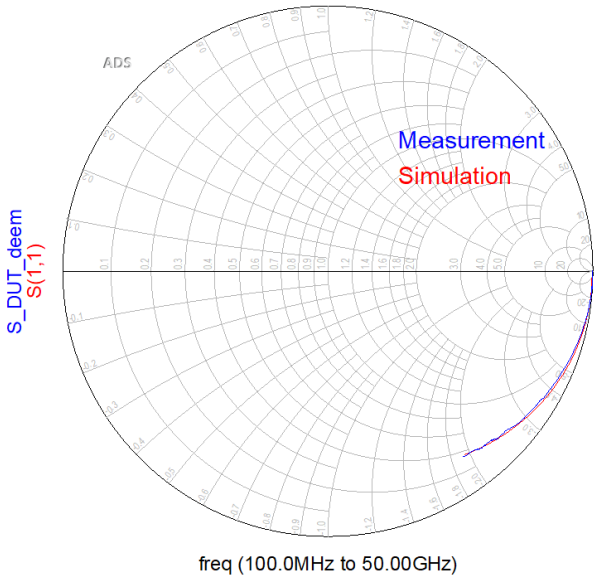


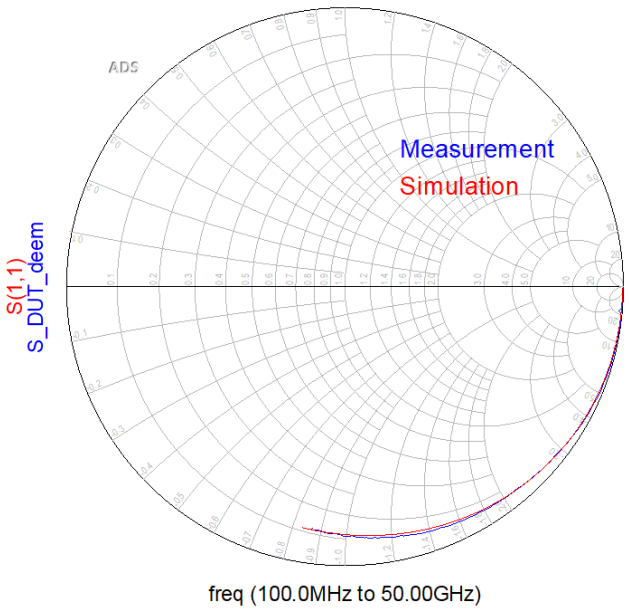
Figure 4.6 Schottky diode small-signal equivalent circuit model

The values of the extracted parameters, including junction capacitance (C_j), junction resistance (R_j), series resistance (R_s), and parasitic capacitance (C_p), for both Diode 1 and Diode 2 are summarized in Table 4.1. These parameters were determined through careful analysis and modelling of the measured data.

To validate the accuracy of the model, the measured and modelled S11 (reflection coefficient) for both devices are plotted in Figure 4.7. The comparison between the measured and modelled S11 curves serves as a crucial step in verifying the precision of the developed equivalent circuit model. The close agreement between the measured and modelled results further confirms the reliability and accuracy of the extracted parameters.



(a) S11 for diode 1



(b) S11 for diode 2

Figure 4.7 Measured and modelled S11 for (a) diode 1 and (b) diode 2

Table 4.1 Extracted parameters for 2-finger diodes

	C_j (fF)	R_j (kΩ)	R_s (Ω)	C_p (fF)
Diode 1 (high resistivity substrate)	15.02	66.06	90.6	19.2
Diode 2 (low resistivity substrate)	19.36	81.3	102.4	15

To evaluate the overall capacitance of the diode, the total capacitance (C) can be calculated using Equation 4.1, which combines the junction capacitance ($\mathrm{C_j}$) and the parasitic capacitance ($\mathrm{C_p}$). By applying this equation, it is determined that the calculated total capacitance of Diode 1 is approximately 0.4% lower than that of Diode 2.

These findings highlight the influence of substrate resistivity on various key parameters of the diode, such as series resistance, junction capacitance, and parasitic capacitance. The differences observed in these parameters contribute to the distinct RF performance characteristics exhibited by the diodes on different substrate resistivities.

$$C = C_j + C_p \tag{4.1}$$

The series resistance ($\mathrm{R_s}$) of the diodes is primarily influenced by the two-dimensional electron gas (2DEG) formed between the AlGaN and GaN layers. A higher resistivity substrate provides better isolation, reducing electron scattering and enhancing electron mobility within the 2DEG. This improved mobility leads to higher electron density and lower sheet resistance, resulting in lower $\mathrm{R_s}$.

In terms of RF performance, resistance plays a more significant role at lower frequencies compared to capacitance. The lower R_s in diode 1 contributes to its superior performance in terms of return loss, as indicated by the measurements. On the other hand, diode 2, fabricated on a low-resistivity substrate, exhibits higher capacitance, as observed in Table 4.1. Higher capacitance results in less return loss at higher frequencies.

Therefore, the observed difference in return loss between diode 1 and diode 2 can be attributed to the combined effects of series resistance and capacitance. The higher resistivity substrate of diode 1 contributes to lower series resistance, leading to better RF performance at lower frequencies. Conversely, diode 2 on the low-resistivity substrate exhibits higher capacitance, resulting in improved RF performance at higher frequencies.

To study the RF losses of different substrates, the coplanar waveguide (CPW) transmission line was designed and simulated in HFSS as shown in figure 4.8. The signal width (w) was designed to be 250nm, and the gap (s) was 2 micrometre.

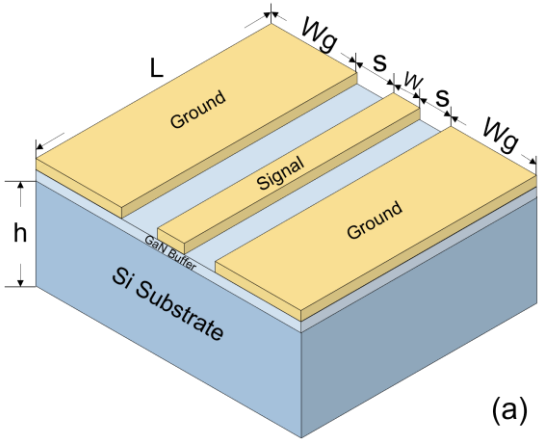
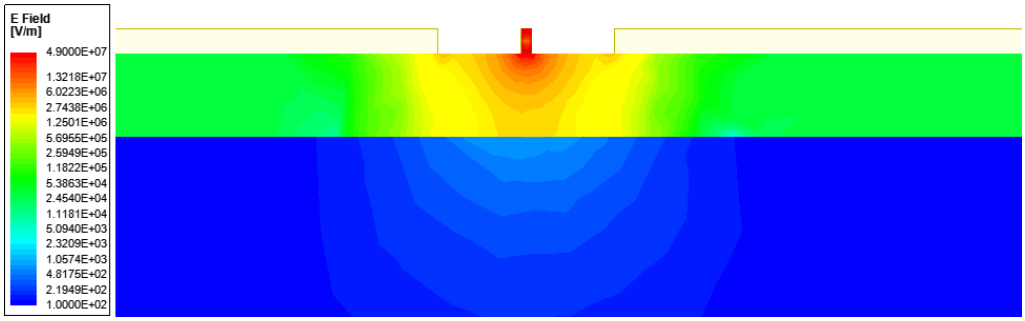


Figure 4.8 CPW structure

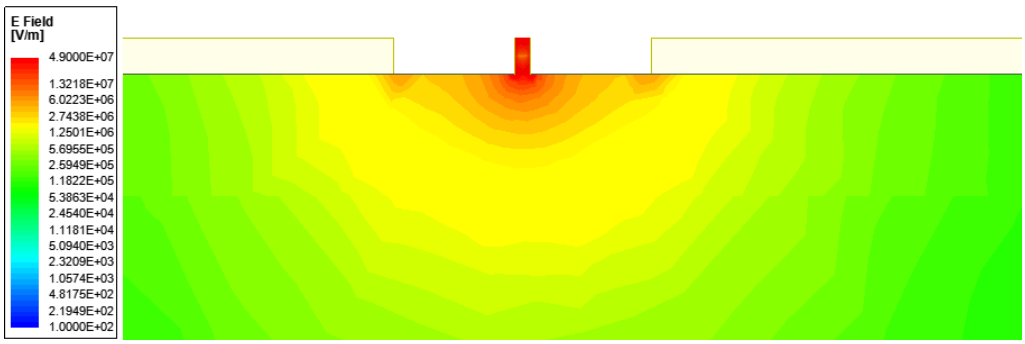
Figure 4.9 shows the simulation results of the electric field distribution within substrates with different resistivity at 50GHz. It can be found that the electric field in high-resistivity Si penetrate deeper into the substrate than that in low-resistivity sub. This simulation indicates that when the gap between electrodes

is small enough (2 micrometre in this case), the electric field distribution is primarily concentrated in the GaN buffer layer instead of penetrating into the substrate. This phenomenon might be helpful for minimizing the effects of a lossy substrate.

Measurements were performed on 4-finger diodes to further validate the observed phenomenon. Figure 4.10 displays the measurement results for diode 3, which uses a high-resistivity Si substrate, and diode 4, which uses a low-resistivity Si substrate. These measurements provide additional insights into the effect of substrate resistivity on the RF performance of the diodes.



(a) Electric field distribution within the low-resistivity Si substrate



(b) Electric field distribution within the high-resistivity Si substrate

Figure 4.9 Electric field distribution within different substrates

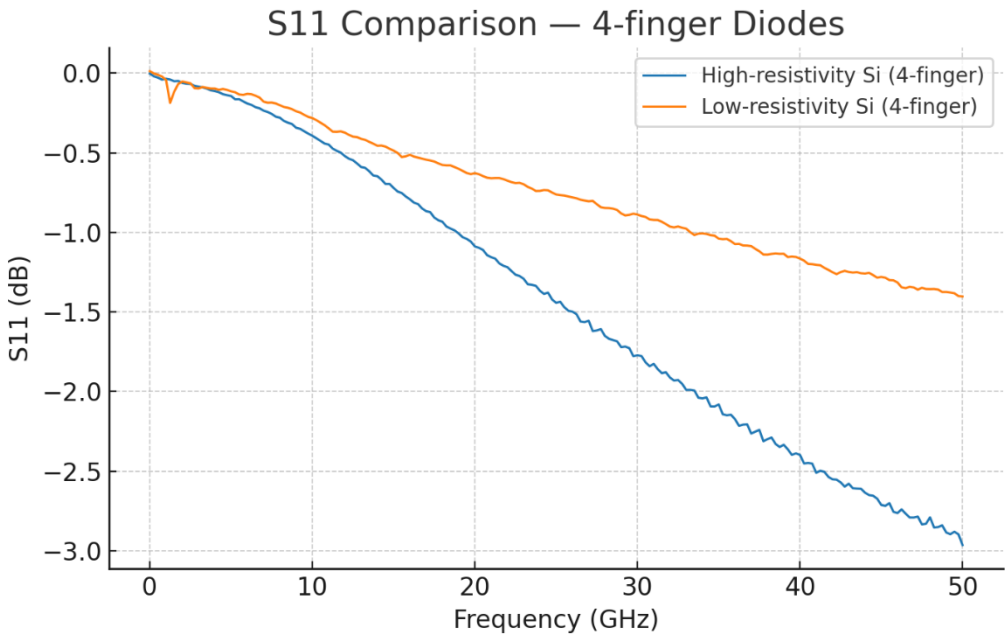
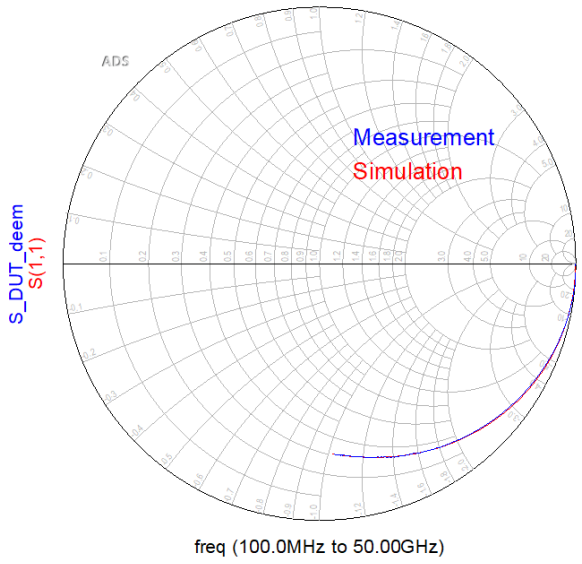
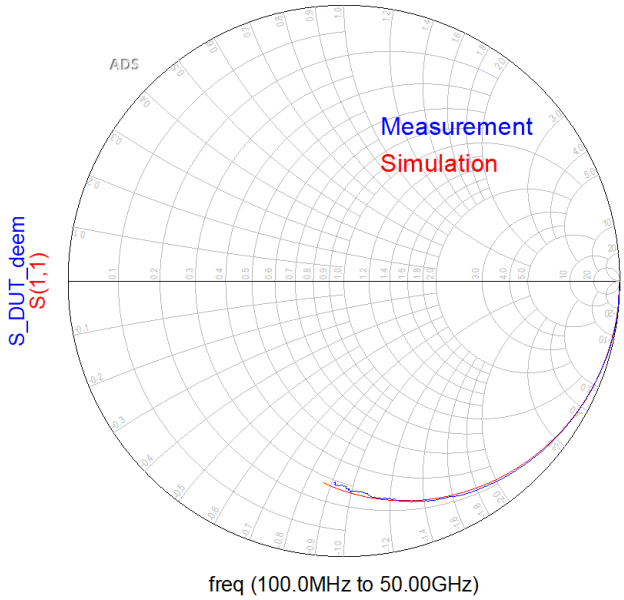


Figure 4.10 Return loss of 4-finger diodes on different substrate

To gain a deeper understanding, simulation results are presented in Figure 4.11, showcasing the agreement between the measured and simulated S11 responses for both diodes. Additionally, the extracted parameters for diode 3 and diode 4 are summarized in Table 4.2.



(a) S11 for diode 3



(b) S11 for diode 3

Figure 4.11 Measured and modelled S11 for (a) diode 3 and (b) diode 4

Table 4.2 Extracted parameters for 4-finger diodes

	C_j (fF)	R_j (KOhm)	R_s (Ohm)	C_p (fF)
Diode 3 (high resistivity substrate)	36	66.06	65.8	34
Diode 4 (low resistivity substrate)	30.7	81.3	72.4	45

Table 4.2 provides valuable insights into the differences between diode 3 and diode 4 in terms of their extracted parameters. Comparing the values, it is observed that diode 3, fabricated on a high-resistivity Si substrate, exhibits a lower series resistance (R_s) and parasitic capacitance (C_p) compared to diode 4, which is fabricated on a low-resistivity Si substrate. Specifically, R_s of diode

3 is approximately 9.1% lower than diode 4, indicating improved electron mobility within the 2DEG formed between AlGaN and GaN. Additionally, C_p of diode 3 is approximately 24% lower than diode 4, indicating reduced parasitic effects.

On the other hand, diode 3 demonstrates a slightly higher junction capacitance (C_j) compared to diode 4. This can be attributed to the influence of the different substrate resistivity levels on the carrier concentration and electrical properties of the diodes.

Considering the calculated total capacitance values, diode 3 exhibits a total capacitance of approximately 70fF, while diode 4 has a total capacitance of approximately 75.7fF. This shows that the total capacitance of diode 3 is approximately 7.5% lower than diode 4. The lower series resistance and total capacitance of diode 3 contribute to its improved S11 performance at lower frequencies (0 - 12 GHz), as depicted in Figure 4.6. However, at higher frequencies (12 GHz - 50 GHz), diode 4 shows a better S11 response due to its higher total capacitance.

The simulation results and extracted parameters provide quantitative evidence supporting the impact of substrate resistivity on the RF performance of the 4-finger diodes. The comparison between diode 3 and diode 4 reveals similar trends as observed in the 2-finger diodes, reaffirming the significance of substrate resistivity in determining the device characteristics.

Table 4.3 presents the comparison of key parameters, namely series resistance (R_s) and total capacitance (C_{total}), between the 2-finger and 4-finger devices.

Table 4.3 Parameter differences of devices

	R_s	C_{total}
2-finger devices	11.5%	0.4%
4-finger devices	9.1%	7.5%

In Table 4.3, it can be observed that the resistance difference of the 4-finger devices is smaller than the 2-finger devices, while the capacitance difference has significantly increased. The differences in these parameters are well demonstrated in Figure 4.3 and Figure 4.6 as well. Lower resistance difference leads to smaller return loss difference at low frequency. Meanwhile, higher capacitance difference results in increased return loss difference at high frequency.

4.4 Diode cut-off frequency

The cut-off frequency of a diode is a fundamental parameter that indicates the highest frequency at which the diode can effectively operate as a signal device. At the cut-off frequency, the diode's response starts to roll off, and its ability to amplify or rectify signals diminishes significantly.

Based on the small-signal equivalent circuit parameters extraction, the diode cut-off frequency can be calculated using equation 4.2 and shown in table 4.4.

$$f_T = \frac{1}{2\pi C_j R_s} \tag{4.2}$$

	Diode 1	Diode 2	Diode 3	Diode4
Cut-off frequency (GHz)	116.9	80.2	67	71.6

The obtained cutoff frequencies for the four diodes provide valuable insights into their RF performance.

Firstly, it can be observed that Diode 1, fabricated on a high-resistivity substrate, exhibits the highest cutoff frequency of 116.9 GHz. This indicates that Diode 1 is capable of operating at higher frequencies before its response starts to roll off. The higher cutoff frequency can be attributed to the lower series resistance ($\mathrm{R_s}$) and lower junction capacitance ($\mathrm{C_j}$) values, as discussed in the previous analysis. These factors contribute to improved high-frequency performance.

In contrast, Diode 2, fabricated on a low-resistivity substrate, has a lower cutoff frequency of 80.2 GHz. This can be attributed to the higher R_s and C_j values, as determined from the equivalent circuit model. The higher resistance and capacitance negatively impact the device's high-frequency response, resulting in a lower cutoff frequency.

Moving on to the 4-finger devices, we observe that Diode 3, fabricated on a high-resistivity substrate, has the lowest cutoff frequency of 67.0 GHz. This can be attributed to the higher R_s and C_j values compared to Diode 1. The presence of more fingers in the device structure does significantly affect the cutoff frequency in this case.

Finally, Diode 4, the 4-finger device fabricated on a low-resistivity substrate, exhibits a slightly higher cutoff frequency of 71.6 GHz compared to Diode 3. The lower C_j value of Diode 4 contribute to the improved high-frequency performance compared to Diode 3.

4.5 Diode RF performance under bias

This section aims to investigate the RF performance of the four diodes under a reverse bias voltage. The reverse bias condition provides valuable insights into the behaviour and performance of the diodes in practical applications. The diodes will be characterized using on-wafer S11 measurements with a Vector Network Analyzer (VNA) in a microwave probe station. By applying a reverse bias voltage of -10V, the diodes will operate under specific biasing conditions, allowing for the examination of their RF response.

Furthermore, this research aims to investigate how different substrate resistivity affects the response of the diodes to the applied bias voltage. By comparing the RF performance of the diodes fabricated on high-resistivity and low-resistivity substrates under the same reverse bias voltage of -10V, we can gain insights into the impact of substrate resistivity on the diode's behaviour, such as changes the diode's capacitance, and overall RF performance.

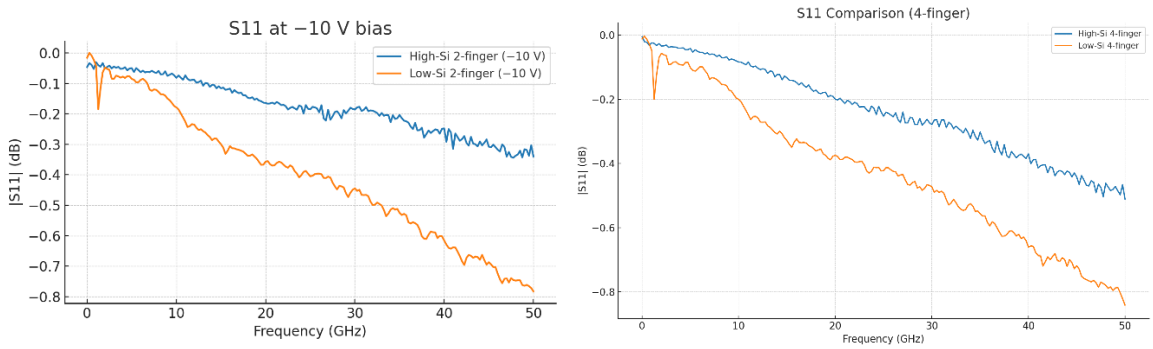


Figure 4.12 S11 measurement of diodes under -10V bias

Figure 4.12(a) presents the S11 measurement results for diode 1 and diode 2, while Figure 4.8(b) showcases the S11 measurement results for diode 3 and diode 4. These measurements were conducted under the same reverse bias condition of -10V. After extracting the parameters from these measurements, it is observed that the only parameter that experiences a notable change after applying the bias voltage is the junction capacitance, which aligns with expectations. Table 4.5 presents the junction capacitance values for each diode under the applied bias voltage of -10V.

Table 4.5 Diodes' junction capacitance under -10V bias

	Diode 1	Diode 2	Diode 3	Diode4
C_j (fF)	6.94	10.56	11.80	10.64

Comparing the values, we can observe a significant decrease in junction capacitance for all diodes after the application of bias. This decrease in capacitance is expected as the applied bias alters the charge distribution and depletion region within the diode structure. With the bias, the junction capacitance decreased 53.9% for diode1, 45.5% for diode 2, 67.2% for diode 3, 51% for diode 4.

Regarding the differential effects of bias on high-resistivity and low-resistivity substrates, we can notice that the bias has a more pronounced effect on diodes fabricated on high-resistivity substrates (Diode 1 and Diode 3) compared to

those on low-resistivity substrates (Diode 2 and Diode 4). The high-resistivity substrates exhibit a greater reduction in junction capacitance after biasing, indicating a stronger influence of bias on the capacitance characteristics.

This phenomenon can be attributed to the high-resistivity substrate's ability to provide better isolation and reduce the scattering of charge carriers, leading to improved electron mobility within the diode structure. As a result, the changes in charge distribution and depletion region width due to biasing have a more significant impact on the capacitance of diodes on high-resistivity substrates.

On the other hand, diodes on low-resistivity substrates may already have a larger capacitance due to increased charge carrier density and reduced mobility. Therefore, the changes in capacitance after biasing may not be as pronounced as in diodes on high-resistivity substrates.

Overall, the bias-induced decrease in junction capacitance for all diodes demonstrates the influence of bias on the internal capacitance characteristics. The more significant effect on diodes on high-resistivity substrates highlights the role of substrate resistivity in modulating the capacitance response to applied bias.

The changes in the junction capacitance are a significant finding, as they reveal the impact of the applied bias on the diode's internal capacitance characteristics. By applying a reverse bias voltage of -10V, the junction capacitance of the diodes is influenced, potentially due to changes in the depletion region width or charge distribution within the device structure. These changes in the junction capacitance can have implications for the diode's overall RF performance.

4.6 Conclusion

In conclusion, the investigation into the RF performance of AlGaN/GaN Schottky diodes with different substrate resistivity values has yielded insightful findings. Under zero bias conditions, it was observed that the diodes fabricated on the low-resistivity substrate exhibited better RF performance at high frequencies due to their relatively high capacitance, which facilitated improved

impedance matching and reduced signal reflection. Conversely, at low frequencies, the diodes on the high-resistivity substrate performed better due to their lower resistance, enabling enhanced RF performance in terms of return loss.

However, when a bias of -10V was applied, a contrasting trend emerged. The diodes fabricated on the high-resistivity substrate demonstrated superior RF performance across the entire frequency range. This can be attributed to the high-resistivity substrate providing better isolation and reduced scattering of electrons, resulting in enhanced electron mobility within the diode structure. With the significant decrease in capacitance under applied bias, resistance starts to play a more important role across the entire frequency range.

Overall, the results highlight the significant impact of substrate resistivity on the RF performance of AlGaN/GaN Schottky diodes. The choice of substrate resistivity can influence the diode's capacitance, series resistance, and overall RF characteristics. Under zero bias, the low-resistivity substrate performs better at high frequencies due to its relatively high capacitance, while the high-resistivity substrate performs better at low frequencies due to its lower resistance. When biased at -10V, the high-resistivity substrate consistently demonstrates superior RF performance across the entire frequency range. These findings underscore the importance of carefully selecting the substrate resistivity to optimize the RF performance of such diodes for specific applications.

Chapter 5

Effect of anode finger on device RF performance

5.1 Introduction

The number of anode fingers plays a crucial role in determining the RF performance of Schottky AlGaN/GaN diodes. These diodes are widely used in high-frequency and high-power applications due to their excellent electron transport properties and high breakdown voltage. The design of the anode structure, particularly the number of anode fingers, directly impacts the device's electrical characteristics and RF performance.

The anode fingers in AlGaN/GaN diodes serve multiple purposes. Firstly, they act as current spreading elements, aiding in the uniform distribution of current across the active region of the diode. This helps to mitigate current crowding effects and improve device efficiency. Secondly, the anode fingers influence the impedance matching between the diode and the external circuitry, which is crucial for achieving optimal RF power transfer.

However, it is essential to strike a balance when selecting the number of anode fingers. Increasing the number of fingers enlarges the total active area, which can reduce current crowding and junction resistance, thereby improving current handling and high-frequency performance. Nevertheless, a larger number of fingers results in more extensive metallization patterns and longer interconnects, which can increase parasitic resistance and inductance. In addition, the presence of more fingers means that local defects in the metal lines or contacts may have a greater impact on device yield and reliability.

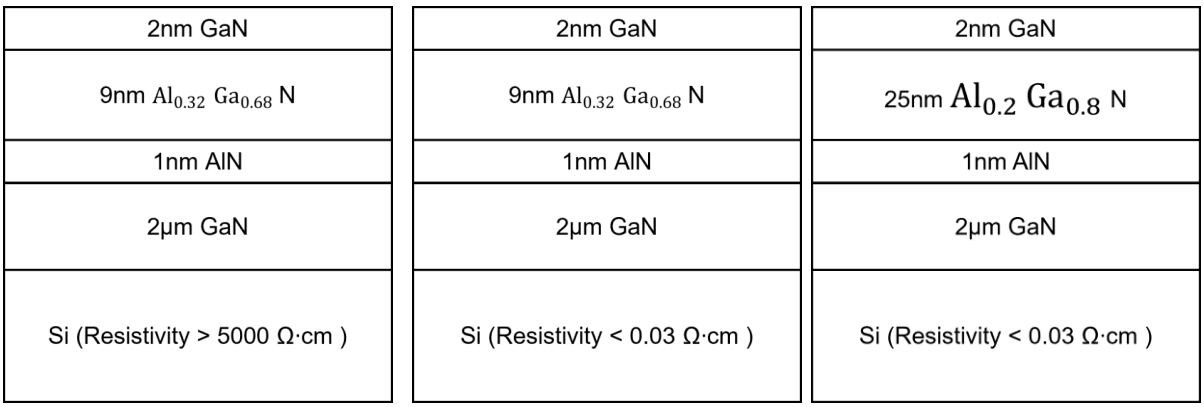
In summary, the number of anode fingers in Schottky AlGaN/GaN diodes significantly influences their RF performance. By carefully selecting the appropriate number of fingers, designers can optimize the electrical characteristics, current distribution, and impedance matching of the diode, leading to improved RF performance in terms of power, efficiency, and bandwidth.

In the previous chapter, we discussed the impact of substrate resistivity on the RF performance of AlGaN/GaN Schottky diodes. Building upon that knowledge, this chapter aims to investigate and reveal the effect of the number of anode fingers on the RF performance of Schottky AlGaN/GaN diodes. The research encompasses a comprehensive experimental study where diodes with varying numbers of anode fingers are fabricated and characterized. The RF performance parameters are carefully measured and analysed for each diode configuration. The chapter focuses on understanding how the number of anode fingers influences these performance, providing valuable insights into the optimal design considerations for achieving enhanced RF performance in Schottky AlGaN/GaN diodes. Through this analysis, the chapter aims to contribute to the knowledge and understanding of the relationship between anode finger design and RF performance in these diodes.

5.2 Epitaxial structure and design considerations

The fabrication process involved six distinct diode structures. For clarity, four of these devices are discussed in Chapter 4 and are denoted as diode 1 to diode 4. The remaining two devices, referred to as diode 5 and diode 6, are described in subsequent sections. Each diode was carefully designed with a specific number of anode fingers, while other parameters such as junction length, anode length, and anode width were kept constant. This systematic approach allowed us to isolate the effects of the anode finger configuration on the diode's RF performance. The wafer information for the different diodes is illustrated in Figure 5.1. Figure 5.1(a) shows the wafer information for diode 1 and diode 3,

Figure 5.1(b) displays the wafer information for diode 2 and diode 4, and Figure 5.1(c) presents the wafer information for diode 5 and diode 6.



(a) (b) (c)

Figure 5.1 Epitaxial structure for (a) Diode 1 and diode 3, (b) Diode 2 and diode 4, (c) Diode 5 and diode 6

5.3 Measurement and results

To assess the impact of the number of anode fingers on diode RF performance, comprehensive RF measurements were conducted using a Vector Network Analyzer (VNA) and a microwave probe station. The S11 parameter, representing the reflection coefficient, was measured and analysed for each diode configuration.

Figure 5.2 depicts the return loss (S11) measurement results for diode 1 and diode 3, illustrating the impact of different numbers of anode fingers on the RF performance. The extracted parameters for these diodes are summarized in Table 5.1, includes the junction capacitance, junction resistance, series resistance, and parasitic capacitance. These parameters were determined through careful analysis and modelling of the measured data, providing valuable insights into their characteristics.

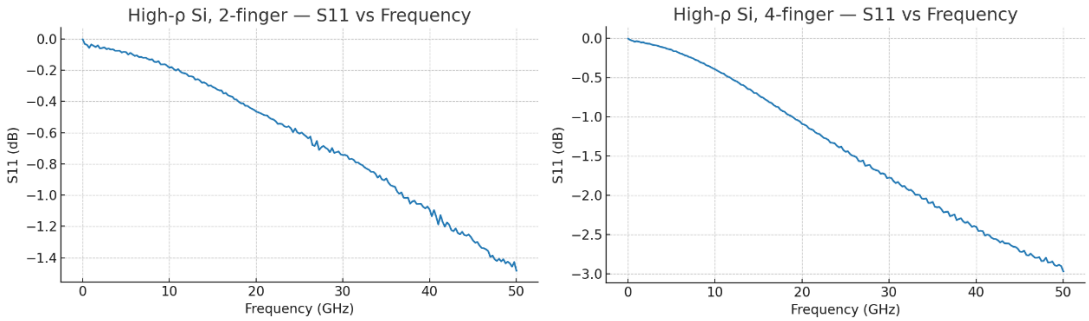


Figure 5.2 Return loss of diodes with different number of finger on wafer 1

Table 5.1

	C_j (fF)	R_j (KOhm)	R_s (Ohm)	C_p (fF)
Diode 1	15.02	66.06	90.6	19.2
Diode 3	36	66.06	65.8	34

The comparison reveals that diode 3, a 4-finger device, exhibits a significantly higher junction capacitance compared to diode 1. This indicates that increasing the number of anode fingers leads to an increase in junction capacitance. While the addition of more fingers enlarges the total anode area, the effect is primarily dominated by the increased parallel periphery between the Schottky anode and the adjacent regions. The larger cumulative periphery enhances the charge storage capability at the metal–semiconductor interface, thereby resulting in a higher overall junction capacitance.

The comparison also indicates that diode 3 exhibits a higher parasitic capacitance compared to diode 1, suggesting that increasing the number of anode fingers may contribute to an increase in parasitic capacitance. The additional fingers and interconnects introduce more capacitance, which can affect the overall capacitance characteristics of the diode. The presence of additional anode fingers in the diode structure creates more opportunities for electric field coupling between adjacent fingers. The electric fields generated by one finger can influence the neighbouring fingers, leading to capacitive coupling.

This capacitive coupling contributes to the overall parasitic capacitance of the diode.

Furthermore, the comparison demonstrates that diode 3 exhibits a lower series resistance compared to diode 1, indicating that increasing the number of anode fingers can lead to a reduction in series resistance. The additional fingers improve the current flow and reduce resistive losses, potentially enhancing the diode's performance at lower frequencies. By effectively increasing the width of the diode structure, the additional anode fingers provide a wider pathway for current conduction. This wider pathway, with its larger cross-sectional area, reduces the resistance encountered by the current, resulting in lower resistive losses.

Figure 5.3 shows the S11 measurement results for diode 2 and diode 4. And the extracted parameters are shown in table 5.2.

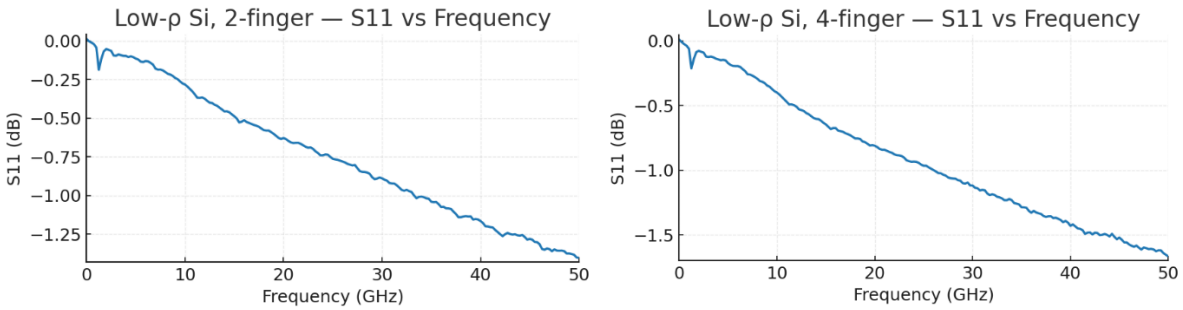


Figure 5.3 Return loss of diodes with different number of finger on wafer 2

Table 5.2 Extracted parameters for 4-finger diodes

	C_j (fF)	R_j (KOhm)	R_s (Ohm)	C_p (fF)
Diode 2	19.36	81.3	102.4	15
Diode 4	30.7	81.3	72.4	45

The comparison between Diode 2 and Diode 4 shows that increasing the number of anode fingers can lead to higher junction capacitance, lower series

resistance, and increased parasitic capacitance. There are similarities between the comparisons of diode 1 and diode 3, and diode 2 and diode 4. Both comparisons highlight the effects of the number of anode fingers on the extracted parameters and RF performance of the diodes. The increase in the number of anode fingers generally leads to higher junction capacitance and parasitic capacitance, as well as lower series resistance.

It can be found from Figure 5.2 and Figure 5.3, the number of anode finger has more effect on the high resistivity substrate devices, which is wafer 1 in this experiment, than low resistivity substrate devices. A suggestion is that when the number of anode fingers is increased, the total surface area of the anode region also increases. This larger surface area allows for a greater interaction between the anode and the surrounding materials, including the semiconductor and the dielectric layers. As a result, the junction capacitance of the diode increases. In high-resistivity substrates, where the resistive losses are already low, the capacitive effects become more prominent and have a greater impact on the overall RF performance.

In Figure 5.4, the return loss of diode 5 and diode 6 is shown with different bias levels applied. Table 5.3 displays the extracted parameters for diode 5 and diode 6

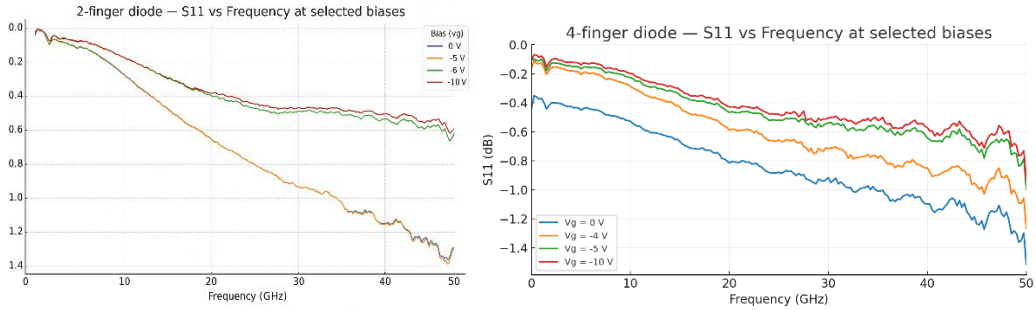


Figure 5.4 Return loss of 2-finger and 4-finger with different bias applied

Table 5.3 Extracted parameters of diode 5 and diode 6 at zero bias

	C_j (fF)	R_j (KOhm)	R_s (Ohm)	C_p (fF)
Diode 5	18.85	56.62	70	40
Diode 6	21.21	56.62	46	46

Comparing diode 5 and diode 6, we can observe some differences in the extracted parameters. Diode 6 exhibits a slightly higher junction capacitance compared to diode 6, indicating a greater ability to store charge at the junction. The junction resistance is the same for both diodes, suggesting similar material properties or fabrication processes for the junction region, the number of anode fingers does not significantly affect the junction resistance. However, there is a notable difference in the series resistance between diode 5 and diode 6. Diode 5 has a higher series resistance compared to diode 6.

5.4 RF response to bias

Figure 5.5 presents a comparison of the S11 parameter between 2-finger and 4-finger diode devices under various bias conditions.

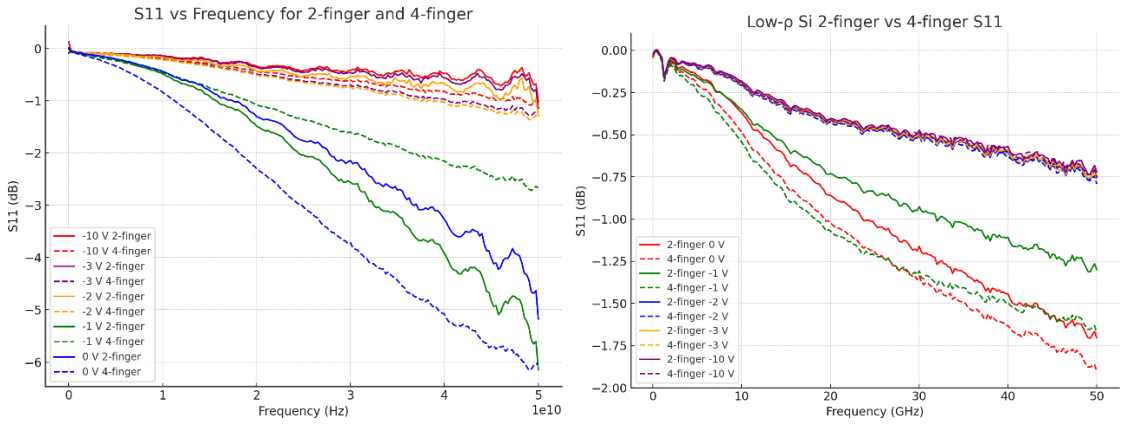


Figure 5.5 S11 comparison between 2-finger device and 4-finger device (a) diode 1 and diode 3, (b) diode 2 and diode 4

In all cases, when a negative bias is applied to the diodes, the return loss decreases. This indicates that the devices exhibit better RF performance with negative bias. In the case of diode 1, the return loss stabilizes at approximately

-3V bias, indicating a state of optimized RF behaviour. Further variations in bias, ranging from -4V to -10V, demonstrate minimal impact on the RF performance, suggesting that diode 1 attains a steady state under these conditions. Consequently, the RF characteristics exhibit consistency, and subsequent adjustments in bias do not exert significant influence. This is because that in the absence of bias (zero or low bias), the semiconductor device may not efficiently control the flow of charge carriers (electrons and holes) across the junction. As the bias is increased, the concentration of carriers near the junction changes, leading to better charge control and improved RF performance. However, beyond a certain bias level, the carrier dynamics reach a saturation point, and further bias changes have limited impact on the carrier concentration. In contrast, diode 3, being a 4-finger device, manifests more discernible changes in response to bias alterations compared to diode 1. Initially, as the bias is increased from zero, an improvement in return loss is observed, signifying an enhancement in RF performance. However, upon reaching a stable point around -2V bias, diode 3's RF performance converges to a level comparable with diode 1's performance at -3V bias. It is noteworthy that diode 3 necessitates a negative bias of approximately -2V to achieve a similar RF performance level observed in diode 1 at -3V bias.

The analogous trend observed in the comparison between diode 2 and diode 4, both fabricated on a low resistivity substrate, reveals a consistent pattern with the previously analysed diode pairs. Initially, diode 2, as a 2-finger device, exhibits an improvement in RF performance as the negative bias is increased from zero. This trend suggests that the additional bias leads to enhanced carrier dynamics and electric field distribution, resulting in improved RF characteristics. However, once the bias reaches a stable point around -3V, diode 2's RF performance plateaus, indicating that further changes in bias have minimal impact on its behaviour. In the case of diode 4, the 4-finger device on the same low resistivity substrate, a similar pattern is observed. The RF performance shows an enhancement as the negative bias is increased from zero, indicating that the additional fingers contribute to a more efficient carrier transport and

electric field manipulation. Once the bias stabilizes at around -3V, diode 4's RF performance remains consistent, closely resembling the performance of diode 2 at the same bias level.

Remarkably, beyond the -3V bias point, diode 2 and diode 4 exhibit nearly identical RF performance. This phenomenon suggests that the number of anode fingers, despite initially influencing the RF behaviour, becomes less consequential after reaching the -3V bias point. At this bias level, the interplay between the carrier dynamics, electric field distribution, and other device parameters becomes consistent for both diodes, leading to similar RF responses.

When a negative bias is applied to the diodes, it modifies the carrier dynamics within the semiconductor material. In Schottky AlGaN/GaN diodes, the negative bias creates an electric field that controls the flow of charge carriers (electrons and holes) across the junction region. This bias-induced electric field alters the concentration of carriers near the junction, resulting in enhanced charge control and improved RF performance. As the bias is increased, the diode becomes more efficient in manipulating the flow of charge carriers, leading to a reduction in reflected RF power and, consequently, a decrease in return loss.

However, there is a point at which further increases in bias have diminishing returns in terms of RF performance improvement. Beyond a certain bias level, the carrier dynamics reach a saturation point, and the influence of the bias-induced electric field on the RF performance plateaus. At this stable bias point, the diode's behavior reaches a consistent state, and subsequent changes in bias have limited impact on the carrier concentration and RF performance.

5.5 Conclusion

In conclusion, this chapter investigated the effect of anode finger design on the RF performance of Schottky AlGaN/GaN diodes. The number of anode fingers was found to play a critical role in determining the electrical characteristics and RF behaviour of these devices.

The comparison between different diode configurations revealed significant variations in junction capacitance, parasitic capacitance, and series resistance with varying numbers of anode fingers. Increasing the number of anode fingers generally led to higher junction capacitance and parasitic capacitance, along with reduced series resistance. This effect was more pronounced in diodes fabricated on high resistivity substrates, where capacitive effects had a greater impact on RF performance.

The study also explored the response of diodes to bias, showing that applying a negative bias improved RF performance for all devices. Diodes on both low and high resistivity substrates exhibited stable RF behaviour after reaching a certain bias level (-3V). Beyond this point, the number of anode fingers became less influential on RF performance, resulting in similar responses for 2-finger and 4-finger diodes.

In summary, careful consideration of the number of anode fingers is essential in optimizing the RF performance of Schottky AlGaN/GaN diodes. The findings from this chapter contribute valuable insights into the design considerations for achieving enhanced RF performance, encompassing power, efficiency, and bandwidth characteristics in these diodes. The knowledge gained serves as a foundation for further advancements in device optimization and application-specific designs, ultimately bolstering the development of high-frequency electronic systems.

Chapter 6

Effect of AlGaN Layer on Device Performance

6.1 Introduction

The AlGaN/GaN heterostructure has emerged as a promising platform for high-frequency and high-power electronic devices, owing to its unique material properties, such as wide bandgap, high electron mobility, and excellent thermal conductivity. The heterojunction formed between the AlGaN barrier layer and the GaN channel layer gives rise to a two-dimensional electron gas (2DEG) with superior electron transport properties, making it an ideal candidate for Schottky diode applications in RF circuits.

This chapter focuses on investigating the impact of the AlGaN layer's composition and thickness on the RF performance of AlGaN/GaN Schottky diodes. The choice of the AlGaN layer significantly influences the diode's electrical characteristics, including the Schottky barrier height, ideality factor, and cut-off frequency, which are essential parameters for RF applications.

As the Al mole fraction (x) in AlGaN is varied, the bandgap of the material changes, affecting the potential barrier height at the metal-semiconductor junction and the carrier density in the 2DEG. The electrical and mechanical properties of AlGaN fall between those of GaN and AlN, providing a tunable range of bandgap values and lattice mismatches. Therefore, careful selection of the AlGaN composition offers a powerful tool for optimizing diode performance for specific RF applications.

Additionally, the thickness of the AlGaN barrier layer plays a crucial role in influencing the diode's RF characteristics. A thicker AlGaN layer may introduce

strain and lattice mismatch, affecting the formation of the 2DEG and the transport properties of charge carriers. Conversely, a thinner AlGaN layer may reduce the barrier height, increasing current leakage and degrading the diode's RF performance.

In this chapter we isolate how AlGaN barrier composition (Al mole fraction, x) and barrier thickness influence both DC and small-signal RF figures of merit. Two wafer sets are compared under identical test conditions: x≈0.32, t_AlGaN = 9 nm (diodes 2 and 4) and x≈0.20, t_AlGaN = 25 nm (diodes 5 and 6), all on low-resistivity Si (ρ≈0.03 Ω·cm) with 2- and 4-finger anodes, respectively. The analysis covers Schottky barrier height (SBH) from DC I–V, extracted small-signal parameters (*Rs, Cj, Rj, Cp*), and the resulting cut-off frequency.

The findings from this study provide valuable insights into the design and optimization of AlGaN/GaN Schottky diodes for RF applications. Understanding the relationship between the AlGaN layer and the diode's RF performance opens up new possibilities for tailoring devices to specific frequency ranges, power levels, and communication standards. Moreover, these insights contribute to the advancement of GaN-based RF technologies and pave the way for the development of more efficient and reliable devices for wireless communication systems, radar applications, and other high-frequency electronics.

6.2 DC measurement result

In this chapter, the investigation into the effect of the AlGaN barrier layer on the device performance is conducted using specific diodes. Among these diodes, we focus on diode 2 and diode 4, which were fabricated on wafer 2, as well as diode 5 and diode 6, which were fabricated on wafer 3, all of which are referenced in Chapter 5. These diodes serve as crucial test structures to explore and analyze the impact of the AlGaN barrier layer's properties on the overall device characteristics.

Table 6.1 provides a comprehensive overview of the configurations for each diode, including the number of fingers used, the Si substrate resistivity in ohm-centimeters, the GaN thickness in nanometers, the AlN thickness, the AlGaN thickness in nanometers, the Al composition, and the GaN cap thickness in nanometers. Diode 2 and diode 4 both feature two fingers each, while diode 5 and diode 6 incorporate four fingers each. The Si substrate resistivity for all the diodes is 0.03 Ω·cm, ensuring consistent conditions for the study.

The GaN thickness is set to 250 nm across all diodes, while the AlN thickness remains at 1 nm. However, a significant variation in the AlGaN thickness is observed, with diode 2 and diode 4 possessing an AlGaN thickness of 9 nm, and diode 5 and diode 6 featuring a higher AlGaN thickness of 25 nm. This variation in AlGaN thickness allows us to examine the impact of this particular parameter on the device performance and behavior.

Another essential parameter considered in these diode configurations is the Al composition in the AlGaN barrier layer. Diode 2, diode 4, diode 5, and diode 6 exhibit Al compositions of 0.32, 0.32, 0.2, and 0.2, respectively. By comparing diodes with different Al compositions, we gain valuable insights into the influence of Al content on the diode's electrical properties.

Table 6.1 Diode configurations

	Number of fingers	Si Substrate Resistivity (Ω·cm)	GaN thickness (nm)	AlN thickness	AlGaN thickness (nm)	Al composition	GaN cap thickness (nm)
Diode2	2	0.03	250	1	9	0.32	2
Diode4	4	0.03	250	1	9	0.32	2
Diode5	2	0.03	250	1	25	0.2	2
Diode6	4	0.03	250	1	25	0.2	2

Figure 6.1 shows representative I–V characteristics for diodes 2, 4 (x≈0.32, 9 nm) and diodes 5, 6 (x≈0.20, 25 nm). It can be found from figure 6.1 that the turn-on voltage of diode 5 and diode 6 is relatively lower than diode 2 and diode4. Schottky barrier height is calculated for all devices using thermionic emission

theory. The Schottky diode's current-voltage characteristics can be described by the following equation 6.1:

$$I = I_0 * \exp\left(\frac{qV}{nk_BT}\right) \quad 6.1$$

Where I is the current flowing through the diode, $I_0$is the reverse-bias saturation current (also known as the reverse leakage current), q is the elementary charge (approximately 1.602 x 10^{-19}C), V is the voltage across the diode, n is the ideality factor, $k_B$is Boltzmann's constant (approximately 8.617 x 10^{-5} eV/K), T is the absolute temperature in Kelvin.

At low forward biases, the exponential term dominates, and we can take the natural logarithm of both sides of the equation:

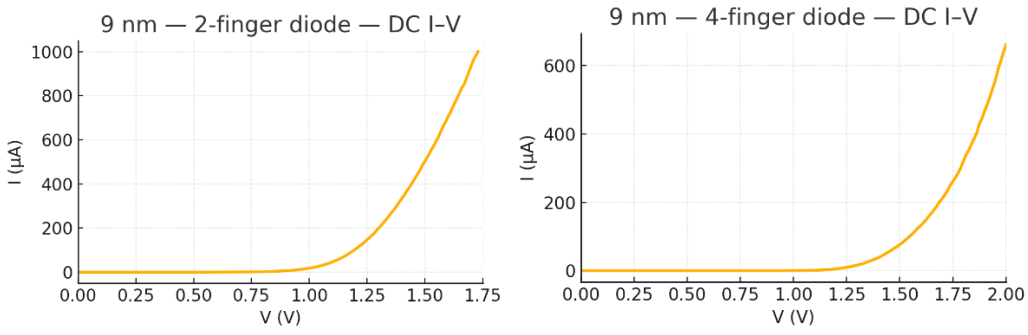
$$\ln(I) = \ln(I_0) + \frac{qV}{nk_BT}$$

The Schottky barrier height (Φ_B)can be extracted from the slope of the linear region of the $\ln(I)$ versus V plot. The slope is given by:

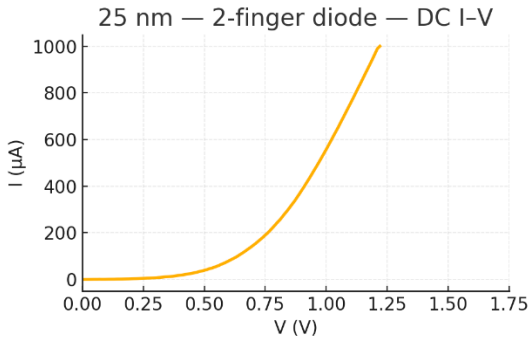
$$Slope = \frac{qV}{nk_BT}$$

Therefore, by knowing the slope, we can calculate the Schottky barrier height:

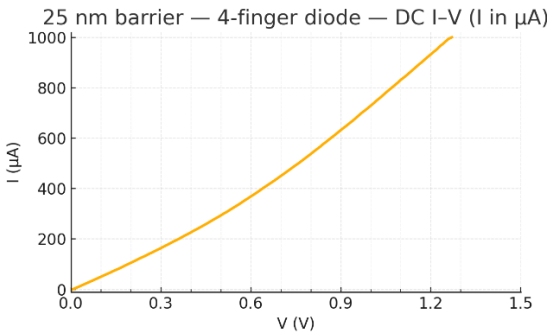
$$\Phi_B = \frac{Slope}{q/n}$$



(a) (b)



(c)



(d)

Figure 6.1 DC measurement for (a) diode 2, (b) diode 4, (c) diode 5, (d) diode 6

Table 6.2 Calculated Schottky barrier height

	Diode 2	Diode 4	Diode 5	Diode 6
Φ_B (eV)	2.02	2.35	1.43	1.54

It can be seen from table 6.2 that diode 2 and diode 4 have a higher SBH than diode 5 and diode6. For Diode 2 and Diode 4, the AlGaN thickness is 9 nm, and the Al composition is 0.32. On the other hand, for Diode 5 and Diode 6, the AlGaN thickness is 25 nm, and the Al composition is 0.2.

The AlGaN layer plays a significant role in determining the Schottky barrier height (SBH) of the diode. The Schottky barrier height is primarily influenced by the difference in work function between the metal contact and the semiconductor material. In this case, the AlGaN layer serves as the semiconductor material in contact with the metal.

A larger AlGaN thickness and a lower Al composition (Diode 5 and Diode 6) may lead to a lower Schottky barrier height. This is because a higher Al composition can reduce the bandgap of the AlGaN layer, which results in a lower electron affinity. Additionally, a thicker AlGaN layer can enhance the quantum tunneling effect, further reducing the SBH.

In contrast, a thinner AlGaN layer with a higher Al composition (Diode 2 and Diode 4) may lead to a higher Schottky barrier height. The larger bandgap and higher electron affinity contribute to the increased SBH.

The apparent SBHs previously reported in Table 6.2 (diode 2: 2.02 eV, diode 4: 2.35 eV, diode 5: 1.43 eV, diode 6: 1.54 eV) follow the expected qualitative trend—higher x → larger ϕB .

Overall, the variation in the AlGaN thickness and Al composition can significantly affect the Schottky barrier height of the diodes, influencing their electrical characteristics and performance in various electronic devices.

6.3 RF characteristics

Table 6.3 summarised the extracted parameters for four diodes.

Table 6.3 Extracted parameters for four diodes

	C_j (fF)	R_j (KOhm)	R_s (Ohm)	C_p (fF)
Diode 2	19.36	81.3	102.4	15
Diode 4	30.7	81.3	72.4	45
Diode 5	18.85	56.62	70	40
Diode 6	21.21	56.62	46	46

By comparing diode 2 and diode 5, both are 2-finger devices, it can be found that the junction capacitance of diode 5 (18.85 fF) is slightly lower than diode 2 (19.36 fF). The difference in junction capacitance can be explained as that the Al composition in the AlGaN layer can influence the effective permittivity of the material, which can further affect the junction capacitance. Generally, higher Al compositions in AlGaN can lead to higher permittivity and, in turn, higher junction capacitance. The same comparison result can be found in diode 4 and diode 6, both are 4-finger devices. This confirms the effect of Al composition on diode junction capacitance.

By comparing the series resistance of four diodes, it can be found that devices on wafer 3 has lower series resistance than diodes on wafer 2. This can also be explained by the decrease of Al composition. The Al composition in the AlGaN layer of a semiconductor device can significantly affect the series resistance in several ways. The first way is the carrier mobility. The Al composition in the AlGaN layer influences the carrier mobility of the material. As the Al content increases, the carrier mobility tends to decrease. Reduced carrier mobility leads to increased resistance to the flow of current, resulting in a higher series resistance. The second way is the scattering mechanism. With higher Al composition, the scattering mechanisms that hinder the movement of charge carriers (such as electrons and holes) become more prominent. As a result, the electrons and holes encounter more resistance while moving through the material, contributing to a higher series resistance. Another way is the bandgap energy. The Al composition affects the bandgap energy of the AlGaN layer. As the Al content increases, the bandgap energy widens. The increased bandgap energy can lead to higher energy barriers for charge carriers, making it more challenging for them to pass through the material, thereby increasing the series resistance.

The thickness of the AlGaN layer plays a crucial role in determining parasitic capacitance. A thicker AlGaN layer results in a larger separation between the metal contact and the semiconductor, which increases the capacitance. This is because the capacitance is directly proportional to the area of the metal-semiconductor interface and inversely proportional to the distance between them. As can be seen from table 6.3. diode 5 and diode 6 (with 25nm AlGaN) shows a higher parasitic capacitance than diode 2 and diode 4 (with 9nm AlGaN).

However, comparing to 2-finger devices, 4-finger devices show a very close difference of parasitic capacitance. A suggestion is that the parasitic capacitance has different sources. One common source of parasitic capacitance in Schottky diodes is the capacitance between the metal fingers

(electrodes). Another source of parasitic capacitance can be the capacitance between different layers of the device, such as the capacitance between the metal layer and the AlGaN semiconductor layer. With the increase of finger numbers, the coupling between metal fingers becomes dominant than other capacitance sources. Thus, the difference of parasitic capacitance of 4-finger diodes is less than that of 2-finger diodes.

The cut-off frequency of four diodes is shown in table 6.4.

Table 6.4 Cut-off frequency of four diodes

	Diode 2	Diode4	Diode 5	Diode 6
Cut-off frequency (GHz)	80.2	71.6	120.6	163.1

6.4 Device response to bias

The comparison of measured S11 under different bias of diode 2 and diode 5 is shown in figure 6.2. The bias vary from 0V to -10V with a step of 1V.

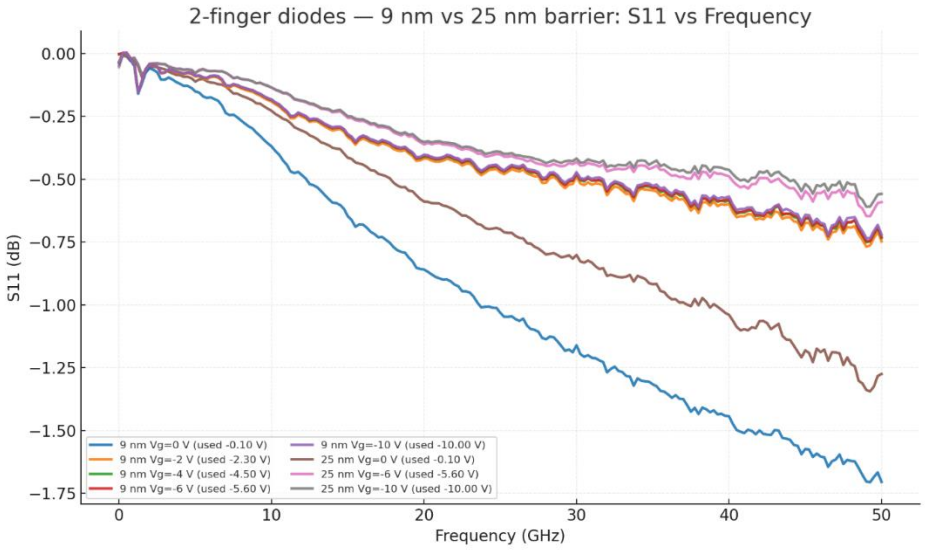


Figure 6.2 Return loss of diode 2 (blue) and diode 5 (red) under bias

It can be observed from figure 6.2 that diode 5 shows a lower return loss at all bias. A lower aluminum composition in AlGaN generally results in a wider bandgap, which can lead to lower leakage currents and better high-voltage

operation characteristics, contributing to the lower return loss. As the reverse bias increases from 0 V to -10 V, the capacitance decreases, resulting in less return loss. However, for diode 2, as the reverse bias increases from 0 V to -2 V, the return loss improves (becomes lower) since the capacitance is decreasing, similar to diode 5. However, after reaching a bias of -2 V, further increases in reverse bias do not significantly affect the return loss. This suggests that the capacitance of diode 2 stabilizes at a bias of -2 V, and additional bias does not have a substantial impact on its performance. On the other hand, the return loss of diode 5 becomes stable at about -4 V bias.

A suggestion on this observation is that diode 2 has a thinner AlGaN layer (9 nm) compared to diode 5 (25 nm). The thinner AlGaN layer results in a narrower depletion region as the reverse bias increases. At a bias of around -2 V, the depletion region stabilizes, and the capacitance reaches a relatively stable value. Further increasing the bias beyond -2 V may not significantly impact the capacitance because the depletion region has already reached its stable configuration. The thicker AlGaN layer leads to a wider depletion region as the reverse bias increases. It takes a higher reverse bias (around -4 V) for the wider depletion region to stabilize and for the capacitance to reach a relatively constant value.

Figure 6.3 shows the return loss of diode 4 (blue) and diode 6 (red) under bias

It can be seen from figure 6.3 that diode 6 shows a lower return loss than diode 4 at almost all bias. Diode 4 stables at -3 V bias, while diode 6 stables at -5 V bias. However, their RF performance becomes comparable once they reach their stable bias points. The information of four diodes include the bias at which the diode stable is shown in table 6.5 to make the comparison clearer.

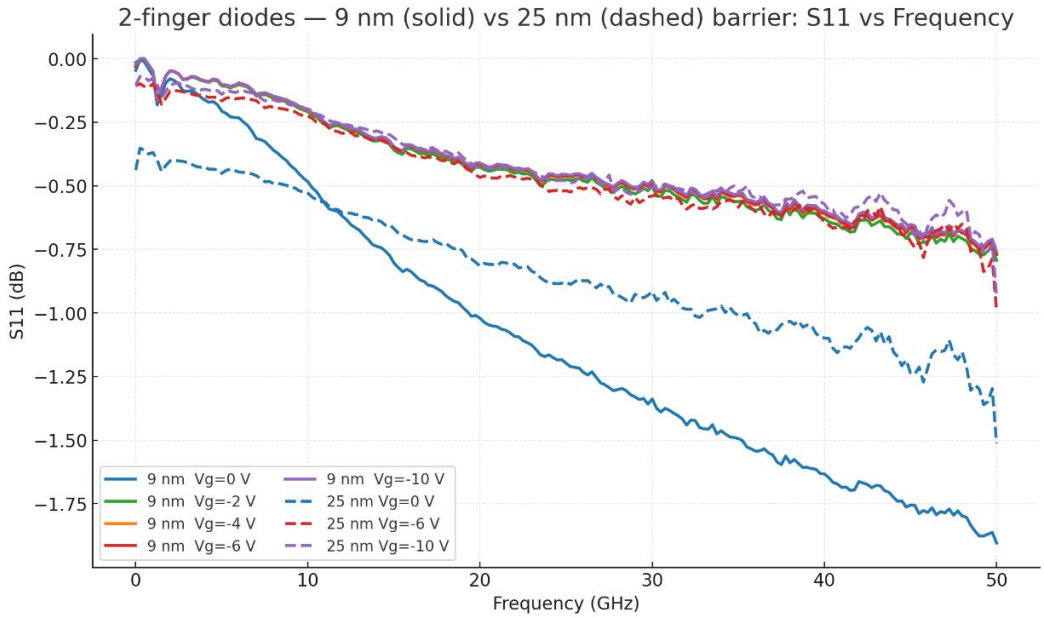


Figure 6.3 Return loss of diode 4 (blue) and diode 6 (red) under bias

Table 6.5 Diode information summary

	Diode 2	Diode 4	Diode5	Diode 6
Finger number	2	4	2	4
AlGaN thickness (nm)	9	9	25	25
Al composition	0.32	0.32	0.2	0.2
Stable bias	-2 V	-3 V	-4 V	-5 V

Diodes 2 and 4 have the same AlGaN thickness and composition, but diode 4, with two additional fingers (4-finger diode), requires a higher stable bias (-3 V vs. -2 V for diode 2). Similarly, for diodes 5 and 6, both have the same AlGaN thickness and composition, but diode 6 (4-finger diode) requires a higher stable bias (-5 V) compared to diode 5 (-4 V). This suggests that 4-finger diodes generally need a higher stable bias compared to 2-finger diodes. The presence of multiple fingers in a diode alters its junction capacitance characteristics. Capacitance is a critical factor in high-frequency applications. The larger active area in 4-finger diodes can increase the junction capacitance, affecting the device's high-frequency response. To compensate for these capacitance

changes and maintain desired performance, a higher stable bias may be necessary.

6.5 Conclusion

In this chapter, we investigated the effect of the AlGaN layer's composition and thickness on the RF performance of AlGaN/GaN Schottky diodes. The AlGaN/GaN heterostructure offers unique material properties, making it an ideal platform for high-frequency and high-power electronic devices. By exploring the impact of the AlGaN layer's properties on diode performance, we gained valuable insights into optimizing diode characteristics for specific RF applications.

Through a systematic study of AlGaN/GaN Schottky diodes with varying AlGaN layer composition and thickness, we extracted critical parameters such as Schottky barrier height, junction capacitance, series resistance, and parasitic capacitance. The results showed that the AlGaN layer significantly influences the Schottky barrier height of the diodes, higher Al content (larger bandgap, lower χ) tends to increase the ideal n-type SBH, while a thicker AlGaN barrier generally reduces tunnelling and lowers Cj at a given geometry; together with improved mobility at lower Al composition, this yields the observed Rs–Cj trade-off and the highest fc for the 25-nm/20%-Al devices.

Furthermore, the series resistance of the diodes was influenced by the Al composition, with higher Al content leading to increased resistance due to reduced carrier mobility and enhanced scattering mechanisms. The thickness of the AlGaN layer played a crucial role in determining the parasitic capacitance, with thicker layers resulting in higher capacitance due to increased metal-semiconductor separation.

Comparing 2-finger diodes to 4-finger diodes, we observed that 4-finger diodes generally required higher stable biases to compensate for the larger active area and altered junction capacitance characteristics. The relationship between the

stable bias and diode performance allowed us to optimize the diodes for specific applications.

Overall, this chapter's findings contribute to the design and optimization of AlGaN/GaN Schottky diodes for RF applications. The insights gained from understanding the impact of the AlGaN layer's properties on device performance open up possibilities for tailoring devices to specific frequency ranges, power levels, and communication standards. Additionally, these findings advance GaN-based RF technologies, leading to the development of more efficient and reliable devices for wireless communication systems, radar applications, and other high-frequency electronics. The exploration of the AlGaN/GaN heterostructure's potential continues to pave the way for innovative electronic devices in the field of RF electronics.

Chapter 7

Conclusion and future directions

7.1 Conclusion

In this thesis, we investigated the design, fabrication, and characterization of AlGaN/GaN Schottky diodes for high-frequency and high-power electronic applications. The AlGaN/GaN heterostructure has emerged as a promising platform for RF devices due to its unique material properties, including wide bandgap, high electron mobility, and excellent thermal conductivity. The research presented in this work focused on understanding the impact of substrate resistivity, number of anode finger, and the AlGaN layer's composition and thickness on the electrical characteristics and RF performance of Schottky diodes.

Chapter 4 discussed the effect of substrate resistivity on diode RF performance. At zero bias, high-resistivity substrates do not universally improve high-frequency return loss; the net effect depends on both *Rs* and *Cj*. Under −10 V reverse bias, however, *Cj* reduction dominates and the high-resistivity substrate shows the best overall reflection, which matches our S-parameter observations.

Chapter 5 explored the impact of anode finger design on the RF performance of Schottky AlGaN/GaN diodes. The investigation focused on understanding how the number of anode fingers influences the electrical characteristics and RF behaviour of these devices. The number of anode fingers was found to play a crucial role in determining the electrical characteristics of Schottky AlGaN/GaN diodes. Increasing the number of anode fingers led to higher

junction capacitance and parasitic capacitance, along with reduced series resistance. This effect was more pronounced in diodes fabricated on high resistivity substrates, where capacitive effects had a greater impact on RF performance. While increasing the number of anode fingers provided performance benefits in terms of improved carrier dynamics and reduced resistive losses, it also introduced additional parasitic. Applying a negative bias to the diodes improved RF performance in all cases. Beyond a certain bias level, the carrier dynamics reached a saturation point, leading to stable RF behavior. At this stable bias point, the number of anode fingers became less influential on RF performance, resulting in similar responses for 2-finger and 4-finger diodes.

The findings from Chapter 6 highlighted the significance of the Al composition in determining the Schottky barrier height of the diodes. Lower Al composition (e.g., around 0.2) led to a lower Schottky barrier height, making the diodes suitable for high-frequency applications that require fast switching and low signal loss. On the other hand, higher Al composition (e.g., around 0.32) resulted in a higher Schottky barrier height, making the diodes more suitable for applications that demand higher power handling capabilities and improved linearity in power amplification. The thickness of the AlGaN layer was also a critical parameter in determining the diode's performance. Thicker AlGaN layers (e.g., around 25 nm) led to higher parasitic capacitance, which could be advantageous for high-power amplification applications. In contrast, thinner AlGaN layers (e.g., around 9 nm) reduced parasitic capacitance, making them suitable for high-frequency applications with reduced signal loss.

Parameters of all devices designed in this work is summarized in table 7.1.

Design guidance distilled from the data is that:

- Ka-band front-ends (26.5–40 GHz): Choose 25 nm, x≈0.20 barriers for margin (fc up to 163 GHz). Use 4-finger layouts where Rs dominates; use 2-finger where minimal Cj is critical. Expect bias plateaus between −2 and −5 V depending on barrier and geometry.

- Substrate choice: HR Si is advantageous under reverse bias for reflection performance; at 0 V its benefit is clearest for compact (2-finger) layouts.

Table 7.1 — Consolidated device summary

Diode	Substrate	Fingers	AlGaN (t / x)	Rs (Ω)	Cj@0 V (fF)	Cp (fF)	f_c (GHz)	Stable bias
1	High-ρ Si	2	9 nm / 0.32	90.6	15.02	19.2	116.9	≈ −3 V
2	Low-ρ Si	2	9 nm / 0.32	102.4	19.36	15	80.2	≈ −2 V
3	High-ρ Si	4	9 nm / 0.32	65.8	36	34	67	≈ −2 V
4	Low-ρ Si	4	9 nm / 0.32	72.4	30.7	45	71.6	≈ −3 V
5	Low-ρ Si	2	25 nm / 0.20	70	18.85	40	120.6	≈ −4 V
6	Low-ρ Si	4	25 nm / 0.20	46	21.21	46	163.1	≈ −5 V

7.2 Future directions

7.2.1 Substrate–barrier decoupling

To disentangle substrate and barrier contributions that were coupled across Chapters 4–6, a control pair will be fabricated by transferring the 25 nm / x≈0.20 barrier (currently on low-resistivity Si) onto high-resistivity Si, keeping the 2-/4-finger geometries, CPW pads and metal stacks unchanged. A side-by-side comparison of *Rs*, *Cj* (at 0 V and −10 V), *Cp* and *fc* between HR, 25 nm/20%-Al and LR, 25 nm/20%-Al will indicate whether the reflection-band improvements observed under reverse bias are predominantly substrate-driven (via *Cj* suppression) or barrier-driven.

7.2.2 Geometry-driven Pareto optimisation

Given the *Rs* – *Cj* – *Cp* trade-off, a targeted design-of-experiments will be undertaken. A 3×3 sweep is proposed: finger count = 2/4/6, junction length *Lj*=3/4/5, and finger pitch = 10/15/20 µm; pads/tapers and metal stacks will be held constant. The outcome will be a geometry selector for Ka-band applications under bandwidth-limited constraints fc>170 GHz together with |S11 |<10 dB across 26.5–40 GHz will be used as a practical optimisation target.

References

1. Łukasiak, L. and A. Jakubowski, *History of semiconductors.* Journal of Telecommunications and information technology, 2010(1): p. 3-9.
2. Liu, A.-C., et al., *The evolution of manufacturing technology for GaN electronic devices.* Micromachines, 2021. **12**(7): p. 737.
3. Kemerley, R.T., H.B. Wallace, and M.N. Yoder, *Impact of wide bandgap microwave devices on DoD systems.* Proceedings of the IEEE, 2002. **90**(6): p. 1059-1064.
4. Mimura, T., et al., *A new field-effect transistor with selectively doped GaAs/n-AlxGa1-xAs heterojunctions.* Japanese journal of applied physics, 1980. **19**(5): p. L225.
5. Ibbetson, J.P., et al., *Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors.* Applied Physics Letters, 2000. **77**(2): p. 250-252.
6. Mehdi, I., et al., *THz diode technology: Status, prospects, and applications.* Proceedings of the IEEE, 2017. **105**(6): p. 990-1007.
7. Wang, T., et al., *Fabrication of high performance of AlGaN/GaN-based UV light-emitting diodes.* Journal of crystal growth, 2002. **235**(1-4): p. 177-182.
8. Lorenz, K., et al., *Comparative study of GaN and AlN nucleation layers and their role in growth of GaN on sapphire by metalorganic chemical vapor deposition.* Applied Physics Letters, 2000. **77**(21): p. 3391-3393.
9. Li, C., et al., *Growth of thin AlN nucleation layer and its impact on GaN-on-SiC heteroepitaxy.* Journal of Alloys and Compounds, 2020. **838**: p. 155557.
10. Feng, Y., et al., *High quality GaN-on-SiC with low thermal boundary resistance by employing an ultrathin AlGaN buffer layer.* Applied Physics Letters, 2021. **118**(5).
11. Zhong, Y., et al., *A review on the GaN-on-Si power electronic devices.* Fundamental Research, 2022. **2**(3): p. 462-475.
12. Chao, P.-C., et al., *Low-temperature bonded GaN-on-diamond HEMTs with 11 W/mm output power at 10 GHz.* IEEE Transactions on Electron Devices, 2015. **62**(11): p. 3658-3664.

13. Liu, T., et al., *3-inch GaN-on-diamond HEMTs with device-first transfer technology.* IEEE Electron Device Letters, 2017. **38**(10): p. 1417-1420.
14. Kuzmík, J., *Power electronics on InAlN/(In) GaN: Prospect for a record performance.* IEEE Electron Device Letters, 2001. **22**(11): p. 510-512.
15. Ng, T.K., et al., *Group-III-nitride and halide-perovskite semiconductor gain media for amplified spontaneous emission and lasing applications.* Journal of Physics D: Applied Physics, 2021. **54**(14): p. 143001.
16. Zhu, D., D. Wallis, and C. Humphreys, *Prospects of III-nitride optoelectronics grown on Si.* Reports on Progress in Physics, 2013. **76**(10): p. 106501.
17. Leszczynski, M., et al., *Lattice constants, thermal expansion and compressibility of gallium nitride.* Journal of Physics D: Applied Physics, 1995. **28**(4A): p. A149.
18. Zang, K., et al., *Structural analysis of metalorganic chemical vapor deposited AlN nucleation layers on Si (1 1 1).* Journal of crystal growth, 2004. **268**(3-4): p. 515-520.
19. Haeberlen, M., et al. *Dislocation reduction in MOVPE grown GaN layers on (111) Si using SiNx and AlGaN layers*. in *Journal of Physics: Conference Series*. 2010. IOP Publishing.
20. Able, A., et al., *Growth of crack-free GaN on Si (1 1 1) with graded AlGaN buffer layers.* Journal of Crystal Growth, 2005. **276**(3-4): p. 415-418.
21. Seon, M., et al., *Selective growth of high quality GaN on Si (111) substrates.* Applied physics letters, 2000. **76**(14): p. 1842-1844.
22. Einfeldt, S., et al., *Strain relaxation in AlGaN/GaN superlattices grown on GaN.* Journal of Applied Physics, 2001. **89**(4): p. 2160-2167.
23. Feltin, E., et al., *Crack‐free thick GaN layers on silicon (111) by metalorganic vapor phase epitaxy.* physica status solidi (a), 2001. **188**(2): p. 531-535.
24. Ni, Y., et al., *Effect of AlN/GaN superlattice buffer on the strain state in GaN-on-Si (111) system.* Japanese Journal of Applied Physics, 2014. **54**(1): p. 015505.
25. Li, M., et al., *Low-leakage-current AlGaN/GaN HEMTs on Si substrates with partially Mg-doped GaN buffer layer by metal organic chemical vapor deposition.* Chinese Physics B, 2014. **23**(3): p. 038403.

26. Choi, Y.C., et al., *The effect of an Fe-doped GaN buffer on off-state breakdown characteristics in AlGaN/GaN HEMTs on Si substrate.* IEEE transactions on Electron devices, 2006. **53**(12): p. 2926-2931.
27. Haffouz, S., et al., *AlGaN/GaN field effect transistors with C-doped GaN buffer layer as an electrical isolation template grown by molecular beam epitaxy.* Solid-state electronics, 2005. **49**(5): p. 802-807.
28. Leone, S., et al., *Suppression of iron memory effect in GaN epitaxial layers.* physica status solidi (b), 2018. **255**(5): p. 1700377.
29. Simon, J., et al., *Spontaneous polarization effects in GaN/Al x Ga 1− x N quantum wells.* Physical Review B, 2000. **61**(11): p. 7211.
30. Supryadkina, I., et al., *Study of the polarizations of (Al, Ga, AlGa) N nitride compounds and the charge density of various interfaces based on them.* Semiconductors, 2013. **47**: p. 1621-1625.
31. Lu, W., et al., *DC, RF, and microwave noise performance of AlGaN-GaN field effect transistors dependence of aluminum concentration.* IEEE Transactions on Electron Devices, 2003. **50**(4): p. 1069-1074.
32. Wong, Y.-Y., et al. *Growth and fabrication of AlGaN/GaN HEMT on SiC substrate*. in *2012 10th IEEE International Conference on Semiconductor Electronics (ICSE)*. 2012. IEEE.
33. Wu, Y.-F., et al., *High Al-content AlGaN/GaN MODFETs for ultrahigh performance.* IEEE Electron Device Letters, 1998. **19**(2): p. 50-53.
34. Shrestha, N.M., Y. Li, and E.Y. Chang, *Simulation study on electrical characteristic of AlGaN/GaN high electron mobility transistors with AlN spacer layer.* Japanese Journal of Applied Physics, 2014. **53**(4S): p. 04EF08.
35. Wosko, M., et al., *Influence of AlN spacer on the properties of AlGaN/AlN/GaN heterostructures.* Optica Applicata, 2013. **43**(1): p. 61-66.
36. Smorchkova, I., et al., *AlN/GaN and (Al, Ga) N/AlN/GaN two-dimensional electron gas structures grown by plasma-assisted molecular-beam epitaxy.* Journal of Applied Physics, 2001. **90**(10): p. 5196-5201.
37. Tan, S., et al., *Influence of growth parameters and thickness of AlN spacer on electrical properties of AlGaN/AlN/GaN high-electron-mobility transistors grown on 4-inch Si substrate.* Japanese Journal of Applied Physics, 2009. **48**(11R): p. 111002.

38. Hsueh, K.-P., et al., *Effect of AlN spacer layer thickness on AlGaN/GaN/Si Schottky barrier diodes.* Materials Science in Semiconductor Processing, 2017. **66**: p. 69-73.
39. Akkal, B., et al., *Electrical characterization of Au/n-GaN Schottky diodes.* Materials Chemistry and Physics, 2004. **85**(1): p. 27-31.
40. Reddy, V.R., et al., *Electrical characterization of Au/n-GaN metal–semiconductor and Au/SiO2/n-GaN metal–insulator–semiconductor structures.* Journal of alloys and compounds, 2011. **509**(31): p. 8001-8007.
41. Jung, H., et al., *Reliability behavior of GaN HEMTs related to Au diffusion at the Schottky interface.* physica status solidi c, 2009. **6**(S2 2): p. S976-S979.
42. Wang, L., et al., *High barrier height gan schottky diodes: Pt/gan and pd/gan.* Applied Physics Letters, 1996. **68**(9): p. 1267-1269.
43. Ofuonye, B., et al., *Electrical and microstructural properties of thermally annealed Ni/Au and Ni/Pt/Au Schottky contacts on AlGaN/GaN heterostructures.* Semiconductor science and technology, 2014. **29**(9): p. 095005.
44. Miura, N., et al., *Thermal annealing effects on Ni/Au based Schottky contacts on n-GaN and AlGaN/GaN with insertion of high work function metal.* Solid-State Electronics, 2004. **48**(5): p. 689-695.
45. Sun, Y., et al., *Thermal annealing behaviour of Ni/Au on n-GaN Schottky contacts.* Journal of Physics D: Applied Physics, 2002. **35**(20): p. 2648.
46. Yan, D., et al., *Forward current transport mechanisms in Ni/Au-AlGaN/GaN Schottky diodes.* Journal of Applied Physics, 2013. **114**(14).
47. Akkaya, A., et al., *Effect of thermal annealing on electrical and structural properties of Ni/Au/n-GaN Schottky contacts.* Microelectronic engineering, 2014. **130**: p. 62-68.
48. Mohammad, S.N., *Contact mechanisms and design principles for alloyed ohmic contacts to n-GaN.* Journal of Applied Physics, 2004. **95**(12): p. 7940-7953.
49. Van Daele, B., et al., *The role of Al on Ohmic contact formation on n-type GaN and AlGaN ／ GaN.* Applied Physics Letters, 2005. **87**(6).
50. Papanicolaou, N., et al., *Reliable Ti/Al and Ti/Al/Ni/Au ohmic contacts to n-type GaN formed by vacuum annealing.* Journal of Vacuum Science &

Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 2001. **19**(1): p. 261-267.

51. Qin, Z., et al., *Study of Ti/Au, Ti/Al/Au, and Ti/Al/Ni/Au ohmic contacts to n-GaN.* Applied Physics A, 2004. **78**: p. 729-731.
52. Wang, D.-F., et al., *Low-resistance Ti/Al/Ti/Au multilayer ohmic contact to n-GaN.* Journal of Applied Physics, 2001. **89**(11): p. 6214-6217.
53. Davydov, A., et al., *Combinatorial optimization of Ti/Al/Ti/Au ohmic contacts to n-GaN.* physica status solidi (c), 2005. **2**(7): p. 2551-2554.
54. Zhao, Z., et al., *Ti/al/pt/au and al ohmic contacts on si-substrated gan.* Applied Physics Letters, 2001. **79**(2): p. 218-220.
55. Lee, C.-T. and H.-W. Kao, *Long-term thermal stability of Ti/Al/Pt/Au Ohmic contacts to n-type GaN.* Applied Physics Letters, 2000. **76**(17): p. 2364-2366.
56. Grabowski, S., et al., *Electron affinity of Al x Ga 1− x N (0001) surfaces.* Applied Physics Letters, 2001. **78**(17): p. 2503-2505.
57. Kamada, A., et al. *High-voltage AlGaN/GaN Schottky barrier diodes on Si substrate with low-temperature GaN cap layer for edge termination*. in *2008 20th International Symposium on Power Semiconductor Devices and IC's*. 2008. IEEE.
58. Meneghesso, G., et al., *Current Collapse and High-Electric-Field Reliability of Unpassivated GaN/AlGaN/GaN HEMTs.* IEEE Transactions on Electron Devices, 2006. **53**(12): p. 2932-2941.
59. Wong, K.-Y., et al., *Zero-bias mixer based on AlGaN/GaN lateral field-effect diodes for high-temperature wireless sensor and RFID applications.* IEEE transactions on electron devices, 2009. **56**(12): p. 2888-2894.
60. Oh, J.-H., et al., *High-performance 94-GHz single-balanced diode mixer using disk-shaped GaAs Schottky diodes.* IEEE electron device letters, 2009. **30**(3): p. 206-208.
61. Guo, J., et al., *W band single diode fundamental mixer with high intermediate frequency.* Microwave and Optical Technology Letters, 2018. **60**(9): p. 2191-2193.
62. Ding, D., J. Xu, and Z. Chen. *A W-band low conversion loss single balanced mixer with planar GAAS schottky diodes*. in *2012 International Conference on Microwave and Millimeter Wave Technology (ICMMT)*. 2012. IEEE.

63. Ren, L., J. Xu, and C. Wang, *Design of a full V-band fundamental mixer with an ultra-wide IF from 0.01 to 22 GHz.* Electronics Letters, 2021. **57**(25): p. 961-963.
64. Ballamy, W.C. and Y. Ota, *Low barrier height Schottky mixer diode using super thin silicon films by molecular beam epitaxy.* Applied Physics Letters, 1981. **39**(8): p. 629-630.
65. Crowe, T. and R. Mattauch, *Conversion loss in GaAs Schottky-barrier mixer diodes.* IEEE transactions on microwave theory and techniques, 1986. **34**(7): p. 753-760.
66. Gastellóu, E., et al., *A brief review of growth techniques for obtaining of III-V semiconductor compounds.* European Journal of Engineering and Technology Research, 2019. **4**(9): p. 17-21.
67. Rabiee Golgir, H., et al., *Fast Growth of GaN Epilayers via Laser-Assisted Metal–Organic Chemical Vapor Deposition for Ultraviolet Photodetector Applications.* ACS applied materials & interfaces, 2017. **9**(25): p. 21539-21547.
68. Liu, B., et al., *MOCVD growth of device-quality GaN on sapphire using a three-step approach.* Journal of crystal growth, 2002. **234**(4): p. 637-645.
69. Song, K.-M., et al., *Characteristics of GaN grown by metalorganic chemical vapor deposition using trimethylgallium and triethylgallium.* Journal of crystal growth, 2001. **233**(3): p. 439-445.
70. Zhuang, D. and J. Edgar, *Wet etching of GaN, AlN, and SiC: a review.* Materials Science and Engineering: R: Reports, 2005. **48**(1): p. 1-46.
71. Pankove, J., *Electrolytic etching of GaN.* Journal of The Electrochemical Society, 1972. **119**(8): p. 1118.
72. Koolen, M., J. Geelen, and M. Versleijen. *An improved de-embedding technique for on-wafer high-frequency characterization*. in *Proc. Bipolar Circuits Technol. Meeting*. 1991. Citeseer.
73. Minko, A., et al., *High microwave and noise performance of 0.17-μm AlGaN-GaN HEMTs on high-resistivity silicon substrates.* IEEE Electron Device Letters, 2004. **25**(4): p. 167-169.

74. Benakaprasad, B., et al., *Optimization of ohmic contact for AlGaN/GaN HEMT on low-resistivity silicon.* IEEE Transactions on Electron Devices, 2020. **67**(3): p. 863-868.
75. Eblabla, A., et al., *High performance GaN high electron mobility transistors on low resistivity silicon for $ X $-band applications.* IEEE Electron Device Letters, 2015. **36**(9): p. 899-901.

Appendix A

ADS equations for De-embedding:

S_DUT = S (1,1)

S_Open = S (2,2)

S_Short = S (3,3)

Y_DUT = stoy (S_DUT)

Y_Open = stoy (S_open)

Y_Short = stoy (S_Short)

Y_DUT_Open = Y_DUT - Y_Open

Y_Short_Open = Y_Short - Y_Open

Z_DUT_Open = ytoz (Y_DUT_Open)

Z_Short_Open = ytoz (Y_Short_Open)

Z_DUT_Deem = Z_DUT_Open - Z_Short_Open

S_DUT_Deem = ztos (Z_DUT_Deem)

Python code for SBH calculation

```
import numpy as np

import matplotlib.pyplot as plt


# Given data

V = np.array([0, 0.01, 0.02, ..., 1.21, 1.22])  # Voltage in volts

I = np.array([-2.30E-08, 5.18E-08, 2.42E-07, ..., 9.45E-04, 9.68E-04])  # Current in amperes


# Calculate I0
```

```
I0 = -2.30e-8  # A

# Calculate the slope of the linear fit
slope, _ = np.polyfit(V[10:], np.log(I[10:]), 1)

# Calculate the Schottky barrier height (Phi_B)
q = 1.602e-19  # Elementary charge in coulombs
n = 1  # Ideality factor
kB = 8.617e-5  # Boltzmann's constant in eV/K
T = 298  # Room temperature in Kelvin

Phi_B = (slope / (q / n)) / (kB * T)

print("Schottky Barrier Height (Phi_B):", Phi_B, "eV")
```