Distributed Arc Suppression Strategy for Single-Line-to-Ground Faults in Distribution Networks Based on Cooperative Control of Multiple Power Routers

Jinmu Lai, *Member, IEEE,* Zhu Li, Junhong Chen, Jun Liang, *Fellow, IEEE,* Jinrui Tang, *Member, IEEE*
Fan Xiao, *Member, IEEE,* and Xin Yin, *Member, IEEE*

***Abstract*—Traditional arc suppression devices for single-line-to-ground (SLG) faults in distribution networks often suffer from functional singularity, low utilization rates during non-fault conditions, and excessive capacity sizing requirements. To address these limitations, this paper proposes a distributed arc suppression strategy leveraging the cooperative control of multiple power routers (PRs). In steady-state operation, distributed PRs execute active ground parameter compensation (AGPC) to dynamically mitigate zero-sequence voltage offsets induced by three-phase line-to-ground parameter asymmetry. Upon the occurrence of an SLG fault, a voltage-current coordinated mechanism is activated. Specifically, the current-controlled PR (CC-PR) serves as a current support unit by injecting adjustable currents to undertake the primary burden of fault current compensation. Simultaneously, a voltage-controlled PR (VC-PR) acts as a voltage clamping unit to ensure precise control of the residual voltage via a unified voltage reference. This method facilitates the flexible allocation of suppression capacity among multiple PRs, thereby effectively alleviating individual capacity demands. The proposed strategy is validated through MATLAB/Simulink simulations and hardware-in-the-loop (HIL) real-time results.**

***Index Terms*—Single-line-to-ground (SLG) fault, power router (PR), voltage-current coordinated control, distributed arc suppression, distribution network.**

I. Introduction

WITH the rapid development of modern power systems, the increasing penetration of power electronic converters is reshaping distribution networks into complex hybrid AC/DC systems. Owing to extensive feeder coverage and diverse operating environments, distribution networks experience a high frequency of faults, among which single-line-to-ground (SLG) faults account for more than 70% of all fault types [1]. Under non-effectively grounded neutral systems, such faults tend to trigger arcing overvoltages and sustained arc burning, thereby posing significant threats to equipment insulation and operational reliability [2]. Consequently, the rapid and reliable suppression of ground fault arcs has become a critical requirement for ensuring the secure operation of distribution networks.

In distribution networks with high penetration of power electronic converters and renewable energy sources, the amplitude and spectral characteristics of single-line-to-ground fault currents may differ significantly from those in conventional systems [3]. Meanwhile, due to line electromagnetic coupling and three-phase load asymmetry, zero-sequence voltage unbalance commonly exists even under steady-state operating conditions [4], [5]. These characteristics impose higher requirements on fault analysis and arc suppression in modern distribution networks. Owing to their inherently passive nature, traditional arc suppression coils (ASCs) are incapable of compensating for the active and harmonic components of the fault current [6]. To address this limitation, active arc suppression technologies based on power electronic converters have been proposed, which enhance ground fault mitigation capability by injecting controllable active, reactive, and harmonic currents.

Existing approaches predominantly employ active compensation devices installed at the neutral point of substation. Representative implementations include single-phase inverters interfaced through step-up transformers for neutral-point voltage regulation [7], [8], cascaded H-bridge (CHB) converters for adaptive voltage compensation [9], [10], and hybrid configurations combining phase-power-fed arc suppression devices with CHB-based converters for arc extinction [11]. Furthermore, some schemes attempt to directly integrate three-phase CHB or four-leg converters into the distribution network. Supported by DC-side capacitors or energy storage units, these schemes regulate the system's zero-sequence voltage to suppress fault currents while simultaneously achieving active and reactive power compensation [12], [13]. Some hybrid four-leg converters can perform mode transitions between reactive power compensation and fault regulation, thereby enabling multifunctional operation under normal and fault conditions [14], [15]. A four-leg voltage source converter (VSC) with independent phase control can also provide ground-fault compensation while maintaining power supply continuity [16].

However, most of the aforementioned schemes rely on dedicated, large-capacity arc suppression devices centrally installed at the substation side [17]. Some topologies also require independent DC power supplies, resulting in complex

This work was supported by the National Natural Science Foundation of China under Grant No. 52307148.(Corresponding author: Jinrui Tang.)

Jinmu Lai is with the School of New Energy and Electrical Engineering, Wuhan University of Technology, Wuhan 430070, China, and also with the School of Electrical and Information Engineering, Zhengzhou University, Zhengzhou 450001, China (e-mail: laijinmu@whut.edu.cn; laijinmu@zzu.edu.cn).

Zhu Li and Junhong Chen are with the School of Electrical and Information Engineering, Zhengzhou University, Zhengzhou 450001, China (e-mail: lizhu1115@gs.zzu.edu.cn; chenjunhong1004@gs.zzu.edu.cn).

Jun Liang is with the School of Engineering, Cardiff University, Cardiff CF24 3AA, U.K. (e-mail: LiangJ1@cardiff.ac.uk).

Jinrui Tang, Fan Xiao, and Xin Yin are with the School of Automation, Wuhan University of Technology, Wuhan 430070, China (e-mail: tangjinrui@whut.edu.cn; xiaofan@whut.edu.cn; yinxin@whut.edu.cn).

system structures and high investment costs. Moreover, these devices are functionally single-purpose and remain under low-load or idle conditions for prolonged periods during normal operation, leading to low equipment utilization and limited engineering economic viability [18].

To address the aforementioned issue of low equipment utilization, leveraging widely distributed power electronic resources on the feeder side of distribution networks for distributed mitigation has attracted increasing research interest. With the development of hybrid AC/DC distribution networks (HDNs), power electronic interfaces such as power routers (PRs) and solid-state transformers (SSTs) have been increasingly deployed to enable flexible interconnection and power flow regulation between the AC and DC sides [19]–[21]. Among these devices, the PR serves as a key power electronic interface in HDNs. It not only possesses controllable fault ride-through (FRT) capability to enhance system stability but also exhibits superior dynamic performance, enabling auxiliary functions beyond basic power transfer. In particular, for distribution network fault management, the coordinated operation of PRs for both power flow regulation and fault handling has been preliminarily demonstrated in relevant pilot projects [22], [23].

In recent years, research on utilizing PRs for fault management in distribution networks has attracted growing attention. Reference [24] employed a modular multilevel converter (MMC)-based power router for fault handling, achieving the functional multiplexing of power transmission and fault regulation. With the continuous expansion of PR application scenarios and the increase in installed capacity within distribution networks, a grounding branch on the DC side of the PR was further introduced in [25], [26]. This allows for the active control of the zero-sequence circuit, thereby realizing the arc suppression function and providing a new technical approach for the safe and stable operation of distribution networks.

However, the participation of PRs in fault handling must be balanced with their primary task of power transmission. Reference [27] provided an in-depth analysis of how the PR capacity proportion during arc suppression affects its transmission characteristics, clarifying that PRs must allocate a portion of their capacity for fault handling during the suppression period. For multi-device scenarios, cooperative arc suppression and proportional capacity allocation among multiple devices were achieved based on the virtual zero-sequence synchronous generator (VZSG) theory in [28]. Nevertheless, the involvement of PRs in the arc suppression process inevitably occupies their finite power capacity. How to realize multi-PR cooperative arc suppression and rational suppression capacity allocation while ensuring secure power transmission still lacks systematic theoretical analysis. Particularly in distribution network scenarios characterized by multiple feeders and multiple PRs, the functional division, capacity allocation, and their impacts on system operational characteristics among different PRs during the arc suppression process have not yet been thoroughly studied.

To address the above limitations in multi-feeder distribution networks, this paper proposes a distributed arc suppression strategy based on the cooperative control of multiple power routers (PRs) for SLG faults. During the steady-state operation, distributed current-controlled PRs (CC-PRs) execute active ground parameter compensation (AGPC) to mitigate the zero-sequence voltage. Upon the occurrence of an SLG fault, multiple CC-PRs provide the primary arc suppression current support, while a single voltage-controlled PR (VC-PR) regulates and establishes the zero-sequence voltage reference. This mechanism enables precise control of the fault-point voltage, thereby achieving effective arc suppression. The main contributions of this paper are summarized as follows:

1) A distributed arc suppression framework based on the cooperative control of multiple power routers (PRs) is proposed for SLG faults in distribution networks. The proposed framework enables PRs to perform AGPC in the steady state and arc suppression in the fault state, thereby unifying zero-sequence voltage regulation and fault mitigation within the same hardware infrastructure.
2) A voltage-current coordinated control strategy for multi-PR arc suppression is developed. The CC-PRs provide adjustable fault-current compensation, while the VC-PR regulates the residual fault voltage through a unified voltage reference. In this way, accurate fault-point voltage suppression and flexible sharing of arc suppression effort among multiple PRs are achieved.
3) An analytical model for the arc suppression process in multi-PR distribution networks is established. Based on this model, the power and capacity allocation relationships of different PRs are derived, which reveal the capacity-sharing mechanism of the proposed strategy and provide a quantitative basis for PR sizing and coordinated control design.

II. System Configuration and Operating Principle

A. Topology of Distribution Network with Multiple PRs

Figure 1 illustrates the topology of a distribution network integrated with multiple PRs. This system comprises multiple feeders and loads, with PRs distributed and connected across various feeders. Relevant DC equipment, including photovoltaic (PV) generation systems and distributed energy resources (DERs), can be connected to their DC sides, forming independent local distribution zones. To ensure system safety and stability, regardless of whether it is in steady-state operation or arc suppression mode, the DC grid connected to each PR must operate within its maximum power limits, thereby guaranteeing the normal transmission of both AC and DC networks.

PRs integrated into distribution networks can be realized with different converter topologies, such as CHB- and MMC-based structures [11], [25]. In this paper, an MMC-based PR is adopted as the studied object. It should be noted that the proposed arc suppression strategy is not strictly limited to the MMC topology. This topology is selected because its DC grounding branch provides a controllable zero-sequence path for voltage/current regulation. For other PR topologies or power electronic devices, the proposed arc suppression strategy can also be extended if they can provide controllable zero-sequence current injection and zero-sequence voltage

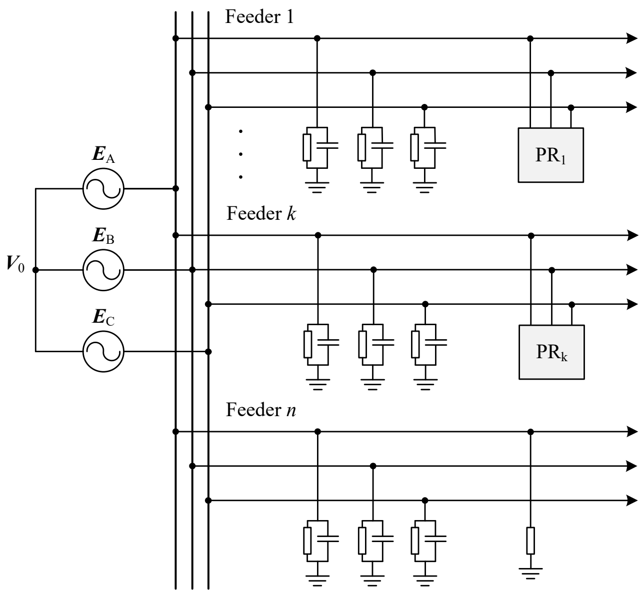

Fig. 1. Topology of distribution network with multiple PRs.

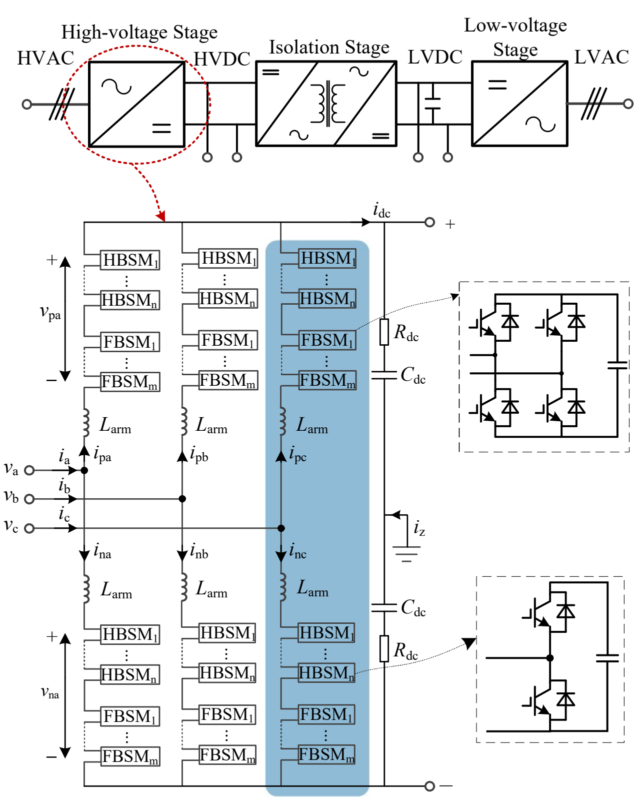

Fig. 2. Topology of MMC-PR.

regulation. The adopted MMC-PR consists of high-voltage, medium-voltage, and low-voltage stages. The arc suppression function investigated in this paper is mainly concentrated in the high-voltage stage of MMC [27]. As shown in Fig. 2, the MMC-PR is directly connected to the distribution network without an isolation transformer.

The MMC consists of three-phase arms, where each arm

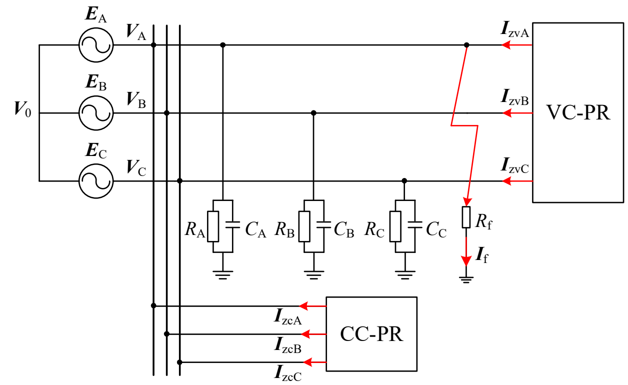

Fig. 3. Equivalent topology of CC-PR and VC-PR with arc suppression under an SLG fault condition.

contains an arm inductor L_{arm} and N submodules comprising a proportional configuration of full-bridge submodules (FBSMs) and half-bridge submodules (HBSMs). To construct a zero-sequence current path for arc suppression, a DC grounding branch is added to the traditional three-phase MMC. The grounding branches at both the positive and negative DC poles each consist of a capacitor C_{dc} and a resistor R_{dc} connected in series.

In Fig. 2, v_a, v_b, v_c and i_a, i_b, i_c denote the three-phase AC voltages and currents, respectively. For phase j ($j = a, b, c$), v_{pj} and v_{nj} represent the output voltages of the upper and lower arm submodules, while i_{pj} and i_{nj} are the corresponding arm currents. Furthermore, V_{dc} and i_{dc} denote the pole-to-pole DC voltage and DC-side current. Finally, i_z is the zero-sequence current flowing through the DC grounding branch of the PR during the arc suppression period.

B. Principle of SLG Fault Regulation

In the proposed multi-PR cooperative arc suppression scheme, the n PRs are classified into two categories, i.e., CC-PRs and one VC-PR. Specifically, the $(n-1)$ units are configured as CC-PRs, and one unit operates as a VC-PR. For analytical convenience, the $(n-1)$ CC-PRs can be modeled as a single equivalent centralized controlled current source. In a 10-kV non-effectively grounded AC distribution network, the fault current of an SLG fault is primarily supplied by the line-to-ground leakage capacitance. The extensive installation of underground cables during urbanization has led to a significant increase in this fault current [17], [18]. If a single PR is required to provide the entire arc suppression current, its required power rating becomes excessive, thereby substantially increasing equipment costs. Therefore, multiple PRs are required to operate cooperatively to share the arc suppression current. To this end, this paper proposes a cooperative arc suppression strategy utilizing CC-PRs and a VC-PR. Assuming an SLG fault occurs in phase A and the line impedance is neglected, the corresponding equivalent circuit is shown in Fig. 3.

In Fig. 3, $\boldsymbol{E}_{\text{A}}$, $\boldsymbol{E}_{\text{B}}$, $\boldsymbol{E}_{\text{C}}$ and $\boldsymbol{V}_{\text{A}}$, $\boldsymbol{V}_{\text{B}}$, $\boldsymbol{V}_{\text{C}}$ denote the three-phase power supply and phase-to-ground voltage phasors, respectively. $\boldsymbol{V}_0$ is the neutral-point voltage phasor. For phase

j ($j = \mathrm{A,B,C}$), R_j and C_j represent the equivalent phase-to-ground resistance and capacitance of the lines. R_f denotes the fault resistance. Furthermore, $\boldsymbol{I}_{zv\mathrm{A}}$, $\boldsymbol{I}_{zv\mathrm{B}}$, and $\boldsymbol{I}_{zv\mathrm{C}}$ are the currents injected by the VC-PR, whereas $\boldsymbol{I}_{zc\mathrm{A}}$, $\boldsymbol{I}_{zc\mathrm{B}}$, and $\boldsymbol{I}_{zc\mathrm{C}}$ represent the currents injected by the CC-PR. The positive directions of the PR-injected current phasors are defined as flowing from the PR grounding branches into the AC network, whereas the fault current is defined as flowing from the AC network into the ground.

In practical lines, the degree of asymmetry is typically 0.5% to 1.5%, and can reach up to 3.5% under severe conditions [4]. Under three-phase asymmetric conditions, a zero-sequence voltage is generated in the distribution network, indicating that the neutral-point voltage is non-zero. According to Kirchhoff's current law (KCL), during the normal operation of the distribution network, the following is satisfied:

$$(\boldsymbol{V}_0 + \boldsymbol{E}_\mathrm{A})Y_\mathrm{A} + (\boldsymbol{V}_0 + \boldsymbol{E}_\mathrm{B})Y_\mathrm{B} + (\boldsymbol{V}_0 + \boldsymbol{E}_\mathrm{C})Y_\mathrm{C} = 0 \tag{1}$$

where $Y_j = \frac{1}{R_j} + \mathrm{j}\omega C_j$ are the phase-to-ground admittance phasors. Consequently, the expression for the zero-sequence voltage is given by:

$$\boldsymbol{V}_0 = -\frac{\boldsymbol{E}_\mathrm{A}(Y_\mathrm{A} + a^2 Y_\mathrm{B} + aY_\mathrm{C})}{Y_\mathrm{A} + Y_\mathrm{B} + Y_\mathrm{C}} \tag{2}$$

where a is the rotation operator, given by $a = -\frac{1}{2} + \mathrm{j}\frac{\sqrt{3}}{2}$. Under asymmetric parameter conditions, the distribution network generates a zero-sequence voltage, which adversely affects the normal operation of the system. By controlling the CC-PRs to inject a zero-sequence current to compensate for this parameter asymmetry, the zero-sequence voltage can be suppressed to zero. Assuming the injected zero-sequence current is $\boldsymbol{I}_\mathrm{s}$, the following relationship holds:

$$\boldsymbol{I}_\mathrm{s} = (\boldsymbol{V}_0 + \boldsymbol{E}_\mathrm{A})Y_\mathrm{A} + (\boldsymbol{V}_0 + \boldsymbol{E}_\mathrm{B})Y_\mathrm{B} + (\boldsymbol{V}_0 + \boldsymbol{E}_\mathrm{C})Y_\mathrm{C} \tag{3}$$

By injecting the zero-sequence compensation current $\boldsymbol{I}_\mathrm{s}$ via the CC-PRs, the zero-sequence voltage can be effectively suppressed. Consequently, the compensated zero-sequence voltage is given by:

$$\boldsymbol{V}_0 = \frac{\boldsymbol{I}_\mathrm{s} - \boldsymbol{E}_\mathrm{A}(Y_\mathrm{A} + a^2 Y_\mathrm{B} + aY_\mathrm{C})}{Y_\mathrm{A} + Y_\mathrm{B} + Y_\mathrm{C}} \tag{4}$$

To force the zero-sequence voltage to zero under asymmetric parameter condition, the injected current must be equal to the inherent unbalanced current of the system, denoted as $\boldsymbol{I}_\mathrm{unb}$, which yields:

$$\boldsymbol{I}_\mathrm{s} = \boldsymbol{E}_\mathrm{A}(Y_\mathrm{A} + a^2 Y_\mathrm{B} + aY_\mathrm{C}) = \boldsymbol{I}_\mathrm{unb} \tag{5}$$

When an SLG fault occurs, the total injected current $\boldsymbol{I}_\mathrm{z}$ required to achieve arc suppression satisfies the KCL equation as follows:

$$\boldsymbol{I}_\mathrm{z} = \boldsymbol{V}_\mathrm{A}(Y_\mathrm{A} + G_\mathrm{f}) + \boldsymbol{V}_\mathrm{B} Y_\mathrm{B} + \boldsymbol{V}_\mathrm{C} Y_\mathrm{C} \tag{6}$$

Since the neutral-point voltage is non-zero during the fault period, the phase-to-ground voltage satisfies $\boldsymbol{V}_j = \boldsymbol{E}_j + \boldsymbol{V}_0$. Substituting this relationship into (6) yields:

$$\begin{aligned} \boldsymbol{I}_\mathrm{z} = \boldsymbol{V}_0(Y_\mathrm{A} + Y_\mathrm{B} + Y_\mathrm{C} + G_\mathrm{f}) + \\ \boldsymbol{E}_\mathrm{A}(Y_\mathrm{A} + a^2 Y_\mathrm{B} + aY_\mathrm{C} + G_\mathrm{f}) \end{aligned} \tag{7}$$

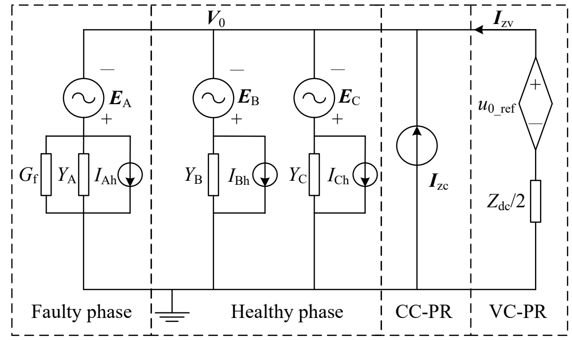

Fig. 4. Equivalent circuit of CC-PR and VC-PR with arc suppression under an SLG fault condition.

After achieving arc suppression, the fault current at the fault location drops to zero, and the voltage of the faulted phase is consequently reduced to zero. As a result, the zero-sequence voltage is equal to the negative of the power supply voltage phasor of the faulted phase, i.e., $\boldsymbol{V}_0 = -\boldsymbol{E}_\mathrm{A}$. Therefore, the total injected current $\boldsymbol{I}_\mathrm{z}$ during the arc suppression period must satisfy the following equation:

$$\boldsymbol{I}_\mathrm{z} = \boldsymbol{E}_\mathrm{A}(Y_\mathrm{A} + a^2 Y_\mathrm{B} + aY_\mathrm{C}) - \boldsymbol{E}_\mathrm{A}(Y_\mathrm{A} + Y_\mathrm{B} + Y_\mathrm{C}) \tag{8}$$

It can be deduced from (8) that the required arc suppression current consists of the system's inherent unbalanced current $\boldsymbol{I}_\mathrm{unb}$ and the current determined by the total zero-sequence admittance. Currently, the widespread use of underground cables in distribution networks significantly increases the phase-to-ground capacitive current. Therefore, coordinating CC-PRs and a VC-PR for arc suppression effectively reduces the power capacity requirement of any individual PR. Furthermore, practical distribution networks exhibit asymmetric line parameters, and the large-scale integration of renewable energy sources introduces background harmonics. Considering these practical conditions, the equivalent circuit of CC-PR and VC-PR with arc suppression is illustrated in Fig. 4.

Based on the preceding analysis, the total current required for fault arc suppression is denoted as $\boldsymbol{I}_\mathrm{z}$. The CC-PRs, modeled as an equivalent current source outputting $\boldsymbol{I}_\mathrm{zc}$, undertake the primary task of arc suppression. Concurrently, the VC-PR, modeled as a controlled voltage source, clamps the voltage of the faulted phase to zero, thereby regulating the residual fault current following the CC-PR compensation as well as the harmonic current $\boldsymbol{I}_\mathrm{h}$. Consequently, the current that must be injected by the VC-PR is given by:

$$\boldsymbol{I}_\mathrm{zv} = \boldsymbol{I}_\mathrm{z} + \boldsymbol{I}_\mathrm{h} - \boldsymbol{I}_\mathrm{zc} \tag{9}$$

Through the functional coordination between the CC-PRs and the VC-PR, voltage-current coordinated arc suppression is achieved. This approach not only ensures precise control over the fault current but also avoids the excessive capacity burden on any individual PR.

C. Mathematical Modeling and Power Analysis of PRs Considering Arc Suppression

When an SLG fault occurs in the distribution network, the CC-PR is controlled to perform current-based arc suppression.

The total single-phase phase-to-ground parameters of the system, denoted as $\sum R_0$ and $\sum C_0$, can be acquired using well-established methods [29], [30]. By injecting a zero-sequence current, the CC-PR compensates for the capacitive component of the fault current. The additional capacity occupation S_{as} required during this process is expressed as:

$$\begin{aligned} S_{\text{as}} &= \frac{1}{3}(\boldsymbol{V}_{\text{A}} + \boldsymbol{V}_{\text{B}} + \boldsymbol{V}_{\text{C}})\boldsymbol{I}_{\text{z}}^{*} + 2\left|\frac{\boldsymbol{I}_{\text{z}}}{2}\right|^2 Z_{\text{dc}} \\ &= -\boldsymbol{E}_{\text{A}}\boldsymbol{I}_{\text{z}}^{*} + 2\left|\frac{\boldsymbol{I}_{\text{z}}}{2}\right|^2 Z_{\text{dc}} \end{aligned} \tag{10}$$

where the first term represents the capacity occupation associated with zero-sequence current injection, and the second term represents the additional capacity occupation of the positive- and negative-pole grounding branches.

By introducing a current allocation coefficient k ($0 < k < 1$), defined as the ratio of the CC-PR output current $\boldsymbol{I}_{\text{zc}}$ to the total phase-to-ground capacitive current of the grid, the current injected by the CC-PR for arc suppression is given by:

$$\boldsymbol{I}_{\text{zc}} = -3\boldsymbol{E}_{\text{A}}\text{j}\omega\Sigma C_0 k \tag{11}$$

The impedance of the DC-side grounding branch Z_{dc} is given by:

$$Z_{\text{dc}} = R_{\text{dc}} + \frac{1}{\text{j}\omega C_{\text{dc}}} \tag{12}$$

Consequently, the additional power occupied by the CC-PR for arc suppression can be expressed as:

$$\begin{aligned} S_{\text{as,c}} &= -3\text{j}\omega\Sigma C_0 k\left|\boldsymbol{E}_{\text{A}}\right|^2 + \\ &\frac{9}{2}\left|\boldsymbol{E}_{\text{A}}\text{j}\omega\Sigma C_0 k\right|^2\left(R_{\text{dc}} + \frac{1}{\text{j}\omega C_{\text{dc}}}\right) \end{aligned} \tag{13}$$

The residual fault current after CC-PR compensation is precisely regulated by the VC-PR. The corresponding output current $\boldsymbol{I}_{\text{zv}}$ can be expressed as:

$$\boldsymbol{I}_{\text{zv}} = -3\boldsymbol{E}_{\text{A}}\left[\frac{1}{\Sigma R_0} + \text{j}\omega\Sigma C_0(1-k)\right] \tag{14}$$

Consequently, the additional power required by the VC-PR for arc suppression, denoted as $S_{\text{as,v}}$, can be expressed as:

$$\begin{aligned} S_{\text{as,v}} &= 3\left|\boldsymbol{E}_{\text{A}}\right|^2\left[\frac{1}{\Sigma R_0} - \text{j}\omega\Sigma C_0(1-k)\right] + \\ &\frac{9}{2}\left|\boldsymbol{E}_{\text{A}}\left[\frac{1}{\Sigma R_0} + \text{j}\omega\Sigma C_0(1-k)\right]\right|^2\left(R_{\text{dc}} + \frac{1}{\text{j}\omega C_{\text{dc}}}\right) \end{aligned} \tag{15}$$

The variation of the coefficient k directly impacts the power allocation between the CC-PR and the VC-PR. Fig. 5 illustrates the theoretical curves of the apparent power ($S_{\text{as,v}}$, $S_{\text{as,c}}$), active power ($P_{\text{as,v}}$, $P_{\text{as,c}}$), and reactive power ($Q_{\text{as,v}}$, $Q_{\text{as,c}}$) for both the CC-PR and VC-PR during arc suppression as k varies. The parameters remain consistent with the subsequent simulations, as detailed in Table I and Table II. As k increases, both the active power $P_{\text{as,v}}$ and reactive power $Q_{\text{as,v}}$ of the VC-PR decrease, whereas $P_{\text{as,c}}$ and $Q_{\text{as,c}}$ of the CC-PR increase. This indicates that the arc suppression power burden gradually shifts toward the CC-PR. Since the arc suppression process is predominantly governed by reactive power, with the active component induced by the phase-to-ground resistance R_0 accounting for an extremely small proportion, the apparent power ($S_{\text{as,v}}$, $S_{\text{as,c}}$) exhibits an approximately linear relationship with k. This demonstrates that k can serve as an equivalent engineering capacity allocation ratio. It should be noted that the coefficient k in the above analysis represents the total current-sharing ratio of the equivalent CC-PR group, which can be further decomposed into the coefficients of individual CC-PRs in a practical multi-PR implementation.

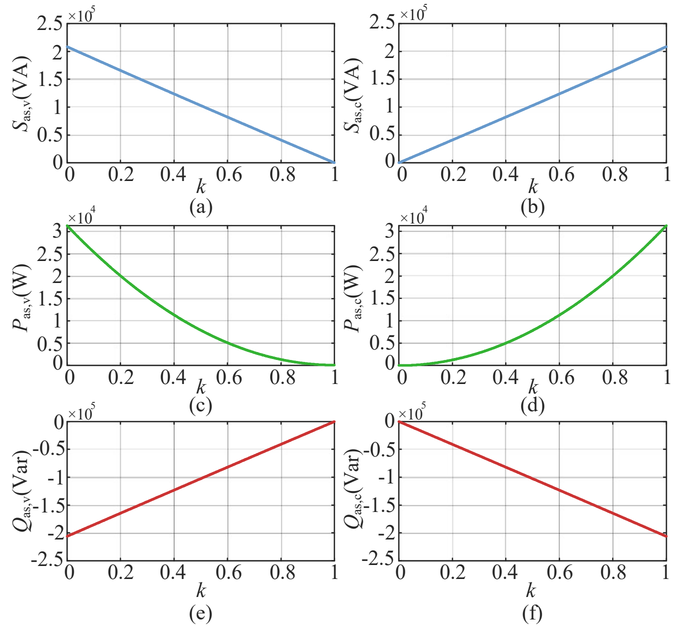

Fig. 5. Power allocation characteristics of CC-PR and VC-PR during arc suppression.

Furthermore, the line length L of the distribution network directly affects the phase-to-ground parameters and the magnitude of the leakage current. Fig. 6 further illustrates the three-dimensional relationship of the arc suppression capacities of the CC-PR and VC-PR with respect to the variations in k and L. It can be clearly observed from the figure that, on the one hand, under the same capacity allocation ratio k, both the arc suppression capacity $S_{\text{as,c}}$ of the CC-PR and $S_{\text{as,v}}$ of the VC-PR exhibit a significant upward trend as the line length L increases. This corroborates the dominant influence of the line length on the arc suppression capacity requirements. Different line types can be incorporated into this analysis through the equivalent phase-to-ground parameters. Since cable feeders generally have larger line-to-ground capacitance than overhead feeders, a higher cable proportion leads to a larger capacitive grounding current and thus higher arc-suppression capacity demand.

On the other hand, for a given line length, the allocation proportion of the arc suppression capacity between the CC-PR and VC-PR consistently demonstrates a linear regulation characteristic with respect to the variation of k. As k increases, the proportion of the capacity borne by the CC-PR continuously rises, while that of the VC-PR correspondingly decreases. Notably, this regulation pattern remains consistent across scenarios with different line lengths.

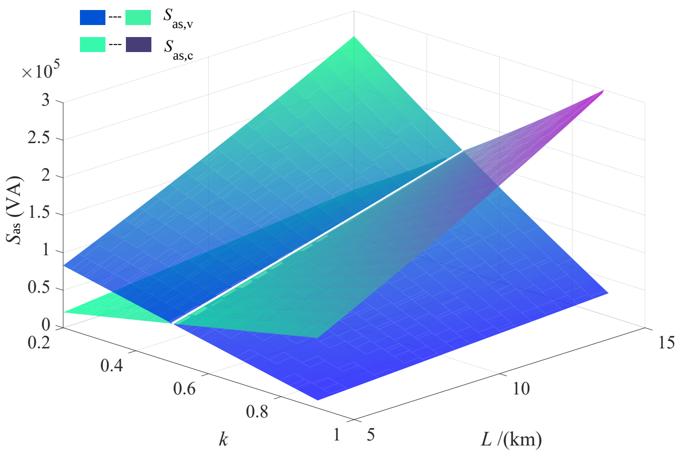

Fig. 6. Diagram of power variation for CC-PR and VC-PR with different k and L values during arc suppression.

Regardless of variations in the distribution network scale, the precise allocation of the arc suppression capacity among multiple PRs can be achieved simply by adjusting the value of k. This ensures that, under the premise of satisfying the arc-suppression requirements, the capacity burden on any single PR is minimized to the greatest extent possible, thereby enhancing the economic efficiency and reliability of the overall system operation.

D. Selection Method of Allocation Coefficient and PRs

In the proposed strategy, the allocation coefficient and the PRs for different control modes are determined in advance according to the feeder configuration, PR ratings, reserved arc-suppression capacities, and equivalent line impedances. The CC-PRs are used to provide the main fault-current compensation, while the VC-PR is used to clamp the residual faulted-phase voltage. Since the PR roles and allocation coefficients are determined in advance, the proposed basic implementation does not require a dedicated real-time communication link between PRs for calculating or updating the compensation references.

For multiple PRs, the PRs with zero-sequence current injection capability and reserved compensation capacity are selected as CC-PRs. The compensation burden of different CC-PRs is allocated according to their reserved arc-suppression capacities, which are generally evaluated based on their rated capacities. The total current-sharing coefficient of the CC-PR group is denoted as k_Σ. Considering the planned capacity sharing between the CC-PR group and the selected VC-PR, k_Σ can be determined by

$$k_\Sigma = \frac{\sum_{m=1}^{N_c} S_{\mathrm{res},m}}{\sum_{m=1}^{N_c} S_{\mathrm{res},m} + S_{\mathrm{res,V}}} \tag{16}$$

where $S_{\mathrm{res},m}$ is the reserved arc-suppression capacity of the m-th CC-PR, $S_{\mathrm{res,V}}$ is the reserved arc-suppression capacity of the selected VC-PR, and N_c is the number of CC-PRs.

The coefficient assigned to the i-th CC-PR is determined by

$$k_i = k_\Sigma \frac{S_{\mathrm{res},i}}{\sum_{m=1}^{N_c} S_{\mathrm{res},m}} \tag{17}$$

where $S_{\mathrm{res},i}$ is the reserved arc-suppression capacity of the i-th CC-PR. Accordingly, the reference current of the i-th CC-PR can be expressed as

$$\boldsymbol{I}_{zc,i} = -3\boldsymbol{E}_{\mathrm{A}}\mathrm{j}\omega\Sigma C_0 k_i \tag{18}$$

The total reference current provided by all CC-PRs is then obtained as

$$\boldsymbol{I}_{zc,\Sigma} = \sum_{i=1}^{N_c} \boldsymbol{I}_{zc,i} = -3\boldsymbol{E}_{\mathrm{A}}\mathrm{j}\omega\Sigma C_0 k_\Sigma \tag{19}$$

Therefore, the equivalent allocation coefficient k used in the analytical model corresponds to k_Σ in the practical multi-PR implementation. This relationship enables the analytical model based on an equivalent CC-PR to be extended to multiple CC-PRs with different reserved capacities.

For resonant grounded systems, the ASC provides an additional passive zero-sequence compensation branch. Compared with the ungrounded case, the proposed PR-based coordination structure remains unchanged, while the current reference of the CC-PRs should be modified according to the residual compensation current after ASC compensation. Under the same current-direction convention, the reference current of the i-th CC-PR can be expressed as

$$\boldsymbol{I}_{zc,i} = -\boldsymbol{E}_{\mathrm{A}}\mathrm{j}\left(3\omega\Sigma C_0 - \frac{1}{\omega L_{\mathrm{ASC}}}\right) k_i \tag{20}$$

where L_{ASC} is the inductance of the ASC. This expression indicates that the required PR compensation current is changed from the total line-to-ground capacitive-current compensation to the residual compensation current after considering the ASC compensation effect. In resonant grounded systems, the CC-PRs share the residual current compensation burden after ASC compensation, while the VC-PR still clamps the residual faulted-phase voltage through voltage closed-loop control.

Changes in the feeder topology can be monitored through the existing SCADA/EMS. When feeder reconfiguration occurs, k_Σ and k_i can be recalculated offline according to the updated network parameters and the predetermined reserved capacities of the PRs, and then transmitted to the local controllers. During the fault transient, the latest valid coefficients remain fixed without real-time redistribution.

The VC-PR is preferably selected from the PRs with smaller equivalent line impedance to the bus at the substation and reliable voltage-control performance, while sufficient reserved arc-suppression capacity should also be ensured. Since the VC-PR is responsible for clamping the residual faulted-phase voltage, a smaller equivalent line impedance can reduce the influence of line voltage drop and improve the effectiveness of voltage clamping [12], [31]. The actual output of the VC-PR is determined by the voltage-clamping control according to the residual faulted-phase voltage after the CC-PR compensation, including the remaining capacitive current component and the small residual component caused by system asymmetry.

Based on the above control-role assignment, although multiple grounding branches provide multiple zero-sequence channels during arc suppression, the proposed scheme does not introduce multiple independently controlled zero-sequence voltage sources. Similar to the voltage-current control-role assignment adopted in coordinated converter systems [32], only one PR operates as the VC-PR to clamp the residual faulted-phase voltage, while the other PRs operate as CC-PRs and inject their assigned zero-sequence compensation currents according to the predetermined coefficients. Since the CC-PRs do not impose independent zero-sequence voltage references on the grounding loops, the principal mechanism of uncontrolled circulating currents caused by competing voltage sources among different PR grounding loops is avoided.

In addition, a backup VC-PR can also be predetermined during offline coordination according to the same selection criteria. If the designated VC-PR is unavailable before fault operation, the backup VC-PR can be selected under the updated operating configuration.

If one CC-PR reaches its current limit or becomes unavailable, only its assigned compensation component is lost. Since the arc-suppression capacity occupied by each CC-PR is generally small compared with the PR rating, the uncompensated residual component can usually be further suppressed by the VC-PR under the designed capacity margin. Therefore, the voltage-clamping function can still be maintained without real-time redistribution of the allocation coefficients.

III. Coordinated Arc Suppression Control Strategy of CC-PR and VC-PR

The CC-PRs and the VC-PR are connected to different feeders within the distribution network. During an SLG fault, distributed coordinated control among multiple PRs is achieved by integrating the voltage- and current-based arc suppression methods. This strategy effectively suppresses the fault current while simultaneously realizing dynamic power coordination among the different PRs, thereby guaranteeing the safe and stable operation of both the distribution network and the PR devices under fault conditions.

A. Current Compensation Control for CC-PR

During an SLG fault, the CC-PR is controlled in current mode for arc suppression, injecting a zero-sequence current to suppress a portion of the fault current and facilitate arc extinction. The control objectives encompass both the fundamental fault current and the inherent unbalanced zero-sequence current of the system. As deduced from (5), the CC-PR executes active ground parameter compensation (AGPC) control during steady-state operation to offset the system's unbalanced current. For the AGPC control, the required phase-to-ground parameters are not fixed manual settings. They can be obtained and updated by existing online parameter measurement or identification methods [29], [30]. Under fault conditions, it injects a specific compensation current based on (11) to realize active current-type arc suppression (ACAS) control. Because the control targets are AC signals at the fundamental grid frequency, a proportional-resonant controller is employed to achieve zero-steady-state-error tracking of the zero-sequence current. The detailed control block diagram is depicted in Fig. 7.

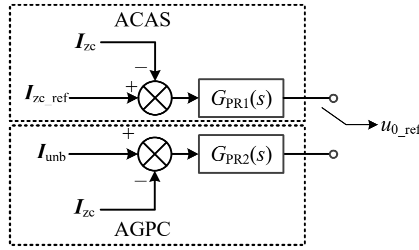

Fig. 7. Block diagram of current compensation control for the CC-PR.

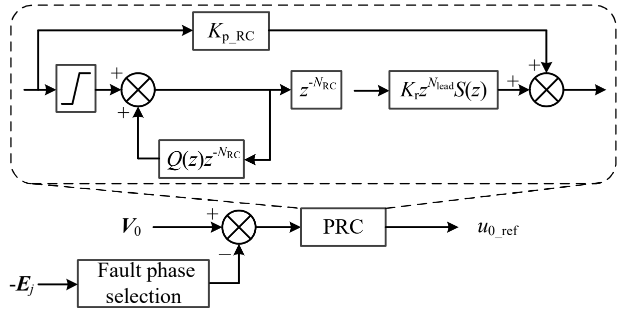

Fig. 8. Block diagram of voltage-based arc suppression control for VC-PR.

The transfer function of the proportional-resonant controller, denoted as $G_{\mathrm{PR}}(s)$, is expressed as:

$$G_{\mathrm{PR}}(s) = k_{\mathrm{p}} + \frac{2k_{\mathrm{r}}\omega_{\mathrm{c}}s}{s^2 + 2\omega_{\mathrm{c}}s + \omega_0^2} \tag{21}$$

where k_{p} is the proportional gain, k_{r} is the resonant gain, ω_{c} is the cutoff frequency, ω_0 is the resonant frequency, and s represents the Laplace operator.

B. Voltage-based Arc Suppression Control for VC-PR

Following the current compensation by the CC-PRs, residual fundamental and harmonic components persist within the fault current. To address this, the VC-PR regulates the residual voltage at the fault location below the arc extinction threshold via voltage-based arc suppression control. Its primary control objective is to regulate the neutral-point voltage to the negative power supply voltage phasor of the faulted phase, yielding $\boldsymbol{V}_0 = -\boldsymbol{E}_j$. This consequently regulates the faulted-phase voltage toward zero, thereby suppressing the conditions for arc reignition and achieving effective arc suppression. In practical distribution networks, the voltage typically contains abundant background harmonics. Conventional proportional-integral (PI) controllers are only suitable for tracking DC components, whereas proportional-resonant controllers struggle to simultaneously suppress multiple harmonic frequencies. Therefore, a proportional-repetitive controller is employed to achieve the precise regulation of the neutral-point voltage. The corresponding control block diagram is depicted in Fig. 8.

In Fig. 8, the parameter N_{RC} is defined as $N_{\mathrm{RC}} = f_{\mathrm{s}}/f_1$, where f_{s} and f_1 denote the sampling frequency and the fundamental frequency, respectively. K_{r} represents the repetitive-controller gain, and $Q(z)$ is a robustness filter designed to enhance the stability of the repetitive-control loop. The term $z^{N_{\mathrm{lead}}}$ provides an N_{lead}-sample phase-lead compensation

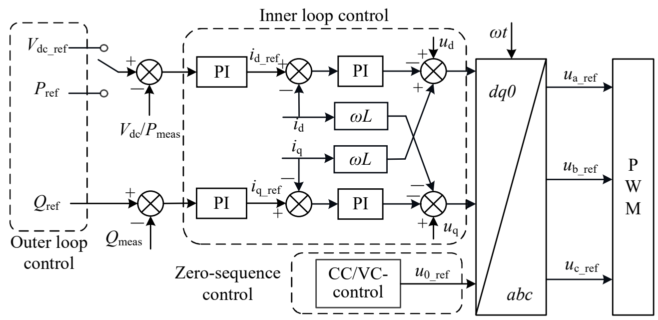

Fig. 9. Overall control block diagram for CC-PR and VC-PR.

to offset the inherent delays introduced by the controller and the controlled plant. $S(z)$ serves as a low-pass filter, further contributing to system stability. Additionally, $K_{\mathrm{p\_RC}}$ is the parallel proportional gain incorporated to accelerate the dynamic response of the control system. This comprehensive scheme regulates the fundamental-frequency component and its integer-order harmonics, thereby achieving fundamental-frequency arc suppression, facilitating arc extinction, and simultaneously suppressing harmonics. Through this strategy, the faulted-phase voltage is regulated toward zero, and the corresponding zero-sequence voltage reference, denoted as u_{0_ref}, is generated for the VC-PR.

C. Distributed Coordinated Control Strategy for Arc Suppression

The PRs on each feeder employ a dq dual-closed-loop control architecture within the synchronous rotating reference frame. The outer loop operates in either the $V_{\mathrm{dc}}Q$ or PQ control mode, achieving independent control over the DC bus voltage (or active power) and reactive power via dq-axis decoupling. Simultaneously, asymmetric parameter compensation and arc suppression control are executed through the zero-sequence channel. Specifically, the zero-sequence voltage reference for the PR is generated using the control logic depicted in Figs. 7 and 8. The three-phase output voltage references are subsequently derived via the inverse Park transformation ($dq0$-abc). These references are then processed by the modulation module to generate the driving signals for the PR submodules. This comprehensive strategy achieves the concurrent regulation of normal power transmission, unbalance mitigation, and transient arc suppression, enabling the normal power-control and zero-sequence-control objectives to be implemented through decoupled control channels. The overall control block diagram is illustrated in Fig. 9.

The analysis of the arc suppression principle involving multiple PRs presented in this paper encompasses both the compensation of asymmetric phase-to-ground parameters by the CC-PRs during steady-state operation and the coordinated control during an SLG fault. During this fault period, $(n-1)$ CC-PRs implement current-based arc suppression control, while a VC-PR executes voltage-based arc suppression control. In practical systems, the coordination among multiple PRs and the continuous monitoring of the system state must be considered. The corresponding control flowchart is illustrated in Fig. 10.

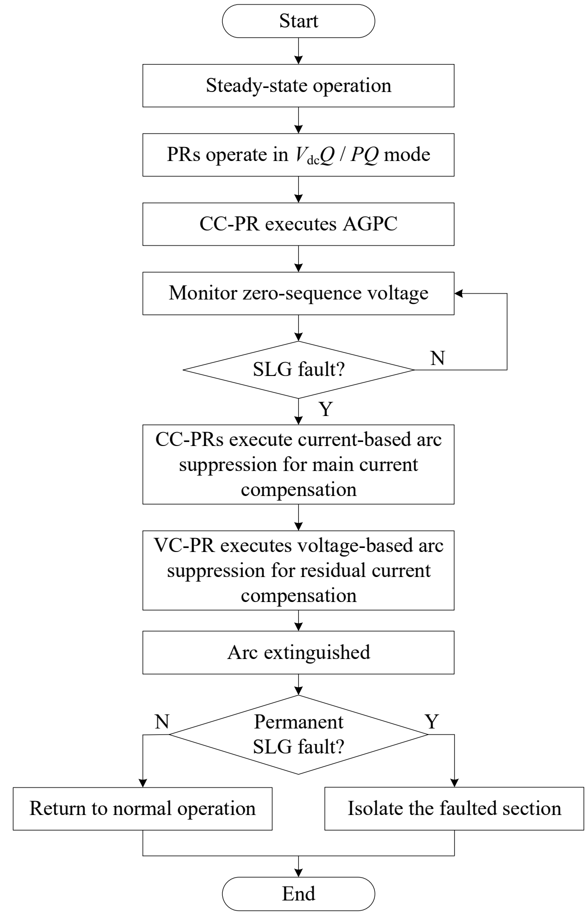

Fig. 10. Control flowchart of the proposed distributed arc suppression strategy.

During steady-state operation, each PR operates in the $V_{\mathrm{dc}}Q$ or PQ mode, continuously monitoring the three-phase and zero-sequence voltages. Upon identifying an asymmetry in the phase-to-ground parameters, the AGPC control of the CC-PR on the corresponding line is activated to suppress the zero-sequence voltage to zero. In the absence of parameter asymmetry, the PR maintains stable operation. If an SLG fault occurs, the ACAS control of the CC-PRs is immediately initiated, operating in coordination with the voltage control of the VC-PR to achieve effective arc suppression.

IV. Simulation Results

A. Simulation Model

To verify the effectiveness of the proposed distributed coordinated arc suppression strategy using multiple PRs, a 10-kV distribution network simulation model is developed in MATLAB/Simulink, as depicted in Fig. 11. The simulated system comprises four feeders, with the PRs integrated into Feeder 1 and Feeder 4. Within this model, the multiple PRs are equivalently represented by two distinct units corresponding to the CC-PR and the VC-PR. Here, PR_1 represents the CC-PR, while PR_2 represents the VC-PR. The specific parameters of these PRs are detailed in Table I. The line models incorporate

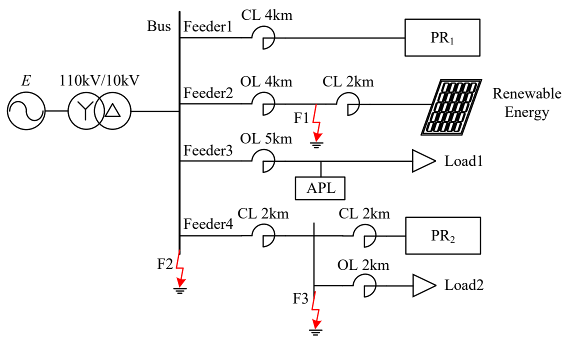

Fig. 11. Topology of simulation model.

TABLE I
DISTRIBUTION NETWORK AND PR PARAMETERS

Parameter	Value
Line voltage	10 kV
System frequency	50 Hz
Fault resistance	50, 100, 500, 1000 Ω
DC voltage	± 10 kV
DC grounding impedance $Z_{\rm dc}$	1000 μF, 50 Ω
CC-PR rated capacity	2.5 MVA
VC-PR rated capacity	2.5 MVA
Submodules per arm	15
Arm inductance	40 mH
SM capacitor voltage	2000 V
SM capacitance	2 mF
SM IGBT voltage rating	3300 V
SM IGBT current rating	180 A

both cable lines (CL) and overhead lines (OL). To emulate the asymmetric phase-to-ground parameters typical of practical distribution networks, an adjustable parameter line (APL) is introduced into Feeder 3. The phase-to-ground capacitances for phases A, B, and C of this line are set to 4 μF, 4 μF, and 3 μF, respectively, while the phase-to-ground resistance is specified as 200 kΩ. The detailed parameters for the overhead and cable lines are provided in Table II. According to practical neutral-grounding requirements, resonant grounding or other compensated grounding methods should generally be considered for medium-voltage distribution systems with relatively large line-to-ground capacitive currents [33], [34]. Therefore, both the resonant grounding and the ungrounded cases are adopted as the benchmark for evaluating the proposed method. Furthermore, to evaluate the performance of the arc suppression under different fault conditions, four fault resistance values are selected – 50 Ω, 100 Ω, 500 Ω, and 1000 Ω. Three distinct fault locations, designated F1, F2, and F3, are established to evaluate the proposed method under different fault resistances and fault locations.

The key parameters of the proportional–resonant and repetitive controllers used in the simulations are listed in Table III. These parameters are selected to balance steady-state tracking accuracy, transient response, and control robustness.

B. Simulation of AGPC with CC-PR under Asymmetric Parameters

During the initial simulation stage, both the CC-PR and the VC-PR operate in the power transmission mode, transferring

TABLE II
LINE PARAMETERS

Line Type	Sequence	Resistance /(Ω/km)	Inductance /(mH/km)	Capacitance /(μF/km)
Overhead line	Positive	0.1250	1.3000	0.0096
	Zero	0.2750	4.6000	0.0054
Cable line	Positive	0.2700	0.2550	0.3390
	Zero	2.7000	1.0190	0.2800

TABLE III
KEY CONTROLLER PARAMETERS USED IN THE SIMULATIONS

Parameter	Value
$k_{p\_{\rm AGPC}}$	5
$k_{r\_{\rm AGPC}}$	3600
$k_{p\_{\rm ACAS}}$	5
$k_{r\_{\rm ACAS}}$	800
ω_c	1 rad/s
ω_0	314.159 rad/s
$K_{p\_{\rm RC}}$	1.2
$K_{r\_{\rm RC}}$	1.2
$Q(z)$	0.97
$S(z)$	$(1+2z^{-1}+z^{-2})/4$
$N_{\rm RC}$	500
$N_{\rm lead}$	6
T_s	40 μs
f_s	25 kHz
f_1	50 Hz

active powers of 2 MW and 1 MW to the DC side, respectively. Influenced by the asymmetric phase-to-ground parameters, the system experiences a three-phase voltage unbalance in the steady state, accompanied by a neutral-point voltage shift. At $t = 0.3$ s, the CC-PR initiates the AGPC control strategy. This approach compensates for the system's inherent unbalanced components by measuring the distribution network phase-to-ground leakage parameters in real time and injecting the appropriately calculated zero-sequence current. As depicted in the simulation results in Fig. 12, after a brief transient regulation by the CC-PR, the neutral-point voltage is effectively suppressed to zero potential, thereby restoring the symmetry of the three-phase voltages. Throughout this procedure, the VC-PR refrains from participating in the zero-sequence regulation, dedicating its operation solely to maintaining AC/DC power transmission.

C. Simulation of the Distributed PRs Arc Suppression Strategy

In this paper, the arc-suppression performance is evaluated considering both the residual fault current and the residual faulted-phase voltage. The residual fault current is used to quantify the remaining fault-current component after compensation, while the residual faulted-phase voltage is used to evaluate the recovery voltage across the fault path and the risk of arc reignition. According to the arc-extinction voltage criterion reported for 10-kV non-effectively grounded distribution networks, the critical arc-extinction peak voltage can be taken as approximately $0.22V_{\rm ph,peak}$, where $V_{\rm ph,peak}$ is the rated phase-voltage peak value [35], [36]. Therefore, the engineering arc-suppression criterion adopted in this paper is defined as

$$V_{\rm f,res,peak} \leq 0.22V_{\rm ph,peak} \tag{22}$$

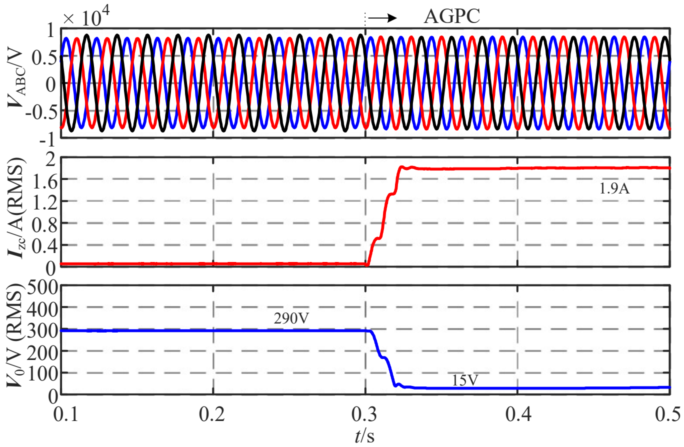

Fig. 12. Simulation waveforms of AGPC strategy using CC-PR under asymmetric phase-to-ground parameter conditions.

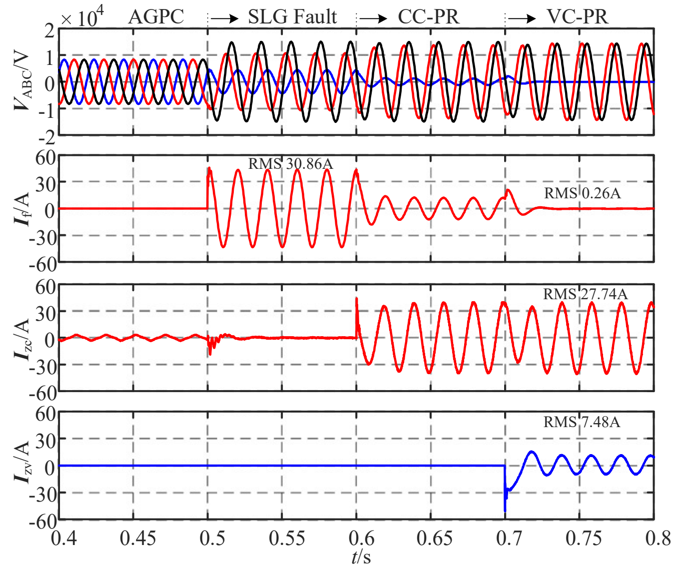

Fig. 13. Simulation waveforms of distributed arc suppression with multiple PRs under an SLG fault at F1 with R_{f} = 100 Ω.

For the 10-kV system studied in this paper, $0.22V_{\mathrm{ph,peak}}$ is approximately 1.80 kV. When the residual faulted-phase voltage remains below this threshold after the control reaches steady state, the adopted arc-suppression criterion is considered to be satisfied. The residual fault-current values are also reported to quantify the compensation performance.

Fig. 13 illustrates the distributed arc suppression simulation waveforms for an SLG fault occurring at location F1. As observed from the figure, during the steady-state phase, the CC-PR injects a zero-sequence current to compensate for the unbalance caused by the asymmetric three-phase-to-ground parameters. At $t = 0.5$ s, the SLG fault with a fault resistance of 100 Ω occurs. Consequently, the voltage of the faulted phase drops precipitously while the voltages of the healthy phases rise, and the RMS value of the fault current reaches 30.86 A. To prevent the DC grounding branch from forming a fault loop that would otherwise increase the current, this branch within the CC-PR executes zero-sequence current blocking and fault ride-through during the fault period. At $t = 0.6$ s, the CC-PR initiates the current-based arc suppression control, which significantly reduces the fault current, although a small residual component remains. Subsequently, at $t = 0.7$ s, the VC-PR activates the voltage-based arc suppression control. This action suppresses both the residual faulted-phase voltage and the residual fault current to low levels, confirming the effectiveness of the proposed arc-suppression strategy. At this stage, the RMS value of the injected current from the CC-PR is 27.74 A, whereas that from the VC-PR is merely 7.48 A. This result indicates that the vast majority of the arc suppression capacity is borne by the CC-PR, leaving only a minor fraction for the VC-PR. This allocation effectively alleviates the capacity demands on the VC-PR while achieving the precise regulation of the fault-point voltage and current. Furthermore, following the fault, the network's total phase-to-ground leakage current flows primarily through the CC-PR and the VC-PR. The currents injected by both types of PRs are completely in phase, and their superposition exactly equals the total phase-to-ground current of the entire distribution network. It should be noted that the activation instants of the CC-PR and VC-PR in the simulation are intentionally separated to distinguish different operating stages. This time separation is used only for stage demonstration and is not a required delay for the proposed method. After fault detection and faulted-phase identification, the CC-PRs and VC-PR can be activated simultaneously for arc suppression.

To evaluate the robustness of the proposed distributed arc suppression strategy, the current allocation ratio is set to $k = 0.8$, and simulation validations were conducted across fault resistances of 50 Ω, 100 Ω, 500 Ω, and 1000 Ω. As shown in Fig. 14, increasing fault resistance results in a gradual rise in the faulted-phase voltage and a corresponding reduction in the fault current magnitude. After activation of the distributed arc suppression control, the injected zero-sequence current rapidly compensates for the fault component, effectively suppressing the residual fault current and maintaining stable arc-suppression performance.

According to the simulation results, after the CC-PR and VC-PR are both activated, the fault current can be reduced to a low level within approximately 40 ms. This indicates that the proposed arc-suppression control has a fast dynamic response after activation.

Once steady state is reached, the CC-PR and VC-PR consistently maintain the preset capacity allocation ratio. The simulation results indicate that the proposed coordinated allocation mechanism is insensitive to variations in fault resistance. Reliable arc suppression is achieved across a wide range of fault resistances while preserving the preset capacity allocation ratio. The corresponding quantitative results are summarized in Table IV.

In practical distribution networks, individual PRs often have different rated capacities. To further evaluate the adaptability of the proposed distributed arc suppression strategy to the coordinated operation of PRs with varying capacities, an additional simulation case was performed with the allocation coefficient set to $k = 0.6$. As indicated in Table V, under

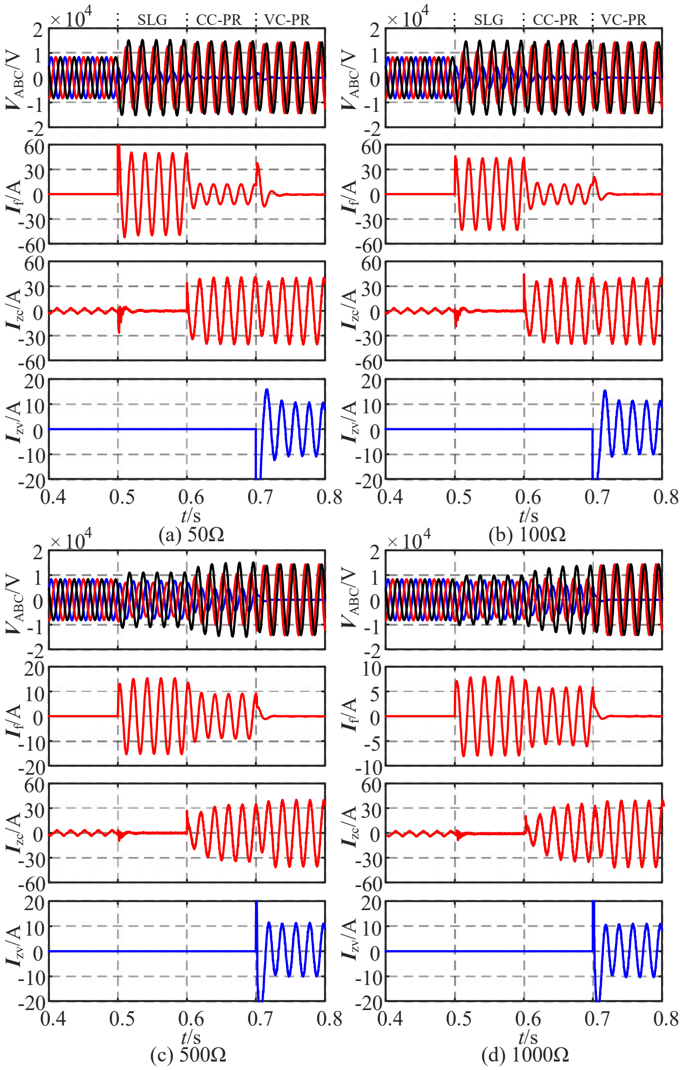

Fig. 14. Simulation waveforms of distributed arc suppression at F1 under different fault resistances with k = 0.8.

TABLE IV
COMPARISON OF DISTRIBUTED ARC-SUPPRESSION PERFORMANCE AT F1 UNDER DIFFERENT FAULT RESISTANCES WITH k = 0.8

Resistance R_f/Ω	Fault I_f/A	Residual $I_{f,res}$/A	CC-PR I_{zc}/A	VC-PR I_{zv}/A
50	35.22	0.48	27.75	7.45
100	30.86	0.26	27.74	7.48
500	10.85	0.03	27.82	7.45
1000	5.64	0.02	27.82	7.45

varying fault resistances during the SLG fault, the actual output currents of the CC-PR and the VC-PR are consistently distributed at approximately a 3:2 ratio. Meanwhile, the fault current is suppressed to a safe level.

A comparison between Tables IV and V shows that the capacity sharing between the CC-PR and the VC-PR can be flexibly adjusted by the preset allocation coefficient. When k is changed from 0.8 to 0.6, the output current of the CC-PR decreases, while that of the VC-PR increases accordingly. Meanwhile, effective fault-current suppression is maintained under both allocation settings.

TABLE V
COMPARISON OF DISTRIBUTED ARC-SUPPRESSION PERFORMANCE AT F1 UNDER DIFFERENT FAULT RESISTANCES WITH k = 0.6

Resistance R_f/Ω	Fault I_f/A	Residual $I_{f,res}$/A	CC-PR I_{zc}/A	VC-PR I_{zv}/A
50	35.22	0.52	21.19	13.96
100	30.92	0.27	21.18	13.99
500	10.85	0.03	21.25	13.96
1000	5.64	0.02	21.26	13.97

TABLE VI
COMPARISON OF DISTRIBUTED ARC-SUPPRESSION PERFORMANCE AT DIFFERENT FAULT LOCATIONS AND FAULT RESISTANCES WITH k = 0.8

Location	Resistance R_f/Ω	Fault I_f/A	Residual $I_{f,res}$/A	CC-PR I_{zc}/A	VC-PR I_{zv}/A
F2	50	35.32	0.58	28.22	7.53
	100	31.14	0.27	28.21	7.58
	500	11.04	0.05	28.21	7.59
	1000	5.73	0.03	28.20	7.58
F3	50	34.91	0.57	27.97	7.41
	100	30.71	0.29	27.87	7.44
	500	10.88	0.06	27.97	7.48
	1000	5.66	0.03	27.98	7.48

Furthermore, Fig. 15 presents the distributed arc suppression waveforms at fault location F2 under $k = 0.8$, and Table VI summarizes the quantitative results at fault locations F2 and F3. The results show that, although the fault location and fault resistance vary, the CC-PR and VC-PR still provide compensation currents according to the preset allocation relationship, and the residual fault current is suppressed to a low level. This verifies that the proposed strategy can maintain stable arc-suppression performance under different fault locations and fault resistances while enabling flexible power sharing among PRs.

To further evaluate the robustness of the proposed method under practical disturbances, additional simulations are conducted considering background harmonic distortion, phase-to-ground parameter estimation error, and measurement noise.

For the background-harmonic test, typical 5th- and 7th-order harmonic voltage components with a peak amplitude of 300 V are superimposed on the grid voltage. At $t = 0.6$ s, the CC-PR and VC-PR are activated simultaneously for arc suppression. The THD values are obtained by FFT analysis using two complete fundamental-frequency cycles under steady-state conditions. As shown in Fig. 16 and Table VII, the THD values of the faulted-phase voltage and fault current are both 9.41% before compensation and become 19.37% and 18.90% after compensation, respectively. Meanwhile, the fundamental voltage and current components are reduced from 3366.1 V and 33.67 A to 64.83 V and 0.66 A, respectively. The 5th- and 7th-order voltage components decrease from 218.3 V and 229.4 V to 6.87 V and 7.61 V, while the corresponding current components decrease from 2.18 A and 2.29 A to 0.07 A and 0.08 A, respectively. Accordingly, the RMS values of 5th- and 7th-order voltage and current harmonic components are reduced by more than 96%. Since conventional THD is normalized by

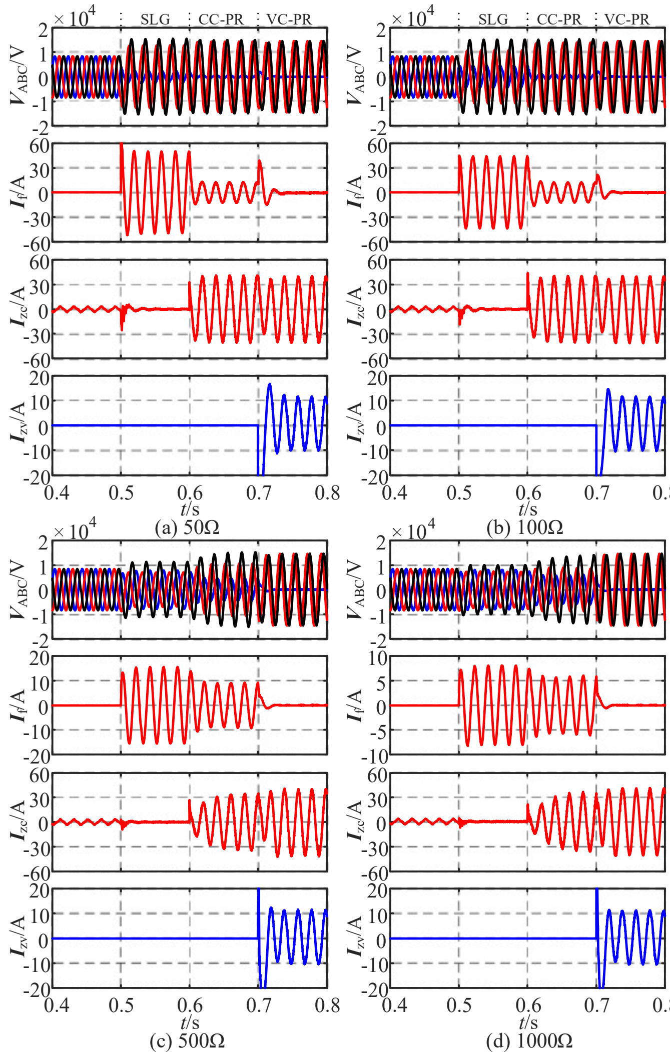

Fig. 15. Simulation waveforms of distributed arc suppression at F2 under different fault resistances with k = 0.8.

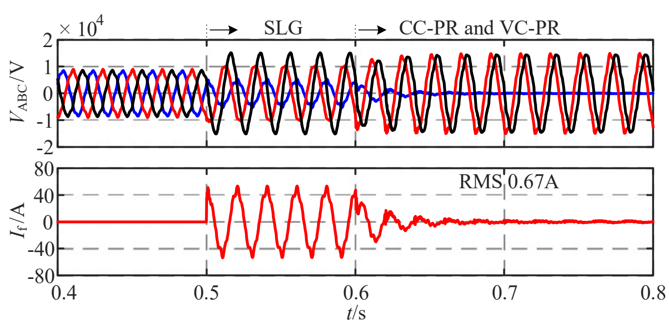

Fig. 16. Simulation waveforms under background harmonic distortion.

TABLE VII
QUANTITATIVE HARMONIC ANALYSIS BEFORE AND AFTER COMPENSATION

Quantity	Before	After
$V_{\mathrm{total,rms}}/\mathrm{V}$	3381.0	66.00
$V_{1,\mathrm{rms}}/\mathrm{V}$	3366.1	64.83
$V_{5,\mathrm{rms}}/\mathrm{V}$	218.3	6.87
$V_{7,\mathrm{rms}}/\mathrm{V}$	229.4	7.61
$\mathrm{THD}_{V_\mathrm{f}}/\%$	9.41	19.37
$I_{\mathrm{total,rms}}/\mathrm{A}$	33.82	0.67
$I_{1,\mathrm{rms}}/\mathrm{A}$	33.67	0.66
$I_{5,\mathrm{rms}}/\mathrm{A}$	2.18	0.07
$I_{7,\mathrm{rms}}/\mathrm{A}$	2.29	0.08
$\mathrm{THD}_{I_\mathrm{f}}/\%$	9.41	18.90

Note: The higher THD after arc suppression results from the reduced fundamental components, while the RMS values of the 5th- and 7th-order voltage and current harmonics decrease by more than 96%.

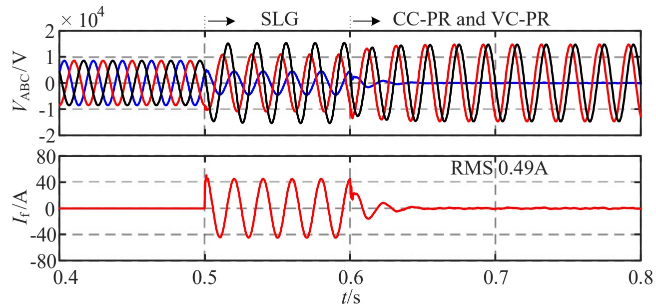

Fig. 17. Simulation results under a 5% phase-to-ground parameter estimation error and 5% Gaussian measurement noise.

the fundamental component, the substantial reductions in the residual fundamental voltage and current components lead to relatively high THD values after arc suppression. Therefore, the increased normalized THD values do not indicate deterioration of the harmonic-suppression performance. Instead, the quantitative results demonstrate effective suppression of both the fundamental and harmonic components, confirming the harmonic-suppression capability of the proportional-repetitive controller under background harmonic distortion.

The effects of phase-to-ground parameter estimation error and measurement noise are further evaluated under the same operating condition. A 5% parameter estimation error is introduced in the controller, while independent zero-mean Gaussian noise with a standard deviation of 5% of the corresponding measurement base is added to the voltage and current feedback signals of both the CC-PR and VC-PR. As shown in Fig. 17, the introduced uncertainties cause only limited fluctuations in the controlled variables, while the residual fault current and residual faulted-phase voltage remain effectively suppressed after control activation. These results confirm that the proposed cooperative control retains its arc-suppression capability under the tested uncertainties.

D. Arc Suppression in Resonant Grounded System

To further verify the applicability of the proposed method to resonant grounded systems, additional simulations are conducted at F1 with an ASC connected to the neutral point under R_f = 50 Ω, 100 Ω, 500 Ω, and 1000 Ω. The SLG fault is introduced at $t = 0.5$ s, the ASC is connected at $t = 0.6$ s, and the CC-PR and VC-PR are simultaneously activated at $t = 0.7$ s. The ASC inductance is set to $L_{\mathrm{ASC}} = 0.65$ H, corresponding to approximately 80% compensation of the total capacitive grounding current. The allocation coefficient is set

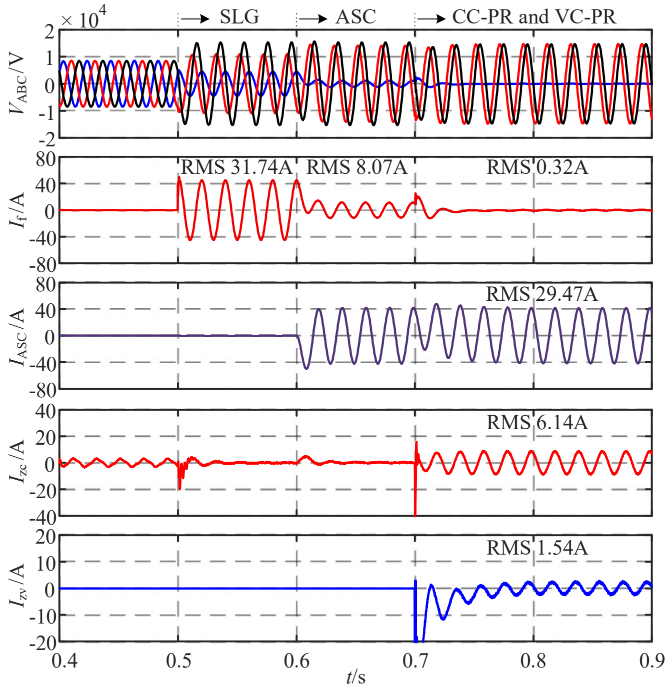

Fig. 18. Simulation waveforms of the proposed arc-suppression strategy in the resonant grounded system at F1 with R_f = 100 Ω.

TABLE VIII
ARC-SUPPRESSION RESULTS IN THE RESONANT GROUNDED SYSTEM

Resistance R_f/Ω	Fault I_f/A	Residual $I_{\mathrm{f,res}}/\mathrm{A}$	ASC $I_{\mathrm{ASC}}/\mathrm{A}$	CC-PR I_{zc}/A	VC-PR I_{zv}/A
50	36.10	0.58	29.55	6.14	1.64
100	31.74	0.32	29.47	6.14	1.54
500	11.17	0.09	29.48	6.14	1.66
1000	5.78	0.04	29.48	6.14	1.67

to $k = 0.8$, and the CC-PR reference current is calculated according to (20) based on the residual compensation current after ASC compensation.

As shown in Fig. 18, the ASC provides the main passive compensation for the capacitive grounding current after the SLG fault occurs. After the coordinated control is activated, the CC-PR compensates for the assigned residual current component, while the VC-PR clamps the residual faulted-phase voltage. Consequently, both the residual fault current and the residual faulted-phase voltage are effectively suppressed.

The corresponding quantitative results are summarized in Table VIII. Since the ASC compensates for most of the capacitive grounding current, the compensation burden of the PRs is reduced. These results verify the effectiveness of the proposed method in a resonant grounded system.

E. Three PRs Cooperative Arc Suppression Case

To further verify the practical multi-PR implementation, an additional simulation case with three MMC-PRs is carried out under the representative fault condition at F1 with $R_\mathrm{f} = 100\ \Omega$. The corresponding topology is shown in Fig. 19. In this case, PR_1 and PR_2 operate as CC-PRs to provide the main zero-sequence current compensation, while PR_3 operates as the VC-PR to clamp the residual faulted-phase voltage. The rated capacities of PR_1, PR_2, and PR_3 are set to 2.5 MVA, 2.5 MVA, and 1.25 MVA, respectively, while their normal active power transfers are 2 MW, 2 MW, and 1 MW, respectively. The allocation coefficients are set as $k_1 = 0.4$, $k_2 = 0.4$, and $1 - k_\Sigma = 0.2$, where $k_\Sigma = k_1 + k_2 = 0.8$. All three PRs are simultaneously activated during the fault.

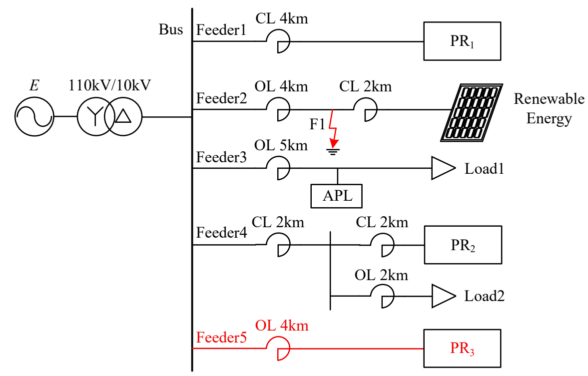

Fig. 19. Topology of the three PRs simulation model.

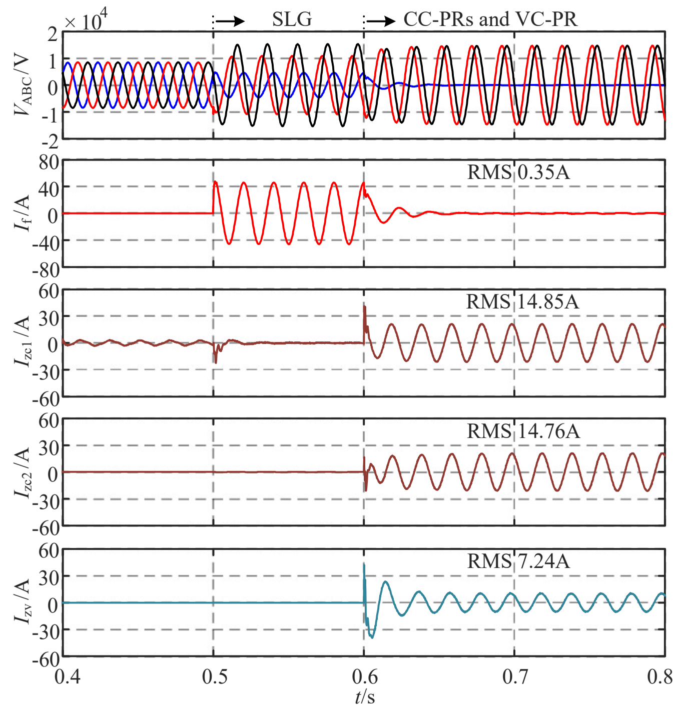

Fig. 20. Cooperative arc-suppression waveforms of the three PRs implementation.

As shown in Fig. 20, PR_1 and PR_2 inject the assigned compensation currents according to the preset allocation coefficients, while PR_3 provides the residual voltage-clamping control. After the three PRs are activated, the residual fault current and residual faulted-phase voltage are both effectively suppressed. These results verify that the equivalent CC-PR in the analytical model can be implemented by multiple independently controlled CC-PRs.

The corresponding converter-level waveforms of the three PRs are further shown in Fig. 21, including the dc-link

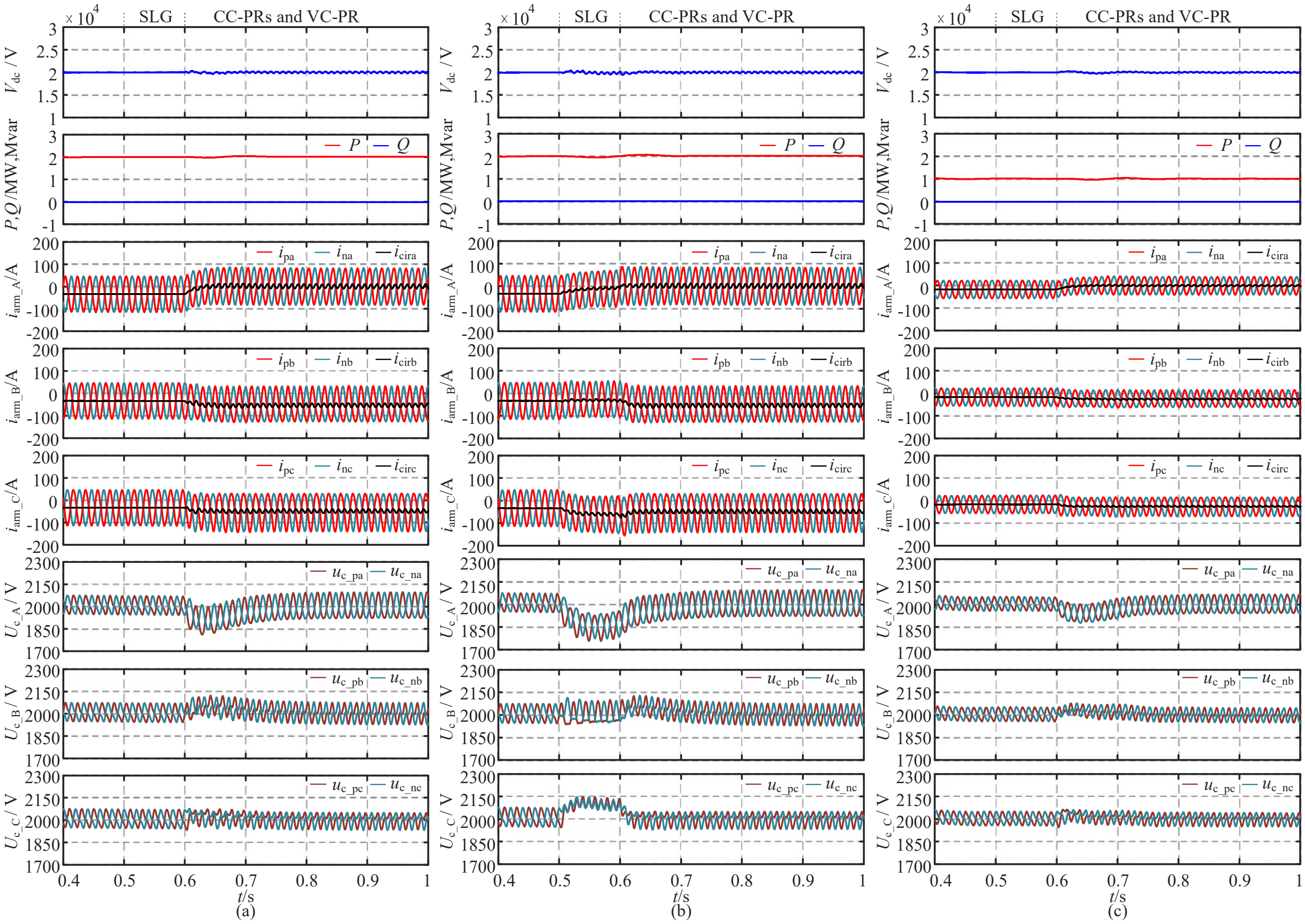

Fig. 21. Converter-level waveforms of the three MMC-PRs: (a) PR_1; (b) PR_2; and (c) PR_3.

voltages, active and reactive powers, arm currents, circulating currents, and submodule capacitor voltages. It can be seen that the dc-link voltages and power transmission remain stable, except for limited transient fluctuations during the control transition. Meanwhile, the arm currents and circulating currents exhibit brief transients following the activation of arc suppression and rapidly settle to new steady-state values. The submodule capacitor voltages remain close to their rated value of 2 kV, with peak-to-peak voltage fluctuations below 200 V, corresponding to less than 10% of the rated voltage. These results indicate that the proposed arc-suppression control does not introduce excessive converter stress or significantly disturb normal AC/DC power transmission under the tested condition.

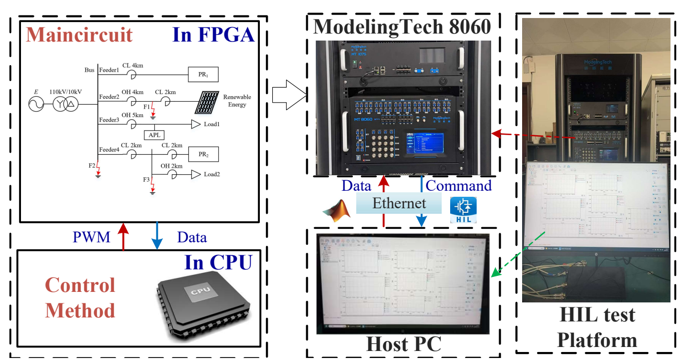

Fig. 22. HIL test platform.

V. HARDWARE-IN-THE-LOOP RESULTS

To further validate the effectiveness and real-time performance of the proposed distributed arc suppression strategy, a hardware-in-the-loop (HIL) experimental platform was established based on the ModelingTech MT8060 real-time simulator, as illustrated in Fig. 22.

The HIL platform employs identical parameter settings to those used in the simulation model to ensure consistency. Owing to the limited FPGA resources available for implementing the main circuit on the HIL platform, multiple detailed MMC-PR models cannot be implemented simultaneously. Therefore, the PRs are equivalently implemented using three-phase H-bridge converters. In the equivalent implementation, a grounding branch is constructed for each three-phase H-bridge converter to provide the required zero-sequence current path. With this zero-sequence path, the H-bridge-based PR can realize the zero-sequence current injection and zero-sequence voltage regulation required by the proposed strategy. Therefore, the H-

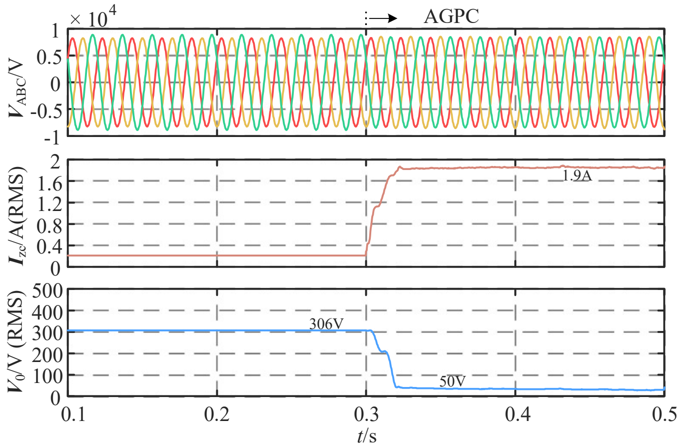

Fig. 23. HIL results of AGPC strategy using CC-PR under asymmetric phase-to-ground parameter conditions.

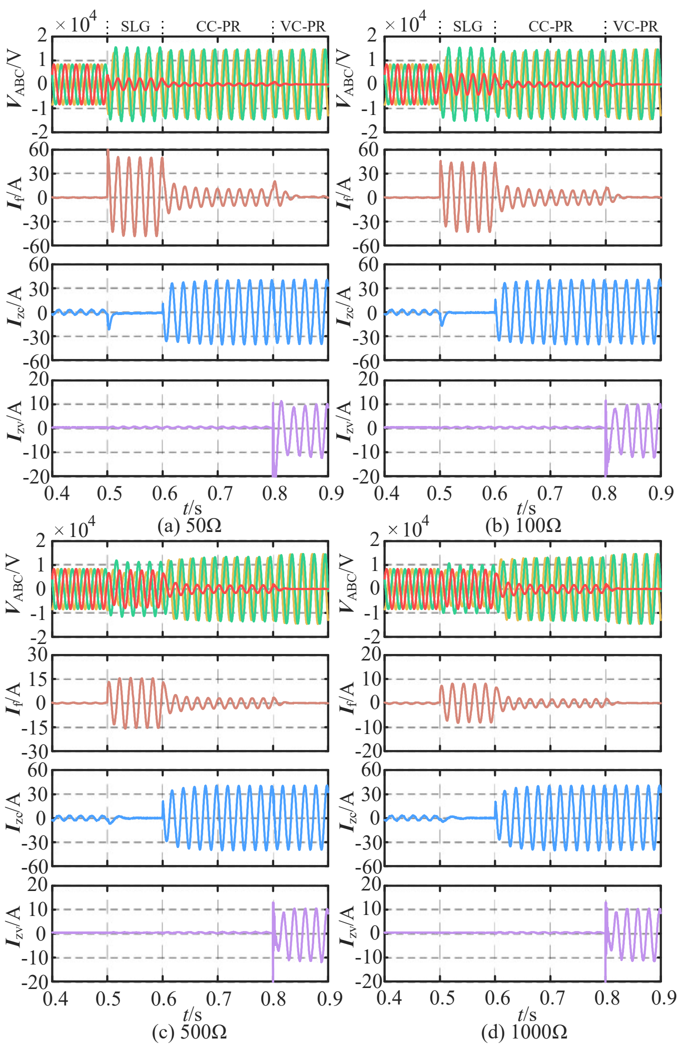

Fig. 24. HIL results of distributed arc suppression at F1 under different fault resistances with k = 0.8.

bridge-based implementation can be used to verify the system-level coordination logic, fault-current compensation, residual faulted-phase voltage clamping, and dynamic response of the

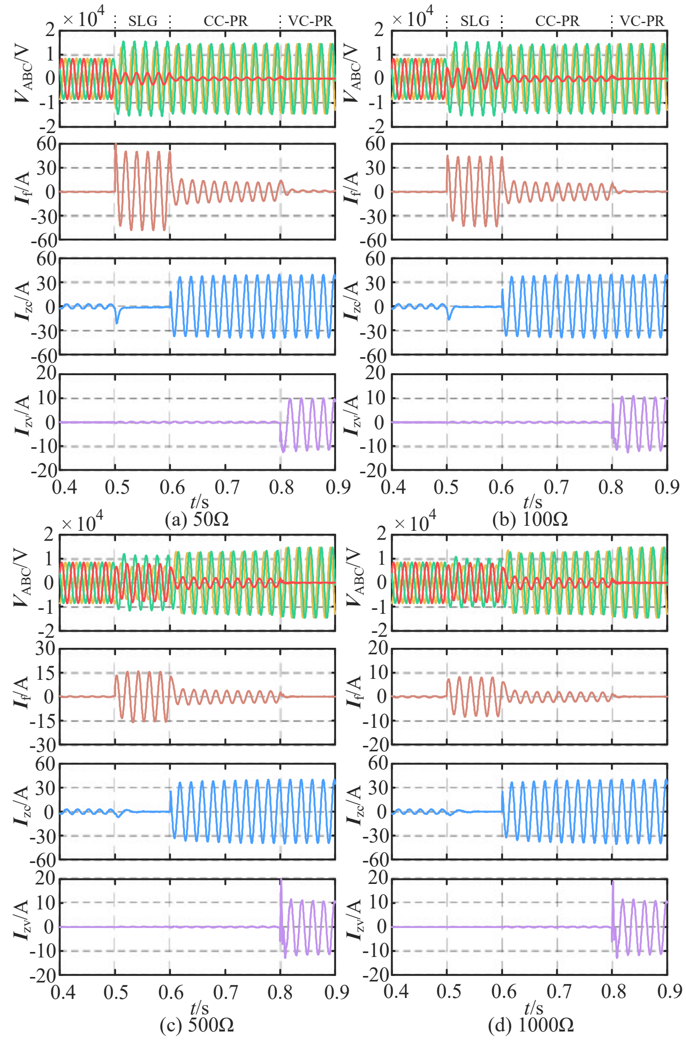

Fig. 25. HIL results of distributed arc suppression at F2 under different fault resistances with k = 0.8.

proposed method. Both the distribution network model and the control algorithm are deployed on the real-time simulator. The network model is executed on the FPGA with a time step of 1 μs, while the control algorithm runs on the CPU with a sampling period of 40 μs.

A. HIL Results of the AGPC Strategy

The HIL results presented in the following sections are utilized to evaluate the suppression performance of the proposed distributed arc suppression strategy under different scenarios. The experimental data are recorded and transferred to the host PC for post-processing and visualization in MATLAB.

To experimentally validate the asymmetric compensation capability of the proposed AGPC strategy, the same operating condition was reproduced on the HIL platform. During the initial stage, both the CC-PR and the VC-PR operated in the power transmission mode.

Due to the inherent phase-to-ground parameter asymmetry, the system exhibited a steady-state three-phase voltage unbalance, accompanied by a neutral-point voltage deviation of approximately 306 V. At t = 0.3 s, the AGPC strategy

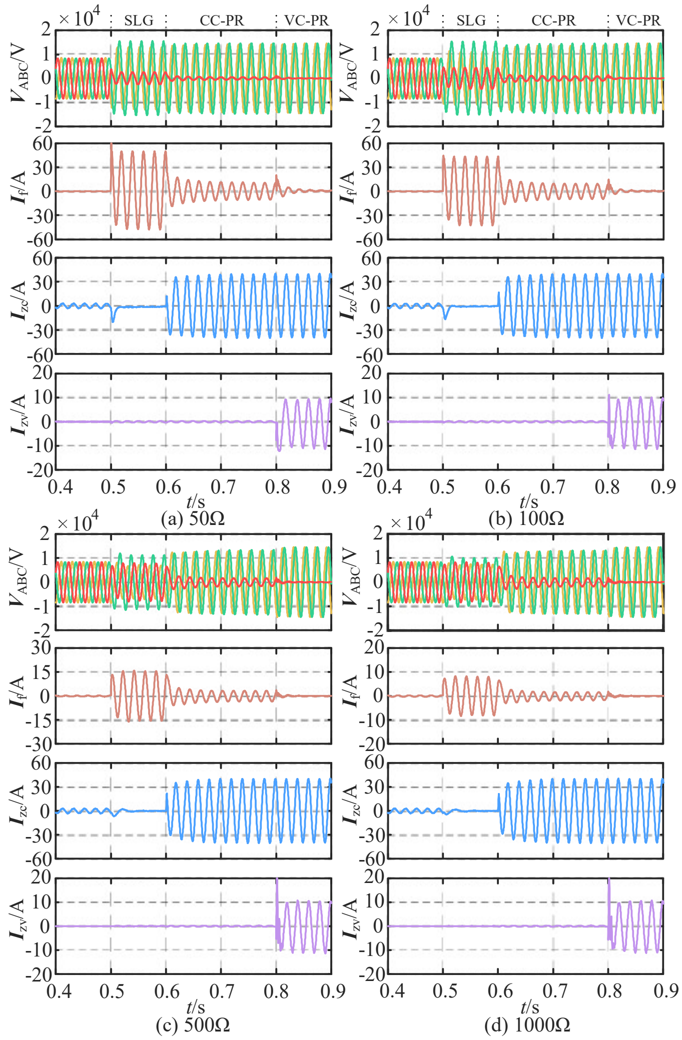

Fig. 26. HIL results of distributed arc suppression at F3 under different fault resistances with k = 0.8.

was activated in the CC-PR. As shown in Fig. 23, the CC-PR injected an asymmetric compensation current of approximately 1.9 A, which effectively mitigated the system unbalance. After a short dynamic adjustment process, the neutral-point voltage was reduced from 306 V to about 50 V, and the three-phase voltage symmetry was significantly improved. The HIL results confirm the effectiveness of the proposed AGPC strategy.

B. HIL Results of the Distributed PRs Arc Suppression Strategy

Figs. 24–26 present the HIL validation results of the proposed distributed arc suppression strategy for SLG faults occurring at F1, F2, and F3, respectively. For each fault location, four fault resistances (50 Ω, 100 Ω, 500 Ω, and 1000 Ω) are examined with the preset allocation coefficient $k = 0.8$. In all cases, the SLG fault is introduced at 0.5 s, the CC-PR is activated at 0.6 s to execute current-based arc suppression, and the VC-PR is activated at 0.8 s to execute voltage-based arc suppression.

The HIL results also show that the fault current can be reduced to a low level within approximately 40 ms after the

TABLE IX
HIL-BASED COMPARISON OF DISTRIBUTED ARC-SUPPRESSION PERFORMANCE AT DIFFERENT FAULT LOCATIONS AND FAULT RESISTANCES WITH k = 0.8

Location	Resistance R_f/Ω	Fault I_f/A	Residual $I_{f,res}$/A	CC-PR I_{zc}/A	VC-PR I_{zv}/A
F1	50	34.84	0.69	28.45	7.76
	100	30.76	0.35	28.43	7.67
	500	10.98	0.07	28.40	7.58
	1000	5.71	0.04	28.43	7.52
F2	50	34.72	0.68	28.29	7.31
	100	30.79	0.38	28.24	7.55
	500	11.06	0.08	28.26	7.69
	1000	5.76	0.04	28.21	7.75
F3	50	34.58	0.61	28.42	7.21
	100	30.58	0.34	28.38	7.38
	500	11.00	0.07	28.39	7.46
	1000	5.74	0.04	28.40	7.47

TABLE X
HIL-BASED COMPARISON OF DISTRIBUTED ARC-SUPPRESSION PERFORMANCE AT F1 UNDER DIFFERENT FAULT RESISTANCES WITH k = 0.6

Resistance R_f/Ω	Fault I_f/A	Residual $I_{f,res}$/A	CC-PR I_{zc}/A	VC-PR I_{zv}/A
50	34.84	0.69	21.37	14.35
100	30.77	0.38	21.30	14.54
500	10.98	0.11	21.26	14.65
1000	5.67	0.04	21.30	14.60

CC-PR and VC-PR are both activated, which further verifies the fast response capability of the proposed method.

Under all tested conditions, the fault current is effectively suppressed after activation of the distributed arc-suppression control, and stable arc-suppression performance is achieved. The suppression performance remains consistent across different fault locations and fault resistances, indicating that the proposed strategy is robust against variations in fault conditions.

A quantitative comparison of the HIL results is summarized in Table IX, including the RMS values of the fault current, residual current, and the injected zero-sequence currents of the CC-PR and VC-PR. The CC-PR consistently provides the majority of the compensation current, while the VC-PR supplies the remaining portion. The measured current ratio closely matches the preset allocation coefficient k, and the superposition of the injected currents from both PRs approximately matches the total phase-to-ground current of the distribution network, verifying the correctness of the current distribution mechanism. To further evaluate the flexibility of the proposed allocation mechanism, additional HIL tests are conducted at F1 with a different preset allocation coefficient ($k = 0.6$), and the corresponding results are summarized in Table X. Compared with the case of $k = 0.8$, the compensation currents of the CC-PR and VC-PR are redistributed in accordance with the adjusted allocation coefficient, while reliable arc suppression performance is maintained, further confirming the capability of flexible capacity allocation among PRs.

Overall, the HIL results demonstrate that the proposed dis-

TABLE XI
QUALITATIVE ENGINEERING COMPARISON OF DIFFERENT ARC-SUPPRESSION SCHEMES

Scheme	Additional device	Capacity burden	Normal utilization	Capacity sharing	Control complexity
Centralized AAS [6], [11]	Required	Centralized	Low	No	Low
ASC-coordinated AAS [2]	Required	Centralized	Medium	No	Medium
Single-PR AAS [25], [26]	No additional	Centralized	High	No	Low
VZSG/PEC [28]	No additional	Distributed	High	Yes	High
Proposed multi-PR	No additional	Distributed	High	Yes	Medium

tributed arc suppression strategy maintains stable suppression performance under variations in fault resistance, fault location, and allocation coefficient. In addition to achieving reliable arc-suppression performance, the strategy enables precise and controllable capacity allocation among multiple PRs, thereby enhancing system-level operational flexibility and improving the utilization efficiency of distributed PR resources.

VI. DISCUSSION

To further clarify the engineering advantages and applicable scenarios of the proposed method, a qualitative comparison of different arc-suppression schemes is summarized in Table XI. Here, AAS denotes active arc suppression, ASC denotes arc-suppression coil, and PEC denotes power electronic converter. The proposed scheme is mainly intended for hybrid AC/DC distribution networks with multiple feeder-side PRs already installed. In practical PR design, a certain capacity margin is generally retained relative to the normal power-transfer requirement. The available current and apparent-power margins can be reused for arc suppression, while the compensation burden can be shared among different PRs.

As shown in Table XI, centralized AAS and ASC-coordinated AAS usually require dedicated arc-suppression equipment, while single-PR AAS concentrates the compensation burden on one device. In contrast, the proposed method distributes the compensation burden among the installed feeder-side PRs. Compared with the VZSG/PEC scheme, the proposed method adopts a voltage-current coordinated structure, where the CC-PRs provide preset zero-sequence current compensation and the VC-PR clamps the residual faulted-phase voltage. The control complexity is qualitatively assessed according to the number of participating devices, the requirement for inter-device communication or synchronization, and whether online compensation redistribution is involved. Since the PR roles and allocation coefficients are predetermined and no dedicated real-time inter-PR communication or online redistribution is required, the control complexity of the proposed method is classified as medium.

A quantitative comparison is further carried out under a representative SLG fault condition, as shown in Table XII, where the fault is located at F1 with $R_{\mathrm{f}} = 100\ \Omega$. Since the active compensation current in ASC-coordinated AAS depends on the ASC compensation state, the quantitative comparison focuses on centralized AAS, single-PR AAS, and the proposed multi-PR scheme. The capacity burden is evaluated by the equivalent apparent compensation capacity, and the maximum individual value is used for multi-device schemes. For the proposed scheme, the three PRs allocation of (0.4/0.4/0.2) is adopted, and the maximum individual compensation capacity is therefore determined by the coefficient of 0.4.

TABLE XII
QUANTITATIVE COMPARISON UNDER A REPRESENTATIVE SLG FAULT CONDITION

Scheme	$V_{\mathrm{f,res}}$/V	$I_{\mathrm{f,res}}$/A	Max individual S_{as}/kVA
Centralized AAS	21.9	0.22	205.0
Single-PR AAS	26.4	0.25	205.0
Proposed multi-PR	26.5	0.26	82.0

As shown in Table XII, all the compared schemes achieve effective residual-current and residual-voltage suppression under the tested condition. The proposed method does not reduce the total arc-suppression requirement determined by the network parameters and fault condition, but distributes the required compensation among multiple PRs, thereby reducing the maximum individual compensation capacity.

VII. CONCLUSION

This paper proposes a distributed arc suppression strategy based on the coordinated control of multiple PRs for distribution networks. To support this strategy, the operating mechanisms under steady-state asymmetric phase-to-ground parameters and SLG fault conditions are analyzed.

During the steady-state operation, the CC-PRs on individual feeders are utilized to execute AGPC, thereby correcting the zero-sequence unbalance caused by parameter asymmetry. Upon the occurrence of an SLG fault, the CC-PRs provide current-based fault-current compensation, while a single VC-PR performs voltage-based arc suppression to regulate the residual faulted-phase voltage. Compared with traditional centralized schemes, the proposed method guarantees normal AC/DC power transmission while simultaneously achieving steady-state unbalance compensation and fault arc suppression, which significantly enhances the operational utilization rate of the power electronic equipment.

Furthermore, by establishing a multi-device capacity analysis model, the capacity occupation mechanisms and allocation principles of different PRs are clarified. This strategy shifts the arc suppression burden from a centralized configuration to distributed devices, avoiding the excessive capacity requirements on a single PR, ultimately improving both the equipment utilization efficiency and the overall economic viability of the system.

References

[1] X. Wei, X. Wang, J. Gao, D. Yang, K. Wei, and L. Guo, "Faulty feeder detection for single-phase-to-ground fault in distribution networks based on transient energy and cosine similarity," *IEEE Trans. Power Del.*, vol. 37, no. 5, pp. 3968–3979, Oct. 2022.

[2] W. S. P. Fernando and M. A. Mahmud, "A nonlinear discrete-time backstepping model predictive controller design for active arc suppression coils in compensated power systems to mitigate powerline bushfire hazards," *IEEE Trans. Ind. Electron.*, vol. 71, no. 11, pp. 15077–15088, Nov. 2024.

[3] J. Lai, X. Yin, X. Yin, Z. Ullah, L. Jiang, and Z. Wang, "Improved comprehensive control of modular multilevel converter under AC/DC grid faults and harmonic operation conditions," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6537–6556, Jun. 2021.

[4] B. Liu, C. Wang, X. Zeng, L. Cui, and Z. Wan, "Single line-to-ground fault protection method considering three phase-to-ground parameters asymmetry in active flexible grounding systems," *IEEE Trans. Power Del.*, vol. 39, no. 4, pp. 2207–2218, Aug. 2024.

[5] W. Wang, X. Gao, B. Fan, X. Zeng, and G. Yao, "Faulty phase detection method under single-line-to-ground fault considering distributed parameters asymmetry and line impedance in distribution networks," *IEEE Trans. Power Del.*, vol. 37, no. 3, pp. 1513–1522, Jun. 2022.

[6] B. Fan *et al.*, "Principle and control design of a novel hybrid arc suppression device in distribution networks," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 41–51, Jan. 2022.

[7] X. Luan, X. Li, S. Wu, C. Jia, H. Mei, and L. Gao, "Arc suppression control with adaptive parameters of active grounding device considering ground fault resistance uncertainty," *IEEE Trans. Power Del.*, vol. 39, no. 1, pp. 426–435, Feb. 2024.

[8] W. Wang, X. Zeng, L. Yan, X. Xu, and J. M. Guerrero, "Principle and control design of active ground-fault arc suppression device for full compensation of ground current," *IEEE Trans. Ind. Electron.*, vol. 64, no. 6, pp. 4561–4570, Jun. 2017.

[9] G. Zhao, M. Guo, B. Zhang, Z. Zheng, and X. Zeng, "Flexible arc suppression method using cascaded H-bridge converters with adaptive voltage drop compensation," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 13, no. 4, pp. 5188–5200, Aug. 2025.

[10] G.-J. Zhao, M.-F. Guo, B.-L. Zhang, Z.-Y. Zheng, and Q. Hong, "A flexible arc suppression method for single-line-to-ground faults adaptive to transition resistance variations using cascaded H-bridge converters," *IEEE Trans. Ind. Electron.*, vol. 73, no. 7, pp. 9545–9556, Jul. 2026.

[11] G. Zhao, M. Guo, B. Zhang, Z. Zheng, and Q. Hong, "Cascaded H-bridge converter-based flexible arc suppression method adapting to line parameter variations," *IEEE Trans. Power Electron.*, vol. 40, no. 8, pp. 11809–11819, Aug. 2025.

[12] Y. Hou *et al.*, "Adaptive active voltage-type arc suppression strategy considering the influence of line parameters in active distribution network," *IEEE Trans. Ind. Electron.*, vol. 70, no. 5, pp. 4799–4808, May 2023.

[13] M. Guo, C. Han, Q. Ke, J. You, Z. Wang, and X. Zeng, "Voltage-current sliding mode control strategy for three-phase four-bridge-arm active converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 14, no. 1, pp. 1085–1096, Feb. 2026.

[14] Z. Huang *et al.*, "A multifunctional arc suppression device based on hybrid grid-connected converters," *IEEE Trans. Ind. Electron.*, vol. 72, no. 8, pp. 8174–8183, Aug. 2025.

[15] Z. Huang *et al.*, "Hybrid multifunctional arc suppression inverter with its steady and transient state operation optimization method," *IEEE Trans. Power Electron.*, vol. 40, no. 8, pp. 10313–10323, Aug. 2025.

[16] A. Dávila, T. Komrska, A. Arias, J. A. Cortajarena, E. Planas Fullaondo, and Z. Peroutka, "Four-leg voltage source converter with independent phase control for ground fault compensation," *IEEE Trans. Power Del.*, vol. 41, no. 2, pp. 789–800, Apr. 2026.

[17] Y. Hou *et al.*, "A review of single-phase-to-ground fault regulation devices for distribution networks," *Renew. Sustain. Energy Rev.*, vol. 200, Art. no. 114602, Aug. 2024.

[18] K. Liu *et al.*, "Flexible grounding system for single-phase to ground faults in distribution networks: A systematic review of developments," *IEEE Trans. Power Del.*, vol. 37, no. 3, pp. 1640–1649, Jun. 2022.

[19] Z. Li, Y. Pei, J. Liu, L. Wang, and Z. Leng, "Design and optimization of the MMC-based power electronic transformer considering ripple power transfer," *IEEE Trans. Power Electron.*, vol. 40, no. 4, pp. 5352–5370, Apr. 2025.

[20] X. Zhu, J. Hou, L. Liu, B. Zhang, and Y. Wu, "A modular multiport DC power electronic transformer based on triple-active-bridge for multiple distributed DC units," *IEEE Trans. Power Electron.*, vol. 39, no. 11, pp. 15191–15205, Nov. 2024.

[21] X. Zhu, J. Hou, and B. Zhang, "A multiport power electronic transformer with MVDC integration interface for multiple DC units," *IEEE Trans. Ind. Electron.*, vol. 71, no. 9, pp. 10704–10715, Sep. 2024.

[22] Y. Li, X. Pei, M. Yang, X. Lin, and Z. Li, "An advanced fault control of transformerless modular multilevel converters in AC/DC hybrid distribution networks under the single-phase grounding fault," *IEEE Trans. Power Del.*, vol. 36, no. 2, pp. 932–942, Apr. 2021.

[23] M. Wong, M. Xiao, F. Ma, and L. Wang, "Reliability evaluation of pilot virtual-mesh FREEDMSs by SST series and three-port power hub parallel energy routers," *IEEE Trans. Smart Grid*, vol. 15, no. 4, pp. 3418–3431, Jul. 2024.

[24] R. Xu, Z. Chang, G. Song, K. Jia, and J. Yang, "Fault isolation and arc suppression for single-line-to-ground faults in transformer-less SOP-based flexible interconnected distribution networks," *J. Mod. Power Syst. Clean Energy*, vol. 13, no. 6, pp. 2120–2130, Nov. 2025.

[25] L. Jiang *et al.*, "Flexible voltage arc suppression in distribution networks considering asymmetric ground parameters based on power router," *IEEE Trans. Ind. Electron.*, vol. 72, no. 12, pp. 14116–14127, Dec. 2025.

[26] J. Lai *et al.*, "Principle and implementation of active ground fault arc suppression based on hybrid MMC in AC/DC distribution network," *IEEE Trans. Power Del.*, vol. 40, no. 5, pp. 2503–2519, Oct. 2025.

[27] L. Jiang *et al.*, "A novel voltage arc suppression method for single-phase grounding fault in distribution network based on power router," *Electr. Power Syst. Res.*, vol. 231, Jun. 2024, Art. no. 110369.

[28] B. Zhang, M. Guo, M. Lak, C. Lin, and Q. Hong, "Theory and method of distributed virtual zero-sequence synchronous generators for cooperative fault arc suppression in active distribution networks," *IEEE Trans. Ind. Electron.*, vol. 73, no. 1, pp. 631–645, Jan. 2026.

[29] K. Yu, S. Liu, X. Zeng, H. Peng, F. Liu, and Z. Wang, "A novel insulation parameter online measuring technique based on two voltage transformers for distribution networks," *IEEE Trans. Power Del.*, vol. 36, no. 6, pp. 3383–3392, Dec. 2021.

[30] M. Guo, Y. Jiao, Z. Zheng, B. Zhang, J. Lin, and Q. Hong, "Online split-phase identification of asymmetric parameters between distribution lines and ground for unbalanced voltage compensation based on power electronics," *IEEE Trans. Power Electron.*, vol. 39, no. 8, pp. 10067–10078, Aug. 2024.

[31] B.-L. Zhang, M.-F. Guo, C.-M. Lin, M. Lak, S. Solemanifard, and Q. Hong, "Fault arc suppression method with elimination of line voltage drop influence for flexible distribution networks connected via power electronics," *IEEE Trans. Ind. Electron.*, vol. 73, no. 5, pp. 7133–7144, May 2026.

[32] S. Y. M. Mousavi, A. Jalilian, M. Savaghebi, and J. M. Guerrero, "Autonomous control of current- and voltage-controlled DG interface inverters for reactive power sharing and harmonics compensation in islanded microgrids," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9375–9386, Nov. 2018.

[33] *IEEE Guide for the Application of Neutral Grounding in Electrical Utility Systems—Part IV: Distribution*, IEEE Std C62.92.4-2014, 2015.

[34] *Code for Design of Overvoltage Protection and Insulation Coordination for AC Electrical Installations*, GB/T 50064-2014, 2014 (in Chinese).

[35] X. Zeng, C. Zhuo, K. Yu, G. Xiang, J. Li, and H. Zou, "A novel method of faults arc extinguishing and feeder protection based on voltage regulating intervention with grounding transformer winding taps for distribution networks," *Proc. CSEE*, vol. 40, no. 5, pp. 1523–1534, Mar. 2020 (in Chinese).

[36] H. Yao and M. Cao, *Power System Resonance Grounding Theory*, 2nd ed. Beijing, China: China Electric Power Press, 2009, pp. 40–45 (in Chinese).

Jinmu Lai (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2014, 2017, and 2020, respectively. From 2021 to 2026, he was a Lecturer/Associate Professor with Zhengzhou University, Zhengzhou, China. From 2025 to 2026, he was a Research Associate with Cardiff University, Cardiff, U.K. He is currently an Associate Professor with the School of New Energy and Electrical Engineering, Wuhan University of Technology, Wuhan, China. His research interests include power routers, power quality control, and the application of power electronics in power systems.

Zhu Li was born in Shangqiu, China, in 2001. He received the B.S. degree in Xi'an Polytechnic University, Xi'an, China, in 2024. He is currently working toward the M.S. degree in electrical engineering with Zhengzhou University, Zhengzhou, China. His research interests include power router and the application of power electronics in power systems.

Junhong Chen was born in Xinxiang, China, in 2001. He received the B.S. degree in electrical engineering from Northeast Electric Power University, Jilin, China, in 2023. He is currently working toward the M.S. degree in electrical engineering with Zhengzhou University, Zhengzhou, China.

His research interests include energy router, power quality control, and the application of power electronics in power systems.

Jun Liang (Fellow, IEEE) received the B.S. degree from Huazhong University of Science and Technology, Wuhan, China, in 1992, and the M.S. and Ph.D. degrees from China Electric Power Research Institute (CEPRI), Beijing, China in 1995 and 1998, respectively, all in electric power system and its automation.

From 1998 to 2001, he was a Senior Engineer with CEPRI. From 2001 to 2005, he was a Research Associate with Imperial College London, London, U.K. From 2005 to 2007, he was with the University of Glamorgan as a Senior Lecturer. Currently, he is a Professor in power electronics with the School of Engineering, Cardiff University, Cardiff, U.K. He is the Coordinator and Scientist-in-Charge of two European Commission Marie-Curie Action ITN/ETN projects: MEDOW (e3.9M) and InnoDC (e3.9M). His research interests include high voltage direct current (HVDC), medium voltage direct current (MVDC), flexible AC transmission system (FACTS), power system stability control, power electronics, and renewable power generation.

Prof. Liang is a fellow of the Institute of Electrical and Electronics Engineers (IEEE) and Institution of Engineering and Technology (IET). He is the Chair of IEEE U.K. and Ireland Power Electronics Chapter. He is an Editorial Board Member of CSEE JPES. He is an Editor of the IEEE TRANSACTIONS ON SUSTAINABLE ENERGY.

Jinrui Tang (Senior Member, IEEE) received the B.S. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2009, and the Ph.D. degree in electrical engineering from the School of Electrical and Electronics Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2014. He is currently an Associate Professor with the School of Automation, Wuhan University of Technology, Wuhan. His research interests include power system protection and control.

Fan Xiao (Member, IEEE) received Ph.D. degree in Electrical Engineering from the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, Wuhan, in 2016. From 2018 to 2023, he was a Senior Engineer with the State Grid Corporation of China. He is currently an Associate Professor with the School of New Energy and Electrical Engineering, Wuhan University of Technology, Wuhan, China. His current research interests include control and protection of HVDC systems, and relay protection for power systems.

Xin Yin (Member, IEEE) received the B.Eng. degree in electronic engineering from the University of Sheffield, Sheffield, U.K., in 2008, and the M.Sc. degree in telecommunication from University College London, London, U.K., in 2009, and the Ph.D. degree in electrical and electronic engineering from the University of Manchester, Manchester, U.K., in 2016.

He is currently a Professor with the School of New Energy and Electrical Engineering, Wuhan University of Technology, Wuhan, China. His research interests include the protection and control of the distribution grid with renewable resources and hybrid power electronic transformer.